A fully digital feedback control of gate driver for current balancing of parallel connected power devices

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A fully digital feedback control of gate driver for current balancing of parallel connected power devices

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Abstract

Parallel connected power devices such as Insulated Gate Bipolar Transistors (IGBTs) can be used to realize a system with higher current and higher power rating. However, the operation of parallel connected IGBTs is prone to unbalancing due to variation in parameters of the semiconductor devices and asymmetric parallel system. In this paper, feedback control is proposed for peak overshoot minimization as well as current balancing of parallel connected IGBTs. A fully digital feedback control (DFC) is implemented using the universal clock for balanced operation of the two parallel connected IGBTs.

1. Introduction

High power conversion and control requiring power devices with high enough voltage-current rating for power electronic converters. In order to achieve high power converter rating, devices can be connected in parallel-series to attain high voltage-current ratings. Current higher than a few kA is required for a given application with a specified voltage rating of the system. State-of-the-art devices cannot meet such requirement and a single IGBT module can supply a maximum current of few kA. Parallel connection of IGBTs is a way to match the desired current as well as the power rating. The system reliability and cost-per-ampere ratio also improved through parallelism of IGBTs **[1].**

Nevertheless, the operation of parallel connected IGBTs leads to unbalancing: uneven switching and uneven steady state characteristics (unbalanced dynamic and static current sharing) of devices **[2]**. In turn results in diminished and de-rated performance. The unbalanced behavior may cause the device operation out of the safe operating area (SOA) and subsequently, it may lead to the issue of device reliability as well as system reliability. Minimization of the IGBT current peak and current balancing through gate driver control is a possible way to avoid such problems up to an extent.

Previous works have focused on gate driver

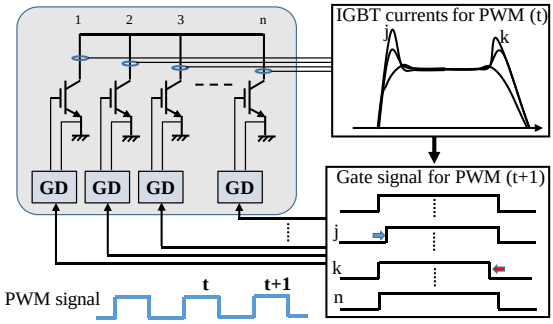

Fig.1. Feedback control for peak overshoot and current balancing of parallel connected power devices.

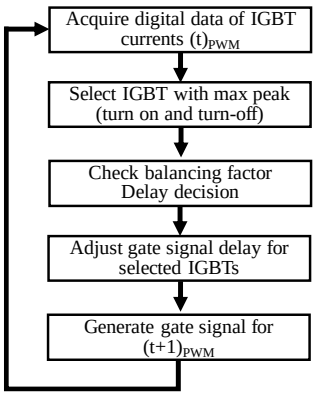

Fig. 2. Flow-chart of proposed feedback control.

control for optimizing the switching characteristics of a single IGBT **[3,4,5,6].** However, it does not automatically guarantee the balanced operation for parallel connected devices due to asymmetrical system and variation in a parameter of devices **[1,7]**.

The active gate control strategies **[7-8]** are proposed for IGBTs connected in parallel based on the rising and falling edges of current. The analog signal processing circuitry is used in **[7-8]** to detect the current edges for the control action and achieve the balanced current sharing. In **[7],** the communication among the control units is essential for decentralized control action. Moreover, the delays are adjusted considering a defined set of four delay values for the case of four IGBTs. The IGBTs are subtle to change in the parameter, therefore, the gradual adjustment in delays should have to be preferred concerning system stability. Also, the unavoidable delay caused by asynchronous FPGAs clocks of the decentralized control is also a concern.

In **[8],** DSP-FPGA board used for the control action: FPGA board computes the rise and fall time and the active gate control action is implemented in DSP board. The active gate control comprises of rise and fall time control and peak current control. The gate signals switching times are controlled using rising and falling edges of currents, and termed as rise and fall time control. And, the monitoring of current balancing using peak amplitude of the currents is termed as peak current control.

In general, most of the active gate control strategies for parallel connected devices are extensively focused on the current imbalance from the uneven current sharing point of view. The uneven current sharing lead to the thermal de-rating of the devices **[9].** Although, the currents may become almost evenly shared, that eventually cannot ensure the peak overshoot minimization of current for individual IGBTs. The overshoot in device current during switching is also a point of concern of imbalance and can lead to the SOA de-rating **[9].**

The peak overshoot minimization of the individual devices as well as even current sharing is required to improve the SOA de-rating as well as the thermal de-rating respectively. The improvement in SOA de-rating and thermal de-rating consequently approach towards the better device as well as system reliability.

The peak overshoot minimization and current balancing are the problems that need to be addressed simultaneously to enhance overall system performance. In this paper, a general concept of

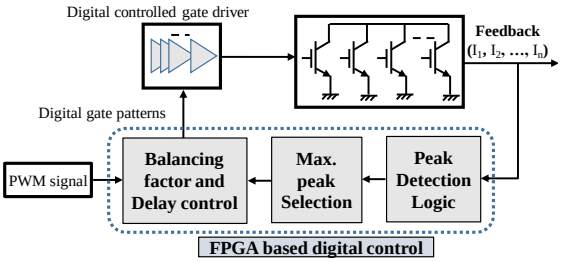

Fig.3 Block diagram of digital feedback control (DFC).

feedback control based on peak detection and minimization, for current balancing of parallel connected IGBTs, is presented. A fully digital feedback control of gate driver (DFC-GD) for two parallel connected IGBTs is implemented to demonstrate the current balancing. The unit step of 10ns is used for delay adjustment. The DFC is modeled in realistic digital design simulator and implemented using Field Programmable Gate Array (FPGA) providing a universal clock for controlled operation of parallel connected IGBT.

The organization of the paper is as follows: **Section II** digital feedback control, general operating principle and implementation for two parallel connected IGBT. **Section III** the description of signal processing through ADC to feed the signal to FPGA, implementation of a noise filter and peak detection of the signal inside FPGA. **Section IV** Experimental system implementation and results are explained and the conclusion is presented in **Section V**.

2. Digital feedback control

2.1. General Operating Principle

The feedback control algorithm (see in Fig.1 and Fig.2) is represented for n parallel connected IGBTs. The general operating principle for the development of the DFC (see in Fig.3) is based on the peak detection during turn-on and turn-off. Sampled digital data of IGBTs current are acquired corresponding to each pulse width modulated (PWM) signal sequence and used for the peak detection. The IGBT having maximum peak current during on-off switching is selected for control of turn-on and turn-off time.

At next step, a delay decision is executed corresponding to balancing factor criteria. According to the delay decision, the delay is adjusted to control the turn on and turn off time of gate signal to achieve peak overshoot minimization and even sharing of current. This feedback control can is defined as

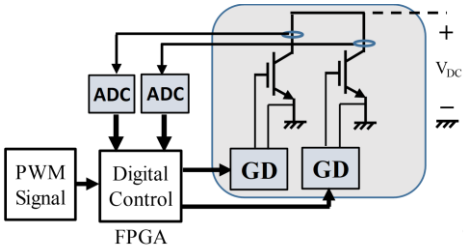

Fig.4 DFC system of two parallel connected IGBTs.

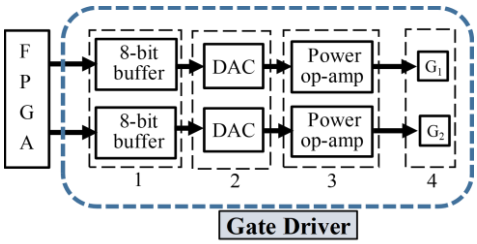

Fig.5 Block diagram of digital controlled GD board.

overshoot and balancing control (OBC).

2.2. DFC for two parallel connected IGBTs

The DFC system (see in Fig.4) is considered to implement for two parallel connected IGBTs and drive IGBT through digital controlled GD board (see in Fig.5) having two gate driving units. The DFC implemented in FPGA is represented through block diagram (see in Fig.6). The measured currents are fed to FPGA through ADC. The digital signal fed to FPGA is passed through the median filter and further peak tracking logic is applied to detect the peak corresponding to each IGBT current. The amplitude of the peak value is stored in RAM.

The peak current is used to control the turn-on and turn-off time individually for each gate drivers. The devices with maximum and minimum peak current are selected among all the devices. And, IGBT with maximum peak current monitored by the balancing factor introduced in this paper. The balancing factor for the parallel connected IGBTs is defined as

$$Balancing\ factor = I_{max}(t) - I_{max}(t\text{-}1) \quad (1)$$

The balancing factor and max-min selection criterion will generate a trigger signal to the counter. The counter increases the count by one unit and this is applied to the select line of the multiplexer. The desired delays are selected and incorporated into the

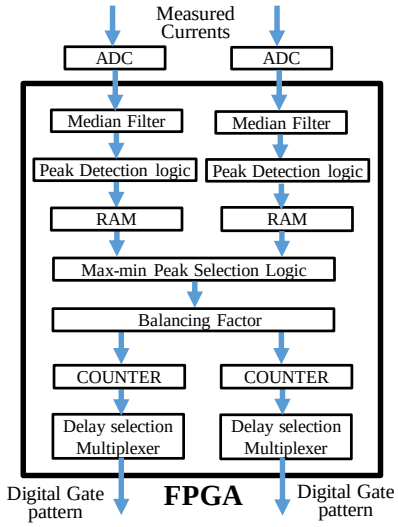

Fig.6 DFC implementation in FPGA for two parallel connected IGBTs.

gate signal for the next PWM switching sequence. Tolerance band can be added to balancing factor to avoid undesired delay activation in gate signal pattern.

3. Feedback signal

3.1. Analog to Digital Converter (ADC)

The AD conversion of feedback signal is required for implementation of the DFC by feeding the signal to digital controller. The sampling rate for AD conversion is crucial to satisfy sampling criteria as well as to capture the rapidly varying feedback signal. In this case, the sampling frequency of the ADC is adopted to capture the dynamic characteristic of IGBT currents significantly considering the fundamental clock frequency of FPGA.

The DFC (see in Fig.4) comprises of ADC to process IGBT current as a feedback signal. The IGBTs currents are measured using Pearson current probe and fed to ADC (Texas Instruments ADC08L060). This 8bit parallel ADC can operate at a sampling frequency of 10MHz min to 60MHz max. In addition, the internal circuitry of ADC is having an inbuilt coarse comparator, error correction, and sample-hold functions that minimize the possibility of error in the conversion.

A small printed circuit ADC board is developed for interconnection to FPGA. The supply voltage of 3.3V and sampling clock are provided from FPGA for functioning of ADC. The sampling clock of 50MHz

is generated using the fundamental FPGA clock of 100MHz.

3.2. Noise Filter

Noise as an unwanted signal can affect the output of AD converter that results in a distorted signal. It is crucial to retrieve the signal through noise reduction for further processing. The filter is designed based on the noise problem of the signal by analyzing the data. In this case, the unwanted peaks at zero crossing are affecting the signal.

The median filter is implemented for removal of the unwanted peak noise. The median filter is a non-linear filter that selects the median data out of the considered number of samples. The number of samples is defined as a window. The median is middle value for a window size of the odd number. The median filter for a window of 3 and 5 is designed and satisfactory outputs are obtained for both the cases. Finally, the window of 5 sampled data (see in Fig.7) is adopted for safe and stable operation.

3.3. Peak Detection

The detection of the current peak overshoot is core of the concept presented in this paper to implement DFC and achieve OBC for parallel connected IGBTs currents. The 8bit digital output of measured IGBTs currents utilized for peak detection. The peak detection logic is designed for digital implementation. And, additional mathematical constraints are included to track the peak appropriately. In addition, the detected peak value is stored in RAM and compared to next peak value to avoid local extrema trap (avoid false detection) during each switching sequence of PWM signal. The stored data reset to zero corresponding to next on/off sequence of PWM signal.

The magnitude of IGBT current is measured and fed to the FPGA through ADC. Also, the peak value of current and corresponding IGBT is detected to minimize and monitor the peak current overshoot. The real-time peak current monitoring can ensure the protection in case of overcurrent caused by overloading and short-circuiting. In addition, to protect from the special case of overcurrent that can occur in parallel connected IGBTs system due to unbalancing. The response time for overcurrent protection is required in few µs/hundreds of ns. The digital control system can respond to the overcurrent event promptly and satisfy the response time

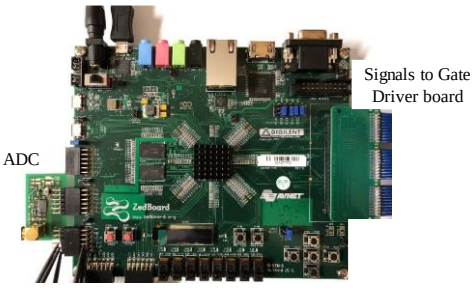

Fig.7 FPGA with ADC to generate gate signals output.

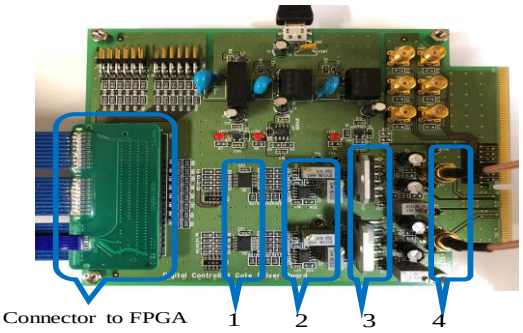

Fig.8 Developed digital controlled GD board.

condition because of high fundamental clock frequency based operation lead to significantly high-speed response.

4. Experimental results and validation

4.1. Experimental System

The experimental system set-up is developed for the digital feedback control of two parallel connected IGBT system. The experimental system consists of FPGA with ADC (see in Fig.7), digital controlled GD board (see in Fig.8), and a power circuit (see in Fig.9). The power circuit consisting of TO-247 (IRG7PH46U) IGBTs of International Rectifier, discharging the capacitor, dc bus, and load. Pearson Current sensor 8105-03 (see in Fig.9) used for measurement of IGBT current and it is usable for a rise time of as fast as of 10ns.

The DFC is modeled in realistic digital design simulator: Xilinx system generator (XSG) to program FPGA and generate controlled digital gate patterns. The digital controlled GD board converts generated 8bit digital patterns into gate voltage signal for controlled operation of two parallel connected IGBTs. The digital controlled GD board (see in Fig.8) is also

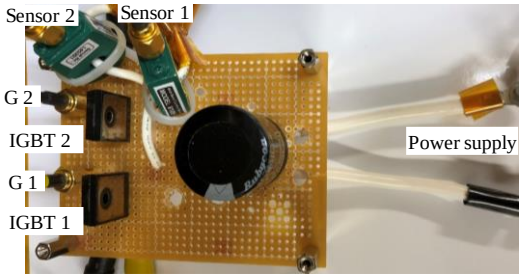

Fig.9 Two parallel connected discrete IGBTs.

capable of controlling and adjusting gate voltage digitally corresponding to digital gate patterns with the resolution of 300mV.

The output stage power op-amp of digitally controlled gate driver board is the governing factor for the maximum operating frequency range that is the bandwidth of feedback control. The power bandwidth of the op-amp is 55kHz (typical). Moreover, there are power op-amps with higher power bandwidth (more than 1MHz) that can be further used to improve the overall bandwidth of the feedback control for high switching frequency application.

4.2. Validation

The operation of parallel connected discrete IGBTs was performed with and without DFC-GD. And, the current sharing of IGBTs was measured to demonstrate the performance. For the case when DFC-GD was not employed, overshoot occurred in an IGBT current (see in Fig.10) during turn-on due to asynchronous switching due to unbalanced system behavior. And, the asynchronous switching is not controlled for the parallel operation without DFC-GD.

The parallel operation with DFC-GD enables the system to control asynchronous switching by compensating gate delays of corresponding IGBTs. DFC-GD minimizes the overshoot (see in Fig.11) and consequently resulted in almost balanced dynamic as well as steady state current sharing. The overshoot, as well as current sharing, is improved through activated and adjusted delays in digital gate patterns for the IGBT having overshoot. The delay in digital patterns corresponding to balancing factor resulted in balanced current sharing for delay of 250ns during turn-on.

The rapid and random change in gate delay can easily result in system instability. The delay compensation with unit step delay resolution of 10ns is employed to ensure system stability considering one of the crucial concern. The trade-off between a

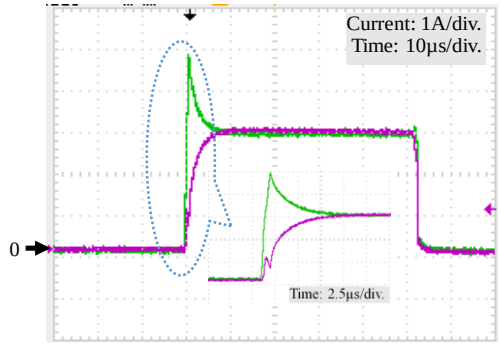

Fig.10. IGBT currents without DFC-GD.

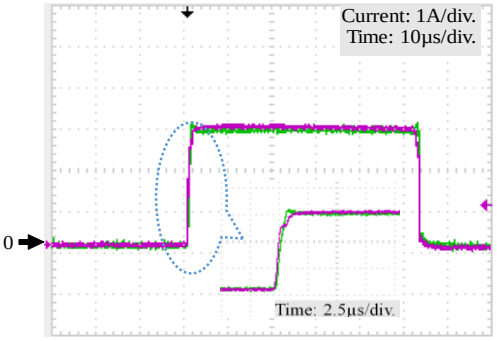

Fig.11. IGBT currents with DFC-GD.

unit step change in gate delay and number of cycles needed to achieve balanced operation is essential considering rapid current balancing and overall system stability. This can be further improved through optimization methods.

5. Conclusions

In this paper, the peak detection based DFC-GD is implemented for balanced dynamic current sharing of parallel connected IGBTs. Digital controlled GD board has been developed and DFC is validated experimentally for two parallel connected IGBTs. As demonstrated, the peak overshoot current of IGBT is minimized, as well as, DFC-GD is able to balance the dynamic current sharing by adjusting switching times of the digital gate patterns for unbalancing occurred during turn-on.

The peak minimization concept based DFC-GD require detection of peak only and capable of serving both the purposes: peak overshoot minimization of individual IGBT and current balancing. The system was operated using the universal clock to avoid undesired delay addition.

Acknowledgments

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