The Readout System for the ITk Pixel Demonstrator for the ATLAS High-Luminosity Upgrade

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Abstract

The upgrade of the Large Hadron Collider to the High Luminosity Large Hadron Collider starting in 2024 will allow the experiments to collect approximately ten times more data for precision measurements of Standard Model processes and searches for new physics. The increase in luminosity poses challenges in terms of radiation hardness and detector readout. The ATLAS experiment will replace the current tracking detector with the new Inner Tracker (ITk) to cope with these challenges, which in particular includes the development of a new generation of readout chips.

The Outer Barrel Demonstrator is a prototype stave in the context of the ITk pixel upgrade, but is still equipped with the legacy readout chip. This thesis is focused on the readout of the Outer Barrel Demonstrator. A new readout scheme for the demonstrator is developed and implemented and extensive tests and measurements are performed on the demonstrator and presented here.

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Zusammenfassung

Der Ausbau des Large Hadron Colliders zum High Luminosity Large Hadron Collider beginnt 2024 und wird den Experimenten erlauben etwa zehn mal größere Datenmengen für Präzisionsmessungen von Standardmodell-Prozessen und der Suche nach neuer Physik zu nehmen. Dabei stellt die erhöhte Luminosität Herausforderungen an die Strahlenhärte und Detektorauslese. Dafür wird das ATLAS Experiment den aktuellen Spurdetektor durch den neuen Inner Tracker (ITk) ersetzen. Dies beinhaltet insbesondere die Entwicklung einer neuen Generation von Auslesechips.
Der Outer Barrel Demonstrator ist ein Stave-Prototyp für das ITk Pixel Upgrade, aber ist noch mit der bisherigen Generation von Auslesechips ausgestattet. Der Fokus dieser Arbeit liegt auf der Auslese des Outer Barrel Demonstrators. Ein neues Ausleseschema wird für den Demonstrator entwickelt und umgesetzt und ausgiebige Tests und Messungen am Demonstrator werden durchgeführt und hier vorgestellt.

Contents

CHAPTER 1

Introduction

The Standard Model of particle physics describes the known elementary particles and their interactions and is the most complete description of particle physics to date, which has been tested experimentally to a high degree of precision. Despite this success, the Standard Model can not explain all observations. The desire to complete the Standard Model and the search for new physics has driven the development of new high-energy and high-intensity particle accelerators over the last decades, leading to the discovery of the Higgs boson in 2012, which was the last missing particle in the Standard Model.

Chapter 2 introduces the Standard Model of particle physics and motivates the need for new particle accelerators and detectors. The currently largest and most powerful particle accelerator is the Large Hadron Collider at CERN, which houses several experiments including the ATLAS detector. The ATLAS detector uses a wide range of technologies to measure the properties of particles such as trajectory, energy, and momentum. One important type of particle detectors is the semiconductor pixel detector, which is covered in Chapter 3.

The upgrade of the Large Hadron Collider to the High Luminosity Large Hadron Collider starting 2024 will increase the luminosity significantly and enable the experiments to collect more data for precision measurements and searches for new physics. This is a challenge especially for the pixel detector close to the interaction point, as it increases the particle flux which leads to more radiation damage as well as higher hit rates on the detector elements. Current and future upgrades of the ATLAS pixel detector are described in Chapter 4, which also introduces the current and next generation of frontend readout chips designed to cope with the high data rates.

Prototypes for the upgrade of the ATLAS detector with a new tracking detector in the context of the high luminosity upgrade are under development. The Outer Barrel Demonstrator is a prototype stave of the new pixel detector and is used for prototyping and validation of the design and system integration. It is introduced in Chapter 5 and

the new readout scheme that is developed and implemented in the scope of this thesis to enable the readout of the demonstrator is described. The tests and measurements performed on the demonstrator for this thesis are covered in Chapter 6. This includes the validation of the new readout and a range of measurements on the modules of the demonstrator.

CHAPTER 2

The Large Hadron Collider and the ATLAS Experiment

This chapter is based on and contains sections from Ref. [1].

2.1. Overview

The *Large Hadron Collider* (LHC) is the world's largest and most powerful particle accelerator, designed for proton-proton collisions at a centre of mass energy up to 14 TeV and a peak luminosity of $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. While proton-proton collisions are the primary mode of operation, proton-ion or ion-ion collisions are also possible. It provides collisions to the four large experiments ALICE, ATLAS, CMS, and LHCb and is located at CERN inside the 27 km long tunnel previously occupied by LEP. ATLAS and CMS (Compact Muon Solenoid) are the two general-purpose detectors, which are used in a wide range of searches for new physics such as supersymmetry and extra dimensions. Their operation led to the discovery of the Higgs boson in 2012 [2, 3]. ALICE (A Large Ion Collider Experiment) is designed to study heavy-ion collisions and the quark-gluon plasma. LHCb (Large Hadron Collider beauty) investigates the decay of B-mesons and CP-violation.

In 2011, the LHC operated at a centre-of-mass energy of $\sqrt{s} = 7\,\mathrm{TeV}$ with ATLAS recording an integrated luminosity of about $5\,\mathrm{fb}^{-1}$. Operation resumed after the end-of-year shutdown in 2012 with increased energy of $\sqrt{s} = 8\,\mathrm{TeV}$ and approximately $20\,\mathrm{fb}^{-1}$ of data were recorded by ATLAS at the end of the run. February 2013 marked the beginning of the first long shutdown, necessary to enable proton-proton collisions at $\sqrt{s} = 13\,\mathrm{TeV}$ and to reach the design luminosity. This was accompanied by upgrades to the experiments to cope with the new running conditions. Approximately $140\,\mathrm{fb}^{-1}$ were recorded by ATLAS.

The second long shutdown is scheduled for 2019-2020 and will increase the peak luminosity to $2 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The third long shutdown starting in 2024 is dedicated to the *High Luminosity-LHC* (HL-LHC) upgrade, further increasing the luminosity to

$5–7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

2.2. Physics at the LHC

2.2.1. The Standard Model of Particle Physics

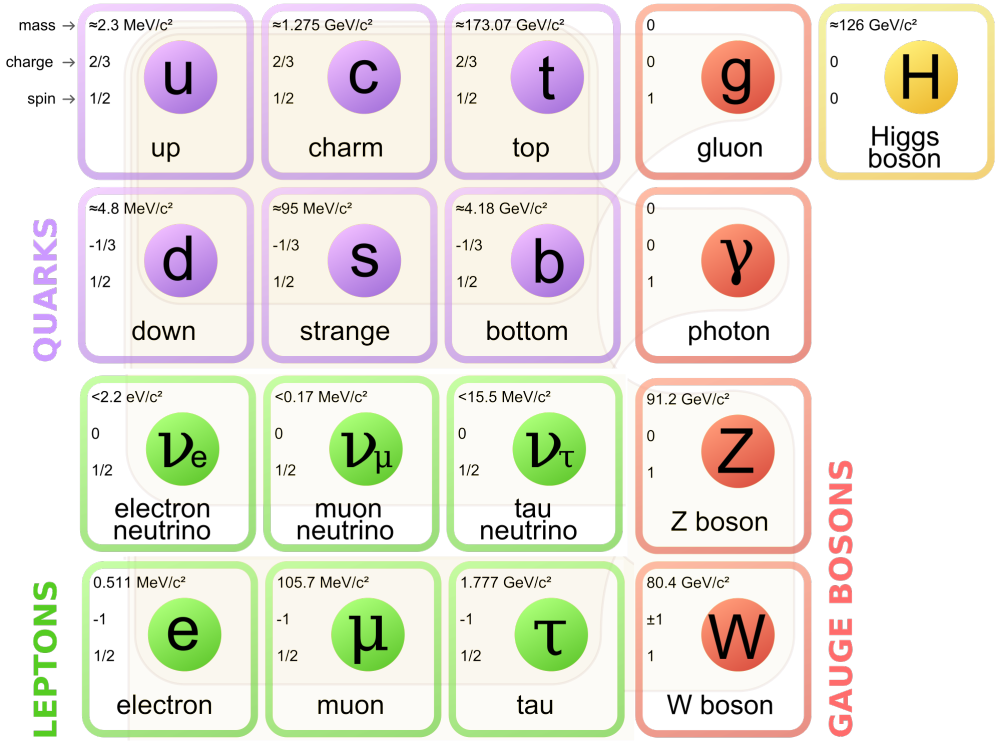


Figure 2.1.: The particles described by the Standard Model of Particle Physics.

The *Standard Model of Particle Physics* contains all known elementary particles and their interactions via the *electromagnetic interaction*, the *weak interaction*, and the *strong interaction*. Mathematically, the Standard Model is described as a quantum field theory with a local $SU(3)_c \times SU(2)_L \times U(1)_Y$ symmetry.

The Standard Model contains spin-$\frac{1}{2}$ particles, the *fermions*, and integer-spin particles, the *bosons* (see Figure 2.1). The fermions in turn are divided into the *leptons* and the *quarks*, which are arranged in three generations with two leptons and two quarks each. The first generation contains the lightest particles which therefore cannot decay and are stable. They are the constituents of ordinary matter. The masses increase with the generation, which makes the particles in the second and third generation unstable. The exception are the *neutrinos*, which are assumed to be massless in the Standard Model.

Leptons carry an electric charge of -1 or 0, quarks carry an electric charge of $^2/_3$ or $-^1/_3$ and are associated with a *colour charge* of *red*, *green*, or *blue*. To each particle

corresponds an antiparticle, which has the same mass as the particle but the opposite charges.

The interactions between particles are mediated by four spin-1 *gauge bosons*. The strong force is mediated by eight massless *gluons* (g), which differ in their colour charge and couple to all particles with colour charge, namely the quarks and the gluons themselves. The electromagnetic force is mediated by the massless *photon* (γ), which couples to all electrically charged particles. The massive *intermediate vector bosons*, the charged $W^{\pm}$ boson and the neutral Z boson, are the force carriers of the weak interaction. They couple to all fermions as well as to themselves. Since the $W^{\pm}$ boson is electrically charged, the photon also couples to it.

The Higgs boson is the only scalar spin-0 particle in the Standard Model, unlike the fermions and gauge bosons. It is an excitation of the Higgs field, which has a non-zero vacuum expectation value. By interacting with this field, the massive gauge bosons and fermions acquire their mass.

2.2.2. Limits of the Standard Model

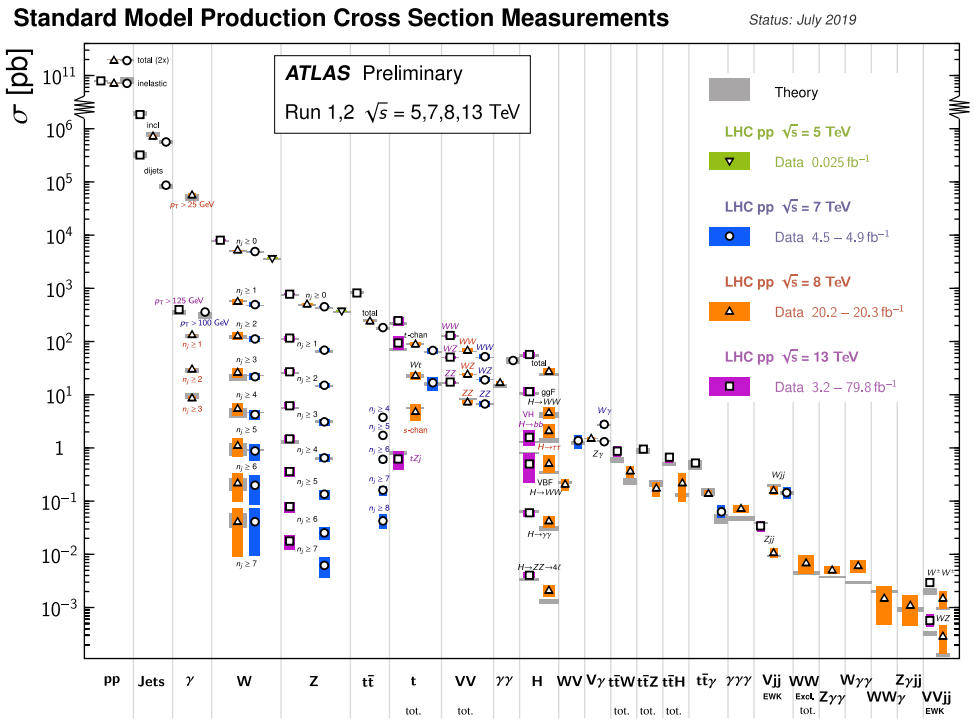


Figure 2.2.: Summary of several Standard Model cross section measurements compared to the corresponding theoretical expectations [4].

With the discovery of the Higgs boson, all particles in the Standard Model have been found. The Standard Model is very successful in the description of particle physics and

has made predictions that are in good agreement with experiments. An example is given in Figure 2.2, which summarises several Standard Model cross section measurements performed at ATLAS compared to the theoretical expectations.

Despite the good agreement between theory and experiment over many orders of magnitude, not all observations can be explained by the Standard Model alone, but indicate that it is incomplete and has to be extended. Also, gravity as one of the fundamental forces is not included. Many theories were proposed over the years, but ultimately, new experimental discoveries are necessary to select compatible theories. The search for physics beyond the standard model remains an ongoing effort at ATLAS and many other experiments.

Neutrino Oscillation and Neutrino Mass

In the 1960s the Homestake experiment measured the electron neutrino flux originating from the Sun, but measured only a fraction of the expected rate [5]. This discrepancy was later confirmed by other experiments, giving rise to the solar neutrino problem.

By assuming a small but non-zero mass, the neutrinos would be able to oscillate between different flavours, explaining the apparent disappearance of electron neutrinos. First evidence for oscillation of neutrinos was announced in 1998 by the Super-Kamiokande experiment in atmospheric neutrinos [6], and in 2002 the Sudbury Neutrino Observatory (SNO) published direct evidence for neutrino flavour transformations [7], measuring both the flux of electron neutrinos and the total flux.

The Standard Model can be extended to include neutrino masses and explain the oscillation with an additional mixing matrix, but it offers no explanation as to why the neutrinos have much smaller masses than the other leptons and quarks.

Dark Matter

Astronomical observations give evidence for the existence of dark matter, a stable form of matter that does not interact electromagnetically, making it invisible for astronomical instruments.

Already in 1933, observations of galaxies in the Coma cluster indicated that the visible matter of the galaxies is not sufficient to gravitationally bind the galaxies together [8]. Another indication for the existence of dark matter are galaxy rotation curves. The observed rotation curves of spiral galaxies [9] do not match the predictions assuming that only visible matter is present. For large radii, the rotational velocity does not decrease as would be expected from the decreasing density of visible matter, but stays roughly constant. This can also be accounted for by adding dark matter.

Measurements of anisotropies in the cosmic microwave background are an indirect method to calculate the dark matter density. Observations by WMAP and Planck give a content of about 5% baryonic matter and 26% dark matter in the universe [10, 11]. The rest is attributed to dark energy, which is also not part of the Standard Model.

The Standard Model has no suitable candidate for a particle that could make up dark matter, making the search for new particles beyond the standard model an active field

of research.

CP Violation

While the Standard Model allows for violation of the CP symmetry via the CKM matrix, the observed effect is not large enough to explain the matter-antimatter asymmetry in the universe. On the other hand, no CP violation is observed in the strong interaction [12], but the Standard Model offers no explanation as to why there is no CP violation in the strong interaction, as it is allowed by the theory.

This requires fine-tuning of parameters, which is often considered unnatural and is known as the Strong CP Problem. Some theories try to solve this problem by introducing new mechanisms which suppress CP violation in the strong interaction without fine-tuning.

2.3. CERN Accelerator Complex

The LHC is part of a large complex of particle accelerators at CERN. The LHC itself is unable to accelerate particles at rest, and instead a series of pre-accelerators is used to gradually increase the energy. Two beams revolve inside the LHC in opposite directions and are intersecting at the collision points where the detectors are housed.

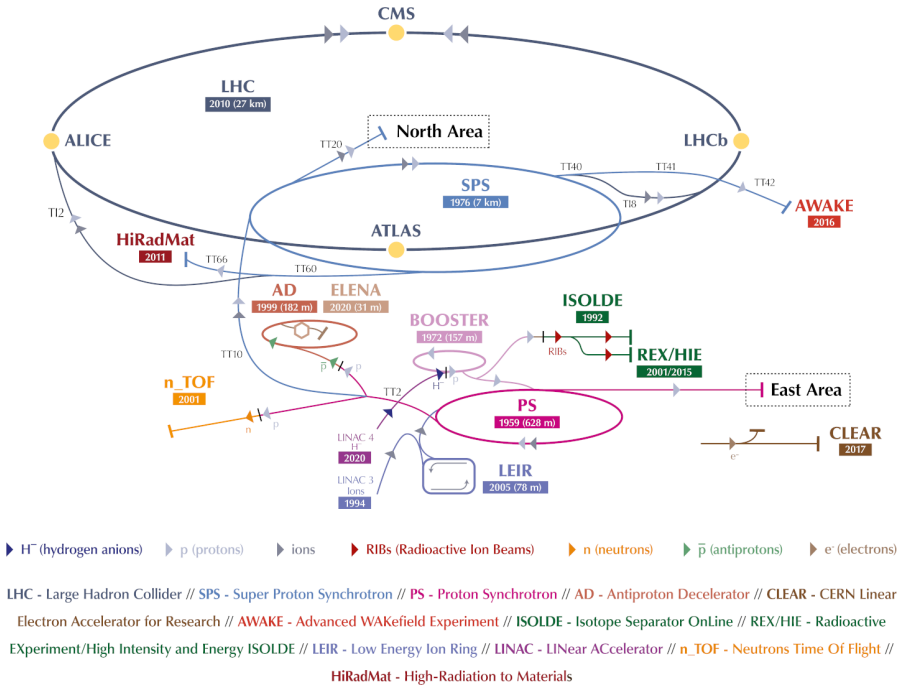


Figure 2.3.: CERN accelerator complex. Copyright and image credit: CERN.

Figure 2.3 shows an overview of the accelerators and connected experiments at CERN.

The colliders were constructed consecutively over many decades and often repurposed the existing accelerators as pre-accelerators.

Protons or heavy ions are injected into the complex with two linear accelerators. Up to the end of 2018, *Linac2* was used to accelerate protons, but it was then decommissioned in favour of the newly constructed *Linac4*, which accelerates negative hydrogen ions instead of bare protons which are then passed through a stripping foil to remove the electrons. Linac4 will help to increase the luminosity for the HL-LHC upgrade [13]. The protons are then injected into the *Proton Synchrotron Booster* and further accelerated, followed by the *Proton Synchrotron* (PS), the *Super Proton Synchrotron* (SPS), and finally the LHC. Heavy ions are accelerated with *Linac3* followed by the *Low Energy Ion Ring* (LEIR) and then also go into the PS. The beams are also used by other experiments and testbeam areas connected to the complex.

The LHC does not operate with a continuous beam, but the protons are grouped into bunches, packets of protons that collide in 25 ns intervals, the so called bunch crossing interval.

Assuming a Gaussian beam profile with a width of $\sigma_{x,y}$ and B bunches with $N_{1,2}$ particles per bunch, revolving at frequency f and colliding head-on, the luminosity is given by:

$$\mathcal{L} = \frac{BN_1N_2f}{4\pi\sigma_x\sigma_y}$$

The rate of a process with cross-section σ_p is

$$\frac{\mathrm{d}N}{\mathrm{d}t} = \sigma_p\mathcal{L}.$$

Because the cross sections of processes studied in today's experiments are very small, high luminosities are necessary to collect enough data in a reasonable amount of time.

The integrated luminosity

$$\mathcal{L}_{int} = \int \mathcal{L}\,\mathrm{d}t$$

is an indication for the amount of data collected and is directly related to the number of events $N = \sigma_p\mathcal{L}_{int}$. Maximising this quantity is therefore also the goal of upgrades to the LHC.

2.4. The ATLAS Detector

With 44 m length and 25 m diameter, ATLAS is the largest detector at the LHC. The requirements for the detector design are dictated by the physical processes that are of interest or could indicate new physics. This includes the mechanism of spontaneous electroweak symmetry-breaking and the Higgs boson in the Standard Model as well as Supersymmetric (SUSY) extensions, searches for SUSY particles, top-quark physics and B physics [14].

The basic design criteria of the detector include very good electromagnetic calorimetry and full-coverage hadronic calorimetry, accurate jet and missing transverse energy

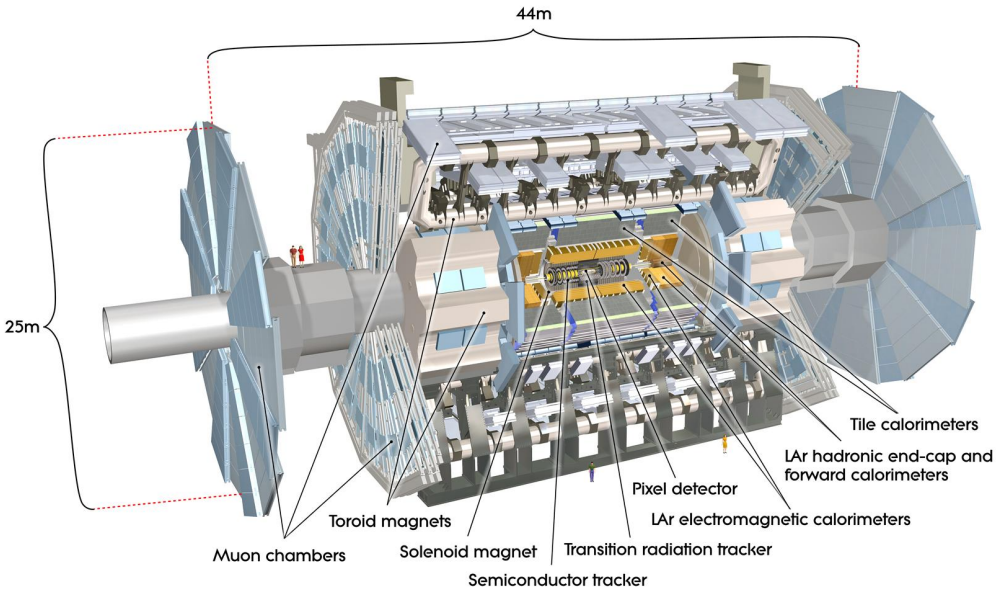


Figure 2.4.: Overview of the ATLAS detector. ATLAS Experiment © 2019 CERN.

measurements, high-precision muon momentum measurements, efficient tracking at high luminosity for high-p_T lepton-momentum measurements, electron and photon identification, τ-lepton and heavy-flavour identification and full event reconstruction capability at lower luminosity. Large acceptance in pseudorapidity with almost full azimuthal angle coverage as well as triggering and measurements of particles at low-p_T thresholds are also required.

The overall layout of the ATLAS detector is shown in Figure 2.4. The *Inner Detector* (ID) is the detector closest to the interaction point. It is surrounded by a thin superconducting solenoid, followed by the calorimeter system, which is enclosed by the toroid magnets and the Muon chambers [15].

2.4.1. Inner Detector

The *Inner Detector* is 7 m long and has a radius of 1.15 m. It contains three different detector technologies and is used for pattern recognition, momentum and vertex measurements and electron identification. Closest to the beam pipe is the *Pixel Detector*, followed by the *Semiconductor Tracker* (SCT) and the *Transition Radiation Tracker* (TRT). One quadrant of the Inner Detector is shown in Figure 2.5.

The *Pixel Detector* [16] consists of three barrel layers and two endcaps with three disks on each side (see Figure 2.6). It offers the highest granularity, as required for momentum and vertex measurements close to the interaction point. Typically, each track crosses three pixel layers, which is necessary to determine the transverse momentum from the

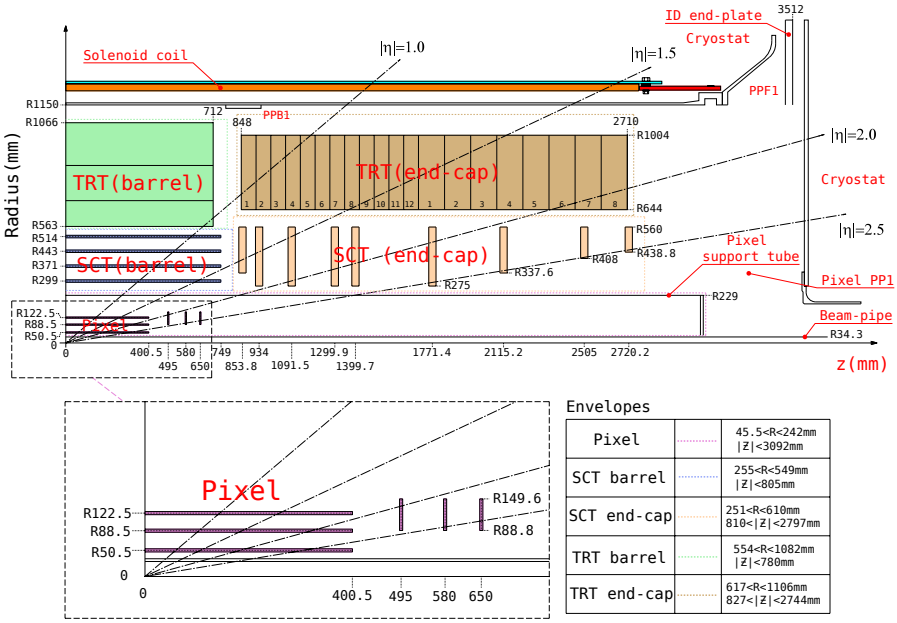


Figure 2.5.: Plan view of a quarter-section of the ATLAS inner detector. ATLAS Experiment © 2019 CERN.

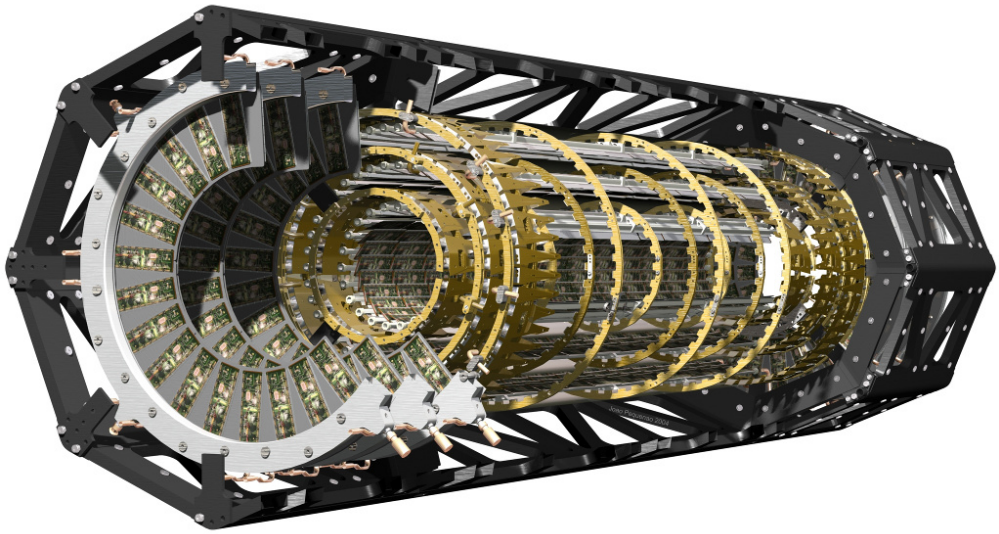


Figure 2.6.: The ATLAS pixel detector with three barrel layers and three disk layers at each end. ATLAS Experiment © 2019 CERN.

track. The detector contains identical pixel modules in the barrel and the disks. 1456 pixel modules are used in the barrel and 288 modules in the disks. Each module is composed of a silicon sensor with 47,232 pixels connected to 16 frontend chips (FE-I3) with 2880 pixel cells each. Also included is the *module control chip* (MCC) and a flexible printed circuit to route signals and power. The detector has an active area of about $1.7\,\mathrm{m}^2$.

The SCT [17] is arranged in four barrel layers and two endcaps of nine disks and is designed to provide eight measurements per track. The SCT uses single-sided p-on-n silicon microstrip detectors. Two detectors are glued together back-to-back at a 40 mrad angle to obtain measurements in the direction of the beam pipe.

The TRT is based on the use of proportional counters. The TRT consists of about 300,000 tubes (straws) filled with a gas mixture and containing a sense wire at the centre. The TRT barrel has three layers of 32 modules each, with the straws parallel to the beam. In the end-caps, they are arranged radially with a total of 224 layers of straws on each side. The layers are interleaved with the radiators. The straws are operated as drift tubes, while the radiators produce detectable X-rays when traversed by electrons. The detector can discriminate between tracking hits and transition-radiation hits, thus providing excellent electron identification.

2.4.2. Calorimeters

The ID is enclosed by the *electromagnetic calorimeter* and the *hadronic calorimeter*, which measure the energy of particles leaving the ID.

The electromagnetic calorimeter is a sampling calorimeter with lead absorbers and liquid argon. It has a thickness of over 22 radiation lengths in the barrel and over 24 radiation lengths in the end-caps [17].

The *hadronic calorimeter* consists of the hadronic barrel calorimeter, a sampling calorimeter with plastic scintillator tiles interleaved with iron absorbers, the hadronic end-cap calorimeter with copper and liquid argon, and the high density forward calorimeter with copper and tungsten absorbers and liquid argon. The hadronic calorimeter is thick enough to provide good containment for hadronic showers and to reduce punch-through into the muon system to a minimum.

2.4.3. Muon Spectrometer

The *Muon Spectrometer* uses the large barrel and two smaller end-cap toroid magnets to bend muon tracks and four different chamber technologies to measure them. In the barrel region, the chambers are arranged in three cylindrical layers around the beam axis. In the end-caps, the chambers are installed vertically, again in three layers. The track coordinates are measured by *Monitored Drift Tubes* (MDTs) and *Cathode Strip Chambers* (CSCs). The trigger system uses *Resistive Plate Chambers* (RPCs) in the barrel and *Thin Gap Chambers* (TGCs) in the end-cap regions.

2.4.4. Trigger System

The purpose of the trigger system is to reduce the rate of recorded events from the 40 MHz collision rate to a manageable rate of a few hundred events per second that can be written to storage. The trigger system consists of several levels, where each reduces the rate further [17].

The L1 trigger is hardware based and uses inputs from the calorimeter and the muon spectrometer to select events. It reduces the rate to about 75 kHz and provides a *Region of Interest* (RoI) to the next trigger level. The L2 trigger uses the full detector data inside the RoI for its decision and reduces the trigger rate to approximately 3.5 kHz. The last stage is performed by the *event filter*, which performs event reconstruction and reduces the rate to about 200 Hz.

2.5. LHC and ATLAS Detector Upgrades

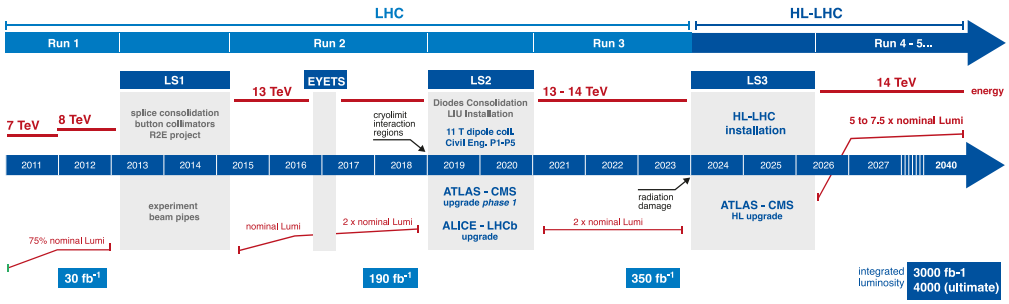


Figure 2.7.: LHC upgrade timeline.

Figure 2.7 shows a timeline of the LHC. Between the periods where the LHC is in operation and the experiments are collecting data are three longer shutdown periods dedicated to maintenance and upgrades of the accelerator and experiments.

Phase-0 Upgrade

The first long shutdown lasted from 2013 to the beginning of 2015 and splices between the superconducting magnets in the LHC were improved in response to the quench incident in 2008 [18]. This also allowed to increase the beam energy from 4 TeV to 6.5 TeV. The luminosity was increased to the nominal luminosity.

During the shutdown, the *Insertable B-Layer* (IBL) was inserted into the ATLAS inner detector. It is an additional pixel layer installed between the current inner pixel layer (B-layer) and a new beam-pipe. By adding an additional layer, the degrading tracking efficiency of the existing detector due to the higher luminosity, failing modules, and radiation damage can be compensated and the tracking precision is improved.

For the design of the IBL, several new constraints had to be taken into account. The smaller radius required development of a more radiation hard technology and placed

restrictions on the arrangement of modules and support structures. The IBL consists of 14 staves with 32 modules each, arranged around the beam pipe and tilted with a slight overlap. This gives full coverage in ϕ, but there is not enough space to overlap modules along z, which leaves gaps in z direction. The material in the IBL is reduced to almost half the radiation length of the existing B-layer, reaching 1.54% of X_0 [19]. Two sensor technologies are used in the modules: planar sensors with two front end chips and one sensor per module (2-chip module), or 3D sensors with a single chip and sensor (1-chip module). Planar sensors usually consist of a lowly doped substrate with highly doped implants on the surface, while the electrode structure of 3D sensors extends well into the substrate.

The FE-I3 front end chips used in the present detector do not have a sufficient hit rate capability and radiation hardness and the active fraction of the chip is too small to build a compact layer with high geometric acceptance. This led to the development of the FE-I4, which is described in more detail in Chapter 4.3.

The upgrade of the Inner Detector with the IBL is covered in more detail in Chapter 4.1.

Phase-I Upgrade

During the second long shutdown from 2019 to 2020, Linac2 will be replaced by Linac4 and several accelerators in the injector chain will be upgraded in preparation for the high luminosity upgrade. The LHC will operate at twice the nominal luminosity.

ATLAS will undergo several improvements to the detectors and trigger system. An upgrade of the muon system will replace the current muon tracking in the forward region (known as the *Small Wheels*), with a new set of tracking and trigger detectors, the *New Small Wheels* [20]. This will improve the tracking and trigger performance of the muon spectrometer, which would otherwise suffer from the higher background rates at higher luminosity.

The granularity of the liquid argon calorimeter is increased to improve the L1 trigger performance [21]. The trigger system is upgraded to take advantage of the improved liquid argon calorimeter, the New Small Wheels, and parts of the tile calorimeter [22]. This is accompanied by the new *Fast Tracker* (FTK), which provides tracking information to the L2 trigger.

Phase-II Upgrade

The third long shutdown is scheduled from 2024 to 2026 and will upgrade the LHC to the *High Luminosity-LHC* (HL-LHC), increasing the luminosity to 5-7.5 times the nominal luminosity while remaining at a centre-of-mass energy of 14 TeV. The average number of proton-proton interactions per bunch crossing (pile-up) is expected to rise to $\langle\mu\rangle = 200$.

The LHC experiments are upgraded to cope with the increase in radiation and occupancy.

For ATLAS, a complete replacement of the ID with an all-silicon design is planned [23, 24]. The design consists of cylinders with five pixel layers followed by four strip

module layers. The forward regions are covered by five pixel layers with inclined or vertical rings and six strip disks. The sensors are of finer granularity to deal with the very high pile-up and to be able to reconstruct tracks in high-energy jets.

Especially the innermost layer has to withstand the high fluences close to the interaction point. 3D sensors are used for the innermost pixel layer [25]. The 3D sensors require a relatively low depletion voltage even after high irradiation dose and are more radiation tolerant than planar sensors, but are still relatively expensive. Planar sensors can be mass produced by multiple vendors in high quality with high yields and low cost, which makes them interesting for the large area required for the outer layers.

Readout of the sensors also entails the need for new pixel readout chips beyond the FE-I4 to accommodate for both the smaller pixels as well as the higher bandwidth and new data acquisition (DAQ) and trigger protocols. Chapter 4.4 covers the upgrade of the Inner Detector to the Inner Tracker in more detail.

A new *High-Granularity Timing Detector* (HGTD) in the forward region improves the object reconstruction and identification performance to match the performance in the central region [26].

CHAPTER 3

Semiconductor Pixel Detectors

This chapter is based on and contains sections from Ref. [1].

3.1. Interaction of Particles with Matter

To register particles traversing a detector, they have to interact with the material in a way that induces a measurable signal in the detector. For semiconductor detectors, this is the creation of electron-hole pairs due to ionisation, which in turn are separated by an externally applied electric field and cause a measurable current.

Depending on the type of particles, the interaction processes differ. They can be grouped into light charged particles, the electron and positron, heavy charged particles such as muons, protons or α-particles, and photons. Other neutral particles are not considered here.

Heavy Charged Particles

The predominant interactions of heavy charged particles with matter are inelastic collisions with electrons of the material, and elastic scattering from nuclei, while the emission of Cherenkov radiation, nuclear reactions, and bremsstrahlung are extremely rare processes [27].

The average energy loss per distance of a heavy charged particle is given by the *Bethe-Bloch formula*

$$-\left\langle \frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle = 2\pi N_a r_e^2 m_e c^2 \rho \frac{Z}{A} \frac{z^2}{\beta^2} \left[\ln\left(\frac{2m_e\gamma^2 v^2 W_{max}}{I^2} \right) - 2\beta^2 - \delta - 2\frac{C}{Z} \right]$$

with the symbols listed in Table 3.1. The formula remains valid down to $\beta \simeq 0.1$ and up to $\beta \simeq 1000$, where radiative losses start to dominate. This is shown in Figure 3.1 for muons in copper.

For $\beta\gamma \approx 3.5$, the energy loss reaches a minimum where $-\left\langle \frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle_{mip} = 1.5\,\frac{\mathrm{GeV}}{\mathrm{g\,cm^{-2}}}$ is a good approximation for most materials. Particles at this point are called *minimum ionizing particles* (mip) and are useful to estimate the smallest signal of a charged particle to be expected in a detector.

Table 3.1.: Symbols in the Bethe-Bloch formula [27].

r_e	classical electron radius
m_e	electron mass
N_a	Avogadro's number
I	mean excitation potential
Z	atomic number of absorbing material
A	atomic weight of absorbing material
ρ	density of absorbing material
z	charge of incident particle in units of e
β	v/c of the incident particle
γ	$1/\sqrt{1-\beta^2}$
δ	density correction
C	shell correction
W_{max}	maximum energy transfer in a single collision

Electrons

Electrons and positrons lose energy via similar mechanisms as heavy charged particles, but due to their low mass, bremsstrahlung is much more dominant and the scattering on shell electrons has different kinematic constraints. At low energies, ionisation is still the dominant process, but above the *critical energy* of approximately [29]

$$E_c \approx \frac{800}{Z}\,\mathrm{MeV},$$

with the charge Z of the nucleus, bremsstrahlung becomes dominant.

For high energy electrons and photons, the electromagnetic interactions are characterised by the *radiation length* X_0, which is the mean distance after which the energy is reduced by a factor of $1/e$. It is approximated by [29]

$$X_0 \approx \frac{1}{4\alpha n Z^2 r_e^2 \ln(287/Z^{1/2})},$$

where n is the number density of nuclei and r_e is the classical electron radius. For silicon, the radiation length is 9.36 cm.

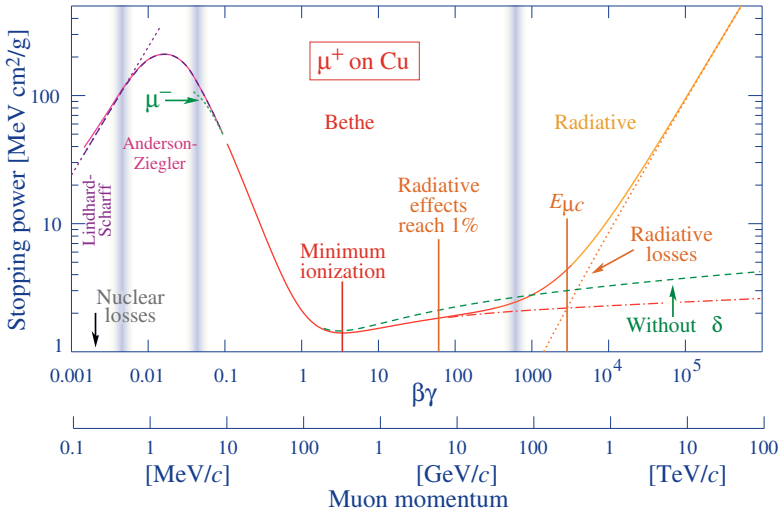


Figure 3.1.: Energy loss for muons in copper over nine orders of magnitude in momentum [28].

Photons

The interactions of photons are very different to charged particles, partly due to the lack of an electric charge. To detect photons, they first have to create charged particles in the material, which in turn cause ionisation and a measurable signal. Photons are either completely absorbed or scattered under relatively large angles, which is in contrast to the behaviour of charged particles. This leads to the intensity of a beam passing through a material decreasing exponentially with the distance x [29]

$$I = I_0 e^{-\mu x},$$

where I_0 is the initial intensity and μ is the material specific attenuation coefficient.

The predominant interactions of photons with matter for increasing energy are:

1. Photoelectric effect
2. Compton scattering
3. Pair production

The cross sections for photons in carbon are shown in Figure 3.2. For low photon energies, the photoelectric effect is the dominant process. The photon is absorbed by an electron, which is then ejected from the atom and carries the energy of the photon reduced by the binding energy. For higher energies, photons can scatter on electrons in the material instead of being absorbed. At sufficiently large photon energies, the electrons can be considered essentially free and the process is described by Compton

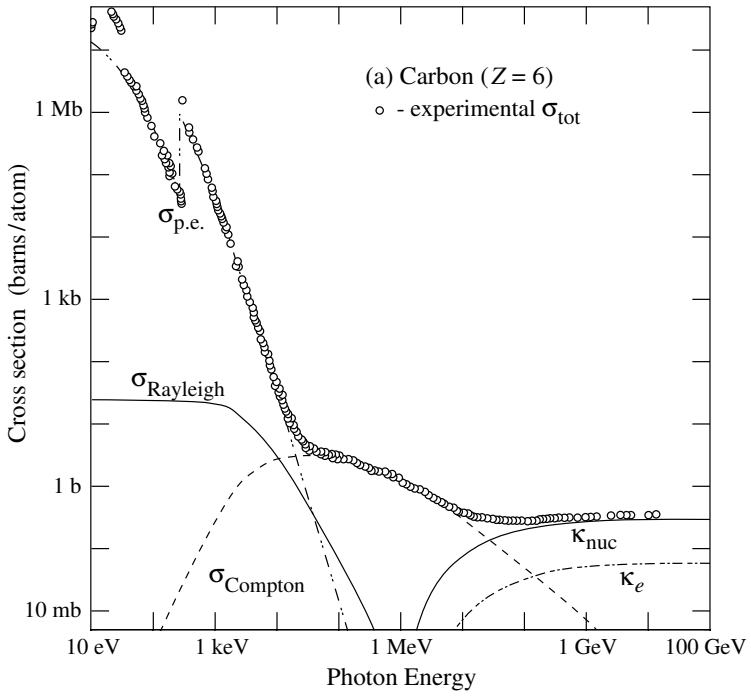


Figure 3.2.: Photon cross section in carbon with the contributing cross sections $\sigma_{\text{p.e.}}$ for the photoelectric effect, σ_{Rayleigh} for Rayleigh scattering, σ_{Compton} for Compton scattering, and κ_{nuc} and κ_e for pair production in the nuclear respective in the electron field [28].

scattering. Pair creation becomes possible above energies of twice the electron mass. A photon can be converted into an electron-positron pair, which requires the presence of a nucleus or an electron to satisfy conservation of momentum. Here, the radiation length corresponds to 7/9 of the mean free path for pair production.

3.2. Semiconductor Detectors

The detection mechanism for particles in semiconductors is based on the creation of electron-hole pairs. For silicon, an average energy of 3.61 eV is required to create one electron-hole pair.

pn Semiconductor Junction

A pn-junction in a semiconductor forms between n-type and p-type material, where the n-type material has been doped with *donor* atoms that have one additional valence electron and the p-type has been doped with *acceptor* atoms that have one valence electron less than the material. For silicon with four valence electrons, typical elements used as p-type dopant are gallium, aluminium, indium and boron, while phosphorus and arsenic are typical dopants for n-type materials.

Pn-junctions are the basic building block of semiconductor detectors. Because the concentrations of electrons and holes differ between p-type and n-type materials, holes diffuse towards the n-region and electrons diffuse towards the p-region, which then recombine and form the *depletion zone*. As both regions were initially neutral and the atoms remain stationary, an electric field is formed which eventually halts the diffusion process. The depletion zone is devoid of free charge carriers and has a very high resistivity compared to the n-type and p-type materials alone.

The potential across the depletion zone can separate electron-hole pairs created inside, but the width is determined by the doping concentration and the low intrinsic potential offers poor charge collection. To increase the sensitive volume of the detector and provide efficient charge collection, the pn-junction is operated with reverse bias, which increases the potential across the junction. By applying a voltage across the junction with the negative terminal on the p-region and the positive terminal on the n-region, holes from the p-region and electrons from the n-region are attracted towards the contacts and the depletion zone widens. In contrast to a pn-junction with forward bias which becomes conductive, the pn-junction with reverse bias conducts very little current. Inside the depletion zone, electron-hole pairs are separated by the electric field and drift towards the electrodes, which causes a measurable current according to the *Shockley–Ramo theorem* [30, 31]. The current i induced by a charge q on an electrode is

$$i = q\vec{E}_w\vec{v},$$

where $\vec{v}$ is the velocity of the charge carriers and $\vec{E}_w$ is the weighting field of the electrode. The weighting field is determined by considering the electrode at unit potential, all other electrodes at ground potential, and removing all free charges.

The pairs are created by the energy deposition of particles, but a current is also caused by thermal effects and by diffusion from the undepleted volume, which is the undesired *leakage current* that contributes to the noise of the detector.

For sufficiently large voltages, the depletion zone can be extended to cover most of the detector volume and is no longer determined by the doping concentration. The achievable width is limited by the breakdown voltage of the junction. The width of the depletion zone is [29]

$$d = x_n + x_p = \sqrt{(V_0 + V_B)\frac{2\varepsilon}{e}\frac{(N_A + N_D)}{N_A N_D}},$$

where d is the total width and x_n and x_p are the widths on the n- and p-side. N_A and N_D are the acceptor and donor concentrations and V_0 and V_B are the potential of the junction itself and the external bias voltage. When the concentrations are very different, the depletion zone extends mostly into the lower doped side of the junction. Together with a depletion voltage well above the built-in potential, the width is approximated by

$$d \approx \sqrt{\frac{2\varepsilon V_B}{e N_D}}.$$

3.3. Noise

A detector not only produces the desired signals caused by the particles traversing the detector, but different sources of noise in the detector and the readout electronics have to be taken into account as well. This limits the smallest detectable signal and the resolution and is therefore an important property of the detector.

It is often useful to state the noise relative to the measured quantity, in this case in terms of the charge. The noise in a detector and the connected readout electronics can then be quantified as *Equivalent Noise Charge* (ENC), which is the amount of charge necessary to produce a signal to noise ratio of one. The total ENC in a system is given by the square sum of the individual contributions.

Thermal Noise

This noise is caused by the thermal motion of charge carriers in a conductor and the resulting random fluctuations of the electron distribution, which is present even without an external voltage. Its spectral density is proportional to the temperature and it is present at all frequencies.

Shot Noise

Shot Noise is caused by the discrete nature of charge carriers and the statistical fluctuation of the number of charge carriers passing through a conductor. Its noise spectrum does not depend on frequency or temperature, but is proportional to the current. In a semiconductor detector, the main contribution to shot noise is the leakage current passing through the sensor, which increases with the temperature of the sensor.

Flicker Noise

This type of noise is produced by many different mechanisms and is present in most electronic systems. Its noise power spectrum has an approximate $1/f$ dependence unlike the thermal and shot noise. In semiconductors and especially in transistors, it is associated with the trapping of charge carriers by crystal defects. They become trapped and are released again with some delay. Due to its frequency dependence, this noise can become dominant at low frequencies, but is exceeded by other noise sources at high frequencies.

3.4. Hybrid Pixel Detectors

For use in a tracking detector, the sensor has to provide spatial resolution for tracks passing through it. To this end, the sensor is segmented into pixels which consist of individual pn-junctions and have to be read out separately. The segmentation is usually achieved by introducing small implants with opposite doping type into the wafer.

With the number of pixels in the order of several ten thousands per sensor not being uncommon, the readout poses a significant challenge. The two usual approaches are *monolithic sensors*, where the readout electronics are integrated on the same chip as the sensor, and *hybrid sensors*, where the readout is performed by a separate chip which has to be connected to the sensor.

The ATLAS pixel detector uses hybrid modules consisting of sensors bump-bonded to the FE-I3 or FE-I4 readout chips. A schematic for a single pixel is shown in Figure 3.3. The pixels are connected to the readout chip with small conductive bump balls. The sensor is operated with reverse bias and the electron-hole pairs created by particles are separated and drift toward the electrodes. The readout chip processes the induced current signal for all individual pixels. Each channel consists of an analog part, which uses an amplifier and a discriminator to generate a pulse with a length proportional to the charge signal, and a digital part, which measures the pulse width and passes the data to a buffer shared between several pixels until readout. Deviations between channels can be compensated by adjusting the discriminator threshold and other settings individually. The parallel readout is necessary in order to achieve the high bandwidth required for the ATLAS detector.

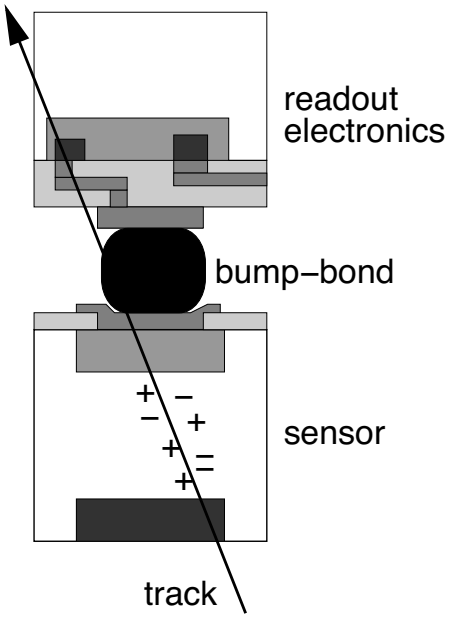


Figure 3.3.: Cross section of a single pixel of a hybrid pixel detector [16].

CHAPTER 4

IBL and ITk Upgrade of the ATLAS Pixel Detector

Upgrades to the LHC aiming for the HL-LHC increase the instantaneous luminosity to 5–7.5 times the nominal luminosity and hence allow the experiments to collect more data in the same amount of time, targeting an integrated luminosity of up to $4000\,\mathrm{fb}^{-1}$ over the runtime of the HL-LHC. This, however, also imposes new challenges on the detectors to sustain a high level of performance.

This chapter covers the intermediate upgrade of the ATLAS inner detector with a new pixel layer and the upcoming upgrade to the Inner Tracker for the HL-LHC. This chapter is based on and contains sections from Ref. [1].

4.1. IBL Upgrade

During the first long shutdown from 2013 to 2015, a new pixel layer was installed in the ATLAS inner detector, the *Insertable B-Layer* (IBL). This was motivated by the need for high precision vertexing and b-tagging, which depends on the performance of the innermost layer. With the increase in luminosity, resulting higher radiation damage, and limits to the hardware lifetime, this step was also necessary to maintain good performance, especially after the Phase-I upgrade [19].

Figure 4.1 shows a schematic view of the ATLAS Pixel Detector with the IBL installed. The beam pipe was replaced by a new pipe with smaller radius to make room for the IBL. Being closer to the interaction point, the tracking resolution is improved, however, the granularity of the sensors and readout has to be increased to deal with the higher fluence. This also increases the requirements in terms of radiation hardness and readout bandwidth.

The IBL is installed at a radius of 33.25 mm around the new beam pipe and consists of 14 staves which are tilted by about 14 degrees and overlap slightly. The staves are $20\,\mathrm{mm}\times664\,\mathrm{mm}$ in size and provide mechanical support to the modules as well as the

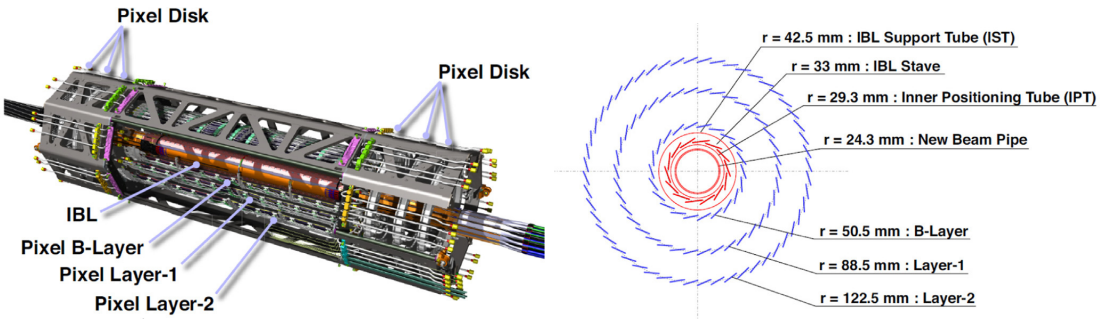


Figure 4.1.: Schematic view of the ATLAS 4-Layer Pixel Detector for Run 2 [32].

electrical connections to power supplies, readout system, and detector control system (DCS). They run along the direction of the beam pipe. A titanium cooling pipe is embedded into the staves, which are made out of a carbon foam material that conducts heat while minimising the amount of material. The staves are reinforced with a carbon fibre laminate for mechanical stability. The cooling pipes are connected to a new CO_2 based cooling plant for IBL which can cool the sensors below $-20\,°C$ during operation and provides a cooling capability of 1.5 kW [33].

A new frontend readout chip, the FE-I4, was developed for the IBL. It is described in Section 4.3. Each stave is equipped with 32 FE-I4 chips, which are arranged into double-chip modules with two FE-I4 bump-bonded to one planar sensor, or into single-chip modules with one FE-I4 bump-bonded to one 3D sensor.

The modules are connected to the on-stave *type 0* electrical services, which are on a flexible circuit board (the *stave flex*) running along the stave. The stave flexes are connected to the *type I* services at the End of Stave (EoS) card, which is mounted on the support structures on both ends of a stave. The type I service cables are about 3 m long and run from the EoS region to the Patch Panel 1 (PP1) at the edges of the Inner Detector, where they are plugged into the *type II* services. Here, the signal lines are connected to electrical-to-optical converters and continue as fibres. Further outside on Patch Panel 2 (PP2) are the voltage regulators that supply the IBL with power [19].

The connection of the services to the IBL is shown in Figure 4.2. Outside of the detector, the services run to the USA15 counting room next to the main ATLAS cavern.

4.2. Phase-0 Pixel Readout

A schematic overview of the IBL readout is shown in Figure 4.3. It consists of the *Back-of-Crate* (BOC) and the *Read-Out Driver* (ROD) card, which are installed in a crate. This is similar to the system used for the other parts of the pixel detector, but adopted to deal with the higher bandwidth and the different data format of the FE-I4. Each ROD-BOC pair is connected optically to two optoboards, corresponding to the 32 FE-I4 on a stave. [33]

The BOC card interfaces optically to the detector and also receives the global LHC

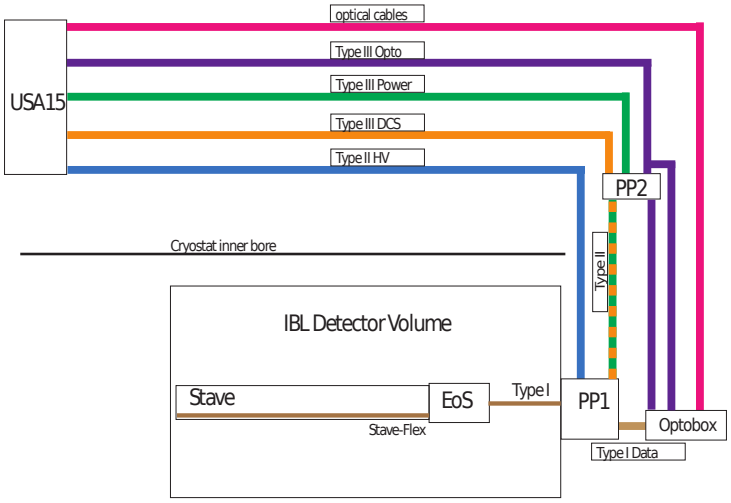


Figure 4.2.: Schematic overview of the location and usage of services types [19].

clock and distributes it to the detector and the ROD card. It also decodes the data coming from the detector and provides it to the ROD. Data from the ROD is handled by the BOC and transmitted optically via custom *S-LINK* channels to the global ATLAS *Readout System* (ROS).

The ROD card is responsible for steering the IBL detector and formatting the data received from the detector. It generates the trigger, configuration, and control data that is sent to the detector, and can perform histogramming of the received data for detector calibration, or can pass it to the higher level readout system via the BOC during data taking.

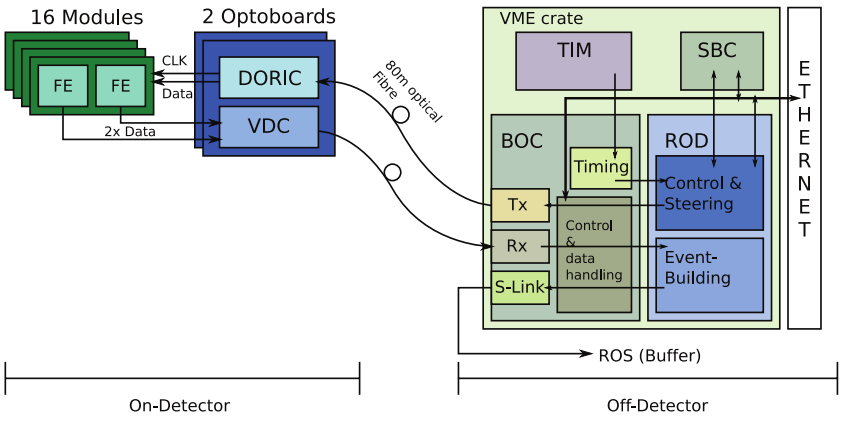


Figure 4.3.: Schematical overview of IBL readout. The VME crate houses a timing, trigger, and control Interface Board (TIM), a Single Board Computer (SBC), and the ROD and BOC cards [33].

4.3. The FE-I4 Frontend Readout Chip for IBL

4.3.1. Motivation

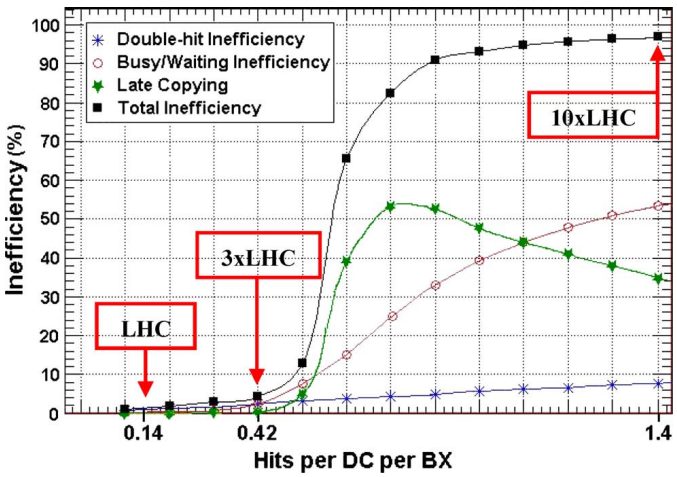


Figure 4.4.: Inefficiencies of the FE-I3 with increasing hit-rate [34].

The planned upgrade of the LHC to the HL-LHC exceed the capabilities of the frontend chips currently used for pixel readout. Figure 4.4 shows the inefficiency of the FE-I3 as function of the hit rate. At around three times the LHC luminosity, the inefficiency starts to increase significantly. Double-hit inefficiency occurs, when a pixel is hit twice in fast succession and the second hit is not recognized as separate event. The busy/waiting inefficiency is caused by the read-out architecture of the pixel array, which uses a shared bus inside each double-column. Every registered hit in the FE-I3 is transferred over this bus and buffered. As the bus is shared between all pixels in a double-column, but can only be used for one transfer at a time, the waiting time increases with the hit rate. As the pixels can only store a single hit, subsequent hits during this time are lost. This effect increases as the bus becomes saturated. A high waiting time can also cause the hit data to arrive too late for readout, which is the late copying inefficiency.

The increasing hit rates lead to problems both for the readout efficiency and the additional requirements for radiation hardness. The FE-I4 is the first step in addressing these issues, as it is designed to meet the requirements for operating closer to the interaction point in the IBL upgrade [34]. A new frontend chip for the HL-LHC upgrade is still under development and is described in Section 4.6.1.

4.3.2. Design of the FE-I4 Chip

The FE-I4 is manufactured in a 130 nm process with a reduced pixel size of 50 µm × 250 µm compared to the FE-I3 with 50 µm × 400 µm pixels and a 250 nm process. This helps to reduce the double-hit inefficiency and increases the spatial resolution. Figure 4.5 shows the FE-I4 in comparison to the FE-I3. With 20.2 mm × 18.8 mm, the FE-I4 is

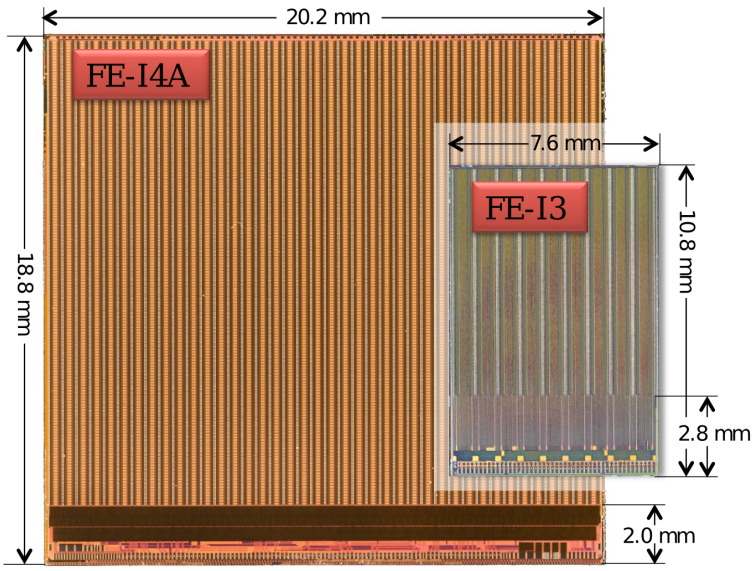


Figure 4.5.: Comparison of the FE-I4A and the FE-I3 at same scale [35].

significantly larger than the FE-I3 with only 7.6 mm × 10.8 mm. The pixel array of the FE-I4 takes up 89% of the chip, while the active area of the FE-I3 is only 74%.

Figure 4.6 shows a schematic overview of the chip. The FE-I4 pixel array is comprised of 26880 pixels, organised in 336 rows and 80 columns. Two columns each are grouped together to form 40 double-columns. The double-columns in turn are divided into 2x2 pixel regions with four separate analogue pixels and one common *Pixel Digital Region* (PDR). Hits are stored in the PDR alongside timing information. An external trigger can then select events with the matching trigger latency, which are transferred to the *End of Digital Column Logic* (EODCL). Hits which exceed the trigger latency are discarded. By only transferring the selected events, the bus is not congested by unwanted events, as was the case for the FE-I3. The double-hit inefficiency is addressed by the reduced pixel size, which automatically reduces the pixel hit probability, and a faster return of the signal to baseline, which reduces the dead time of the analog pixel.

The lower edge of the chip contains the *End of Chip Logic* (EOCHL), which is responsible for processing the hit data and triggers and inserting service records and register readbacks into the data stream. The *Data Output Block* (DOB) then encodes the data stream and sends it to the transmitter. The *Command Decoder* (CMD) receives commands and generates the appropriate signals to control the other components of the chip. All global parameters of the FE-I4 are stored in the *Configuration Memory* (CNFGMEM). The *Phase Locked Loop* (PLL) is locked to the 40 MHz clock input and provides multiples (1x, 2x, 4x and 8x) of the clock input to the data transmitter and other blocks. The FE-I4 also contains several voltage and current regulators, some of which are programmable.

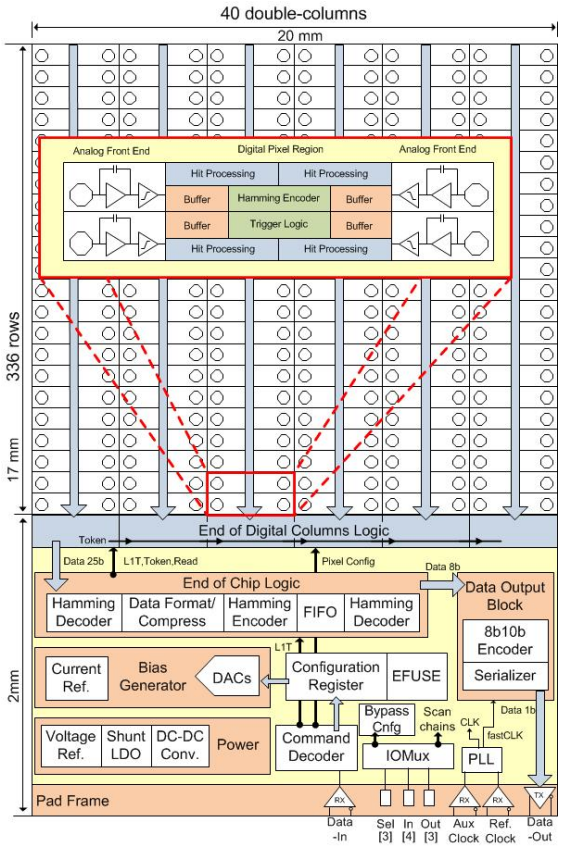


Figure 4.6.: FE-I4 chip diagram [36].

Many internal signals can be routed to pads on the edge of the chip. With this, parts of the chip can be bypassed or accessed directly. This is useful for testing, but not necessary for operating the FE-I4 under normal circumstances.

There are two revisions of the FE-I4, namely the prototype FE-I4A and the FE-I4B, the improved revision used in the IBL detector.

Analog Pixel

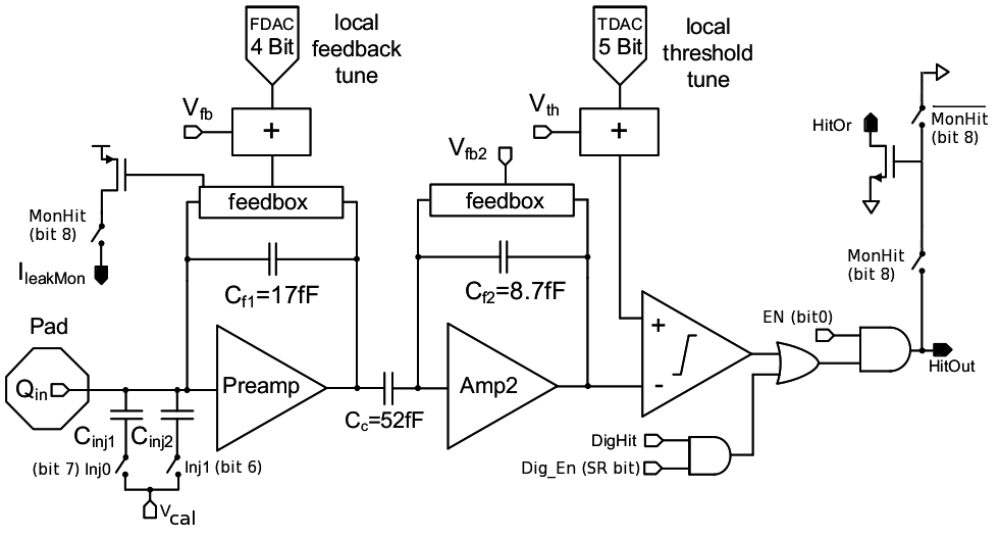


Figure 4.7.: Schematic diagram of an analog pixel [36].

Figure 4.7 illustrates the inner structure of an analog pixel. The sensor is connected to the input pad on the left, which feeds into the first stage of the two-stage amplifier, followed by the discriminator. The capacitors for charge injection are also connected to the amplifier. They allow the injection of a known amount of charge into the pixel, independent from the sensor. This is used for testing and characterisation of the pixels, where the response to the injected charge is measured.

The discriminator converts the analog charge signal into a digital square wave signal. The output of the discriminator is zero as long as the input is below the threshold, and otherwise one. The return to baseline of the amplifier and the discriminator threshold are adjustable for each pixel. The amplifier has a nearly linear return to baseline, which leads to a pulse width of the discriminator approximately proportional to the input charge. This in turn can be measured as the *Time over Threshold* (ToT) of the discriminator.

4.3.3. Operation

Registers

The FE-I4 contains programmable registers which control certain aspects of the chip. There are two types of registers. The global registers (GR) are common to the whole frontend and control parameters that affect the entire chip, while each pixel has its own independent set of pixel registers, which directly control the pixel electronics. The global registers are organised and accessed as 36 words with 16 bit each and subdivided into configuration parameters of one bit to 40 bit size.

Each pixel has six pixel registers with a combined size of 13 bit. The pixel registers are accessed over the pixel shift register. This register is 672 bit long, directly corresponding to the 672 pixels in a double column. The pixel registers are shown in Figure 4.7, labelled as *FDAC*, *TDAC*, *Inj0*, *Inj1*, *MonHit* and *EN*. The pixel shift register is also connected to the *Dig_En* input. *FDAC* controls the feedback current of the preamplifier which steers the return to baseline and hence the ToT and *TDAC* adjusts the threshold of the discriminator. *Inj0*, *Inj1* and *Dig_En* are used to inject signals into the analog and digital part of the pixel respectively, which is explained in more detail in Chapter 4.3.4. The *EN* register enables the pixel for readout.

All registers are designed to be tolerant to *Single Event Upsets* (SEU), as bit errors can disturb the operation of the chip. SEUs are unexpected changes of state caused by ionising particles in semiconductor circuits. They do not damage the chip, but interfere with the electronics and can cause undefined or erratic behaviour. The tolerance is achieved by triplicating all registers and using error-correcting codes [36].

Commands

Name	Field 1	Field 2	Description
size (bits):	5	4	
LV1	11101	-	Level 1 Trigger
BCR	10110	0001	Bunch Counter Reset
ECR	10110	0010	Event Counter Reset
CAL	10110	0100	Calibration Pulse
Slow	10110	1000	Slow command header

Table 4.1.: Trigger and Fast Commands [36].

The FE-I4 receives commands over a simple serial link, typically at 40 MHz clock speed. Commands are divided into the three classes *Trigger*, *Fast* and *Slow*. The chip can either be in *Run Mode*, where it only responds to triggers and fast commands, or in *Slow Mode*, where it only executes slow commands. The only exception is the *RunMode* command, which switches between the two modes and therefore has to be executed in both modes. Table 4.1 shows the trigger command, the fast commands and

Name	Field 3	Field 4	Field 5	Field 6	Description
size (bits):	4	4	6		
RdRegister	0001	ChipId	Address	-	Read addressed global memory register
WrRegister	0010	ChipId	Address	Data	Write into addressed global memory register
WrFrontEnd	0100	ChipId	xxxxxx	Data	Write conf data to selected shift register(s)
GlobalReset	1000	ChipId	-	-	Reset command; Puts the chip in its idle state
GlobalPulse	1001	ChipId	Width	-	Has variable pulse width and functionality
RunMode	1010	ChipId	Mode	-	Sets Run Mode or Conf Mode

Table 4.2.: Slow Commands [36].

the unique header that identifies slow commands. The trigger command is the shortest command and initiates the acquisition of hit data. The *BCR* commands resets the bunch counter of the FE-I4, which counts the number of 40 MHz pulses from the external clock, corresponding to the bunch crossing rate at the LHC. The *ECR* command clears the data path of the frontend and can be issued to restore synchronisation across several chips. The *CAL* command generates calibration pulses which can be used to inject signals into the digital or analog parts of the pixel array.

The slow commands are listed in Table 4.2. They are longer than the other commands and include a chip identification to address a specific FE-I4. This allows sharing the same command link between up to eight chips while being able to address each of them individually. One bit in the identifier indicates that all FE-I4 should execute the command. The slow commands *RdRegister* and *WrRegister* are responsible for reading and writing the global registers. The *WrFrontEnd* command writes 672 bits into the shift registers of the selected double-columns. Issuing the *GlobalReset* command resets the chip to its initial state and clears the content of the whole frontend. The *GlobalPulse* command generates a pulse which can be routed to different parts of the chip to invoke special behaviour such as copying the content of the pixel shift register into the pixel registers. The *RunMode* command selects Run Mode when field 5 is set to 111000 and Conf Mode for 000111.

Output Format

In contrast to the control link, which receives the commands unencoded at 40 Mbit/s, the data link transmits data with 8b10b encoding at a configurable rate between 40 Mbit/s and 320 Mbit/s. While 160 MHz is the default setting and is currently used in ATLAS, the clock can be selected to be 1x, 2x, 4x or 8x the 40 MHz clock input.

8b10b encoding translates each 8-bit byte into a 10-bit sequence with desirable properties to facilitate clock recovery, AC-coupling and error detection. As only a subset of the 1024 possible 10-bit sequences is used for encoding, additional symbols are introduced to mark the start and end of packets or to indicate that the transmitter is idle.

Before encoding, the data are organised in 24-bit records as shown in Table 4.3. The *Empty Record* is only transmitted when 8b10b encoding is disabled. All records except

the *Data Record* and the *Empty Record* start with the pattern 11101, followed by a 3-bit identifier and the 16-bit payload.

The start of pixel data is marked by the *DataHeader*, which contains a trigger counter and a BCID (Bunch-Crossing Identifier) counter. The actual pixel data consisting of the column, row and ToT of a hit is stored in a *DataRecord*. In the case of two hits in neighbouring pixels of the same column, both hits are stored in the two ToT fields of the same record. *AddressRecords* and *ValueRecords* are used to read global registers and pixel registers. The address of the register is stored in an *AddressRecord*, followed by the value of the register in a *ValueRecord*. *ServiceRecords* indicate errors or additional information and hold a code that expresses the kind of condition alongside with a 10-bit value.

Record Word	Field 1	Field 2	Field 3	Field 4	Field 5
Data Header (DH)	11101	001	Flag	LV1ID [4:0]	bcID [9:0]
Data Record (DR)	Column [6:0]	Row [8:0]	ToT(1) [3:0]	ToT(2) [3:0]	
Address Record (AR)	11101	010	Type	Address [14:0]	
Value Record (VR)	11101	100	Value [15:0]		
Service Record (SR)	11101	111	Code [5:0]	Number [9:0]	
Empty Record (ER)	abcdefgh	abcdefgh	abcdefgh		

Table 4.3.: The six 24-bit Record Words [36].

4.3.4. Data Acquisition

On power-up, all registers are cleared and the FE-I4 is left in *ConfMode*. For data acquisition, an appropriate configuration has to be written to the registers and the chip has to be placed in *RunMode*. Signals from a connected sensor or from the internal pulse generator are registered and stored as hits in the corresponding pixel, as long as they exceed the discriminator threshold. They can then be read-out by issuing a trigger command.

Triggering

When a hit is detected, it is stored locally alongside with an 8-bit counter that measures the time since the hit was registered. The counter starts at 255 and counts down until it reaches the trigger latency stored in a global register. If a trigger is issued, all regions that have a counter matching this latency value are flagged for read-out. Otherwise, the hits are discarded and the counters are reset.

Triggers can be supplied externally by executing the *LV1* command, or generated internally by enabling the *HitBus*, which is the logical *OR* of all selected discriminator outputs. By setting a pixel register, individual pixels can be connected to the *HitBus*. When one of the connected pixels detects a hit, this becomes visible on the *HitBus* and a trigger command is issued.

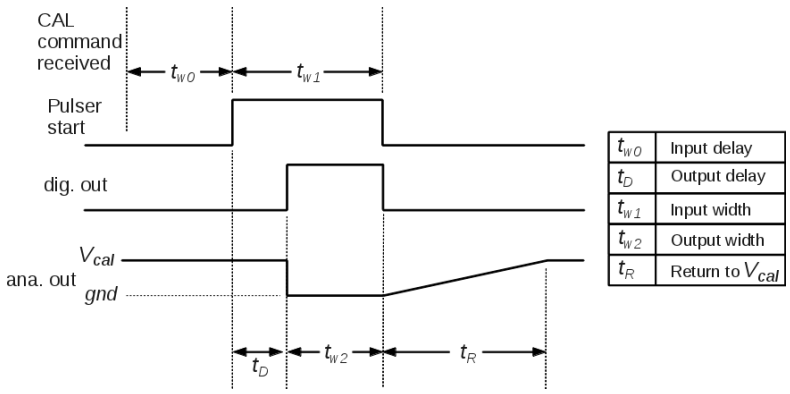


Figure 4.8.: Outputs of the pulse generator [36].

Pulse Generator

The programmable pulse generator of the FE-I4 can be used to inject signals into both the analog and the digital part of each pixel. This is called *Analog Injection* or *Digital Injection* and allows producing hits even when no sensor is connected, which is used to test various parts of the pixel by injecting a known signal and measuring the response.

Figure 4.8 shows the analog and digital waveforms generated by the pulse generator in response to a *CAL* command. Almost all parameters of the signal, such as the delay and the pulse width are configurable via global registers. The pulse generator can also be activated by executing a *GlobalPulse* command and routing the global pulse to the pulse generator.

For *Analog Injection*, each pixel has two capacitors, C_{inj1} and C_{inj2}, which can be selected by the corresponding pixel registers. They are connected in parallel to the preamplifier and the calibration voltage V_{cal}, as can be seen in Figure 4.7. The shape of the applied signal is controlled by the pulse generator. The output of the pulse generator is at V_{cal} and with a certain delay after receiving the *CAL* command, the output is pulled to ground and held there for the duration t_{w2}. Afterwards, the voltage increases over the duration t_{R} and returns to V_{cal}. The falling edge injects a negative charge into the amplifier, possibly generating a hit.

Digital Injection has to be enabled globally in a global register and for individual pixels in the pixel shift register. The pulse generator will then generate a hit in the selected pixels, completely bypassing the amplifier and the discriminator.

When selecting double-columns for injection, the behaviour between analog and digital injection differs slightly. For *Digital Injection*, selecting[1] the double-column n selects the columns $2n + 1$ and $2n + 2$, while for *Analog Injection*, the columns $2n$ and $2n + 1$ are selected and selecting double-column 0 only selects column 1, but selecting double-column 39 selects the columns 78, 79 and 80.

[1] Columns are numbered from 1 to 80 while double-columns are numbered from 0 to 39.

4.3.5. Tests and Scans on the FE-I4

Aside from the operation of the FE-I4 in a tracking detector, the functions described in the previous sections are also used for standalone tests and measurements. For this, all readout systems, both for smaller test setups as well as for the IBL in the ATLAS detector, implement a set of test and scan procedures. In this context, scans describe procedures performed by the readout system to measure the response of the frontend chip for different values of a frontend parameter, but the term is also used more loosely for measurements in general.

Scans consist of one or several nested loops and use the internal injection mechanism of the FE-I4. To prevent overloading the analog injection mechanism and to reduce crosstalk between pixels, not all pixels are injected at the same time. Masks are used in which only every n-th pixel is enabled, where n depends on the type of scan. All enabled pixels are injected several times and the mask is then shifted by one pixel and the injection is repeated until all pixels are covered. The number of injections also depends on the scan.

The innermost loop over the pixels is usually implemented in the firmware of the readout system for performance reasons. The outer loops are implemented in software and loop over frontend parameters such as the injected charge or the discriminator threshold. Together with the scan, collected data are analysed and histograms are generated or measured parameters are determined.

Digital and Analog Test

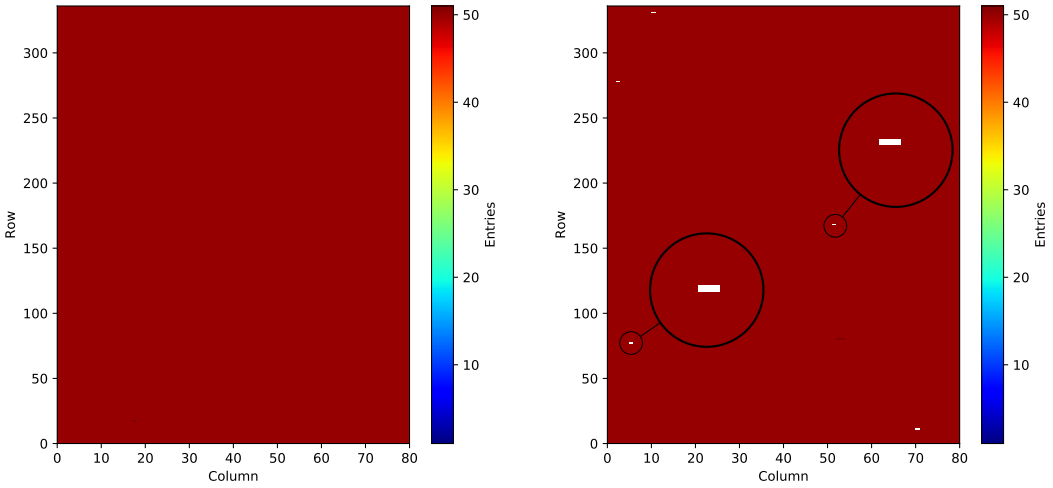
These tests use the digital or the analog injection mechanism respectively, to inject hits into all pixels of the frontend. For the analog test this means that the injected charge is well above the discriminator threshold. With these tests the basic operation of all pixels can be verified.

Figure 4.9 shows occupancy maps with the number of hits per pixel for a digital and an analog test. In this case, every pixel is injected 50 times and should therefore also report 50 hits. For the digital test this is indeed the case for all pixels, but the analog test shows several pixels with less than 50 hits. Those pixels can then be masked to exclude them from readout in other measurements.

Threshold Scan

The frontends use a discriminator to suppress noise and other signals below an adjustable threshold. An ideal discriminator would never fire for signals below the threshold and would always fire for signals above the threshold, leading to a hit probability described by a step function centred around the threshold. A real discriminator however is also influenced by noise in the system, leading to a smeared-out response around the threshold as illustrated in Figure 4.10(a). In this case, the hit probability is described by

$$P_{\text{hit}}(Q) = \frac{1}{2}\text{Erfc}\left(\frac{Q_{\text{threshold}} - Q}{\sqrt{2}\sigma_{\text{noise}}}\right),$$



(a) Digital Test.

(b) Analog Test.

Figure 4.9.: Occupancy maps for the Digital and Analog Test. Shown is the number of hits per pixel. A few broken pixels are highlighted in (b).

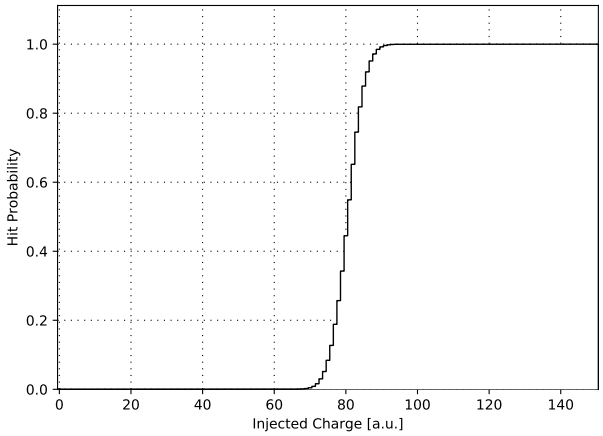
where Q is the charge, $Q_{\text{threshold}}$ is the discriminator threshold, and σ_{noise} is the noise. Erfc is the complementary error function defined as

$$\text{Erfc}(x) = \frac{2}{\sqrt{\pi}} \int_x^\infty e^{-y^2} \, \mathrm{d}y.$$

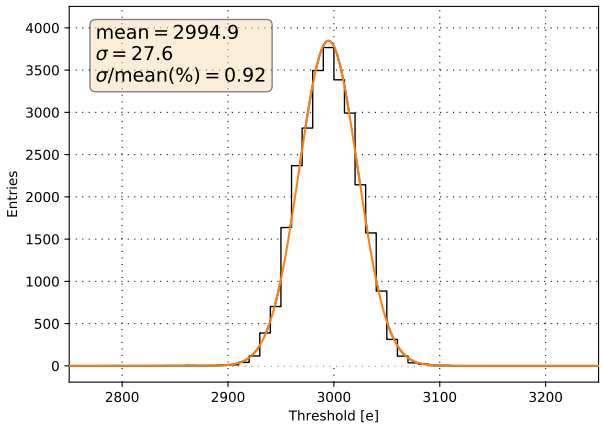
With this, the threshold $Q_{\text{threshold}}$ is defined as the point with a hit probability of 50%.

A threshold scan measures the discriminator threshold and noise of a frontend. It uses the injection mechanism to inject different amounts of charge into the analog pixels and measures the response of the discriminators. By fitting the hit probability of all pixels, the discriminator threshold and noise are determined. Figure 4.10(b) shows a histogram of all measured thresholds on a frontend. This distribution has a Gaussian shape and the overall threshold of a frontend is usually characterised by the mean and width of this distribution. Figure 4.10(c) shows the same but for the measured noise values. Again, the characteristic quantities are the mean and the width of the distribution.

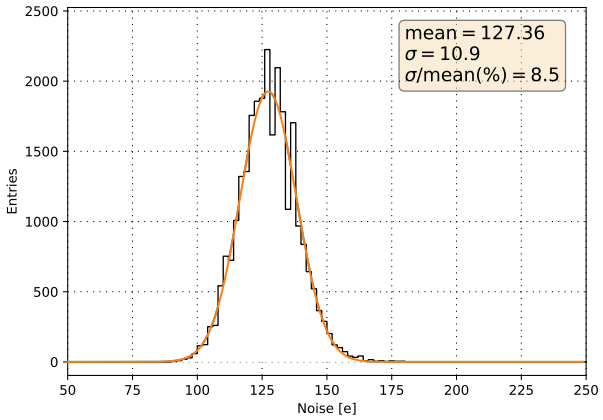
To measure the threshold in terms of an electric charge, a conversion between the global register setting the voltage of the injection pulse generator and the injected charge via the injection capacitors is necessary. Due to manufacturing variances, this conversion should be measured individually for each frontend to get a better accuracy for charge measurements. The FE-I4 has a dedicated circuit to determine the capacitance of the charge injection capacitors, but it is only accessible during wafer probing. The electric charge is typically quoted in units of the elementary charge e.



(a) Hit probability.

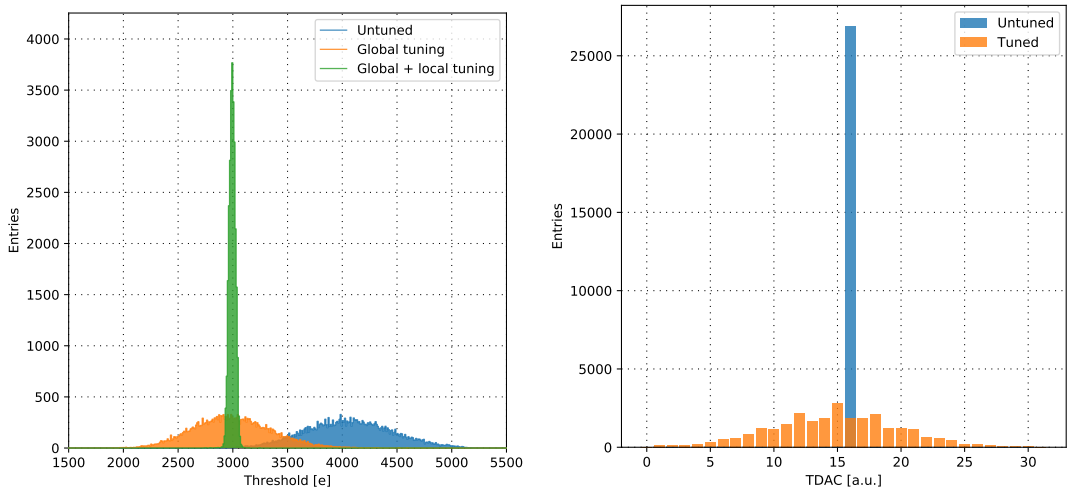


(b) Threshold distribution.



(c) Noise distribution.

Figure 4.10.: Hit probability, discriminator threshold distribution and noise distribution measured by a threshold scan.



(a) Threshold distributions without tuning, after the global tuning, and after the local tuning.

(b) TDAC distributions before and after the local tuning.

Figure 4.11.: Discriminator threshold and TDAC distributions for different steps in the tuning process.

Threshold and ToT Tuning

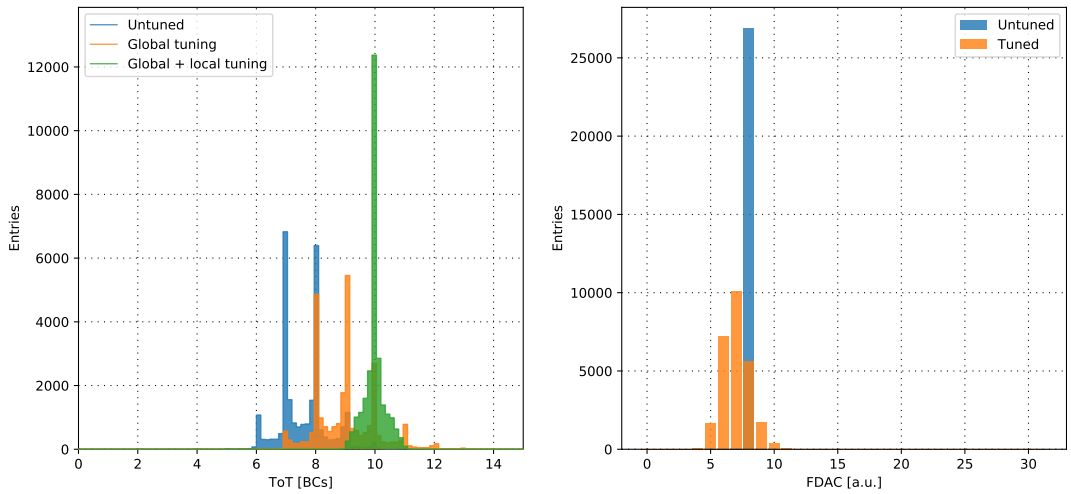
Both the discriminator threshold and the time over threshold (ToT) are adjustable. This is used to compensate for manufacturing spread and changes during operation, such as damage from irradiation, and to set them to a value suitable for the experiment.

The discriminator threshold can be set globally via the *VthinAlt_Coarse* and *VthinAlt_Fine* registers. In addition, each pixel has a 4-bit *TDAC* register to fine-tune the per-pixel discriminator threshold. Similarly, the time over threshold can be set globally via the *PrmpVbpf* register and trimmed for each pixel using the 5-bit *FDAC* registers.

A dedicated tuning procedure is used to adjust the threshold and time over threshold to a uniform target value.

It starts with a frontend that has been configured with a default configuration. The global threshold is set to an arbitrary value and the per-pixel threshold trims are set to the center of their range. The threshold distribution has a wide Gaussian shape and is centred around a value corresponding to the arbitrarily set global threshold. This is illustrated in Figure 4.11(a), which shows the discriminator threshold distribution of a frontend at different steps of the tuning procedure with a target threshold of 3000 e.

The first step of the tuning procedure adjusts the global threshold so that the average matches the target. This causes the distribution to be centred around the correct value, but it still has a large spread. The second step uses the per-pixel TDAC trims to bring the discriminator threshold of the individual pixels closer to the target. The distribution is still centred around the target, but has become much narrower. The TDAC distribution



(a) ToT distributions without tuning, after the global tuning, and after the local tuning.

(b) FDAC distributions before and after the local tuning.

Figure 4.12.: Time over threshold and FDAC distributions for different steps in the tuning process.

before and after this step is shown in Figure 4.11(b).

The step size of the per-pixel trim is another important parameter for the tuning. A small step size improves the accuracy of the tuning, as the difference to the target threshold can be controlled more precisely, effectively reducing the width of the threshold distribution. On the other hand, the trim has a limited range that is reduced by a smaller step size and limits the largest deviation that can be compensated by the trim. The TDAC step size is set by the *TdacVbp* register.

A similar procedure is used to set the ToT response of the frontend and the individual pixels to a target value. As the time over threshold is approximately proportional to the deposited energy, a uniform ToT response over all pixels is desirable to measure the energy spectrum.

The different steps of the procedure are illustrated in Figure 4.12(a), which shows a histogram of the average ToT responses when the pixels are injected with a signal of 16000 e. The structure is caused by the relatively low time resolution of the ToT. As each pixel is injected 50 times and then averaged, some pixels are assigned a non-integer value.

The first step adjusts the feedback current globally for all pixels and moves the average of the distribution to the target, which is set to 10×25 ns at 16000 e in this example. The second step then corrects the feedback current with the finer per-pixel FDAC trim to bring the pixels closer to the target value. The FDAC distribution before and after this step is shown in Figure 4.12(b). In this example, only a small part of the available FDAC range is used. A smaller FDAC step size could improve the tuning by taking

advantage of the better resolution without exceeding the available range. The FDAC step size is set by the *FdacVbn* register.

The discriminator threshold tuning changes the threshold of the discriminator and therefore also the time over threshold for a given signal. Similarly, the time over threshold tuning changes the signal shaping of the preamplifier, which influences the signal on the discriminator. Because both tuning procedures influence each other, special care has to be taken to ensure the proper tuning of both parameters at the same time. This is usually achieved by alternating the tuning steps for global threshold and ToT several times and then the steps for local threshold and ToT several times. As the changes made by each tuning step gradually become smaller, the influence on the other also diminishes.

Noise Scan

A noise scan is used to determine how likely it is that a pixel registers a hit even when no signal is present. Noise can become a problem, especially when operating at very low discriminator thresholds.

It does not use the injection mechanism and sends trigger commands to the frontend at a fixed frequency. The recorded hits are either caused by noise on the pixel, random coincidences between triggers and external signals, such as hits from cosmic radiation, or broken frontend pixels that do not work properly. Pixels above a certain noise level are usually masked.

Source Scan

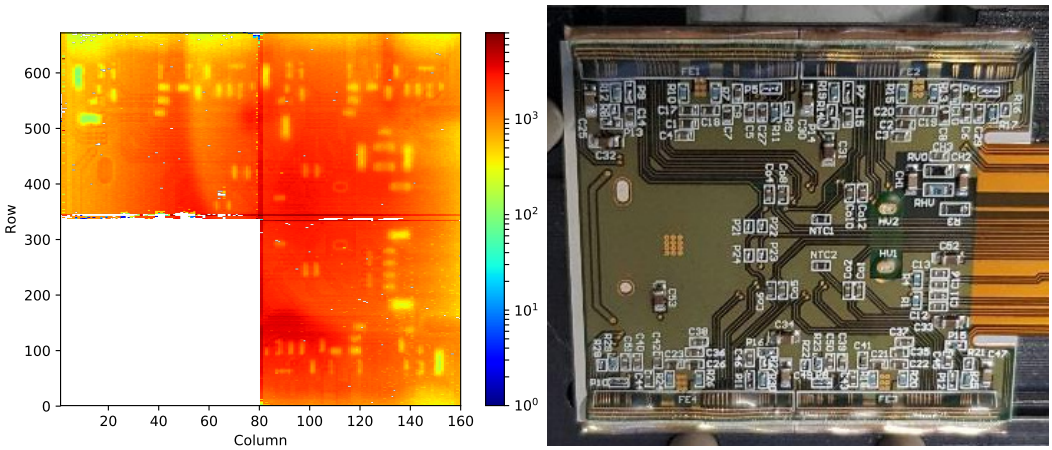


Figure 4.13.: Measurement with ^{90}Sr source and picture of the flexible circuit board and components on top of the module [37].

Instead of using the injection mechanism, the source scan records physical hits coming from the sensor connected to the frontend, for example from a radioactive source or from cosmic radiation. The hits are read out by issuing triggers to the frontend chip. This

can be achieved by using the HitBus self-trigger mechanism of the FE-I4 or with an external trigger source such as a scintillator connected to the readout system.

Each hit is associated with its position and the ToT, also allowing to measure the energy spectrum. To measure a clean energy spectrum and to properly use the self-trigger mechanism, pixels that are too noisy or keep the HitBus constantly active have to be masked. This masking is usually part of the setup procedure and also includes the threshold and ToT tuning.

Figure 4.13 shows an occupancy histogram of a quad-chip module with four FE-I4 bump-bonded to a sensor. One frontend is inoperative. The module is placed under a ^{90}Sr source and is recording hits from the source. Also shown is a picture of the module with a flexible circuit board on top which is wirebonded to the FE-I4 chips and connects them to the readout system and power supplies. The sensor is between the circuit board and the frontends. The components on the board attenuate the radiation from the source, making them visible in the histogram.

4.4. ITk Upgrade

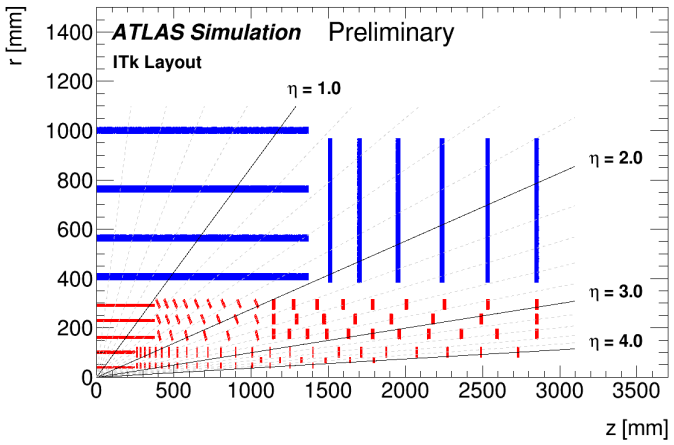
The upgrade of the ATLAS detector for the HL-LHC encompasses the complete replacement of the current Inner Detector with the new *Inner Tracker* (ITk). The HL-LHC will reach a peak luminosity of $7.5 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$, which corresponds to about 200 proton-proton collisions per bunch-crossing. The ITk will operate for over ten years and the ATLAS detector is expected to collect a dataset of $4000\,\mathrm{fb^{-1}}$ during this time. A replacement of the inner two layers of the ITk pixel detector with a new detector is foreseen to maintain good tracking performance and to account for radiation damage during the lifetime of the detector. This also allows taking advantage of new technologies for the replacement detector [25].

A schematic view of one quadrant of the ITk is shown in Figure 4.14. The detector consists of a strip subsystem and a pixel subsystem. The strip detector shown in blue is composed of four layers in the barrel region and six disks in the end-caps. The pixel system consists of five flat barrel layers and five layers of inclined or vertical rings providing coverage in the forward region [24]. This layout differs from the layout described in the ITk pixel detector technical design report (see Ref. [25]) and the ITk strips detector technical design report (see Ref. [38]).

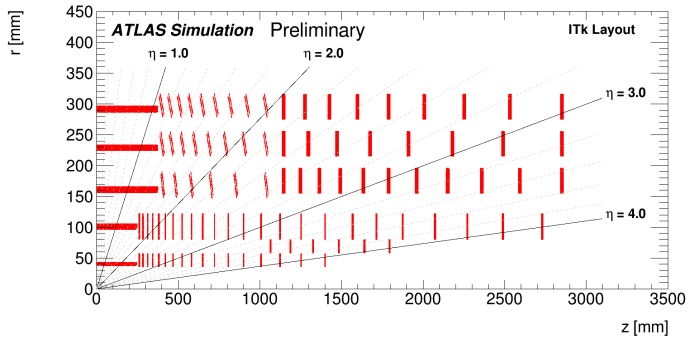
The innermost flat barrel layer is equipped with single-chip modules, while all other barrel layers and inclined sections are equipped with quad-chip modules. A new readout chip for the ITK pixel detector is being developed and can achieve a data bandwidth of up to $4 \times 1.28\,\mathrm{Gbit/s}$. It is described in more detail in Section 4.6.1.

4.5. Phase-II Pixel Readout

The readout for the ITk pixel detector is split into the on-detector and the off-detector part, which are connected with optical fibres. This is similar to the current pixel detector, but with the links operating at up to $10\,\mathrm{Gbit/s}$. Optical to electrical or electrical to



(a)



(b)

Figure 4.14.: Schematic of one quadrant of the ITk. The strip detector is shown in blue, the pixel detector in red. (b) shows a magnified view of the pixel detector [24].

optical conversion of the optical links depending on the direction of transmission is performed on the detector and an aggregation scheme is used to connect several frontend chips to one optical link.

For the links transmitting commands to the frontend chips, a lpGBTX (Low Power GigaBit Transceiver) chip is used after the optical to electrical conversion to split the link bandwidth between up to 16 modules receiving commands at 160 Mbit/s each. See Chapter 5.2 for a description the GBTX, which is the predecessor of the lpGBTX and performs a similar function but at a lower bandwidth.

In the other transmission direction, a similar scheme is used to aggregate several of the 1.28 Gbit/s frontend links into one optical link. As each frontend can use up to four 1.28 Gbit/s links, different configurations are possible and are chosen depending on the expected data rate of the frontend for a given position in the detector.

4.5.1. FELIX

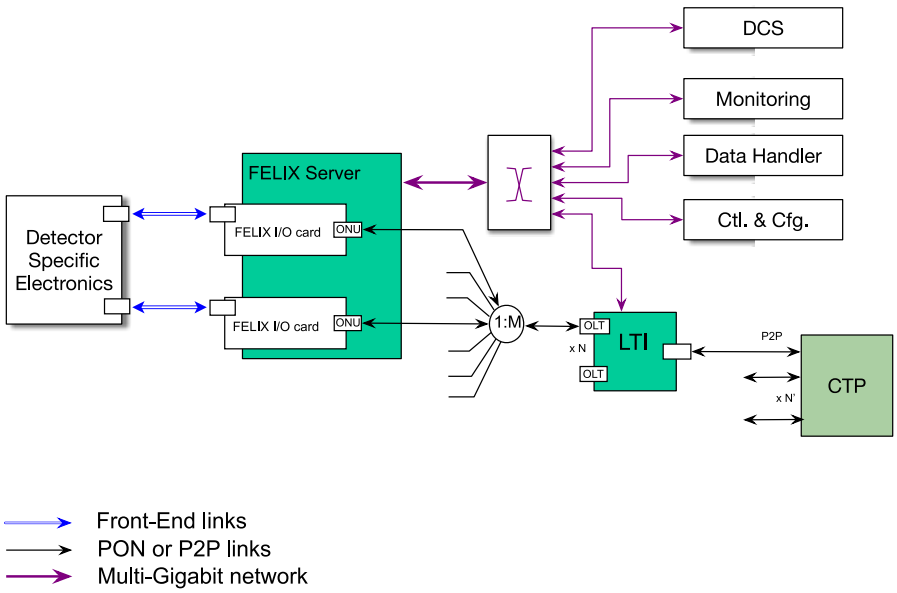


Figure 4.15.: Overview block schematic of the off-detector electronics with FELIX as first-stage detector interface and LTI as trigger interface [25].

The *Front-End Link eXchange* (FELIX) system is an interface between the data acquisition system and the detector frontend and trigger electronics and will be installed during the Phase-I upgrade for the New Small Wheel and the trigger readout of the liquid argon calorimeter [39].

Compared to the readout scheme described in Section 4.2, FELIX replaces most of the custom off-detector hardware with commercial off-the-shelf hardware, including the BOC-ROD system and the ROS. The FELIX system is connected to a multi-gigabit network and routes the data to the clients on the network for processing. All further analysis is performed on commodity servers connected to the network.

The FELIX hardware consists of custom PCI Express cards installed in servers. The FELIX cards interface directly with the optical links to the detector and house FPGAs to implement the custom protocols used for communication with the detector, for example the protocols used by the GBTX and in the future the lpGBTX. The scheme is shown in Figure 4.15. The FELIX cards are also connected directly to the Local Trigger Interface (LTI) to inject trigger commands into the command stream. The Phase-II upgrade will adopt FELIX as the common readout system for ATLAS [40].

4.6. RD53 collaboration

The RD53 collaboration was created to design the next generation of hybrid pixel readout chips to enable the ATLAS and CMS Phase 2 pixel upgrades [41]. It was formed in 2013

and resulted in the development of the RD53A readout chip, which demonstrates the suitability of the chosen technology for the HL-LHC upgrade but is not intended as a final design and includes design variations for testing purposes [42].

Following the successful development of the RD53A prototype chip, the scope of the collaboration was extended to produce a common design that can be adjusted to meet the requirements of both ATLAS and CMS. This is the RD53B, based on which two different chips will be produced for ATLAS and CMS, differing in the size of the pixel matrix to meet the different geometrical constraints of the detector layouts and using the features appropriate for the experiments [43].

4.6.1. RD53A Readout Chip

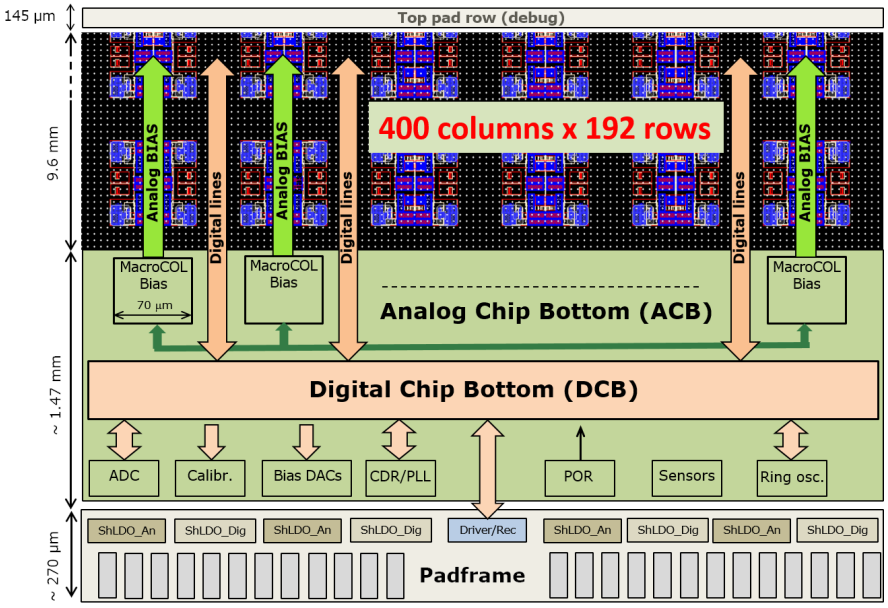


Figure 4.16.: RD53A floorplan, functional view [44].

The functional floorplan of the RD53A is shown in Figure 4.16. The chip is 20 mm in width and 11.6 mm in height with a pixel matrix of 400×192 pixels. The bottom of the chip contains the analog and digital circuitry for biasing, configuration, and readout. The lower edge of the chip contains a row of pads for wirebonding which provide all electrical connections.

The RD53A contains three different pixel frontend types, namely the *synchronous*, *linear*, and *differential* frontends which are arranged on the chip as shown in Figure 4.17. This allows evaluating the performance of the different designs on the same chip.

The pixel matrix is split up into 8×8 pixels making up a pixel *core*, which is synthesised as one digital circuit. Four analog pixel frontends each are grouped together and surrounded by the digital logic of the pixel cores (dubbed *analog islands in digital sea*).

The cores provide the digital configuration to the analog frontends and receive the digital outputs from the frontends for processing. Two different core flavours are implemented on the RD53A with different tradeoffs in terms of data storage and readout.

The RD53A is controlled via a single 160 Mbit/s link from which also all clocks on the chip are derived. Data output is provided on up to four links operating at up to 1.28 Gbit/s. Data is encoded in a custom Aurora 64b66b format. The RD53A supports trickle configuration and can be configured continuously during operation by constantly writing the configuration registers. This avoids the need for single event upset hard configuration registers [44].

The chip is designed to be powered serially with integrated regulators, in which case several frontends can be connected into a chain that is supplied with a constant current. This reduces the power losses in the cables and allows reducing the material compared to a parallel powered system. For testing purposes, the regulators on the RD53A can be bypassed and the voltages can be supplied directly.

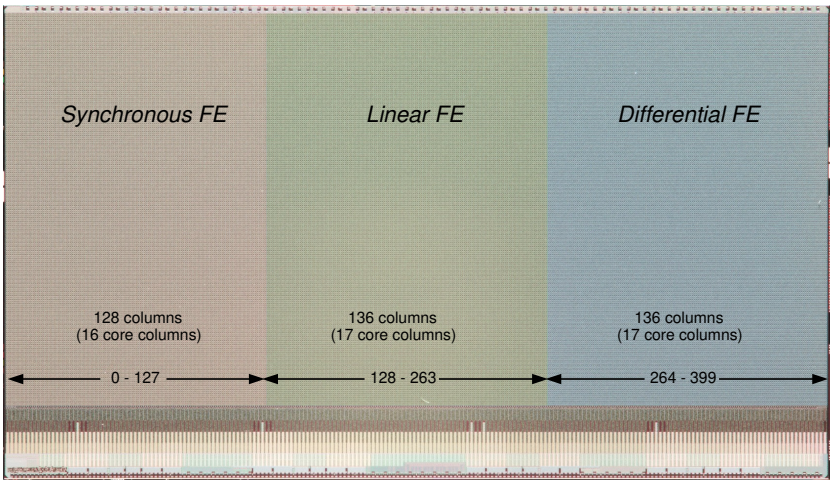


Figure 4.17.: Arrangement of front end flavours in RD53A. The pixel column number range of each flavour is shown along the bottom [44].

4.6.2. RD53B Readout Chips

After showing the feasibility of the design with the RD53A prototype, the RD53B is intended as a common concept and basis for the full-size readout chips that meet the requirements for the high-luminosity upgrades of the ATLAS and CMS pixel detectors. The pixel matrix is expanded to 400×384 pixels for ATLAS, while CMS requires a 432×336 pixel matrix. The pre-production chip for the ITk pixel detector is called the ITkPixV1. Table 4.4 compares the basic design parameters of the ITkPixV1 and the previous frontend chips in ATLAS.

	FE-I3	FE-I4B	RD53A	ITkPixV1
Feature size [nm]	250	130	65	
Chip Size [mm^2]	7.6×10.8	20.2×18.8	20×11.6	$\approx 20 \times 20$
Pixel size [μm^2]	50×400	50×250	50×50	
Pixel matrix	18×160	80×336	400×192	400×384
Data bandwidth	40 Mbit/s	160 Mbit/s	4×1.28 Gbit/s	
Data encoding		8b10b	64b66b	

Table 4.4.: Design parameters of the frontend chips for the current and future ATLAS pixel detector [36, 44–46].

The RD53B implements a number of improvements over the RD53A, including enhancements to the serial powering regulators, clocking, a new triggering and readout scheme, new data encoding which increases the encoding efficiency by over 20%, and data merging from other chips [45].

The RD53B keeps the readout scheme of the RD53A, in which a trigger command automatically causes the data to be transmitted to the readout, and adds a new scheme that differentiates between triggering and readout. This is required by a 2-level trigger mode for ATLAS, in which not all triggers are read out. Three new input lanes operating at 320 Mbit/s or 640 Mbit/s are added. Up to four RD53B based chips can be connected together and the data from up to three slave chips connected to the input lanes is merged into the output of the master chip.

CHAPTER 5

Outer Barrel Demonstrator Readout

This chapter describes the readout scheme that was developed and implemented for the *Outer Barrel Demonstrator*, an intermediate prototype stave in the development toward the ITk pixel detector. The main work of this thesis focuses on the readout setup described in this chapter and the tests and measurements performed with it in the next chapter.

5.1. Outer Barrel Demonstrator

The Outer Barrel Demonstrator is part of an ongoing effort to build prototypes of ITk staves to test and validate various aspects such as assembly, cooling, detector control system (DCS), serial powering, and readout. This project includes different prototypes such as short and long thermal and electrical prototypes.

The Outer Barrel Demonstrator follows the mechanical structure of the outer barrel region according to the ITk TDR, but is still equipped with FE-I4 modules. It will host up to 120 FE-I4 with 60 frontends per side. Each side will be equipped with 7 quad chip modules in the flat barrel section and 16 double chip modules in the inclined section.

At the moment, only one side is loaded with 7 quad chip modules labelled BM1-7 and 13 double chip modules labelled IM1-13.

It was constructed after the short electrical prototype which is a smaller prototype equipped with 7 quad chip modules [37, 47].

Setup

The demonstrator is housed at CERN and is installed in a lightproof and isolated box that can be seen in Figure 5.1(a). On the top of the box is a motorised stage that can be used to move radioactive sources over the modules. The box can also be flushed with

dry air to control the dew point to avoid condensation at low temperatures with the CO_2 cooling.

Figure 5.1(b) shows one side of the stave loaded with inclined double chip and flat quad chip modules. The stave itself is mounted in a handling frame. Also visible are the flex cables connecting the modules to the services on the stave.

The services on the stave are connected to a cable saver board on each side, which provides the connectors to the readout, connects the high voltage lines for the sensors, power for the modules, and connects to the DCS and interlock. VHDCI (very-high-density cable interconnect) connectors and cables are used to connect the stave to the readout.

The modules are powered serially with several modules connected together in a chain. The frontends on a module are powered in parallel. Figure 5.2 shows the schematic of one serial powering chain. Each module is equipped with a *Pixel Serial Power Protection* (PSPP) chip [48, 49] as part of the DCS that monitors the module and can bypass it if necessary. A constant current is applied across the chain and a shunt regulator on the frontend stabilises the supply voltage and shunts the additional current.

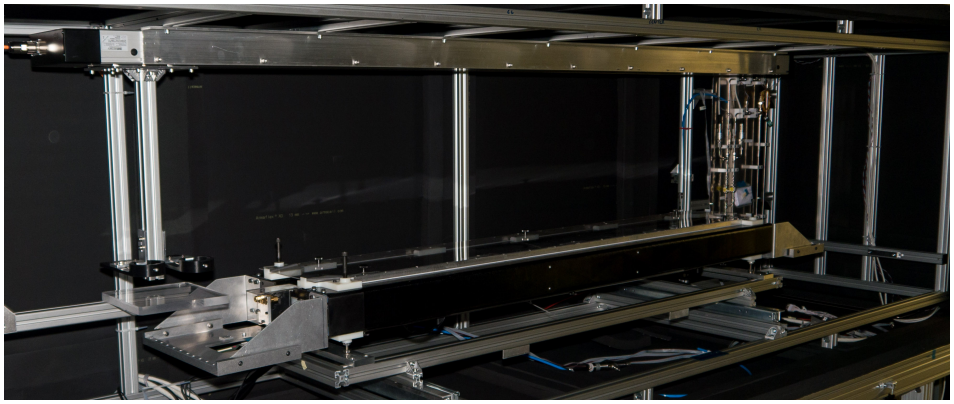
The modules are attached to cooling pipes, which are connected to a CO_2 cooling plant. The cooling temperature can be adjusted to perform measurements at different operating temperatures.

5.2. GBT Project

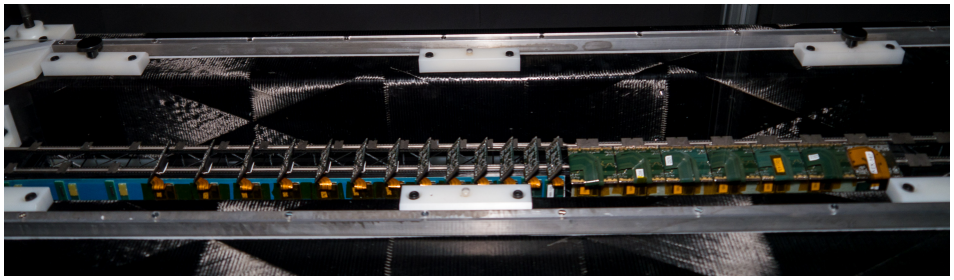
The GBTX is a radiation tolerant chip that can be used to implement multipurpose high speed (3.2 - 4.48 Gbit/s user bandwidth) bidirectional optical links for high-energy physics experiments [50] and is developed by the GBT project as part of the GBT chipset [51, 52].

Logically the link provides three "distinct" data paths for Timing and Trigger Control (TTC), Data Acquisition (DAQ) and Slow Control (SC) information. In practice, the three logical paths do not need to be physically separated and are merged on a single optical link as indicated in Figure 5.3. The aim of this architecture is to allow a single bidirectional link to be used simultaneously for data readout, trigger data, timing control distribution, and experiment slow control and monitoring. This link establishes a point-to-point, optical, bidirectional (two fibres), constant latency connection that can function with very high reliability in the harsh radiation environment typical of high energy physics experiments at LHC [50].

The GBT chipset consists of the GBTX ASIC, a transimpedance amplifier for the optical receiver (GBTIA), a laser driver (GBLD), and a slow control adapter ASIC (GBT-SCA) [50]. The typical structure of a GBT system is shown in Figure 5.3 and can be divided into the custom radiation hard on-detector part including the GBTX ASIC, connected to the off-detector part implemented using off-the-shelf components and an FPGA implementation of the GBTX [53, 54]. The radiation hard optical link is implemented with components developed by the Versatile Link project, namely the



(a) Box with demonstrator in handling frame and motorised stage.



(b) One side of the stave loaded with double and quad chip modules.

Figure 5.1.: Pictures of demonstrator setup.

Versatile Transceiver (VTRx) based on a commercial small form pluggable (SFP+) package [55, 56].

The GBTX provides up to 40 duplex serial links (e-links) to connect to frontend electronics. Each e-link consists of three differential pairs: a clock, a line transmitting signals to the frontend, and a line receiving signals from the frontend [50]. This is illustrated in Figure 5.4.

The optical link of the GBTX operates at 4.8 Gbit/s and depending on the operating mode of the GBTX, different user bandwidths are available. The default mode provides full forward error correction, but the user bandwidth can be increased at the cost of the error correction capability. With full forward error correction, the GBTX has 3.36 Gbit/s user bandwidth and 3.2 Gbit/s bandwidth for the e-links and can operate 40 e-links at 80 Mbit/s, 20 e-links at 160 Mbit/s, or 10 e-links at 320 Mbit/s.

The e-links are aggregated into a single optical link, which uses a custom format for transmission. One GBT frame is 120 bit long and is transmitted during a single 25 ns LHC bunch crossing interval, resulting in a line rate of 4.8 Gbit/s [50].

The GBTX is configured with a set of pins and configuration registers. The registers can be accessed over an I^2C bus or with reserved bits in the GBT frame.

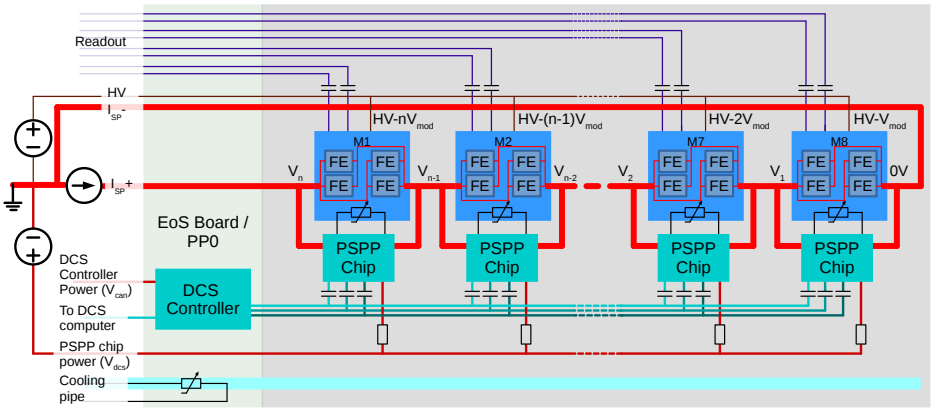


Figure 5.2.: Schematic of the Serial Powering distribution on the local support [25].

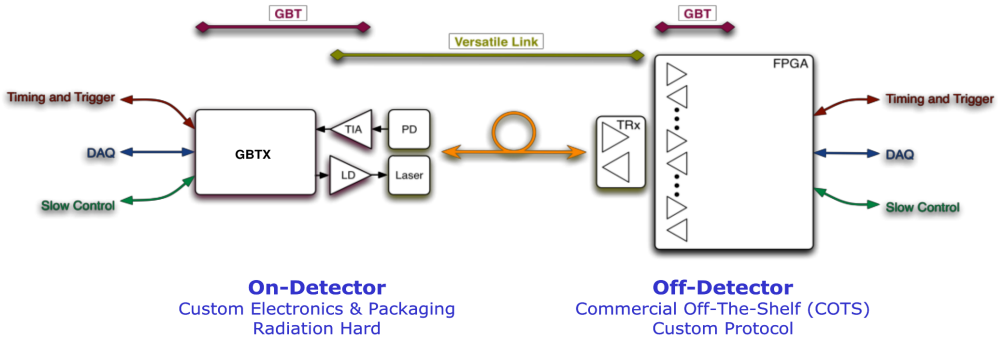


Figure 5.3.: Link architecture with the GBT chip set and the Versatile Link opto-components [50].

5.3. RCE Readout System

The SLAC RCE platform is a general purpose clustered data acquisition system implemented on a custom ATCA compliant blade, called the Cluster On Board (COB). The core of the system is the Reconfigurable Cluster Element (RCE), which is a system-on-chip design based upon the Xilinx Zynq family of FPGAs, mounted on custom COB daughter-boards. [57]

The COB consists of the ATCA board, which houses up to four Data Processing Modules (DPM) with two RCEs each, a Data Transport Module (DTM) with one RCE, and the Rear Transition Module (RTM), which provides the experiment-specific connections for data transmission. A COB with four DPMs, a DTM and RTM can be seen in Figure 5.5. The RCEs run Linux and the RCEs on the DPMs run the readout software, which also performs the data analysis and is controlled over the network.

RCE was already used as readout system for IBL stave quality assurance [58], and

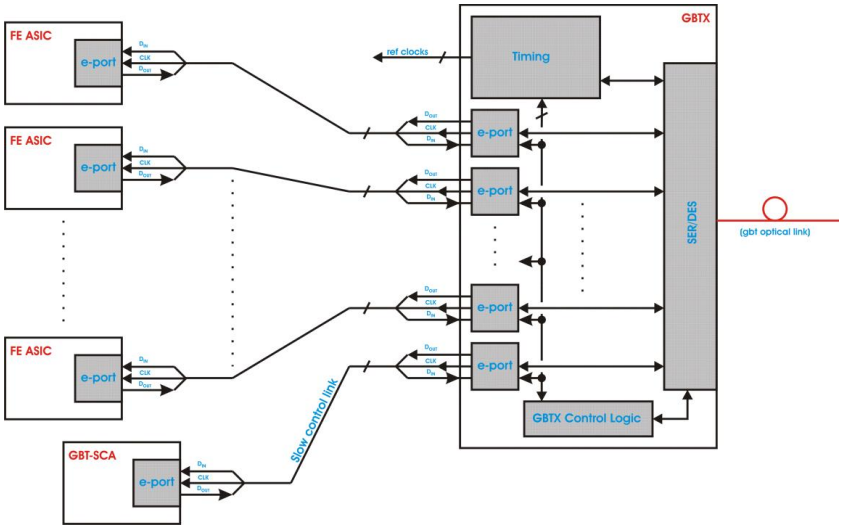


Figure 5.4.: E-link connection topology [50].

is used as readout system for other detectors and experiments, including the ATLAS Forward Proton (AFP) detector [59] and the ATLAS muon Cathode Strip Chamber (CSC) [60].

RCE-GBT is a variant of the RCE readout system that uses the FPGA implementation of the GBTX on the RCEs to interface with GBTXs on the detector-side. An RTM with SFP+ transceivers is used to connect the optical links.

5.4. Demonstrator Readout

Aside from RCE, the other readout systems used on the demonstrator are USBPix, Phase-I FELIX [61], and Yarr [62].

The goal of this thesis is to provide a readout system based on the GBTX that can read out the whole demonstrator at once. The main focus is on RCE-GBT, but other readout systems implementing the GBTX protocol such as Phase-I FELIX can use the same setup to read out the demonstrator by connecting to the optical links. This way, the setup can be reused and RCE can also serve as reference and benchmark for FELIX tests on the demonstrator.

In addition, most other readout systems used on the demonstrator are limited in the number of available channels and can therefore only read out a smaller number of frontends at the same time, making RCE an interesting option as reference readout system.

The data bandwidth from the GBTX at up to 3.2 Gbit/s is similar to the RD53A with up to 4×1.28 Gbit/s, allowing to perform readout tests at similar data rates, if only with a small number of aggregated channels.

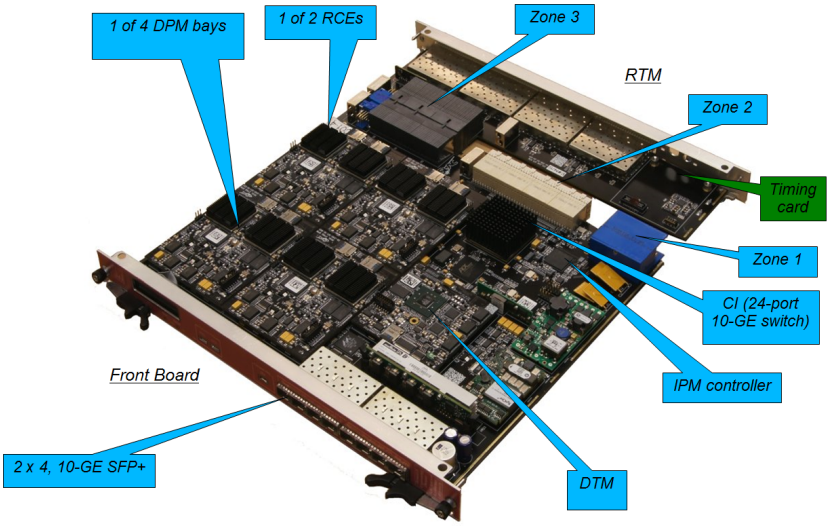


Figure 5.5.: COB equipped with 4 DPMs and a DTM. The RTM houses 16 SFP+ connectors, two for each RCE.

5.4.1. Readout Scheme

The 60 frontends on each side of the demonstrator are organized in 16 double and 7 quad-chip modules, with the same layout and connectivity on both sides. Connection to the demonstrator is provided via VHDCI connectors with 12 or 16 channels each, corresponding to four quads (16 channels), three quads (12 channels), or 8 doubles (16 channels). The pinout of the connector was chosen such that double and quad connectors are interchangeable on the readout side. Those connectors are the common interface to the demonstrator for all readout systems and adapters on the readout side have to accommodate for this [37].

Each module is connected via differential clock and command lines from the readout, as well as 2 data pairs for a double-chip and 4 data pairs to the readout for a quad-chip module. As the modules are operated in a serial powering setup, AC coupling of all signals is mandatory [37].

At 160 Mbit/s per channel, the GBTX can support 20 channels which means that at least 6 GBTX are required to read out the full demonstrator. And due to the different number of channels per connector, additional mapping is required to get the minimal number of GBTX. This is achieved by splitting the 20 channels into 16 and 4, where the 16 channels are connected directly to the VHDCI, and the 4 remaining channels are combined across 3 GBTX with a passive adapter to provide the 12 channel connector [37].

The GBTX are then connected optically to the readout. The overall readout scheme is shown in Figure 5.6. With 6 GBTX, one RCE COB with 3 DPMs is sufficient to read out the whole demonstrator.

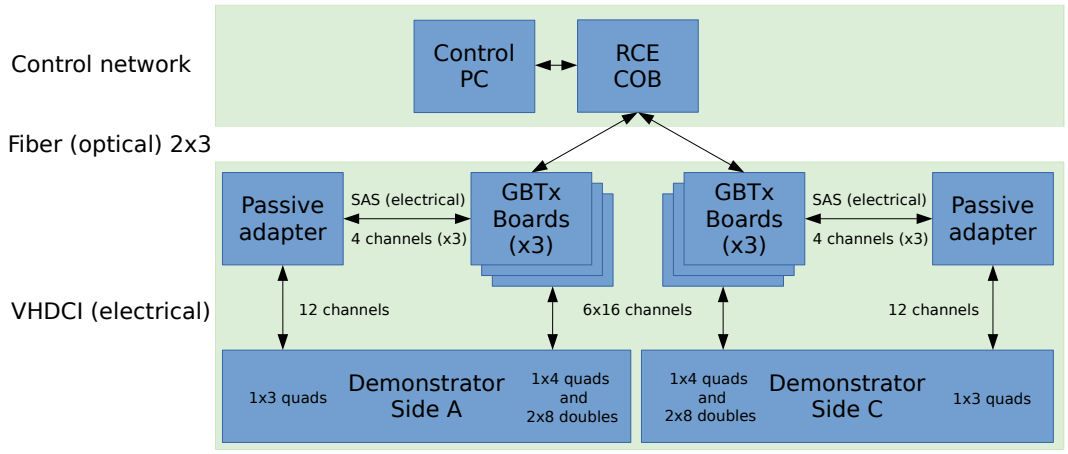


Figure 5.6.: Readout architecture for the demonstrator with RCE-GBT [37].

5.4.2. Readout Boards

To interface the demonstrator to the RCE via the GBTX, custom readout boards were developed.

The first version of the readout boards was based on the Versatile Link Demonstrator Board (VLDB), an evaluation board for the GBTX [63]. This board provides the channels on HDMI-connectors, which required additional adapters, made the setup very large and unwieldy, and caused significant signal degradation. Therefore, a new version which avoids those issues was developed. The current approach is based on GBT mezzanine boards originally developed as end-of-substructure card prototype for ITk strips. By using an existing and already working design, the prototyping is simplified and the development effort is greatly reduced [37].

The readout boards are specifically designed for the demonstrator, provide compatible VHDCI connectors and implement the mapping scheme between the 20 e-links per optical link and the 12 or 16 channel VHDCI connectors. The connection to the RCE COB uses standard commercial 10 Gbit/s SFP+ transceivers and optical fibres.

Due to the serial powering scheme from Figure 5.2, each module is at a different voltage level and signals cannot be connected directly to the GBTX. Coupling capacitors on the board block the DC component of the signals while letting the AC components pass. As this also removes the common mode voltage of the differential signals, additional resistors are added to bias the GBTX inputs to the correct voltage levels.

Different encoding schemes are used to guarantee DC-balanced signals necessary for AC-coupling. The clock signal is DC-balanced by design and the data returned from the frontends is 8b10b encoded, which is also DC-balanced. The FE-I4 commands are not DC-balanced by themselves, but can be encoded to be DC-balanced on the RCE using Manchester encoding.

Manchester encoding encodes every bit as a DC-balanced 2 bit sequence, effectively doubling the bandwidth. A 0 can be encoded as 01 and a 1 as 10 or vice versa. The

clock and command signals generated by the RCE are aligned in such a way that the frontend always samples the signal during the correct half-bit.

The first version of the carrier board after assembly and wirebonding is shown in Figure 5.7. The VHDCI cable to the demonstrator can be seen on the left, the fiber to the RCE and the power connector on the right. The connector provides 1.5 V and 3.3 V for the GBTX and the SFP+. On the bottom of the board are DIP switches connected to the configuration pins of the GBTX, status LEDs, I^2C connector and a reset button.

The assembly and wirebonding of all boards was performed locally. Figure 5.8 shows a board during inspection after soldering and wirebonding.

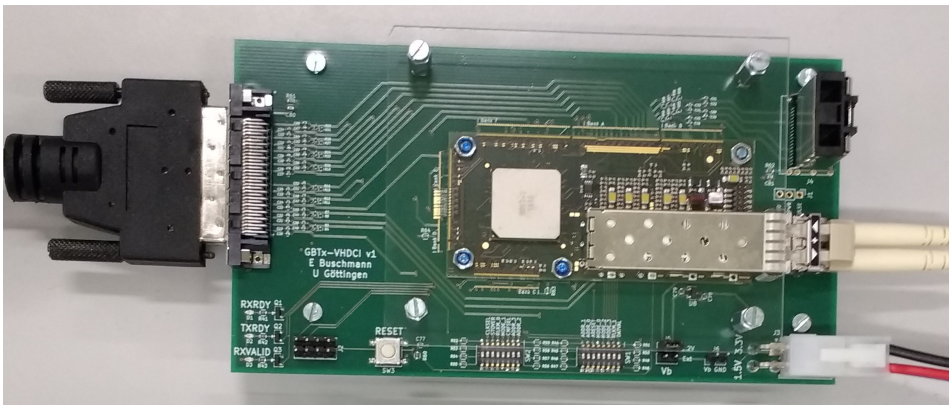


Figure 5.7.: Carrier board with mezzanine, VHDCI cable to the demonstrator on the left, and optical link to the readout on the right [37].

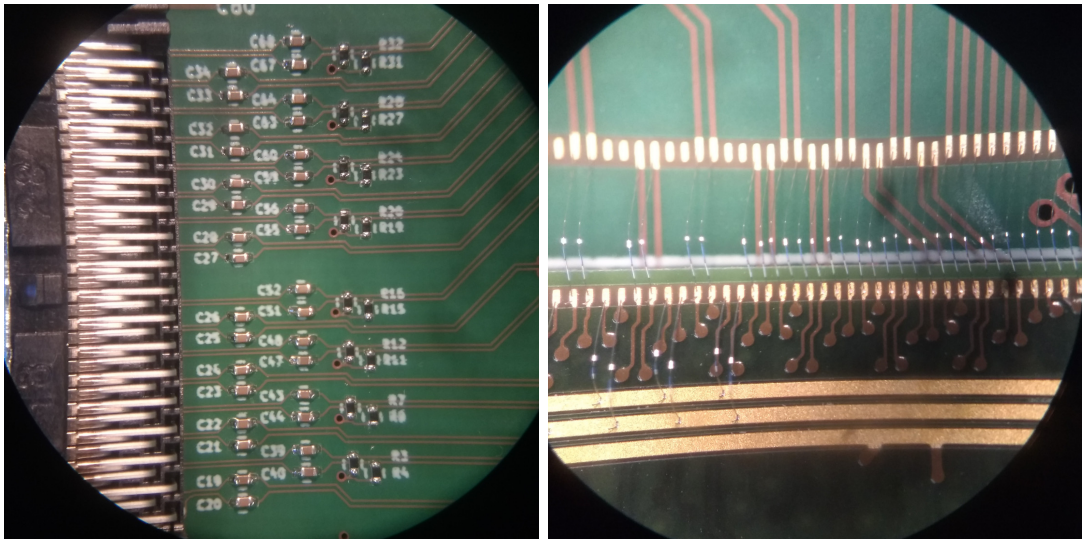
Second Version

After the readout boards were tested and the overall readout scheme was verified with the short electrical prototype (see Ref. [37]), a second version of the readout boards was designed to address some of the shortcomings of the previous version.

One of the first version boards was damaged during a later test, which is assumed to be caused by a faulty power supply. And because providing several supply voltages externally turned out to be problematic, dedicated DC-DC converters were added in the next version. The DC-DC converters generate the 1.5 V and 3.3 V rails needed for the GBTX and SFP+ from an external 12 V supply. The boards can now be powered with a simple 12 V AC-adaptor and the converters can operate over a wide voltage range, compensating for the voltage drop across the cables and providing some protection against faulty power supplies.

Voltage level shifters were added to the I^2C bus to translate between the 1.5 V signals used by the GBTX and more commonly used 3.3 V levels. This allows connecting the boards directly to an external I^2C bus.

Six more boards of the new design were assembled. Figure 5.9 shows the GBTX boards and adapter board necessary to read out one side of the demonstrator. The flat



(a) Coupling capacitors and biasing resistors. (b) Wirebonds.

Figure 5.8.: Inspection of the readout board after soldering of SMD components (a) and after wirebonding (b).

ribbon cable provides the common I^2C bus used for configuration of the GBTXs. The adapter board combines 3×4 channels from three GBTX boards together into one 12 channel VHDCI. GBTX boards and adapter are connected using mini-SAS cables.

Mini-SAS (Serial Attached SCSI) is a connector that is typically used for storage applications. It was chosen because it has 8 differential pairs, while 6 are needed to connect a quad chip module. It is designed for high-bandwidth differential signals up to several gigabit per second and cables are widely available.

The impact of the additional mini-SAS cable and adapter can be seen in the eye-diagrams in Figure 5.10, which compare a 320 MHz signal after a 1 m VHDCI cable connected directly (Figure 5.10(a)) or via the additional cable and adapter (Figure 5.10(b)). Some attenuation is visible, but the eye remains wide open.

5.4.3. Final Setup

The final system should be self-contained and operate with minimal manual intervention. The GBTX readout for each side of the demonstrator is installed in a box which is then mounted in the readout rack next to the demonstrator. The full system after assembly and installation can be seen in Figure 5.11.

Each box contains three GBTX boards in the first three slots from the left, followed by the adapter board and a Raspberry PI computer to control the powering and configuration of the GBTXs. The box is powered with a 5 V AC-adaptor for the Raspberry PI and a 12 V AC-adaptor for the GBTX boards. The VHDCI connectors are available on the front panel together with the optical links which are connected to the SFP+

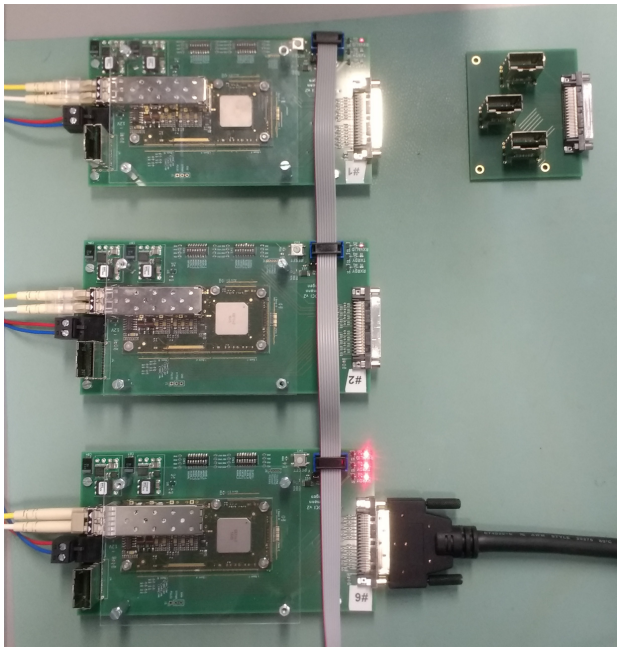
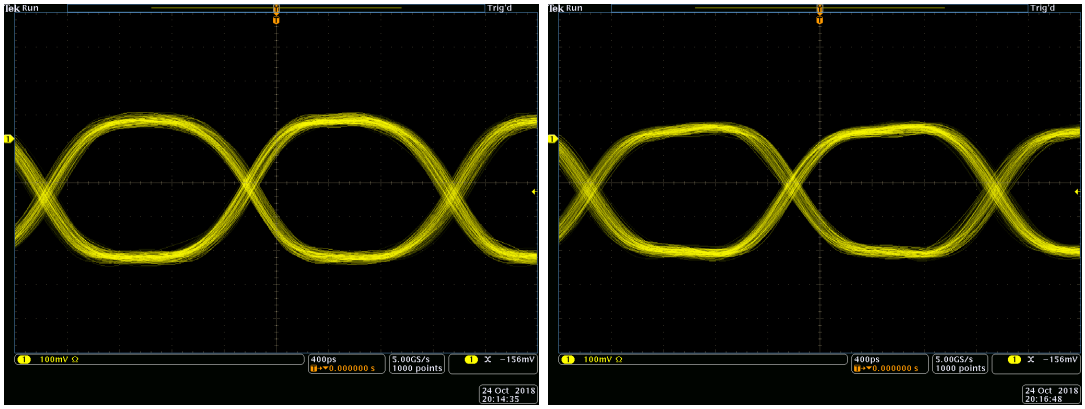


Figure 5.9.: Second version of GBTX boards and adapter necessary to read out one side of the demonstrator.

transceivers on the boards with a short fibre. This makes opening the boxes unnecessary during normal operation as all connections can be changed from the outside.

The Raspberry PI allows controlling the system remotely. It is equipped with a relay board that is connected to the 12 V lines going to the GBTX boards and can power the boards individually.

A fully equipped RCE COB is already available on-site and is now used for the demonstrator readout. With the installation of additional fibres, all GBTX are now connected to the COB.



(a) Direct connection. (b) Connection with adapter.

Figure 5.10.: Eye diagram for a 320 MHz signal after a 1 m VHDCI cable connected directly (a) and via a 50 cm mini-SAS cable with adapter (b) to the readout board.

Figure 5.11.: Picture of the readout rack next to the demonstrator with both readout boxes installed.

Control Interface

Two tools were developed to facilitate operating the GBTX setup, namely a low-level programmer for the GBTX which communicates with the chips via an I^2C bus, and a web interface that controls the programmer and the relays remotely. This is running on the Raspberry PI inside the readout boxes.

I^2C is a commonly used low-speed serial bus. It supports multiple masters and slaves and typically runs at a bitrate between 100 kbit/s and a few Mbit/s, depending on the hardware. It uses two signal lines, one for a clock signal and the other for bidirectional data transmission. Devices on the bus are identified by a 7-bit address and a master can initiate a transfer to either write to or read from a device with the corresponding address. The configuration and status registers of the GBTX can be read and written via I^2C, which allows configuring the chip, changing settings at runtime, or reading the current status.

The GBTX programmer was originally intended as an alternative to the Java configuration GUI provided by the GBT project, which is useful for manual configuration and adjustment of parameters, but cannot be automated and is especially cumbersome when operating many GBTX in parallel. The programmer is written in Rust and implements the same USB protocol also used by the Java GUI to communicate with the USB-I^2C dongle that is typically used with the GBTX. As the Raspberry PI already has an I^2C interface built-in, the programmer was extended to make use of it. This also removes the need for a special USB dongle.

The programmer is specifically designed to operate a larger number of GBTXs and offers functions such as scanning the bus for GBTXs, reading and writing of registers, uploading configuration files, and displaying the current status.

A typical output of the programmer when scanning the bus is:

```
$ gbtx -s
IDs: [1, 2, 6]
State: [pauseForConfig(5), pauseForConfig(5), pauseForConfig(5)]
```

It detects three GBTXs with the addresses 1, 2, and 6. As the setup was just switched on, the GBTX are still unconfigured and in the *pauseForConfig* state. A configuration file can then be uploaded:

```
$ gbtx -s -c gbtx.txt
IDs: [1, 2, 6]
State: [waitDESLock(10), waitDESLock(10), Idle(24)]
```

The GBTXs are now configured and the *Idle* state indicates that the GBTX is configured properly and that the optical link with the readout system is established. The other two GBTXs are not connected to the readout system and are waiting for the link to be established, indicated by the *waitDESLock* state.

To further simplify the operation of the GBTX setup, a web interface was developed that uses the programmer to control the GBTXs and can also power the GBTX boards. It is written in Python and uses the Dash framework for web applications.

The interface is shown in Figure 5.12 and is divided into three columns, one for each GBTX board. The power buttons at the top switch the boards on or off using the

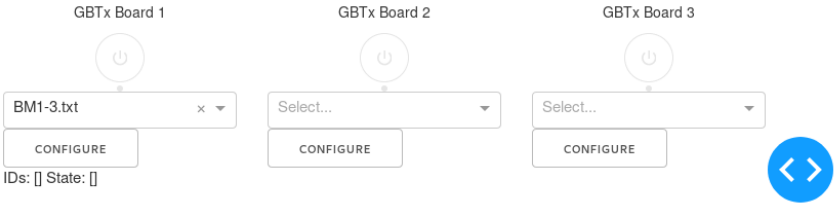


Figure 5.12.: Web interface running on the Raspberry PI.

relays and also indicate if a board is powered. Configuration files for the GBTXs can be selected from a dropdown menu and are applied using the GBTX programmer when the button is pressed. The output from the programmer is shown at the bottom and includes a list of active GBTXs and the corresponding states. This status display is refreshed periodically.

The powering is performed with an extra relay board, which has an IC with programmable outputs connected to the I^2C bus to switch the relays. The overall control and powering scheme is shown in Figure 5.13.

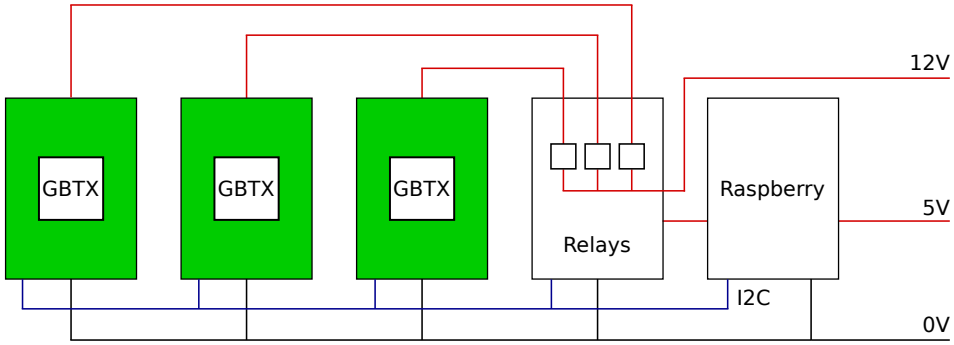


Figure 5.13.: Control and powering scheme for a GBTX readout box.

CHAPTER 6

Measurements and Results

This chapter covers the measurements and tests performed on the demonstrator for this thesis using the RCE-GBT readout system. The goals are to test the new readout boards in the full environment of the demonstrator, to verify that the RCE-GBT system can read out the demonstrator, and to perform measurements on the modules.

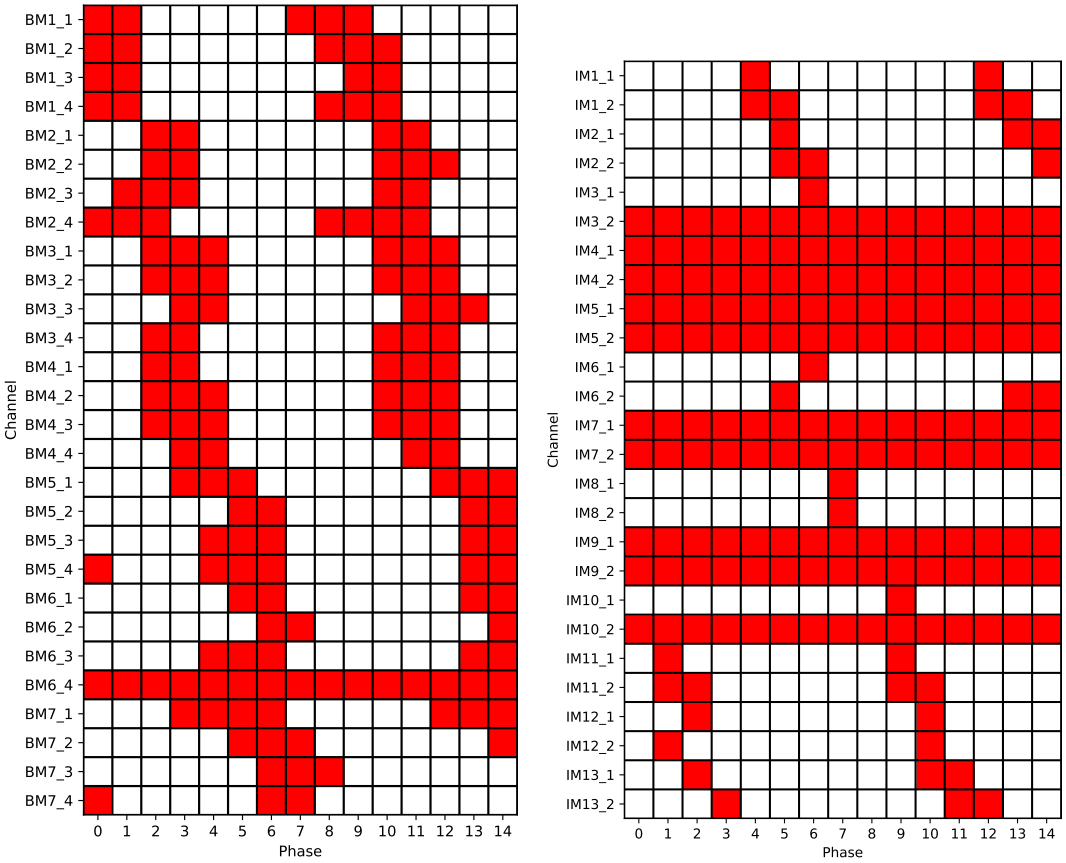
At the time of the following measurements, only one side of the demonstrator was loaded with modules. And for most of the time, only the 7 quad chip modules were operational. The tests and measurements performed on the FE-I4 modules use the scans described in Chapter 4.3.5.

6.1. Commissioning and System Test

This section summarises the tests and measurements performed during commissioning of the RCE-GBT readout for the demonstrator to verify the proper functionality of the readout chain and to test basic operation of the demonstrator setup.

6.1.1. GBTX Phases

The GBTX is the interface between the high-speed optical link to the readout system and the slower electrical links to the frontend chips. Special care has to be taken with the electrical signals to achieve stable data transmission. The clock and command signals generated by the GBT are synchronous with a fixed 90° phase shift introduced by the RCE. By matching the lengths of the signal traces, the frontend receives the signals with the correct phase relation and can sample them at the right time. This is already guaranteed by the routing of the signals on the readout boards and cables and the fixed phase shift introduced by the RCE and requires no adjustment.



(a) Quad chip modules.

(b) Double chip modules.

Figure 6.1.: Successful (white) and failing scans (red) for different phases.

	BM1	BM2	BM3	BM4	BM5	BM6	BM7
1	OK	OK	OK	OK	OK	OK	OK
2	OK	OK	OK	OK	OK	OK	OK
3	OK	OK	OK	OK	OK	OK	OK
4	OK	OK	OK	OK	OK	-	OK

(a) Quad chip modules.

	IM1	IM2	IM3	IM4	IM5	IM6	IM7	IM8	IM9	IM10	IM11	IM12	IM13
1	OK	OK	OK	-	-	OK	-	OK	bypassed	OK	No HV	No HV	No HV
2	OK	OK	-	-	-	OK	-	OK	bypassed	-	No HV	No HV	No HV

(b) Double chip modules.

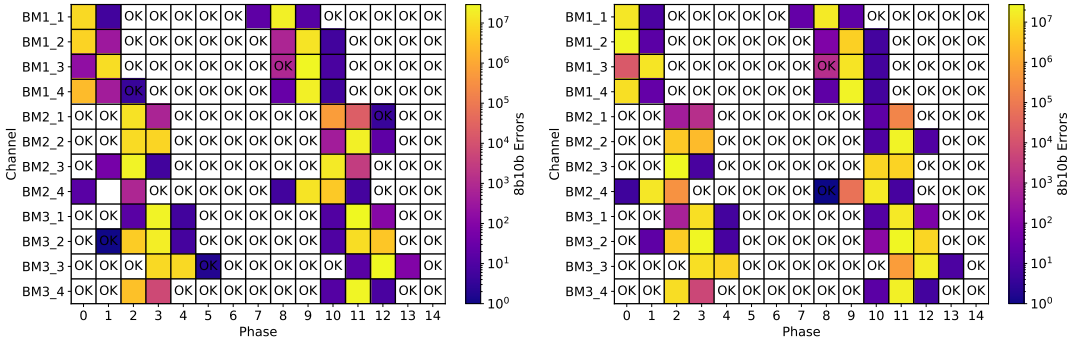
Table 6.1.: Status of frontends and communication with frontends.

The relative phase of the incoming signals is unknown and depends on the signal length to and from the frontend as well as delays introduced by the frontend. To allow for stable data transmission from the frontend chips to the readout, the GBTXs have to sample the incoming signals at the correct moment relative to the common clock. The GBTX receivers have an adjustable delay to account for the difference in phase and the GBTX offers two methods set the phases.

In automatic phase tracking mode, the GBTX uses signal transitions to determine the phase and adjusts the delay accordingly. This mode turned out to be unreliable for the demonstrator setup, probably due to signal degradation, caused many transmission errors, and was often unable to reliably lock to the phase and keep it. Instead, fixed phases were set using the static phase selection mode. In this case, the correct phases have to be determined by other means and remain fixed once the GBTX is configured.

The phases are determined by running a digital test on each frontend for all possible phase settings of the GBTX. A wrong phase causes the GBTX to sample the signal too close to a signal transition, leading to transmission errors and ultimately a failed digital test. Non-working or not communicating frontends will also result in failing scans, independent of the selected phase. Figure 6.1(a) shows a map of the channels and phases for the quad chip modules, Figure 6.1(b) for the double chip modules. Succeeding scans are marked white, failing are marked red. Each step in the phase setting corresponds to a shift of the signal by 1/8th of a clock period of the 160 MHz clock. For most channels there are two regions which allow for stable data transmission, separated by two bands with unstable data transmission. A slight slope is visible, which is assumed to be caused by the increasing signal delay due to the longer signal lines along the stave.

Out of the 54 frontends present on the stave, communication could be established with 43 of them. On the quad chip modules, only frontend BM6_4 is not transmitting data. For the dual chip modules, IM9 is bypassed by the PSPP chip because it draws too much current, and communication with IM4, 5 and 7 as well as IM3_2 and IM10_2 is not possible. IM11, 12 and 13 are operational but have no high voltage connected to the sensors. The overall status of the frontends and communication with the frontends is summarised in Table 6.1.



(a) All frontends active.

(b) Only one frontend active.

Figure 6.2.: 8b10b errors recorded during the scans. Successful scans are marked with "OK".

8b10b Errors

Because not all 10 bit sequences are valid 8b10b symbols, some transmission errors can be detected. Error counters were added to the RCE firmware to count the number of 8b10b errors on the individual channels during a measurement.

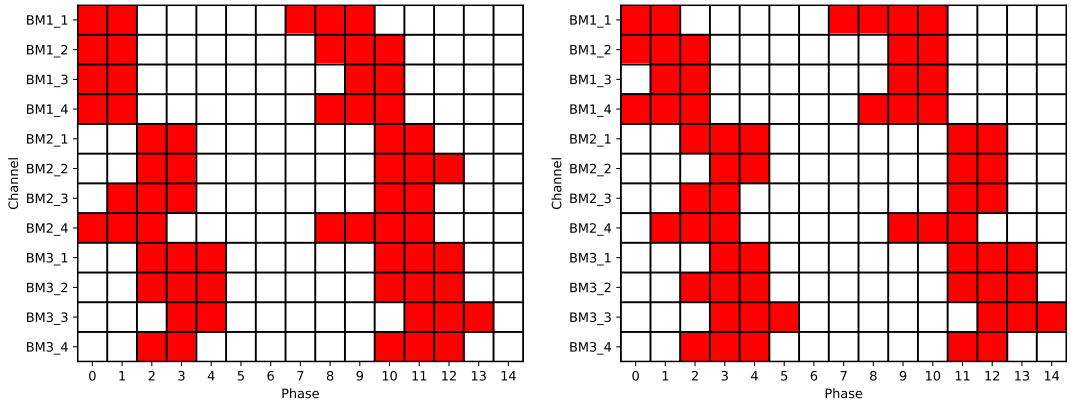
Figure 6.2 again shows a map of channels and phases, but also includes the number of recorded 8b10b errors. As expected, the failed scans coincide with transmission errors, but not all recorded transmission errors caused the scan to fail. Because no data corruption is visible in the recorded histograms, these transmission errors are assumed to have occurred during the transmission of idle words or in a part of the data format that is not analysed in a digital test.

Previous tests with the USBPix readout suffered from 8b10b errors when more than a few (≈ 4) frontends were read out in parallel, making the operation of more frontends in parallel unreliable. To test if a similar effect can be observed with the RCE-GBT readout, another comparison is performed in Figure 6.2, where the influence of one channel on the others is tested. While for the measurement in Figure 6.2(a) all frontends are configured and transmitting idle words, the frontends in Figure 6.2(b) are only enabled one at a time. This apparently has no impact on the result. This means that the crosstalk from the data lines of other frontends is not large enough to cause additional transmission errors outside of the bands.

A more rigorous approach is used in Section 6.3.2 to test data transmission under different load scenarios. This approach can also be used to determine the correct phases.

Low Temperatures

The operating temperature could also have an impact on the phases of the frontends. This is compared with the CO_2 cooling operating at 17 °C in Figure 6.3(a) and at −25 °C in Figure 6.3(b). No significant change in the phases is observed, meaning that obtaining



(a) 17 °C.

(b) −25 °C.

Figure 6.3.: Successful (white) and failing scans (red) for different phases at 17 °C and −25 °C.

the phases once is sufficient over a large range of operating temperatures.

6.1.2. Digital and Analog Test

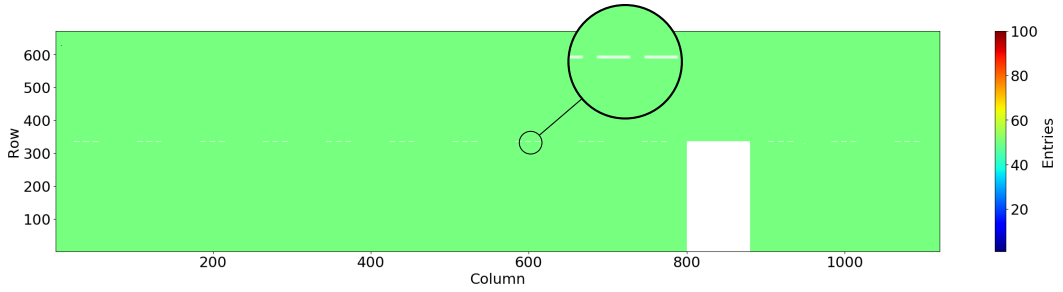
The FE-I4 injection mechanism can be used to inject a signal before or after the discriminator of a pixel cell. The digital and analog tests use this to inject a fixed number of hits into all pixels without relying on an external signal on the sensor, such as from a radioactive source. This test checks the correct operation of all frontend pixels and can identify damaged or problematic pixels.

It is also a good way to probe the operation of the readout chain, as it involves the transmission of clock and command signals from the readout via the GBTX to the frontends, the digital and analog parts of the individual frontend pixels, the on-chip readout electronics and drivers, and the transmission of data back via the GBTX to the RCE.

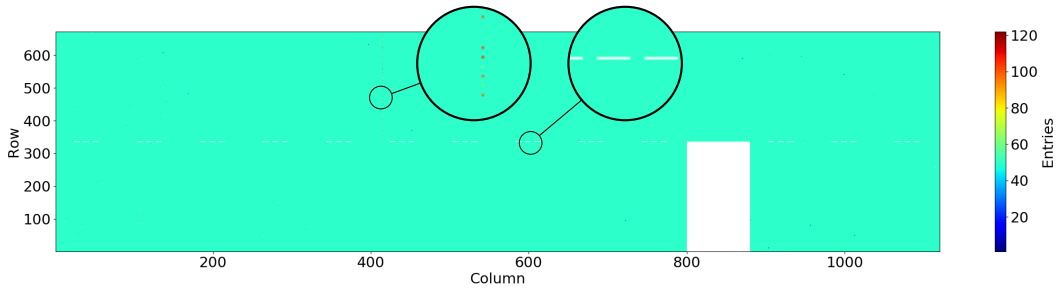
Figure 6.4(a) shows the occupancy map of a digital test, Figure 6.4(b) shows the occupancy map of an analog test for all quad modules. In both cases, a signal is injected 50 times into every pixel, and all working pixels should report 50 hits. Both tests show a region of non-working pixels on the edges between frontends on a module. One column of pixels on BM3_2 also does not show the expected number of hits during the analog test. Both regions are also shown magnified.

6.1.3. Source Measurements

After verifying the correct operation of the frontends and the readout chain with digital and analog tests, another test uses a radioactive source to generate signals in the sensor and readout chip instead of using the internal injection mechanism. A measurement is



(a) Digital test.



(b) Analog test.

Figure 6.4.: Occupancy map of digital (a) and analog test (b) on the quad modules. Some regions with problematic pixels are magnified.

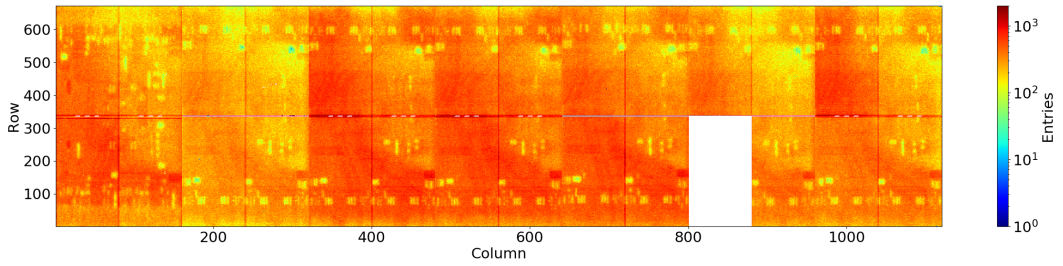
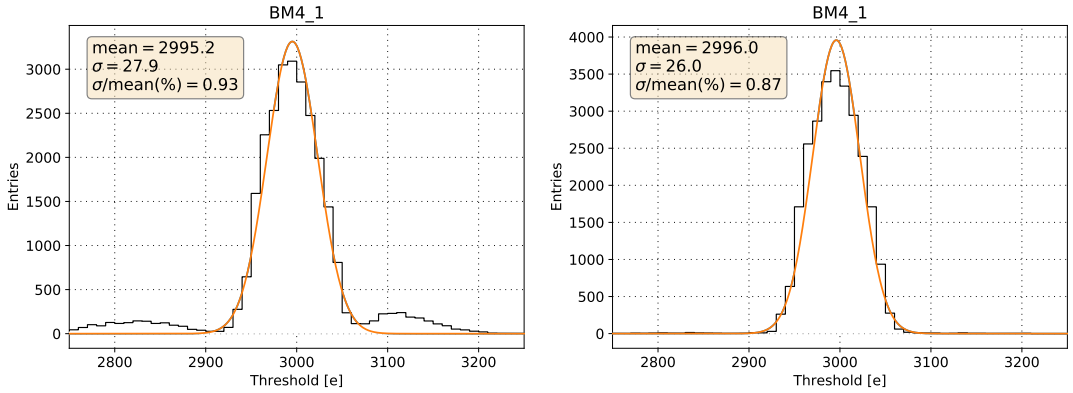


Figure 6.5.: Occupancy map of a source measurement with two ^{90}Sr sources after 30 minutes.



(a) Default procedure.

(b) Additional step.

Figure 6.6.: Threshold distribution after the default tuning procedure (a) and with an additional TDAC and FDAC tuning (b).

performed with two ^{90}Sr sources which can be moved across the stave on a motorised stage. The internal selftrigger of the FE-I4 is used to trigger the readout of hits.

Figure 6.5 shows the occupancy map for this measurement performed with the cooling at −25 °C and with a duration of 30 minutes. The material between the source and the sensor attenuates the radiation and the passive components on the module flex as well as the flex cable attaching the module to the stave flex become visible. No 8b10b errors were recorded during the measurement.

6.2. Characterisation Measurements

This section describes the characterisation measurements performed on the modules of the demonstrator, focusing on threshold measurements and tunings under different conditions.

6.2.1. Threshold and ToT Tuning

The frontends use a discriminator to suppress noise and other signals below an adjustable threshold. This threshold is adjustable and can be set globally and in addition individually for all pixels. A dedicated tuning procedure is used to adjust the threshold and time over threshold (ToT) to a uniform target value. This procedure is described in Chapter 4.3.5.

The pixels are tuned to a threshold of 3000 e and a ToT of 10 BCs for a signal of 16000 e. The tuning depends on the knowledge of the pulser DAC to voltage calibration and the values of the injection capacitances. The parameters can be measured by probing pads on the frontend chip and is usually done during frontend wafer probing. Because the calibration values are not available for most modules and measuring them on the

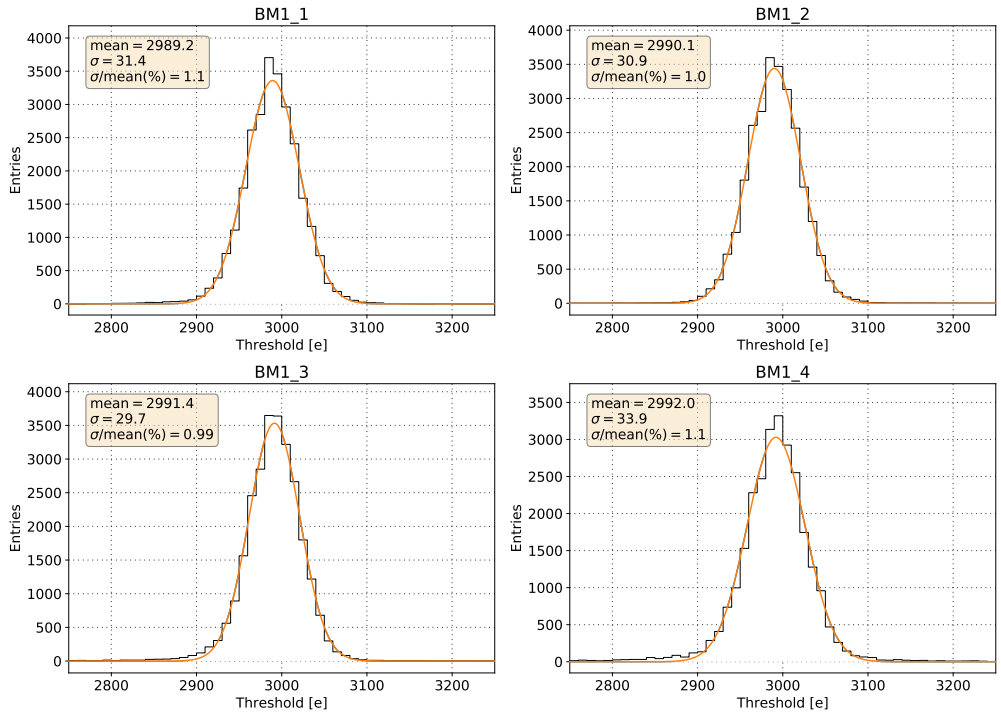


Figure 6.7.: Threshold distributions for the module BM1 after tuning to a discriminator threshold of 3000 e.

stave is not feasible, a calibration using the design values is assumed for all frontends. This applies to all measured threshold and noise values.

The tuning procedure used on the demonstrator is based on a tuning procedure already present in RCE and used for previous tests with the FE-I4. The tuned registers in order are: VthinAlt_Coarse, VthinAlt_Fine, PrmpVbpf, VthinAlt_Fine, TDAC, PrmpVbpf, FDAC, TDAC, FDAC, TDAC, FDAC. Because some of the threshold and ToT tuning steps change the ToT response by altering the threshold or vice versa, they have to be repeated several times to achieve a good tuning. A second pair of TDAC and FDAC tuning steps was added to the tuning procedure to improve the tuning on some frontends as shown in Figure 6.6.

Threshold and noise distributions of one module are presented in Figure 6.7 and 6.8. ToT distributions for the module are shown in Figure 6.9. The results for all quad chip modules are summarised in Figure 6.10. All frontends are tuned successfully to a discriminator threshold of 3000 e and most frontends exhibit a noise below 150 e with the exception of BM1 and BM7_1. The ToT response after the tuning is close to 10 BCs as expected. The detailed plots for all modules can be found in Appendix A.

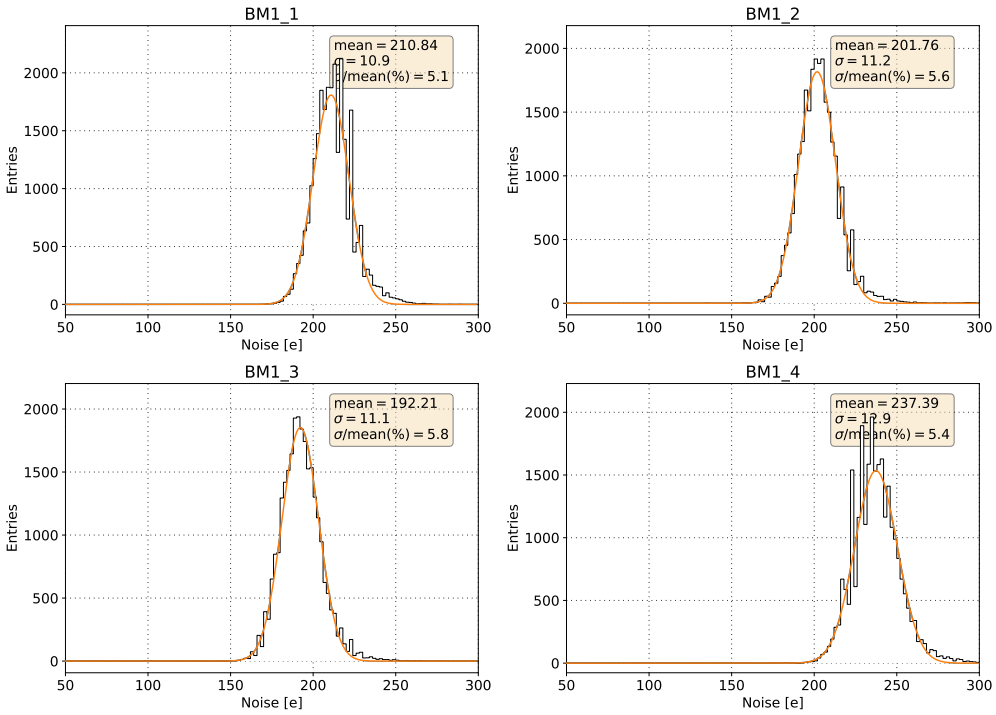


Figure 6.8.: Noise distributions for the module BM1 after tuning to a discriminator threshold of 3000 e.

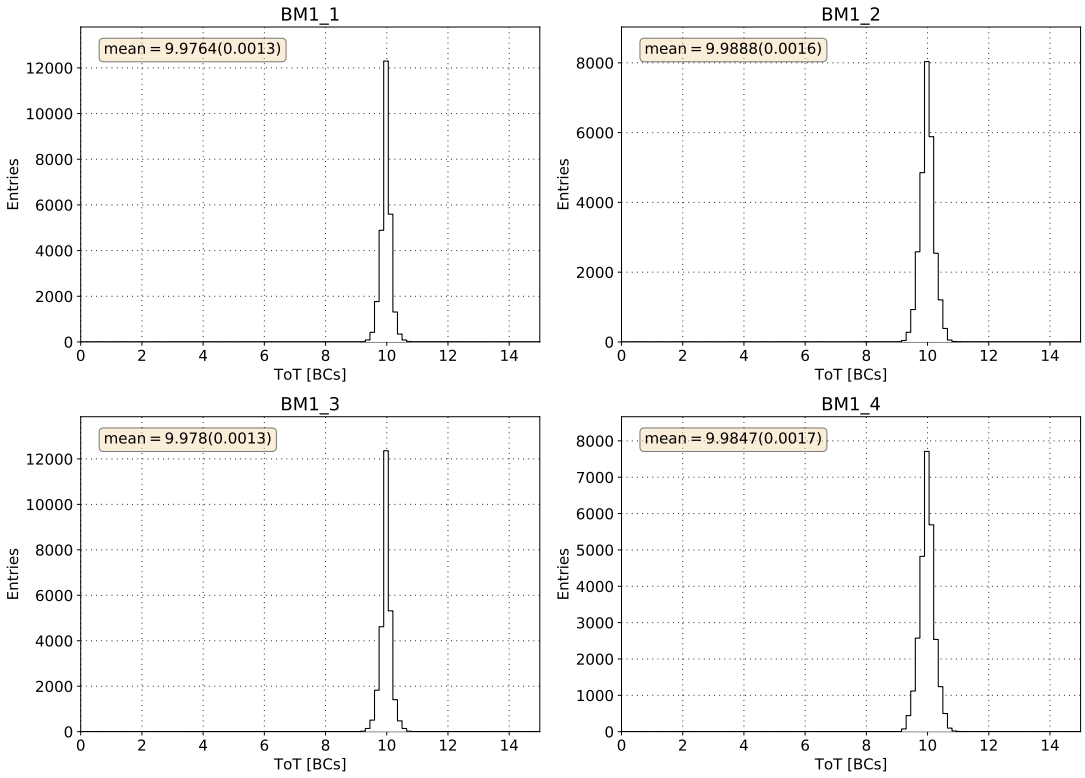


Figure 6.9.: ToT distributions for the module BM1 after tuning to a ToT response of 10 BCs for a signal of 16000 e.

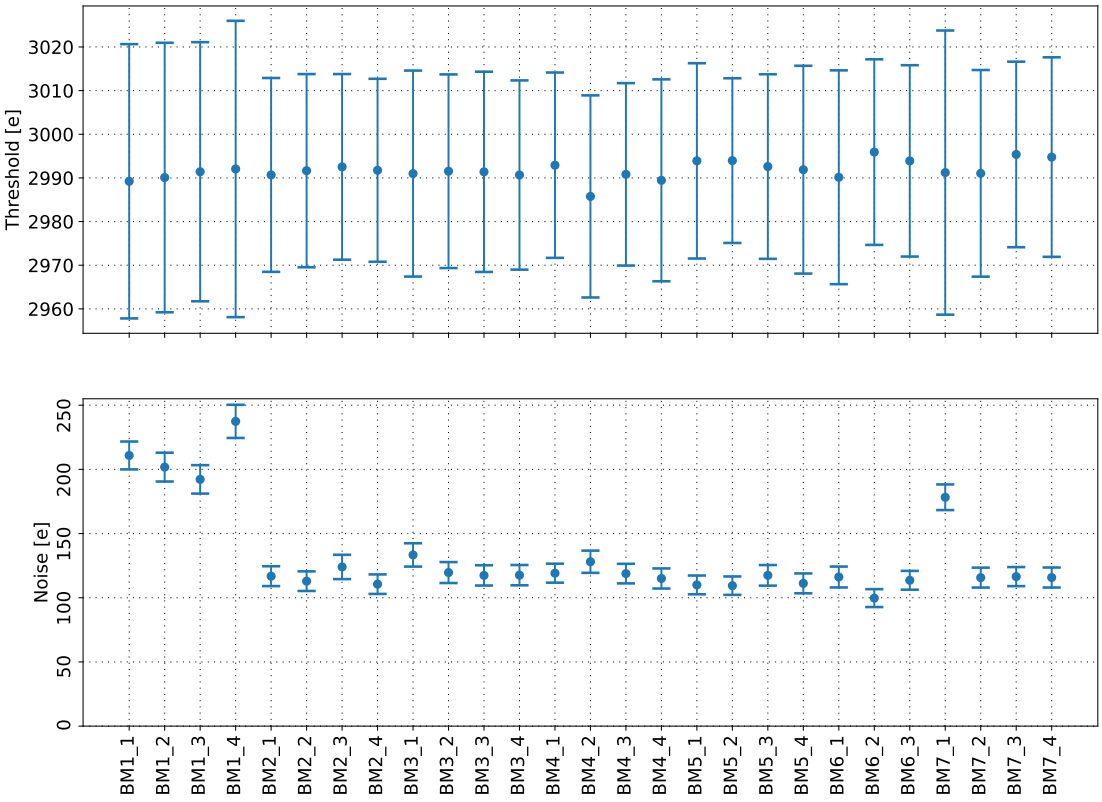


Figure 6.10.: Summary of threshold and noise distributions for all quad modules after tuning to a discriminator threshold of 3000 e. The bars show the standard deviation of the distribution.

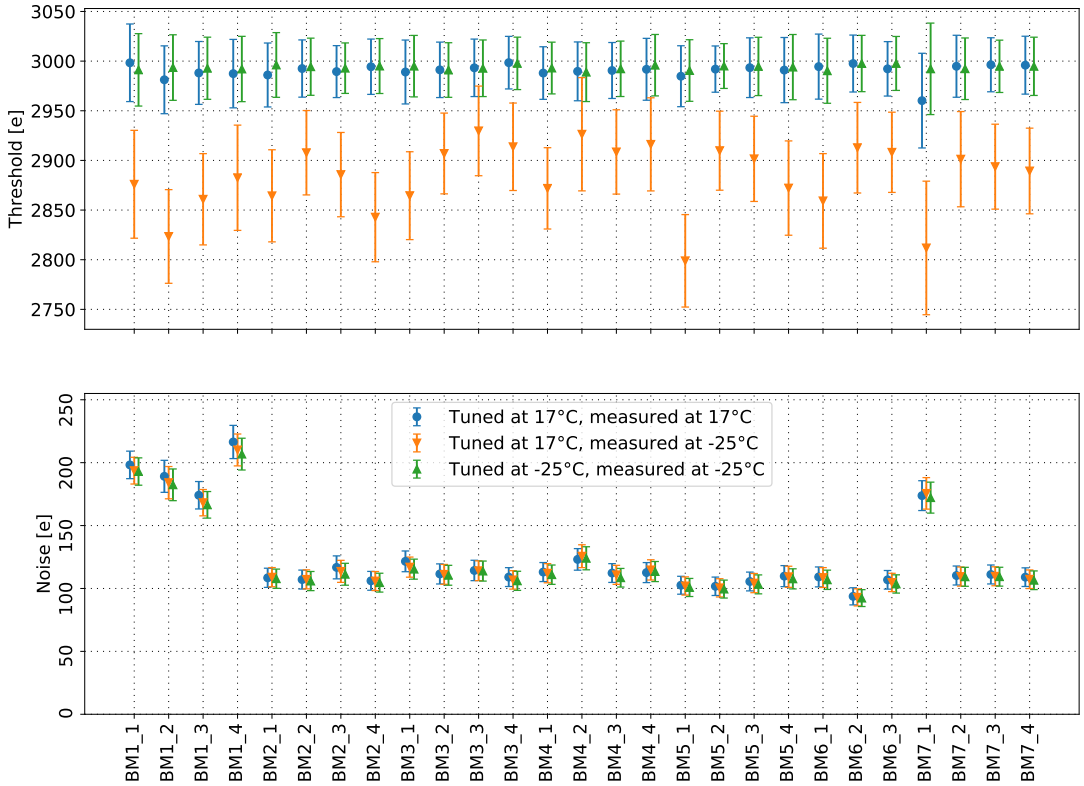


Figure 6.11.: Temperature dependence of threshold and noise distributions for a discriminator threshold of 3000 e. The bars show the standard deviation of the distribution.

6.2.2. Threshold at lower Temperatures

The previous threshold and ToT tunings were performed with the CO_2 cooling set to 17 °C, while the cooling for ITk is designed to operate below −40 °C. Different temperatures are also expected to have an impact on the threshold tunings and the noise distributions of the frontends, as was already observed for the IBL in Ref. [58].

The threshold and ToT tuning is repeated at 17 °C, the cooling temperature is then lowered to −25 °C and the thresholds are measured again. Finally, the tuning is repeated at −25 °C. The threshold and noise distributions after each step are summarised in Figure 6.11. Lowering the temperature also lowers the threshold and noise on all frontends. Repeating the tuning restores the frontends to the target threshold.

The threshold distributions are not directly comparable to Section 6.2.1 because the tunings were performed with a larger threshold step size defined by TdacVbp, leading to wider distributions.

	BM1	BM2	BM3	BM4	BM5	BM6	BM7
1	45	45	44	51	49	51	41
2	52	46	47	40	38	46	52
3	57	47	50	43	42	48	42
4	47	46	44	58	55	-	43

Table 6.2.: Lowest possible setting of VthinAlt_Fine that does not exceed the threshold of 1% noisy pixels at 17 °C. Prematurely noisy pixels on BM1 are masked.

6.2.3. Minimum Threshold

Besides operating the frontends at a fixed threshold, another interesting characteristic is the lowest achievable threshold at which a frontend is operating above a certain noise threshold. This is important for operation in a high-rate environment, as the expected signal decreases with radiation damage to the sensor and a low threshold is necessary to maintain a high efficiency [64].

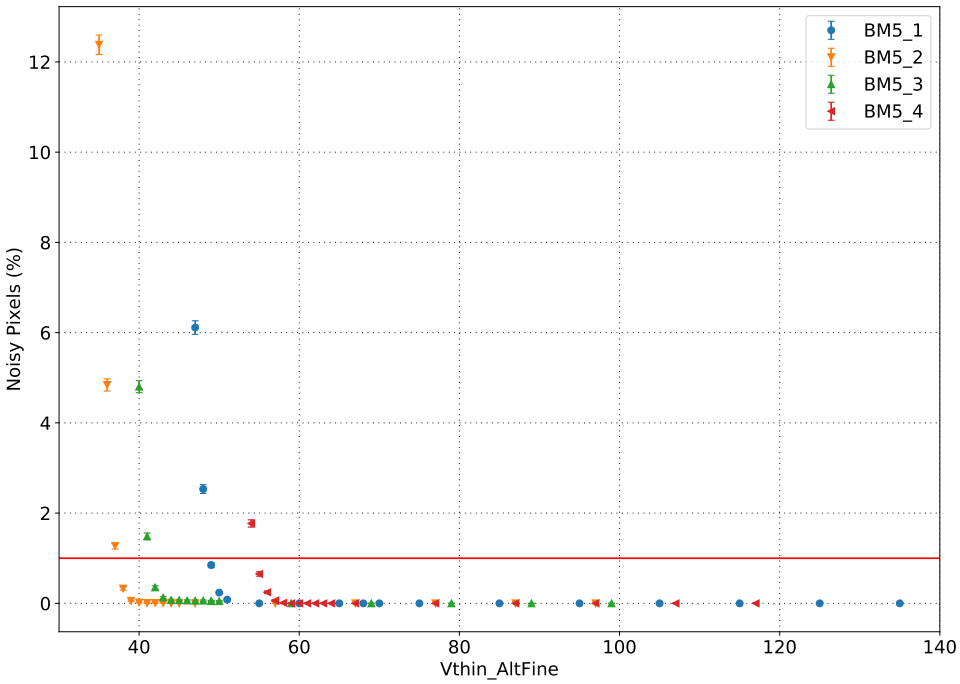
Starting from the threshold tuning obtained in Section 6.2.1, the global threshold VthinAlt_Fine is lowered and for each step, a noise scan and a threshold scan are performed. This is repeated until the fraction of noisy pixels during a noise scan exceeds 1% of the total number of pixels. A pixel is considered noisy if it exceeds one noise hit per one million triggers. A frontend is considered noisy if more than 1% of its pixels are noisy.

An example is shown in Figure 6.12(a). The number of noisy pixels remains almost constant and close to zero for most of the range of VthinAlt_Fine, but then rises exponentially and quickly exceeds the 1% threshold. The measured threshold and noise distributions for this module are shown in Figure 6.12(b) and 6.13(a).

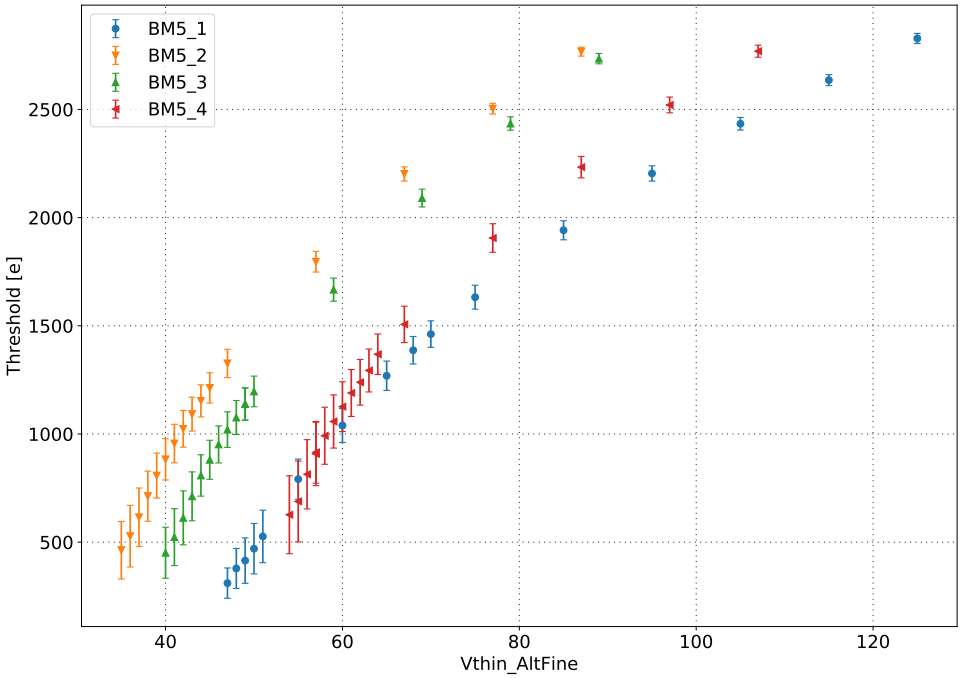
The threshold distributions become wider with lower threshold which is in part caused by lowering the global threshold without retuning the per-pixel threshold. This can also be seen in Figure 6.13(b).

The BM1 module is noisier than the others and shows an increase in noisy pixels much earlier than the other modules, as can be seen in Figure 6.14(a). Figure 6.15 shows the noise occupancy for two frontends on BM1. The noisy pixels are concentrated on the upper and lower edge of the chip. By masking the upper and lower 10 rows on all frontends on BM1, the behaviour shown in Figure 6.14(b) is achieved, showing that all the prematurely noisy pixels are indeed only present on the upper and lower edges of the chips.

The minimal thresholds for all quad modules are summarised in Table 6.2. The detailed plots for all modules can be found in Appendix B. All modules behave similarly when excluding the prematurely noisy pixels on BM1, but care has to be taken not to operate the frontends too far into the noisy low-threshold region, as the powering and operation of the frontends become unstable.

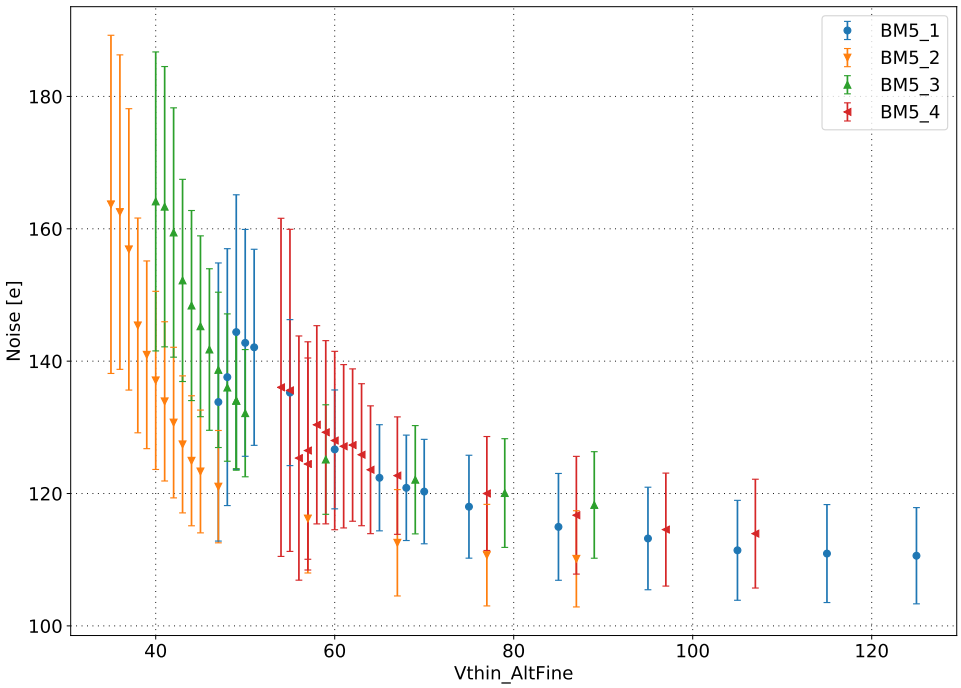


(a) BM5: Noisy pixels.

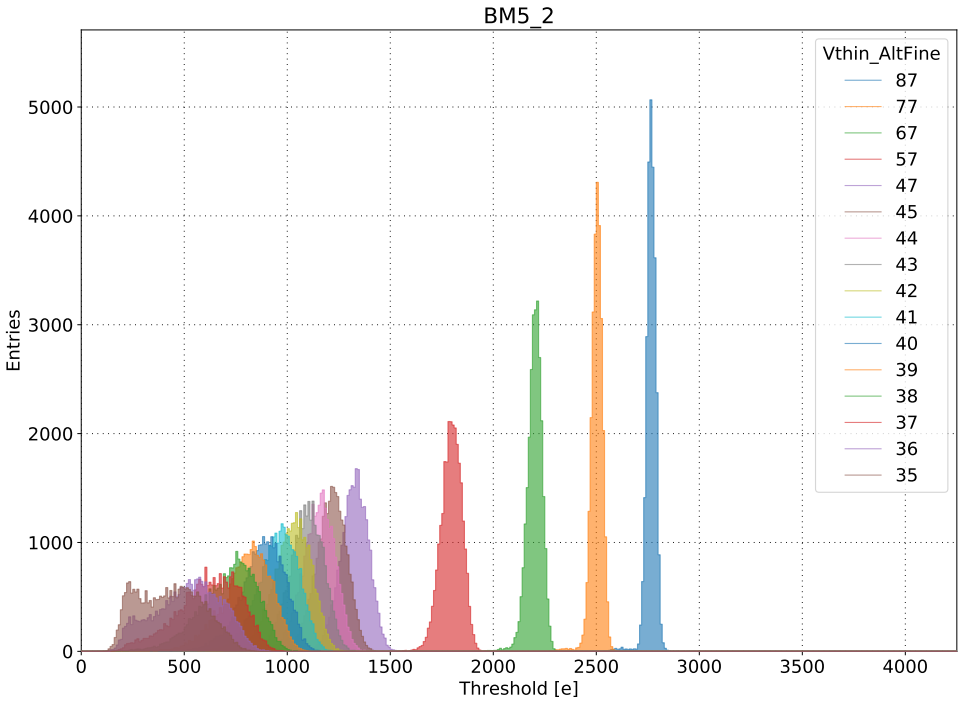


(b) BM5: Threshold.

Figure 6.12.: Fraction of noisy pixels (a) and measured threshold (b) for decreasing values of VthinAlt_Fine on BM5. The bars in (b) show the standard deviation of the distribution.

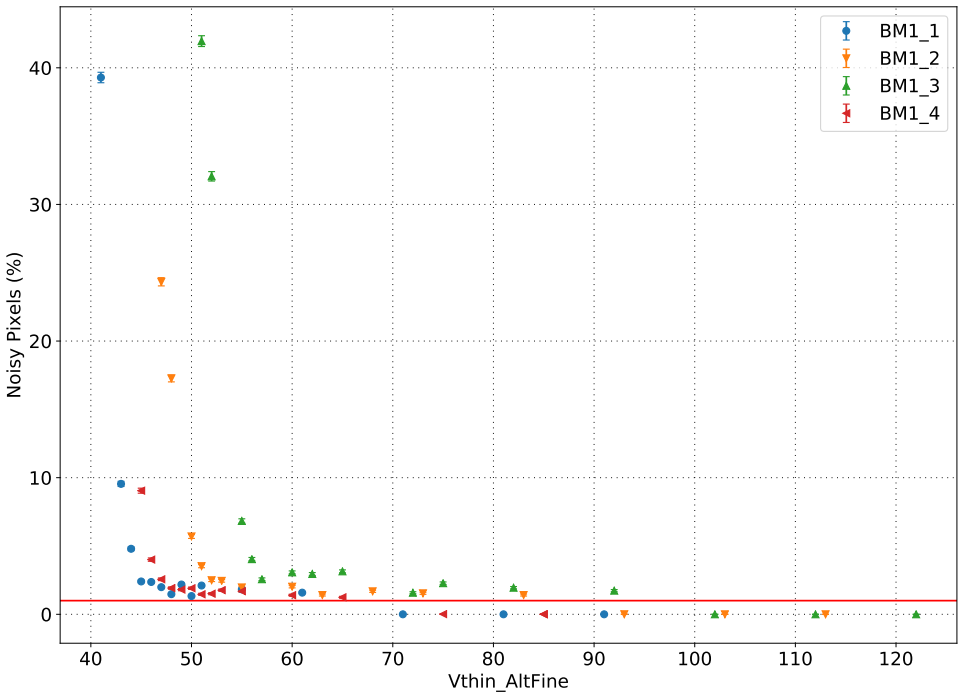


(a) BM5: Noise.

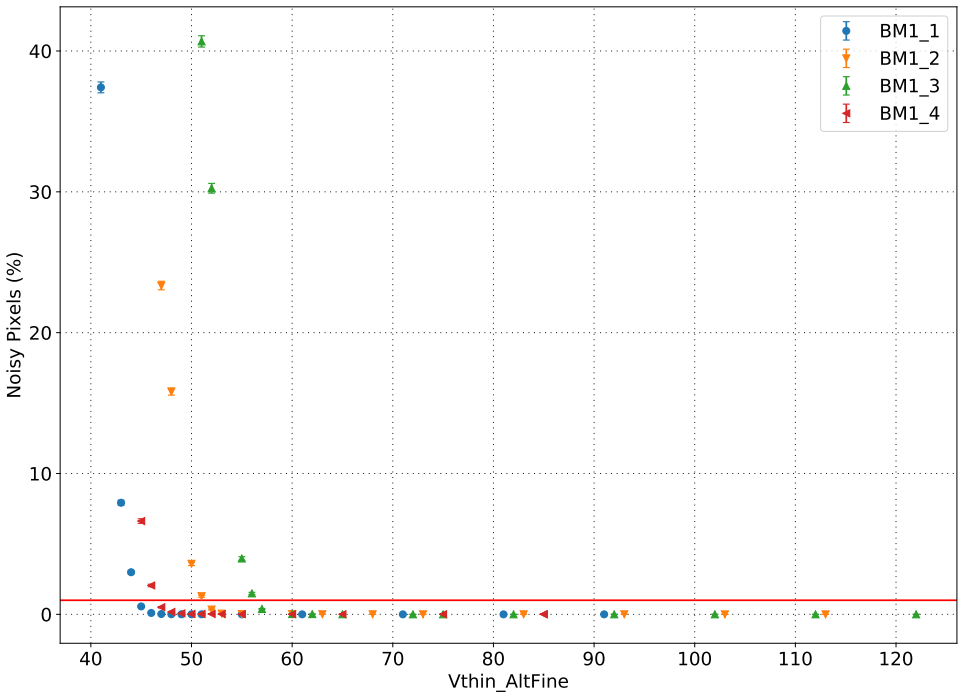


(b) BM5: Threshold.

Figure 6.13.: Measured noise (a) and threshold distributions (b) for decreasing values of VthinAlt_Fine on BM5. The bars show the standard deviation of the distribution.



(a) Prematurely noisy pixels included.



(b) Prematurely noisy pixels masked.

Figure 6.14.: Minimum threshold measurement on BM1 with prematurely noisy pixels included (a) and masked (b).

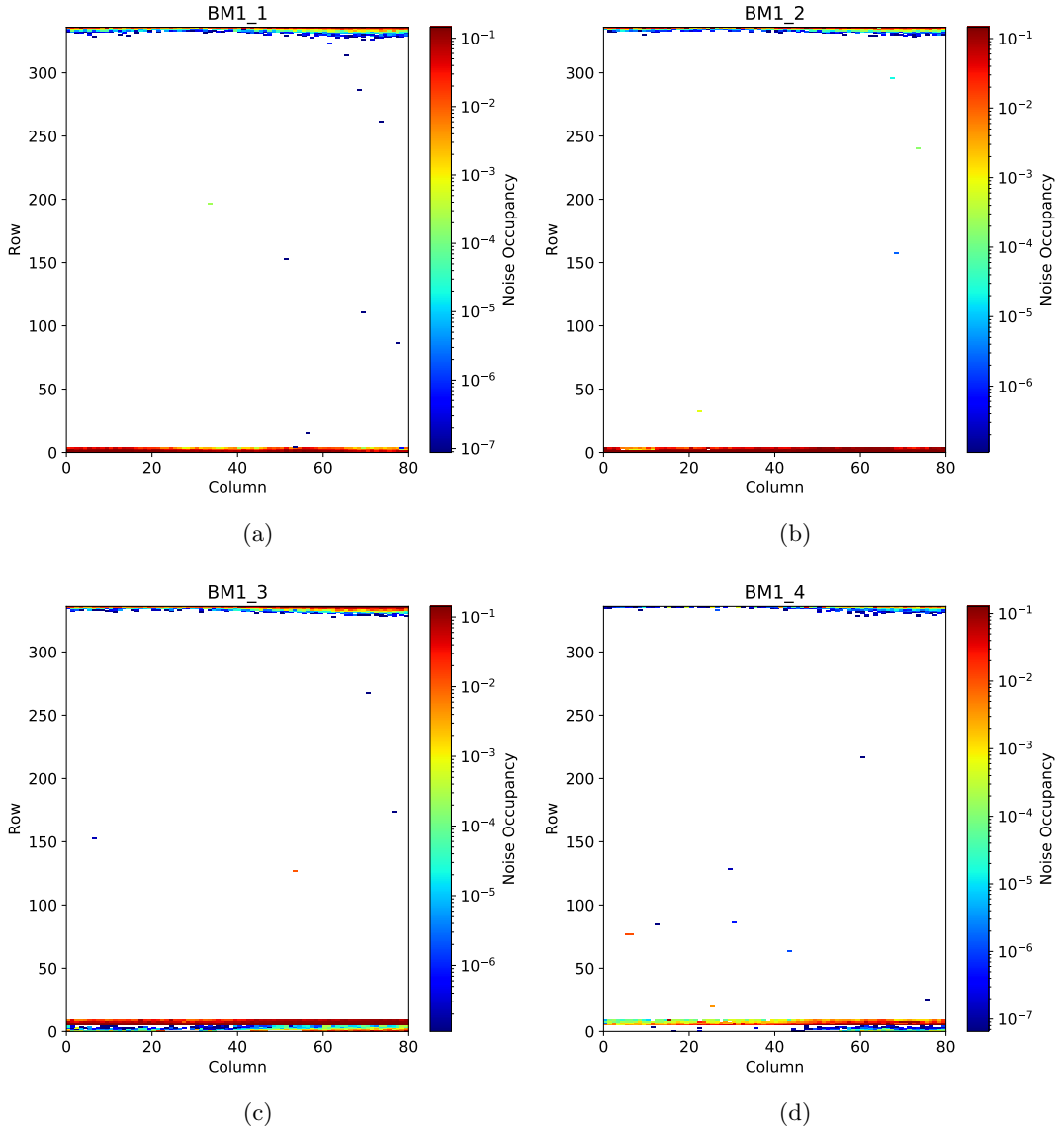


Figure 6.15.: Prematurely noisy pixels on BM1. Plotted is the number of noise hits per trigger.

6.2.4. Noise & Crosstalk

To test if the clock, command, and data signals or activity on frontends in the serial powering chain have a measurable impact on other frontends in the chain, several threshold scans are performed and the number of simultaneously enabled frontends is increased with each scan. This is summarised in Figure 6.16 for BM1_1, BM2_1, BM3_1, and BM4_1. There is no impact on the threshold and noise distributions visible.

A similar test was performed in Ref. [65] on a serially powered stave prototype which comes to the same result.

6.2.5. Double Trigger

A double trigger threshold scan consists of two interleaved threshold scans where the second scan probes the effect of the first scan on the threshold and noise distributions [58]. The scan performs two injection commands with a variable delay and each injection is followed by a trigger command after a fixed interval. This is illustrated in Figure 6.17.

Figure 6.18 shows the measured threshold and noise distributions of one module for the first and second trigger with an interval ranging from 20 to 280 bunch crossings. The first threshold remains constant over the whole range as expected, but is higher than the 3000 e target on some frontends. The second threshold starts below the first and rises to the same value, on some frontends with some overshoot. A gap is visible for delays between 210×25 ns and 240×25 ns, which is also the trigger delay of the first trigger command. An interval of 13 bunch crossings in this gap can not be used for injection, as the second injection command would overlap with the first trigger command. For intervals above 240×25 ns, the second threshold is oscillating around the first threshold, usually by over- and then undershooting the first threshold. The used interval is not large enough to see the second threshold settle on a constant value.

The noise measured on the first trigger also remains constant over the whole range. For the second trigger, it also remains roughly constant for delays below 210×25 ns with a slight drop for delays below 100×25 ns. It peaks at around 260×25 ns, which coincides with the oscillation of the threshold.

For a delay below 50×25 ns, both threshold and noise can not be measured properly on most frontends. In this case, almost all pixels return no hits on the second trigger, behaving as if the injected signal is always below the threshold. Figure 6.19(a) and 6.19(b) show the thresholds of the individual pixels and a summary of all pixels for the second trigger on BM2_1 with a delay of 40×25 ns. This shows that not all pixels start returning hits at the same delay, but some start returning hits at a lower delay than others and all pixels then gradually approach a uniform response for larger delays. This is also not random, but a clear dependence on the double-column structure of the frontend is visible. A similar effect can be seen with varying degree on the other frontends as well.

After reaching a uniform threshold distribution for delays roughly between 100×25 ns and 210×25 ns, the distribution again becomes non-uniform in the oscillating region, which is shown in Figure 6.19(c) and 6.19(d). In this case a different pattern becomes

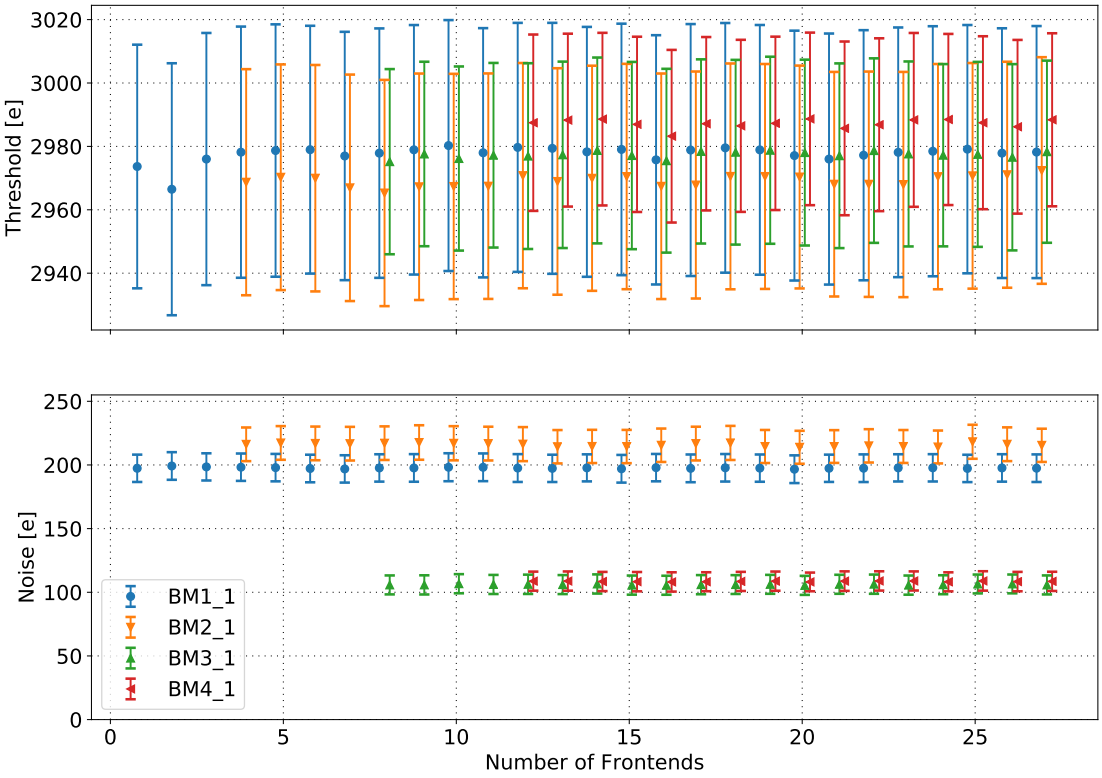


Figure 6.16.: Threshold and noise with an increasing number of frontends enabled at the same time. The bars show the standard deviation of the distribution.

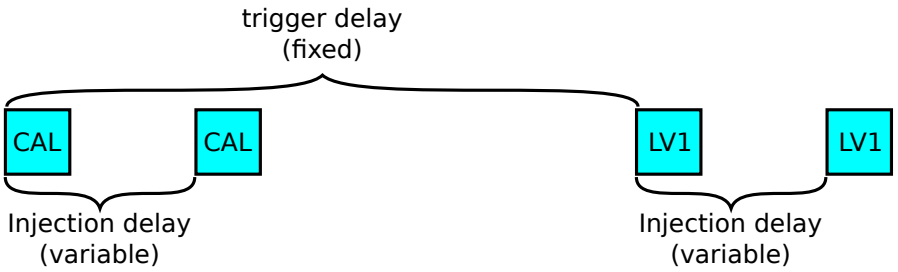
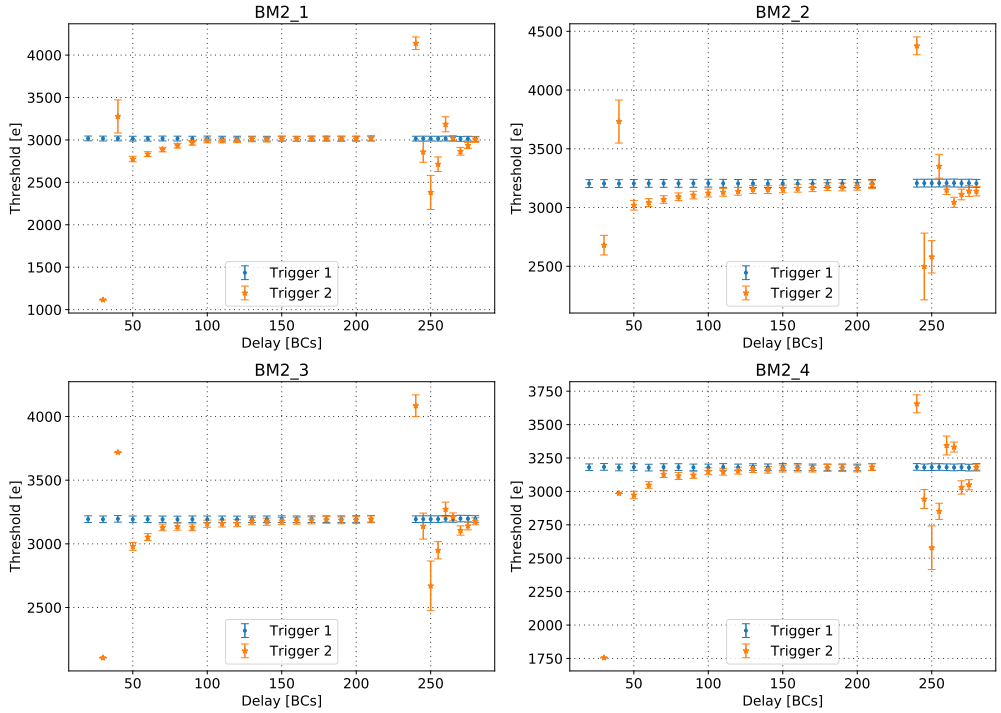
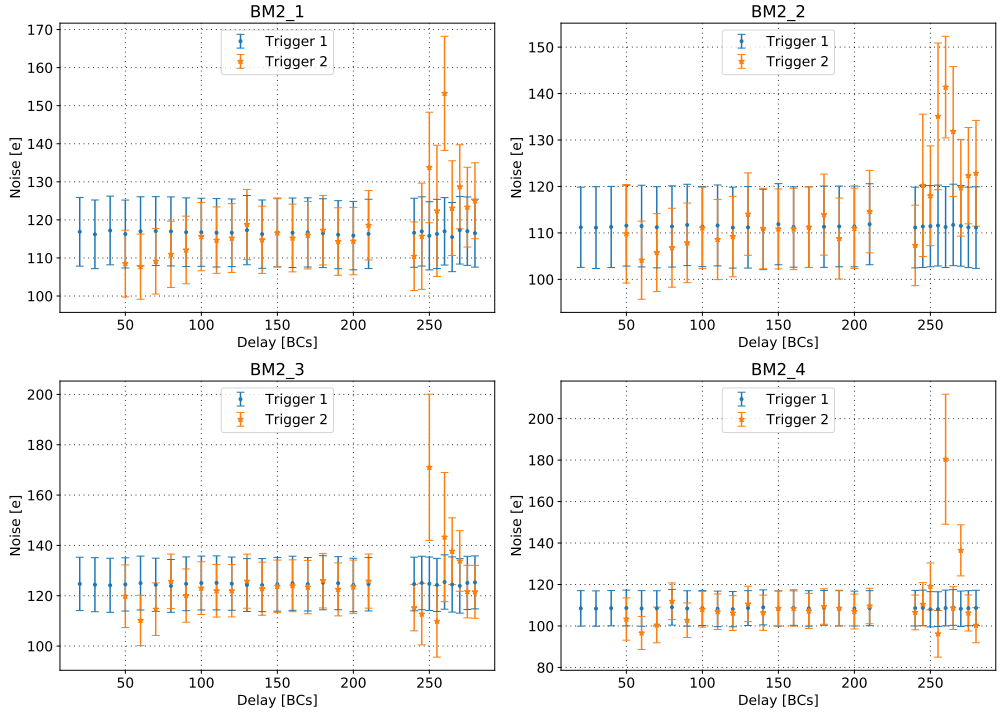


Figure 6.17.: Double trigger threshold scan.



(a) BM2: Threshold distributions.



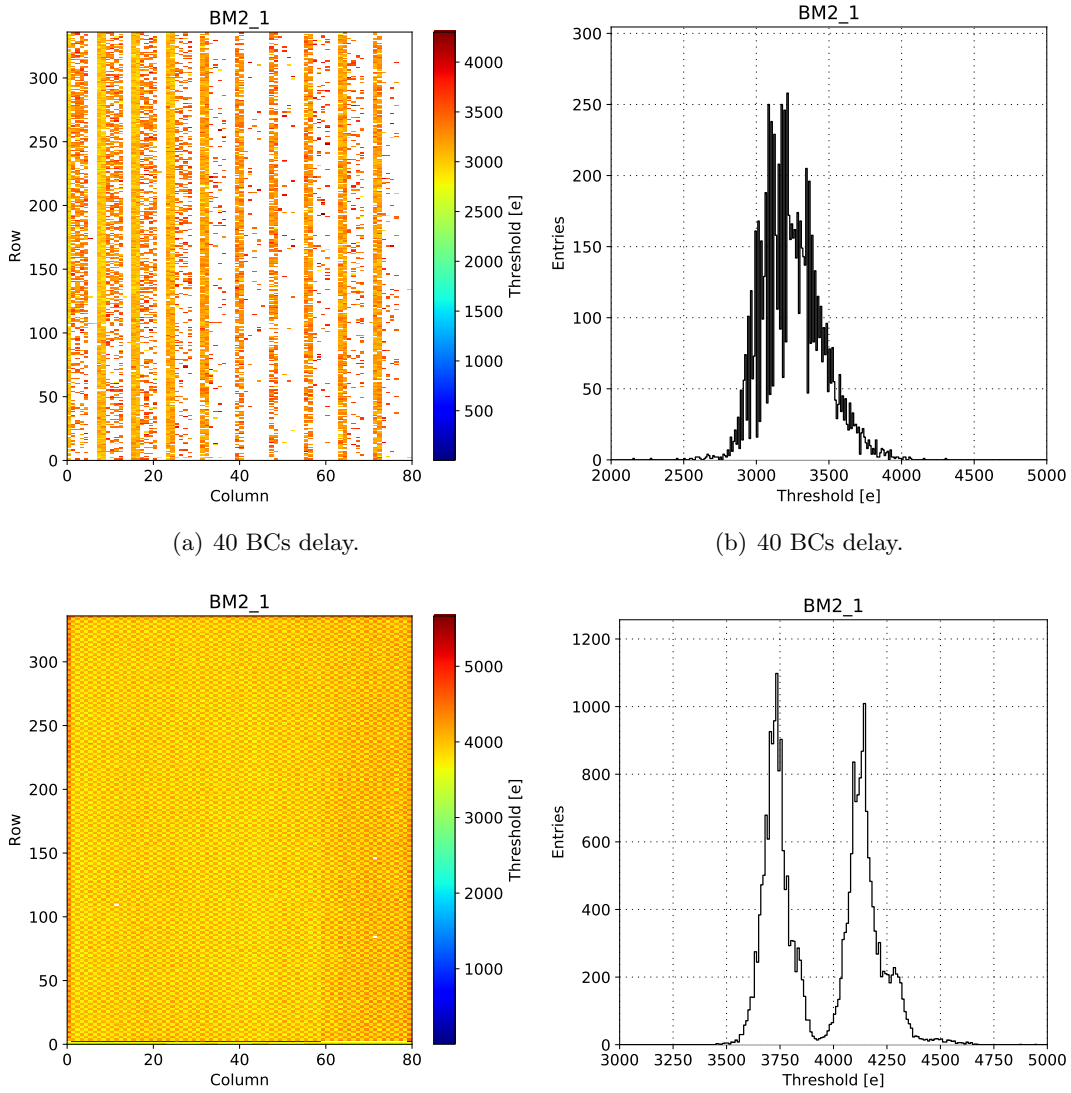
(b) BM2: Noise distributions.

Figure 6.18.: Double trigger threshold scan on BM2. The bars show the standard deviation of the distribution.

visible, where neighbouring pixels are alternating between two different thresholds.

The two regions below and above a $210 \times 25\,\text{ns}$ delay show the impact of the first injection command below $210 \times 25\,\text{ns}$, and of the first trigger command above $210 \times 25\,\text{ns}$. The detailed plots for all modules can be found in Appendix C.

Previous double trigger scans were performed for IBL staves in Ref. [58] and for a serially powered prototype in Ref. [64] and observe a similar change of the threshold for small delays. The effect is attributed to a change in some voltages such as the discriminator bias caused by a change in current consumption when a command is processed.



(a) 40 BCs delay.

(b) 40 BCs delay.

(c) 240 BCs delay.

(d) 240 BCs delay.

Figure 6.19.: Threshold distributions for the second trigger at different injection delays before (a, b) and after (c, d) the first trigger.

6.3. Performance Tests

This section describes the measurements and tests performed to test the duration of scans and the behaviour of the readout chain under different load conditions.

6.3.1. Scan Duration

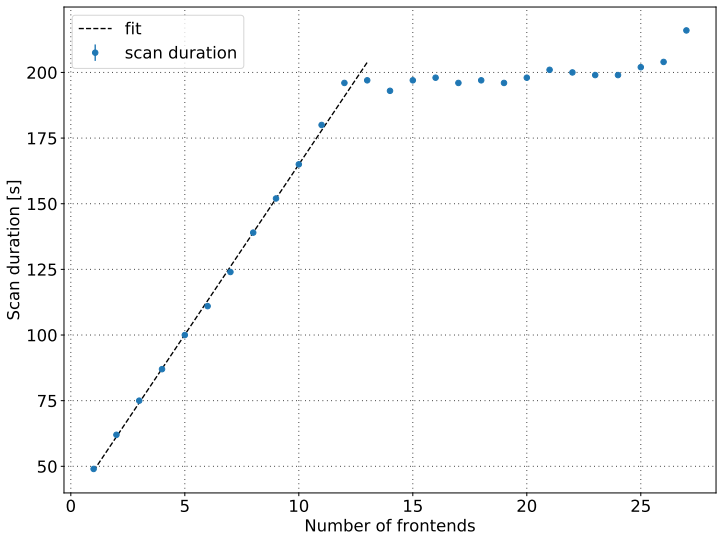


Figure 6.20.: Duration of threshold scans with an increasing number of frontends recorded with 1 second resolution.

The duration of a scan is affected by all operations performed during the scan, including for example the configuration of the frontends, changing the scan parameter before every scan step, injecting and triggering pixels, and the analysis of the data. This is an important performance measure for a readout system when operating a detector, as it determines how many measurements can be performed in the allotted time, and the scaling with the number of frontends is important especially for a large detector with many frontends and when the amount of time for calibration is limited.

The duration of several threshold scans with an increasing number of frontends is recorded in Figure 6.20. The 27 frontends are split across two RCEs with 12 frontends connected to the first and 15 frontends connected to the second RCE. It can be seen that the duration increases linearly up to 12 frontends by about 13 seconds per frontend, then plateaus, and rises again after 26 frontends.

This shows that both RCEs perform the scans independently from each other with the total scan time determined by the RCE with the most enabled frontends. The scans are also not performed completely in parallel as each additional frontend adds to the scan duration.

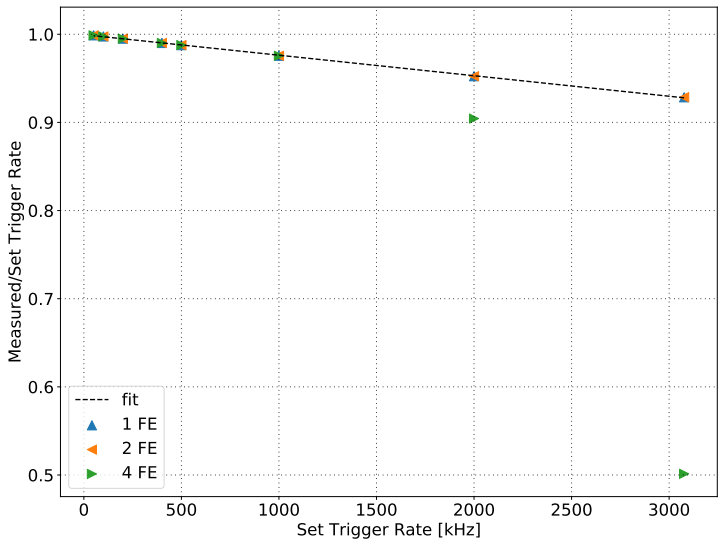


Figure 6.21.: Trigger rate set in software compared to the achieved trigger rate for different numbers of frontends.

6.3.2. Load Tests

To test the overall stability of data transmission, a load test is performed where the fraction of bandwidth of the frontends used for data transmission and idle words is varied. A noise scan was chosen as basis for this measurement because it sends triggers to the frontends at a fixed frequency and runs for a fixed duration.

The main difference to the measurement in Section 6.1.1 is that all frontends are read out at the same time, using a well defined fraction of the link bandwidth for events and a fixed time interval for the measurement. This makes the measurements under different conditions comparable and allows calculating the transmission error rate.

It was observed during measurements that the trigger rate achieved by the RCE is lower than the set trigger rate. This is assumed to be caused by the RCE delaying a trigger when unable to receive more data to avoid incomplete events. This has to be taken into account when calculating the expected data rate. Figure 6.21 compares the set trigger rate to the average trigger rate calculated from the duration of the scan and the number of issued triggers. The ratio decreases linearly from almost 100% for low trigger rates of a few kilohertz to about 93% at the maximum of 3.1 MHz when one or two frontends are enabled. With four frontends enabled, the ratio decreases faster above 1 MHz.

A very high discriminator threshold is set to suppress all hits during the scan and to generate a predictable stream of empty events. Each event then consists of the 10-bit *Start of Frame*, the 30-bit *Data Header*, and the 10-bit *End of Frame* for a total of 50 bit per event (see Chapter 4.3.3). Unused bandwidth is filled with 10-bit idle words. With this, the trigger rate necessary to saturate a 160 Mbit/s link at different trigger

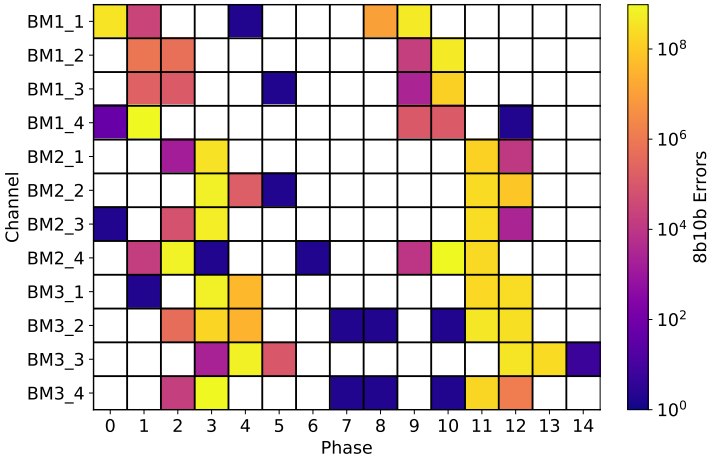


Figure 6.22.: 8b10b errors recorded at a trigger rate of 2 MHz and one minute duration for each phase setting.

multiplicities can be calculated:

Trigger mult.	Trigger interval [BCs]	Trigger rate [kHz]
1	12.5	3200
2	25	1600
4	50	800
8	100	400
16	200	200

This is verified with a single frontend by enabling a service record on the frontend that reports the number of skipped triggers. If the frontend receives triggers faster than it can transmit the data, it will drop some of the triggers and report this in the service record. The trigger interval is lowered until skipped triggers are observed. The lowest trigger intervals achieved without dropped triggers are:

Trigger mult.	Trigger interval [BCs]	Trigger rate [kHz]
2	24	≈1667
4	49	≈816
8	99	≈404
16	199	≈201

Correcting for the effectively lower trigger rates shown in Figure 6.21, the measured values match the expected rates.

The measurement was planned to use all 20 channels of the GBTX at different trigger rates, but was not completed due to problems with the CO_2 cooling plant. An intermediate measurement is shown in Figure 6.22, which uses twelve channels and runs at a trigger rate of 2 MHz. All twelve channels are set to the same phase and read out for one minute. This is repeated for all phases. The pattern is comparable to the 8b10b

measurement presented in Figure 6.2 and allows determining the optimal phases. But in addition, single 8b10b errors are also observed on some channels outside of the typical error bands.

This measurement could be improved further to detect all transmission errors. As the data transmitted by the frontends under these conditions is known beforehand, this approach could be extended to directly compare the received data with the expected patterns to detect all possible transmission errors instead of just 8b10b errors. This would however require changes to the firmware and software of the readout system to perform this comparison.

CHAPTER 7

Conclusion and Outlook

7.1. Conclusion

In this thesis, a readout scheme for the FE-I4 version of the Outer Barrel Demonstrator at CERN was developed and implemented successfully. It was developed with the goal of providing a self-contained setup that can read out the whole demonstrator and can be used for both the RCE-GBT and the FELIX readout system. This is especially important as most other readout systems for the FE-I4 are limited in the number of available channels and can not operate all frontends in parallel. This also makes the system suitable for high bandwidth readout tests and development. The development of the readout chain was focused on the development of the GBTX readout boards and the associated control interface. By using the GBTX mezzanine boards developed by DESY, the development of the carrier boards was simplified.

Extensive tests were performed on the half of the demonstrator that was loaded with modules and operational at that time. During those tests, the successful readout of the demonstrator with RCE-GBT was demonstrated and the whole readout chain, including the new GBTX boards was validated. Commissioning of the setup included the proper adjustment of all GBTX receivers and several different approaches were tested, leading to comparable results. No transmission errors were recorded even during long source measurements with radioactive sources, but the attempts to measure the transmission error rates under different load conditions were not completed due to problems with the CO_2 cooling.

The frontends were successfully tuned to a typical discriminator threshold and time over threshold target using the tuning procedure implemented by the RCE software. Some adjustments to the procedure and frontend configurations were necessary to reach a satisfying result. The minimum threshold measurement showed comparable results for all modules except one, which has pixels on the upper and lower edges of the frontends

that turn noisy at significantly higher thresholds.

The double trigger threshold measurement explored the impact that the charge injection and trigger processing has on the behaviour of the chip, observed consistently across all frontends. Similar results for small delays were seen in previous measurements for IBL (see Ref. [58]). Changing scan parameters or the scan combined with a double trigger noise scan allows studying this effect in more detail. For example, the first trigger command seems to have an impact if it is performed before the second injection. Other relevant parameters are the number of pixels injected into at the same time, or the number of consecutive triggers for one trigger command.

The RCE-GBT system is now also used as the default readout system for the demonstrator, because the previous setup was struggling with transmission errors. This made reading out the whole demonstrator at once possible and enabled many tests in the first place, especially the serial powering tests. This is an important step toward the ITk with the next generation of frontend chips. First tests with the FELIX readout system using the GBTX setup were also performed, but are not covered here. The modular setup makes it very easy to switch between readout systems and once connected, can be operated remotely.

7.2. Outlook

The demonstrator programme is still ongoing and working on prototypes for the upcoming ITk upgrade of the ATLAS detector for the HL-LHC. In the immediate future, the loading of the remaining modules onto the other half of the demonstrator is planned. This will also allow running the readout setup at full scale and perform more measurements on the full demonstrator.

Future measurements on the demonstrator should repeat the previous measurements on the full setup and could also improve on them by testing under different conditions such as the cooling temperature, study the operation with serial powering in more detail, and perform more tests on the data transmission. The results obtained with RCE-GBT can be used for comparison with FELIX and other readout systems.

In the future, a new demonstrator with RD53A frontend chips will be built. This will require a new readout and aggregation scheme when operating more than a few RD53A and could use the upcoming lpGBTX to combine frontend links. Most of the tests and measurements presented here are also possible on the RD53A, in particular studying serial powering with the improved on-chip regulators and the high transfer-rate.

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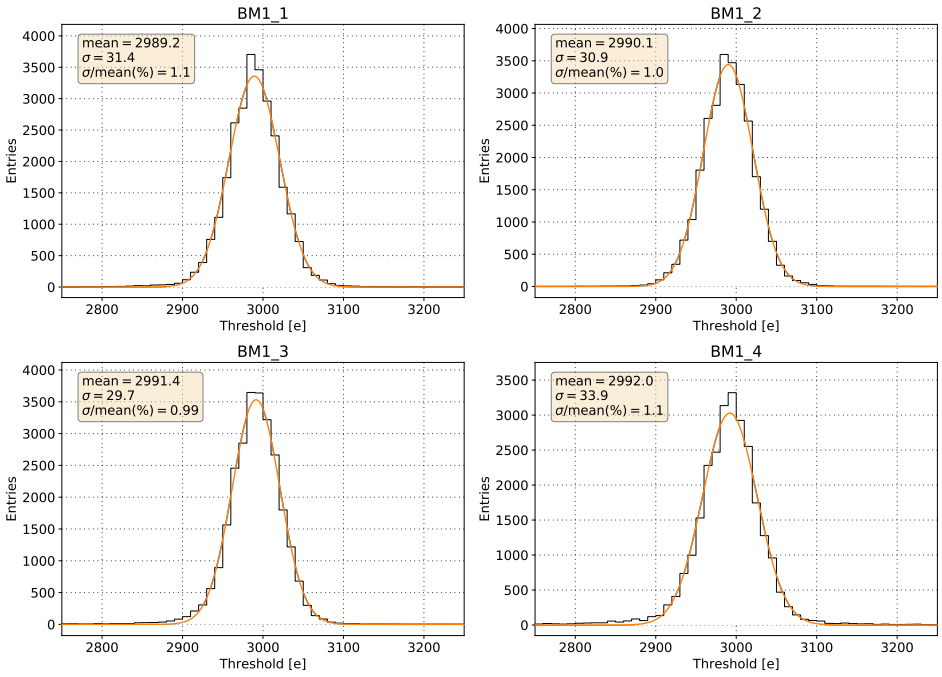
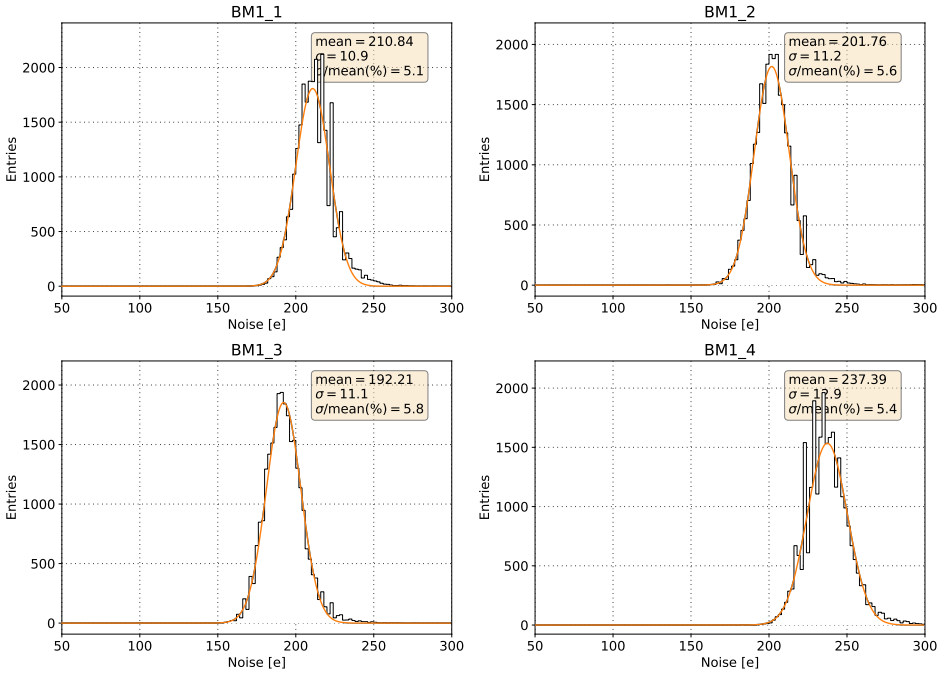
Appendices

APPENDIX A

Threshold and Noise

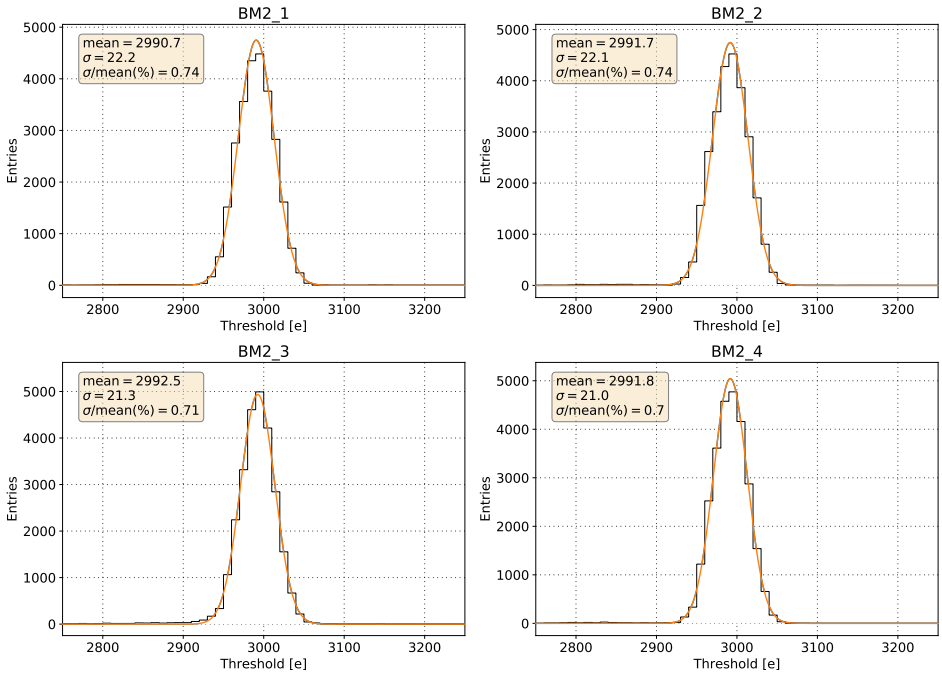


(a) BM1: Threshold.

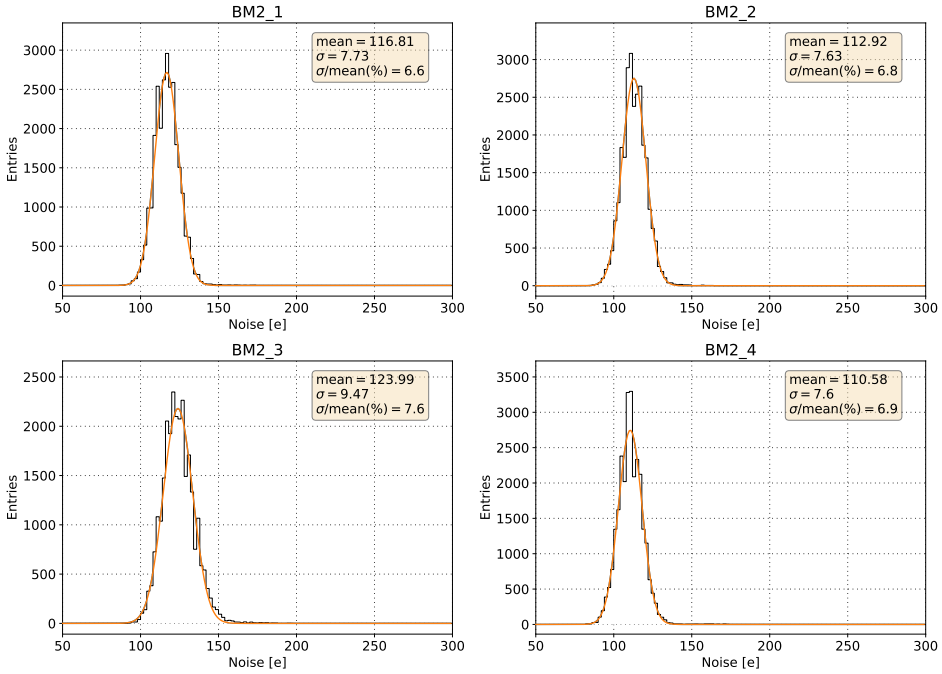


(b) BM1: Noise.

Figure A.1.: Threshold and noise distributions for the module BM1 after tuning to a discriminator threshold of 3000 e.

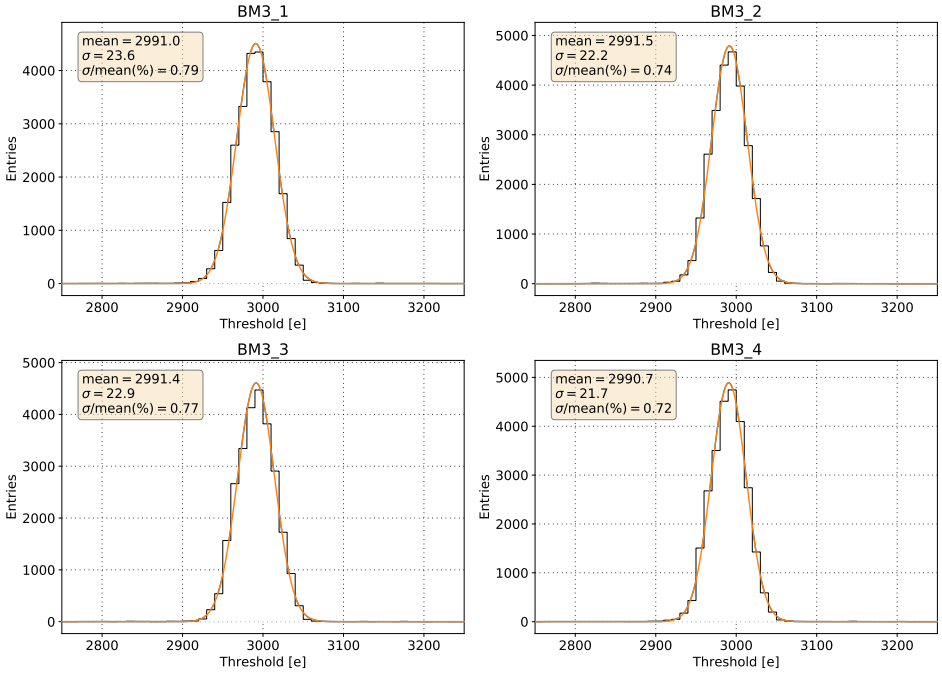


(a) BM2: Threshold.

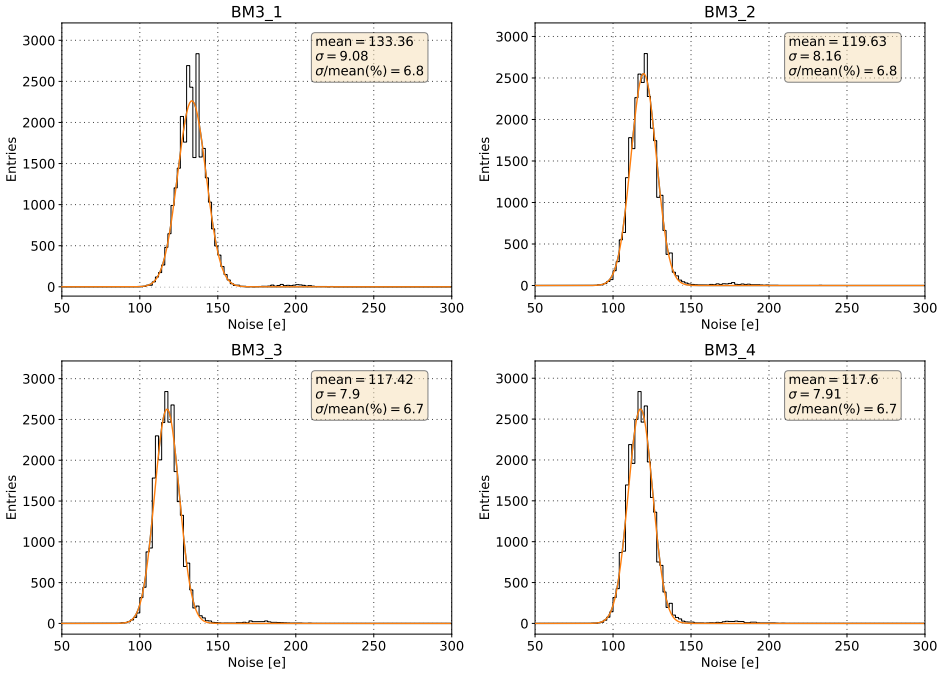


(b) BM2: Noise.

Figure A.2.: Threshold and noise distributions for the module BM2 after tuning to a discriminator threshold of 3000 e.

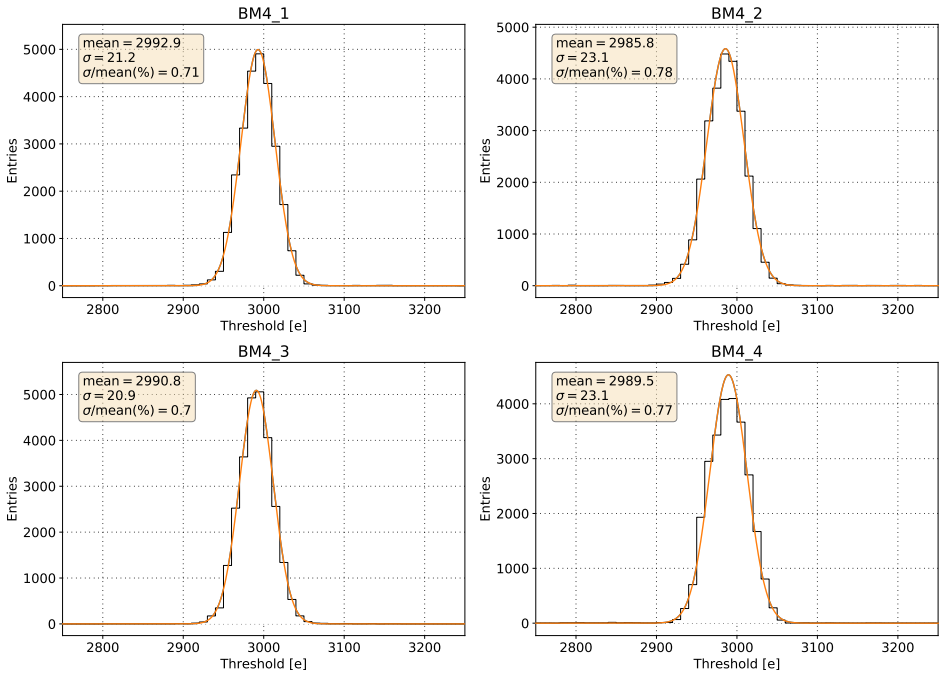


(a) BM3: Threshold.

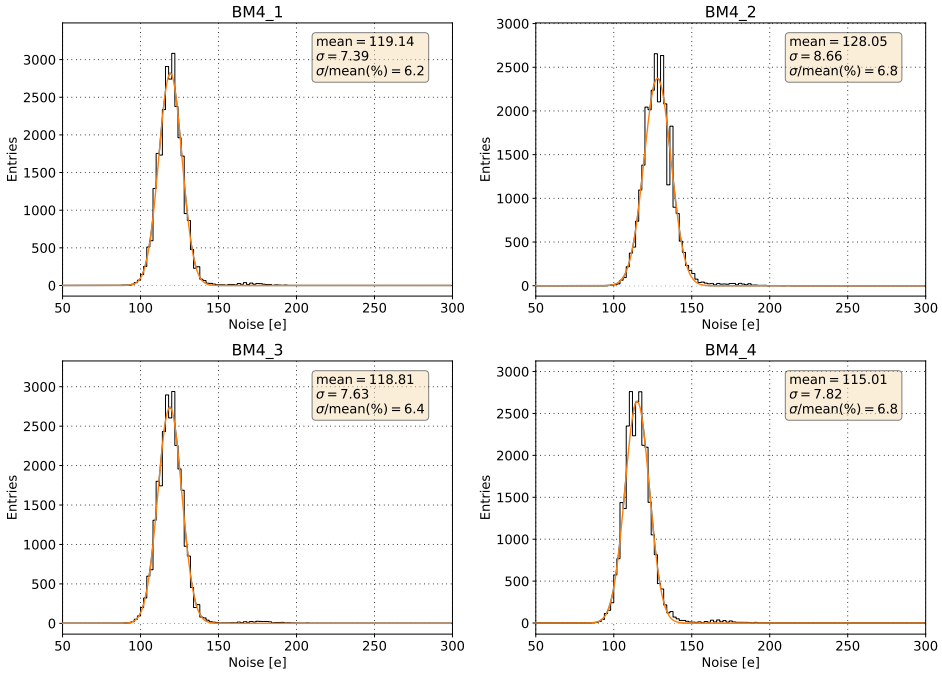


(b) BM3: Noise.

Figure A.3.: Threshold and noise distributions for the module BM3 after tuning to a discriminator threshold of 3000 e.

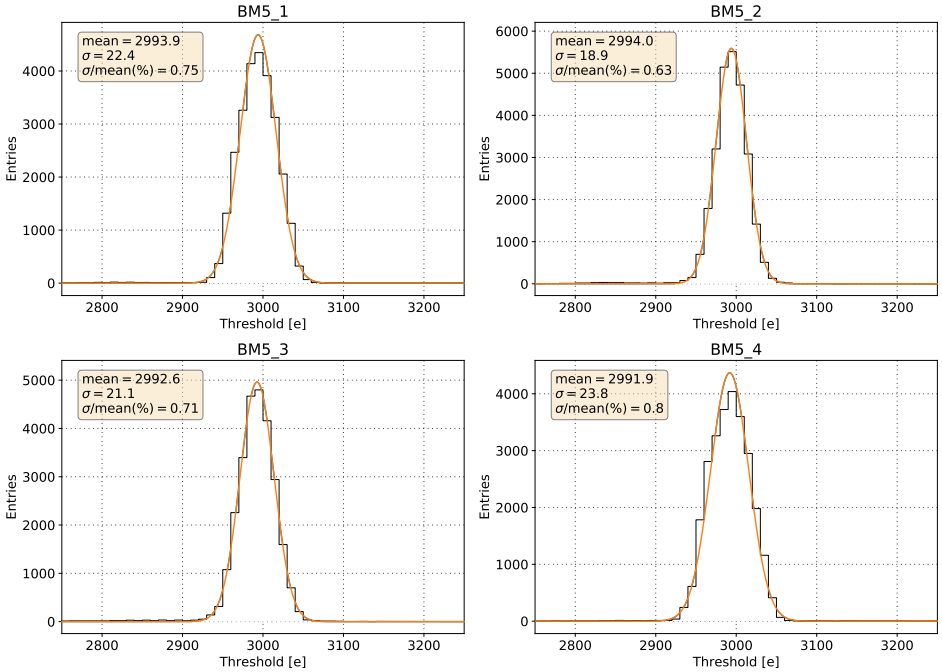


(a) BM4: Threshold.

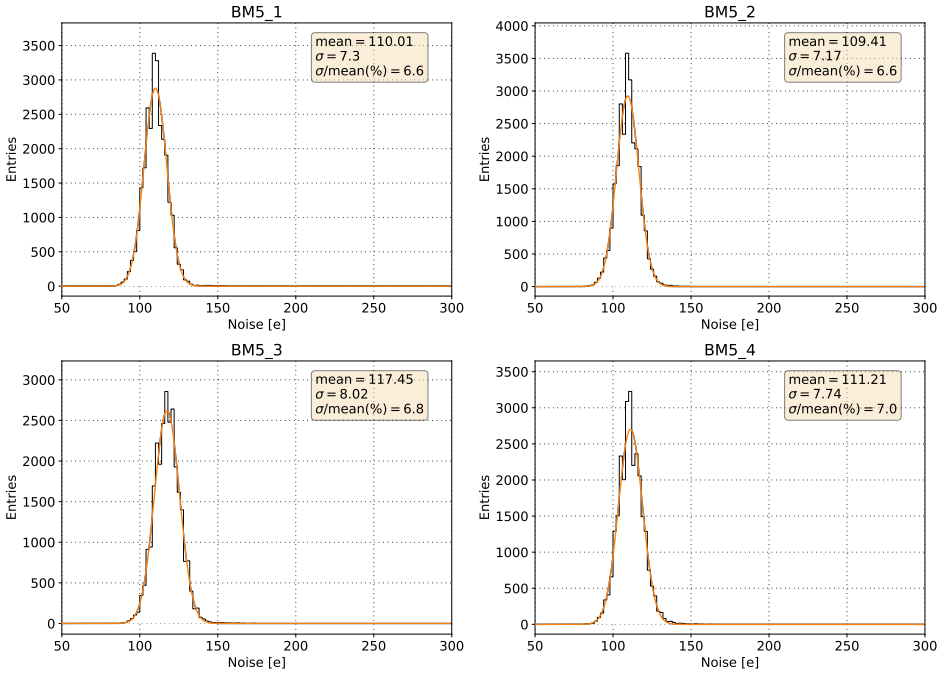


(b) BM4: Noise.

Figure A.4.: Threshold and noise distributions for the module BM4 after tuning to a discriminator threshold of 3000 e.

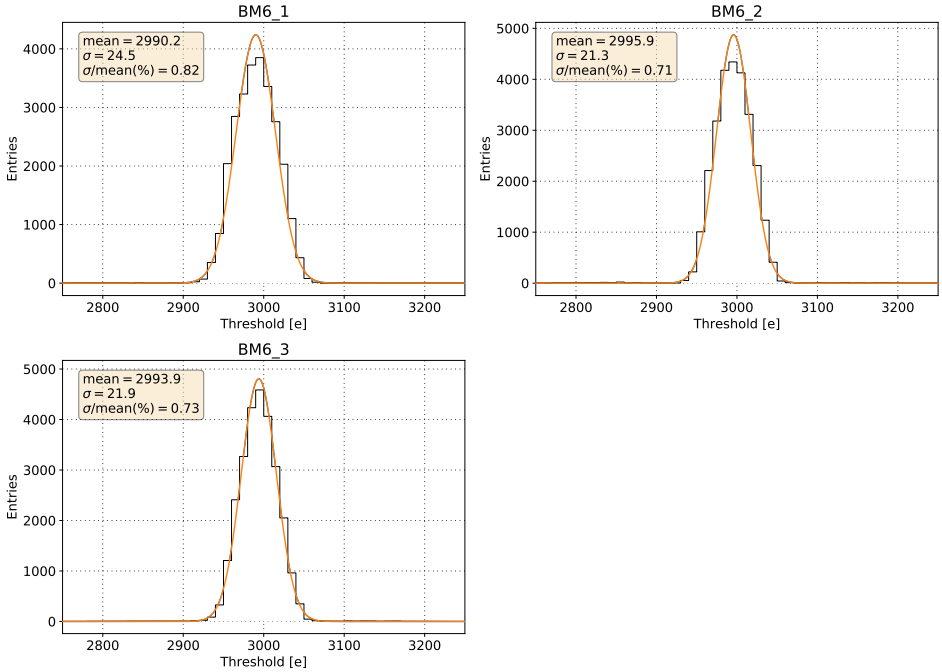


(a) BM5: Threshold.

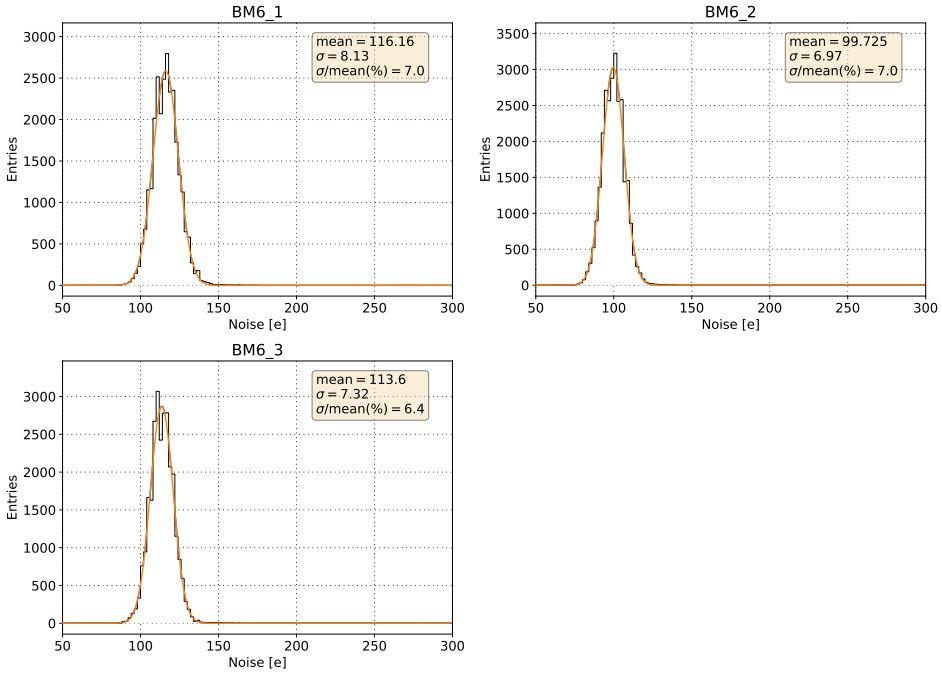


(b) BM5: Noise.

Figure A.5.: Threshold and noise distributions for the module BM5 after tuning to a discriminator threshold of 3000 e.

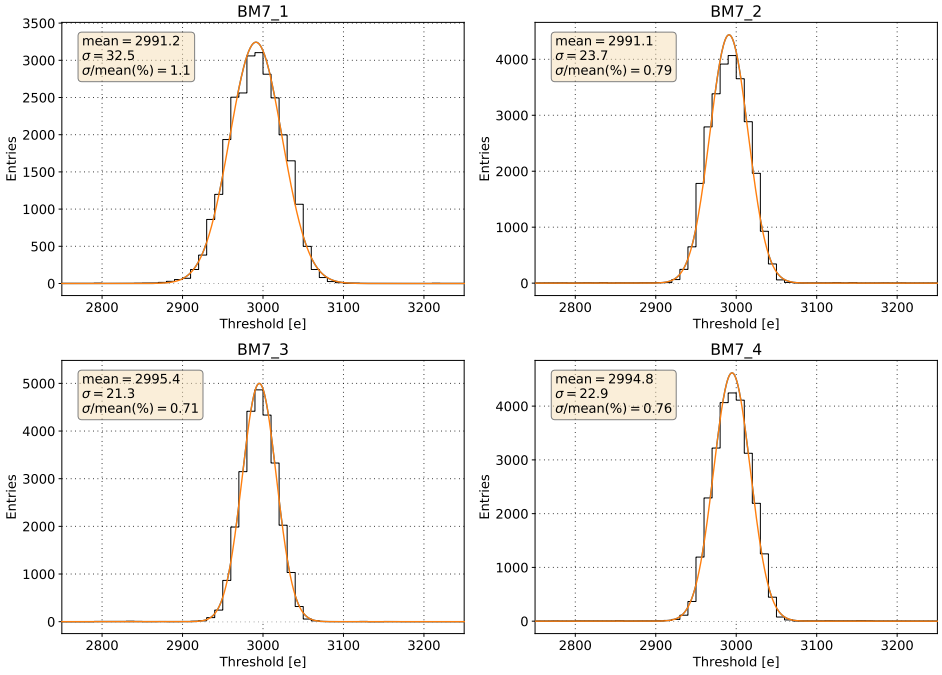


(a) BM6: Threshold.

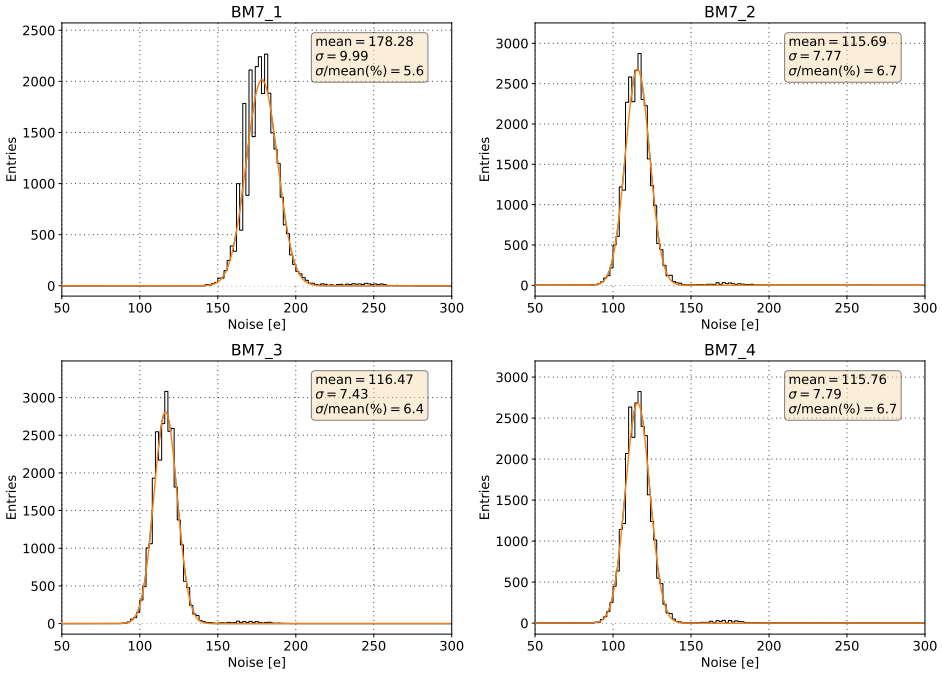


(b) BM6: Noise.

Figure A.6.: Threshold and noise distributions for the module BM6 after tuning to a discriminator threshold of 3000 e.



(a) BM7: Threshold.

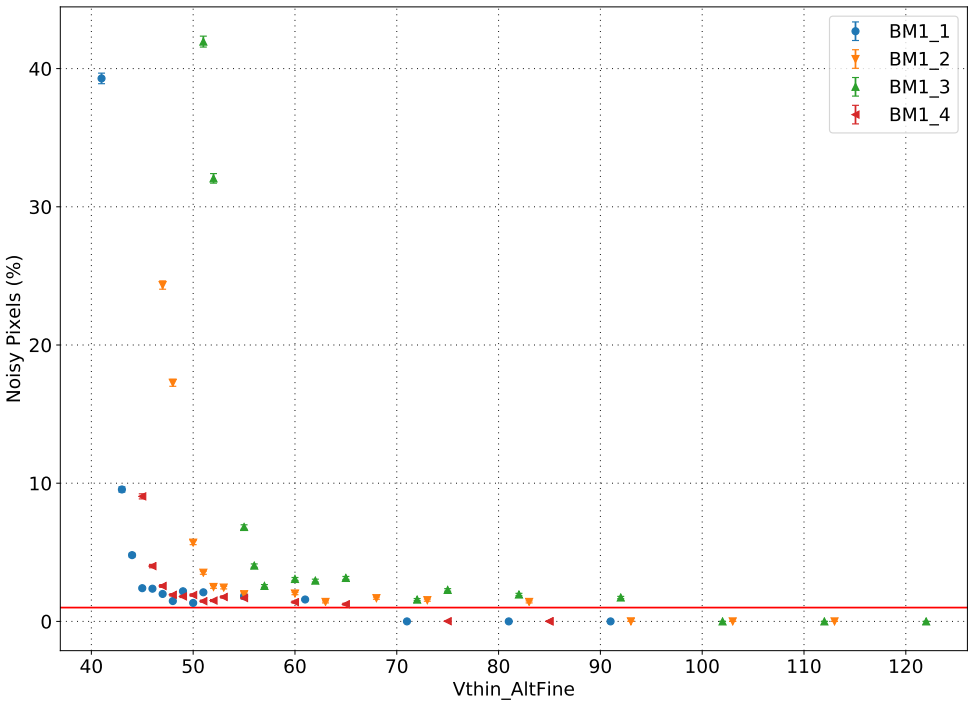


(b) BM7: Noise.

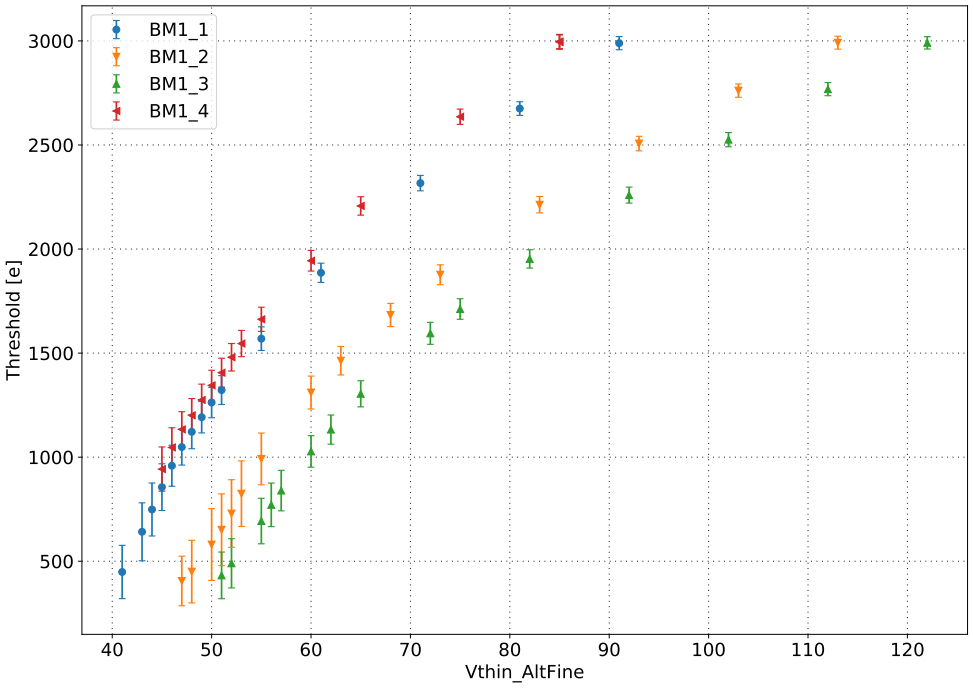
Figure A.7.: Threshold and noise distributions for the module BM7 after tuning to a discriminator threshold of 3000 e.

APPENDIX B

Minimum Threshold

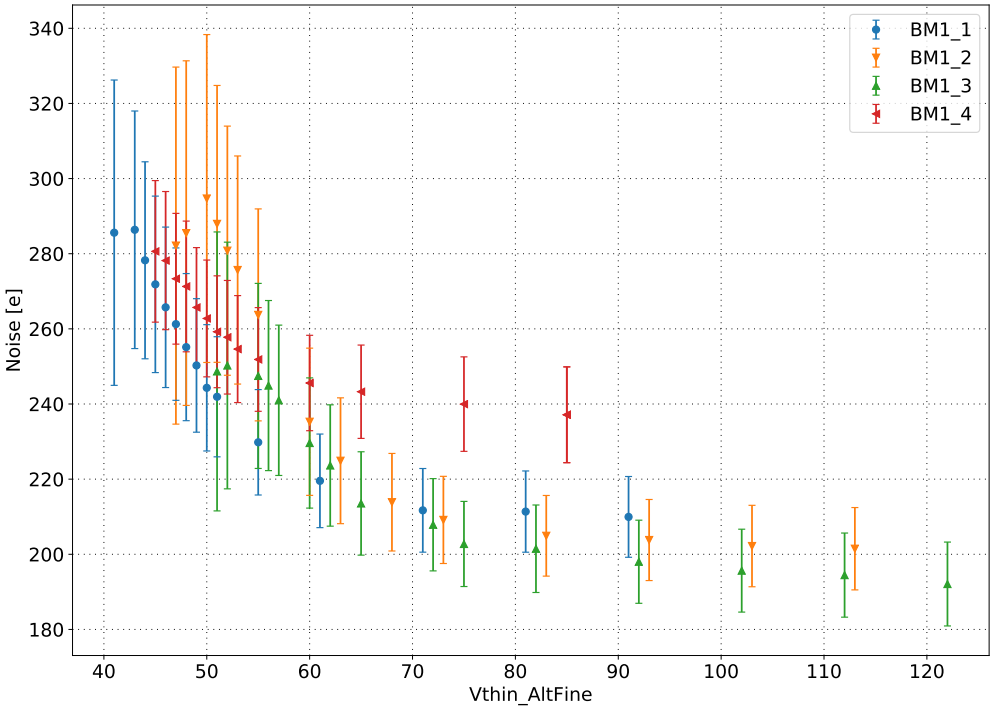


(a) BM1: Noisy pixels.



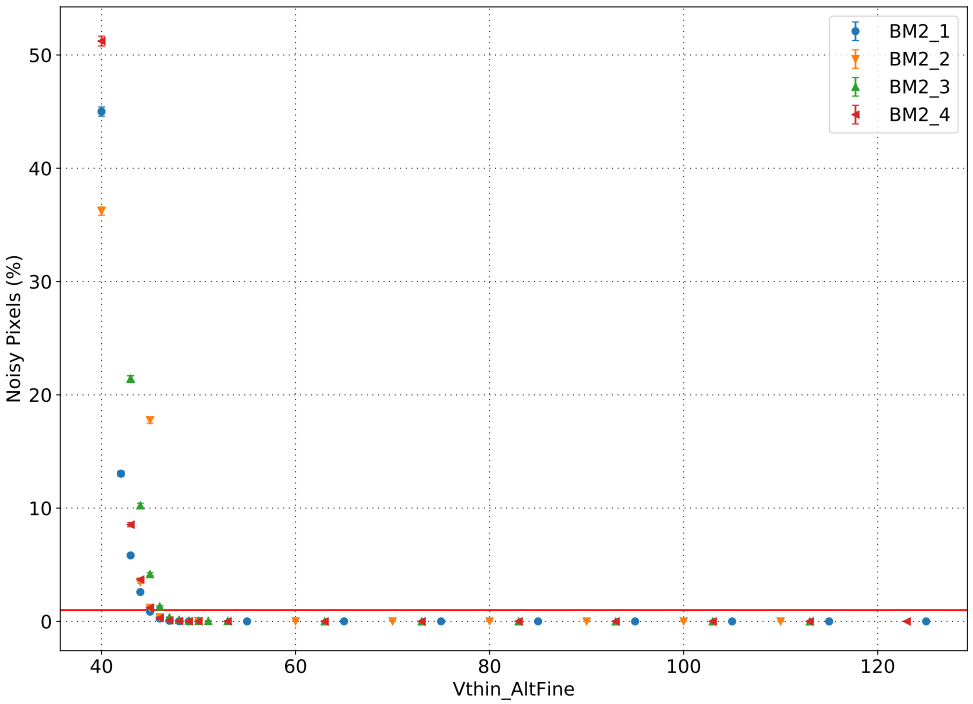
(b) BM1: Threshold.

Figure B.1.: Fraction of noisy pixels (a) and measured threshold (b) for decreasing values of VthinAlt_Fine on BM1. The bars in (b) show the standard deviation of the distribution.

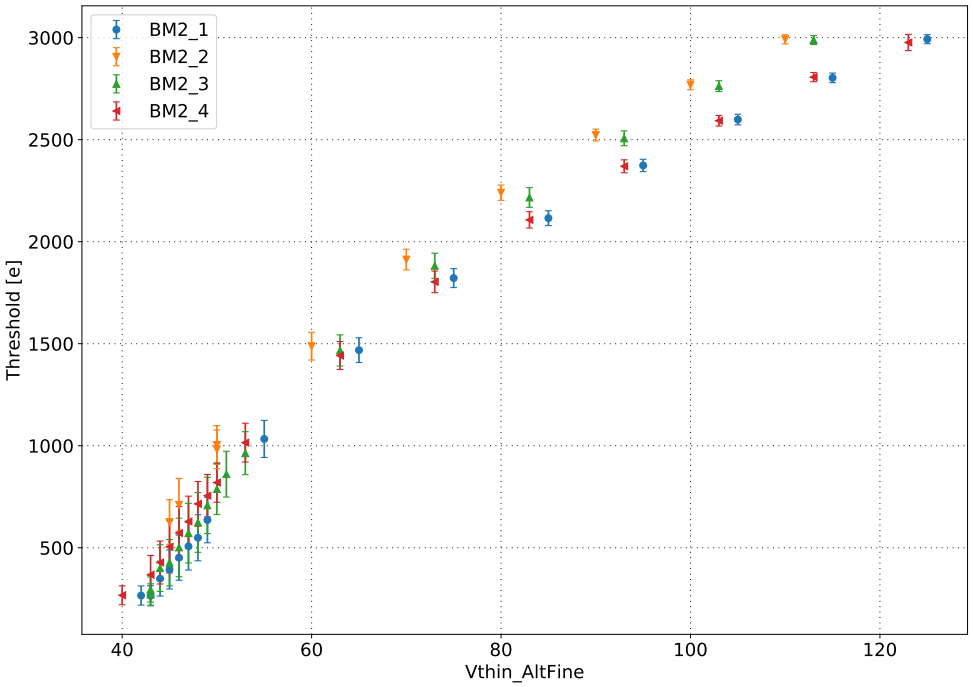


(a) BM1: Noise.

Figure B.2.: Measured noise for decreasing values of VthinAlt_Fine on BM1. The bars show the standard deviation of the distribution.

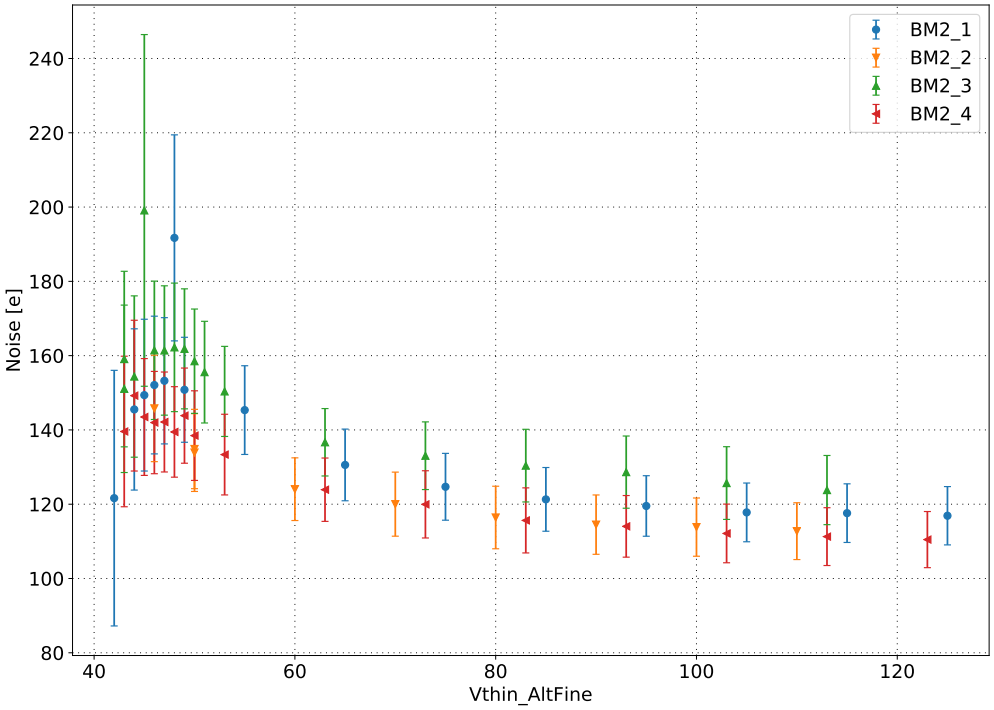


(a) BM2: Noisy pixels.



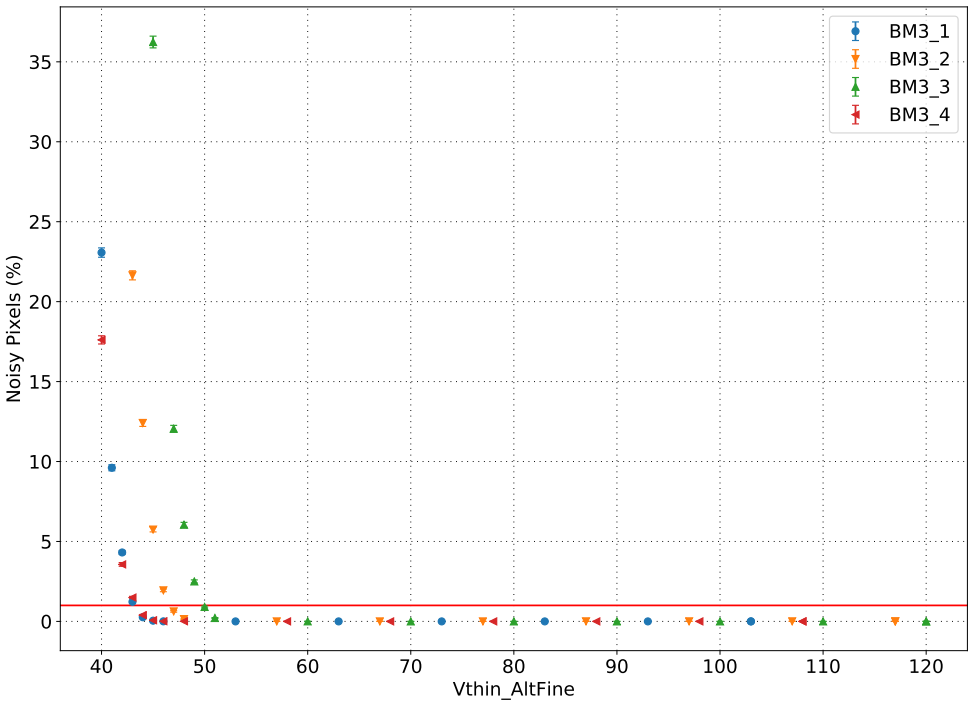
(b) BM2: Threshold.

Figure B.3.: Fraction of noisy pixels (a) and measured threshold (b) for decreasing values of VthinAlt_Fine on BM2. The bars in (b) show the standard deviation of the distribution.

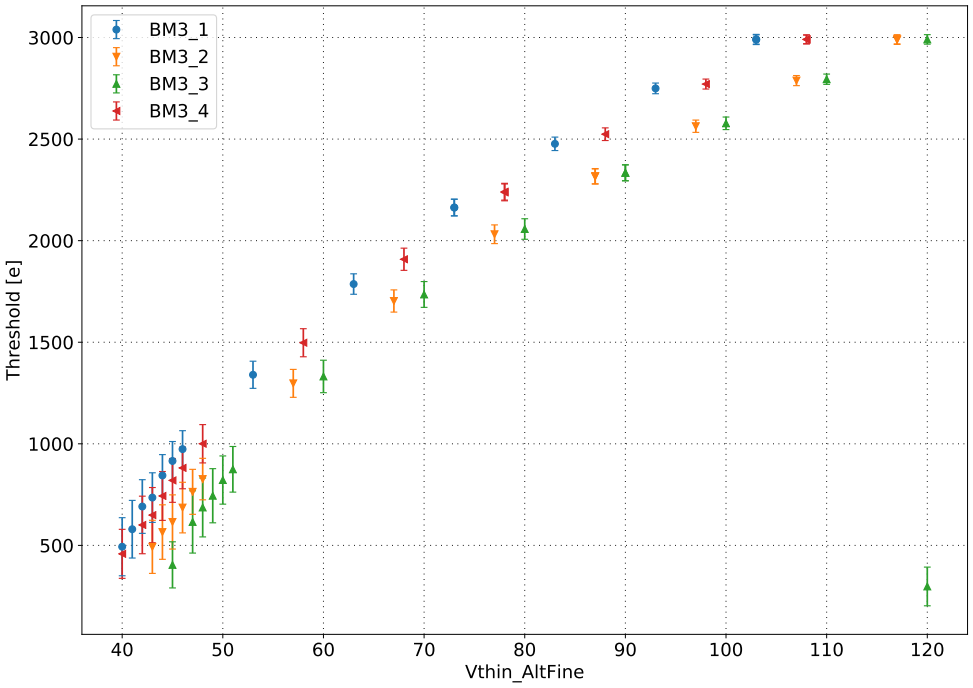


(a) BM2: Noise.

Figure B.4.: Measured noise for decreasing values of VthinAlt_Fine on BM2. The bars show the standard deviation of the distribution.

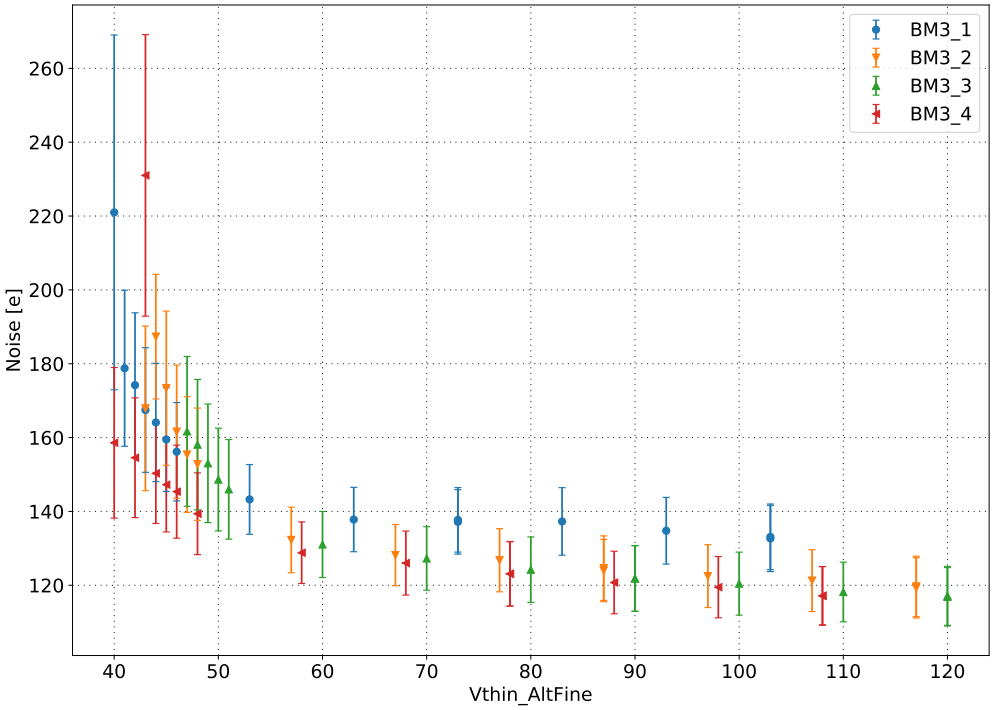


(a) BM3: Noisy pixels.



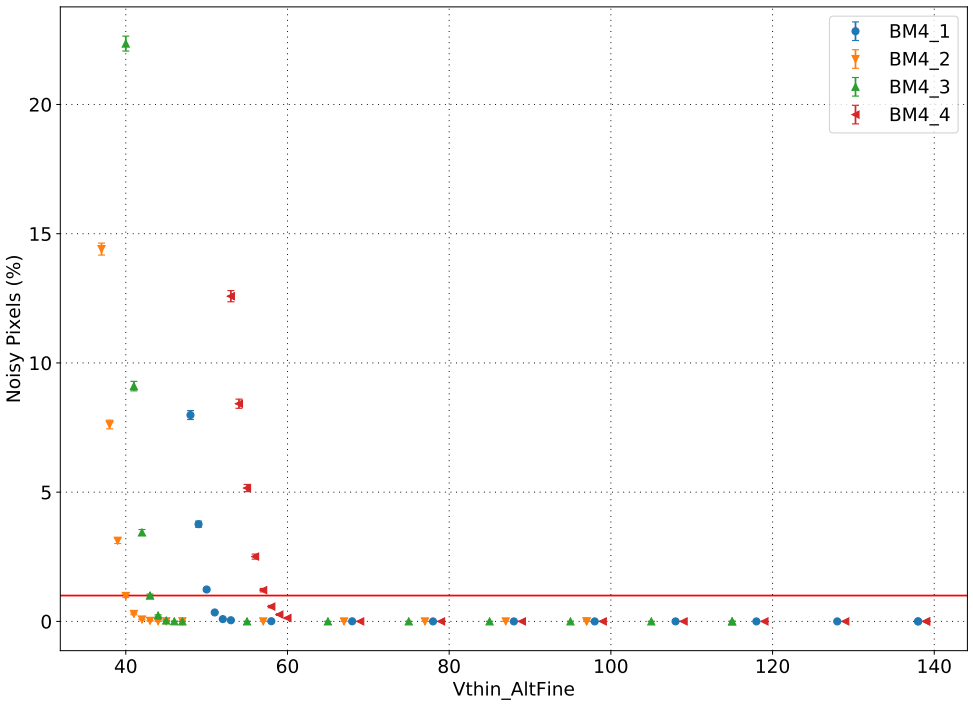
(b) BM3: Threshold.

Figure B.5.: Fraction of noisy pixels (a) and measured threshold (b) for decreasing values of VthinAlt_Fine on BM3. The bars in (b) show the standard deviation of the distribution.

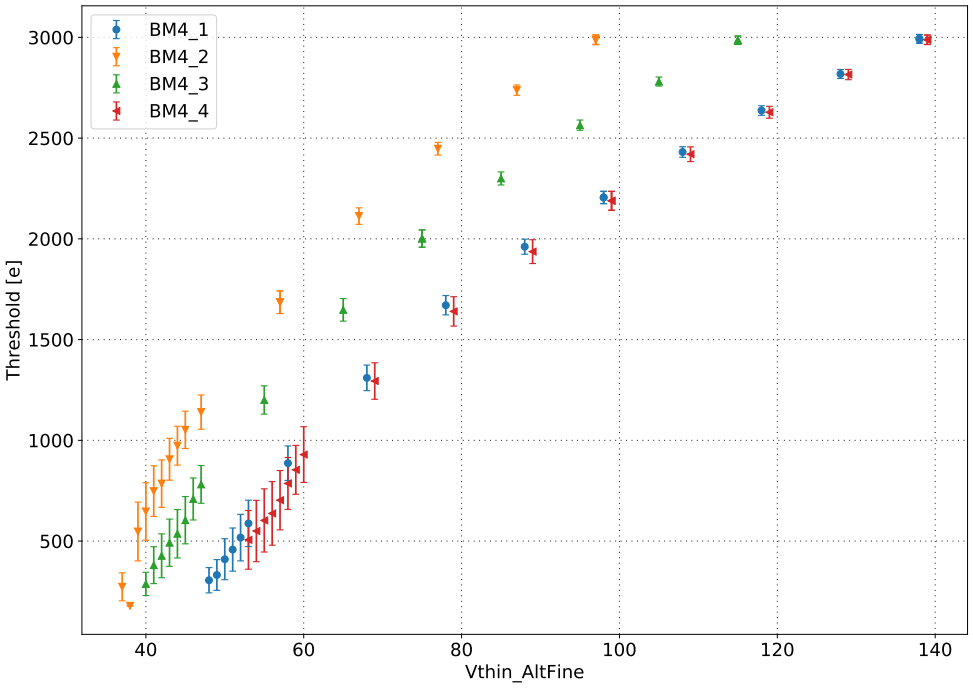


(a) BM3: Noise.

Figure B.6.: Measured noise for decreasing values of VthinAlt_Fine on BM3. The bars show the standard deviation of the distribution.

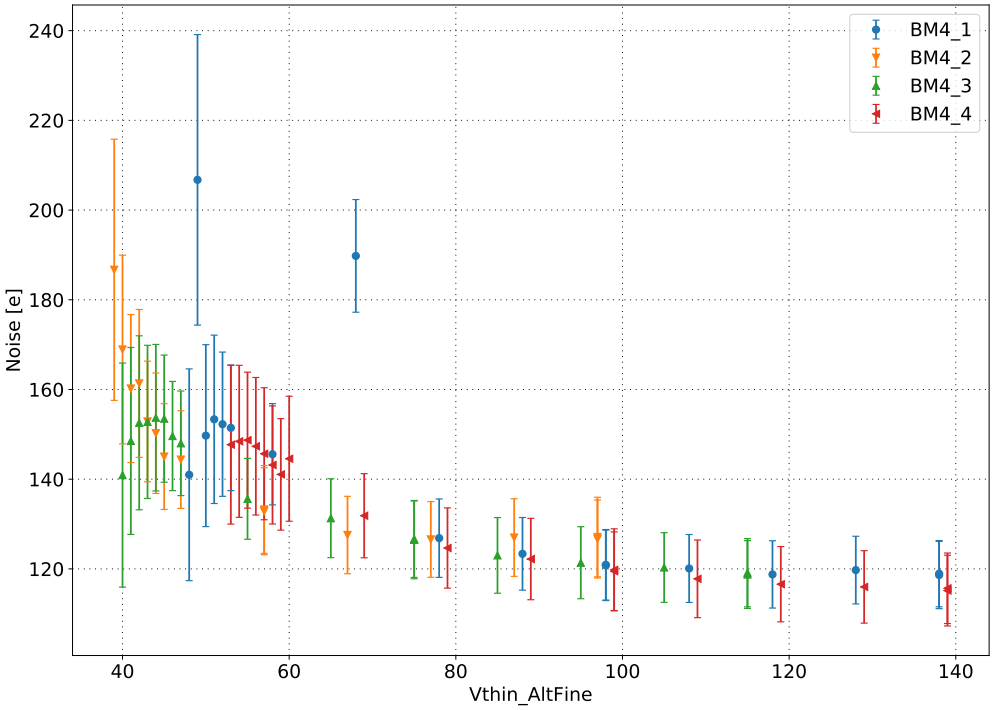


(a) BM4: Noisy pixels.



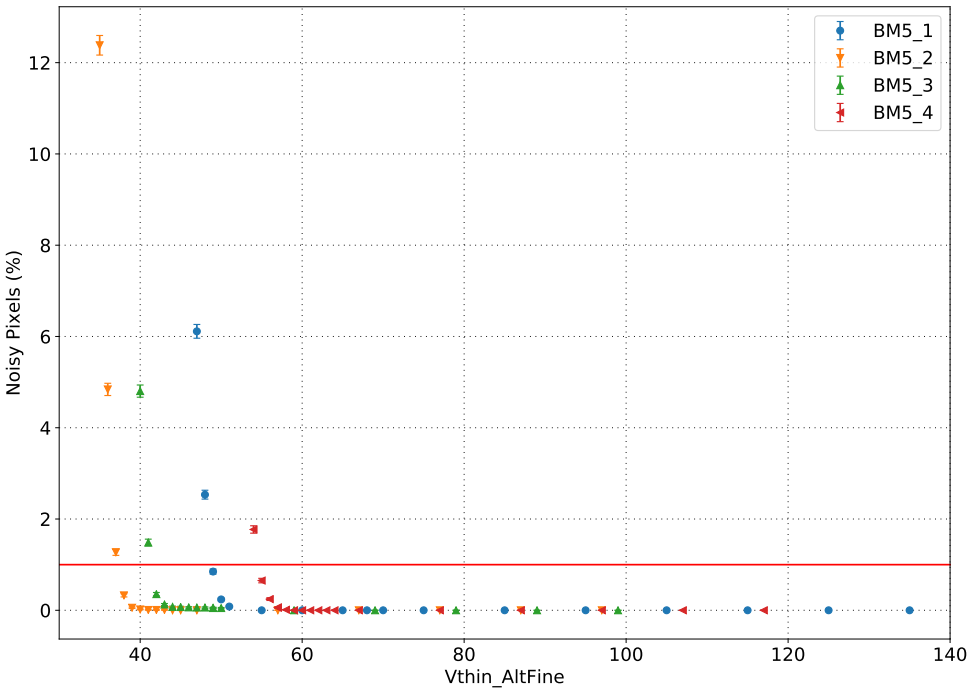
(b) BM4: Threshold.

Figure B.7.: Fraction of noisy pixels (a) and measured threshold (b) for decreasing values of VthinAlt_Fine on BM4. The bars in (b) show the standard deviation of the distribution.

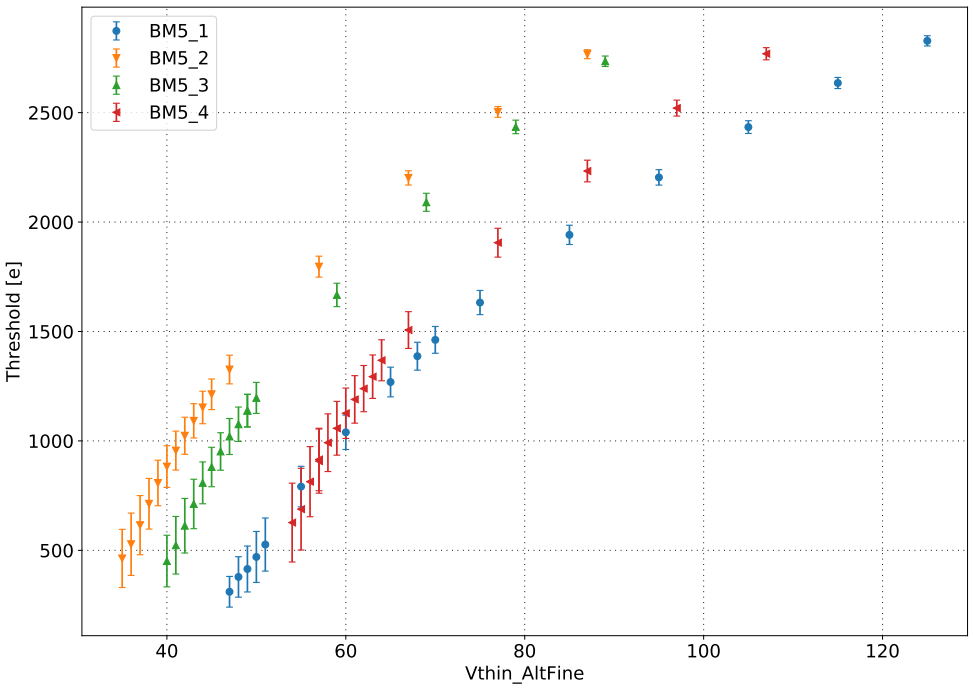


(a) BM4: Noise.

Figure B.8.: Measured noise for decreasing values of VthinAlt_Fine on BM4. The bars show the standard deviation of the distribution.

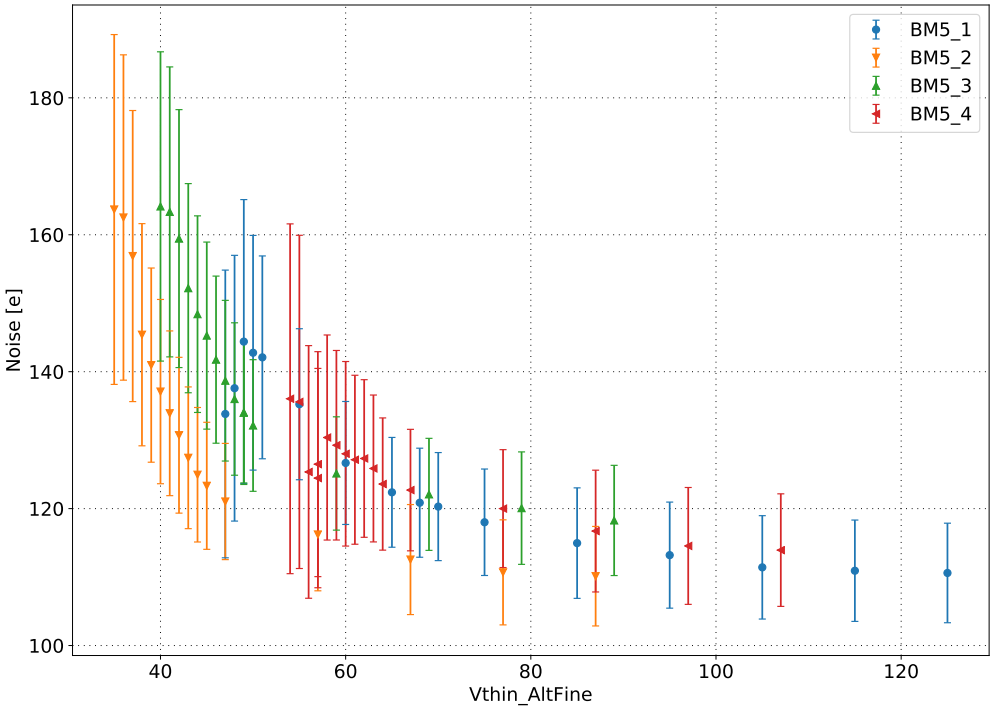


(a) BM5: Noisy pixels.



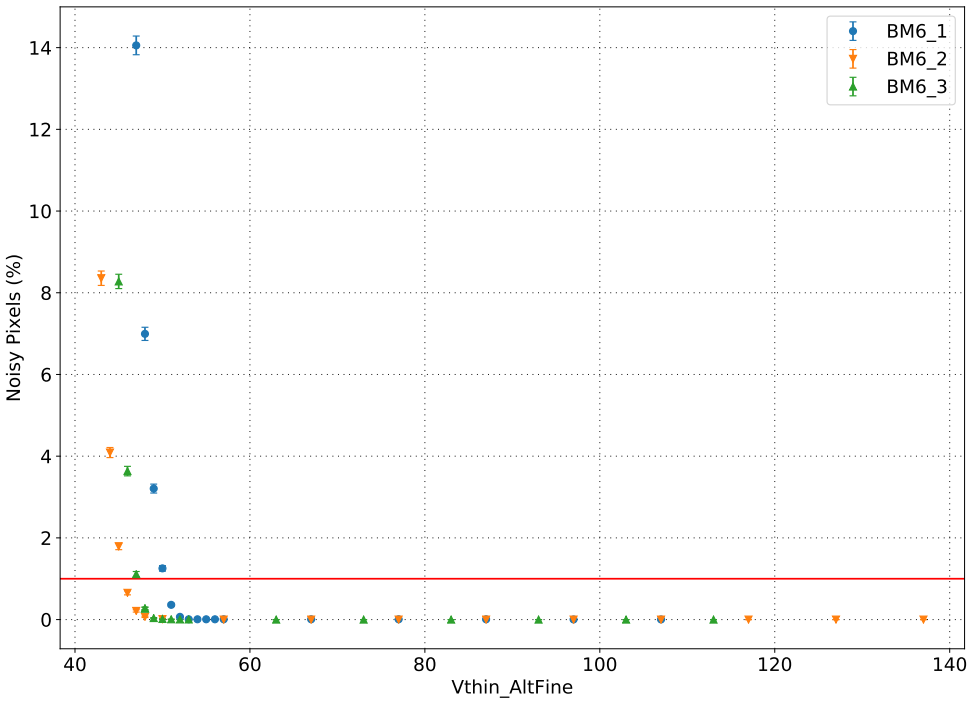
(b) BM5: Threshold.

Figure B.9.: Fraction of noisy pixels (a) and measured threshold (b) for decreasing values of VthinAlt_Fine on BM5. The bars in (b) show the standard deviation of the distribution.

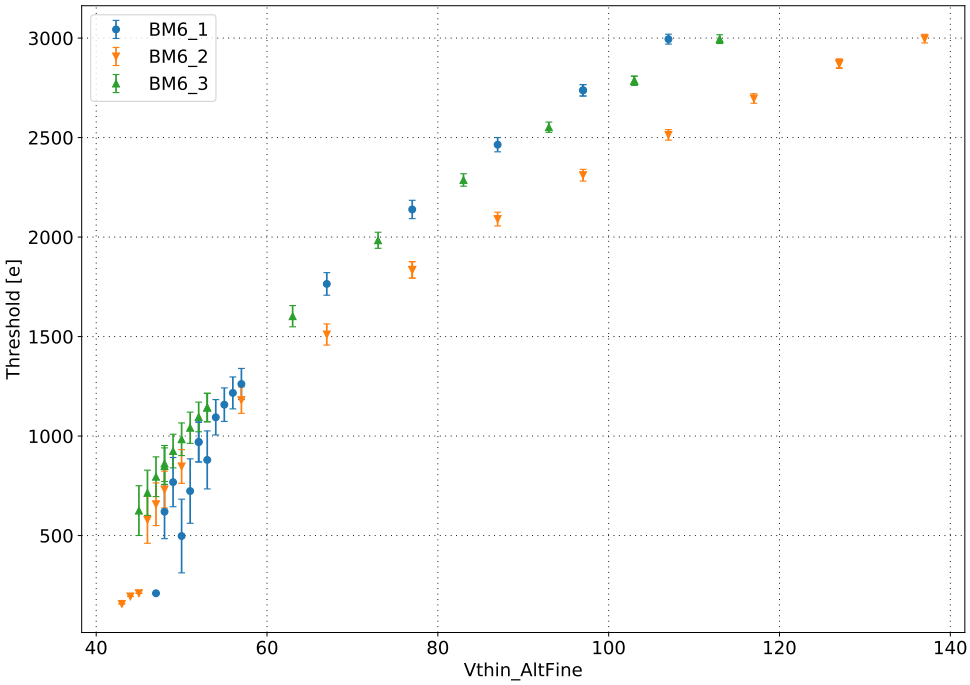


(a) BM5: Noise.

Figure B.10.: Measured noise for decreasing values of VthinAlt_Fine on BM5. The bars show the standard deviation of the distribution.

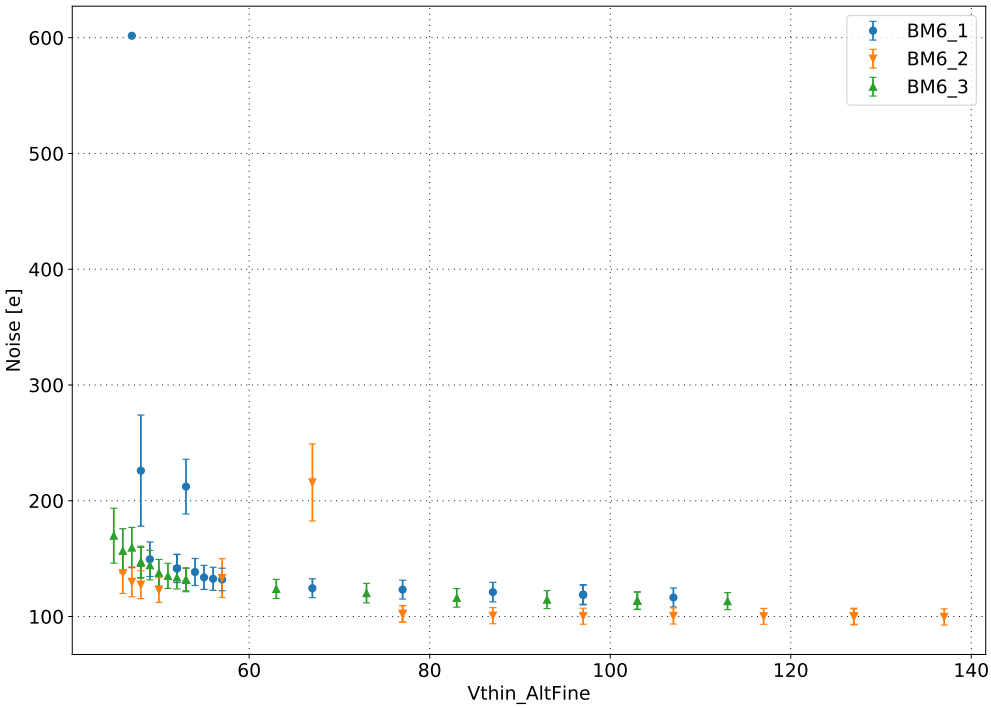


(a) BM6: Noisy pixels.



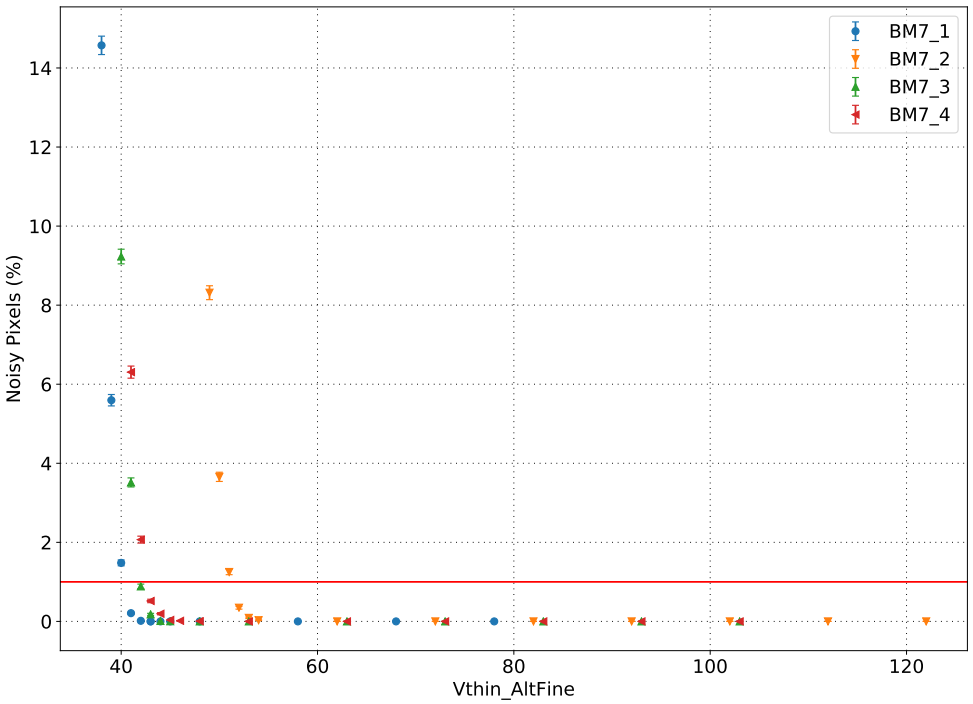
(b) BM6: Threshold.

Figure B.11.: Fraction of noisy pixels (a) and measured threshold (b) for decreasing values of VthinAlt_Fine on BM6. The bars in (b) show the standard deviation of the distribution.

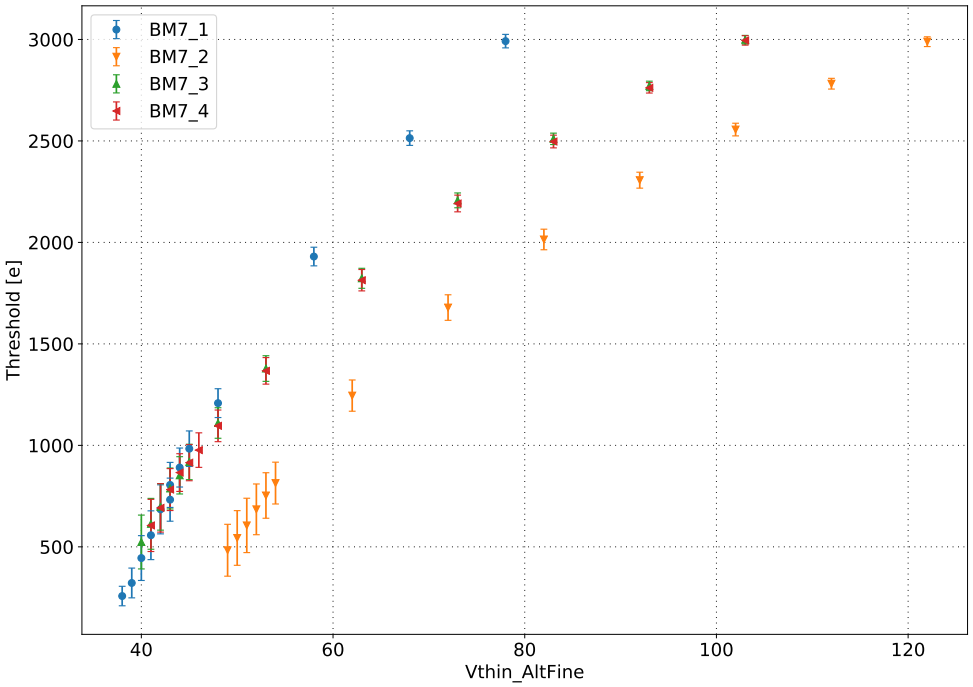


(a) BM6: Noise.

Figure B.12.: Measured noise for decreasing values of VthinAlt_Fine on BM6. The bars show the standard deviation of the distribution.

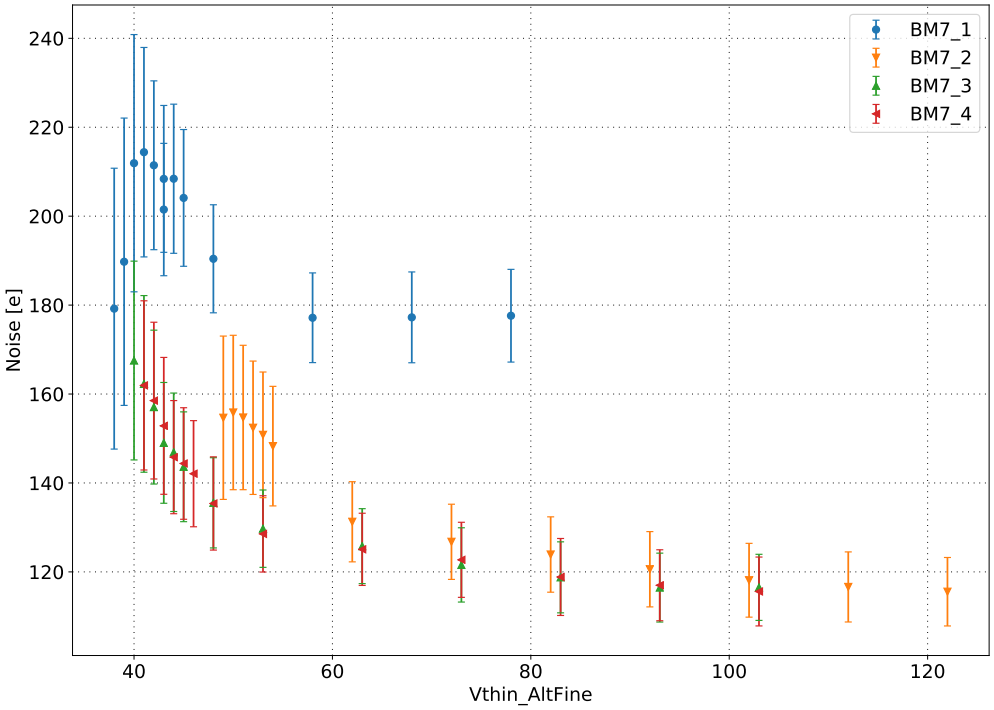


(a) BM7: Noisy pixels.



(b) BM7: Threshold.

Figure B.13.: Fraction of noisy pixels (a) and measured threshold (b) for decreasing values of VthinAlt_Fine on BM7. The bars in (b) show the standard deviation of the distribution.

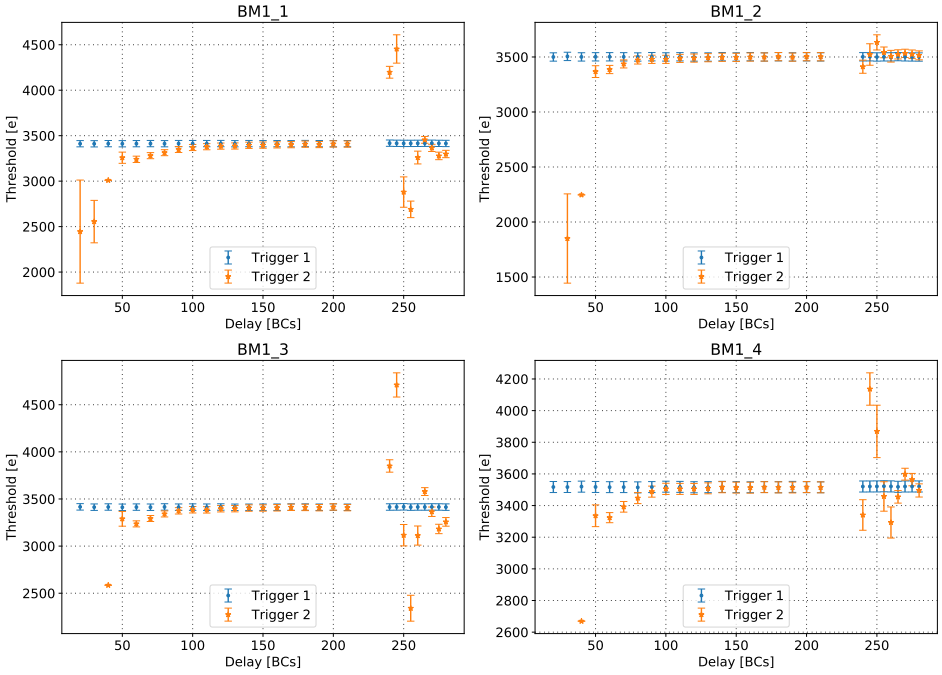


(a) BM7: Noise.

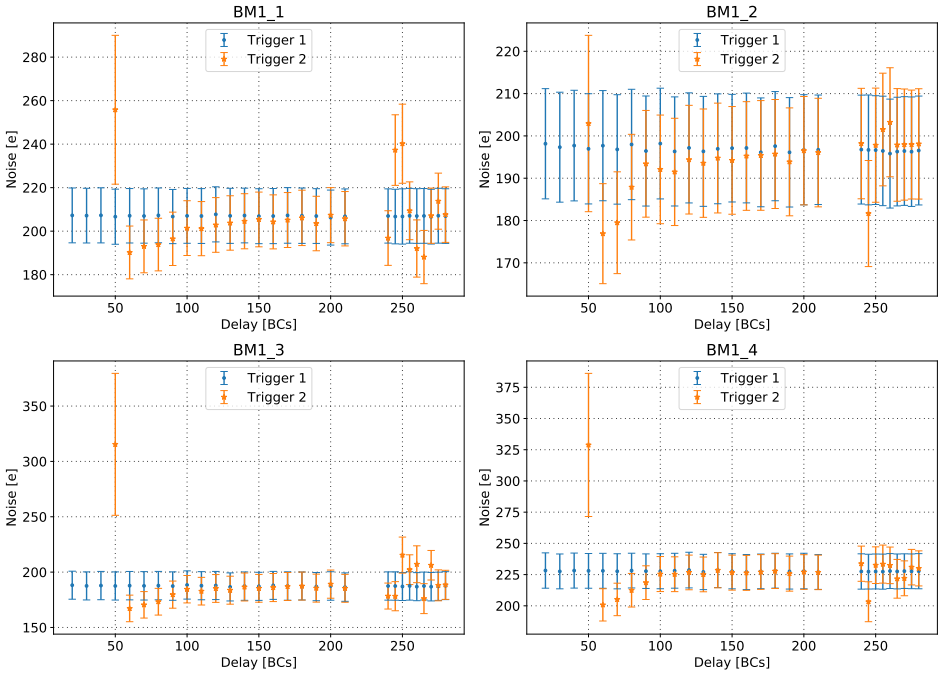
Figure B.14.: Measured noise for decreasing values of VthinAlt_Fine on BM7. The bars show the standard deviation of the distribution.

APPENDIX C

Double Trigger Threshold

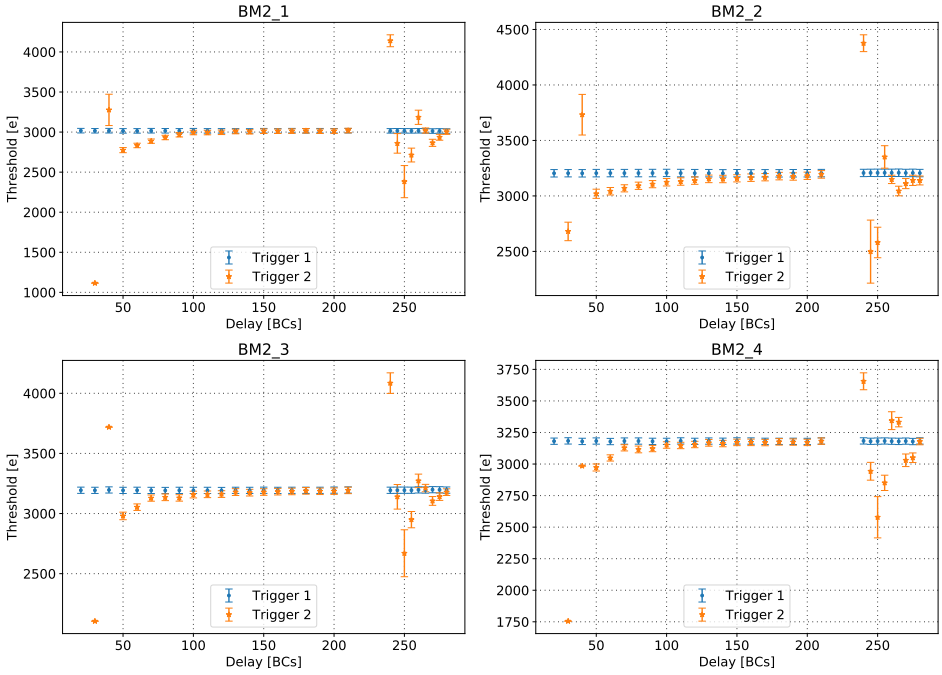


(a) BM1: Threshold distributions.

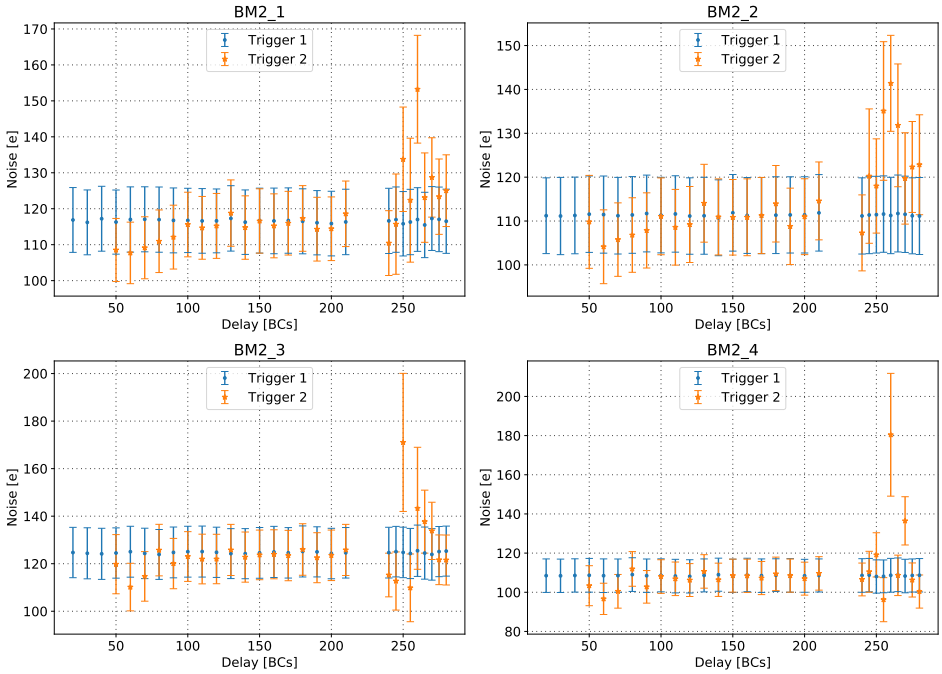


(b) BM1: Noise distributions.

Figure C.1.: Double trigger threshold scan on BM1. The bars show the standard deviation of the distribution.

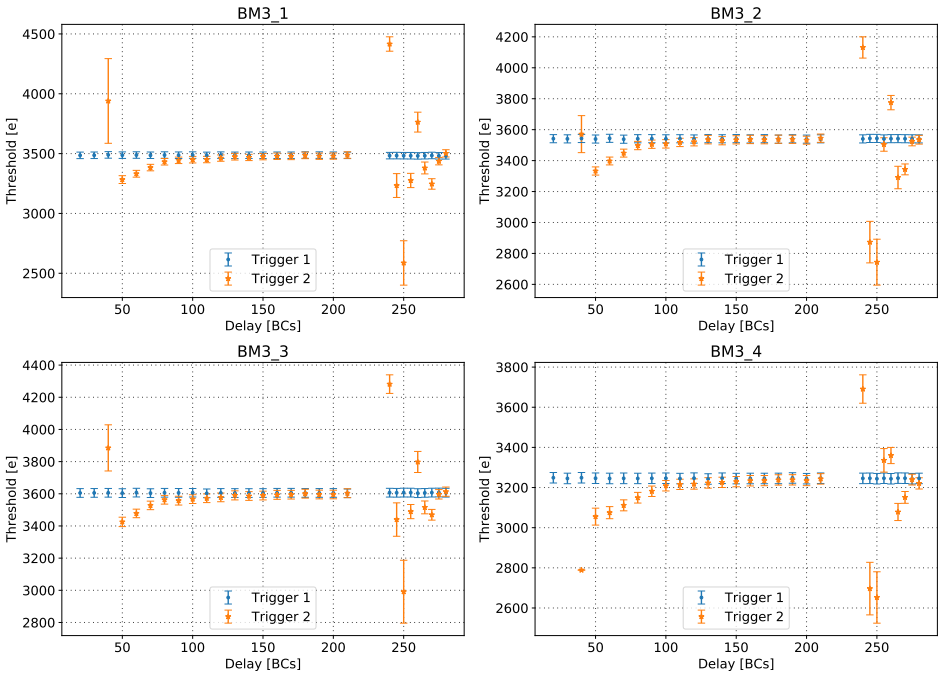


(a) BM2: Threshold distributions.

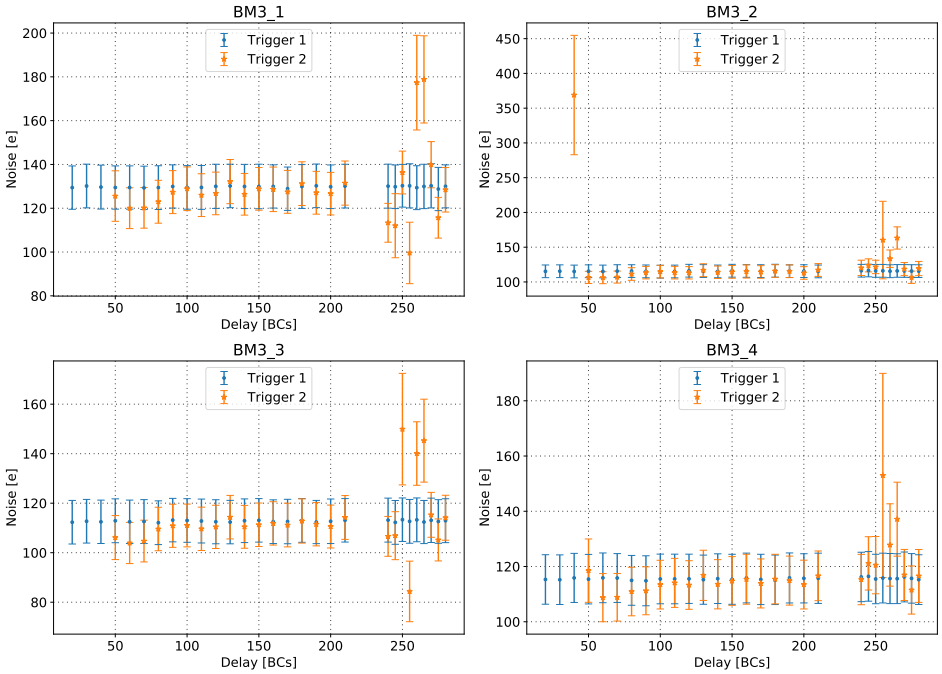


(b) BM2: Noise distributions.

Figure C.2.: Double trigger threshold scan on BM2. The bars show the standard deviation of the distribution.

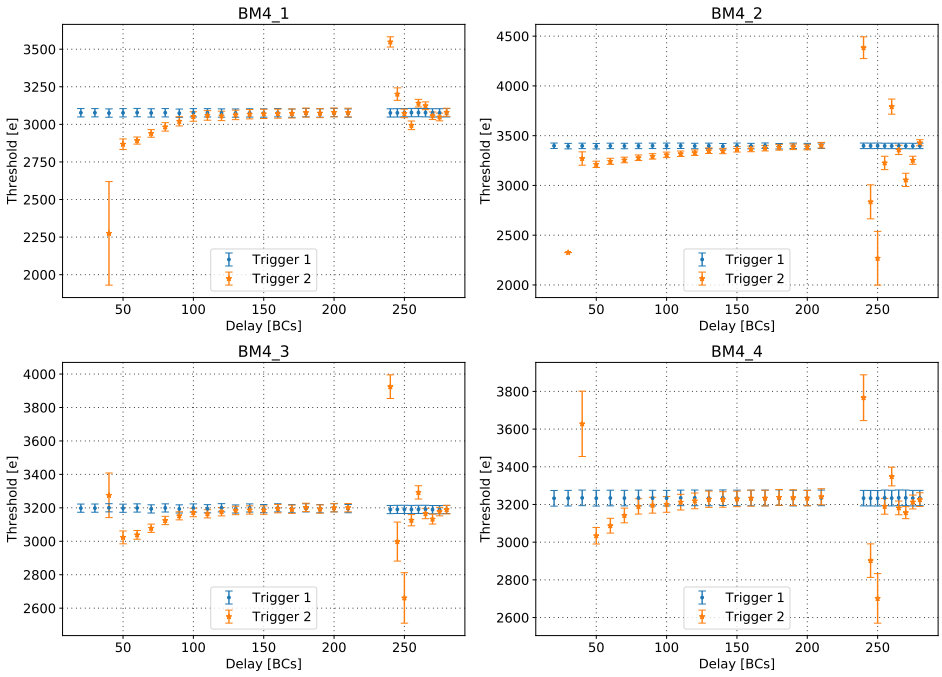


(a) BM3: Threshold distributions.

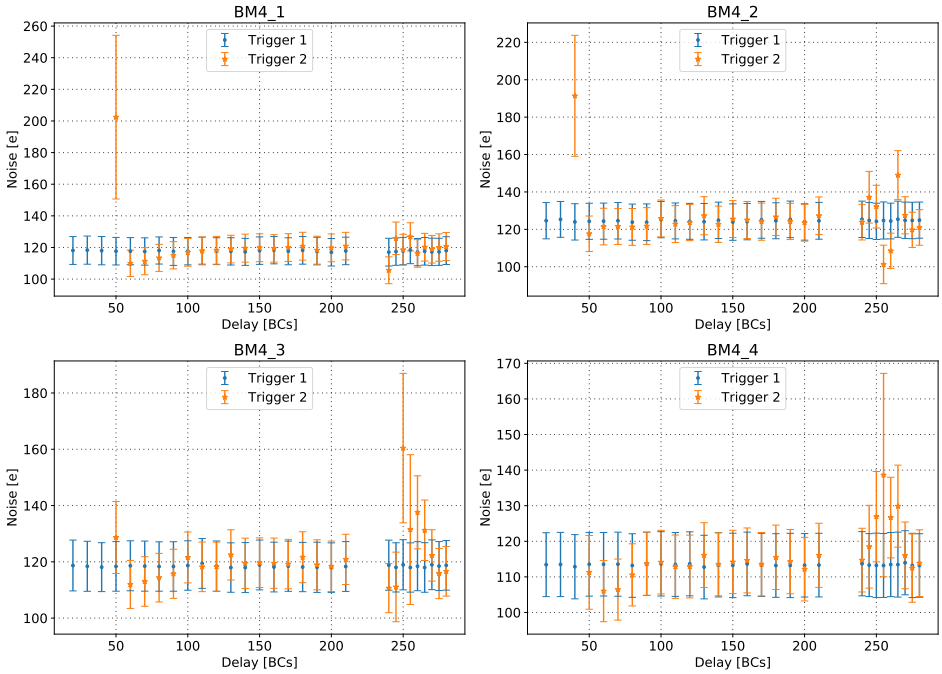


(b) BM3: Noise distributions.

Figure C.3.: Double trigger threshold scan on BM3. The bars show the standard deviation of the distribution.

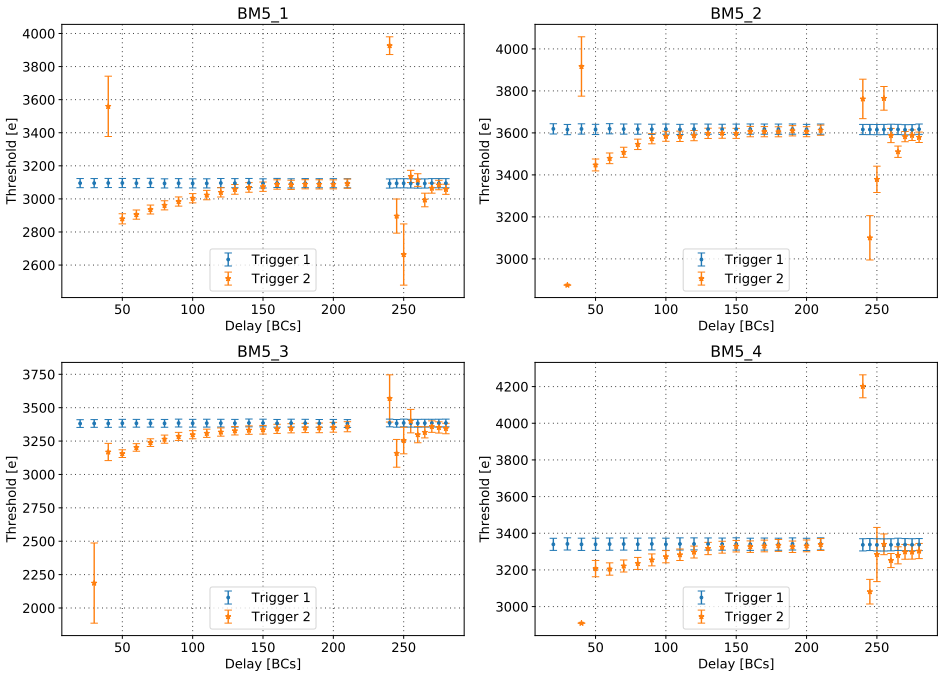


(a) BM4: Threshold distributions.

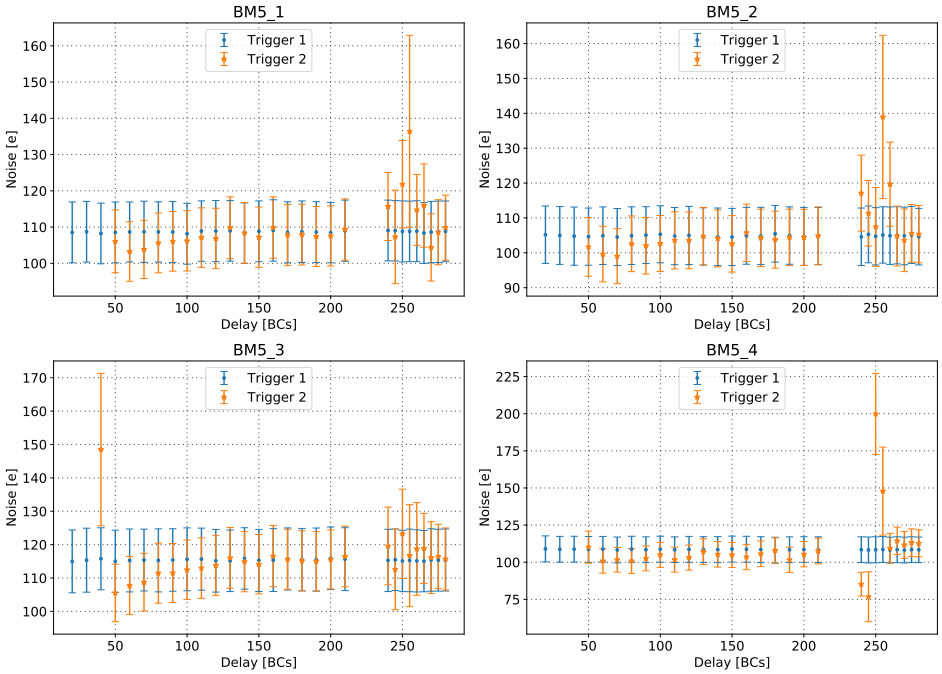


(b) BM4: Noise distributions.

Figure C.4.: Double trigger threshold scan on BM4. The bars show the standard deviation of the distribution.

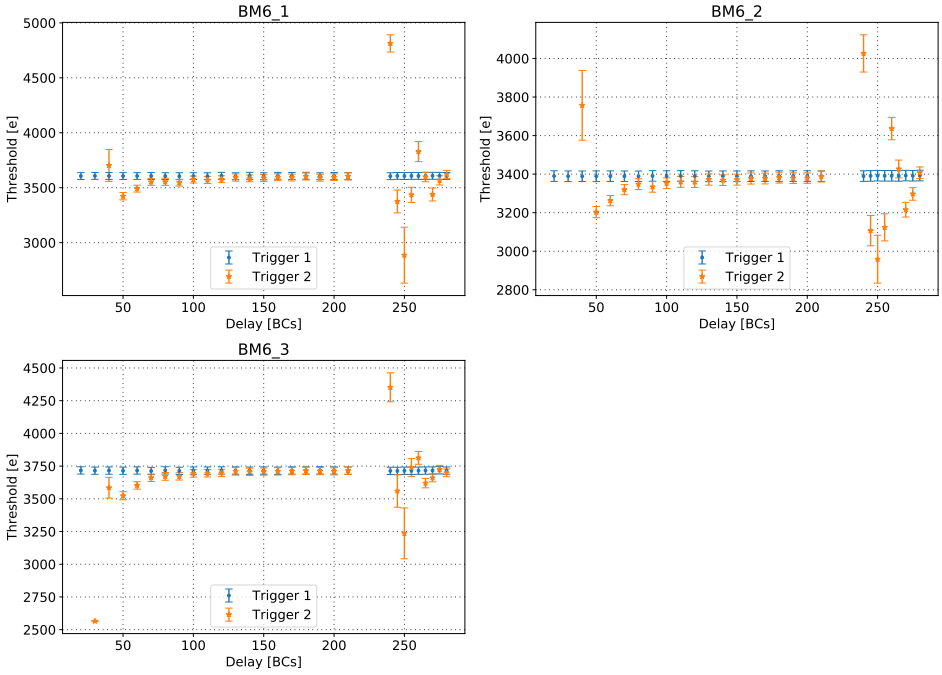


(a) BM5: Threshold distributions.

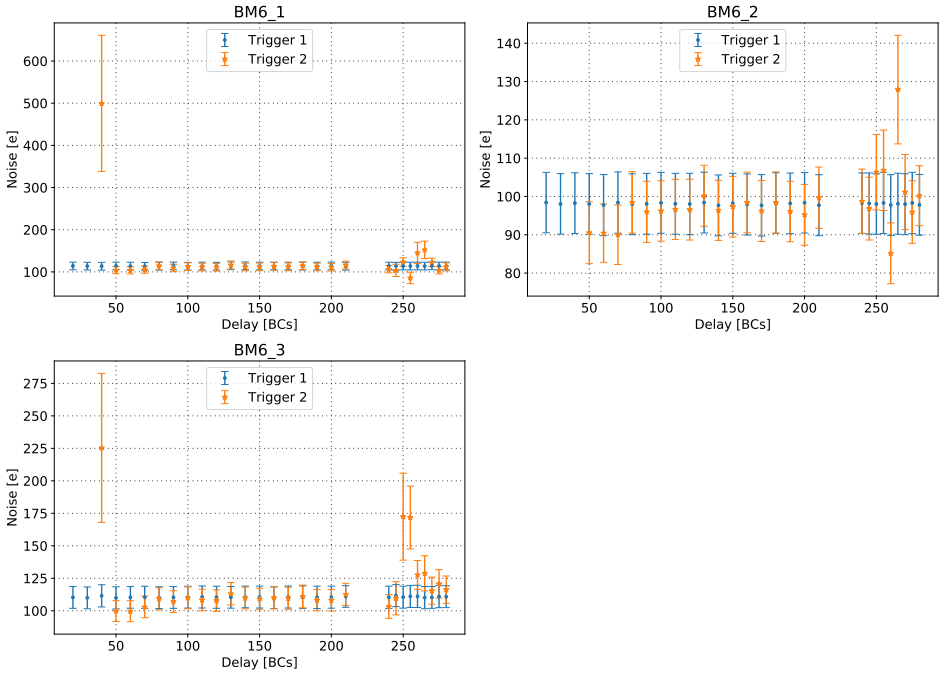


(b) BM5: Noise distributions.

Figure C.5.: Double trigger threshold scan on BM5. The bars show the standard deviation of the distribution.

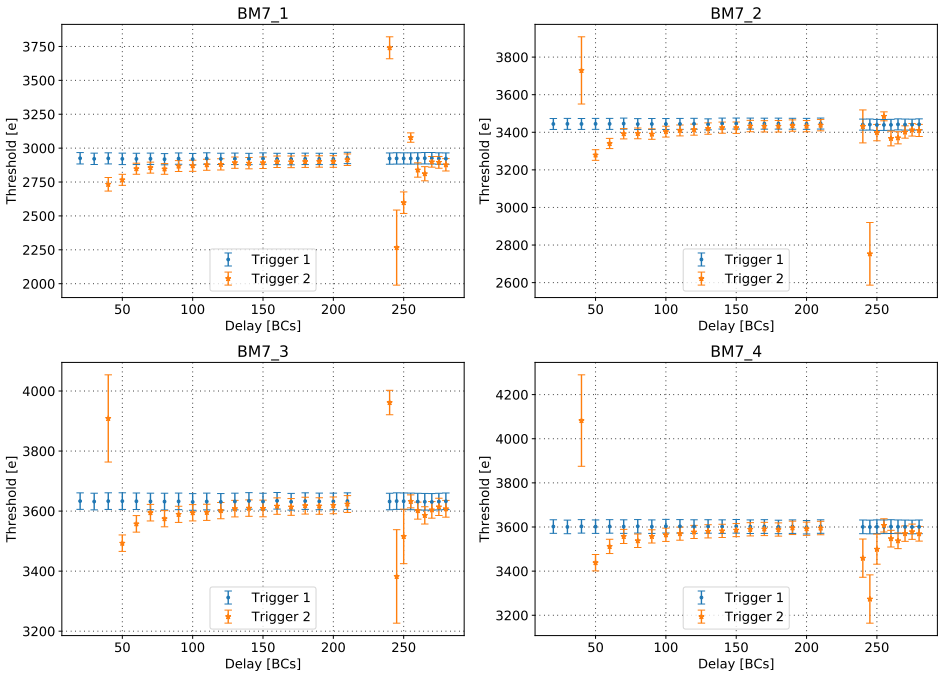


(a) BM6: Threshold distributions.

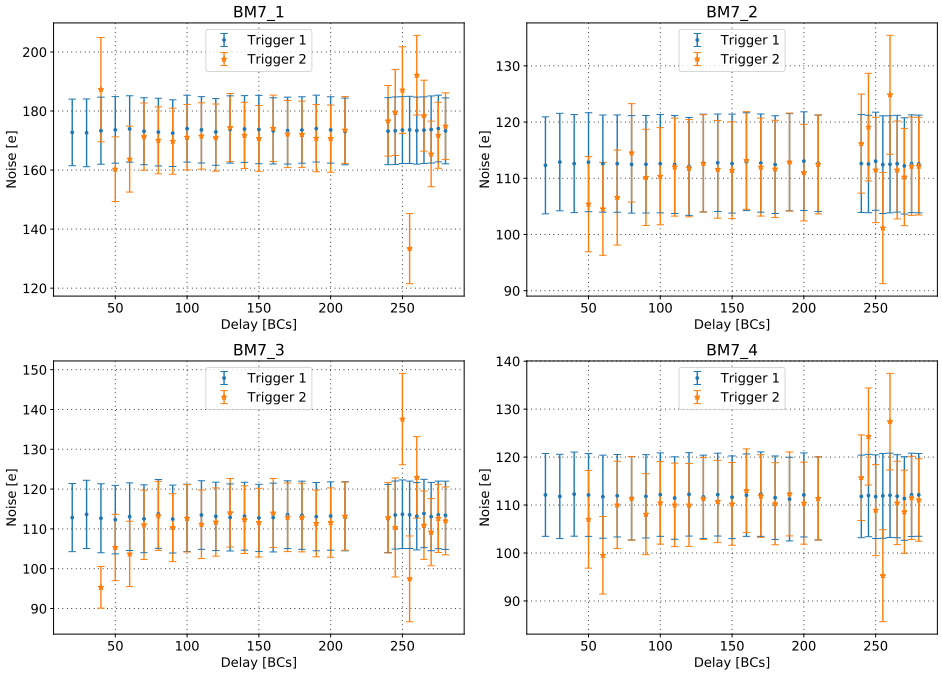


(b) BM6: Noise distributions.

Figure C.6.: Double trigger threshold scan on BM6. The bars show the standard deviation of the distribution.



(a) BM7: Threshold distributions.



(b) BM7: Noise distributions.

Figure C.7.: Double trigger threshold scan on BM7. The bars show the standard deviation of the distribution.

APPENDIX D

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