Investigation of potential induced degradation as a performance limiting defect in photovoltaic modules

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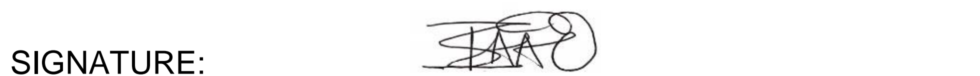
SIGNATURE: 

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DEDICATION

To my parents the **late Richard Chepoto Kwembur** and **Beatrice Tamnai**

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ABSTRACT

Potential Induced Degradation (PID) impacts negatively on photovoltaic (PV) module durability because it significantly affects the output of PV modules and systems. Unless detected at infancy, PID progression can be catastrophic. This study involved systematic PID stressing of PV modules using a custom-built environmental chamber that can achieve suitable environmental conditions, viz., of the 35 °C ± 1 °C and relative humidity of 75 % ± 5 %. The first part of this work was to induce PID using three approaches: climate chamber testing, inducing PID using a conductive aluminium plate on the surface of the module without touching the frame and a localised PID induction on one cell in a module. The second part is to detect induced PID using Electroluminescence (EL) images taken at current corresponding to 10% I_{sc}, EL histograms analysis and V_{oc} ratio taken at 1000 W/m^2 to 200 W/m^2. The third part is to study module regeneration after PID shunting degradation in two ways, viz., forced reverse polarization and natural recovery.

The PID detection tools used in this work are well known module characterization techniques such as EL imaging, Infrared imaging, and light and dark current-voltage measurements. These characterisation tools are used in combination to detect defects such as optical losses, cracks, breakage, electric circuit degradation and PID. Under normal testing PID was detected and in some cases, modules were able to recover, while for advanced stage PID regeneration or PID reversal was difficult. This thesis focuses on PID detection at infancy using three approaches; EL imaging at current corresponding to 10% of I_{sc}. Light and dark current – voltage measurements (L-IV & D-IV) and open circuit voltage (V_{oc}) ratios at low irradiance.

The early detection procedures are essential in reversing the degradation caused by PID which is reversible. The time taken to reverse the PID degradation will depend on the extent of the degradation. If detected early, it will take a short period of time to completely reverse lost power. Infrared thermography is a non-contact characteristic tool that can be deployed in large scale plants using drones to detect the presence of PID in PV plants.

Module performance and device parameters extracted from the L-IV curves on a module before and after PID stress, such as P_{mpp}, V_{oc}, I_{sc} Fill Factor (FF), shunt resistance (R_{sh}) and series resistance (R_s) and ideality (n) are sensitive to PID shunting. V_{oc} and R_{sh} drop significantly with the onset of PID, while R_s increases. The decrease in V_{oc} and R_{sh} is due to heavy shunting on the module resulting in increased carrier recombination, while the increase in R_s is due to increased shunting paths leading to decreased photocurrent. When substantial degradation on a module occurs P_{mpp}, FF and n will drop and at very advanced stage of PID degradation I_{sc} may drop excessively.

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CHAPTER 1

1. INTRODUCTION

1.1 Background and motivation

1.1.1 Status of the PV industry

Photovoltaic (PV) modules convert solar energy to electrical energy and are a proven reliable and sustainable energy source. Over the past decade the number of photovoltaic installations has increased substantially. By the end of 2018 the global PV solar Electricity generation exceeded 0.5 TW contributing 2.6 % of global electricity needs [1]. It is estimated that by 2050, the total PV installed capacity is projected to reach 4.7 TW contributing 16.0% of the global electricity needs [2][3]. Attainment of 16 % by 2050 seems possible with the current record module efficiency of 26.1% and 22.8% for mono and multi- crystalline modules, respectively [4]. This is attributed to the effort of both the industry and academic research.

Photovoltaics (PV) is an important form of renewable energy that has attracted the attention of the world`s leading economies with a global cumulative installed capacity of 404.5 GW [5]. The annual installation for 2017 stood at 99.1 GW [5]. Figure 1.1 show the exponential growth of PV industry over the years up to 2017, the growth has been made possible by favourable support policies in renewable energy sector. In 2011, the South African government introduced Renewable Energy Independent Power Producer Procurement Programme (REIPPPP) with grid contribution of 1,474 MW against the set goal of 8, 400 MW from PV [6]. The total cumulative installation in South Africa stood at 1.8 GW at end of 2017 [7]

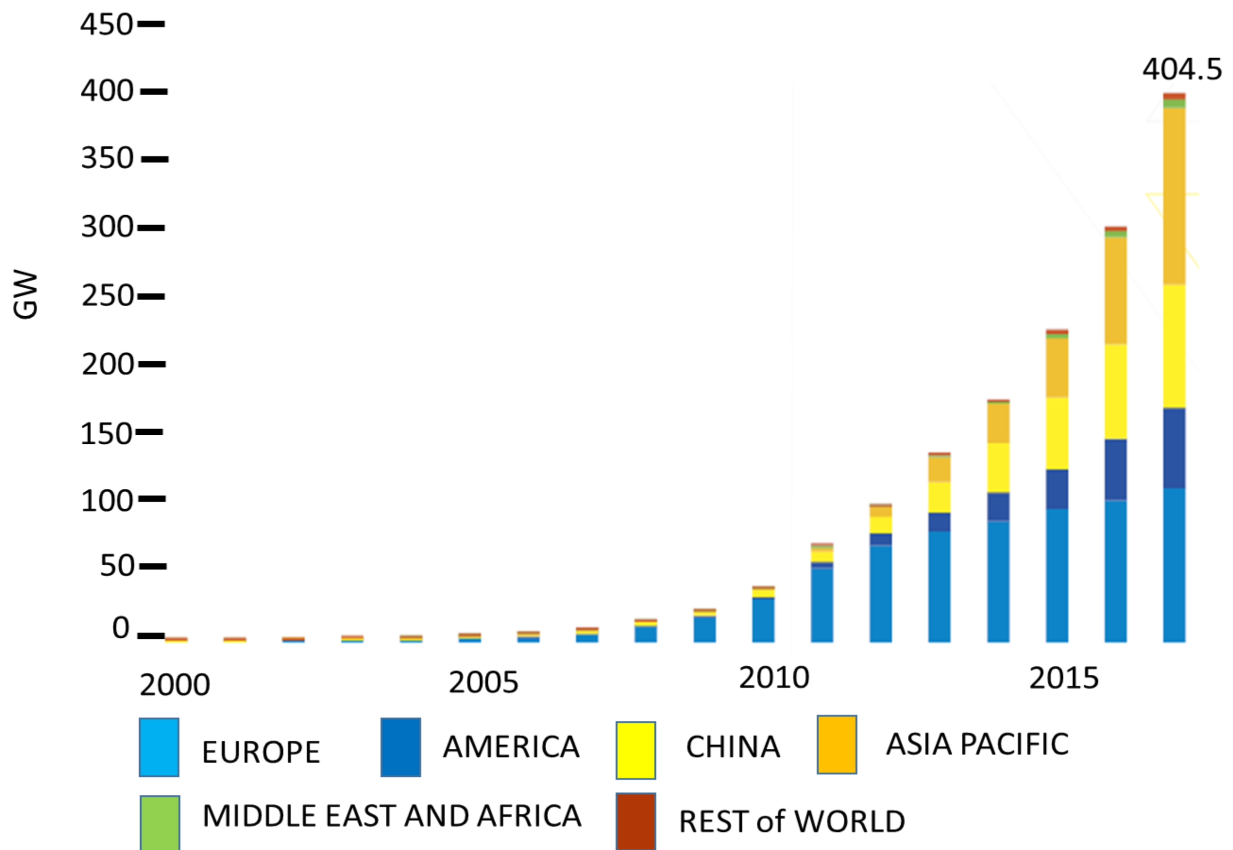

Figure 1. 1*: Annual worldwide PV installations according to EPIA* [5]

Silicon crystalline modules dominate the world market with about 95% of the market being silicon-based wafers with multi-crystalline accounting for 62% of modules produced in 2017. Multi-crystalline modules have a laboratory efficiency of about 22.3% and commercial efficiency increasing from 12% to 17% from 2007 to 2017 [8]

PV modules have a warranty of up to 30 years [9] and allowable degradation rate of 0.8% per annum based on long term photovoltaic data analysis, financial and statistical modelling undertaken on old modules [9]. Module's initial performance would be expected to drop within 72 hours of deployment due to Light Induced degradation (LID) [10].

Ordinarily modules undergo design qualification test such as IEC 61215, IEC 61730 for module safety and IEC TS 60904-13 for Electroluminescence. The aim of the qualification test is to help detect flaws the PV module may have suffered right from the factory processes, handling during transportation, storage and installation. Module degradation in the field varies greatly depending on climatic conditions (temperatures and humidity levels), PV power plant cleaning routine and surrounding human activity

[11]. Most crystalline modules located in high temperature regions suffer degradation due to discoloration of the encapsulate which promotes a higher degradation as compared to those at moderate cool environment [12]. Unprecedented degradation rates on a PV power plant over a long period of time may pose a risk of the generation of the power plant and may, in the long term, affect plant lifetime power generation and its reliability.

1.2 Summary of possible module degradation modes crystalline modules.

Figure 1.2 shows possible degradation that PV modules suffer in the course of their lifetime in the field. Modules suffer LID (Light Induced Degradation) immediately after deployment losing between 0.5-5.0 percent of the module power [13]. At infancy common module defects such as contact failures, string interconnect, glass breakage and loose frame are caused by during transportation, storage and installation [11]. At mid - life modules may suffer degradation such as Potential Induced Degradation (PID), diode failure and cell interconnect breakage [14], caused by system issues, thermo - cycling and moisture ingress. Some of the degradation modes such as EVA discoloration, delamination, cracked cells are exacerbated with module aging, leading to wear-out failure [11].

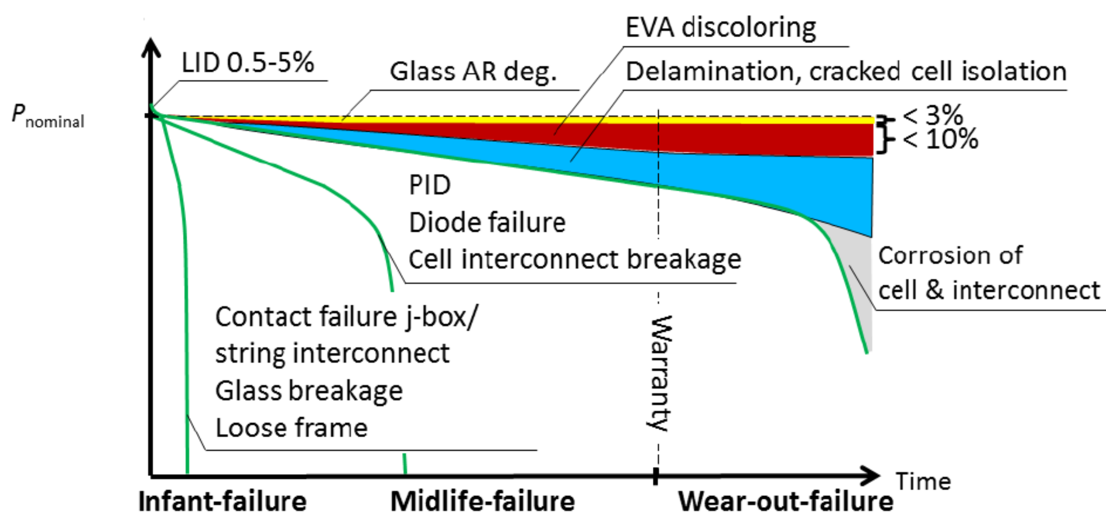

Figure 1. 2: *Wafer-based crystalline photovoltaic modules degradation scenarios, infancy, mid-life and wear out failures. LID – light-induced degradation, PID – potential induced degradation, EVA – ethylene vinyl acetate, j-box – junction box* [3].

1.3 Potential Induced Degradation (PID) and module reliability

Performance limiting defects such as PID in the modules are being managed by adjustment on the structural orientation of the module and by developing new materials to be used in module fabrication. Module reliability has attracted the attention of different PV industry players such as researchers, manufacturers, financers, insurers and investors [15]. Ordinarily PV modules of different technologies and manufactures are considered reliable and can attract insurance guarantees of up to 30 years of general liability, property and environmental risk [16].

Whereas modules are assumed to be reliable, they may be susceptibility to failures such as corrosion, delamination, cracks discoloration and PID. PID in some cases has resulted in losses of up to 30% of the initial power at string level [13]. In a PV power plant several modules are connected in series to form a string whose string voltage is the sum of voltages of individual module voltage. Modules in a string are also required to be grounded for safety reasons depending on the type of the inverter used, a high potential may develop between the frame and string's electrically active string circuitry. The potential difference can cause a leakage current to flow either from the cells to the module ground or from module ground to the cells depending whether it is n- or p-type. The consequence of PID may get worse with plans to increase string voltage to 1500 V.

PID has been an issue for a while in modules, at least during reliability test in laboratories. In 1978 Jet Propulsion Laboratory (JPL) observed PID in both crystalline and amorphous Si modules [17], and in 2005, at the SunPower Laboratory reported PID in n-type modules [18]. From 2009 much research has been undertaken, especially on conventional p-type modules [19][20]. Mitigating PID in modules has been elusive because of the complexity of causes which touches on environmental conditions (temperature and humidity), system topologies (grounding) and properties of module components such as encapsulation, ARC (Anti Reflecting Coating) and glass cover [15]. While complete elimination may be possible in future with continued research as significant proposals have been implemented to manage PID progression in strings, modules and cells. The measures are implemented to remain relevant in the cost competitive renewable energy market. This work proposes techniques to

detect PID at infancy which will play a big role in managing power failures that are associated with PID, especially at PV plant level.

1.4 Research problem

The general objective is to induce, detect and monitor PID as a PV performance limiting defect using tools such as Electroluminescence (EL), Power measurements and dark current-voltage measurement. Specific objectives are:

- (i) To Induce PID using three different approaches and quantify the PV module power degradation
- (ii) To use EL imaging to detect the onset of PID
- (iii) To utilise EL image histogram distributions to analyse PID
- (iv) To monitor power regeneration of PID degraded PV modules, naturally and by way of reverse polarity.

1.5 Thesis outline summary

This section outlines the summary overview of each of the chapters

Chapter 2: This chapter describes the basic operational principles of the semiconductor devices. The chapter describes p-type and n-type semiconductors and the formation of PN junction devices. Basic device operation that pertains to this study such as charge transport, recombination, charge collection probability, quantum efficiency and module parameters are introduced and explained. Device modelling utilises both the single- and two-diode model for device parameter extraction is also introduced.

Chapter 3: This chapter describes the cell ingot growth for multi and mono crystalline modules, the development of p- and n- type's cells, and fabrication of the modules. Description of causes, detection and prevention measures of PID are also covered. The three PID stress method used in this work are introduced and explained, as well as PID regeneration modelling.

Chapter 4: This chapter introduces physical characteristics of modules used in this investigation, the experimental details and procedures are explained in detail. The module characterization tools such as EL imaging, IR thermography, Light and Dark current-voltage (I-V) characteristics are introduced, including the type of the equipment

used. EL imaging histograms are introduced, and the formulas used in calculation of active/inactive areas and the standard deviation calculations are also presented

Chapter 5: This chapter presents results and analysis obtained from the experiments. PID detection using Electroluminescence imaging recorded at 10% of I_{sc} and normalised EL image histograms. Other PID detection tools include use of open circuit voltage under low irradiance and I-V measurements in the dark and under illumination. The PID stress results from the three methods are explained in detail. PID regeneration for both natural and forced recovery are discussed in detail including deriving an empirical function to estimate regeneration with the aim of projecting estimated performance regeneration.

Chapter 6: This chapter gives a conclusion of this study and proposes some work for future investigations on PID in PV modules.

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CHAPTER TWO

2. SEMICONDUCTOR DEVICES

2.1 Introduction

Photovoltaics devices use the principle of photoelectric effect to convert sunlight into electricity. The physics behind the semiconductor materials and diodes are discussed in this chapter. A solar cell and PV modules behave as diodes, and utilizing some of the operational principles of diodes, crystalline based modules can be characterised. The basic characterisation techniques include current-voltage (I-V) measurements and forward bias electroluminescence imaging.

2.2 PV devices

Atoms consist of a nucleus and electrons orbiting the nucleus [1]. Electrons orbit around the nucleus on allowed orbits and only exist in specific discrete levels, called the energy levels. A large number of atoms normally gather together to form a crystal [2]. The energy levels may become closely packed to form energy band. The energy bands are of two types the valance band and the conduction band [3][4]. In metals the conduction and valence bands overlap, while in semiconductors there exists a small energy gap, E_g, which separates occupied valence band from unoccupied conduction band [4].

For a semiconductor to conduct electrons in the valance band must be excited by either increase in temperature or from interaction with photons [5]. For semiconductor materials to conduct at room temperature introduction of additional energy levels through doping must be done [6]. Doping is the introduction of a group III (trivalent) atom for example boron or introduction of group V element (pentavalent) for example phosphorous into the silicon crystal structure [2]. When silicon is doped with a trivalent the three electrons will participate in covalent bonding leaving a free hole to conduct, resulting in p-type semiconductor as shown in Figure 2.1a) [1]. On the other hand, if silicon is doped with a pentavalent four electrons will participate in covalent bonding with four from the doping element the excess electron be free to conduct at room temperature hence an n-type semiconductor shown in Figure 1.2b). The band gap of pure silicon is about 1.12 eV while doped silicon has band gap of as low as 0.02 eV, the dopant introduces donor and acceptor levels within the band gap [5]. In p-type

semiconductors holes are the majority charge carriers while electrons are minority charge carries. In n-type semiconductors electrons are majority charge carriers while holes are minority charge carriers [7].

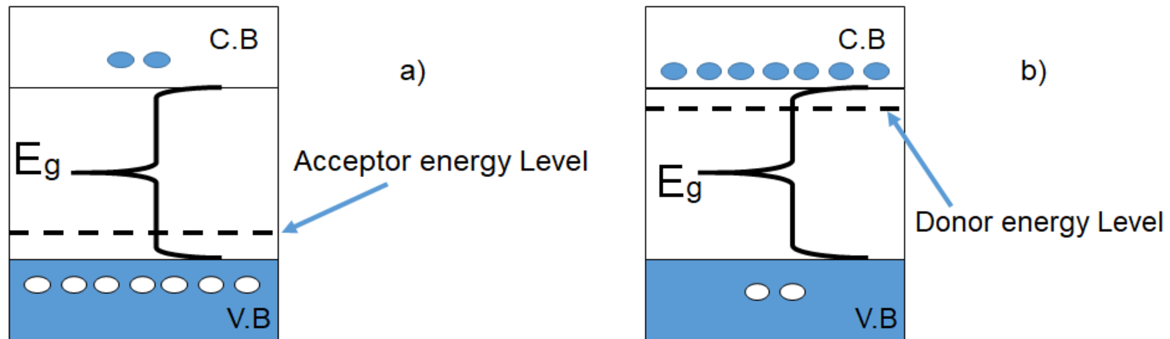

Figure 2. 1*: The band gap structure of doped p- and n-type semiconductors: a) p-type doped semiconductor. b) n-type doped semiconductor [5][6]*

2.3 The PN junction

When a p-type and n-type semiconductors are combined they create an electron hole concentration gradient. The p-type has high concentration of holes while n-type has high concentration of electrons [4]. The concentration gradient between the p-type and n-type causes electrons to diffuse from the n-side to p-side while holes diffuse from p-side to n-side [6]. When electrons and holes move to either sides of the junctions the fixed ions in the crystal lattice become activated within what is to become a depletion region resulting in a built in electric field. The built-in electric field is responsible for causing the transition zone or what is called depletion region [6].

In a p-conductor semiconductor the Fermi energy level E_{Fp} is closer to the valance band (V.B) as shown in Figure 2.2a) while in Figure 2.2b) n-type semiconductor the Fermi energy level E_{Fn} is closer to conduction band (C.B). At thermal and chemical equilibrium, the Fermi level E_F must be constant hence the V.B and C.B must adjust accordingly. V_i is the built potential, resulting from the requirement to keep the Fermi level constant in the material Figure 2.3. The energy difference between V.B and C.B is qV_i, where q is the elementary charge of an electron. The mobility of charge carriers is made possible only through drift and diffusion currents [7][8].

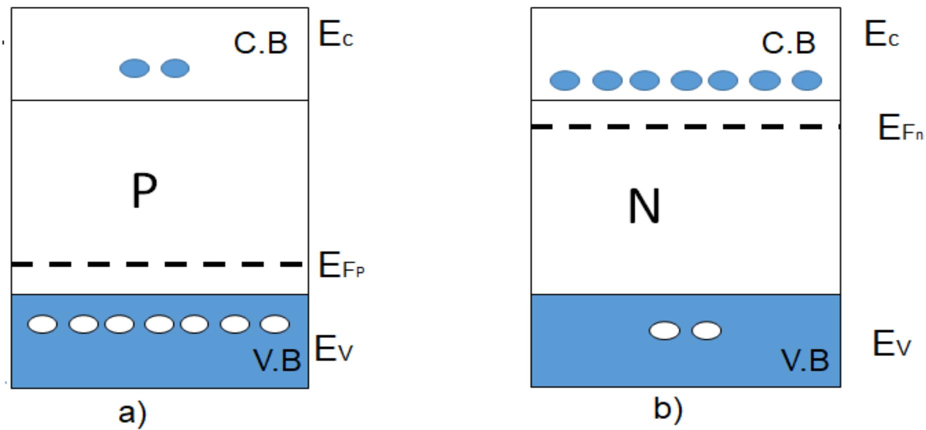

***Figure 2. 2**: Isolated p- and n- type semiconductor material energy band structure [9]*

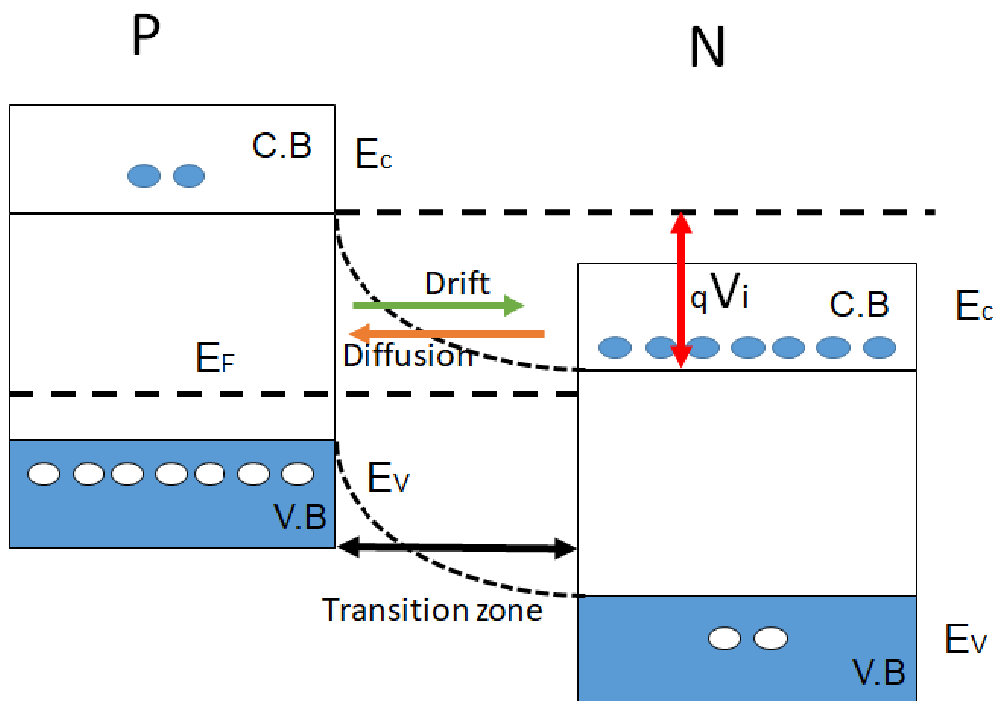

***Figure 2. 3**: The PN junction structure with band gap diagram at thermal equilibrium [9]*

2.4 Mobility of charge carriers

In semiconductor material charge carriers are forced to move either by way of an electric field (drifting) or by carrier concentration gradient (diffusion). The charges in a semiconductor can be fixed ions or mobile, for example in n-type semiconductors positive ions are fixed while majority of mobile charges are electrons *viz.* in p-type negative ions are fixed while majority of charge carriers are positive [9]. Mobile ions

are free to move from one contact device while fixed ions may only distribute within its equilibrium position. The mobility of charge carriers in a semiconductor may be determined by the strength of the electric field, doping levels in the semiconductor material and temperature [2]. In a semiconductor material charge equilibrium is reached through charge flow from a region of high concentration to regions of low concentration. The charge flow to equilibrium is governed by velocity and scattering events in the bulk of the material. The diffusion allows carriers induced by absorption and recombination to reach an equilibrium without application of external force [10].

2.5 Recombination

When electrons lose energy, they fall from conduction band to valence band where they recombine with the holes. There are three types of recombination namely Radiative, Shockley – Read – Hole (SRH) and Auger recombination [9]. In silicon solar cells Auger and SRH recombination are dominant. Any electron in the conduction band will eventually stabilize into the valence band filling in the hole that was empty this process is called recombination [11].

2.5.1 Radiative recombination

Radiative recombination is the dominant recombination mechanism in direct band gap semiconductors [12]. Most common places of radiative recombination devices include Light Emitting Diodes (LED), concentrators and space solar cell application made from gallium arsenide (GaAs), Gallium Indium Phosphide (GaInP) and Cadmium Telluride (CdTe) [9]. In direct recombination an electron from the conduction band directly recombines with a hole in the valence band and release a photon with energy equivalent to band gap hence weakly absorbed as it exits the semiconductor device as shown in Figure 2.4a) [13]. In Indirect recombination the conservation of momentum dictates that photon absorption should involve additional particles. The process of light emission involves either phonon absorption or emission. Radiative recombination in indirect recombination such as Silicon (Si) based cells and Gallium (Ge) as shown in Figure 2.4b) have a very small coefficient of recombination compared to direct recombination enabling greater penetration of light making indirect band gap unique with electroluminescence techniques used ion silicon based degradation detection technique [14][6].

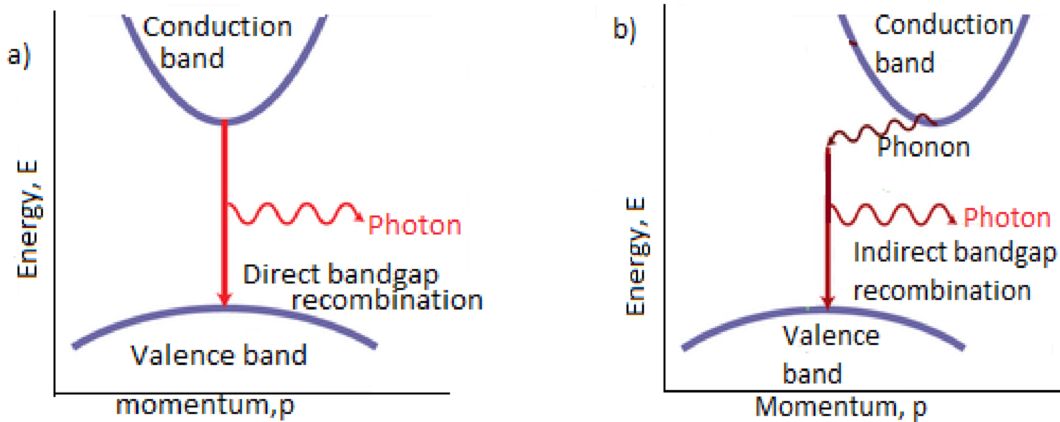

Figure 2. 4*: The energy-momentum diagram of radiative recombination [13]. a) Direct band gap. b) Indirect band gap.*

2.5.2 Auger Recombination

Auger recombination involves three carriers, when an electron and a hole recombine instead of emitting energy as thermal or a photon. It transfers the energy to a third carrier, which is an electron in the conduction band [9]. The third electron then thermalizes to the edges of conduction band [6]. Auger recombination is most prevalent in high carrier concentration due to heavy doping and injection levels [6]. In silicon-based semiconductors, auger recombination limits the lifetime and efficiency. Heavily doped materials have a shorter Auger recombination lifetime [13].

2.5.3 Shockley-Read Hall (SRH) recombination

SRH recombination occurs through defects, it takes place in two steps. In the first case an electron or a hole is trapped by an energy state in the depletion region which is introduced through introducing a dopant into the crystal lattice structure [9]. In the second case an electron moves up to the same energy state before the electron is thermally re-emitted into the conduction band which then recombines [13]. The rate of electron movement into the depletion region depends on distance of introduced energy state from the either conduction or valence band. This implies that energy state introduced closer to the either bands recombines less since the electron is likely to be re-emitted to the conduction band than recombine with a hole which moves into the same energy state. This implies that energy levels near the mid-gap (Fermi level) are very effective recombination sites [2].

2.6 Carrier properties

In a PN junction the forbidden or the depletion layer separates the n-type and p-type. Electrons are majority charge carriers while the holes are minority charge carriers on the n-type side [13]. On the p-type material minority charge carriers are the electrons while holes are minority charge carriers on the n- type material. For a solar cell to work optimally photo generated carriers on the either side must be collected by external circuit before electron-holes recombine, this is made possible by the forbidden region. To ensure status quo the carrier lifetime or the diffusion length must be made sufficiently long to ensure carrier collection [12].

When diode is not biased, there is equilibrium in carrier generation, carrier recombination, diffusion and drift currents due to the depletion at the PN junction. The electric field due to fixed ions prevents majority charge carriers from crossing the junction. Minority charge carriers which are thermally generated exist on either side of the PN junction [9]. Recombination takes place when charge carriers travel a distance, known as the diffusion length (L_x). The diffusion length relates to the carrier lifetime τ and diffusivity, D, as expressed in equation 2.1. In silicon-based PV module the carrier lifetime is large for high efficiency solar cells [15].

$$L_x = \sqrt{D\tau} \quad (2.1)$$

2.7 Charge carrier transportation

In a semiconductor material electrons and holes behave as free particles, hence subject to drift or diffusion [12]. Drift is a response of charged particles to an electric field, when an electric field is applied across a uniformly doped semiconductor, the bands bend in the direction of the electric field. The electrons in conduction band are then forced to move in the opposite direction to the field, while holes would move along the electric field i.e. electrons sink while holes float. During the drift carriers may scatter if they collide with crystals in the atom, dopant ions, crystal defects and even other holes and electrons [2]. Due to random thermal excitations, electrons and hole may move or diffuse from regions of high concentration to regions of low concentration until an equilibrium is reached, where there is no net electron current flow [13].

2.8 Collection probability

Collection probability describes the chances that photo generated electron-holes (e - h) will be collected as photo current before they recombine. The probability depends on the distance the carrier should travel in relation with the diffusion length. The probability of charge collection drops away from the PN junction, the e - h generated at the PN junction is almost guaranteed since they are collected immediately upon generation. The surface properties of the material also play an important role. Generated e - h at the surface of the emitter often surfers surface recombination hence needs for surface passivation [16].

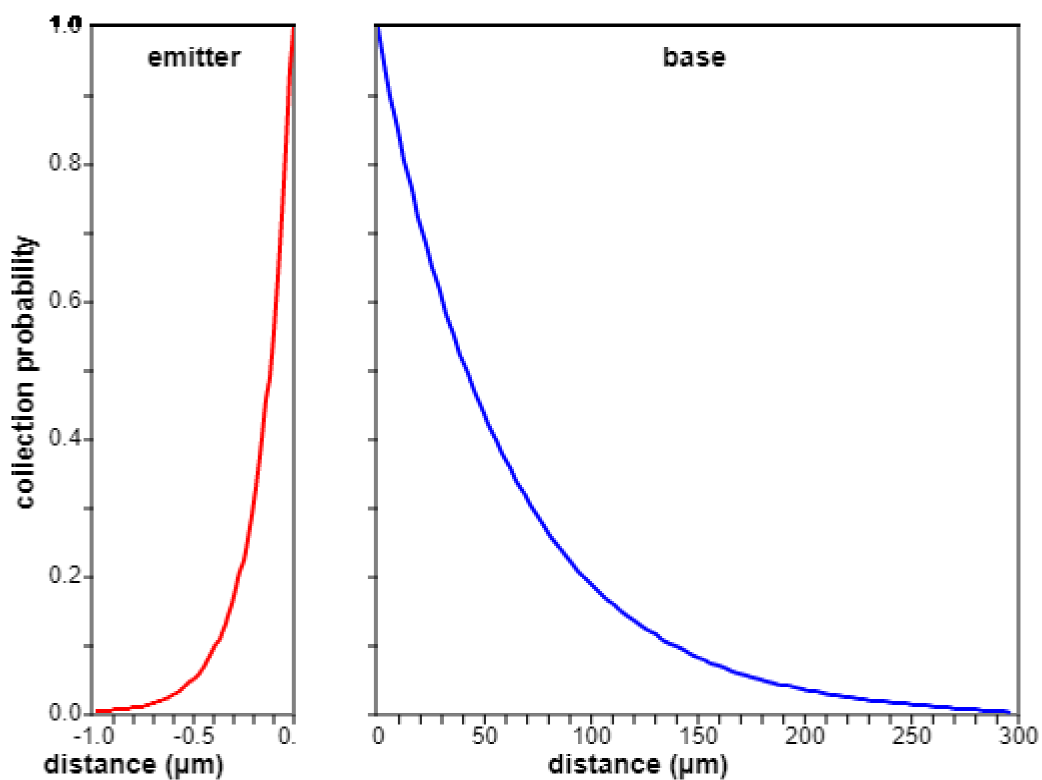

Figure 2. 5*: The diffusion length in the emitter and in the base respectively [16]*

The lifetime of minority charge carriers will be the determinant for collection to take place. For high efficiency in silicon based solar cells with indirect band gap, the diffusion length and minority lifetime must be long enough to avoid recombination as shown in Figure 2.5 [16].

2.9 Quantum efficiency

External quantum efficiency (EQE) is the ratio of collected carriers to the number of photons of certain wavelength incident on the surface of the cell [9]. EQE increases with decrease in recombination both in surface recombination and bulk [9]. Silicon for example has very low EQE in blue light region, because blue light is absorbed within few microns hence photo generated e - h generated closer to the surface hence high likelihood of surface recombination. Quantum efficiency is mainly affected by the minority carrier diffusion length and recombination velocity. Internal Quantum efficiency (IQE) refers to photons that are reflected or transmitted out of the cells capable of generating collectable carriers. By quantifying devices reflectance and transmission, IQE can be derived from the EQE efficiency as shown in figure 2.6 [17].

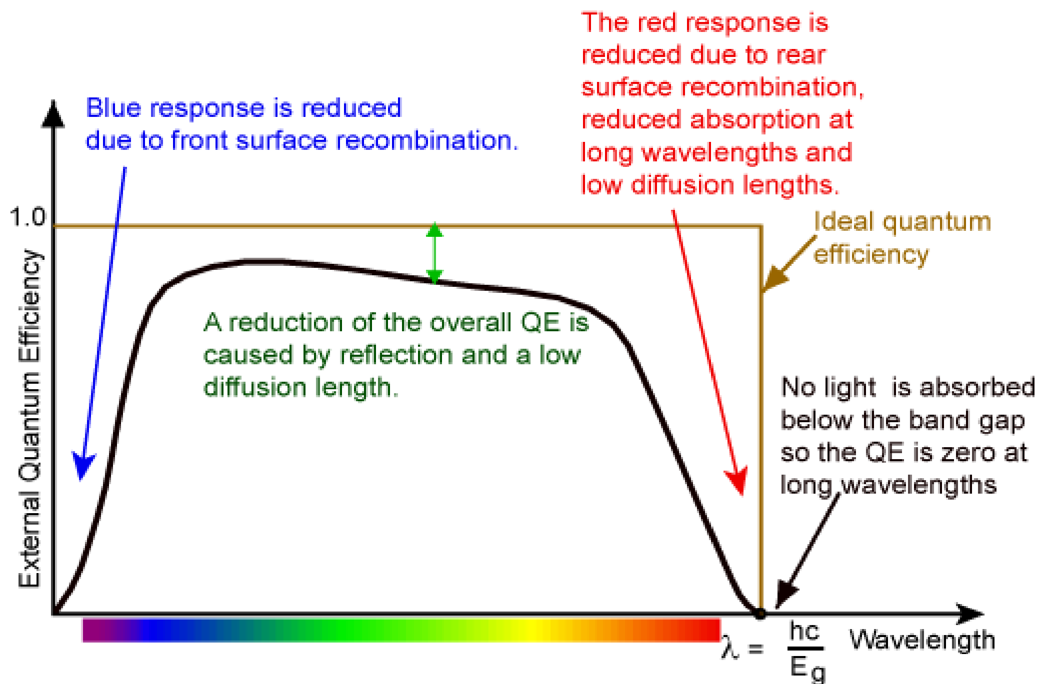

Figure 2. 6*: Silicon quantum efficiency [17]*

2.10 Diode Under forward bias

A diode is in forward bias when voltage is applied on the device in a manner that the electric field developed reduces the depletion layer [2]. The p-type is connected to the positive while the n-type is connected to the negative terminal of the power source. The electric current will flow in the opposite direction to the electric field in the depletion layer [1]. Reducing the electric field disturbs the junction equilibrium hence decreasing

the potential barrier at the junction resulting in increased diffusion current. The drift current would remain unchanged because it depends on carriers generated by diffusion from one side of the junction to another [1]. The number of minority charge carriers remains the same on either side of the PN junction since the reduction in depletion layer width is small as shown in Figure 2.7 [7].

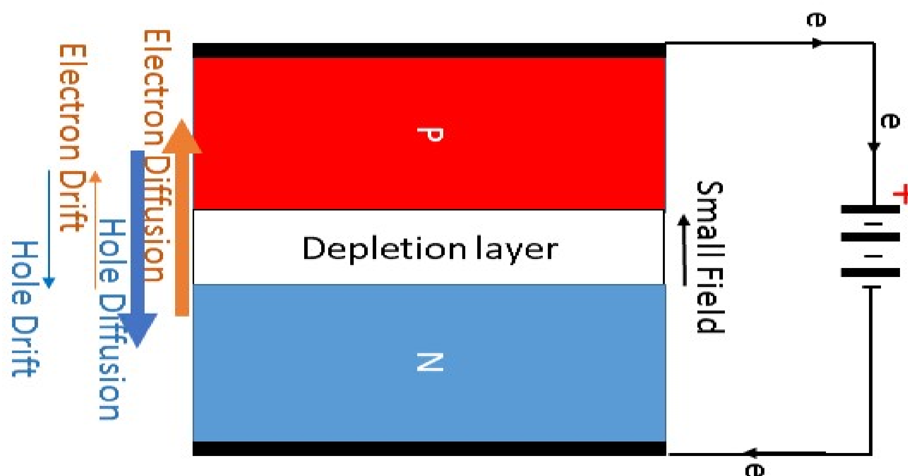

***Figure 2. 7**: Behaviour of solar cell in forward bias [7]*

2.11 Basic principles of electroluminescence (EL) imaging

EL imaging depends on the principle of radiative/non radiative recombination. During EL imaging the module is connected in forward bias. Minority charge carriers are then injected into the p-side of the PN junction where they undergo radiative recombination. The emitted EL spectrum is between 900 nm to 1300 nm[18]. The number of minority charge carriers in a cell will determine the intensity of EL signal. Regions within the cells which appear darker undergo undetectable recombination. Such regions are potential defect areas in a cell [19]. The minority carrier concentration at the junction is given by equation 2.2

Under forward bias, electrons are injected at the p-side of the p-n junction and the distribution of these minority carriers (electrons) in the p-side of the p-n junction is discussed in this section.

The minority carrier concentration, n_p, at the junction (x=0) is given in equation 2.2 and is dependent on the intrinsic carrier concentration, n_i, the doping concentration of the base, N_A, applied junction voltage, V, the Boltzmann's constant, k, the temperature , T and the electron charge, e [18].

$$n_p(0) = \frac{n_i^2}{N_A} \exp\left(\frac{eV}{kT}\right) \qquad 2.2$$

The injected excess minority carrier concentration at a distance x, from the junction is given in equation 2.3 and is determined by the equilibrium minority carrier density at the junction $n_{p(0)}$ and the Diffusion Length (L_e).

$$n_{p(x)} = n_{p(o)} \exp\left(\frac{-x}{L_e}\right) \qquad 2.3$$

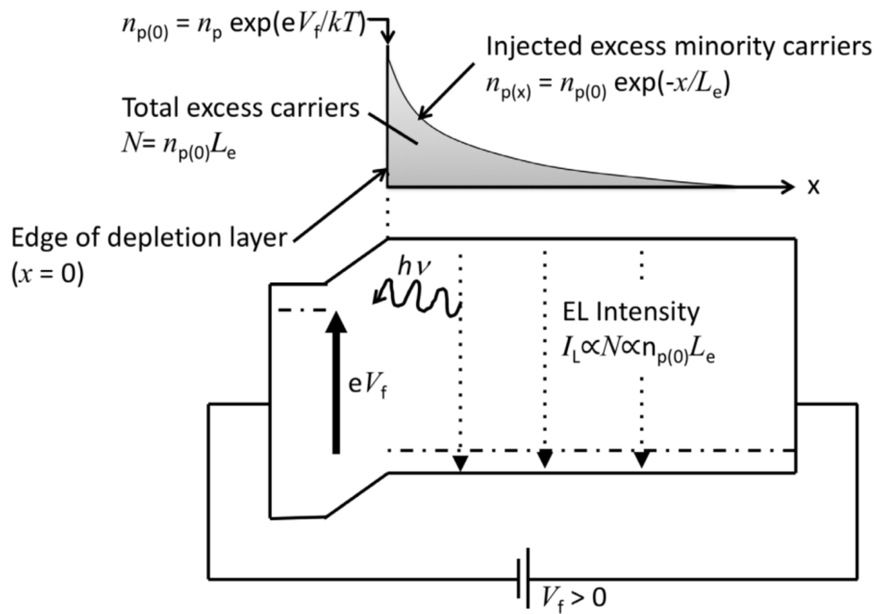

Figure 2. 8*: Emission of light associated with electroluminescence in PV modules [20]*

Figure 2.8 describes the number of minority charge carriers at the junction and the change in the number of charge carriers as distance increases away from the PN junction [20].

2.12 Solar cell models

Behaviour of solar cells of solar cells have been modelled using a two-part system i.e under solar illumination and in the dark. The model under solar illumination has photo current generation, while the model in the dark has no photo currents. Under illumination the solar cell is assumed to act under direct PN junction carrier injection whereas the solar cell in the dark operate in charge recombination with small diffusion currents. Two models are discussed in this section that is single diode model and two

diode model which accounts for solar cell recombination processes in the dark and in the light [9].

2.12.1 Single exponential model

The single model consists of a photo current, a diode, a parallel resistor representing leakage current and a series resistance representing internal resistance to current flow. The one diode solar cell dark equation is given in 2.4 and illustrated in Figure 2.9a).

$$I = I_L - I_0\left[\exp\left(\frac{q(V-IR_S)}{nkT} - 1\right)\right] - \left(\frac{(V-IR_S)}{R_{sh}}\right) \qquad 2.4$$

Where I_o represents the diode dark saturation current, n is the ideality factor, T is the PN junction temperature, k is the Boltzmann constant, V is the applied voltage and IR_s is the voltage measured across the series resistor [21].

Under illumination the diode expression introduced the photo current term is introduced and its *I-V* characteristics is as expressed in the Equation 2.5

$$I = I_o\left[\exp\left(\frac{q(V_d)}{nkT} - 1\right)\right] - \left(\frac{V_d}{R_{sh}}\right) - I_L \qquad 2.5$$

Where; I_L is photo-induced current with direction opposite to that of the dark current and V_d is the diode voltage. Since I_L is greater than the dark current, the net current generated by the cell is in the direction of I_L. Hence, the diode voltage expressed with respect to measured voltage, V was given as $V + IR_S$ and the light-IV characteristics can be written as shown in Equation 2.6 and illustrated in Figure 2.9b)

$$I = I_L - I_0\left[\exp\left(\frac{q(V+IR_S)}{nkT} - 1\right)\right] - \left(\frac{V+IR_S}{R_{sh}}\right) \qquad 2.6$$

The Equation 2.4 is useful when analysing dark-IV characteristics while Equation 2.5 gives light-IV characteristics that are used to define, calculate and analyse solar cell device and performance parameters. Figure 2.9 shows one diode equivalent solar cell under illumination and in the dark.

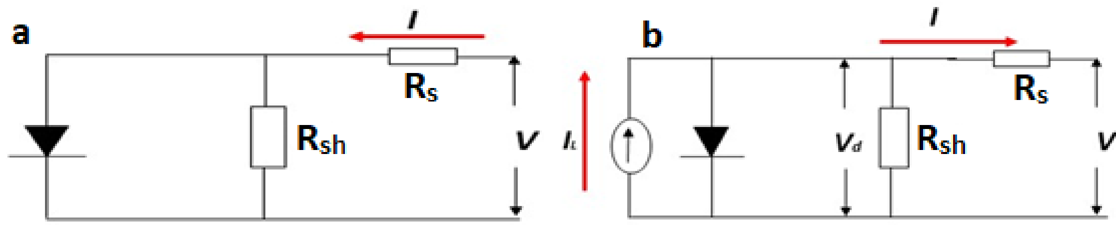

***Figure 2. 9**: The schematic illustration of a single diode equivalent solar cell circuit when a) in the dark environment b) under illumination.*

2.12.2 Two diode model

Single diode equation assumes single ideality factor *n*. In reality the ideality factor is influenced by voltage across the devices. At high voltages surface recombination dominates while at lower voltages the bulk recombination dominates hence two diode model gives $n_1 \approx 1$, while n_2 is a value ≈ 2. The two diodes also describe two saturation currents I_{01} and I_{02}. The dark-IV equation is as shown in equation 2.7

$$I = I_{01}\left[\exp\left(\frac{q(V-IR_S)}{n_1kT}-1\right)\right] + I_{02}\left[\exp\left(\frac{q(V-IR_S)}{n_2kT}-1\right)\right] - \left(\frac{V-IR_S}{R_{sh}}\right) \quad 2.7$$

Where I_{01} and I_{02} are saturation currents which depend on processes corresponding to diode quality factors $n_1$and n_2 and the voltage V measured or applied in the dark. The Illuminated light-IV characteristics can be expressed as equation 2.8.

$$I = I_{01}\left[\exp\left(\frac{q(V_d)}{n_1kT}-1\right)\right] + I_{02}\left[\exp\left(\frac{q(V_d)}{n_2kT}-1\right)\right] + \left(\frac{V_d}{R_{sh}}\right) - I_L \quad 2.8$$

In this equation the diode voltage (V_d) can be expressed as $V + IR_s$ and the inverted light-IV characteristics will be as represented in equation 2.9.

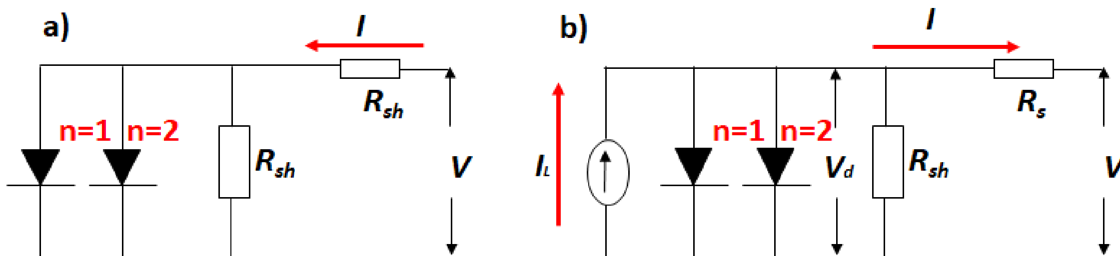

***Figure 2. 10**: The two-diode model schematic representation a) two diode equivalent solar cell circuit when in the dark environment b) when under illumination.*

$$I = I_{01}\left[\exp\left(\frac{q(V+IR_s)}{n_1 kT} - 1\right)\right] + I_{02}\left[\exp\left(\frac{q(V+IR_s)}{n_2 kT} - 1\right)\right] - \left(\frac{V+IR_s}{R_{sh}}\right) \quad 2.9$$

The two-diode equation has a limitation at higher efficiency because the number of charge carriers increase with the applied voltage, resulting in a dramatic change in rear surface recombination, complicating ideality factors in two diode model which depend on surface and bulk recombination. In this work the single diode model parameter equation was used to extract light-IV module parameters, using particle swarm optimization algorithm (PSO) to extract the module light-IV characteristics before and after PID stress [22]. The comparison is essential in estimating the severity PID degradation on module performance of parameters such as open circuit voltage V_{oc}, maximum power point, shunt resistance (R_{sh}) and series resistance (R_s) [22][23].

2.13 Module I-V curves and Solar cell parameters

The electrical characteristics of a module are obtained when a curve of current against applied voltage is plotted under illumination. The curve normally occurs at the fourth quadrant, but it is inverted to the first quadrant. In a light-IV curve maximum power point P_{mpp} is found at a point when the product of current (I_{mpp}) and voltage (V_{mpp}) is maximum. When Voltage is zero (*V=0*), the current is at short circuit current (I_{sc}), similarly when the current is zero (I=0), the voltage is at open circuit voltage (V_{oc}).

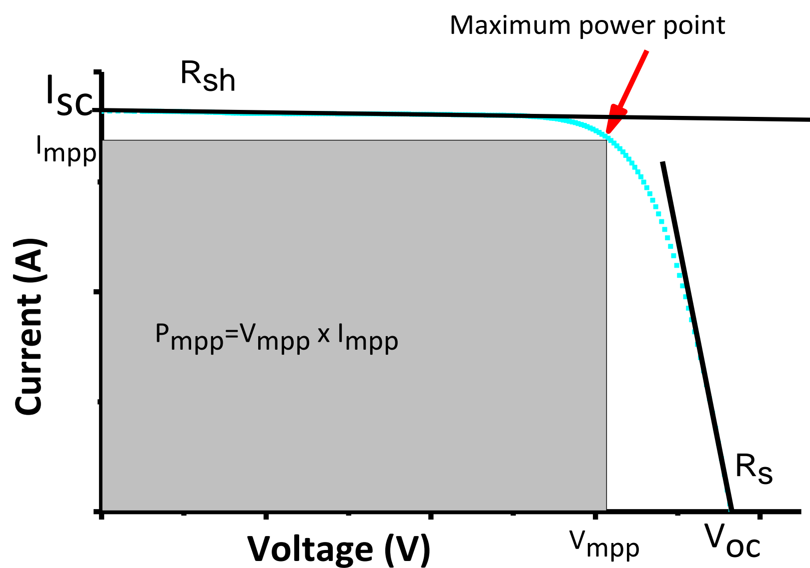

***Figure 2. 11**: Characteristic IV curve of a PV module; I_{sc}-Module short circuit current, I_{mpp}- current at maximum power point, V_{mpp}-Voltage at maximum power point, V_{oc}-open circuit voltage. R_s- Series resistance region and R_{sh}-shunt resistance [6]*

Light-IV curve measurements are done using indoor solar simulator measurements system. The standard test condition (STC) for power measurement are 1000 W/m^2 and 25 °C and A.M 1.5. The I_{sc} may be equivalent to photo generated current (I_L) under ideal condition but may decrease with increase in R_s or leakage current. The V_{oc} is the measure of strength of the bias at the PN junction caused by I_L. Fill Factor (FF) is obtained as a measure of the ratio between maximum power to the product of I_{sc} and V_{oc}. FF gives an indication of the impact of series R_s and shunt resistance R_{sh} on the I-V curve shape. R_s may occur along the metallization and external cabling, bulk, emitter, contacts and bus bars. The net impact of R_s is to limit current output and cause a drop in voltage. The increased R_s is observed as flatted I-V at the 'knee' and at very high resistance the light-IV curve would resemble an Ohmic graph (a linear graph from I_{sc} to V_{oc}).

The module current output is directly linked to irradiance levels. Lower irradiance levels or shading decreases the current output of the module. The decrease can also be occasioned by module encapsulant discoloration or if cells in multiple strings are badly damaged. Damage to a section of the cell(s) would impact negatively on the current levels since the effective area of photo current generation is reduced.

Solar power plants are constructed using solar PV modules comprising of either 60 or 72 cells connected in series. The total voltage output of a solar PV module is the sum of the individual cell's V_{oc}. Modules that output a lower than expected V_{oc} may be due to shunting, faulty interconnection or bypass diodes and increased temperatures. Light-IV curves may have steps especially at lower voltages, this may be caused by mismatch of current in the strings resulting in bypass diode activation. Multiple cracks on a cell my lead to localised heating on a cell activating the bypass diode. The gradient taken at low voltages near I_{sc} represents R_{sh}. A decrease in R_{sh} results in a steeper gradient. At high voltages the slope represents R_s. A less steep slope represents the undesired high series resistance which may be as result of poor soldering, soiling or bad contacts and junction box [25].

2.14 Summary and conclusion

This chapter discusses the theoretical processes and mechanisms that describe basic solar PV module operation. The solar PV module is a diode whose operation is governed by single diode or two diode model. The recombination mechanism inside

the module is of significance especially in techniques such as electroluminescence measurements when the module is connected in forward bias. Charge transportation mechanism is crucial in understanding the module operation especially under illumination. Processes such as charge transport, recombination, collection probability and quantum efficiency summaries e - h generation in a solar PV device and determines device efficiency. Module parameters such as FF, I_{sc}, V_{oc}, P_{mpp}, I_{mpp}, R_{sh} and R_s are introduced and explained in the last section. It's imperative to note that PID defects, affects parameter such V_{oc} (especially at low irradiance), P_{mpp}, FF, R_{sh} and R_s.

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CHAPTER 3

3. POTENTIAL INDUCED DEGRADATION – MECHANISMS, DETECTION AND PREVENTION

3.1 Introduction

Potential Induced Degradation (PID) is a form of module degradation that occurs due to the high system voltages experienced by modules in PV plants. PID susceptibility is determined by the cell technology, module construction and string configuration. This chapter starts with an introduction into these concepts. Manufacturers have made structural adjustments to the cells, modules and system topologies in order to manage the power drop caused by PID. This chapter discusses the manufacturing process of silicon-based modules and PID as performance limiting defects in detail.

3.2 PV cell technologies

3.2.1 Monocrystalline cells

Monocrystalline silicon has an ordered crystal lattice structure that is assumed to be defect free [1]. The cells are of high quality and are better performing than multi-crystalline under optimum controlled conditions. The disadvantage associated with monocrystalline solar cells is the cost of the complicated manufacturing process. Two of the most common methods used in growth of single crystalline silicon are; the Czochralski (CZ) and the floating zone (FZ) methods. The processes involve growing monocrystalline material by way of seed contact with molten silicon [1][2]. In CZ method a monocrystalline seed crystal is brought in contact with molten silicon allowing crystalline lattice to propagate as the seed is pulled up gradually while undergoing slow rotary motion [3][4]. The monocrystalline boule growth condition would determine the quality and energy efficiency of the resulting monocrystalline cell [5]. The single crystalline boule is sliced into thin wafers of less than 400 µm [6], after which they are processed to fabricate solar cells for integration into a PV module.

3.2.2 Multi-crystalline cells

The multi-crystalline silicon (m-Si) cells are cast from pure molten multi-crystalline silicon material into square shaped block ingot [3]. The ingot is sliced into thin wafers

using a diamond infused wire [6]. The m-Si are formed in square wafer cells implying that there is less material wastage [3]. Lack of additional crystal growth steps reduces the cost of production; however, this implies that the m-Si cell has more imperfection (defects) which may limit charge carrier mobility resulting in reduced cell performance and conversion efficiency. The imperfection in m-Si cells manifest itself as grain boundaries and crystal dislocations. Grain boundaries create possible regions of local carrier recombination, reduced carrier lifetime and increased local diffusion current densities [3].

In the lattice structure the grain boundaries are visualised as the interface between two different crystal orientations [3]. Dislocations may result from mechanical or thermal stress gradients during ingot growth and wafer slicing [5]. The dislocation and grain boundary defects in cells may have a compounded effect of reducing the I_{sc} and V_{oc} of m-Si modules. Multi-crystalline modules are made from cell material with large and unequal grains in the crystal structure oriented at different planes. This gives m-Si a heterogeneous appearance with a blue hue depending on the grain's crystal orientation [3].

3.3 Module construction

3.3.1 Cell preparation

The wafers are processed into either p-type or n-type cells for use in a module. For p-type cells the wafer is doped with phosphorous, then boron is diffused from one side until its concentration exceeds the phosphorus [2] [3]. Similarly, for n-type the wafer is doped with boron, then phosphorous is diffused into the wafer from one side until its concentration exceeds that of boron [1][3]. P-type cells have the advantage of being resistant to space radiation and degradation hence modules fabricated from it can be deployed for outer space exploration [3]. Alternatively, n-type cells are immune to boron-oxygen defects which decreases the efficiency in p-type modules. The n-type modules are more efficient and are immune to light induced degradation (LID) [3]. Fingers and busbars are then screen printed on the front surface of the cell and then annealed. The back of the cell has an aluminium alloy applied on as the base [3].

3.3.2 Crystalline Silicon module construction

A PV module comprises of cells soldered in series connected strings, as shown in Figure 3.1. Each of the strings has a bypass diode connected across it, so that in an event of cell mismatch the bypass diode will be activated and minimise the power losses.

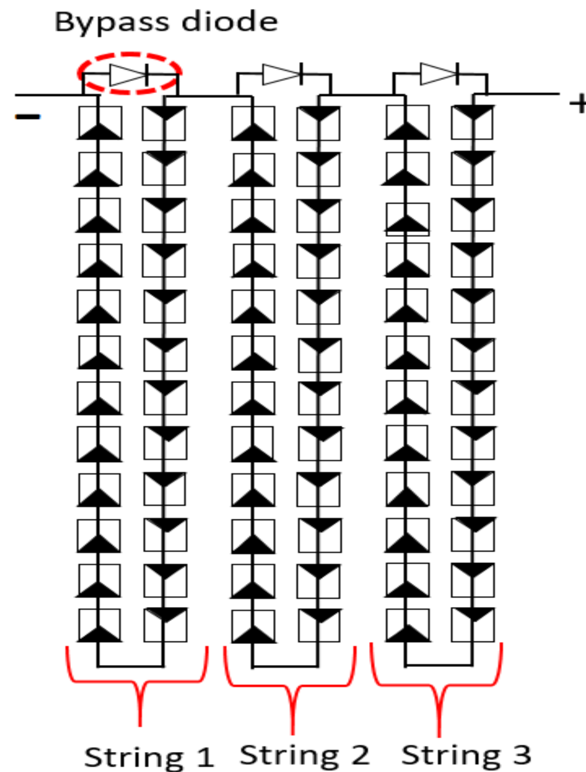


Figure 3. 1: *PV module configuration, for a 72 cell modules arranged in 3 string each of 2 cells. Three bypass diodes are connected across each string.*

Most PV modules in use today comprise of a glass surface, the solar cells that are sandwiched between two polymeric encapsulation layers and the back sheet shown in Figure 3.2 [7]. The glass surface provides mechanical stability, high transparency, good spectral response and environmental protection of the cells and metallization from external impacts [8]. The encapsulation provides mechanical stability to silicon cells which are brittle in nature. In many modules, EVA (ethylene vinyl acetate) is chosen due to its good UV stability and better glass adhesion to minimise chances of delamination. The back sheet which is generally a permeable polymer, provides mechanical stability and electrical safety. The ARC increases photon absorption and prevents surface reflection [9].

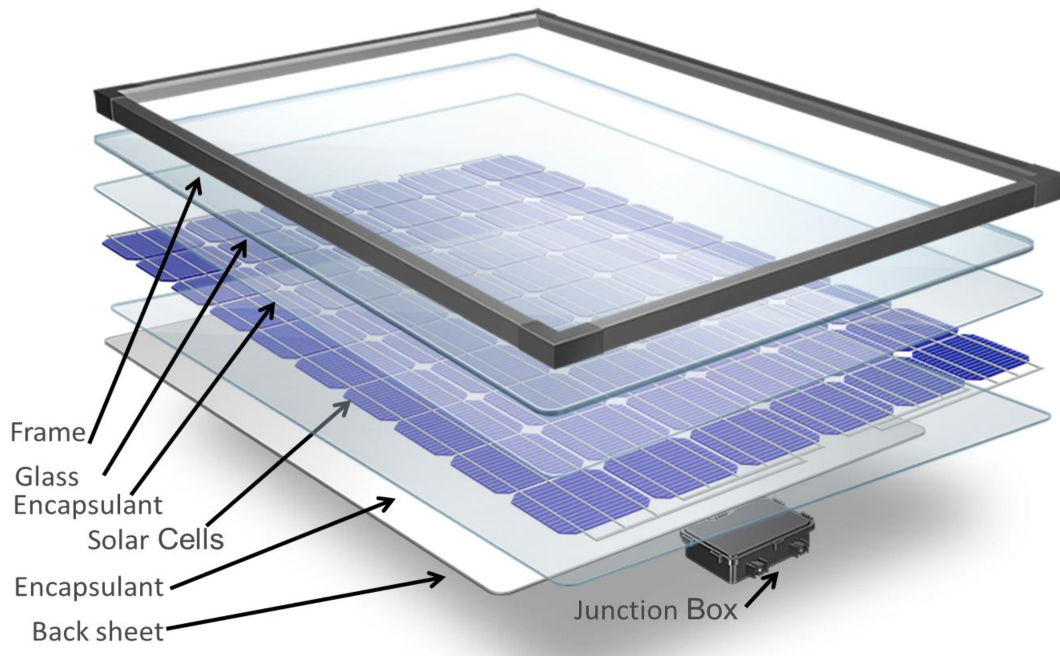


Figure 3. 2: *A sample structure of a 60 cell monocrystalline module; comprising of the frame, glass cover, encapsulant, back sheet and junction box* [7]

In order to produce a required system string voltage, PV modules are connected in series. The number of modules and thus the magnitude of the string voltage, vary from one PV power plant to another. A large string has the advantage of mobilizing a higher system voltage leading to low yield losses, efficient power transmission and the potential for reduced installation and maintenance cost [10][11]. PV power plants are capital intensive and as such the modules deployed should be durable and reliable enough for the duration of the contract which falls between 25-30 years [12]. Figure 3.3 below shows a string with 14 modules (3.5 kW system), with a total output voltage of 516.6 V and current of 8.25 A.

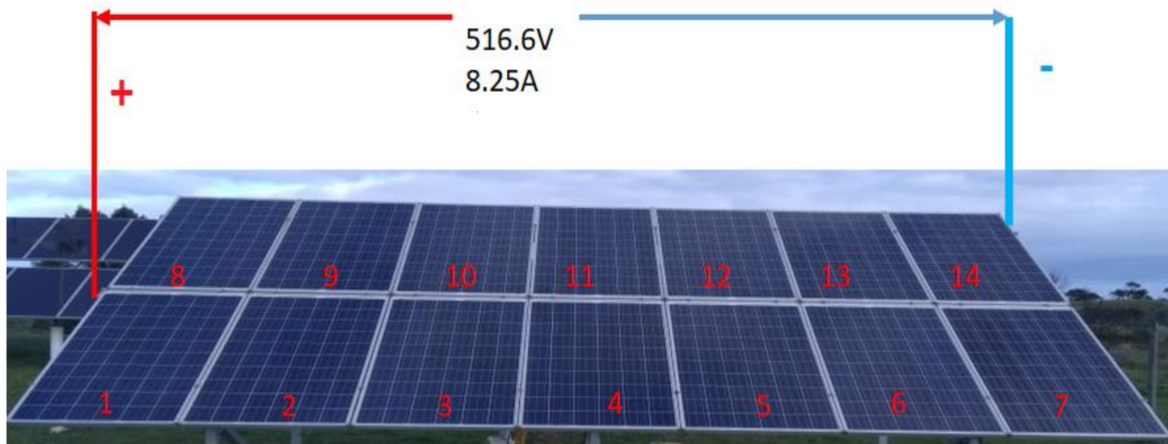


Figure 3. 3: *A 3.5 kW module string at Outdoor Research Facility at Nelson Mandela University, string Voltage 516.6 V and current of 8.25 A.*

3.4 Potential Induced Degradation (PID)

3.4.1 PID overview

In 1978 at the Jet Propulsion Laboratory PID stress factors was first observed [13]. The degradation was as a result of voltage stress exerted between the frame and the cells. In 2005, a similar effect was observed on n-type modules at SunPower laboratories [14], as the number of large solar power grid tied systems became a reality with reduction in module prices there was increased interest in PID stress [9]. The degradation was associated with negative potential which gave rise to PV module cell current shunting due to positive ions accumulation and forming a layer beneath the ARC resulting in decreased R_{sh} and increased R_s, of the affected modules [15]. These results were confirmed when shunting regions showed Na^+ accumulation and other alkali ions such as potassium (K^+) within the ARC and stacking faults across the PN junction which provide Na^+ diffusion channels [16]. Drifting Na^+ from glass surface to the ARC require a large electric potential of nearly 1000 V. Upon reaching the cell-ARC interface they spontaneously diffuse into the stalking faults creating an electrically conductive layer which causes the PN junction to behave like it had short circuits [17].

Hara *at el.*, 2015 [18] reported PID in n-type modules where positive charge (K^+) centres are trapped within the ARC as opposed to Na^+ which accumulate for the case of p-type modules. This kind of PID shunting was found to be reversible and may be avoided by grounding the negative terminal of the PV array, which would automatically impose positive potential to all modules in a string [9] [18] [19]. In a PV module PID

progresses as a dynamic process because the size of leakage current flowing between the ground and cells causing displacement of ions depends on the applied voltage and the resistance in the path between individual affected cells and the grounded frame. Under outdoor PV operating conditions, the surface of the glass plays the role of a major leakage current pathway. In the morning, the glass is more conductive due to dew accumulation on the glass surface, this can be replicated on rainy days where the glass bulk and encapsulation become more conductive than on dry days [20].

Surface soiling may play a significant role by creating a humidity matrix which behaves like a sponge which extend to the grounding resulting in increased leakage currents [9]. As the day progresses the dew evaporates and the resistance to leakage current increases to very high value halting the leakage current [21]. As the temperature increases, PID recovery takes place at the module operating temperature and high solar irradiance [22]. At night the module PID recovery may still be possible even with the presence of dew on the module's glass surface [23]. Module recovery during the day at higher temperatures is much higher than PID recovery during the night at low temperatures [9]. Accelerated PID recovery can be done at night on a power plant using reverse polarity using commercial anti-PID devices. PID lowers energy yield output of a power plant and increases the mismatch losses which if uncorrected my quickly develop into hot spots especially shunted cells.

PID will not develop in a PV system where recovery surpasses the PID stress. The balance between module PID recovery and PID stress become evident with time as the module is deployed to the field for continued operation under harsh environmental conditions [21]. The PID degradation may be influenced by intrinsic characteristic of PV module technology, PV array grounding scheme and system operation voltage which can be up to 1500 V on multi-megawatt PV plants [23]. If PID continues for a long period of time, irreversible electrical corrosion might take place which may require module replacement [4].

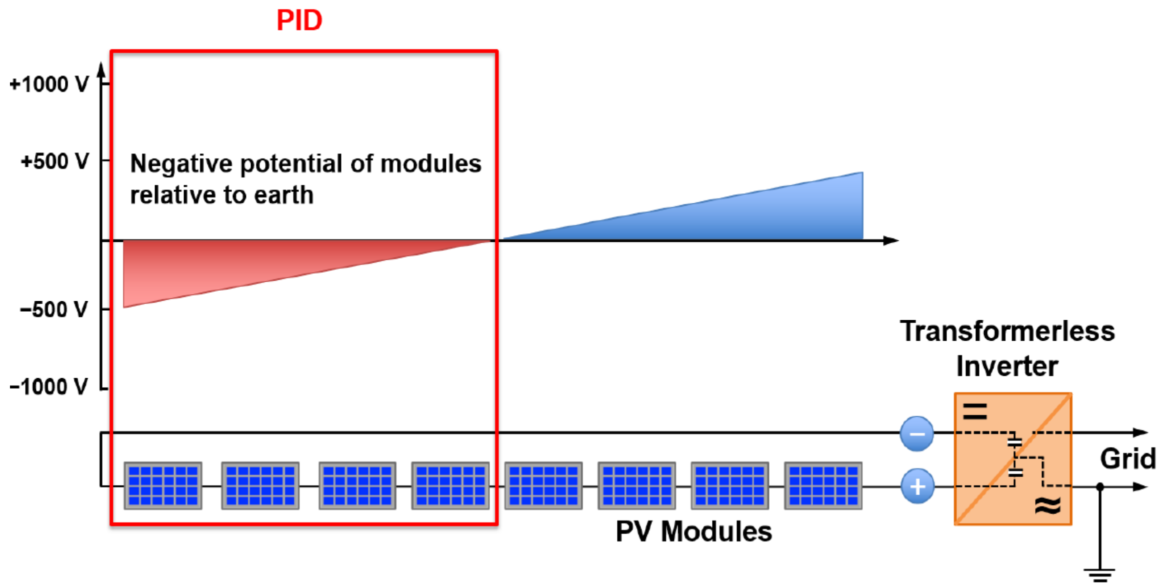
3.4.2 PID at system, module and cell level

PID defects are observed in modules with both n-type and p-type cells at cell, module and string level. The polarization is caused when a high potential develops between the cells and the module frame. Many factors contribute to PID progression which may include environmental factors (temperature and humidity), at module level the type of

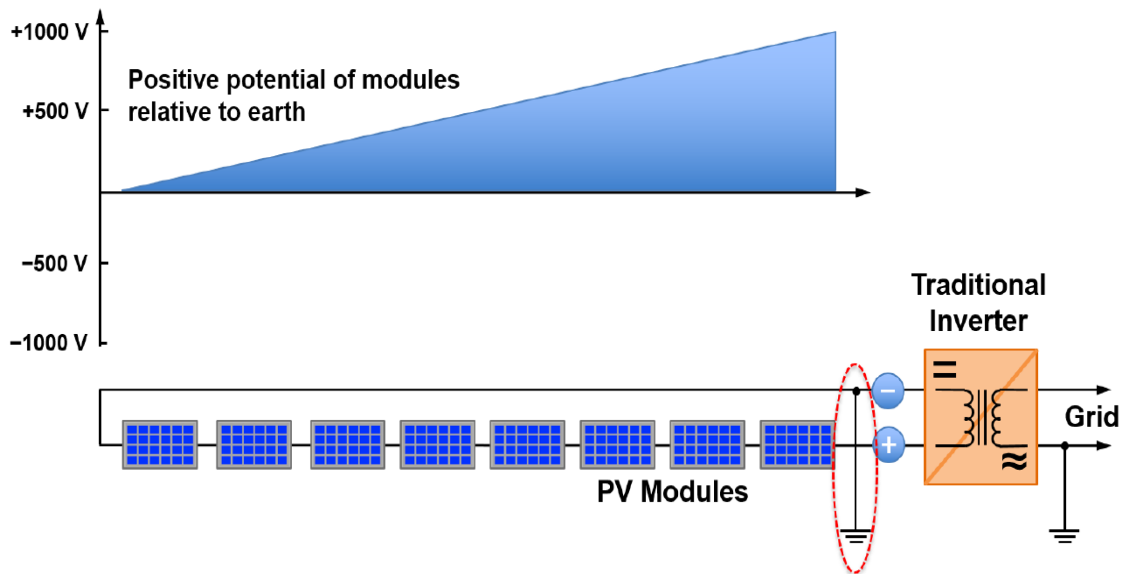
glass, encapsulation, ARC and cells may determine module PID susceptibility. At string or system level the string voltage and type of earthing would play a role.

3.4.2.1 String level

The size of system voltage is determined by the number of modules connected in series on a string [17]. The string voltage should be designed not to exceed the allowed module system voltage currently set at 1000 V or 1500 V [24]. The type of grounding of the string plays an important role in deterring PID. Three common grounding configurations are used; positive pole grounding, negative pole grounding and no grounding (floating) are used in PV systems depending on inverter capabilities. Whenever a string is not grounded its potential is said to be floating and half of the system is at positive potential while the other half is at negative potential as shown in Figure 3.4. PID affects modules only on the negative potential end of the string[25], [26]. Floating potential is observed when a transformerless inverter without grounding capability is used in a string as shown in Figure 3.4 a). For either positive or negative grounding the naming depends on grounding pole and the type of modules used either n-type or p-type. Figure 3.4b) shows a string of 8 modules that are well grounded. The inverter used isolates the string circuit and the grid circuit hence minimizing chances of high potential developing between the frame and the string circuitry.



a)



b)

Figure 3. 4: *Comparison of Transformerless Inverter with Transformer Inverter in a PV System a) Transformerless inverter, b) Traditional inverter* [25].

In a floating string affected by PID, the string p-type modules on the negative end will be the most affected as shown in EL image shown in Figure 3.5 [26].

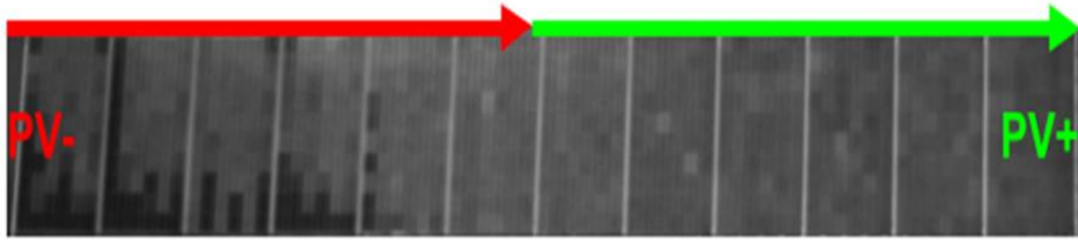


Figure 3. 5: *EL image of PID affected string, modules on the negative side are affected by PID* [26].

3.4.2.1.1 String characterization methods

PID stressed modules in a string can be characterised by taking EL images, IR thermography images or L-IV measurements. In an EL image modules at the negative end will show a checkerboard pattern of black and white on grey scale as observed in Figure 3.5, IR thermography images will show PID affected cells warmer than the rest of cells in a module or string. L-IV measurements will show decreased P_{mpp} and in the worst case or under low irradiance the V_{oc} will drop drastically due to current saturation and increased charge recombination within the cell crystal structures. PID degradation may be prevented by grounding a negative pole of the string if the pole is fixed. Even though the system in Figure 3.4 b) is well grounded there is no guarantee that it will be PID free because other defects in long term such as discoloration and cell interconnect breakage may degrade the module [25].

3.4.2.1.2 PID prevention measures at a system level

In a PV system, inverters are used to convert DC power generated to AC power for transmission into the grid. Two inverter protocols are used, transformer based and transformerless inverters. For transformer-based inverters either positive or negative system pole is grounded leading to either positive or negative bias relative to the ground. In p-type negative bias in relation to the ground results in PID, hence need to prevent this by grounding the negative system pole bring all modules to positive bias hence eliminating the danger of PID shunting from taking place [25].

In the recent past most PV power plants uses transformerless topologies because they are light and have a higher conversion efficiency compared to transformer-based inverter of up to 2% [27]. The disadvantage of transformerless inverters is the absence of galvanic isolation between the string circuit and they also have no grounding. This

results in a floating potential which implies that half of the modules are negative bias while the other half is positively biased. PID in a floating system can be prevented by applying a positive voltage bias at night to recover the power efficiency lost during the day [28]. This measure can also be used in transformer-based system, but it may require additional electronics. Another way to prevent PID in a transformerless inverter system is to use virtual DC bus concept that allows negative system pole to be virtually grounded resulting in all cells shifting to the positive potential. In some cases, micro inverters have been employed where each module is connected to an inverter, while this approach may optimise voltage output of each module effectively, it is however, costly. Because PID is associated with high system voltage of 1000 V between the ground and the string active circuitry the use of micro inverter may be a long-term solution to PID since it will have a system voltage equivalent to modules' V_{oc} [29][25].

3.4.2.2 Module level

The magnitude of the leakage current between the frame and cells depends on temperature, humidity, type of the encapsulation and electric potential between the cells and the frame. Potential between the cells and the frame causes charge carriers (ions) to drift to cell surface and at the right concentration may diffuse into the PN junction. As module operating temperature and humidity increases the leakage current between the cells and frame increases [30][31]. Under high humidity the surface of the glass, the glass bulk becomes more conductive, making it responsible for most of leakage current to the frame. At low humidity glass-encapsulation interface becomes a quick leakage current path, this implies that irrespective of humidity levels. To control leakage current to the ground (frame) proper choice of glass and encapsulation used in PV module fabrication.

3.3.3.2.1 PID prevention measures at module level

Since the detection of PID in commercial PV solar power plants in 2009, the necessary effort has been made on improving the manufacturing processes with an aim of delivering PID free PV module to the market. This effort aims at increasing PV module resistance to leakage currents and has been achieved through proper choice of crystal orientation, use of good quality ARC, introduction of silicon oxide layer between the cell and ARC, use of chemically tempered glass or Titanium coated glass from the inside and use of high resistive encapsulation [25] [32].

Silicate soda-lime glass is the most frequently used for module cover glass because it is low cost and has good optical and other physical properties [32]. However, this glass type provides a conducive environment for PID to take place in p-type modules because it contains alkali ions such as Na^+ and K^+ with sizable bulk resistivity. In an event of a high voltage between the frame and the cells a leakage current will be forced to flow due to Na^+ migration resulting in PID shunting. To prevent PID at module level, soda lime glass should be replaced with a glass with better physical properties such as aluminosilicate glass which reported 5% power drop in 100 hours as opposed to 80% for soda-lime silicate glass in 50 hours [17]. This is because aluminosilcate has only 3% of Na_2O as compared to silicate of 14% of Na_2O [33]. Other prospective soda lime silicate alternatives include borosilicate and quartz glass [34]. The problem of these alternatives to soda lime silicate is they are more expensive hence less sought for by manufacturers.

Improvement on soda lime silicate glass have been proposed such as coating it with a layer of thin SiO_2 film to curtail ion migration from the glass, however this resulted in slight improvement in resistance to PID [35]. Hara *et al*. deposited a thin layer of Titanium dioxide (TiO_2) from inside the glass of up to 200 nm [36]. TiO_2 coating resulted in an excellent inhibition of ion migration [8]. Pop *et al.* equally conducted a similar experiment by coating with different materials. They both got impressive outcome of increased PID resistance [37]. While this modification of a thin layer was successful in preventing PID, the optical properties of the glass were compromised substantially since the additional layer resulted in reflecting, scattering and absorption of the incident light leading to reduced module efficiency. Another approach is to disrupt the glass surface conductivity under damp heat with glass strips and chemical agents [38] [39].

The most important property to prevent PID in an encapsulation is high bulk resistivity. A high bulk resistivity prevents PID by preventing leakage current that causes voltage built up between the cells and the frame [40]. Some PID resistant encapsulation such as silicone and ionomer while they have high bulk resistance, they may not be reliable in PV industry because they can only withstand PID to a certain extend beyond which they severely degrade under high voltage [19].

EVA is the most used encapsulation material in crystalline modules even though it is not PID resistant [41]. EVA from different manufacturers may have variable properties, some may have higher resistivity than others [42]. EVA may be susceptible to PID but has proved to be reliable, affordable, and available and can allow for improvement of on its resistivity without affecting its optical and physical properties hence preferred to any other form of encapsulation[28] [58] [59].

3.4.2.3 Cell Level

At cell level, a leakage current is caused by high electric potential in combination with high humidity and temperature. Na^+ drift through the glass to the encapsulation and accumulate on the cell surface. The accumulated charges are responsible for failure of surface passivation causing major degradation. PID degradation at cell level depends on resistivity of the encapsulation and cell properties such as emitter-base resistivity and ARC [45]. In studies by other researchers' mechanisms leading to current shunting in a cell were investigated where Na^+ was observed at the emitter in a PID affected cell sample as observed in secondary ion mass spectroscopy (SIMS) shown in Figure 3.6 [17] [46]. Figure 3.7 shows an EL image of a cell at advanced recovery from PID, most sections are Na^+ free while on the edge near the frame possible Na^+ sites are still visible.

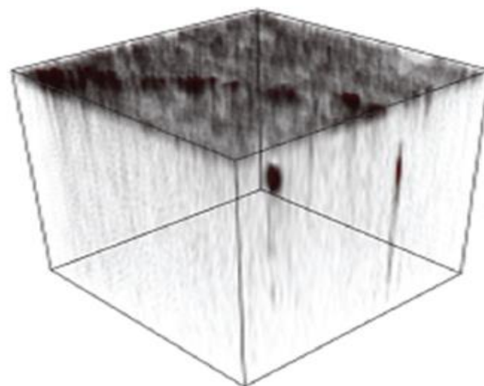


Figure 3. 6: *Time of Flight -SIMS 3-D representation showing sodium ions distribution on 200 µm by 200 µm by 2.2 µm Volume after PID stress* [46].

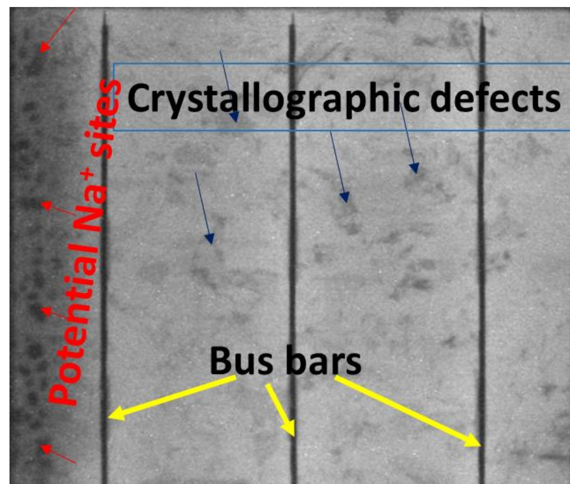


Figure 3. 7: *EL image of a cell in a module recovering from PID. The cell measures 156 mm by 156 mm.*

Naumann *et al* [47], observed that PID shunted areas were not interrupted by busbars and fingers. PID shunting was then concluded not to be caused by metal ions from the contact grid but Na^+ from the glass and ARC contaminants [48]. Because PID causes failures at the PN junction, it is called junction PID shunting [17]. Figure 3.8 shows Dark Lock-In thermography (DLIT) which confirms that PID shunting occurs between the fingers and hence does not affect metallization as reported by Schutze *et al.*, 2011 [49].

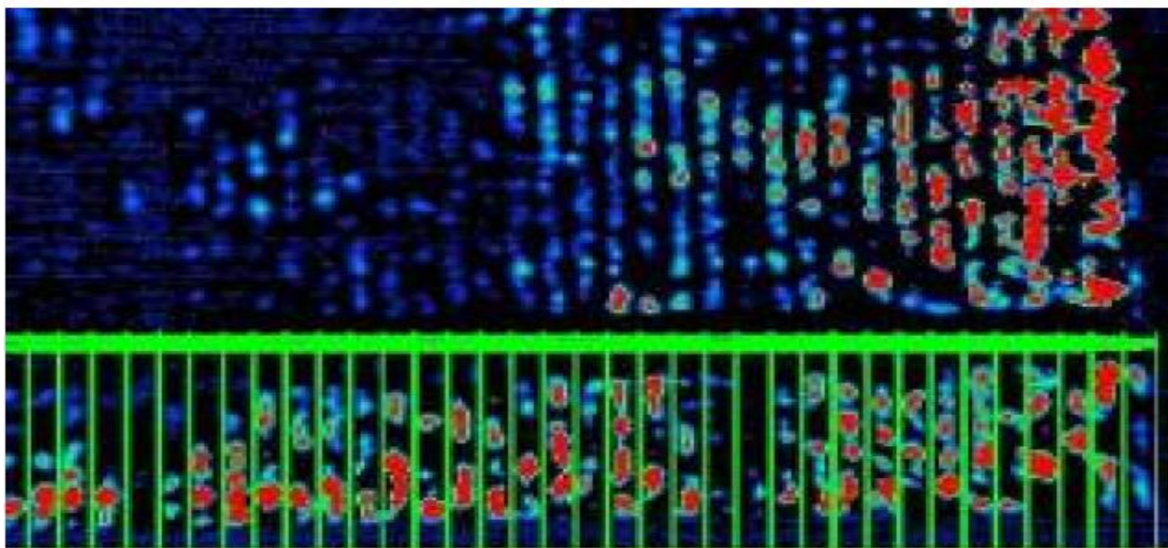


Figure 3. 8*: Dark Lock-In thermography (DLIT) for a PID shunted cell, the red spots are shunts while the green line area the metallization [49]*

3.4.2.3.1 PID prevention at cell level

Increasing base resistivity of p-type cells may lower chances of PID occurring on a cell [50]. Doping the lower base of the cell may lead to a wider depletion region at the PN junction as long as the emitter doping remains constant. Increasing the emitter resistance may lead to minimal PID susceptibility, the emitter resistivity can be increased during the cell manufacturing process [17]. Wafers are normally textured and cleaned before the emitter diffusion process is undertaken. If the cleaning is not done thoroughly, residues on the front surface may affect cell emitter diffusion by increasing sheet resistance, hence increasing PID susceptibility. Silicon Nitride ARC commonly used in p-type modules, has a significant influence on cell PID susceptibility [25]. Increasing the refractive index of the ARC greatly improves cells resistance against PID shunting. This is achieved by increasing silicon nitride (Si/N) ratios during deposition process. Increasing the ratio of Si/N increases refractive index (RI), conductivity and decreases positive charge carriers into ARC leading to decreased susceptibility to PID shunting by neutralizing Na^+. The decreased number of Na^+ drifting towards the ARC is due to diminished electric field [25].

A higher RI of about 2.2 may be effective in completely preventing PID shunting [26]. However, RI of beyond 2.2 may be counterproductive since it results in a thick ARC which absorbs most of the incident photon instead of transmitting to the cell for e-h generation[35],[54]. PID on a cell can further be minimized by introducing a layer of a thin film of between 7-10 nm between the ARC and the emitter [17]. The SiO_2 layer does not prevent PID but slows down migration of ions towards the ARC. If a high voltage is sustained over an extended period of time PID can be observed on the output [17], [52]. The thin film can be made of silicon oxide layers (SiO_2), this offers resistance to sodium ions migration to the cell diminishing chances of PID occurrence [15] [32].

3.4.3 PID module regeneration modelling

PID shunts are localised short circuit current sites within the cell crystallography caused by accumulation of Na^+ within the PN junction. PID shunting caused by polarization degrades solar cells power performance and affects the overall module efficiency and fill factors (FF) [53]. Shunting has the implication of promoting

recombination sites within the faults created in the PN junction [46]. PN junctions naturally have unoccupied faults, when PID occurs due to polarization sodium ions from the glass are forced to drift to the cell surface and eventually diffuse into the PN junctions [16][54]. The Na^+ will find occupancy within the multiple faults. When modules are not stressed under high voltage, Na^+ would normally diffuse back to the glass, the process is slow and may take several months or years before all sodium ions are evacuated from the places of temporal occupancy [17][54].

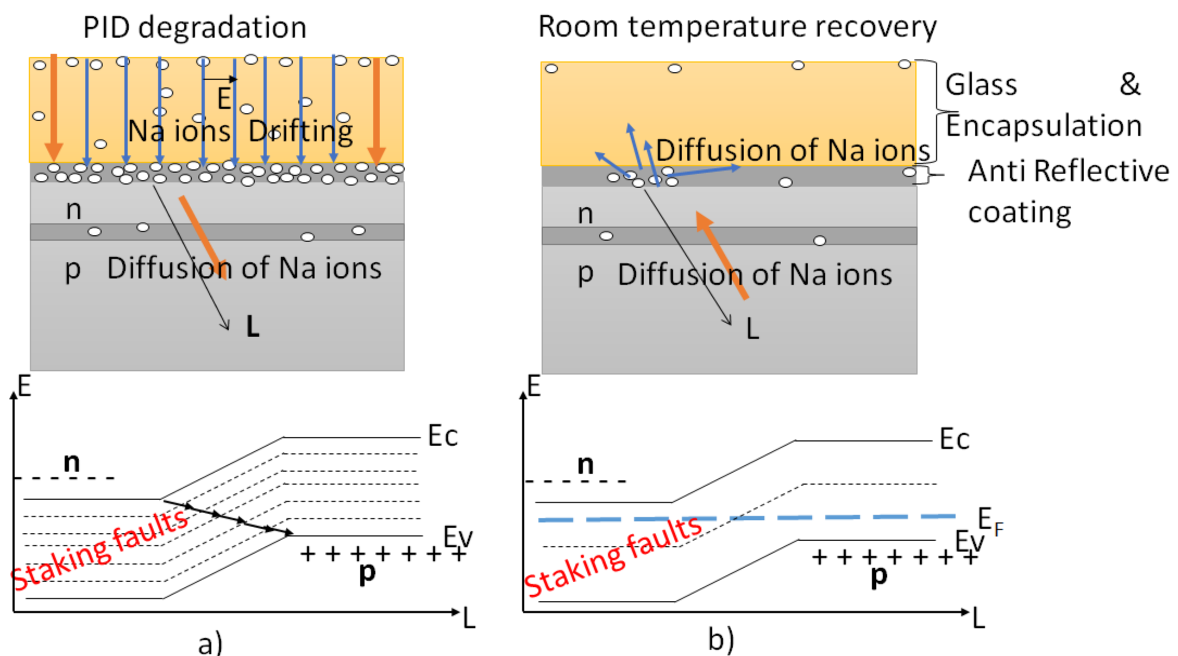


Figure 3. 9: *Modelling of Na^+ migration: a) modelling migration when the module is under PID stress. b) Modelling regeneration after PID stress* [54].

Figure 3.9a) shows a model of Na^+ migration under a strong electric field. The ions drift to the surface of the cell and diffuse into the PN junction. The amount of Na^+ diffusing into the PN junction will depend on the concentration size of Na^+ accumulated on the cell surface. Figure 3.9b) models the diffusion of sodium ions from the surface of the cells back to glass through the encapsulation under no voltage bias, as the concentration drops it becomes difficulty to evacuate some of the Na^+ which may be buried inside the stacking faults within the PN junction. The un-evacuated Na^+ creates minor short circuits or recombination sites which may be responsible for non-attainment of 100% power recovery Figure 3.9b) [54].

PID due to shunting is the most common degradation mechanism observed. In theory, increased recombination in the depletion region are caused by Na^+ decorated stacking faults across the depletion region [40][55]. PID has been shown to strongly influence

recombination leading to increased saturation current, the refractive index of silicon nitride increases as PID manifest itself and the saturation voltages drops drastically, which may result to up to 80% power drop from the module initial power measurements [10].

3.4.4 Test methods for the detection of PID

The IEC–TS-62804-1:2015 standard was published in 2015 as a set procedure for evaluating and testing the durability of crystalline silicon modules to the PID. The standard describes the two methods of inducing the voltage stress and tests the ability of the module to withstand PID in a relatively short time. The actual stresses experienced in the field depend on the operation in different climates and systems. The presence of PID is confirmed by preforming tests before and after PID induction and monitoring the degradation.

Module characterisation tools such visual inspection, power measurement (light-IV), dark-IV measurement, IR thermography and EL imaging are necessary in detecting the presence and degree of PID failure on PV module device. The choice of a diagnostic tool for any degradation detection may depend on the cost of the equipment, how accurately the failure can be detected, duration, additional processing and possibility of automation in order to handle large volumes in a short period of time.

3.4.4.1 PID Stress Induction

Climate chamber condition (Method 1) - This method is an adaption of Method A from the IEC 62804-1:2015 standard, the module is stressed at system voltage for cycles of 96 hours at a temperature of 35 °C ± 1 °C, humidity 75% ± 5% RH. These conditions are lower than the standard requirements of 60 °C ± 2 °C and humidity 85% ± 3% RH, however, they are closer to the real operation conditions. The module was connected as shown in Figure 3.10, but detailed setups are described in Chapter 4. The possible leakage current paths in a module under PID stress are shown in Figure 3.11), 1) through the surface of the glass to the frame, 2) through the glass substrate towards the frame, 3) along the interface between the glass and the encapsulation, 4) through the encapsulation substrate, 5) along the encapsulation and back sheet interface, 6) through the back sheet substrate and 7) through the sheet surface [17]. From Figure 3.11 the simulated electric field in each of the setup is

indicated with the red lines. In Figure 3.11a) the field is concentrated on cells near the frame since the frame is the anode connection to the high voltage. Greater leakage current is expected to flow through the surface and bulk of the cells because of humidity condensation and a strong electric field near the frame. This explains why PID induction using this method 1 often affects cells along the frame more strongly.

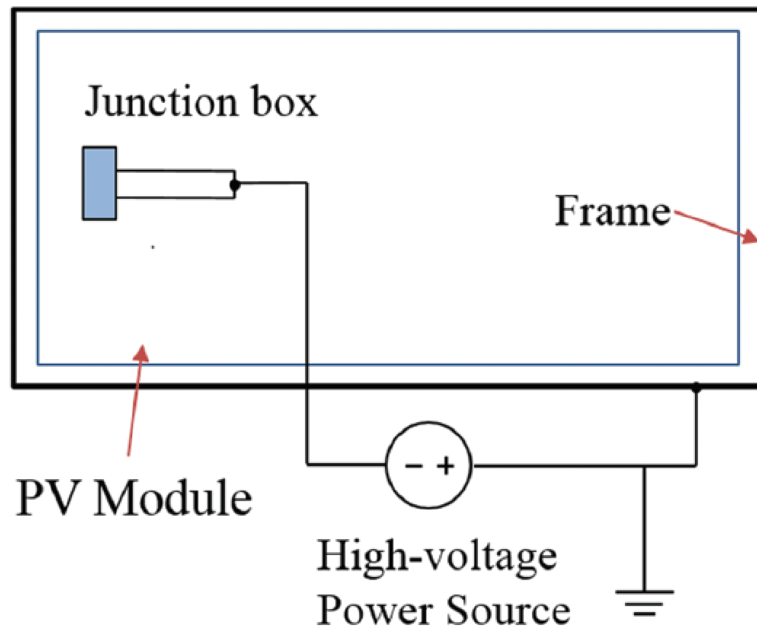


Figure 3.10: *schematic diagram of PID set up inside the climatic chamber, the two module terminals are short circuited and connected to the negative of the Hipot tester while the frame is connected to the positive of the Hipot tester.*

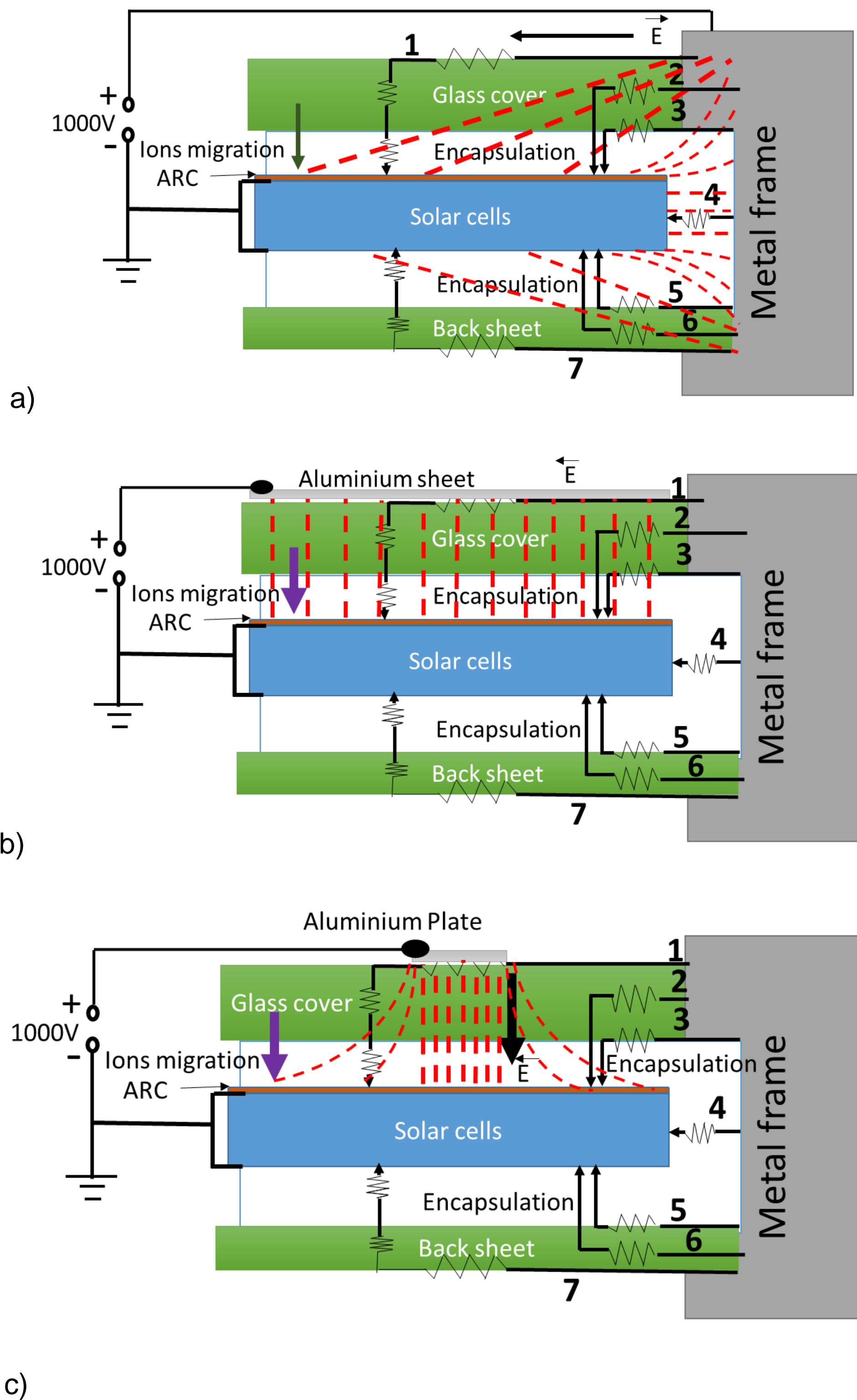


***Figure 3. 11**: Modelled current leakage paths in a module under High electric potential and their associated electric field (red line) a) Method 1 climate chamber conditions. b) Method 2 aluminium plate (conducting layer) resting on the surface of the module without touching the aluminium frame. c) Method 3 a case of localised PID induction using an aluminium pate size of a single cell as an anode.*

Conductive layer on the front surface (Method 2) – In the IEC 62804-1:2015 standard, the module is wrapped with an aluminium foil and stressed at the system voltage for 168 hours. For the purposes of this work, the aluminium plate was used instead of a foil. The plate served as an anode and to make the glass surface conductive. In Figure 3.11b) the electric field is spread uniformly because the aluminium plate positively biased in relation to the cells. Because of the uniformity of the electric field PID affected cells observed in EL images are evenly distributed.

Localised PID induction on a cell in a module (Method 3) - This method had all condition similar to method 2 except that the plate used could only cover one cell. The simulated electric field and current leakage paths in Figure 3.11c) shows electric fields that are concentrated on a single terminal and the field spread outward on the cells. This field distribution justifies the PID shunting that befalls the cell of interest and the neighbouring cells. The conductive nature of the cover glass is brought in test when cells away from the cell of interest are PID shunted.

3.4.4.2 Module Characterisation Tools effective for PID detection

PID degradation mechanisms and the commonly used detection techniques that are used as module characterisation tools may include the following

- Optical losses –visual inspection and power measurement,
- Degradation of electrical circuit – IR thermography, EL imaging and power measurements,
- Mechanical damage – El imaging and PID – EL imaging, IR thermography and Power measurements.

Power measurements are powerful tool in detection of module degradation. In this work Power measurement, dark IV measurements, IR thermography and EL imaging are employed in detection of PID degraded modules [56].

Visual inspection- This involves visual identification of defects such as ; optical impediments, burn marks and physical damage on the frame and front glasses and corrosion on some sections of the cell/module [57]. Visual inspection may not be able to detect PID shunted cells unless the PID shunting resulted in a hotspot, with subsequent thermal damage such as burn marks and yellowing of the encapsulation.

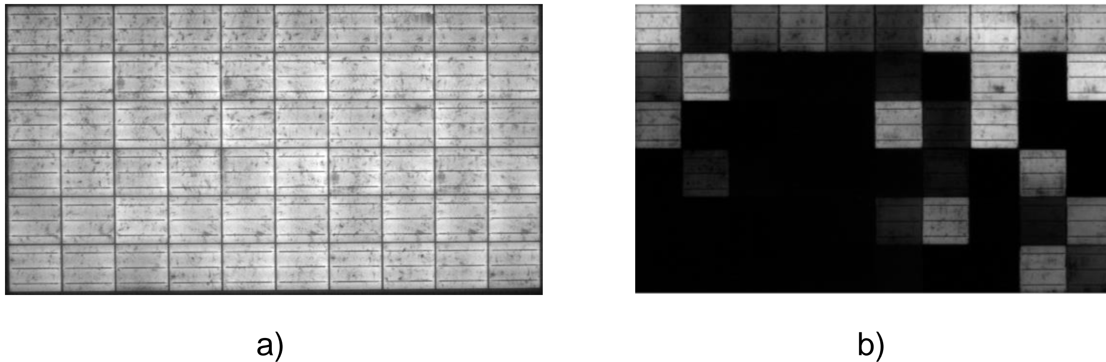
Power measurements (IV measurements) – this technique may be used to identify optical as well as electrical degradation. This can be done in the field or at Standard Test Condition (STC i.e Temperature 25° and irradiance of 1000 W/m^2 and air mass AM 1.5). L-IV measurements collected in the field must be corrected to STC so that the module parameters extracted may be comparable to initial parameters on the specification sheet. In this work Particle Swarm Optimization (PSO) [58] using the single diode model was used to extract parameters such as I_{sc}, V_{oc}, V_{mp}, I_{mp}, FF, R_s and R_{sh}. By comparing initial PV module parameters and after degradation the parameters may vary in a unique way for example for PID, shunt resistance has been proved to drop drastically. PID shunting is characterised by decrease in R_{sh} due to increased shunting, at low irradiance the shunting become more predominant resulting in decreased photocurrent due to increased R_s. A higher shunting level significantly decreases P_{mpp} of a module.

Thermal Infrared (TIR) imaging- this method is capable of detecting electrical failures, especially if the mode of degradation may result in increased R_s, cell shunting and disconnection. Temperature variation distribution can be imaged by IR detectors. Currently TIR imaging is being done on large scale by fitting a drone with IR camera and taking continuous images for analysis. The method is non-destructive and does not interfere with plant operations [53] [59]. At outdoor PID shunted cells are at higher temperatures than the rest of the cells while at indoor the PID shunted cells are at lower temperature than the rest.

Electroluminescence imaging- EL imaging is the most accurate tool that is used to identify several module failures such as: micro-cracks on cells, fractures, disconnected areas of a cell, broken ribbons, and fingers, PID shunted cells, cells with increased R_s and other manufacturing defects like impurities or precipitates [60] [61]. For a comprehensive diagnosis of a module, EL imaging may be correlated with diagnostic tools such as visual inspection and power measurement. For the purposes of this work EL imaging taken at current corresponding to 10% of I_{sc} is vital in detection PID shunted cells.

Before PID stress, all cells in a PV module are supposed to be in good condition. Such cells will appear with near uniform electroluminescence, after PID stress variation level of brightness is observed on the module. An example of EL imaging pre- and post PID

stressing is shown in Figure 3.12 for one of the modules used in this study. The module (Module K) was induced with PID using method 2 described in section 4.6. The figure shows the EL image of Module K before PID stress after 20 hours of PID stress at +1000 V. The module lost 36.4% of its initial power output.



a) b)

Figure 3. 12: *Module K, EL images taken at of I_{sc} (7.8 A), a) Initial EL image, b) EL image after 20 hours of PID stress. The module lost 36.4% of its initial maximum power.*

3.5 Summary and conclusions

The possible causes of PID has been a subject of intense investigation, many researchers have concluded that PID in crystalline based modules was caused by surface polarization, others attributed the defect to Na^+ decorated stacking faults and finally another group suggested it could be due to acetic acid corrosion. Years later what followed was to try to reverse the effects of PID. This has been done by reverse biasing the affected module in an environmental chamber at elevated temperature. In some cases, PID affected cells have been left to recover naturally. Reverse biasing takes a short period of time to recover a PID affected module, while natural recovery may take many days/months or even years. Its worthy noting that PID affected cells due to polarization may recover but PID due to corrosion is irreversible. PID still remains a subject of intense investigation in order to understand and manage the power output drop associated with PID. This work advances the procedures that can be used to detect PID at infancy and proposes module regeneration procedures and their associated regression.

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CHAPTER 4

4. EXPERIMENTAL MATERIALS AND DETAILS

4.1 Introduction

This chapter describes the PV modules used in this study and the experimental procedures for PID detection techniques such as EL imaging, dark current voltage measurements (D-IV), light current voltage measurements (L-IV) and infrared (IR) thermography are described. The procedure for PID induction or PID stress tests are described. The Image processing and EL Image analysis histogram development is detailed.

The experiments were done following IEC standards on PID, Power measurements, EL imaging and infrared thermography. However, in the cases where standard equipment is not available a workable solution to obtained desired results was considered and pursued like in the case of the environmental chamber.

4.2 Modules used in this study

The modules used in this study are listed in the table 4.1. These modules were commercially available mono-crystalline and multi-crystalline (Poly).

Table 4. 1: *List of module specification used in this study.*

Module	Module type	Number of cells	Module Dimensions (mm)	Cell sizes (mm)	Approximate age (years)
A	Mono-120	6 × 12	1200×550×35	57×125	7
B	Poly-295	6 × 12	1956×992×50	156×156	3
C	Poly -240	6 × 10	1675×1001×31	156×156	12
D	Poly -260	6 × 10	1640×990×35	156×156	4
E	Poly -240	6 × 10	1675×1001×31	156×156	12
F	Poly -240	6 × 10	1675×1001×31	156×156	12
G	Poly- 240	6 × 10	1640×990×35	156×156	12
H	Poly -250	6 × 10	1675×1001×31	156×156	5
I	Poly -240	6 × 10	1675×1001×31	156×156	12
J	Poly -240	6 × 10	1675×1001×31	156×156	12
K	Poly -240	6 × 10	1675×1001×31	156×156	12
L	Poly -250	6 × 10	1675×1001×31	156×156	5

Older modules have higher susceptibility to PID than newer modules, this is because of advancement in manufacturing technology especially on the encapsulation. The current generation of modules are using high resistive EVA encapsulant, which is better than the previous versions.

4.3 PV module characterization techniques

This section explores all possible PV module characterization; Light-IV Measurements (L-IV), Dark-IV Measurements (D-IV), IR thermography and EL imaging. Each of the characterization has its own purpose as described in the sections below

4.3.1 Light Current-Voltage (L-IV) measurements

L-IV measurements are crucial in determining the power performance of a PV module and determining important parameters such as maximum power point (P_{mpp}), Open-circuit Voltage (V_{oc}), Short-circuit current (I_{sc}) and Fill Factor (FF). The power measurements were taken using a solar simulator which corrected all power measurements to STC (temperature 25°C, irradiance of 1000W/m^{2} and spectrum **(AM1.5).** In this study an OptoSolar solar simulator AAA (spectral match (0.75-1.25),

irradiance spatial non-uniformity 2% and temperature stability 2%) was used for L-IV measurements. Shunt resistance (R_{sh}) was obtained from the inverse of a tangent on L-IV curve at low voltages and series resistance (R_s) was obtained from the inverse gradient of the tangent taken on L-IV near V_{oc}. PID drastically decreases R_{sh} by increasing surface recombination and increases leakage current paths due to increased R_s.

4.3.2 Dark Current-Voltage (D-IV) measurements

The D-IV measurement procedure involves placing the module in the dark room to eliminate the possibility of photo generated current. An Agilent E3646A dual output power supply injects current through the module in forward bias. Current (A) and voltage (V) are measured simultaneously using two Agilent 34401A digital multi-meters. The two digital multi-meters are connected such that one is across a shunt resistor (0.05Ω) to measure current and the other across the module to measure voltage [1] the experimental, set up is as shown in Figure 4.1. The resulting direction of current flow is opposite to that when the cell is exposed to light meaning the current paths are different. The D-IV characteristic of the modules are measured in the dark at room temperature of 25°C. The DC power supply has an output voltage range of 0-60 V and output current range of 0-10 A.

In D-IV measurements the DC power supply was controlled by a LabVIEW program to drive the desired voltage through the module and measure the dark current values. The forward bias current was calculated from voltage generated across the shunt resistor.

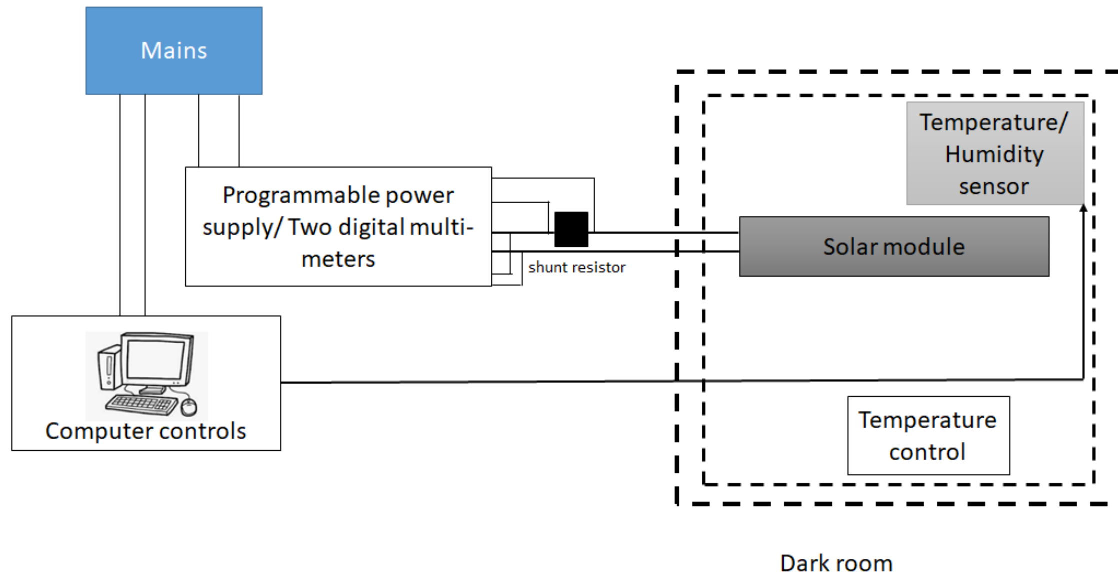


Figure 4. 1: *Schematic illustration of the Dark IV measurement set up*

D-IV semilog curves are used to estimate series and shunt resistance. In D-IV measurements carriers are injected, rather than being photo-generated as is the case for illuminated measurements. The module behaves like a diode, as such information such as ideality factor (*n*), saturation current (I_o), shunt resistance (R_{sh}) and series resistance (R_s) can be accurately obtained from D-IV curves. A PV module may be modelled using a single diode model according to equation 4.1 [2].

$$I = I_O[\exp(\frac{q}{nkT}(V - IR_s)) - 1] + \frac{(V-IRs)}{Rsh} \qquad 4.1$$

Figure 4.2 shows a typical D-IV characteristic curve with the effect of parasitic resistances on the characteristics in different voltage regions indicated. In absence of L-IV measurements D-IV on semilog scale is used to determine indicative series resistance (R_s), shunt resistance (R_{sh}) and ideality (*n*) factors. The D-IV parameters are obtained by calculating the gradients of the tangents as shown in Figure 4.2 [3] [4]. The current is measured as voltage is increased by 0.1 V up until 50.0 V is attained. The data is stored in text file for further analysis and comparisons of dark I-V measurements. The vertical scale of Figure 4.2 is in log scale.

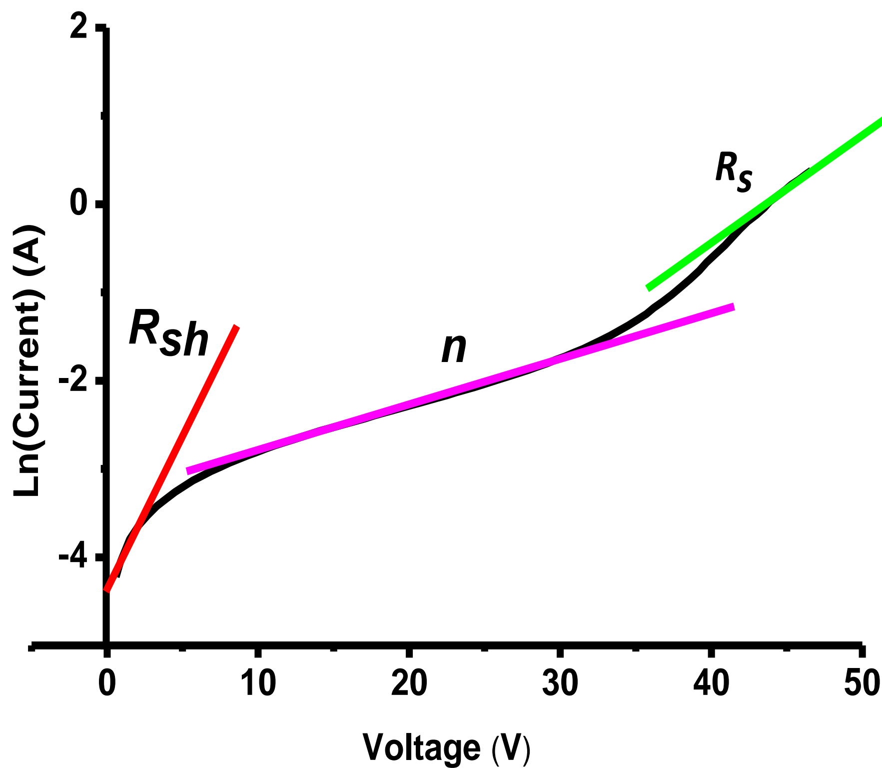


Figure 4. 2 *: A semi log dark I-V graph for the PV module*

4.3.3 Electroluminescence (EL) measurements

The EL setups used in the study comprises of a NIR camera (CCD sensor or CMOS), to capture the EL image. A power supply is required to inject the required current in forward bias. The module is placed on a suitable mounting structure, the camera is placed normal to the surface of the module and adjusted to optimise EL image detection. The EL images are taken in a dark room to avoid stray light from interfering with EL detection. The EL intensity has a slight temperature dependence, to ensure images are comparable the temperature of the room is controlled and in the range of 20 °C to 25 °C the schematic of EL Laboratory set up is as shown in Figure 4.3.

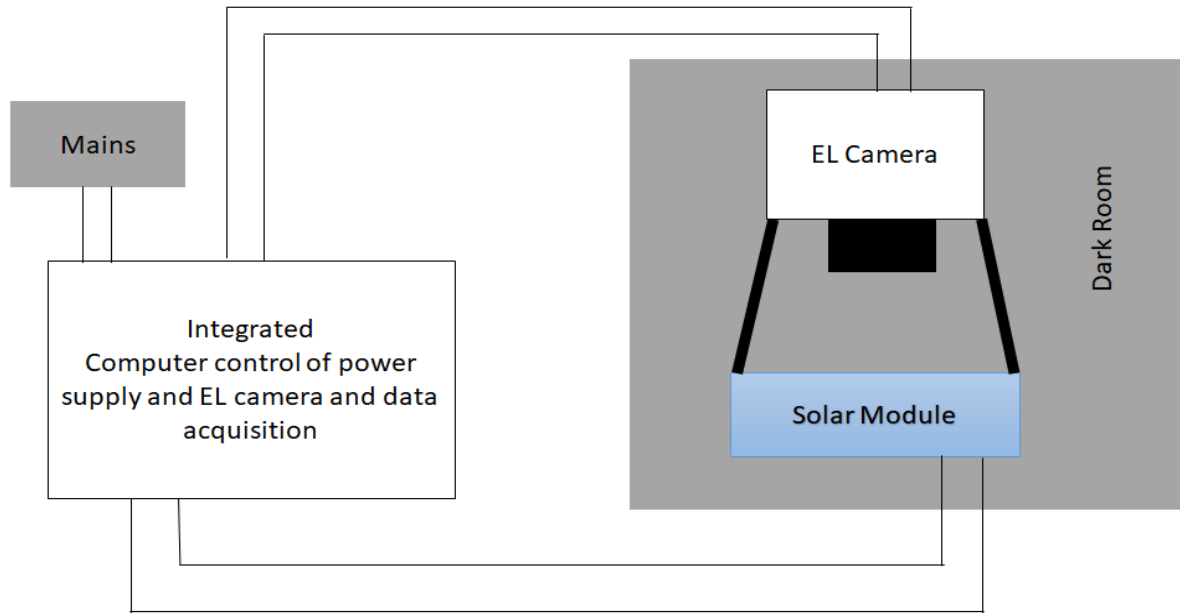


Figure 4. 3*: Schematic illustration of EL measurement set up. Comprising of integrated computer/power supply controls, EL camera, PV module and connecting cables.*

The EL camera should be sensitive to emission spectrum for crystalline silicon which has a peak at 1150 nm. The CCD and CMOS camera response curves partially overlap with the silicon peak as shown in Figure 4.4. The choice of these two cameras was motivated by low cost and considerably high resolution. CCD and CMOS devices have a relatively low sensitively to the EL spectrum so a longer integration time is required. The choice of integration time for EL imaging should be enough to detect an optimised EL image with a good quality contrast and avoid saturation. To ensure comparable analysis of EL images taken before and after PID stress the EL imaging condition were kept constant for subsequent images. The MBJ camera CMOS system is capable of taking EL images at I_{sc} and 10% of I_{sc} in a quick succession and uses multiple images/cameras to taking EL images in small portions of the module which are then stitched together to give a high resolution image of the module. The CCD GreatEyes used in some of the modules can take a single whole module at once resulting in a lower resolution image.

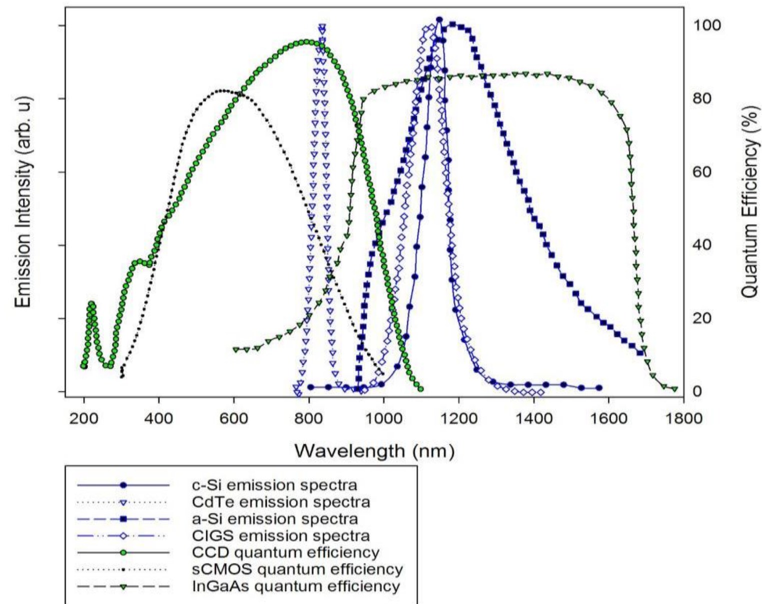
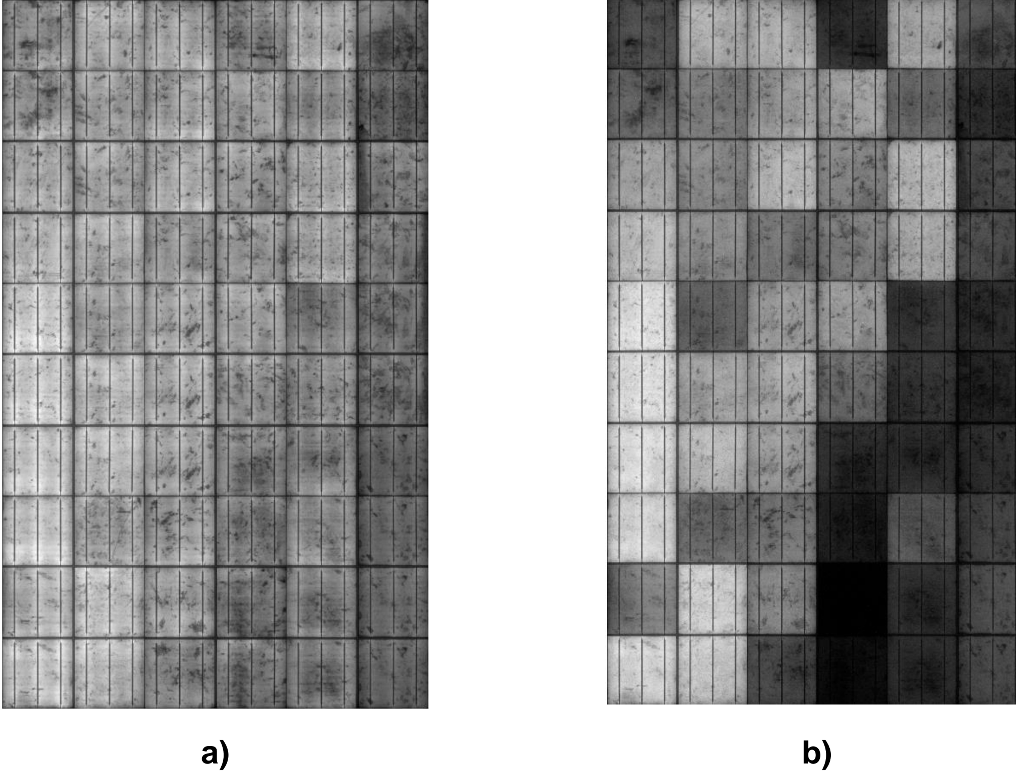


Figure 4. 4: *Emission spectra from a range of solar cell technologies and the quantum efficiency of silicon CCD, CMOS and InGaAs CMOS cameras* [5].

EL images mean nothing unless further analysis are made on them before and after PID stress. The analysis helps to quantify the severity of the degradation induced by PID. The following section details the EL analysis process.

4.3.3.1 EL image distribution analysis

In this study, EL imaging as degradation detection tool has been used to successfully detect cells in a module affected by PID at different stages. EL imaging at a current corresponding to 10% of I_{sc} is an important tool, because shunting of cells lowers R_{sh} and increases considerably R_s, hence, the injected minority carriers will follow a path of least series resistance and eschew cells/sections that are at slightly higher series resistance, such cells will appear with reduced EL signal (dark). When the current is increased to I_{sc} more minority charge carries will find itself into such cells leading to a high EL signal [6]. This implies that EL images taken at I_{sc} will not detect PID except for cells at advanced stage of PID. This is illustrated in Figure 4.5. The EL setup used in this study has the capability of taking EL image at current corresponding to I_{sc} and at 10% of I_{sc} in a quick succession.



a) b)

Figure 4. 5: *EL images of module E: a) EL image taken at current corresponding to I_{sc} (Module E). b) EL image taken at current corresponding to 10% of I_{sc}*

EL images recorded before and after PID stress may be compared to identify the onset of PID and an analysis of image normalised pixel intensity distribution histograms may be used to determine shunting levels. The intensity distribution of shunted regions (inactive) and un-shunted regions (active) are such that two peaks are observed one within the inactive region and the other one on the active regions. The analysis was done using normalised image histogram $p_{EL}(a)$ calculated using equation 4.1.

$$p_{EL}(i) = \frac{n_i}{n}, 0 \leq i < L \tag{4.1}$$

Where i is the grey level pixel, $\boldsymbol{n_i}$ is the number of grey level $\boldsymbol{i}$ occurrences, $\boldsymbol{n}$ is the total number of the pixel in the image L is the total grey levels which is 256 or 1. The calculation of p_{EL} (i) is done on the module before and after PID stress. The histogram is plotted against normalised EL intensities, $0 \leq \boldsymbol{i} < 1$. A normalised threshold of inactive module regions is obtained from calculating standard deviation STD (σ) of the p_{EL} ($\boldsymbol{i}$) values of the EL image and getting its equivalence on normalised pixel intensity. μ is the calculated mean normalised p_{EL} for specified region pixel intensities [7][8].

$$STD\ (\sigma 1) = \sqrt{\sum_{i=0}^{L-1} (P_{EL}(i) - \mu_{Total})^2} \tag{4.2}$$

$$STD\ (\sigma 2) = \sqrt{\sum_{i=0}^{0.34} \left(P_{EL}(i) - \mu_{Inactive\ region}\right)^2} \tag{4.3}$$

$$STD\ (\sigma 3) = \sqrt{\sum_{i=0.34}^{L-1} \left(P_{EL}(i) - \mu_{active\ region}\right)^2} \tag{4.4}$$

The $STD\ (\sigma 1)$ will vary from before PID stress and after PID stress. $STD\ (\sigma 2)$ and $STD\ (\sigma 3)$ will differ in distribution. The inactive area on EL before PID is only limited to dark spots, inter-cell spacing and bus bars. After PID stress a lower normalised peak is expected because of additional shunting occasioned by PID this will be in addition to dark spots, inter-cell spacing and bus bars.

To calculate the percentage of shunted module area (SMA) on the Low EL intensity below the threshold of 0.34 [7]. This can be calculated by first getting the percentage of the inactive area of the module occasioned by dark spots, inter-cell spacing and bus bars this will take as the baseline inactive module area percentage (BIMA). Inactive module area percentage for EL image after PID stress to be taken as IMA for EL image taken at 10% of I_{SC}.

$$BIMA[\%] = 100 \sum_{i=0}^{0.34} P_{EL}(i) \tag{4.5}$$

$$SMA[\%] = BIMA[\%] - IMA[\%] \tag{4.6}$$

4.3.4 Wet leakage current

PV modules are designed to be insulated for wet operating conditions and to minimise moisture ingress that can result in corrosion, ground faults or safety hazards. The purpose of the wet leakage current test is to evaluate the insulation of the module operating in wet operating conditions and to ensure that moisture from rain, fog, dew and molten snow does not infiltrate the active circuitry of the module [9]. The wet leakage test is included in the IEC/TS 62804-1:2015 PID stress test procedure to evaluate the module pre-and post PID stress.

In this study the wet leakage current test was undertaken by submerging the module with the sunny-side down in a shallow trough of water, the short-circuited module terminals are connected to the negative while the frame is connected to the positive. A trough of dimension 2200 mm x 1200 mm x 300 mm and 5.16 mm thick was filled

with water up to about 150 mm as illustrated in Figure 4.6. The is detailed in IEC 61215 paragraph 10.15.2 [10]. 1000 V was applied between the frame and shorted module terminal. The voltage safety analyser ramps 1000 V in 2 s, then the voltage is maintained for 120 s. The standard specifies that for most modules the insulation resistance of the module must be greater than 40 MΩ.m^{-2} to pass this test [10].

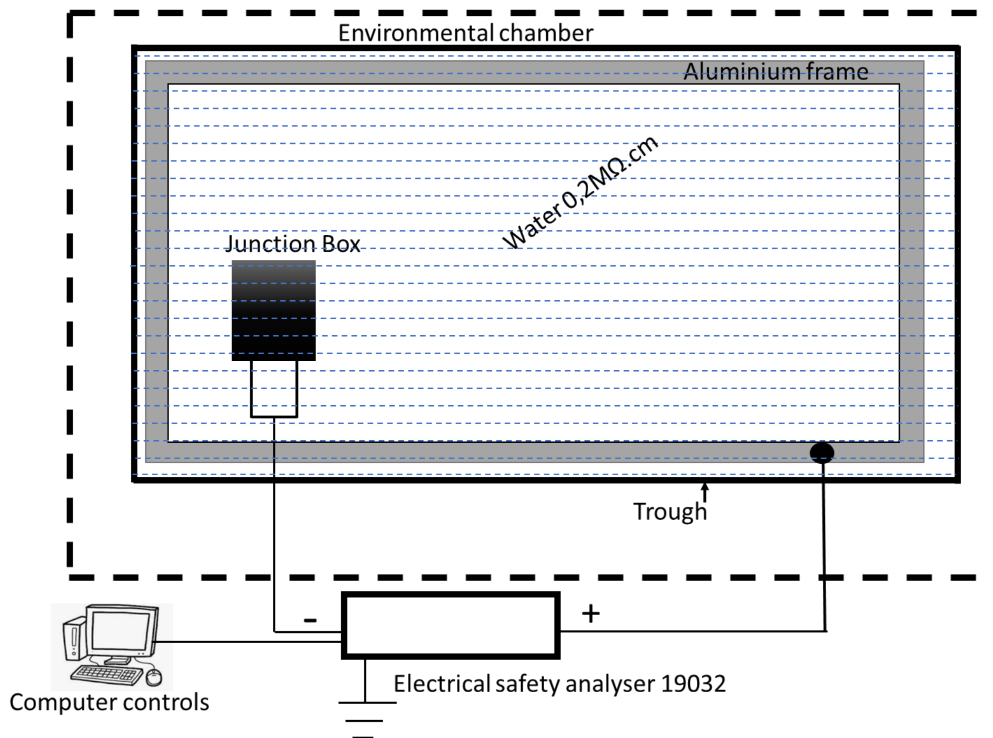


Figure 4. 6: *Wet leakage and Insulation test set up; a trough measuring 2200 mm x 1200 mm x 300 mm and 5.16 mm thick, electrical safety analyser 19032 and computer controls.*

4.3.5 Thermal Infrared (TIR) imaging

Infrared is an important detection tool which can be deployed on large scale PV plants to detect modules affected by PID especially at advanced stage. The cells in a module affected by PID are shunted hence generally operates at lower voltage in comparison to the rest of cells. The PID affected cells underperform hence can easily be set in reverse bias creating a hot spot. PID affected cells in a module on string, especially on the negative terminal of the string exhibiting checkerboard pattern may be as result of PID defect. In the laboratory the module is connected in forward bias, and cells that are PID affected are detected at slightly lower temperatures as compared to adjacent optimally operating cells. For outdoor TIR imaging, the shunted cells will exhibit higher temperatures compared to adjacent cells operating optimally [5].

4.3.6 Worst case cell determination/ cell mismatch investigation

PID affects cells in a module are uniquely shunted, hence there is a need to investigate the extent of PID shunting on individual cell in a module. In this study every cell in module E and L are individually shaded as illustrated in Figure 4.7 and power measurement are taken using a solar simulator, the L-IV measurements are recorded for further analysis. The shading pad is moved from one cell to the next after taking L-IV. The shading pad measures 157 mm by 157 by 3mm and is black to minimise the problem of tab reflection [11]. The cell shading and numbering of cells in this work is as shown in Figure 4.7

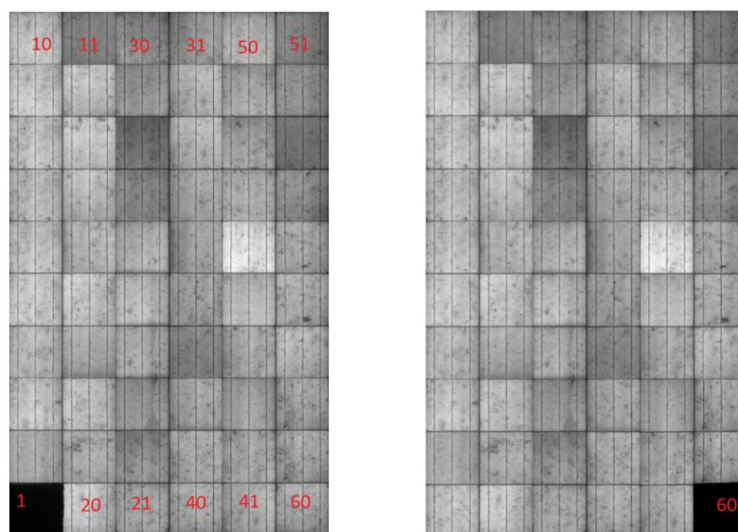


Figure 4. 7: *Show EL image set of module L, the black pad measuring exact size of a cell shades each cell individually from cell 1 up to cell number 60*

4.4 PID Induction and Recovery

PID shunting and forced reverse bias recovery are complementary process. The difference between the two is the polarity for p-type of modules used in this study for PID induction the frame is connected to the positive while for recovery the frame is connected to the negative of the voltage safety analyser. For natural recovery the module is left in open circuit for a very long period of time.

4.4.1 PID Induction Methods

In this study Potential induced degradation was induced in modules by simulating the conditions that result in PID in the field. These techniques are adapted from those

detailed in IEC/TS 62504-1 and literature [12] [13] [14] [15][16][17] and are detailed in the following section. The goal of the PID induction process was to stress the module in cycles of a certain number of hours until PID was detected. If a cycle was complete and no PID was detected (using EL Imaging) then the cycle was repeated.

Method 1: The module terminals were short circuited and biased to the negative terminal while the frame was connected to positive terminal of the voltage safety analyser, as shown in Figure 4.8. The conditions inside the environmental chamber were kept at 35 °C ± 1 °C and Relative humidity 75% RH ± 2% RH. The process was performed in cycles of 96 hours and up to 168 hours.

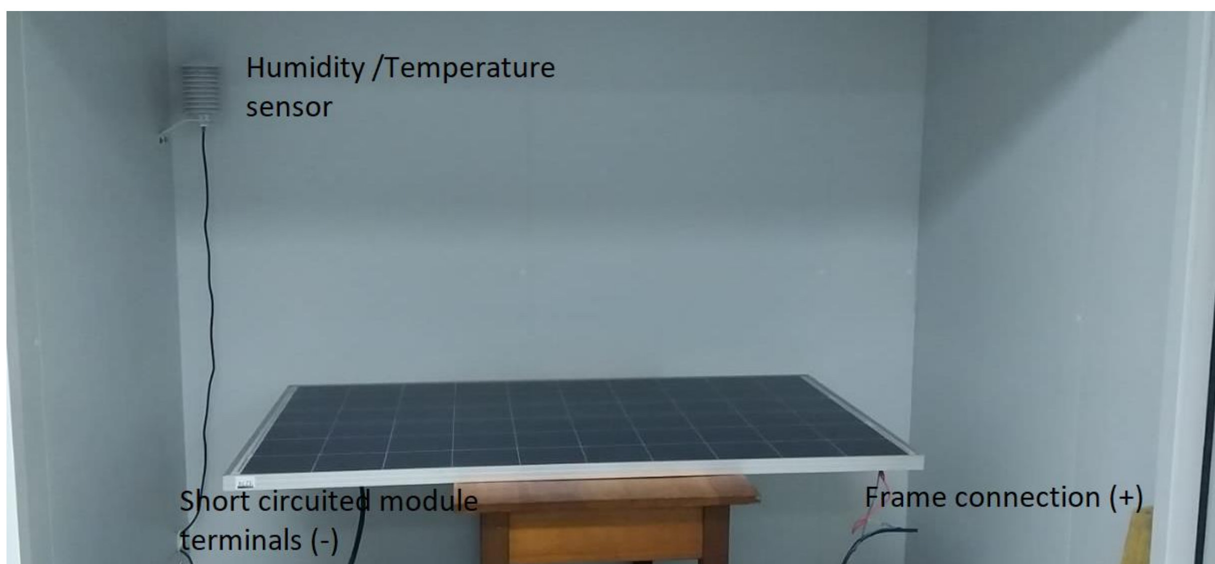


Figure 4. 8: *Potential Induced degradation setup, with a humidity/temperature sensor fixed at upper corner. The module is placed on a wooden bench to avoid charge discharge on the walls or floor of the environmental chamber.*

Method 2: PID stress on a module was carried out in a set up where an Aluminium plate measuring 1625 mm by 955 mm by 3 mm connected to the positive terminal was placed on the module to cover the cells without touching the module frame. The module's terminals were short circuited and connected to the negative terminal of the power supply. The environmental chamber condition was maintained at 35 °C ± 1°C and less than 40% RH throughout the experimentation period. The experimental set up is as shown in Figure 4.9.

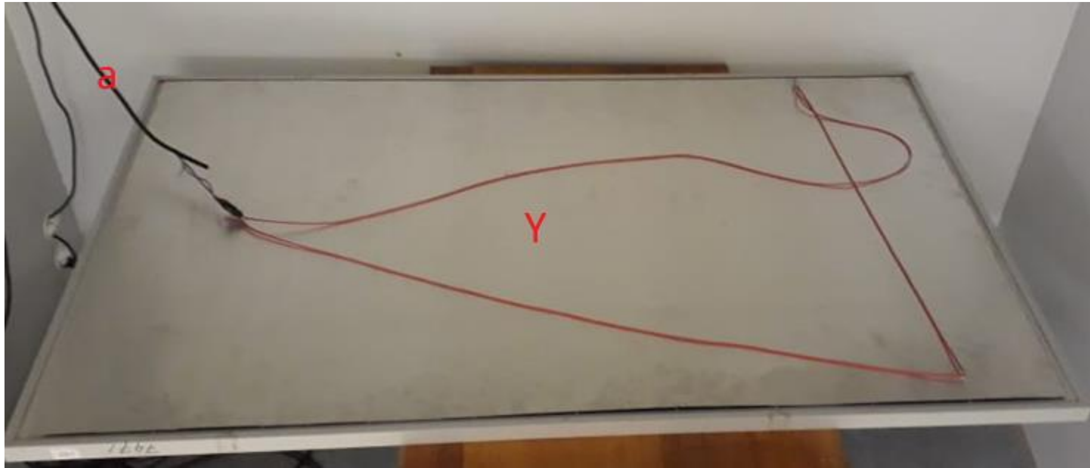


Figure 4. 9: *PID stress procedure method 2; Y is Aluminium plate measuring 1625 mm by 955 mm by 3 mm; a is the positive terminal biased to the power supply source.*

Method 3: PID procedure involved using an aluminium plate measuring 157 mm x 157 mm x 3 mm which was placed to completely cover a single cell biased at +1000 V for 96 hours, while the shorted terminals were connected to the negative of the power supply. The environmental chamber condition was maintained at 35 ^{o}C ± 1 ^{o}C and less than 40% RH throughout the experimentation period, as shown in Figure 4.10 below.

Figure 4. 10*: Module under test inside the environmental chamber, X is an aluminium plate measuring 157mm x 157mm x 3mm, placed on a cell surface and biased to positive terminal of the power supply.*

4.4.2 PID recovery Methods

It is possible that modules can recover from induced PID by reversing the degradation caused by PID shunting. This was done in two ways in this study; 1) forced reverse polarity of a module for 120 minutes or 2) by way of unbiased natural recovery in the

dark at open circuit over a period up to 12 months at room temperature. The recovery percentage is calculated based on the initial power measurements of the module. The recovery procedure was monitored by periodically measuring maximum power output and recording EL images at a current corresponding to 10% of I_{sc}.

4.4.3 The environmental chamber construction

The PID induction and recovery were carried out inside a custom-built environmental chamber constructed in the laboratory. The chamber measured 1735 mm wide, 2550 mm long and 2400 mm high. The walls are 62 mm thick and the door is rubber sealed to limit effects of outside temperatures. A heating element with air circulation capabilities was fixed on one side of the wall. The humidity was maintained stable during the experimentation period using a humidifying/dehumidifying unit. Temperature and humidity sensors monitor the conditions inside the environmental chamber. The module was placed on a wooden bench in order to avoid earthing since the wall and floor of the box were conductive. The chamber is shown in Figure 4.11.

The environmental chamber's maximum temperature is 35 °C ± 1 °C, so it was not possible to reach the high temperatures of (60 °C) required for PID Stress Testing Method 1 [18]. Maximum temperature was conducive for the humidity control unit which optimally works at temperatures less or equal to 35 °C ± 1 °C. The humidity unit maintained the humidity at 70% RH ± 2% RH for the duration of experiments

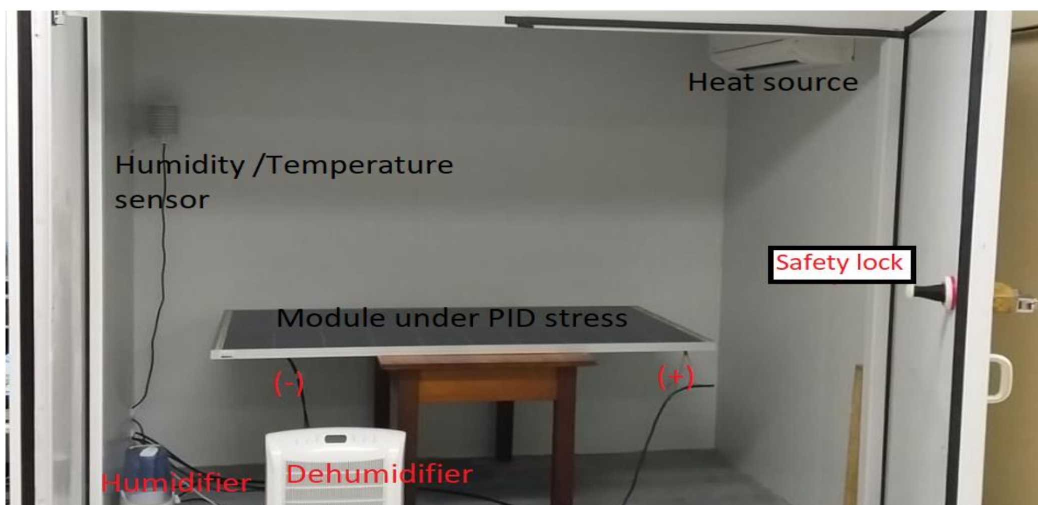


Figure 4. 11: *The environmental chamber consisting of Humidifier, Dehumidifier, heating source, and Humidity/Temperature sensor, the wall is 60mm thick*

4.5 Summary and conclusion

Two types of modules mono and multi-crystalline modules of different age's p-type module samples were used in this study. The module samples included old deployed modules and new unemployed modules. Each of the module samples was subjected to PID stress using the three methods outlined in section 4.4. PID detection was done by taking EL, L-IV and D-IV measurements before and after PID stress. Module recovery was also undertaken and monitored using way of forced reverse biasing and naturally at open circuit voltage for an extended period of time. Determination of worse performing cells after PID stress was undertaken using EL intensity and P_{mpp} at STC by shading one cell at a time. TIR imaging was done in two ways, at outdoor and at indoor. At outdoor the TIR imaging was done when the module was at open circuit Voltage, short circuit and when operating at P_{mpp}. The results obtained using this chapter's experimental procedures are discussed in chapter 5.

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CHAPTER 5

5. RESULTS AND DISCUSSION

5.1 Introduction

This chapter presents results on the PID stressing, detection and module power recovery after PID stress on various modules. The different PID stressing methods discussed in chapter 4 are used to induce PID under various conditions and in designated areas on PV modules. The characterization techniques such as power measurements, EL imaging and IR thermography are used for the analysis. PID shunting occurs due to migration of alkali ions, the majority being Na^+, to the surface of the cells due to high electric potential between the cells and the frame (earthing).

The method used to detect and quantify PID shunting can equally be used to quantify degradation due to transportation, storage, installation and field operation. Cells with dendrite cracks tend to appear darker on the EL image taken at 10%, as compared to EL image taken at I_{SC}. Cells with such behaviour may be under performing and may exhibit hot spots during operation. This behaviour may need further investigation.

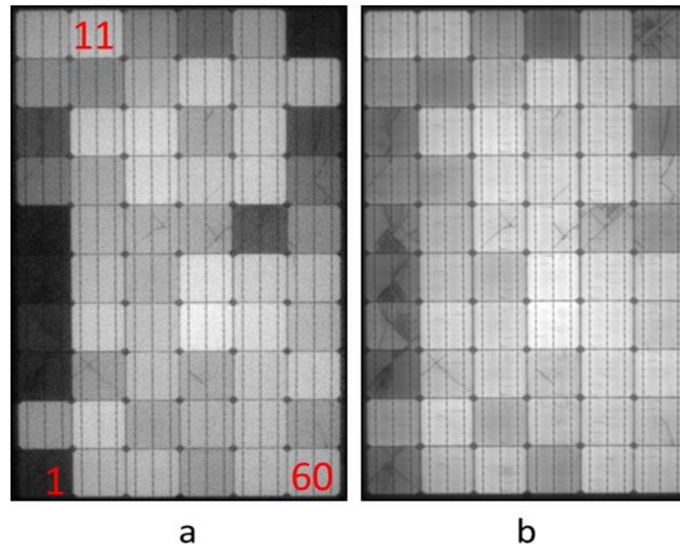


Figure 5. 1: *EL images taken on a module that has been in field operation for more than 8 years. The power drop during this period was only 3.02 %. a) EL image taken at 0.8 A, with cell number (1, 3, 4, 5, 6, 7, 8, 46, 51, 53, and 54) appearing darker than the rest of the cells. b) EL image taken at 8.0 A, with cells (1, 3, 4, 5, 6, 7, 8, 46, 51, 53, and 54) appearing clearly having dendrite cracks.*

Figure 5.1 shows a module that has been in operation for more than 8 years. Module cells with dendrite cracks are cell numbers (1, 3, 4, 5, 6, 7, 8, 46, 51, 53, and 54). These cells appear darker than the rest of the cells on the low EL image taken at 10% of I_{sc}. On the EL image taken at I_{sc} the cells appear with a brightness similar to the rest of the cells. This phenomenon is replicated on the PID detection discussed in the section 5.2. The EL measurement procedure and test conditions used in this work follows the guidelines of the standard IEC TS 60904-13 [1].

Table 5.1 list the modules used in this study, P_{mpp} before and after PID stress and the percentage drop of power. Modules that had been deployed to the field were first cleaned with fresh water and kept dry before power measurements were taken.

Table 5. 1*: List of modules used in this study with Initial Power and Power after PID stress.*

Module	Module type	Number of cells	Initial P_{MPP} (W)	Power After PID stress	% drop in power
A	Mono-120	6 × 12	117.0	102.2	12.6
B	Poly-295	6 × 12	296.0	240.6	18.7
C	Poly -240	6 × 10	230.0	149.6	35.0
D	Poly -260	6 × 10	266.0	187.1	29.7
E	Poly -240	6 × 10	226.9	26.1	88.5
F	Poly -240	6 × 10	230.4	139.3	38.6
G	Poly- 240	6 × 10	228.6	155.7	31.9
H	Poly -250	6 × 10	247.1	246.9	0.1
I	Poly -240	6 × 10	240.1	221.5	7.7
J	Poly -240	6 × 10	240.0	220.3	8.2
K	Poly -240	6 × 10	233.9	148.7	36.4
L	Poly -250	6 × 10	245.7	245.9	-0.1

5.2 PID detection

PID detection is an important aspect of monitoring PV module reliability and long-term performance. PID in modules has traditionally been detected when in a very advanced stage and it may take a longer time to manage and correct the power degradation caused by PID. This work discusses PID detection techniques that, if used correctly can enable detection of PID in its infancy. Such methods include taking EL images at

a current corresponding to 10% of I_{sc} and normalized EL intensity histograms to map out active and inactive areas using origin image analysis software and equations 4.1 to 4.6 in chapter 4. Since R_{sh} decreases drastically due to PID, R_{sh} extracted from Light I-V and Dark I-V measurements may also be used to distinguish PID shunted modules and is detailed in section 5.2.2. Lastly section 5.2.3 discusses methods of comparing V_{oc}, measured at different irradiance levels to detect PID. The percentage decrease in V_{oc} measured at 1000 W/m^2 to that measured at 200 W/m^2 may be used to evaluate PID shunting on the module. Should the drop in V_{oc} be greater than 10%, the module may have undergone PID shunting, because at low irradiance the magnitude of photocurrent decreases significantly. For the purpose of the discussion on PID detection Module A, Module B and Module C listed in Table 5.1 were used. Modules A and B were induced with PID using Method 1, while Module C was stressed using Method 2 as described in 4.4 in chapter 4

5.2.1 EL images taken at a current corresponding to the specified I_{sc} and 10% of I_{sc} of the module

EL images were taken before and after PID stress. EL images and Normalised $P_{EL}(i)$ image intensity histograms are shown in Figures 5.2, 5.3, 5.4 and 5.5 for Modules A and B, respectively. Image histograms plot the normalised $P_{EL}(i)$ (*y-axis)* against normalised pixel intensities of the image. $P_{EL}(i)$ is defined by equation 4.1 in chapter 4. The images shown in figures 5.2 and 5.4 were recorded as follows: Images a) and b) are taken at a current corresponding to I_{sc} of the module, before and after PID stressing, while EL images c) were taken at current corresponding to 10% of I_{sc} of the module after the PID stress. EL imaging taken at a current corresponding to 10% of I_{sc} of the module may result in a less resolved image hence the integration time was optimised in order to record a well resolved EL image.

For Module A, the EL image taken before PID stress in Figure 5.2 a) shows defects such as; cell cracks, impurities and manufacturing defects. After PID stress, Figure 5.2 b) shows cells adversely affected by PID such as (M, N, and O) that are darker than the rest. The overall high EL intensity does, however, make it difficult to identify cells that may have undergone less degradation such as (X, Y, and Z). In Figure 5.2 c), the EL image taken at a current corresponding to 10 % of I_{sc} exhibits overall lower luminescent intensity, the cells appear darker and it is easier to identify

cells that have undergone degradation. It is also then possible to distinguish affected cells that are at a different level of PID.

In the image histograms for Module A shown in Figure 5.3 a) and b) two peaks are observed. The lower intensity peak being visibly smaller, represents dark areas on the images as a result of inactive areas such as busbars, manufacturing defects (dark spots) and inter-cell spaces. The lower EL intensity peak in Figure 5.3 b) broadens marginally since it also includes cells adversely affected by PID. However, all PID affected cells appears masked by the higher intensity peak of the histogram. In the histogram of the low injection (10 % of I_{sc}) EL image (Figure 5.3 (c) the single high intensity peak of Figure 5.3 b) is resolved into two notable peaks with a low intensity peak representing inactive areas that is more pronounced. The middle intensity peak observed at ≈ 0.5 normalised pixel intensity in Figure 5.3 c) (green and red) represents cells least affected by PID and the high intensity EL peak observed at ≈ 0.75 normalised pixel intensity represent cells not affected by PID, as clearly shown for the 10% I_{sc} curve.

For Module B, the EL image in Figure 5.4 b) taken at a current corresponding to I_{sc} after PID stress does not clearly show presence of PID affected cells, as compared to Module A where it was possible to identify cells that are adversely affected by PID when using higher injection levels. However, the EL recorded at a current corresponding to 10 % of I_{sc} in Figure 5.4c) shows several cells such as J, L, and K that have degraded. The cells along the frame are affected more than other cells because, firstly, the frame is biased to +1000 V and secondly, because of a film of moisture on the surface of the glass due to an elevated humidity during the test that serves as a pathway to the electrical ground.

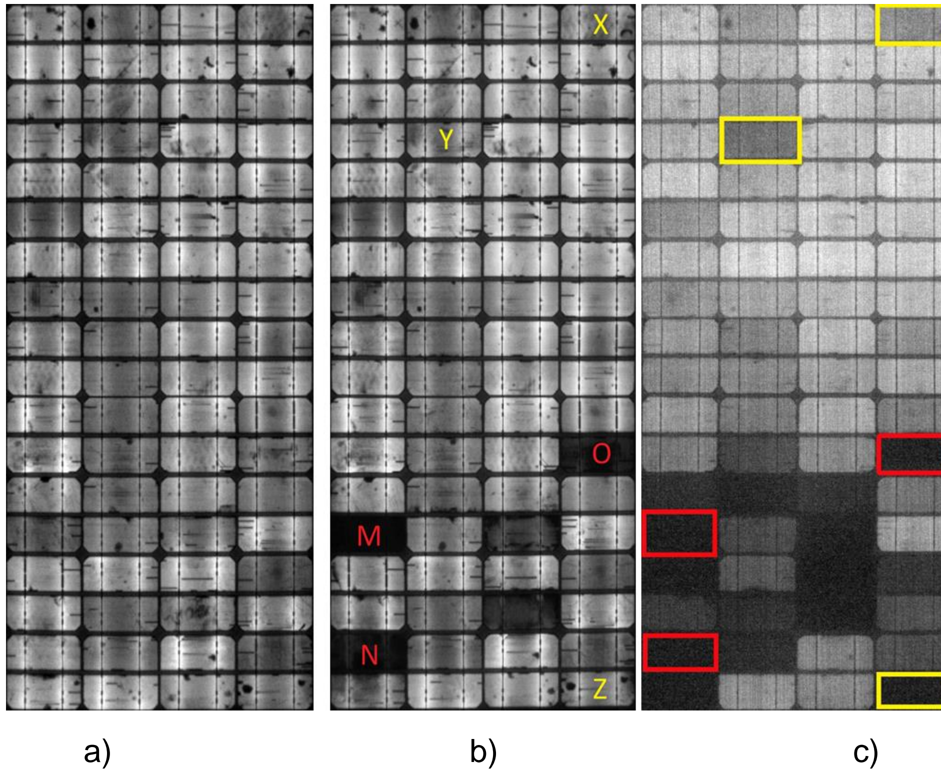


Figure 5. 2: *EL images of Module A. The EL images were obtained as follows: a) and b) EL at I_{sc}, 3.61A, and c) EL at 10% I_{sc}, 0.361A, cells M, N, O are heavily shunted hence visibly dark on figure b) while cells X, Y, Z are less shunted and only observable in figure c).*

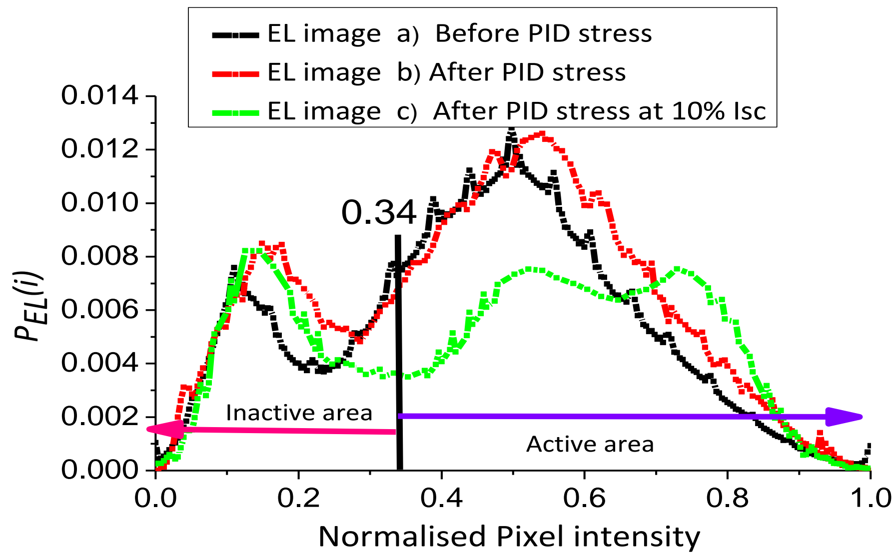


Figure 5. 3: *Normalized (L= 256) EL intensity histograms of Mono-crystalline PV module A, taken before and after 96 hours PID stress. The normalized grey level threshold =0.34 from Otsu`s method [9].*

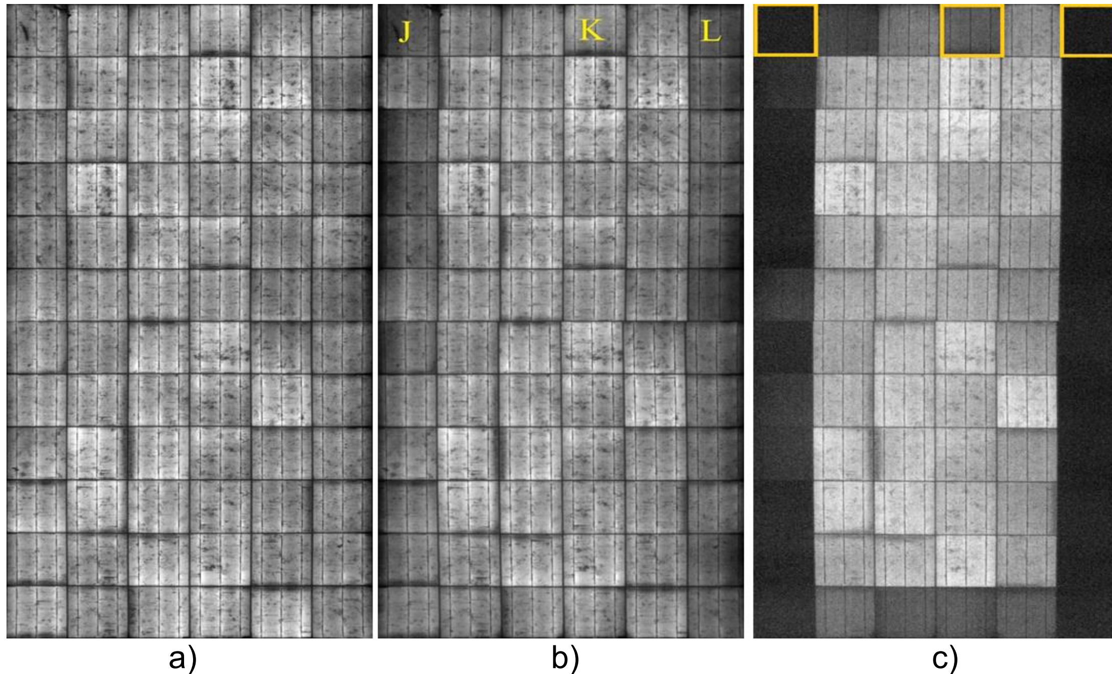


Figure 5. 4: *EL images of Module B. The EL images were obtained as follows: a) and b) EL at I_{sc}, 8.95A, and c) EL at 10% of I_{sc}, 0.895A.*

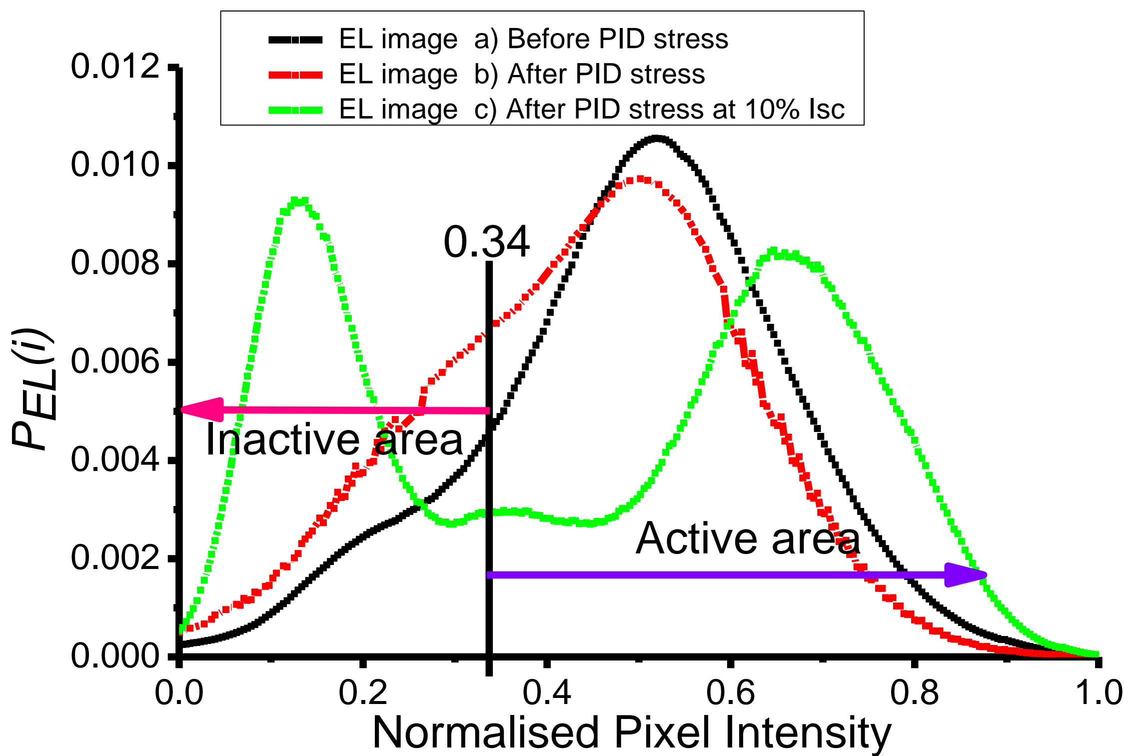


Figure 5. 5: *Normalized (L = 256) EL intensity histograms of multi-crystalline PV Module B, taken before and after 96 hours PID stress. The normalized grey level threshold =0.34 from Otsu`s method [9]*

The image histograms for the EL images for Module B shows a single unresolved peak in Figure 5.5 a) and 5.5 b) at ≈ 0.5 normalized pixel intensity, which may be mistaken as absence of detectable PID affected cells on an EL images taken at I_{sc}. The low injection EL histogram, Figure 5.5 c) however, shows two distinct peaks. The low intensity peak observed at ≈ 0.15 normalized pixel intensity represents PID affected cells along the PV module frame. The second distinct peak observed at ≈ 0.70 normalized pixel intensity represent cells that are not affected by PID, with the majority occurring at the centre of the module. The clear bimodal distribution of the EL intensity histogram in Figure 5.5 c) verifies the value of low injection EL images when the relative effect of low injection currents do not overshadow the detection of PID. This confirms the usefulness of using low injection EL images of modules, recorded at a current corresponding to 10 % of I_{sc} and their corresponding histograms as an accurate and a reliable means of PID detection.

Table 5. 2: *Standard deviation (STD) of The PEL distributions and [%] of module inactive area [MIA], calculated from EL images of Module A and Module B.*

	Module A (STD)			Module B (STD)		
Module Portion	Before PID (I_{sc})	After PID I_{sc}	10% I_{sc}	Before PID I_{sc}	After PID I_{sc}	10% I_{sc}
Entire module	0.040	0.064	0.033	0.056	0.090	0.039
Inactive area only	0.013	0.029	0.018	0.026	0.034	0.025
Active area only	0.037	0.057	0.028	0.050	0.083	0.029
Inactive area [%]	28.37	30.23	32.89	12.07	20.38	37.65

The standard deviation (STD) of the $P_{EL}(i)$ distribution can be used as a relative measure to evaluate the condition and quality of a module. A small STD value is a sign of a good quality module while a higher value hints at a module with defects or of poor quality [2]. Before PID stress, the module can be assumed to be in good condition hence it should have a smaller STD. After PID stress the module can be said to have degraded, hence the STD is expected to increase. Table 5.2 lists the STD for the entire module which increases from 0.040 to 0.064 in Module A, while in Module B the STD increases from 0.056 to 0.090 for EL images taken at current corresponding to I_{sc} of the individual modules before and after PID stress. For the active regions of the modules the STD increases from 0.037 to 0.057 and from 0.050 to 0.083 for Module A and Module B, respectively.

The increase in STD of the active area is because of increased PID shunting which effectively has the implication of decreasing EL signal intensity and the quality of the

module. The STD for inactive area also increases from 0.013 to 0.029 and 0.026 to 0.034 for Module A and Module B respectively. The greater margin of increase in Module A is because cells that are adversely affected PID are visible in Figure 5.2 b) which is not the case in corresponding Figure 5.3 b) of Module B which show no shunted cells.

The [%] inactive area increases in both Module A and Module B after PID stress. The Inactive area percentage is a measure of shunted areas in addition to inter-cell spaces, busbars and manufacturing defects. The [%] inactive area as a result of shunting can be obtained based on equation 4.6. The difference between the [%] inactive area of module before PID at I_{sc} and [%] inactive area after PID at 10% of I_{sc} gives the total possible [%] inactive area which for Modules A and B translates to 4.5 and 25.6 in [%] points, respectively.

EL imaging together with its pixel intensity histograms gives improved accuracy when evaluating observed PID shunting. Of particular significance are EL images taken at current corresponding to 10% of I_{sc}, which display a clear bimodal distribution on the histogram. In order to quantify the PID in terms of power losses, Light-IV and Dark-IV measurements were recorded and the extracted parameters such as R_{sh}, and R_s were used to evaluate the presence of PID shunting in a module in absence of EL images.

5.2.2 Light-IV and Dark-IV curve measurements

Light-IV (L-IV) measurements are essential in detection of PID degradation in PV modules. L- IV characteristics curves recorded for Module A and B before and after PID stress are shown in figure 5.6 a) and figure 5.6 c), respectively. Table 5.3 list the module parameters extracted from the L-IV curves for Modules A and B, before and after PID stress. Figure 5.6 a) shows some rounding of the “knee” at the P_{mpp} point after PID stress for Module A, representing an increase in the ideality factor and a 12.6% power drop and FF drop from 0.76 to 0.66. Figure 5.6 c) shows a more pronounced rounding in the “knee” at P_{mpp} for Module B, which resulted in 18.7% power drop and FF drop from 0.75 to 0.63. The decreasing slope at V_{oc} indicates an increasing R_s. From Table 5.3, R_s increased from 1.3 Ω to 1.7 Ω for Module A and 0.5 Ω to 0.7 Ω for Module B. R_{sh} from Table 5.3 decreases drastically from 10.0 kΩ to 175.4 Ω for Module A and from 1111.1 Ω to 133.3 Ω for Module B. This decrease is manifested as a decrease in the slope of L-IV curve at low voltages.

Since applying PID stress does not affect the module's cell contacts, the main cause of the change in the module's cell resistance can be attributed to changes of the semiconductor material. The R_s increases in both Module A and Module B resulting in a decreased mobility of charge carriers after PID stress [3]. R_{sh} in both modules decreases after PID stress, which may be attributed to presence of Na^+ ions which may be responsible for increased carrier recombination as well as an increase in leakage current paths. The increase in *n* (ideality factor) in both modules is an indication of an increase in saturation current.

The Dark-IV (D-IV) measurements were taken while the module under test was connected in forward bias in the dark and plotted as shown in Figure 5.6 b) and 5.6 d). The region where R_{sh} dominates in a D-IV curves was identified as 0-5 V while R_s dominates between 40-48 V. The reciprocal of the tangent gradients was obtained as indicated in Figure. 5.6b) and 5.6d) and give an indication of the relative resistance values. In Figure. 5.6 b) the obtained R_{sh} decreases from 4.3 Ω to 2.8 Ω while R_s increases from 7.9 Ω to 13.4 Ω. In Figure 5.6 d) R_{sh} decreases from 2.7 Ω to 2.5 Ω while R_s increases from 8.3 Ω to 11.6 Ω. This results confirms that R_{sh} decreases after PID stress while R_s increases as was observed in L-IV curves and listed in Table 5.3. PID shunted modules can then be identified using D-IV measurements as follows: increase in steepness at low voltages indicating decreased R_{sh}. At high voltages the tangent becomes less steep to indicate increasing R_s.

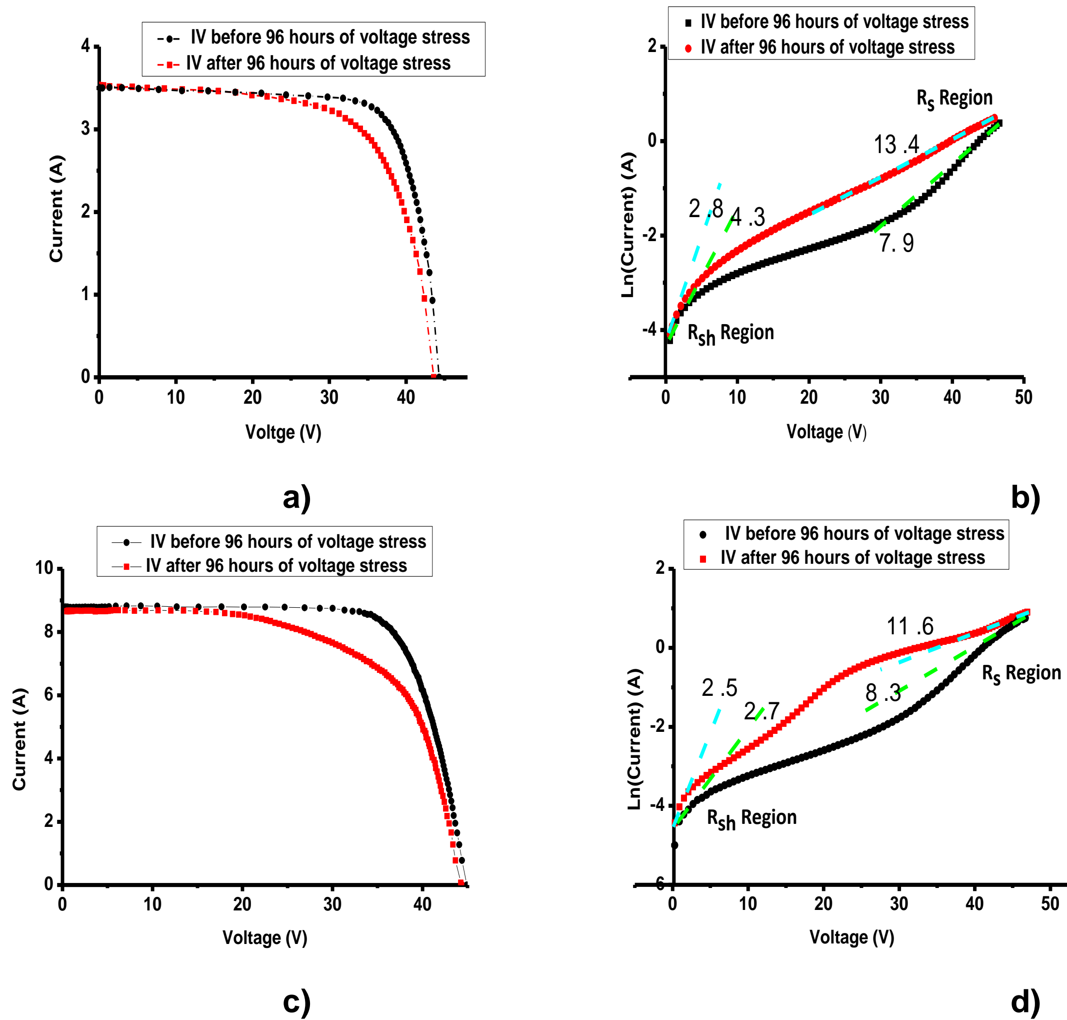


Figure 5. 6: I-V *characteristics of modules before and after PID Stress: a)* L-IV *Curve of Module A. b) D-IV Curve Module A. c) L-IV Curve of Module B. d) D-IV Curve of Module B. The values indicated are reciprocals of the respective tangents in Ω.*

Table 5. 3: *Module A and B extracted solar parameters; V_{oc} (open circuit voltage); I_{sc} (short circuit current; P_{mpp} (maximum power point), FF (Fill Factor), R_{sh} (Shunt resistance), R_s (series resistance and Ideality factor (n).*

Module		V_{oc}	I_{sc}	P_{mpp}	FF	R_{sh} (Ω)	R_s (Ω)	*n*	% increase in *n*
A	Before PID	44.3	3.5	117.0	0.76	10000.0	1.3	1.1	39.5
	After PID	43.6	3.5	102.2	0.66	175.4	1.7	1.6	
B	Before PID	44.9	8.8	296.0	0.75	1111.1	0.5	1.5	35.2
	After PID	44.3	8.7	240.6	0.63	133.3	0.7	2.0	

It is important to note that by considering parameters such as I_{sc} and V_{oc} at STC (25°C, 1000 W.m^{-2} and A.M 1.5) that only change marginally, PID stress cannot conclusively been shown. However, V_{oc} taken at low irradiance is severely affected after PID stress

hence can be used as an important PID shunting detection L-IV parameter. This is because carrier losses to shunting paths become visible with decreased photocurrents [4].

5.2.3 Comparison of open circuit voltage (V_{oc}) at 1000 W.m^{-2} to 200 W.m^{-2}

L-IV measurements were measured first at STC and thereafter at low irradiance, when the simulator is set at a temperature of 25°C, Irradiance of 200 W.m^{-2} and A.M 1.5. The V_{oc} from the two measurements were extracted and compared separately for before and after PID stress. Under a PID free condition the V_{oc} percentage drop, between the V_{oc} recorded at 1000 W.m^{-2} and 200 W.m^{-2} should be less than 10%. However, in a situation where the percentage drop recorded is beyond 10%, the shunting currents are of comparable magnitude with the diminished current generation at low irradiance may be responsible for decreased performance.

Table 5.4 lists the V_{oc} and P_{mpp} taken on Module C before and after PID stress as shown in Table 5.1. The pre PID shunting V_{oc} dropped by 8.0%, while after PID stress the V_{oc} registered a 36.4% drop. The P_{mpp} before PID stress dropped by 82.4% and 91.7% after PID. From Table 5.4 an analysis of V_{oc} shows a drop of 28.4% while P_{mpp} dropped by 9.3%. The V_{oc} dropped by nearly 3 times on percentage points compared to P_{mpp} hence accentuating the significance of V_{oc} parameter in PID detection. The low irradiance power measurements are affected because electron holes generated are lost to shunting paths which become dominant with decreased photocurrent [4].

Table 5. 4: *Table of V_{oc} and P_{mpp} taken at 1000 W.m^{-2} and 200 W.m^{-2} irradiance.*

Module C	Before PID			After PID		
Irradiance	1000 W.m^{-2}	200 W.m^{-2}	%	1000 W.m^{-2}	200 W.m^{-2}	%
V_{oc}(V)	37.3	34.3	8.0	36.0	22.9	36.4
P_{mpp}(W)	230.0	40.5	82.4	149.6	12.4	91.7

5.3 PID stress induction methods

In this study three methods were used to induce PID. The methods were intended to simulate and accelerate module operational conditions that lead to PID. All methods made use of a purpose-built environmental chamber that is able to maintain conditions at a maximum temperature of 35 °C ± 1 °C and humidity of 75% RH ± 5% RH. All methods utilised a bias of 1000 V applied between the electrically active components and either the frame or different size aluminium plates, with or without elevated temperature and humidity conditions. The methods are summarised as follows:

Method 1: The bias is applied to the module frame at 35 °C ± 1 °C and humidity of 75% RH ± 5% RH.

Method 2: The bias is applied to an aluminium plate or foil that covers all the cells in the module without making any contact to the frame at 35 °C and < 40 % RH.

Method 3: The bias is applied to an aluminium plate that covers only one cell at 35 °C and < 40 % RH.

5.3.1 Method 1: PID stress by environmental conditioning

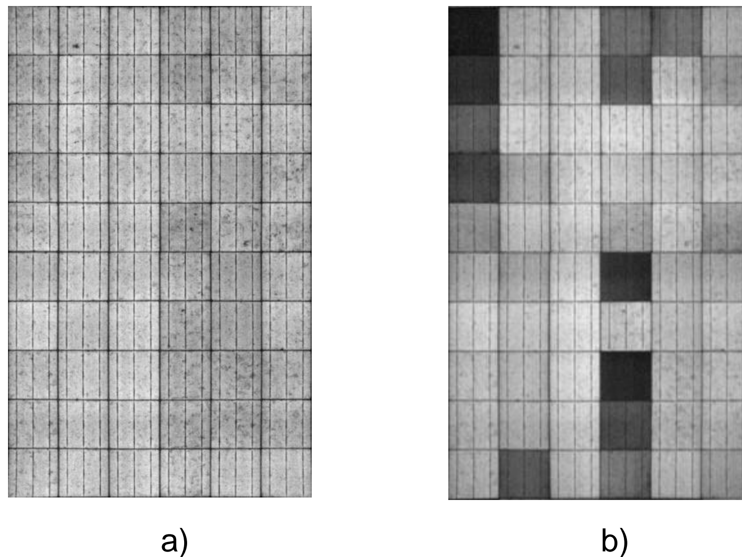
Method 1 of PID stress involved biasing the frame to the positive of the voltage safety analyser and the negative terminal was connected to the short-circuited PV module terminals. A temperature of 35 °C ± 1 °C and a relative humidity of 75%RH ± 5% RH were maintained for the duration of the stress period. The modules under test were subjected to 168 and 288 hours of PID stress and a bias voltage of 1000 V. The magnitude of power degradation due to PID depends on high voltage stress time, environmental chamber temperature, and humidity and voltage bias applied. Module samples A, B, and D as listed in Table 4.1 and Table 5.1 were used for this PID stressing. These modules were new and classified as PID resistant as indicated on the name plates.

Details of the main outcome of the PID stressing using Method 1 are listed in Table 5.5. In the table the module power before and after PID stressing, stress time and power degradation rate are listed. The % rate of degradation is defined as the percentage drop in power due to PID stress divided by PID stress time.

Table 5. 5: *Modules power measurements comparison table before and after PID stress*

Module	P_{mpp} Before PID stress (W)	P_{mpp} after PID stress (W)	PID stress time (h)	% Rate of degradation (%/h)
A	117.0	102.2	168.0	0.08
B	296.0	240.5	168.0	0.11
D	266.0	187.1	288.0	0.10

In Module A the power decreases by ≈ 0.08% per hour while, Modules` B and D show a similar power loss of ≈ 0.11% per hour. Module A is mono-crystalline while B and D are both multi-crystalline, hence the similarity in their degradation rates. In module B cells along the frame are more likely to be affected by PID than those at the centre as observed on the EL images shown in Figure 5.4 c) and Figure 5.7 b) shows a similar trend to a lesser degree for module D. The reason for high susceptibility is first because they are close to the frame which is point of application of voltage bias and secondly because a thin film of water due to high humidity forms close to the frame increasing glass surface conductivity resulting in increased shunting as shown in Figure 5.7 b).



a) b)

Figure 5. 7: *Module D, EL images taken at 10% of I_{sc} (0.982A), a) Initial EL image, b) EL image after 288 hours of PID stress.*

In the absence of the high humidity under environmental chamber conditions, PID can be induced using aluminium foil covering the module glass surface and in contact with the frame for biasing this as stipulated the standard IEC 62804-1. This work presents

two modified methods in section 5.3.2 and 5.3.3 where an aluminium plate not in contact with the frame is used as a positive terminal and to make the surface of the glass conductive.

5.3.2 Method 2: Aluminium sheet cover method

The module short circuited terminals were connected to a negative terminal of the safety voltage analyser while the positive bias was connected to the aluminium plate laid on the glass surface but not touching the aluminium frame. This method is different from the case provided on the standard IEC 62804-1, where the aluminium foil is grounded with the frame and wrapped around the module. The aluminium foil procedure is subject to three limitations, first the aluminium foil may not uniformly touch on the glass surface affecting uniformity of the electric field applied even though the standard advises using a rubber to ensure that the aluminium foil is laid uniformly, secondly it may promote high leakage current which may promote other degradation mechanism and lastly aluminium foil may not be reusable due to wear and tear. In method 2, the leakage current reached a maximum of ≈0.002 mA throughout the stress period. This means that the insulation properties of the module are not affected. For new modules this PID stress degradation method may yield insignificant results due to the absence of free Na^+ near the glass-encapsulant interface. Na^+ only develop due to moisture ingress and other reactions within the encapsulation and glass over a long period of deployment time in the field. Secondly, the present generation of multi-crystalline modules being produced uses encapsulation materials with a very high resistivity. Modules previously deployed in the field when subject to PID stress using method 2 may show signs of PID after 5 hours of PID stress as opposed to 168 hours as proposed in the standard IEC 62804-1 test (as it was in the case for Module F shown in Figure 5.8). The method described here is quick and doesn't affect the insulation and physical integrity of the module. The module reached a saturation point when further PID became insignificant after 20 hours of PID stress.

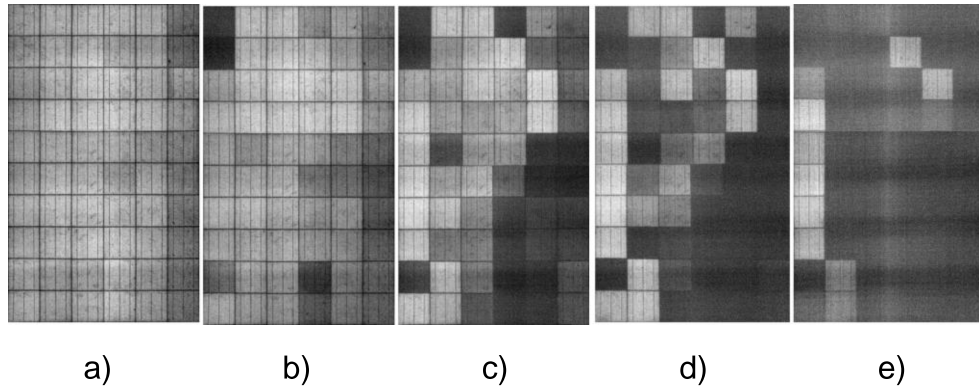


Figure 5. 8: *EL images of Module F were taken at current corresponding to 10% of I_{SC}. The EL images were taken before PID stress and after every 5 hours of PID stress. a) EL taken before PID stress test; b) EL image taken after 5 hours of PID stress; c) EL image taken after 10 hours of PID stress d) EL image taken after 15 hours of PID stress; e) EL image taken after 20 hours of PID stress.*

Figure 5.9 shows D-IV measurements measured before PID stress and after PID stress of every 5 hours for the duration of PID stress of 20 hours. Between 0-42 V there is observation the deviation from the initial D-IV measurements indicating increased shunting in the module after PID stress.

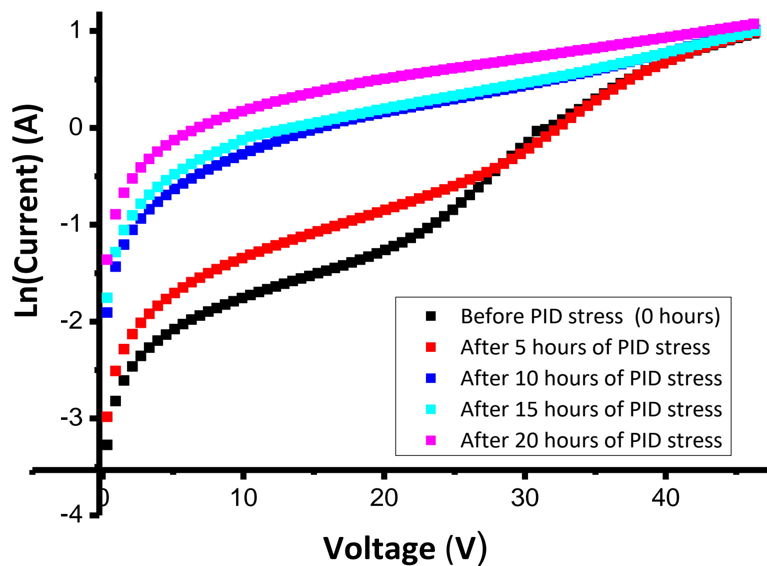
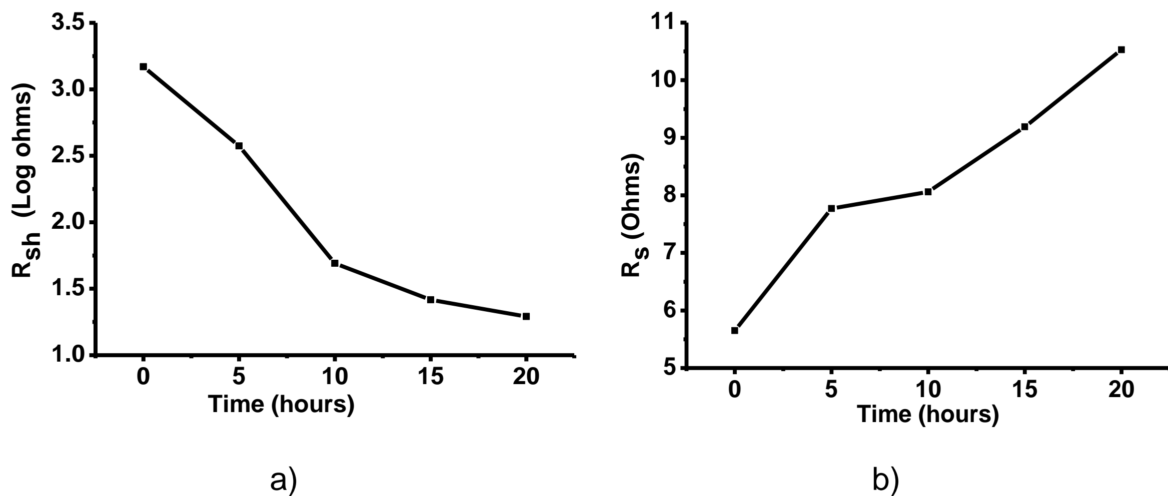


Figure 5. 9: *The dark-IV measurements taken on module sample F, the plotted measurements are for before PID stress and after every five hours of PID stress.*

***Table 5. 6**: List of the extracted R_{sh} and R_s for the Module F at time intervals of 5 hours from the D-IV measurements in Figure 5.9.*

Time (hours)	0	5	10	15	20
R_{sh}(Ω)	1,478.94	374.49	49.12	26.11	19.55
R_s (Ω)	5.65	7.77	8.06	9.19	10.53

Table 5.6 lists the extracted R_{sh} and R_s from the D-IV measurements obtained from Figure 5.9. R_{sh} is obtained at low voltages while R_s is obtained at higher voltages of each graph. Figure 5.10 plots extracted R_{sh} and R_s listed in Table 5.6. The measurements show that as PID progresses with time, R_{sh} decrease as shown in Figure 5.10 a), while R_s shows that as PID stress time progresses the R_s extracted increases as shown in Figure 5.10 b). The decrease in R_{sh} is because of increased shunting which in turn increases charge recombination sites while an increase in R_s confirms increased leakage current. The R_{sh} is plotted on log scale because the R_{sh} drops drastically from thousand to tens hence need for compressed scale.



a) b)

***Figure 5. 10:** a) plots shunt resistance in log scale of the shunt resistance extracted at low voltages of figure 5.9 with respect to time b) plots extracted series resistance at high voltages of figure 5.9 with time*

In addition to Module F, Modules E, G and H were also subjected to PID using Method 2. Module (E, F and G) had been deployed for more than five years, while Module H had not been deployed to the field. The aluminium sheet was used as an anode and to simulate a conductive glass surface. Table 5.7 lists results of Modules that underwent PID stress Method 2. Modules (E, F and G) show significant degradation of more than 1.0% per hour. While Module H showed insignificant drop in power

degradation of 0.002% per hour. The failure to induce PID in model H could be due to use encapsulation with high resistivity.

***Table 5. 7**: Power measurements on modules before and after PID stress in listed modules*

Module	P_{mpp} Before PID stress (W)	P_{mpp} after PID stress (W)	PID stress time (h)	% Power drop per hour (%/h)
E	226.9	26.1	48	1.8
F	230.4	139.3	20	2.0
G	228.6	155.7	24	1.3
H	247.1	246.9	48	0.002

5.3.3 Method 3: A case localised PID

In this method of PID stress, a small plate, equal to the area of a module cell was connected to the positive terminal of the voltage safety analyser while the short-circuited PV module terminals were biased to the negative terminal. A localised electric field develops which induces PID on the cell of interest (cell number 25), neighbouring cells (16, 24, 26 & 36) and other cells on cells not neighbouring the cell of interest (cell numbers 21 & 40) Figure 5.11 b). Since the aluminium plate used was equal in size to the dimension of the cell, it would have been expected that only the cell of interest will be affected and possibly the neighbouring cells. The cell of interest is marked by green block (cell number 25). The numbering orientation is described in Figure 4.8.

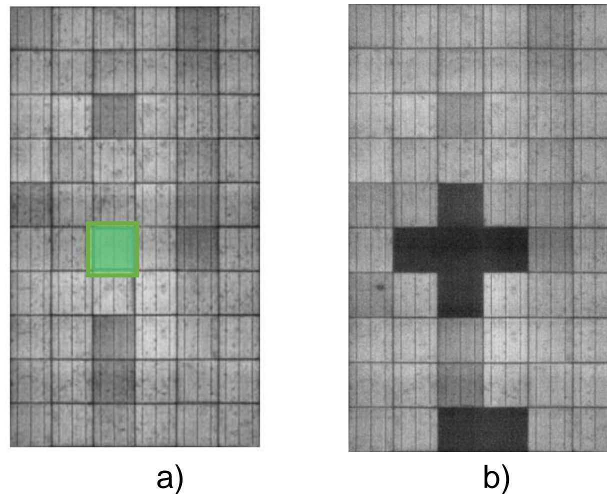


Figure 5. 11: *Module I, EL images taken at 10% of I_{sc} (0.982A), a) Initial EL image, b) EL image after 96 hours of PID stress.*

The modules used in this section are of the same type (multi-crystalline). Module (I and J), are 240 poly which had been deployed for more than 5 years and Module L, a 250-poly new and classified as PID resistant. The % normalized power loss per hour is ≈ 0.08 W/hr, the power loss caused by this localised PID may be substantial considering that only one cell was targeted. For Module L the % power drop is negligible because it is PID resistant and a new module as presented in Table 5.8.

Table 5. 8*: List of modules power measurement before and after PID stress*

Module	P_{max} Before PID stress	P_{max} after PID stress	PID stress time (hours)	% Normalized power drop per hour (W/hr)
I	240.1	221.5	96	0.08
J	240.0	220.3	96	0.09
L	245.7	245.9	336	-0.0006

The results from Method 3 suggests the conductive nature of the glass surface and the fact that some cells are more highly susceptible to PID than other cells in a module. This result may not be conclusive and hence need for more research on the case of localised PID stress induction on a module.

PID induced in modules discussed above is called PID shunting which involves a high potential causing a leakage current to flow between the module frame and module cells. In addition, the high potential causes migration of sodium ions from module glass to the surface of the cell. Eventually at right concentration levels, diffusion into the

PN-junction causing major shunting. PID Method 1 induces PID both on new and deployed modules. This was attributed to the fact that during PID stress inside the environmental chamber the module undergoes accelerated degradation. In addition, new modules take longer to degrade than deployed modules. Method 2 and 3 could only induce PID on modules already deployed to the field for 7 years. The methods were unable to induce any significant PID on the new and un-deployed modules. The PID induced in this section is reversible either by way of natural recovery in the dark at open circuit or by way of forced reverse bias in the dark. Section 5.4 explores the module power recovery in detail in different modules.

5.4 Module power recovery after PID stress by way of natural and forced reverse bias.

The modules were subjected to PID stress and evaluated using the techniques discussed in subsection 4.4. The modules showed varying degrees of PID and the characteristics are summarized in Table 5.9. In Table 5.9 the initial and degraded power of the modules are listed together with the associated % drop in power (the ratio of difference between initial and final power, initial power) and % recovery (ratio of power recovered to power lost). The rate of recovery is determined based on recovery period and is quoted either as per minute or per day, depending on the recovery time.

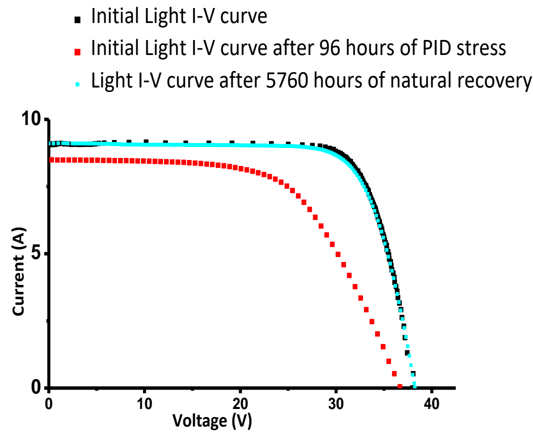
Table 5. 9: *List of modules used for PID stress and recovery investigation.*

Module	Initial P_{mpp} (W)	Post PID stress P_{mpp} (W)	P_{mpp} drop (%)	Type of recovery	Duration	Post Recovery P_{mpp} (W)	P_{mpp} recovery (%)	Rate of Recovery
B	296.0	240.5	18.8	Natural	12 months	280.9	72.8	0.20 W/Day
D	266.0	187.1	29.6	Natural	8 months	261.2	93.9	0.39 W /Day
E	226.9	26.1	88.5	Natural	7 months	116.2	44.8	0.21 W/Day
F	230.4	155.6	32.4	Natural	7 months	209.1	71.5	0.34 W/Day
K	233.9	148.7	36.4	Reverse Polarization	120 min	229.5	94.8	0.79 W/Min

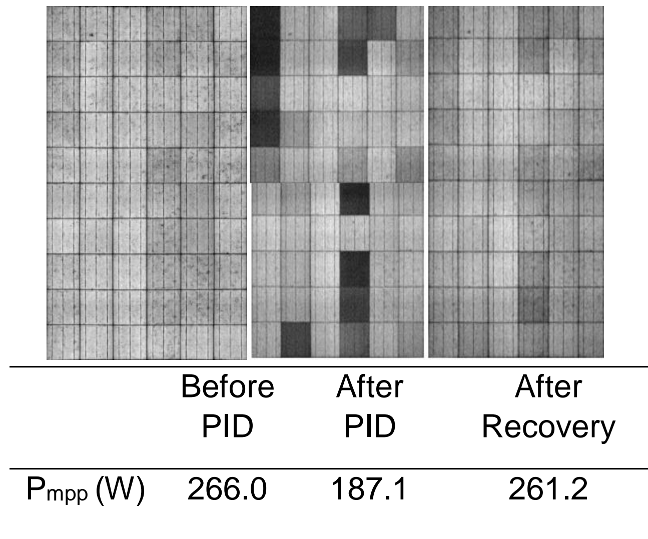
Module B degraded by 18.8% and underwent natural recovery (the module was kept at open circuit in a dark room) for a period of 12 months with 72.8% recovery, making its recovery relatively slow compared to the other modules. Module D was undergoing natural recovery at room temperature in the dark under open circuit conditions. After 8 months the power recovery level was 93.9 % of the initial power. Module E which belongs to the same class as Module F and K underwent extreme PID, with a power loss of 88.5 %. After more than 6 months of natural recovery the module had recovered 44.8% of the lost power. Module F lost 31.9% of its initial power after PID stress and recovered 71.5 % of the lost power. Module K underwent forced reversed biased recovery and after 120 minutes the module power recovered to 94.8% of the degraded power.

In addition to assessing PID recovery based on power measurement, EL images taken at a current corresponding to 10% may also be used as a tool to show recovery. EL images that show no shunting are indicative of modules that may have recovered 100% of lost power. The PID and subsequent recovery of modules D and K serve to illustrate this for extreme degradation and recovery via two different methods. Figure 5.12 shows the respective L-IV curves and EL images of these modules measured before PID, after PID stressing and after PID recovery. The results for Module D are shown in a) and b), and those for Module K in c) and d).

The I-V curves, Figure 5.12(a,c), show that the performance parameters of the modules degraded substantially after PID stress and the P_{mpp} recovered to within 5 W of the initial measurement after the respective recovery treatments. The trend of degradation is also observed in the EL images Figure 5.12 (b,d), with the typical checkerboard pattern of varying luminescence being prominent after PID stress. After recovery the EL images are again relatively uniform with the absence of the checkerboard pattern indicating recovery. The module recovery may not be 100% because Na^+ may not have been completely evacuated from defect sites within the PN junction. In the case of natural recovery procedure, the procedure is slow since it only depended on diffusion as the mechanism to evacuate Na^+ from the defect sites within the PN junction and cell surface. Forced recovery combines both drift and diffusion of Na^+, hence it is quick taking approximately 120 minutes (Module K) as compared to 8 months in the case of natural recovery (Module D).

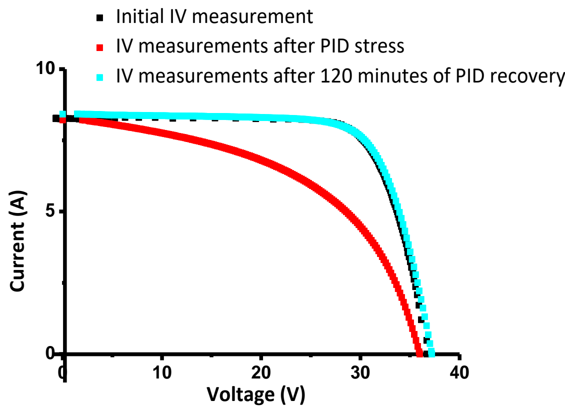


a)

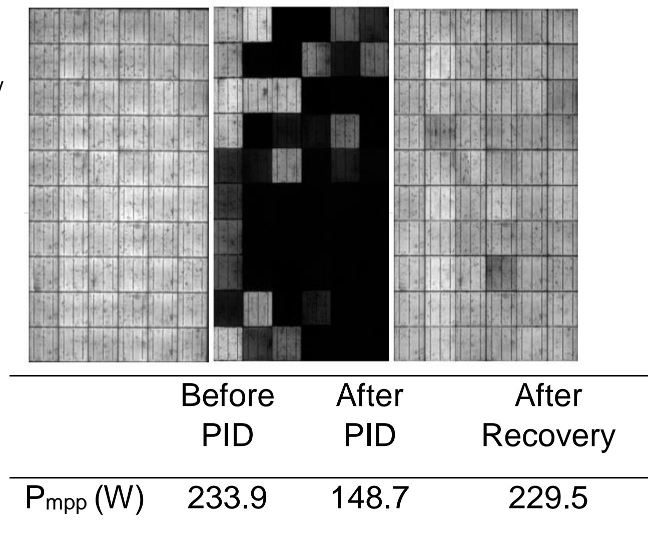


	Before PID	After PID	After Recovery
P_{mpp} (W)	266.0	187.1	261.2

b)



c)



	Before PID	After PID	After Recovery
P_{mpp} (W)	233.9	148.7	229.5

d)

Figure 5. 12: *L-IV curves and EL images taken at (I_{sc} = 10% of I_{sc} of modules D and K; a) Light I-V measurements for Module D. b) EL-images of Module D with the measured P_{mpp} tabulated. c) Light I-V measurements for Module K. d) EL-images of Module K with the measured P_{mpp} tabulated.*

Further investigations on power recovery of regeneration were carried out on 2 modules (E and F) that had been deployed in the field for 5 years prior to being subjected to PID stress. The two modules E and F were subjected to different PID stressing times using Method 2. For Module E the PID stress time was 48 hours, while for Module F, PID stress time was 20 hours. The intention was to induce different levels of degradation and study the subsequent regeneration of power. After degradation, the modules were kept at open circuit in the dark at room temperature.

Power measurements were then taken and EL images recorded periodically over the 6-month natural recovery period. Figure 5.13 shows the respective I-V curves and EL images of the modules at different times during the recovery period. The respective power measurements and associated % regeneration are listed in Table 5.10. Percentage regeneration is calculated as follows

$$\% \, Regeneration = \left(\frac{P_{fmpp} - P_{impp}}{P_{mpp} - P_{impp}}\right) \times 100\% \qquad (1)$$

Where P_{mpp} is the power measurement taken before PID stress, P_{impp} is power measurement taken immediately after PID stress and P_{fmpp} is the subsequent power measurement taken periodically over a span of 6 months after onset of power regeneration.

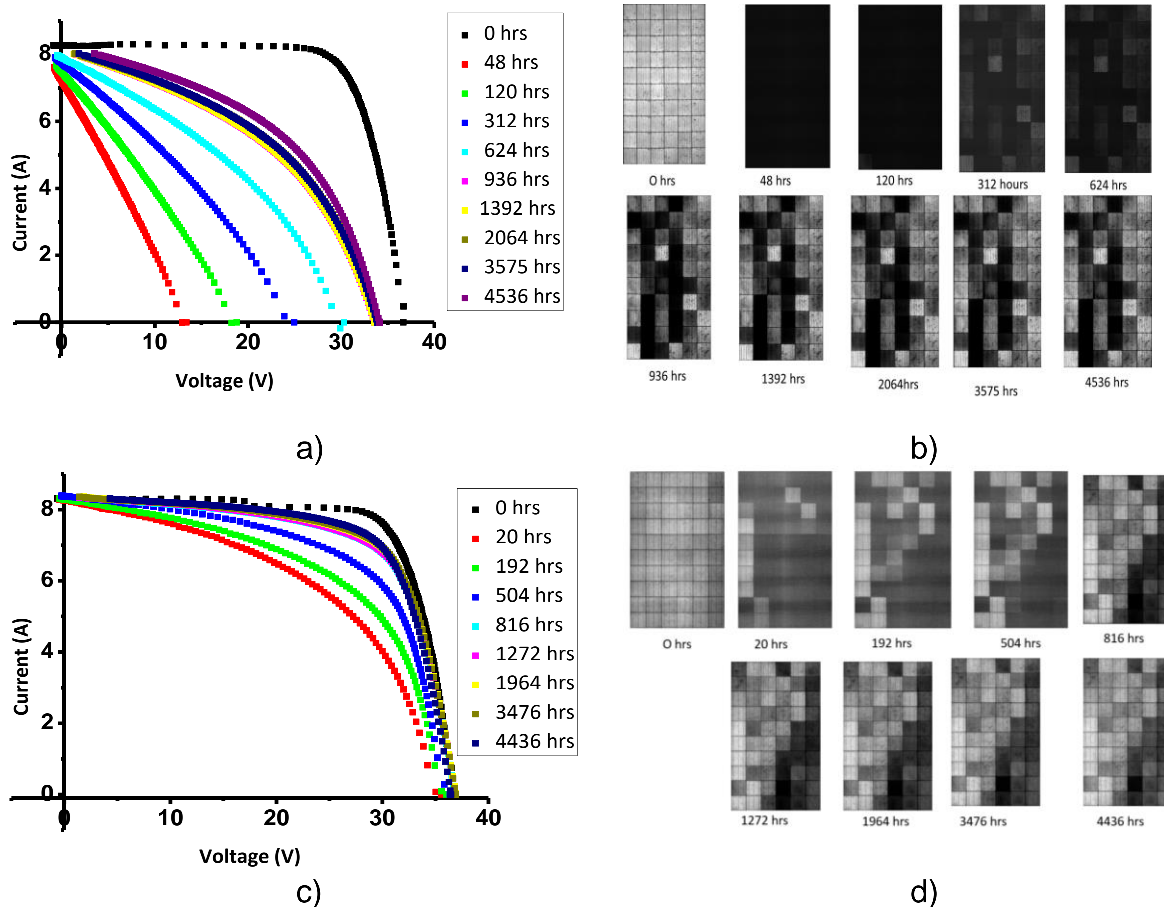


Figure 5. 13: *a) I-V measurements for Module E under PID module recovery; b) EL images of Module E under PID module recovery EL image taken at I_{sc}; c) I-V measurements for Module F under PID module recovery; d) EL images of Module F under PID module recovery. EL images Taken at 10% of I_{sc}*

***Table 5. 10**: P_{mpp} at different times during the recovery period Modules E and F. the initial power measurement for Modules E and F are 226.9 W and 230.4 W respectively*

Time (hours)	0	120	312	624	936	1392	2064	3575	4536
Module E (P_{mpp})(W)	26.14	39.29	58.76	85.60	96.38	109.68	116.20	116.60	120.80

Time (hours)	0	192	504	816	1272	1964	3476	4436
Module F (P_{mpp})(W)	139.26	155.68	178.92	184.16	195.44	204.10	205.20	207.40

The % regeneration as function of time is shown in Figure 5.14 for both modules. The figure also shows the empirical fit used to estimate regeneration progression. Since the regeneration is much faster in the initial hours of regeneration and as time (t) progresses, the regeneration slows down, log-linear plot is appropriate. The derived regeneration equation from Module E is:

$$\% Regeneration = 25.26Log(t) - 43.63 \quad (2)$$

The derived regeneration equation from Module F is:

$$\% Regeneration = 34.14Log(t) - 49.19 \quad (3)$$

The module recovery estimate for Module E to regain 95% of the power lost under room temperature conditions which fluctuate between 20 °C to 25 °C will take approximately 35 years according to equation 1. For Module F under the same conditions it is estimated to regenerate 95% of the lost power in approximately 2 years according to equation 2. These results suggest that the time taken for regeneration is related to the degree of power degradation on the module.

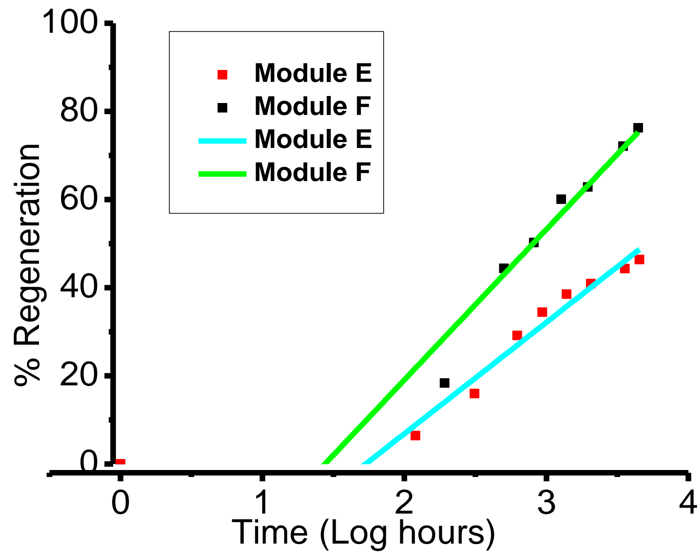


***Figure 5. 14**: % Regeneration against time in hours on a log scale for Module E and F, the modules degraded by 88.5% and 32.4% of Initial P_{MPP}, respectively.*

In a PV power plant natural regeneration takes place at night despite the low temperatures that may be experienced at night [5]. These results suggest that the longer the night the greater the PID regeneration at solar power plant level, this means winter seasons experience greater regeneration than summer.

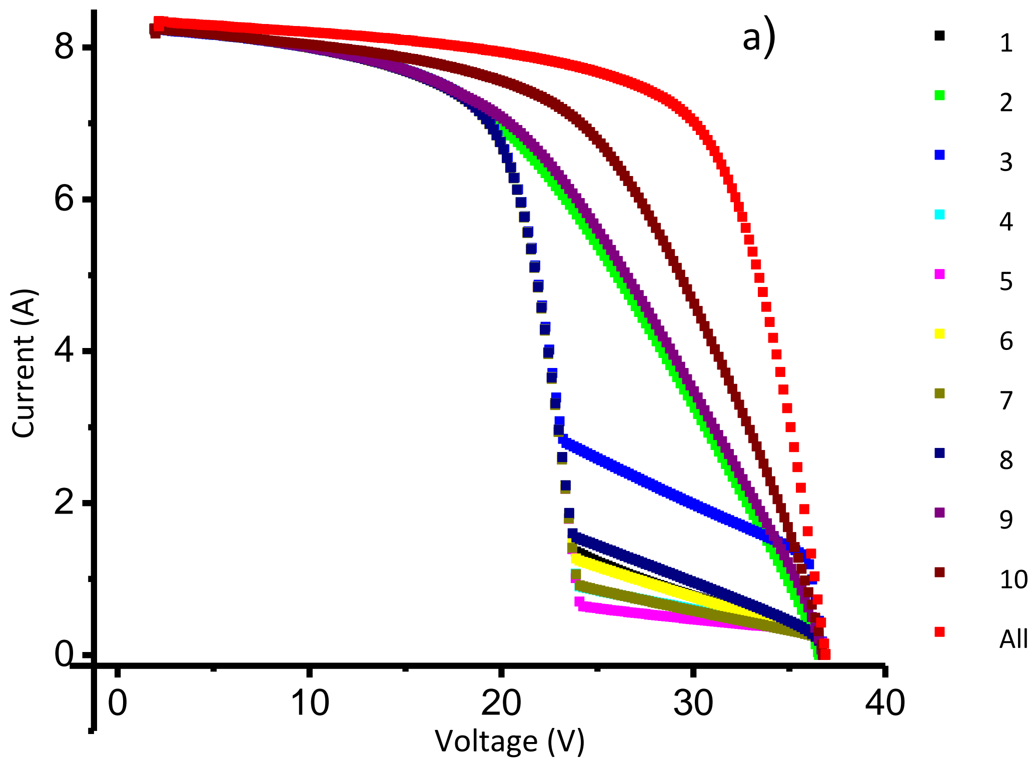
In summary, partial module power recovery on different modules was achieved. The recovery depends on extent of PID severity and time available for modules to recover naturally. Under forced reverse bias, modules recover within a short period of time. PID shunting in modules leads to noticeable cell mismatch where cells that are heavily shunted are worse performing than un-shunted cells. Module F was used to investigate cell mismatch in a module after regeneration at room temperature. This is discussed in detail in section 5.5 below.

5.5 PID cell mismatch analysis

Cell mismatch in a module may be caused by manufacturing defects, defects in the cell crystallography, grain boundaries and soiling or PID shunting. In order to study the effect and level of mismatch caused by PID, a module (Module F) that was subjected to PID stress and allowed to recover to a power recovery level of 73.3% was used. The analysis included the worst-case cell determination using the method proposed by Herrmann et al, 2002 [6] and EL images. For comparison, the analysis was also done on Module L that remained PID free after PID stress using Method 3.

In the worst-case method, the L-IV curves of the module are taken with the cells sequentially shaded and then compared to the unshaded L-IV curve. With one cell shaded, the L-IV curve should have the expected step due to the activation of the bypass diode. However, should the shaded cell be degraded, the shading will not have this impact and the “knee” does not exhibit a step. PID affected cells will thus have L-IV curves that do not have the pronounced step.

Figure 5.15 shows the L-IV curves for Modules F and L with cells in column 1 (cells 1 to 10) shaded and the unshaded L-IV curves. From Figure 5.15 a) it is observed that cells 2, 9 and 10 in column 1 of Module F exhibit shunt-like behaviour and may be considered worst-case cells. For Module L, no cells fall into the category of lower performing cells (worst-case) as shown in figure 5.15 b). These observations were confirmed by the respective EL images of the modules. Figures 5.16 (Module F) and 5.17 (Module L) show the EL images of the modules (a), together with image maps of mean EL intensity per cell (b) and P_{mpp} with respective cells shaded (c).



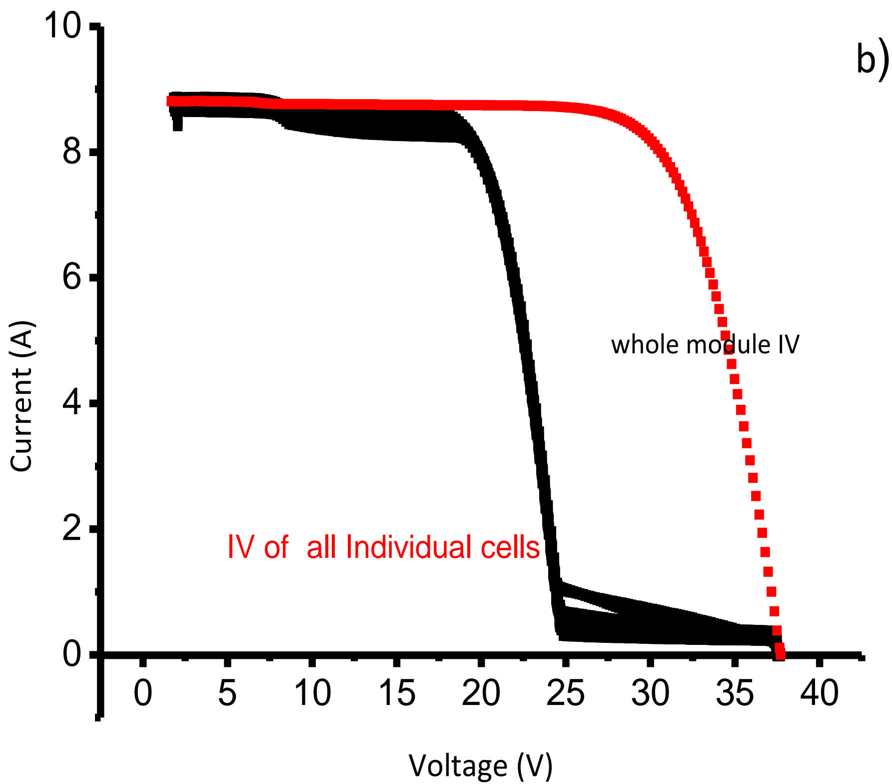


Figure 5. 15: *Light I-V curve of Module E (a) and Module L (b) and Light I-V of all the 60 cells shunted individually*

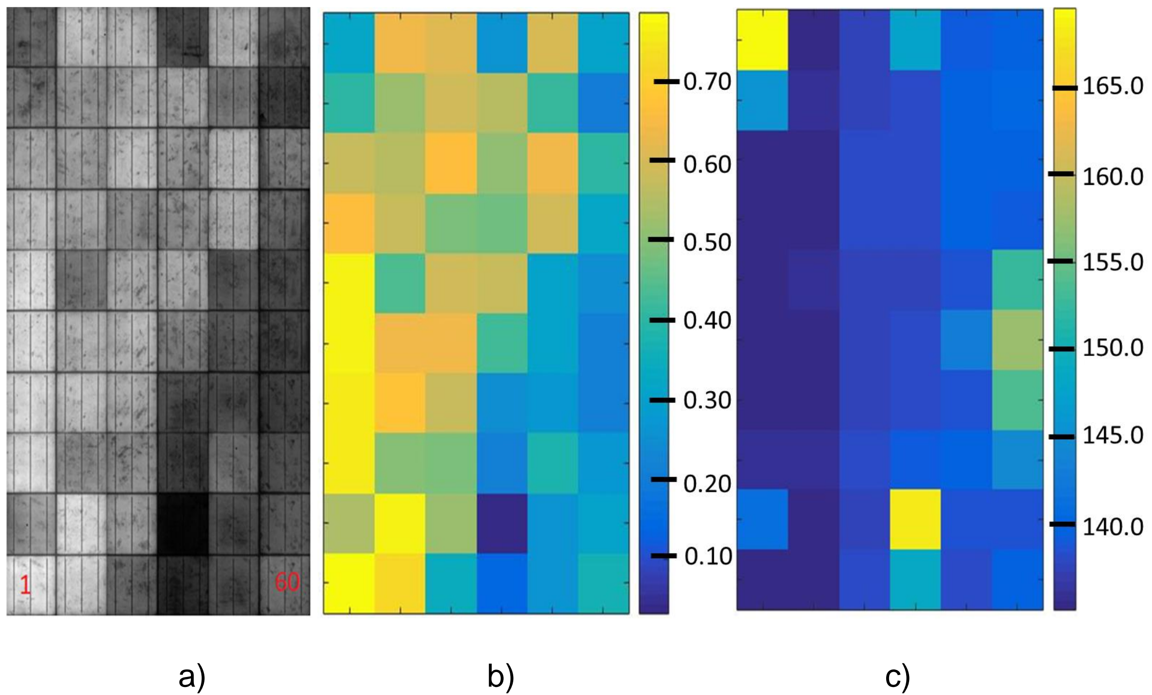


Figure 5. 16: *a) EL images of Module E taken at current corresponding to 10% of I_{SC}. b) Mean EL intensity per cell in arbitrarily units 0 minimum and 1 maximum. c) Maximum power output of module with sequential single cells shaded in watts. The mismatch spread over 34.7 W range at STC.*

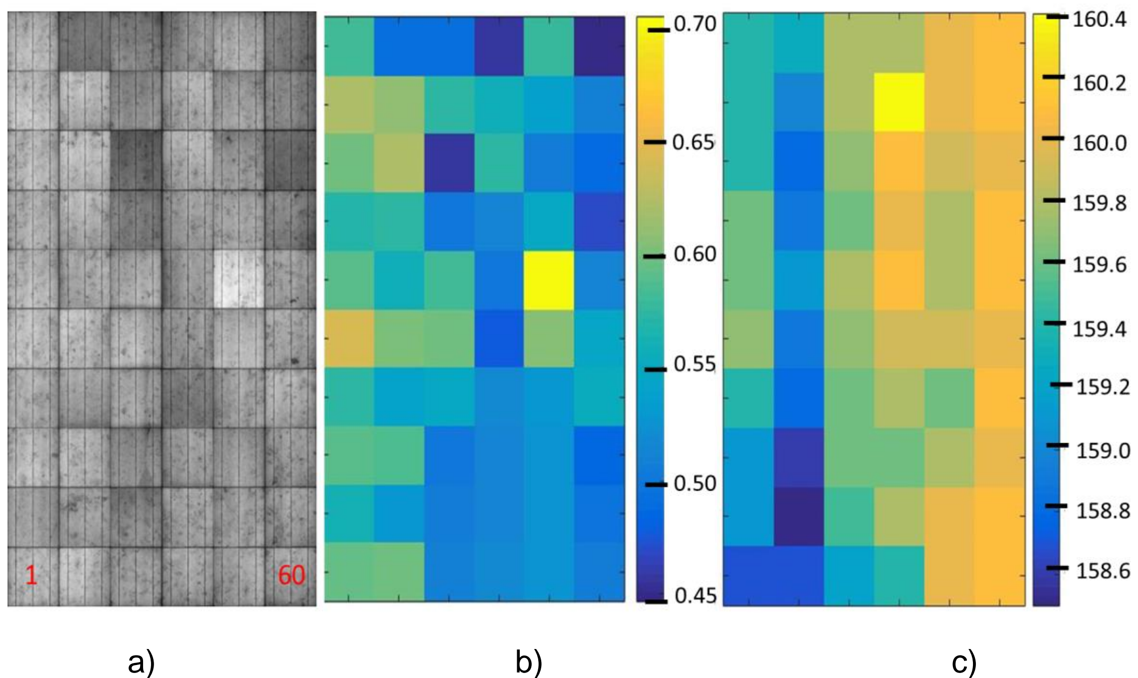


Figure 5. 17: *a) EL images of Module L taken at current corresponding to 10% of I_{SC}. b) Mean EL intensity per cell in arbitrarily units 0 minimum and 1 maximum. c) Maximum power output of module with sequential single cells shaded in watts. The mismatch spread over 1.9 W range at STC.*

In the EL image of Module E (Figure 5.16 a) cells 2, 9 and 10 may be classified as cells that exhibit PID shunting when compared to the rest of the cells in column 1, in

agreement with the worst-case experiment. For the rest of the module, cell number 39 is worse affected because it appears darker than the rest of the cells in the module. The checkerboard pattern of the EL image (a) is clarified by the average EL intensity levels plot (b), where the level of PID severity may also be clearly seen. The maximum power per shaded cell (from worst-case experiment) shown in (c) is further confirmation of the effect of PID shunting and subsequent cell mismatch. Cells that do not have much impacted on the P_{mpp} are the worst performing cells, viz. cells number 10 and 39. The module mismatch based on power measurements on Module F cells spread over 34.7 W at STC

Figure 5.17 shows the EL images Module L taken at 10% of I_{sc} a), its corresponding EL mean cell intensity b) and P_{mpp} mismatch c) for Module L. The P_{mpp} range is 1.9 W at STC which implies that the cells are closely matched, and it is what should be expected of any new module. Cell number 32 in this context is the worst performing based on P_{mpp} contrary to the EL image and EL mean intensity which displays the cell to be normal.

Cell mismatch is more pronounced in a PID shunted Module F as compared to PID free Module L. Extreme cell mismatch in a module may be responsible for hot spots in some cells which may worsen the already degradation module. Whereas modules that degrade by PID can regenerate and can be redeployed to the field for continued power production. It is important to check on module insulations properties. This is done by investigating leakage currents and insulation properties both in air and when wet. Since modules sometimes operate in wet or rainy environments, they are prone to fail insulation tests but rectifies when the skies clears up. Excessive leakage currents in a module may result in catastrophic failure of a module. Leakage currents are investigated in the following section.

5.6 Leakage current analysis

The leakage current and insulation properties values were recorded while the module is submerged in a pool of water at room temperature of 20-25 °C. Each test cycle takes 120 minutes in order to minimise moisture ingress. The power measurements of Modules E and F were taken before and after PID stress as shown in Table 5.1. Module E lost 88.5% of the initial power after PID stress, while Module F lost 39.5%.

Table 5.1 lists the leakage current and insulation properties of the modules before and after PID stress both in air and when submerged in water.

Table 5. 11: *List of Insulation resistance and leakage current results on a module sample*

	Module	Leakage Current(dry) [mA]	Insulation resistance(dry) (MΩ)	Leakage Current (wet) [mA]	Insulation resistance (wet) (MΩ)
Before PID stress	E	0.002	11600	0.039	88
After PID stress	E	0.038	90	0.071	47
Before PID stress	F	0.002	12000	0.034	102
After PID stress	F	0.035	102	0.086	39.2

Under high voltage stress on the module in air the leakage current is lower and increases when the module is submerged sunny side down in water. The IEC standard requires that the leakage current monitoring should not exceed 0.05 mA and the insulation resistance should not be less than 40 $M\Omega.m^{-2}$ (63 MΩ for this module). From the results in Table 5.11 the modules pass the insulation test before PID stress both in air and in water. After PID stress the modules passes the test in air, however in water they both fail in insulation properties while passing the leakage current. The test illustrates that modules that are degraded by way of PID shunting are reversible since the modules only fails when the environment is wet such as when raining. From this results PID shunting in a module may be tested by measuring the insulation properties of the module when submerged. When a module fails this test, chances are it may be PID shunted. Although this method of leakage current analysis cannot conclusively detect PID in the module it may highlight compromised structural properties of a PV module.

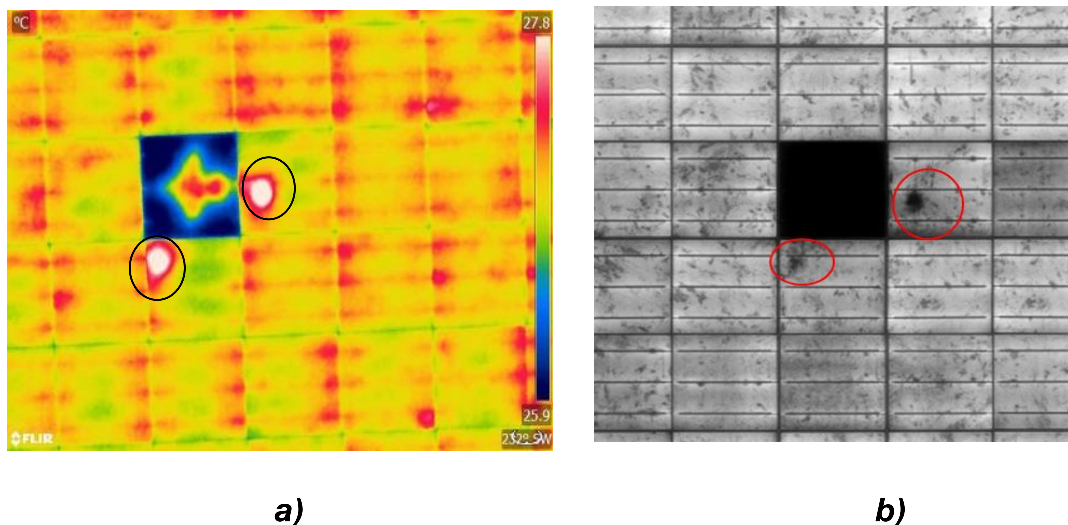
5.7 Thermal Infrared (IR) imaging (TIR)

Infrared thermography is a non-destructive and non-contact defect detection technique. The method can be done in one of two modes. The first method involves biasing a module in the dark and taking the TIR image from the back. The current into the module is then driven to the I_{sc} of the module and left in that state for some time

until the module heats and a reasonable IR image is recorded. The second mode is recording TIR images of modules under normal irradiance at operational point, I_{sc} or V_{oc}.

The TIR image shown in Figure 5.18 a) was recorded from the back of the section of the module I. In indoor IR thermography images cells that are underperforming appear cooler than the rest of cells in the section of the module, while regions of localised shunts appear warmer due to resistive heating. Figure 5.18 b) shows a corresponding front EL image of the section of module I. The two images correlate in such a way that the shunted cell on EL image appears cooler than the rest of the neighbouring cells.

The distribution of heavy shunting starts from the edges of the cells towards the centre of the cell. The centre of the shunted cell on the IR images behaves similar to a delaminated cell based on simulation on cell delamination [7]. This result further suggests that the centre of the shunted cell may be least or partially shunted. The two cells bordering the shunted cells each have a hot spot (encircled) representing defect zones in a cell. The zones may represent onset of heavy shunting since in Figure 5.11b) the EL image of the same section of the module taken at current corresponding to 10% of I_{sc} shows the two cells to be shunted cells.



a) b)

Figure 5. 18: *IR thermography and EL image of a PID affected section of module (Module I) at the same applied test current I_{sc} in the dark. a) The IR image shows that the strongly affected cell is cooler than the rest. b) The EL image shows that the affected cell appears darker.*

In an outdoor setup, Module I was placed outside on a tracker on a clear sunny day. TIR images shown in Figure 5.19 were recorded when the module was at; b) open

circuit, c) short circuit and d) when operating close to P_{mpp}. The EL image shown in a) shows cell number 25 to be heavily shunted, while cell numbers 21, 24 and 36 show some points of shunting on the module as it regenerates 7 months after PID stress. The initial EL image immediately after PID stress showed these cells to be heavily shunted as shown in figure 5.11 b).

The module under open circuit is expected to display homogeneous distribution of temperature which is not the case with localised PID affected cells that displayed inhomogeneous distribution of temperature with cells not affected by PID shunting having higher temperature than the shunted cell as recorded in b). In c) the higher temperatures were observed in cell numbers 18, 39, 54 and 57, these cells may have gotten warmer because they were operating at a current lower than I_{sc} hence becoming hotspots. When the module is operating close to P_{mpp} the PID shunted cell got warmer than the rest of the module cells as shown in d). The results in d) correlated with the EL image in a). PID in modules can only be observed if the module operates under load close to P_{mpp}.

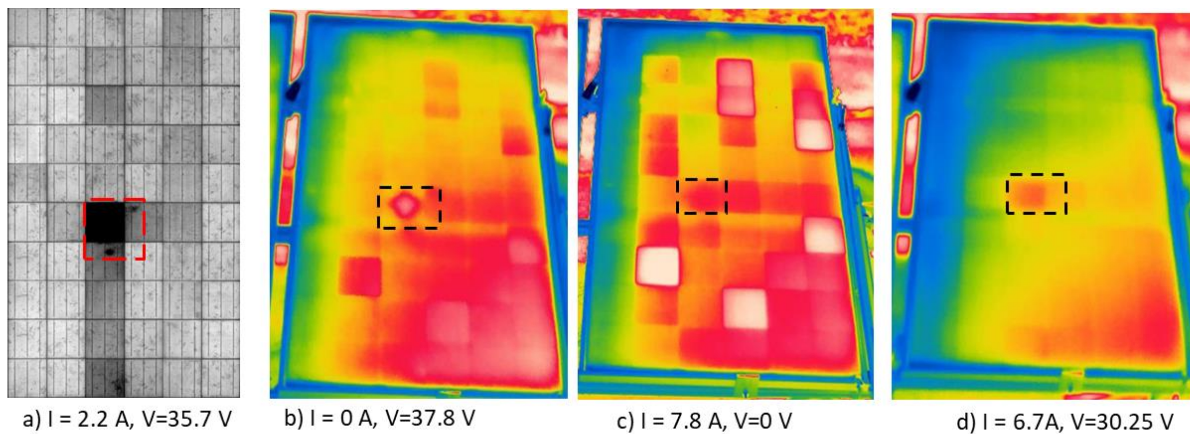


Figure 5. 19*: EL and IR thermography of a PID affected Module I under sunlight conditions (approx. 700 W/m²): a) The EL image taken at low Current to optimise visibility of shunted cells. b) Open circuit, the cell temperature distribution is inhomogeneous and PID-s is not detectable except that the centre of PID affected cell overheats c) Short circuit: several hot cells hot cell (white) cell number (18, 39, 54 and 57) these cells are not PID-s affected, the cells may have overheated by reverse biasing due to lower I_{sc}. d) Close to MPP: the IR image is in good agreement with the EL image [8]*

5.8 Conclusion

PID detection in modules after PID stress was done successfully using the EL images taken at 10% of I_{sc}. A histogram of EL intensity distributions shows a clear bimodal distribution of normalized pixels on EL images taken at low current. Extracted solar power parameters sensitive to PID shunting such R_{sh}, FF, P_{mpp} and R_s from L-IV play a crucial role in PID detection. I_{sc} is the least sensitive while V_{oc} is more sensitive when the module is heavily shunted or when the module is operating under low irradiance. V_{oc} measurement at low irradiance can be quick and less sophisticated way of detecting PID in a module, especially those deployed in the field.

PID shunting quantification on EL images recorded at I_{sc} and 10% of I_{sc} was done in three stages. First visualization of the degree of darkness which represents shunted cells at different levels of PID severity. Followed by statistical quantification on a histogram featuring bimodal distribution and lastly calculation of the STD. EL histograms were used to estimate the [%] area of inactive and inactive sections of the EL images. The calculation of active and inactive areas enabled quantification of dark spots on a module, inter-cell distance and busbars on EL image before PID stress. The quantification of the shunted area was obtained by getting the difference between inactive area before PID stress and after PID stress on the module. It is a considered opinion of this research that detection procedures presented in this section may be integrated into onsite PV system quality control to quantify degradation on modules during handling (transportation, storage and installation) of the module in order to establish baseline degradation module profiling. The baseline measurement can then be used in subsequent tests to quantify any form of PID shunting, if any.

L-IV measurements are crucial in quantifying the impact of shunting on solar power plant output. During L-IV re-testing after years of module operation, a certain minimum threshold power measurement can be set to trigger mandatory low current EL imaging and low irradiance IV measurements. If this is implemented it will help in finding out if PID is the cause of power drop. The three detection techniques explained in section 5.2 are accurate and easy to use to detect PID shunting on a module, a phenomenon that may be common in large PV power plants. To explore these detection techniques and procedures described above, PID was induced in a controlled environment using three methods. Method 1 uses local environmental conditions of a maximum temperature of 35 °C and humidity levels maintained at 75 %RH. Method 1 induced

PID on both new and field deployed modules. Method 2 and method 3 used aluminium plate PID induction procedure commonly used in situation-controlled condition is not possible. The EL results from Method 1 showed PID shunted cell distributed along the frame, while for Method 2 shunted cells were observed distributed evenly in most parts of the module. Method 3 EL images were unique in the sense that the cell neighbouring the cell covered by the aluminium plate and other located away from the cell of interest were shunted. This work could not make a clear conclusion on this EL results from Method 3, hence the need for further investigation.

Module regeneration investigation revealed the reversibility of PID shunting. This work was limited to two procedures of natural recovery at room temperature and forced reverse bias recovery. In both the modules, regeneration reached almost 95% with natural recovery requiring longer period of about 12 months, while the reverse bias recovery only required 120 minutes. There is a need to further investigate the regeneration rate under short circuit and at V_{oc} in outdoor conditions.

IR thermography results on a module that had been induced with PID using Method 3 showed inhomogeneous temperature distribution in open circuit, a condition where the distribution is supposed to be homogenous. At short circuit several cells heat up as a result of mismatch, while during optimum module load conditions, only shunted cells appear to be warm.

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CHAPTER 6

6. SUMMARY AND CONCLUSION

6.1 Summary

In this investigation PID was successfully induced in different PV modules which were thoroughly characterised before and after PID stress using various techniques. These included power measurements (L-IV), D-IV measurements, EL imaging, and TIR imaging. In addition, PID recovery was investigated over a period of 12 months.

Carrier recombination as revealed by electroluminescence (EL) plays an important role in the detection of a degradation mechanism such as PID. Module performance is depended on charge transport, collection probability and quantum efficiency. By comparing module parameters extracted from the IV curves such as FF, I_{sc}, V_{oc}, P_{mpp}, I_{mpp}, R_{sh} and R_s it is possible to determine if the module is undergoing degradation.

The primary causes for PID have been a subject of extensive scientific investigation; some of the possible causes from literature include the accumulation of Na^+ ions in the stacking faults within the PN junction. The source of the Na^+ is the silicate glass cover commonly used in most PV modules. The migration is caused by the electric field caused by the high potential between the frame and the cells and aided further by environmental conditions such as temperature and humidity. Greater effort has been put in place by module manufacturers to limit the migration of the Na^+; they include the use of a high resistive encapsulation materials such as ionomers, introduction a thin layer of silicon oxide between the anti-reflective coating (ARC) and the Si cell surface. These efforts are aimed at limiting or preventing Na^+ from reaching the cell surface hence mitigating the PID defect.

In this study PID was induced using three methods, each of which led to a unique outcome. PID stress Method 1 induced PID on a new module and deployed modules by creating a strong electric field by applying high a DC voltage between the module frame and cells. High humidity levels created a conductive moist surface that may be responsible for accelerated PID degradation. Methods 2 and 3 caused PID by using a conductive aluminium sheet on the module glass surface to simulate a conductive moist surface. These methods failed to induce any significant PID on a new module.

The possible reason could be the encapsulation used has high resistivity. Methods 2 and 3 may be used to test module PID status at a particular point in time because it doesn't involve accelerated module degradation.

Despite several efforts to manage PID, it still may occur, especially in large strings due to exposure to high DC voltage over a long period, hence the need to investigate PID progression in order to manage the PID evolution at infancy. In this work EL images taken at a current corresponding to 10% of I_{sc} were successfully used to detect PID. The normalised image intensity distribution on EL images displayed a bimodal frequency distribution that were more distinguishable on an EL image taken at 10% of I_{sc} as compared to those taken at I_{sc}. Each EL image was divided into inactive and active regions corresponding to the intensity distribution. The standard deviation (STD) of intensity was calculated from each area before and after PID stress. In addition, the V_{oc} of a c-Si module at a low irradiance is affected by PID drops more than expected compared to the V_{oc} drop of a non PID affected module at low irradiance.

PID shunting caused by the drift of Na^+ is reversible. The module PID recovery and power regeneration was successfully investigated and revealed that 100% P_{mpp} module power recovery was not always possible. PID recovery was investigated by using several methods such as keeping the module in the dark for periods up to 12 months in open circuit as well as reverse polarization. Some modules had good recovery of up to 94.5% of P_{mpp}. Further investigations need to be done to monitor module recovery progression under short circuit conditions and under load near the module's P_{mpp} under outdoor irradiance. In general, the time required for a module to regenerate appears to be proportional to magnitude of initial power loss.

PID stress Method 1 induced PID on a new module and previously deployed modules and was attributed to the high humidity levels that increased the conductivity of the cover glass surface leading to accelerated PID degradation. Methods 2 and 3 could only induce PID in old and deployed modules and failed to induce any significant PID in a new module. The possible reason could be that the encapsulation material of the module has high resistivity.

TIR imaging was also successfully used to identify cells that were PID shunted in a module in three ways; when the module was operating at, or close to P_{mpp} only PID

shunted cells are warmer. When a module is placed under short circuit current condition, cells that are not PID shunted but operating below the module I_{sc} become warmer. At the module open circuit condition (V_{oc}) when no external current flows, the cells are not heated by an external current and should show a uniform temperature distribution. However, when cool air blows over the module, uneven cooling may occur that is clearly distinguishable when a group of neighbouring cells on the downwind edge of the module are marginally warmer that the rest of the module. In addition to these warmer cells, cells that are severely affected by PID may show much localised resistive heating from a self-generated recombination current.

6.2 Future Work

Topics that may need further investigation include:

- PV modules' P_{mpp} regeneration after PID stress under outdoor irradiance and in controlled climatic chambers at elevated temperatures.
- The reason for PID shunting to occur on cells not neighbouring the individual cell under PID stress using Method 3.
- Microstructural analysis of PID in various types of module encapsulants and shunting progression in encapsulated cells.

APPENDIX A

Research outputs associated with this work

1. JOURNALS/ REFEREED PUBLICATIONS

1.1 IM Kwembur, JL Crozier, EE van Dyk, FJ Vorster
"DETECTION OF POTENTIAL INDUCED DEGRADATION IN MONO AND MULTI-CRYSTALLINE SILICON PHOTOVOLTAIC MODULES"
Physica B (Submitted May 2019, published online 07 December 2019). Available [https://doi.org/10.1016/j.physb.2019.411938]

2. PUBLISHED PROCEEDINGS

1.2 IM Kwembur, JL Crozier, EE van Dyk, FJ Vorster
"OPTIMISATION OF ELECTROLUMINESCENCE SETUP FOR CHARACTERISATION OF PHOTOVOLTAIC MODULE DEGRADATION"
Proceedings of the 5th Southern African Solar Energy Conference (SASEC 2018), Durban, South Africa (June 2018). (ISBN 978-0-7972-1765-2)

1.3 RM Dix-Peek, IM Kwembur, EE van Dyk, FJ Vorster, CJ Pretorius
"PARAMETER OPTIMISATION OF INDIVIDUAL CELLS THROUH VOLTAGE DEPENDENT ELECTROLUMINESCENCE OF AN EXPERIMENTAL SILICON MODULE"
Proceedings of the 5th Southern African Solar Energy Conference (SASEC 2018), Durban, South Africa (June 2018). (ISBN 978-0-7972-1765-2)

1.4 IM Kwembur, JL Crozier, EE van Dyk, FJ Vorster
"COMPARATIVE STUDY OF POTENTIAL INDUCED DEGRADATION APPROACHES IN MULTICRYSTALLINE SI PV MODULES"
Proceedings of the 6th Southern African Solar Energy Conference (SASEC 2019), East London, South Africa (November 2019). (Under Review)

3. RESEARCH PAPERS AT CONFERENCES

3.1 IM Kwembur, EE van Dyk, JL Crozier, FJ Vorster, RM Dix-Peek and MK Munji
"ASSESSMENT OF PHOTOVOLTAIC MODULE DEGRADATION USING ELECTROLUMINESCENCE AND OTHER OPTO-ELECTRONIC TECHNIQUES."
10th African Laser Centre Student Workshop, University of Stellenbosch, South Africa (November 2017).

3.2 IM Kwembur, EE van Dyk, FJ Vorster, JL Crozier
"STUDY OF POTENTIAL INDUCED DEGRADATION (PID) IN PHOTOVOLTAIC MODULES."
PV Workshop 2018, University of Venda, South Africa (April 2018).

3.3 RM Dix-Peek, IM Kwembur, EE van Dyk, FJ Vorster, CJ Pretorius
"PARAMETER OPTIMISATION OF INDIVIDUAL CELLS THROUHJ VOLTAGE DEPENDENT ELECTROLUMINESCENCE OF AN EXPERIMENTAL SILICON MODULE"
5th Southern African Solar Energy Conference (SASEC 2018), Durban, South Africa (June 2018).

3.4 IM Kwembur, JL Crozier, EE van Dyk, FJ Vorster
"OPTIMISATION OF ELECTROLUMINESCENCE SETUP FOR CHARACTERISATION OF PHOTOVOLTAIC MODULE DEGRADATION"
5th Southern African Solar Energy Conference (SASEC 2018), Durban, South Africa (June 2018).

3.5 IM Kwembur, JL Crozier, EE van Dyk, FJ Vorster
"POTENTIAL INDUCED DEGRADATION (PID) PERFORMANCE LIMITING DEFECT DETECTION IN POLYCRYSTALLINE SILICON MODULES USING LOW CURRENT ELECTROLUMINESCENCE IMAGING."
11th ALC student workshop held on 22 November- 24 November 2018, Wallenburg Research Centre, University of Stellenbosch, South Africa

3.6 IM Kwembur, JL Crozier, EE van Dyk, FJ Vorster
"DETECTION OF POTENTIAL INDUCED DEGRADATION IN MONO AND MULTI-CRYSTALLINE SILICON PHOTOVOLTAIC MODULES"
8th South African Conference on Photonic Materials (SACPM), Kariega Game Reserve, South Africa (May 2019).

3.7 IM Kwembur, EE van Dyk, FJ Vorster, JL Crozier
"A CASE STUDY ON MONOTORING PID RECOVERY ON MULTICRYSTALLINE MODULES" Poster.
64th Annual SAIP Conference, Polokwane, South Africa (July 2019).

3.8 IM Kwembur, EE van Dyk, FJ Vorster, JL Crozier
"COMPARATIVE STUDY OF POTENTIAL INDUCED DEGRADATION APPROACHES IN MULTICRYSTALLINE SI PV MODULES.
6th Southern African Solar Energy Conference (SASEC 2019), East London, South Africa (November 2019).