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Three-Level Converters for Low Voltage Active Front End Motor Drives

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THREE-LEVEL CONVERTERS FOR LOW VOLTAGE ACTIVE FRONT END MOTOR DRIVES

by
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ABSTRACT

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by
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Electric drives with Active Front End (AFE) converters can provide benefits such as lower harmonic current injections to the grid, smaller size filters, lower THD values and cost saving for injection of power to the grid in brake situations. SiC-MOSFET based two-level converters can be a promising topology for Active Front End (AFE) application in electric drives. The possibility of high switching frequency will make the grid filters smaller. Grid filters are used for EMC and power quality issues. However, there are practical limitations for increasing the switching frequency such as dead time in the gating signals, sampling requirements, and electro-magnetic interference (EMI) considerations, besides the need for high frequency magnetic material for the LCL line filter. However, three-level converters provide the opportunity to switch at a lower frequency and also reduce the filter size compared to a two-level IGBT converter. Three-level converters can be built using low voltage rated modules with lower switching losses and reduced cost compared to SiC based two-level converters. In this work, a comparison between three-level converters and two-level converters is presented focusing on power loss, filter size and application benefits. This comparison is based on an optimization algorithm with the objective function of weight, volume and cost.

The topologies and modulation techniques for multilevel converter are categorized at first by a thorough literature survey. The pros and cons for various multilevel topologies and modulation techniques are discussed. The 3-level neutral point clamped (NPC) topology is selected to build a 25 hp, 480V power conversion system.

LCL filter design for comparability with grid requirements has been done and the optimal size of the LCL filter is derived considering thermal limitations.

To make the comparison between different topologies and switch types possible, it is necessary to consider the maximum junction temperature relation to the switching frequency. In this work, a new modulation method is proposed to improve the performance of three-level converters considering losses and thermal performance. Also, a thermal model is derived for SiC MOSFET power modules that takes the effect of MOSFET channel conduction into consideration.

Losses for different modulation methods is analysed and compared for two-level and three-level converters. For a specific application of drives, low speed operation is investigated and the comparison between three-level and two-level converters is considered. The methods for calculating losses are considered carefully to ensure maximizing the utilization of the power semiconductors (for highest power density designs). A novel modulation method is developed for low speed operation of power converters.

Finally, an optimization is done for finding minimum volume, highest efficiency, minimum common mode pulses and complying with EMI constraints. This optimization has been broken into multiple steps for reducing the problem size. This will enable us to validate the results more efficiently. Some parts of this optimization are done automatically such as the inductor magnetic and thermal design.

To my brother Ghassem who inspired me to be an engineer and to my husband Gheisar for his unconditional encouragement and support.

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Chapter 1

Identification of the Problem

In this chapter, the potential applications and research motivation is introduced at first. Then the research objectives and goals are identified followed by the dissertation outline and the scope of the research. The advantages and design challenges are identified for the neutral point clamped (NPC) and SiC converter for a wide range of applications.

1.0.1 Research Application

With the emergence of new semiconductor materials, switching at high frequencies is going to be possible. However, switching at high frequency can result in different problems. Three-level converters can provide the option to switch at lower frequencies and still use the benefits of high switching frequencies. Active front end (AFE) application can be an example of using high switching frequency to achieve higher power quality. Grid-side filter sizes can be reduced significantly with high switching frequency. This can play an important role in motor drive application where there is a limitation for size and weight. In summary, two-level SiC converters and three-level Si converters are the options that can result in lower size low voltage AFE drives.

1.0.2 Research Motivations

The focus of this dissertation is on the comparison of the two-level SiC converters and three-level Si converters. The comparison between two-level and three-level converters with Si modules has been done previously in [2, 3] but the comparison between three-level Si converters and two-level converters SiC has not been done yet.

The research target is NPC three-level converters and two-level SiC converters. All of this topologies have been studied before but there are some reasons for choosing them as a target. First, no general comparison has been done between these converters for AFE application. Second, three-level topologies have other benefits such as common mode voltage that must be compared with SiC or hybrid two-level converters (A SiC IGBT is paralleled with a Si module). In this work, a Si 600 V module is used to implement an NPC converter.

The research motivations can be classified as follow:

- Providing a platform for finding an optimal converter design regarding efficiency, size and weight
- Assessing available technologies and topologies for active front end applications
- Deriving methods of designing filters for grid connected converters

- Analysing benefits of SiC converters in different applications
- Investigation of mulit-level converter benefits in special applications

1.0.3 Research Objectives

This dissertation focuses on low voltage three-level and two-level converters. However, the method used for this comparison can be used for any topology and switch technology. Therefore this comparison sets up a method that enable us to look at new core structures, semiconductor advancements and magentic design. Fig. 1-1 shows the flow chart of this modeling and optimization.

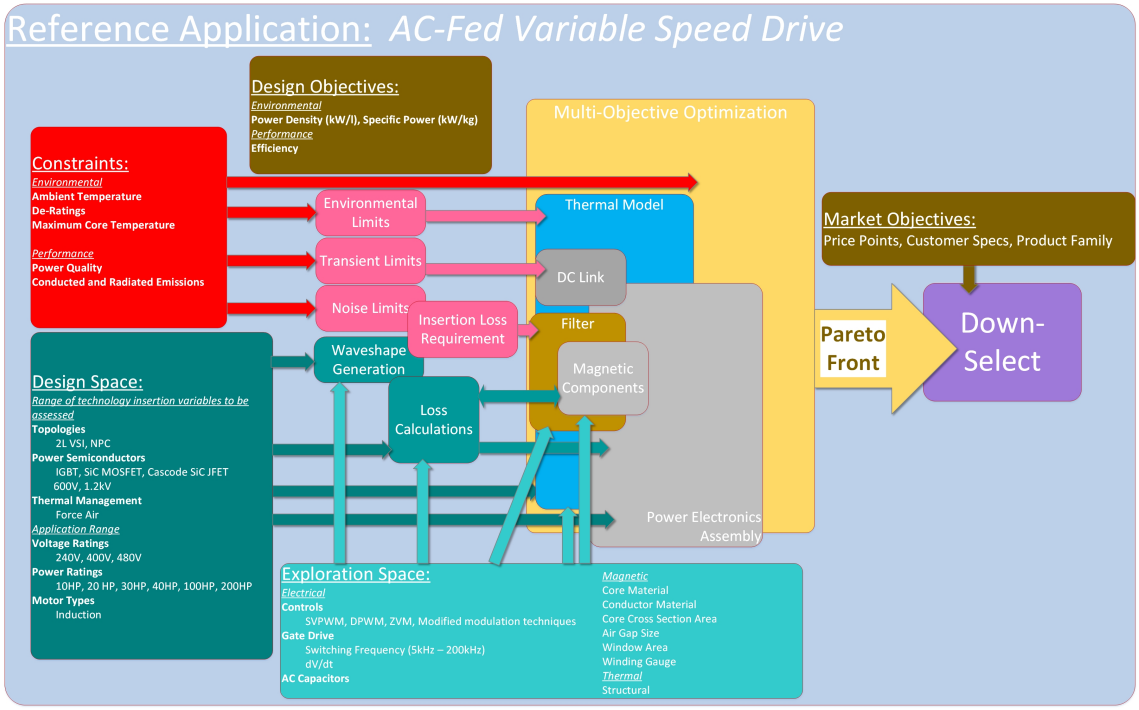

Figure 1-1: The procedure for finding the optimal converter design

The main application is active front end; however, special problems in inverter application is analyzed too. A deterministic optimization is be performed with the objective functions of volume and efficiency. This can provide a path for a generic optimization algorithm to find the proper converter for any application. The two basic comparison areas that are losses and magnetic sizes is investigated to find the optimal design. Two converters with the rating of 480 V and 20 hp are built to verify the methods of loss calculation, filter design and EMC analysis. These converters are a three-level NPC converter and a two-level SiC converter.

1.0.4 Dissertation Outlines

In chapter 1, a thorough survey and literature review of the multilevel converter topology and modulation techniques is given. The applications and motivations for the research are discussed then. The last part of this chapter identifies the research objective and challenges.

In chapter 2, the design of an LCL filter is discussed. LCL filters are used to comply with grid requirements. The design introduced in chapter 2 is aimed for integration to a generic optimization

algorithm. The thermal calculations inside the inductor is performed to find the optimal filter size where the interaction between capacitors and inductors is considered as well.

Loss calculation is performed in chapter 3 where closed form expressions for sinusoidal PWM of three-level converters are derived and different modulation methods performance in decreasing losses, balancing neutral point voltage and reducing THD are compared. A thermal model is derived for SiC MOSFET power modules to predict the junction temperature in the two-level converter.

In chapter 4, low speed operation of drives and the application of three-level converters is investigated. Details about the performance comparison of two-level and three-level converters is provided. In chapter 6, details about the implementation of converters and test results are provided and chapter 7 includes the summary and future work.

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Chapter 2

Introduction

This chapter presents the motivations and objectives of my research work. A literature review of the three-level topologies, SiC two-level converters and representative applications are given. The advantages and design challenges are identified for the neutral point clamped (NPC) and SiC converter for a wide range of applications. The structure and specifications for the research target are provided.

2.1 Research Background

With SiC based power modules that inherently exhibit low switching losses, high PWM switching frequencies can be obtained. Some promising applications include high fundamental frequency motor drives (high speed turbo-compressors, permanent magnet motor drives [4], filter size reduction (LCL filter for active rectifier) and audible noise reduction. Although the possibility of switching SiC devices at high switching frequencies results in a smaller size converter, the disadvantages of these modules should not be neglected. Presently SiC modules are less robust than commercially available IGBT devices for short-circuit performance although the thermal performance of SiC based devices is superior over Si IGBT. Also as SiC power devices have significantly faster rise and fall times, it presents EMC challenges for compliance with regulatory standards. Another concern in using SiC-MOSFET's is the reflected wave transient voltage at the motor terminals due to long cable effects at higher switching frequencies. So far, various aspects of SiC modules have been discussed with respect to IGBT's. However, a generic study comparing SiC two-level converters and IGBT three-level converters is missing. In this work, mathematical optimization is performed to find the best topology for a converter with specified ratings.

2.2 Review of two-level converters with SiC

Owing to recent progress in growth and device technologies of wide bandgap semiconductors, these materials are now realistic candidates for advanced power devices that outperform Si-based devices. Silicon-carbide (SiC) is a IV-IV compound material with unique physical and chemical properties. The strong chemical bonding between Si and C atoms gives this material very high hardness, chemical inertness, and high thermal conductivity. As a semiconductor, SiC exhibits a wide bandgap, high critical electric field strength, and high saturation drift velocity. Both n-type and p-type control across a wide doping range is relativity easy in SiC; this makes SiC exceptional among wide bandgap semiconductors. The ability of SiC to form silicon dioxide as a native oxide is an important

advantage for device fabrication [5]. Because of these properties, SiC is a promising semiconductor for high-power and high-temperature electronics. Silicon carbide (SiC) is especially attractive for high-voltage and high-current applications because of the availability of large-diameter wafers, which enables fabrication of vertical power devices with a large chip size [6]. Other advantages of SiC include p- and n-type doping control in a wide range by either in-situ doping during growth or ion implantation, availability of a native oxide, relatively long carrier lifetimes due to its indirect band structure [7]. Since the first production of SiC Schottky barrier diodes in 2001 and that of SiC power MOSFETs in 2010, the market of SiC unipolar power devices (mainly 1 kV class) has gradually been growing, demonstrating remarkable energy efficiency in real electronic systems [6].

Some promising applications include high fundamental frequency motor drives (high speed turbo-compressors, permanent magnet motor drives, filter size reduction (LCL filter for active rectifier) and audible noise reduction.

In the area of natural gas industry, there is a large interest in converters for driving high speed, medium voltage induction motors. High-speed drive systems are capable of directly driving turbo-compressors at speeds of up to 20,000 rpm / 8 MW. In high speed motor drive applications, the motor fundamental frequency can vary from 100 Hz to 300 Hz, which requires a high switching frequency. However, switching losses increase with switching frequency and these losses represent a critical point for high voltage semiconductors [8]. SiC modules with low switching losses can provide an alternate option for building these converters.

In [4], a SiC three-phase inverter is switched at 50 to 100 kHz where the motor speed can go to 1200 rpm which conventionally could go up to 500 rpm. The potential of using wide-band-gap devices in high-speed drives such as electric turbochargers is investigated in [9]. Focusing on the disadvantages of using SiC, one can mention poor capability of short circuit handling, EMC issues and reflected wave overvoltage at motor terminals. There have been reports showing that the short-circuit capability of SiC MOSFETs is lower than that of the Si IGBTs. The IGBT datasheets typically specify short-circuit capability of 10 μs for 1000 short-circuits with 1 second gap between the consecutive events [10]. Based on the results reported in [11, 12], short-circuit withstand of the SiC devices is around 4 μs to 8 μs, depending on the test voltage. It is also shown that a faster protection mechanism on the gate driver can compensate for this lower short-circuit capability [13, 14]. Driver circuit modification for the usage of De-Sat protection is investigated in [15] where driver circuit needs to be optimized to make sure that the total response time of desat protection is short enough to protect SiC MOSFETs. It should be noted that the desaturation protection technique requires certain blanking time which delays the detection of the short circuit phenomenon. This inherent delay in the desaturation method can potentially lead to failure of the device and the Gate Oxide layer of the SiC MOSFET in particular. Another drawback of desat protection is that the overcurrent level cannot be set accurately as overcurrent is detected by measuring V_{ds} and not the drain current (id). The desat protection method is thus of limited application as the SiC MOSFETs have very little endurance against short circuit faults.

A lot of effort is carried out to emulate shunt resistor (R_{sh}) based current measurement in SiC MOSFET modules [16]. The methods reported in literature use another MOSFET that is fabricated on the same die as the SiC MOSFET and a sensing resistor is suitably placed. However, the overall cost of the solution increases.

There is a set of di/dt based protection techniques for IGBTs which have been adopted for SiC MOSFET [17]. The two prominent di/dt sensing based short circuit protection techniques are the Kelvin voltage sensing based short circuit protection technique and the Rogowski coil based short circuit protection technique.

Kelvin voltage based short circuit protection technique is widely adopted for IGBTs. A similar approach for SiC MOSFETs is reported in [18]. In this technique, the Kelvin voltage is integrated

for detecting the fault. One drawback of this method is the difficulty of measuring the low voltage drop on the Kelvin source in an environment where high voltage switching occurs. High common mode voltage can affect the measurement results [19].

A Rogowski coil based short circuit protection technique is reported in [20] and is very similar to the Kelvin voltage method of [13]. The voltage induced in the Rogowski coil is used to estimate the di/dt of the SiC MOSFET and id is derived using an integrator. However, it's application requires a very careful design of the Rogowski coil and an additional PCB to be mounted on the SiC Module which increases the cost and complexity of the entire solution [13].

Both the di/dt methods discussed above suffer from a problem that they cannot quickly detect faults occurring when the SiC MOSFET is turned-ON [18] commonly known as Fault Under Load (FUL). This drawback is due to the fact that the output of the integrator falls during the ON-state of the MOSFET as the di/dt falls to a very small value [21].

The factors impacting the short circuit capability of in the design of multi-chip modules are reported in [22] which can provide a guideline in comparing different modules. Ongoing research includes manufacturing SiC modules with better short circuit handling capability [23, 24].

High switching frequency can result in high dv/dt and di/dt and therefore high conducted and radiated electromagnetic emissions. This can defeat the purpose of using high switching frequency for smaller filters. For compatibility with EMC standards, in SiC inverters it might be necessary to use bigger EMC filters due to the high switching frequency. EMC measurements are done in [19] which shows the compatibility issues of SiC inverters with high switching frequency. An analytical model is developed to predict the EMC issues [25] for a specific inverter with impedance measurements. An optimization technique is used to match the EMC measurement and simulation results in [26]. It should be noted that it is necessary to avoid EMC issues by designing the system with lower parasitic inductance and capacitance and dv/dt and di/dt consequently. Busbar design plays an important role in here [27].

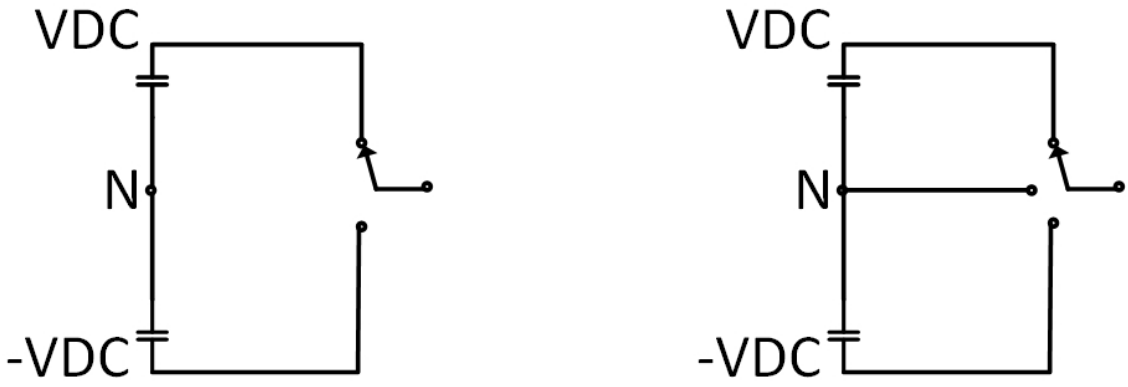
2.3 Review of three-level converters

Multi-level converters were basically developed to satisfy the need for high voltage and high current switches. These converters will remove the need to connect the devices in series or parallel [1]. Fig. 2-1 compares the circuit structure for two-level and three-level converters. output waveform for two-level and three-level converters are shown in Fig. 2-2. The two-level converter in Fig. 2-2(a) can only be connected to positive and negative voltage level. These two levels are modulated to generate the sinusoidal output voltage. On the other hand, the three-level converter in Fig. 2-2(b) can be connected to three levels of voltage positive, negative and neutral. Therefore, there are extra control freedoms to synthesize the output voltage. This makes the voltage quality better with lower harmonics. The lower steps in voltage value and therefore dv/dt makes the common mode noise lower and smaller size CM filters will be needed.

2.3.1 Review of Three-level Converter Topologies

Different types of three-level have been invented. These topologies are shown in Fig. 2-3. A chronological review of the topology for multilevel converters is presented in [28] including three-level converters. In this work, the focus will be on three-level converters.

Neutral Point Clamped (NPC), Active Neutral Point Clamped (ANPC) and Flying Capacitor (FC) topologies provide the opportunity to use low voltage rated components which is not necessary for low voltage drives application. However, T-type topology has less number of switches needed.



(a) Two-level converter circuit topology

(b) Three-level converter circuit topology

Figure 2-1: Comparison of circuit topology of two-level and three-level converter

Also T-type topology may have less conduction losses as on positive and negative rail there is only one switch involved but switching losses may be higher.

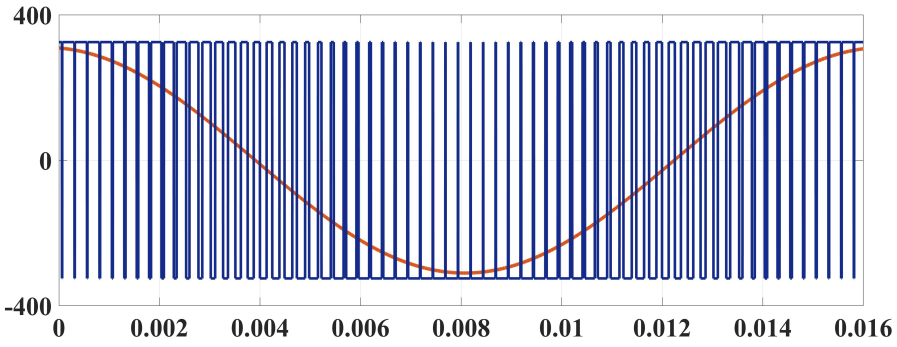
ANPC was first introduced in [29] to balance the losses between all the switches which will increase the power rating of a converter with the expense of adding extra active switches. FC topology has the least number of switches compared to other topologies but at high switching frequencies the required flying capacitor size increases. The flying capacitor size is proportional to the switching frequency. A through comparison including LCL filter size, flying capacitor size and losses between NPC and FC has been performed in [30].

Modular Multilevel Converter (MMC) is a subdivision of cascaded H-bridge topology [31]. MMCs are formed from series connection of submodules which can be full-bridge or half-bridge converters. MMC needs a high number of switches and also bulky capacitors as the DC, AC output and circulating current goes through the submodule capacitors. So not only it needs extra capacitors as submodule capacitors but also this capacitors can be quite bulky and therefore energy storage sizing in this type of converters can be quite challenging [32]. In summary, MMCs are not suitable for low voltage applications because of high number of switches and also bulky capacitors and inductors.

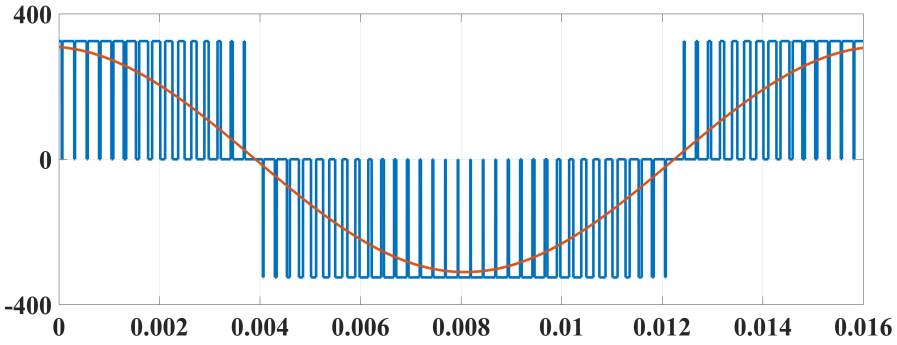
In this thesis, the focus has been on NPC and T-type topologies as they do not extra capacitors as submodule capacitors or flying capacitors and also they have the least number of needed switches. One of the important challenges in NPC and T-type converter design is balancing the neutral point voltage. This makes the control and modulation of these converters complicated [33].

2.3.2 Three-level Converter Modulation Strategies

The modulation strategies for NPC and T-type converter will be discussed in this section. Modulation methods can affect the system performance significantly. They can affect the losses, power quality and EMC issues. Modulation methods can be space vector based or carrier based. The space vector modulation is based on the three-phase system. Using alpha-beta transformation, the different switching states of a three-phase three-level converter can be mapped to the line-line voltage space and they form a space vector hexagon. The voltage reference vector can also be found using alpha-beta transformation. The reference voltage can be synthesized in different ways by

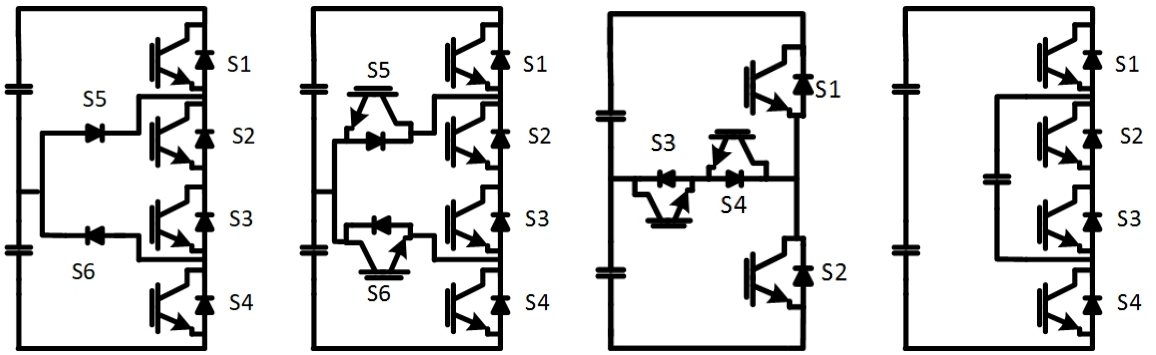


(a) Two-level converter output voltage



(b) Three-level converter output voltage

Figure 2-2: Comparison of output voltage in a two-level and three-level converter

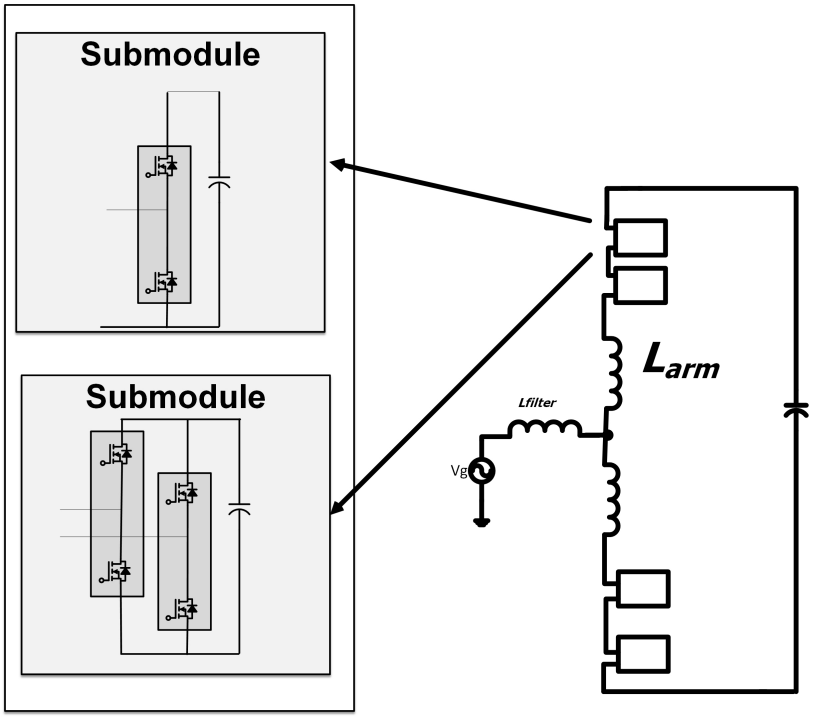


(a) Neutral point clamped (NPC) converter

(b) Active Neutral point clamped (ANPC) converter

(c) T-type converter

(d) Flying capacitor converter



(e) Modular multilevel converter. Submodules can be made from half-bridges or full-bridges

Figure 2-3: Different types of three-level converters

the switching states voltage vector. For a three-level converter, each phase leg has three switching states and the three-phase system has 27 switching states, which corresponds to 19 space vectors in the hexagon as shown in Fig. 2-4. The redundant switching states can be used to change the performance of the converter for different purposes. The number of redundant states are more than two-level converter but higher computation is needed to build the reference voltage.

The redundant states in short vector and small vector can be used for different objectives including neutral point (NP) voltage balance [34], switching loss reduction [35] or common-mode noise reduction [36]. Among these objectives, the neutral point voltage balance is vital to keep the converter working. With the DC voltage out of balance the output voltage will not match with the reference voltage and that will change the output current as well. Also this can harm the DC link

capacitors if overvoltage happens because of unbalanced voltage between the capacitors. Therefore neutral point balance should be the priority in any space vector modulation method. There are

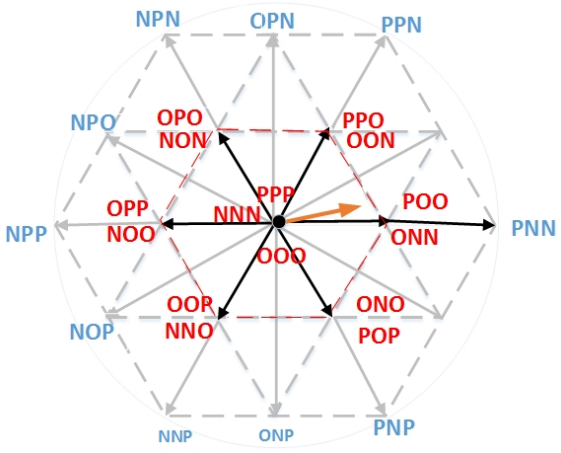
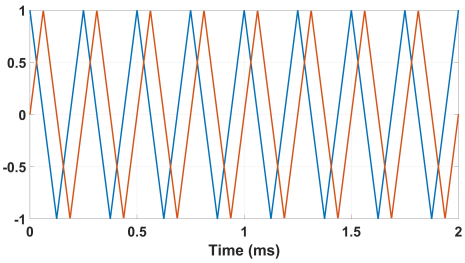


Figure 2-4: Space vector hexagon for the three-level converter

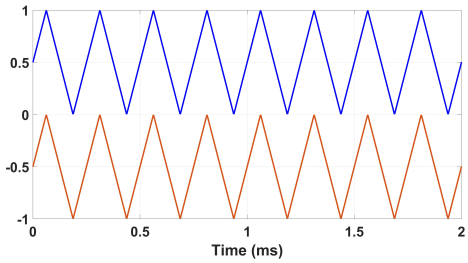
different coordinate systems for the vector space including orthogonal $\alpha - \beta$ and non-orthogonal g-h coordinate. Also, there are several sector division methods to synthesize the reference voltage and to calculate the duty cycle. The details about these methods are provided in [1]. In this work, because of more simplicity g-h coordinate with parallelogram sector division is used. A modulation method is introduced by [1] to balance the objectives of lower losses, CM voltage and neutral point voltage.

Carrier based modulation frequency is easy to implement and it can be applied to each leg separately. For low frequency modulation, staircase synthesis is used which can be further developed for selective harmonic elimination method [37]. However, this method is not suitable for three-level converter as it results in low power quality. For high frequency modulation, phase shifted and level shifted modulation methods are used.

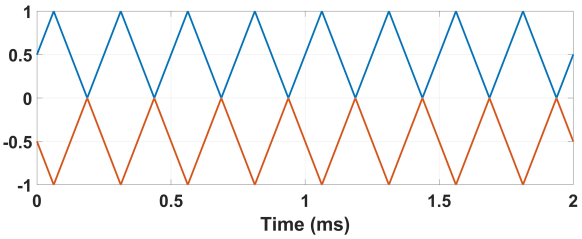
For the phase shifted modulation, the carrier for each voltage level has a phase shift with the other carriers. In three-level converter the two carriers are shifted 90 degree to each other as 2-5(a) shows. The output voltage will have three times higher switching frequency of each module and this will result in lower THD in output. Level shifted modulation is another modulation method in which the carrier waves shift their level with respect to the reference wave as shown in 2-5(b) and 2-5(c). Each of these modulation waveforms generate different switching pattern for each switch. From THD point of view, the level shifted modulation has higher THD than the phase shift modulation.



(a) Phase shifted modulation carriers for a three-level converter



(b) Level shifted modulation carriers for a three-level converter where the waveforms are in phase with each other



(c) Level shifted modulation carriers for a three-level converter

Figure 2-5: Three high frequency level shift modulation methods

2.3.3 Hybrid converters

Reference [38] presents a detailed comparison of the use of Si and SiC devices for a three-level T-type low voltage inverter. The comparison includes semiconductor losses as well. The use of 1200 V SiC with 600 V Si is suggested to be a cost effective option with high performance. SiC modules are mostly used in high-voltage three-level converters [39, 40]. An ANPC topology with 650 V SiC MOSFETs is made in [41]. In addition to SiC modules, GaN HEMTs are also included in [42]. Most of these comparisons between the usage of Si and SiC modules in three-level converters have been done only for losses and only in [38] filter design is also included although the comparison is only for two specific switch types and a more general comparison considering EMI issues is necessary yet. In [43] pareto optimization model is set for a hybrid SiC Ttype converter but the comparison is only done for output and input filters of a UPS.

2.3.4 Conclusions

Literature review was performed in this chapter. Different topologies and their application was discussed and at the end the focus of research was determined. NPC converters were selected as the primary topologies for three-level converters.

Chapter 3

Comparison of Three-level and Two-level Converter Sizes

3.1 LCL Filter Design

To interface a converter to the grid, it is necessary to use a filter. This filter is required to meet the grid standards. Filters can be quite bulky and massive for most of applications. In order to perform a general optimization, it is essential to consider the size of filters. This section investigates the harmonic filter design for AFE converters. Different topologies can be used for this filter. Different toplogical variations for the harmonic filters with complex structures have been analyzed in [44] and [1]. In this dissertation, the LCL filter is the chosen for the harmonic filter because of the best trade-off between attenuation and the component size.

In this section, the basic design guidelines will be reviewed and then the relation between filtering effects and size will be developed. This relation will be one module of the optimization of the converter. This chapter covers LCL filter design for both two-level and three-level converters.

3.1.1 Design guideline for LCL filter

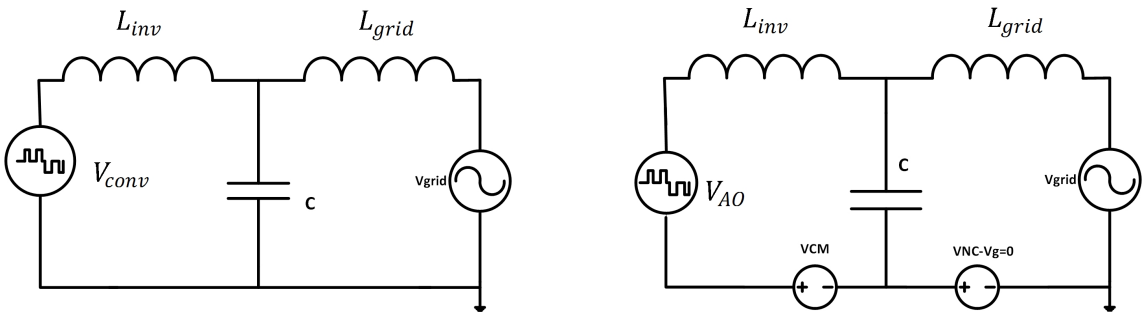
It is necessary to derive the equivalent circuit of the three-phase converter for the filter design and inductor current ripple analysis. Fig. 3-1(a) shows the equivalent circuit where the voltage source V_{AO} represents the converter output voltage of phase A and the voltage source V_g is the grid voltage. Considering common-mode voltage as (3.1), the converter output voltage of phase A can be found as (3.2) and the single-phase equivalent circuit will be similar to Fig.3-1(b).

$$V_{CM} = (V_{AO} + V_{BO} + V_{CO})/3 \tag{3.1}$$

$$V_{con_A} = V_{AO} - V_{CM} \tag{3.2}$$

The capacitor in LCL filter will have a small impedance compare to the grid-side inductance in high frequencies and therefore all the high frequency switching current of the converter will go through this capacitor and the fundamental frequency current will go through the grid-side inductance. Also, all of the converter current will go through the converter-side inductance. Therefore, the converter side inductor will be bigger compared to the grid side inductor.

The LCL filter is designed to meet specific goals. These goals are summarized in Fig. 3-2. A large capacitor will provide more high frequency ripple current sink, but it also consumes more



(a) Circuit representing the LCL filter

(b) single phase equivalent circuit

Figure 3-1: Modeling of the LCL fiter

reactive power at line frequency and shifts the power factor at grid side [1]. The limit for reactive power consumption is 2 to 5 percent of the total power rating. Then the maximum capacitance can be calculated as (3.3) with P_{out} the rated power for the converter and V_{ph} the line to neutral output voltage.

The other limitation on the design of LCL filters is the voltage drop on the inductors. For the AFE application, the converter is either working as an inverter or a rectifier with the power factor close to unity. To limit the voltage drop to 10 %, the converter voltage will be limited as $V_{conv} \leq 1.1\, V_G$. Therefore, the inductances will be limited as (3.4).

Standards for harmonic current of grid-side inductance
- Limited current harmonic content

THD requirements
- THD of grid side current must be less than 5%

Power factor on the grid side
- It is preferred to limit the reactive power consumption

Voltage drop on the inductor
- The voltage drop on the inductor should be limited to use the lowest possible DC voltage.

Resonant frequency limitation
- The filter should not resonate with the switching harmonics and line frequency voltage of converter

Figure 3-2: The requirements for the filter design

$$Q_c = V_{ph}^2\, \omega_{line}\, C \leq 0.02\, (\frac{S_N}{3}) \tag{3.3}$$

$$L_{conv} + L_{grid} \leq \frac{\sqrt{(1.1^2 - 1)}}{w_{line} I_g} \tag{3.4}$$

In [1], the converter side inductance is found for a limited ripple current. The ripple current will make more losses inside the inductor and therefore the higher the ripple current the bulkier inductance will be. On the other hand, for limiting the ripple current an inductor with a higher inductance value should be selected which is more bulky and expensive. So there is a trade-off between the

current ripple and inductance value. The analytical relation between converter current ripple and converter side inductance can be found as (3.5) for a three-level converter [1] and as (3.6) for a two-level converter [45].

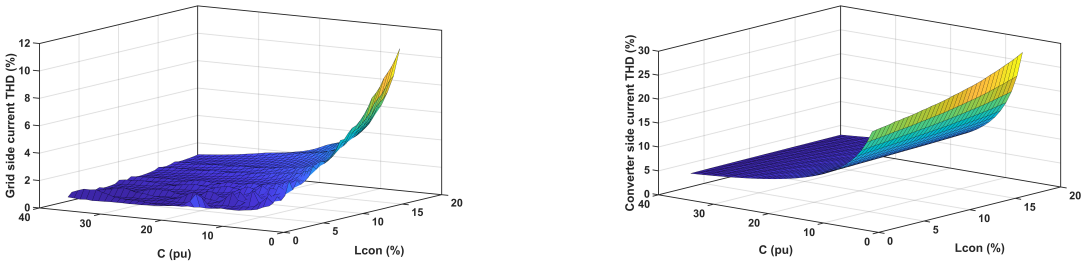
$$\Delta I_{max} \approx \frac{V_{DC}}{12\, L_c\, f_{PWM}} \tag{3.5}$$

$$\Delta I_{max} \approx \frac{\sqrt{3}}{12} \frac{V_{DC}}{f_{PWM} L_c} m_a \tag{3.6}$$

The capacitor can be found for a limited grid current THD value. The value of the inductor can also be adjusted for the limited THD value. Grid side current THD is dependent on both inductor and capacitor value but the current ripple is more dependent on the inductance value. Fig. 3-3 shows the effect of inductance and capacitor value for the converter ratings of Table 3.1.

Table 3.1: Sample case converter ratings

Nominal power (hp)	25
Output RMS current (A)	22
Grid frequency (Hz)	60
Power factor	1
Grid voltage (V)	480
DC voltage (V)	750
Grid inductance (%)	0.306
Modulation method	Space Vector Modulation



(a) Grid side THD

(b) Converter side THD

Figure 3-3: THD value of grid side and coverter side current for different values of inductors and capacitors and switching frequency of 4 kHz

The capacitance is limited by reactive power consumption as well. The grid side inductance is found for the compliance with the grid standards for high frequencies. The grid side inductance will change the grid side current spectrum. Table 3.2 shows the standard limits [1]. The voltage

Table 3.2: IEEE 519 and 1547 standard for harmonic current of grid-tied converter

harmonic order	$\leq 11^{th}$	11-17^{th}	17-23^{rd}	23-35^{th}	$> 35^{th}$	THD
Limit(%)	$< 4\%$	$< 2\%$	$< 1.5\%$	$< 0.6\%$	$< 0.3\%$	$< 5\%$

drop limitation and resonant frequency are the factors for determining the grid side inductane. Pas-

sive damping can be designed as the last step where an RLC branch is placed in parallel with the capacitive branch to dampen the resonant frequency harmonic content or the switching frequency harmonic content of the grid side current.

In [45], the procedure starts with finding the inductor for a limited current ripple using (3.6). Then the capacitance is found for a limited voltage ripple with an analytical expression. The damping branch is designed at this stage for a limited damping value for the transfer function of grid current to the converter voltage ($\frac{i_g}{v_{conv}}$). The grid side inductance is derived for a limited grid ripple current.

In [46], the procedure is finding the converter side inductance for a limited current ripple (r_i). And then the capacitor is found for the voltage ripple. The voltage ripple is defined as the ratio of the capacitor switching voltage to the fundamental component of capacitor voltage $r_v = \frac{V_{c,sw}}{V_{c,1}}$. The grid-side inductance is derived for the ratio of switching frequency component of the grid side current to the converter current at fundamental frequency as $r_g = \frac{I_{g,sw}}{I_{g,1}}$ assuming $I_{g,1} = I_{i,1}$. With the total inductance being limited to 10% of the base inductance value, one of the variables of r_i, r_g and r_v will be dependent on the other two.

The method used in [47], similarly starts from finding the inductance for a limited converter side current ripple. Then the filtering effect is calculated as $\frac{Ig}{V_{conv}}$ for different values of capacitor and grid side inductance. Considering the limitation in reactive power usage and resonant frequency, the optimal values of the L_g and C are selected with a trial and error selection.

In [48], the current transfer function is defined as $\frac{I_g}{I_i}$ and the design is based on having enough attenuation in this transfer function at switching frequency. The other constraints such as reactive power consumption, resonant frequency and voltage drop are taken into consideration. Damping resistance is placed in series with the capacitor and the value of this resistor is selected to be one third of the impedance of the filter capacitance at the resonant frequency.

The LCL filter design algorithm of [1] is shown in Fig. 3-4 where the converter side inductance and capacitance are found for limitation of converter side current ripple and grid side current THD. Grid side inductance is assumed to be equal to a specific starting point. Then the grid side inductance is found for medium frequency range of current spectrum standards and at the end the resonant frequency is checked to be within the limits. The problem with this method and all the other types of iterative optimal filter methods is that a specific range of possible values along with a step size is considered whereas because of the inherent non-linearity nature of resonant frequency and THD values the optimal values might be missed between the step sizes.

In this work, sweeping through a range of possible values and a new mathematical modeling and optimization are chosen as methods of finding optimal LCL values. Instead of using the current ripple as a limitation, current THD in converter side inductance has been limited because losses are directly dependent on harmonic content rather than ripple current. Converter side and grid side current THD values have been limited to 7% and 2.5%. The other limitation is that the resonant frequency ($f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_g+L_{con}}{L_{con}\,L_g\,C_f}}$) must be between grid frequency f_g and $\frac{fPWM}{2}$. Table 3.3 summarizes the constraints considered in this work for finding the optimal filter design values. Other limitations such as reactive power consumption and voltage drop can also be added to the constraints but they are not considered in our algorithm.

A time based simulation has been used for finding the THD values in each combination of inductors and capacitors. The range of possible values of LCL elements can be around the engineering rule of thumb points. The rule of thumb in industry for designing LCL filers is 10% inductor on the converter side, 20 pu capacitor and 3% inductor on the grid side for 4 kHz of switching frequency. Here, these values are linearly changed to fit other switching frequencies. The minimum and maximum value of these elements are selected to be one third and twice of the initial point.

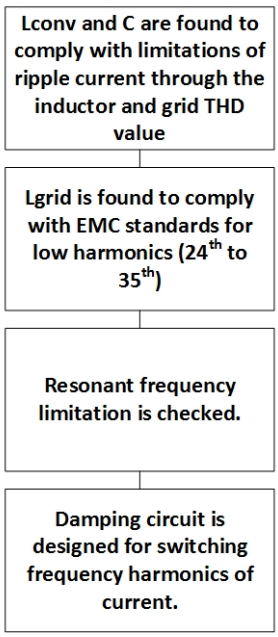


Figure 3-4: Algorithm used in [1] for designing LCL filters

Table 3.3: Allowable range of parameters in sweeping through all the possible values of inductors and capacitors

Parameter	Allowed Minimum Value	Allowed Maximum Value
Grid current THD (%)	0	2.5
Converter current THD (%)	0	7
Resonant frequency	$10 * f_g$	$\frac{fPWM}{2}$
Converter side inductance (%)	$\frac{10*4000}{3*fPWM}$	$\frac{2*10*4000}{fPWM}$
Grid side inductance (%)	$\frac{3*4000}{3*fPWM}$	$\frac{2*3*4000}{fPWM}$
Capacitor (pu)	$\frac{20*fPWM}{4000*3}$	$\frac{2*20*fPWM}{4000}$

Table 3.4 shows the results for sweeping through the LCL values for the switching of 4 kHz. Based on the inductor design and available capacitors in the market, the design with lowest size, weight and cost can be selected.

Although sweeping through the possible values can give insight about the appropriate choices for LCL elements, it does not necessarily results in the optimal design. Sweeping through the possible values of LCL elements can be done with an infinite steps of LCL values. However, the objective and constraint functions such as resonant frequency and THD values are nonlinear function and the optimal points can lay between the loop steps. A heuristic algorithm can be used to find the optimal values of LCL elements. Running an optimization algorithm with a time based simulation can be very time consuming. Therefore it is necessary to derive closed form functions for the constraints and objectives.

Considering the main component of converter voltage to be the angle reference, the grid voltage will have the angle of θ. Therefore the grid side current must have an angle close to θ to ensure unity power factor. The variable θ has a closed form expression that relates it to the L_{conv}, L_{grid},

Table 3.4: Some of LCL design results for a two-level converter with 4 kHz switching frequency and ratings of Table 3.1 from sweeping through values close to conventional method of LCL filter design

L_{grid} (%)	C (pu)	L_{con}(%)	fres (kHz)	THD I_{conv} (%)	THD I_{grid} (%)	Rdamp (Ω)
1.00	6.67	10.00	1.47	5.85	0.82	0.06
2.00	13.33	10.00	1.62	6.03	1.18	0.13
3.00	13.33	10.00	1.40	6.04	0.73	0.13
4.00	13.33	10.00	1.27	6.04	0.65	0.13
5.00	20.00	10.00	1.98	6.17	1.67	0.19
2.00	20.00	10.00	1.71	6.16	1.31	0.19
3.00	20.00	10.00	1.55	6.16	0.81	0.19
4.00	20.00	10.00	1.45	6.15	0.61	0.19
5.00	20.00	10.00	1.37	6.18	0.86	0.19
6.00	20.00	10.00	1.98	6.29	1.58	0.25

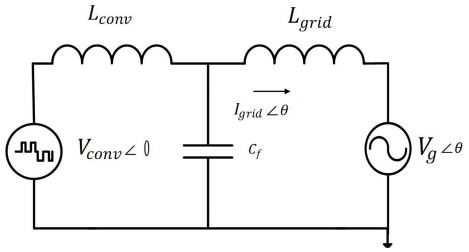


Figure 3-5: The equivalent circuit for finding θ

C_f and R_{damp}. Fig. 3-5 shows the equivalent circuit for finding the closed form expression for θ and V_{CONV}. Grid voltage is equal to $\sqrt{2/3}\,V_g\,cos(2\,\pi\,f_{grid}+\theta)$. For a given LCL set of values, the modulation index can be found from the main component of converter voltage (V_{CONV}). The spectrum of two-level converter voltage includes two main ranges of harmonics: harmonics around switching frequency and double switching frequency. The contributing harmonics to the THD values of grid side and converter side currents are these two ranges of harmonics and the resonant frequency. The resonant frequency can cause high harmonic currents contributing to THD value of grid side and converter side current. Here the converter voltage spectrum is searched for the harmonics close to the resonant frequency and the maximum value of this voltage is used to find the resonant frequency current value of grid-side and converter-side current ($I_{g,f_{res}}$) and ($I_{con,f_{res}}$). THD value of grid side and converter side current can be found as (3.8). Fig. 3-6 shows the process for checking the LCL values given by a heuristic algorithm versus the design constraints. The objective function can be weight, volume and cost of the LCL filter. As we do not have an analytical method to evaluate the inductor size and cost from a given set of parameters, the objective function in this chapter is set as the value of the converter side inductor as (3.1.1) shows. However, in the next section, this analytical function will be derived and a more detailed optimization can be done.

$$I_{ripple} = \frac{I_{rms}^2 - I_1^2}{I_{nom}} \tag{3.7}$$

Table 3.5: LCL optimal values found from Genetic Algorithm for the ratings of Table 3.1 in a two level converter

f_{PWM} (kHz)	L_{grid} (%)	C (pu)	L_{con}(%)	fres (kHz)	THD I_{conv}(%)	THD I_{grid} (%)	Rdamp (Ω)
4	1.89	10	8.85	1.43	6.75	0.80	0.24
6	1.62	15	5.96	1.92	6.74	1.14	0.21
8	2.85	20	4.49	1.97	6.66	0.35	0.33
10	2.35	25	3.60	2.44	6.65	0.42	0.23
12	0.37	30	3.01	4.43	6.68	1.17	0.11
14	1.71	35	2.58	3.35	6.61	0.25	0.35
16	0.95	40	2.26	4.22	6.62	0.48	0.17
18	0.49	45	2.01	5.32	6.61	0.42	0.14
20	1.02	56	1.81	5.18	6.60	0.35	0.06
22	0.71	55	1.65	5.62	6.60	0.40	0.15
24	0.77	67	1.51	6.21	6.61	0.61	0.06
26	0.37	65	1.39	7.17	6.60	0.45	0.15
28	0.75	70	1.29	6.59	6.60	0.32	0.13
30	0.18	75	1.21	8.84	6.62	0.58	0.06
32	0.32	80	1.13	8.50	6.60	0.54	0.22

$$THD_{i_g} = \frac{\sqrt{2{I_{g,sw}}^2 + 2{I_{g,f_{2sw}}}^2 + 2{I_{g,f_{res}}}^2}}{I_{g,1}}$$
$$THD_{i_{con}} = \frac{\sqrt{2{I_{con,sw}}^2 + 2{I_{con,f_{2sw}}}^2 + 2{I_{con,f_{res}}}^2}}{I_{con,1}} \tag{3.8}$$

$$Minimize\, L_{con}$$
$$such\ that \begin{cases} THD_{i_g} < 0.05 \\ THD_{i_{con}} < 0.07 \\ 10\, f_{out} < f_{res} < f_{PWM}/2 \\ C_f < C_{max} \end{cases}$$

Because all the harmonic current goes through the converter side inductor, the size of this inductor determines the total size of the LCL filter. The maximum value for the grid side inductance and filter capacitor (Table 3.3) will avoid the unreasonable values for these two parameters.

Table 3.5 shows the values found from Genetic algorithm with the limitations of Table 3.3. As an example, for 4 kHz, the optimization algorithm gives a smaller value for the converter side inductance which we assumed is the prominent factor of the LCL filter size and cost.

The results found so far are derived only for the requirements of THD in the grid side current and the current spectrum requirements of the standards were ignored. The grid side inductance current spectrum should be checked for compliance with standards. IEEE 519 standard requires limitations on the current spectrum values. For complying with grid standards, it is necessary to consider the standards related to the current spectrum. Fig. 3-7 shows the spectrum of current for 10 % of grid

side inductance, 6.58 pu capacitance and 1% grid side inductance. It can be seen in this picture that the current spectrum does not meet the requirements at 4 kHz.

If we consider the objective of complying with grid standards of current spectrum the options will be very limited in an LCL filter design. Table 3.6 shows the possible LCL filter values with constraint of standards grid current spectrum for 4 kHz found by sweeping through possible values.

Table 3.6: Possible LCL values for switching frequency of 4 kHz and the ratings of Table 3.1 to comply with grid current standards in a two level converter

L_{grid} (%)	C (pu)	L_{con}(%)	fres (kHz)	THD I_{conv} (%)	THD I_{grid} (%)	Rdamp (Ω)
5	13.16	10.00	1.2	6.05	0.46	0.12
4	13.16	13.33	1.2	4.51	0.55	0.12
6	19.14	13.33	1.3	4.59	0.44	0.18
3	13.16	16.67	1.3	3.60	0.46	0.12
4	13.16	16.67	1.2	3.60	0.35	0.12
5	19.14	16.67	1.3	3.66	0.53	0.18
6	19.14	16.67	1.3	3.67	0.45	0.18
1	6.58	20.00	1.4	2.91	0.42	0.06
3	13.16	20.00	1.3	3.00	0.36	0.12
4	13.16	20.00	1.2	3.00	0.30	0.12
4	19.14	20.00	1.4	3.04	0.38	0.18
5	19.14	20.00	1.3	3.05	0.35	0.18
6	19.14	20.00	1.2	3.06	0.50	0.18
6	26.32	20.00	1.4	3.09	0.36	0.25
4	19.14	20.00	1.4	3.04	0.38	0.18
5	19.14	20.00	1.3	3.05	0.35	0.18
6	19.14	20.00	1.2	3.06	0.50	0.18
6	26.32	20.00	1.4	3.09	0.36	0.25

Comparison of Table 3.6 and Table 3.4 results shows that with this requirement, a bigger capacitor and grid side inductance will be required. Using the mathematical modeling and optimization algorithm with the goal of minimum converter side inductance, LCL values of Table 3.7 can be found. The converter side inductance value is equal to the results without considering grid side current spectrum. However, the capacitor, grid side inductance and damping resistance are bigger compared to Table 3.5. The other option can be using an extra damping branch to help to comply with grid standards while the optimal LCL filter is used. A trap filter can be set to damp the switching frequency current as shown in Fig. 3-8. Required LCL and damping branch values for different frequencies is presented at Table 3.8. The capacitor value is designed to have the resonant frequency of the damping branch equal to the switching frequency. These results are very dependent on the transformer and grid inductance values. For a stronger grid with higher amount of grid inductance there might be no need to use a trap filter. To compare the size of the LCL filter with and without a damping branch, an alogrithm for designing inductors is necessary. Because the inductor in the damping branch only passes the current of specific frequencies, there will be less losses inside this inductor and a smaller inductor will be required. Therefore adding a damping branch parallel with the filter capacitor might not increase the filter size significantly.

Table 3.7: LCL optimal values found from Genetic Algorithm for the ratings of Table 3.1 considering the compliance with current spectrum

f_{PWM} (kHz)	L_{grid} (%)	C (pu)	L_{con}(%)	fres (kHz)	THD I_{conv}(%)	THD I_{grid} (%)	Rdamp (Ω)
4	3.61	10.00	8.56	1.16	0.60	7.00	0.09
6	3.74	15.04	5.71	1.51	0.32	7.00	0.07
8	1.33	39.48	4.39	3.45	1.13	7.00	0.11
10	2.10	37.33	3.46	3.08	0.44	7.00	0.38
12	1.97	30.02	2.85	2.92	0.25	7.00	0.38
14	1.40	51.35	2.47	4.28	0.42	7.00	0.11
16	0.84	55.44	2.16	5.17	0.50	7.00	0.15
18	1.16	47.00	1.90	4.52	0.25	7.00	0.35
20	0.95	58.60	1.72	5.39	0.34	7.00	0.29
22	0.25	82.39	1.59	8.49	1.27	7.00	0.16
24	0.99	81.21	1.44	6.55	0.38	7.00	0.30
24	0.59	73.15	1.32	7.02	0.43	7.00	0.10
26	0.15	133.57	1.25	12.04	1.04	7.00	0.32
28	0.77	105.48	1.15	8.26	0.53	7.00	0.30
30	0.16	128.12	1.09	11.85	0.80	7.00	0.38

Table 3.8: LCL and damping branch values for different switching frequencies and the ratings of Table 3.1 in a two level converter

f_{PWM} (kHz)	L_{grid} (%)	C (pu)	L_{con}(%)	Rdamp (Ω)	C_{trap} (μ F)	R_{trap} (Ω)
4	1.15	10.00	8.23	0.30	5.08	0.17
6	1.10	20.44	5.62	0.04	3.65	0.37
8	1.32	20.00	4.18	0.17	10.29	0.23
10	1.08	25.00	3.36	0.22	1.66	0.18
12	1.44	30.00	2.80	0.32	4.56	0.05
14	0.25	35.00	2.41	0.19	1.74	0.20
16	0.46	40.00	2.11	0.24	5.00	0.22
18	1.28	82.15	1.92	0.34	4.67	0.07
20	0.27	50.00	1.69	0.07	4.19	0.33
22	0.69	55.00	1.54	0.36	1.46	0.31
24	0.51	60.48	1.41	0.02	1.79	0.36
26	0.55	120.55	1.33	0.20	0.61	0.11
28	0.64	70.00	1.21	0.25	2.06	0.37
30	0.29	75.00	1.13	0.11	0.77	0.35
32	0.29	80.00	1.06	0.13	0.96	0.18

3.1.2 LCL Filter Design for three level converters

The optimal LCL filter for a three level converter is different with a two level converter with the same rating. The difference between the spectrum of a two-level converter and a three-level converter will result in a different design. The voltage spectrum of a two level and a three level converter for 4 kHz switching frequency, ratings of Table 3.1 and with modulation index of 1 is shown in Fig. 3-9. The dominant harmonics for the three-level converter are around 8 kHz versus 4 kHz for the two level converter. Modulation methods with neutral point balancing and loss reduction have different spectrums. Steady state neutral point imbalance in converters with small DC link capacitors can disturb the output voltage of converter. Details about comparison of different modulation methods will be provided in subsection 4.2.3.

Sweeping through the possible practical values of inductors and capacitors with the limitations of Table 3.1 results in a big variety of design options. Using an optimization algorithm the possible optimal LCL values are shown in tableTable 3.9. Fig. 3-10 compares the minimum converter side inductance values found by the optimization algorithm with a corresponding two-level converter. It can be seen that the inductor value of three-level converters are 2/3 of corresponding two-level converter. Two-level SiC converter needs a 0.2% converter side inductance at 18 kHz but a three-level converter can work at 8 kHz with the same filter size as a 18 kHz SiC converter. This shows that three-level converters can be a good substitute for SiC two-level converters for the goal of lowering filter size. It is worth mentioning that these values are found for having the lowest amount of converter-side inductance. However, a design with lower size of capacitor may result in a total smaller size.

Table 3.9: Optimization results for finding the minimum converter side inductance for the ratings of Table 3.1 in a three level converter

f_{PWM} (kHz)	L_{grid} (%)	C (pu)	$L_{con}(\%)$	fres (kHz)	THD $I_{conv}(\%)$	THD $I_{grid}(\%)$	Rdamp (Ω)
4	3.58	13.32	3.33	1.64	8.22	1.76	0.23
6	2.17	28.32	2.22	2.97	8.63	2.71	0.16
8	1.34	28.21	1.67	3.53	8.02	1.44	0.21
10	0.68	31.30	1.33	4.53	7.90	1.22	0.38
12	1.42	31.27	1.11	4.11	7.77	0.71	0.32
14	1.45	40.11	0.95	4.86	7.78	0.38	0.32
16	0.86	80.08	0.83	7.79	8.17	0.78	0.13
18	1.09	61.02	0.74	6.79	7.84	0.34	0.14
20	0.78	61.70	0.67	7.40	7.81	0.43	0.31
22	0.67	65.60	0.61	8.05	7.79	0.45	0.26
24	0.17	75.08	0.56	10.65	7.86	0.92	0.07
26	0.50	72.29	0.51	9.24	7.77	0.50	0.23
28	0.51	82.87	0.48	10.11	7.79	0.48	0.09
30	0.34	124.6	0.44	13.30	7.99	0.63	0.11
32	0.72	83.02	0.42	10.13	7.72	0.26	0.15

Grid side voltage is assumed to be a 60 Hz voltage source. However, this point can be the connection points of different converters to the grid transformer. Therefore, the resonant frequency should be investigated for the interaction between converters. The limitation of $f_{out} < f_{res} <$

$\frac{f_{PWM}}{2}$ is not enough for avoiding resonance with other converters. A converter switching at 16 kHz with resonance frequency of 4 kHz can interact with other converters switching at 4 kHz.

There is a trade off between current ripple and inductance value. In some cases, reducing inductance to increase current ripple, leads to a more optimal design or vice versa. Using simulation models, different design points have been tested to derive more accurate current harmonic spectrum in an AFE with an inverter load. Table 3.10 summarizes the current harmonics content for various points of design with different capacitor and inductor values. Only current harmonics more than 0.1 A are included in this table. The current harmonic content depends on the achievable bandwidth of the controller is limited by the microcontroller's capability.

For designing the inductors, the material has been limited to M3, M6 and M12 steel due to availability and high permeability allowing gapped inductance stability. Separate inductors for each phase can be used to benefit from the common mode filtering as well. However, in this work the focus has been on three-phase lamination construction to achieve higher power density. Winding ohmic losses and core losses limit minimizing inductor losses.

Table 4.5 summarizes the suggested inductor designs by CramerCoils company. When current ripple is low, the copper losses become dominant and cores can be pushed to max flux density (1.5T). Coil cooling becomes difficult and small cores cannot fit enough copper in the window, even with strong ventilation. In design # 4 the inductance is selected to be double the minimum value and the current ripple is lowered. Only one air gap will be required and the capability of the core gets limited by the winding losses.

When current ripple is high, core losses become dominant and cores have to be significantly reduced in flux density (0.5-0.9T). Larger gaps will be required to lower the flux density and multiple gaps can be the solution. This happens in design # 6 where the inductance value is small and is causing high current ripple content. The cost and size of the inductor are not optimal although the inductor value is very small.

The dependency of steel permeability to switching frequency and flux density must be considered in SiC converters with high switching frequency as well. The solution can be adding extra gap length to provide lower flux density.

Design # 2 and 5 have the same value of converter side inductance. However, because of the difference between the converter topology types, different THD values are resulted. Adding multiple air gaps to design # 5 cannot make the inductor smaller because it is limited by the high current content in high switching frequencies and high THD value.

The filtering performance of design number 1 and 6 are similar as it was discussed. However, it can be seen that using a Si three-level converter can help reducing the inductor size by 23 % and cost by 30 % while the capacitor size is equivalent in both design points. The dimension and structure of design # 1 is presented in Fig. 3-11.

Using a more general algorithm for designing LCL filters such as sweeping through all possible design options needs some performance criteria to find the best design. So it is important to have a criteria in addition to LCL design requirements of Fig. 3-2 to select the best design. Volume, weight and cost can be objective functions to find the optimize design. For example, there are trade-offs between the two acceptable designs that were mentioned regarding volume, weight and size. To calculate the size of the inductor, it is important to analytically model the relation between an inductor value, current spectrum and the design of an inductor. The temperature inside the inductor core and winding is the limiting factor in the design of the inductors. Temperature inside the inductor depends on many elements which includes the losses inside the core. Losses are dependent on the harmonic contents of the current. In this chapter, the temperature in the inductor will be calculated for different modulation methods. Also, the relation between inductor size and harmonic content of the current will be set.

Table 3.10: Converter side current harmonic content for the AFE

Design #	f_{PWM} kHz	L_{grid} (%)	C (pu)	L_{con} (%)	RMS Current Magnitude at frequency (A) at (kHz)				THD (%)
Three-level converters									
1	16	0.45	79	1.26	0.73 at 16	0.64 at 32	0.14 at 48	0.1 at 64	5.23
2	16	0.45	79	2.50	0.30 at 16	0.24 at 32	-	-	0.81
3	16	0.45	79	1.80	0.40 at 16	0.41 at 32	-	-	3.42
4	8	2.53	53	2.50	0.77 at 8	0.65 at 16	0.14 at 32	-	5.30
Two-level converters									
5	16	2.50	53	2.50	0.18 at 4	1.12 at 16	0.45 at 32	-	6.02
6	32	0.45	79	1.26	1.4 at 2	0.27 at 4	1.11 at 32	0.44 at 64	9.23

Table 3.11: Design dimentions for multiple LCL filter designs

Design #	Material Grade	No of Gaps	Relative Losses (%)	Relative Cost (%)	Relative Size (%)
Three-level converters					
1	M6	1	100	100	100
	M3	1	88	100	78
	M6	2	103	70	77
2	M12	1	83	55	82
	M12	1	99	55	97
3	M6	1	93	60	61
4	M6	1	97	80	82
	M6	1	112	75	97
Two-level converters					
5	M6	1	152	140	133
	M6	1	162	130	141
6	M3	1	133	175	117
	M6	1	139	140	132
	M6	2	141	120	118

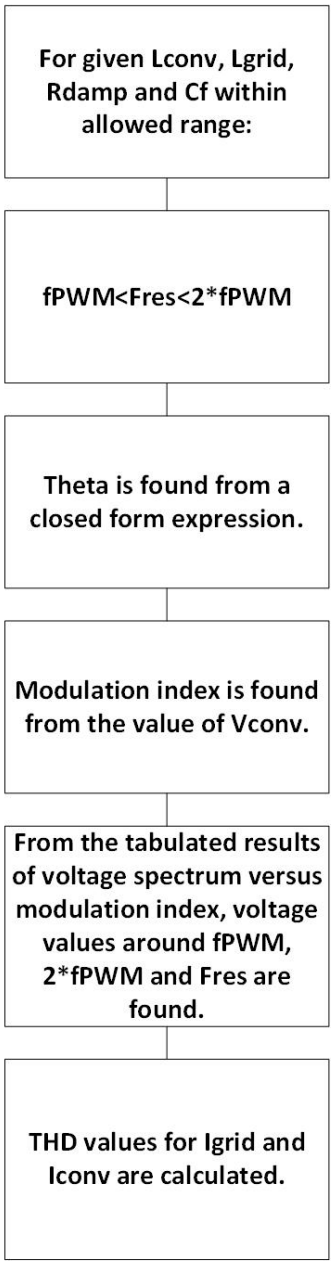


Figure 3-6: The simplified process for using a heuristic algorithm for finding LCL values

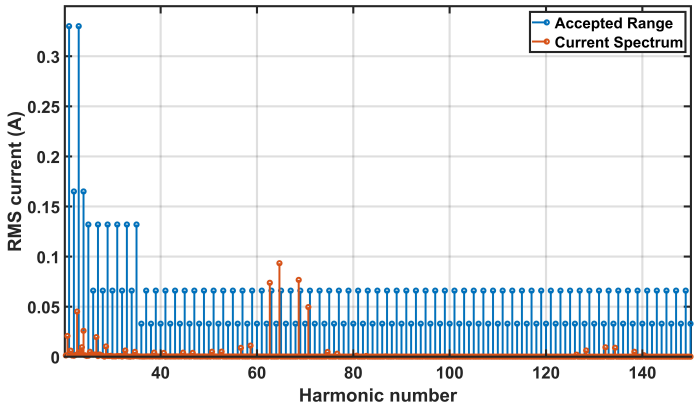


Figure 3-7: Grid current spectrum for a two level converter with switching frequency of 4 kHz

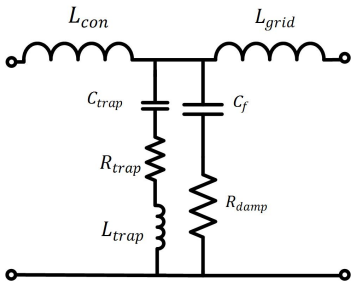
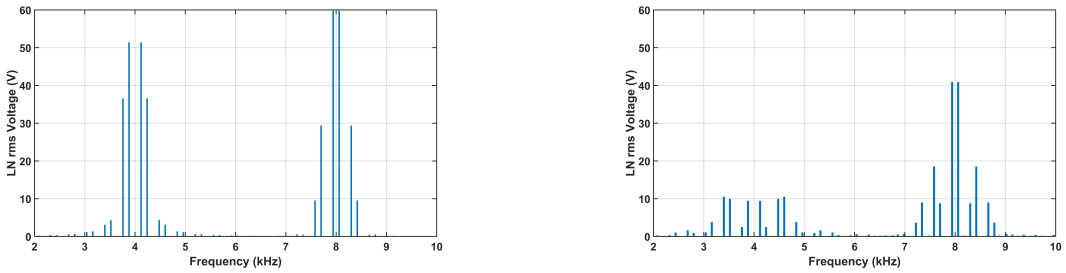


Figure 3-8: Damping branch to meet the current spectrum requirements



(a) Two level converter with space vector modulation

(b) Three level converter with normal space vector modulation method

Figure 3-9: Voltage spectrum of three level and two level converters with 4 kHz of switching frequency

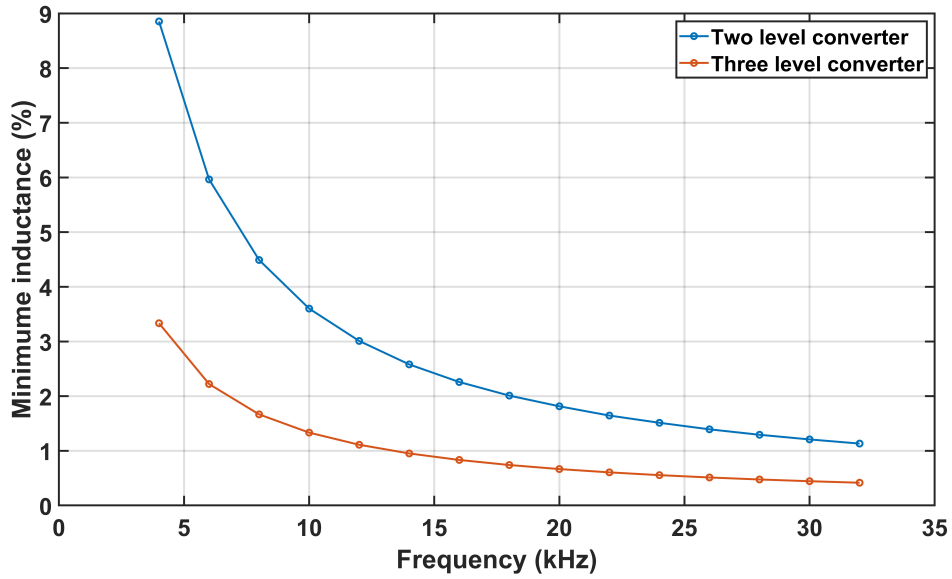


Figure 3-10: Converter side inductance comparison between two level and three level converters for different switching frequencies

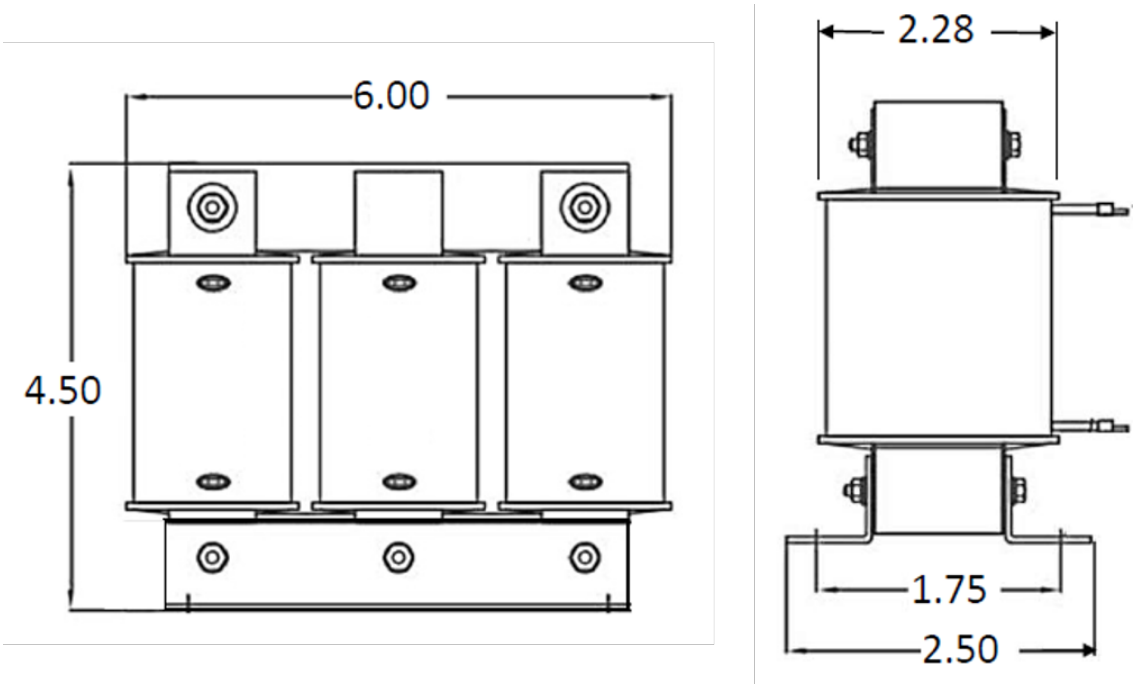


Figure 3-11: Inductor dimensions for NPC with 16 kHz

3.2 Thermal calculations

The inductor size should be compared with the capacitor inside the LCL filter as the performance of the filter can be achieved with either a high capacitor or inductor and the trade-off between the value of these two elements must be based on the objective functions. To find the relation between inductor size and specifications of the inductor such as inductor value and the flowing current, a thermal model needs to be built. The thermal model is necessary to calculate the temperature inside the core and the temperature is the limiting factor in designing inductors. It should be noted that the relation between current ripple and temperature inside the core is not linear. The losses and temperature is more dependent on current harmonic spectrum and changes nonlinearly with frequency value.

Thermal calculation has been usually done using FEA software tools. A simple thermal model for the inductor is considered in [49]. However, thermal calculation is done outside of the loop of designing the LCL filter meaning that the value of the inverter-side inductance is selected based on the current ripple and after the LCL filter design is complete, the thermal model is used for designing the cooling system. FEA software tools can not be used in the optimization process as they can make the process too slow. The thermal model derived in this section is for steady state condition and is simplified to be used in an optimization tool.

3.3 Basics of thermal analysis

In order to make a thermal equivalent circuit for the inductor, a review of heat equation is necessary. The thermal density of a material my be expressed as (3.9)where e has units of J/m^3, c is the specific heat capacity in $J/kg.K$, and T is temperature in K.

$$e = c\,\rho\,T \tag{3.9}$$

The thermal energy in material sample ω of volume V_ω may be expressed as ((3.10)).

$$E_\omega = \int_{V_\omega} e\,dV \tag{3.10}$$

The spatial average of temperature can be found as (3.11). The thermal energy in a specific volume of V_ω can be found as $E_\omega = C_\omega\ < T_\omega >$ where $C_\omega = c\,\rho\,V_\omega$.

$$< T_\omega >= \frac{1}{V_\omega}\int_{V_\omega} T_\omega\,dV \tag{3.11}$$

With Fourier's law the heat flux is proportional to the gradient of the temperature as (3.12) where Q" is a vector that denotes the heat flux in W/m^2; k_x, k_y, and k_z are thermal conductivities in $W/m.K$; and a_x, a_y, and a_z are unit vectors in the x-, y-, and z- directions .

$$Q" = -(k_x\,\frac{\partial T}{\partial x}a_x + k_y\frac{\partial T}{\partial y}a_y + k_z\frac{\partial T}{\partial z}) \tag{3.12}$$

The heat transfer rate through a surface Γ is defined as (3.13) and is measured in watts.

$$\dot{Q}_\Gamma = \int_{S_\Gamma} Q"_\Gamma\,dS \tag{3.13}$$

Net heat transfer through a given surface from a time t_1 to a time t_2 may be expressed as (3.14).

$$Q_\Gamma = \int_{t_1}^{t_2} \dot{Q}_\Gamma \, dt \tag{3.14}$$

The heat equation governs how temperature varies within a material as function of space and time and will be the starting point for thermal analysis. This equation can be manipulated for a cuboid element to find (3.15) where e is thermal energy density and p is power dissipation density.

$$\frac{de}{dt} = p + k_x \frac{\partial^2 T}{\partial x^2} + k_y \frac{\partial^2 T}{\partial y^2} + k_z \frac{\partial^2 T}{\partial z^2} \tag{3.15}$$

The thermal equivalent circuit of a cubical element is shown in Fig. 3-12 . With this thermal model the mean and peak temperature can be determined. The thermal resistance of a region for example in x-direction can be defined as (3.16).

$$R_{\omega x} = \frac{l_{\omega x}}{2\, k_{\omega x}\, S_{\omega x}} \tag{3.16}$$

In order to make the thermal equivalent circuit diagrams more concise, some graphical shorthand

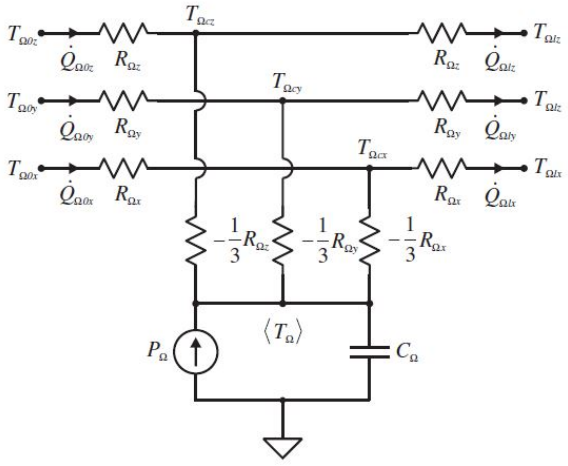


Figure 3-12: Thermal equivalent circuit of a cubical element

notation will prove convenient. Some standard circuit symbols and combinations thereof, and their shorthand notation, are shown in Fig. 3-13. These symbols and combinations of symbols tend to occur very often and so the shorthand notation will save considerable space. The equivalent circuits for the cubical element (Fig. 3-14) is comprised of a small network shown in Fig. 3-12 . In Fig. 3-14, ω denotes the name of the element, N_{cx} is replaced by the name of the central node in the T-equivalent circuit (the node whose temperature is denoted $T_{\omega cx}$ in Figure 10.3), and N_ω is the number of the node whose temperature is that of the mean temperature of the one-dimensional element. The partial dot marked with a 0x is the node corresponding to $T_{\omega 0x}$ in Fig. 3-14; likewise the partial dot marked lx is the node corresponding to $T_{\omega lx}$in Fig. 3-14.

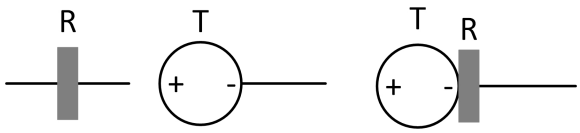


Figure 3-13: Concise circuit symbols symbols.

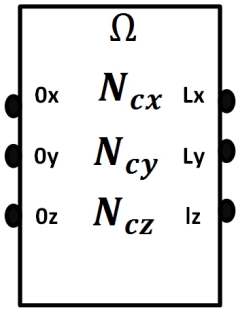


Figure 3-14: Cubical element equivalent circuit symbol symbols.

3.4 Thermal equivalent circuit modeling

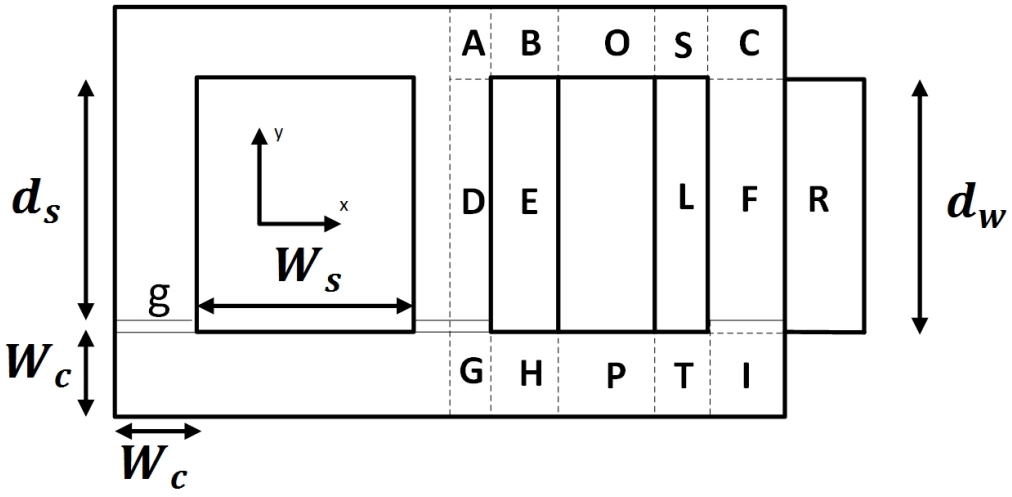
In this section, a thermal model is designed based on the models provided in [50]. First the magnetic circuit of the inductor is modeled. The fringing and leakage effects are ignored to make the model simple. The inductor is divided to four parts. Because of symmetry the thermal calculations need to be done only for one of these parts. Fig. 3-15 shows the inductor from different views with the thermal division.

Each section of the inductor represents a different thermal element of the circuit. Using the nomenclature of Fig. 3-13 and Fig. 3-14, the equivalent circuit is depicted in Fig. 3-16. Therein, the letters A through T indicate the cuboidal elements corresponding to those in Fig. 3-15(c). The numbers listed are node numbers, and an O denotes an open-circuit connection to one of the element's nodes. The temperature Ta denotes ambient temperature.

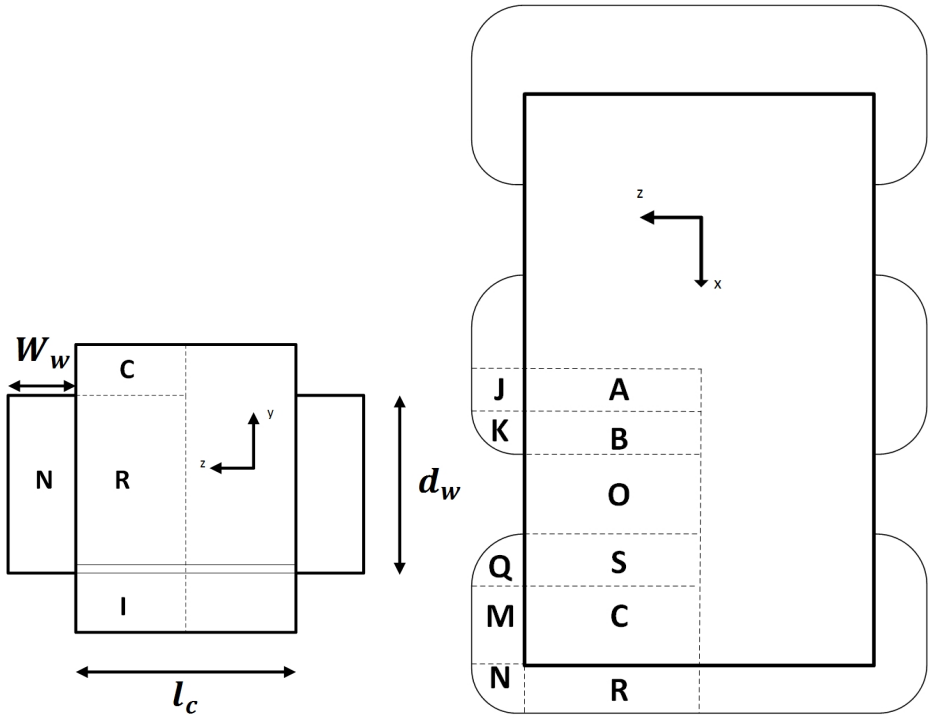
Let us first consider elements A, B, O, S and C. The 0x node of element A is considered to be open since no heat flow will cross the central plane of the electromagnet by thermal symmetry. The lx node of A is linked to the 0x node of element B, the lx node of element B is linked to the 0x node of element O and the connections finishes by the lx node of the C element is connected to the ambient. Some of ly and 0z nodes of these elements, which correspond to the top faces and front faces shown in Fig. 3-15 are also connected to ambient. Consideration of the surface elements of these elements yields the thermal resistance values shown in Table 3.12. Therein, h_{ca} denotes the heat transfer coefficient from the core to air.

We can consider the row of elements D, E, L, F and R now. In this case, elements D and F are core material, while element E, L and R represent the winding bundle. These elements are based on a homogenized representation of the winding, insulator, and air using the approach of [50]. The x- and y-direction within the elements are taken to be orthogonal to the direction of the conductors, which are parallel to the z-direction. This matches the treatment of the rest of the elements in the case of element E, but this will not be the case when we consider elements J, K, Q, M and N.

The lx node of D is connected to the 0x node of E through thermal resistance R_{DE}. These thermal resistances are present because of the differences between materials and is shown in (3.17) and with homogenizing the interface of the winding and air/potting material (shown in Fig. 3-17), the effective heat transfer coefficient (h_{cw}) can be found from (3.18) where h_{sl} is the heat transfer



(a) Cross section



(b) Side view

(c) Top view

Figure 3-15: Cuboids of EE-core inductor

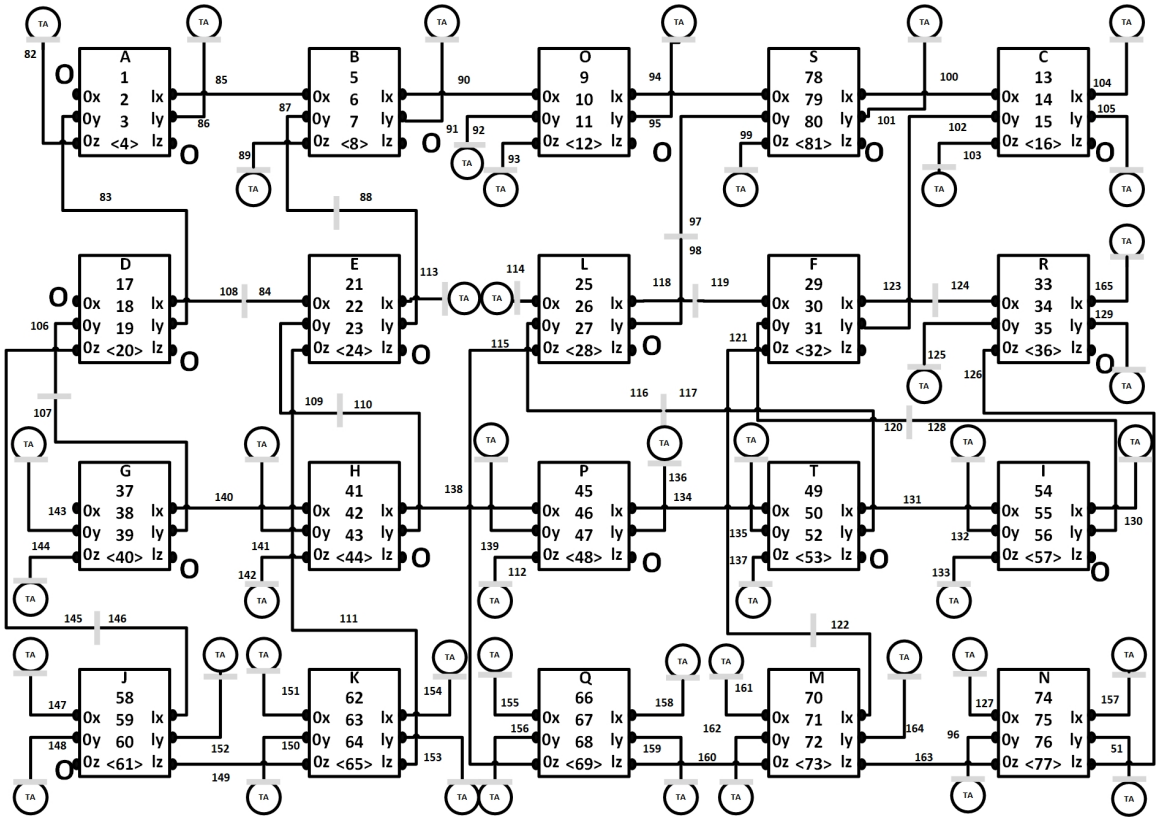


Figure 3-16: Electromagnet thermal equivalent circuit.

coefficient of the slot liner, k_p is the thermal conductivity of the air/potting material. This is the basic formula for the resistance between the core material and the winding. So in summary, R_{DE}, R_{FR}, and R_{FL} can be found from (3.18) with $g_{wc} = 5\,mm$ and $S_{wc} = w_w l_c/2$.

$$R_{CW} = \frac{1}{S_{cw}\, h_{cw}} \tag{3.17}$$

$$h_{CW} = \frac{4\, h_{sl}\, k_p}{4\, k_p + h_{sl}\,(4\, g_{wc} + (4 - \pi\, r_c))} \tag{3.18}$$

The contact point between the core elements D and G can be handled in a way that if the airgap was chosen to be zero the model is still valid. In this case we can find the thermal resistance from (3.19) where S_g is the thermal cross section of the air gap. Finally k_a and h_{cc} denote the thermal conductivity of air and the core-to-core heat transfer coefficient and g is the air gap length. This is used in the thermal resistance between D and G and F and I with $S_g = l_c\, w_c/4$ when calculating R_{DG} and $S_g = l_c\, w_c/2$ for R_{FI} .

$$R_g = max(\frac{g}{k_a\, S_g}, \frac{1}{h_{cc}\, S_g}) \tag{3.19}$$

The resistance R_{EL} is calculated as one-dimensional element through air. This resistor represents a region with one-dimensional heat flow. Air is a lossless and low-density medium. In this case, $P_\omega = 0$ since the material is lossless and C_ω can be neglected since the region has little thermal capacitance. Therefore it can be modeled using a one element resistor.This resistance can be mod-

Table 3.12: Thermal resistances to the ambient

Element A-B			
$R_{Alya} = \frac{4}{h_{ca}\, w_c\, l_c}$	$R_{A0za} = \frac{2}{h_{ca}\, w_c^2}$	$R_{Blya} = \frac{2}{h_{ca}\, w_w\, l_c}$	$R_{B0za} = \frac{1}{h_{ca}\, w_c\, w_w}$
Elements C, G and H			
$R_{Clya} = \frac{2}{h_{ca}\, w_c\, l_c}$	$R_{C0za} = \frac{1}{h_{ca}\, w_c^2}$	$R_{Clxa} = \frac{2}{h_{ca}\, w_c\, l_c}$	$R_{G0ya} = \frac{4}{h_{ca}\, w_c\, l_c}$
$R_{G0za} = \frac{2}{h_{ca}\, w_c^2}$	$R_{H0ya} = \frac{2}{h_{ca}\, w_w\, l_c}$	$R_{H0za} = \frac{2}{h_{ca}\, w_c\, w_w}$	
Element I			
$R_{Ilxa} = \frac{2}{h_{ca}\, w_w\, l_c}$	$R_{I0ya} = \frac{2}{h_{ca}\, l_c\, w_w}$	$R_{I0za} = \frac{2}{h_{ca}\, w_c^2}$	
Element J			
$R_{J0xa} = \frac{2}{h_{ca}\, w_c\, d_w}$	$R_{J0ya} = \frac{2}{h_{ca}\, w_c\, w_w}$	$R_{Jlya} = \frac{2}{h_{ca}\, w_c\, w_w}$	
Element K			
$R_{K0xa} = \frac{4}{h_{ca}\, \pi\, w_w\, d_w}$	$R_{Klxa} = \frac{4}{h_{ca}\, \pi\, w_w\, d_w}$	$R_{K0ya} = \frac{4}{h_{ca}\, \pi\, w_w^2}$	$R_{Klya} = \frac{4}{h_{ca}\, \pi\, w_w^2}$
Element M			
$R_{M0xa} = \frac{2}{h_{ca}\, \pi\, w_c\, d_w}$	$R_{M0ya} = \frac{1}{h_{ca}\, w_w^2}$	$R_{Mlya} = \frac{2}{h_{ca}\, w_w^2}$	
Element O			
$R_{Olya} = \frac{2}{h_{ca}\, w_w\, l_c}$	$R_{O0za} = \frac{1}{h_{ca}\, w_s\, w_c}$		
Element P			
$R_{Plya} = \frac{2}{h_{ca}\, w_w\, l_c}$	$R_{P0za} = \frac{1}{h_{ca}\, w_s\, w_c}$		
Element Q			
$R_{Q0xa} = \frac{4}{h_{ca}\, \pi\, w_w\, d_w}$	$R_{Qlxa} = \frac{4}{h_{ca}\, \pi\, w_w\, d_w}$	$R_{Q0ya} = \frac{4}{h_{ca}\, \pi\, w_w^2}$	$R_{Qlya} = \frac{4}{h_{ca}\, \pi\, w_w^2}$
Element R			
$R_{Rlxa} = \frac{2}{h_{ca}\, d_w\, l_c}$	$R_{R0ya} = \frac{2}{h_{ca}\, w_w\, l_c}$	$R_{Rlya} = \frac{2}{h_{ca}\, w_w\, l_c}$	
Element S			
$R_{Slya} = \frac{2}{h_{ca}\, w_w\, l_c}$	$R_{S0za} = \frac{1}{h_{ca}\, w_w\, w_c}$		
Element T			
$R_{T0ya} = \frac{2}{h_{ca}\, w_w\, l_c}$	$R_{T0za} = \frac{1}{h_{ca}\, w_c\, w_w}$		

eled as $R_{\omega x} = \frac{l_{\omega x}}{k_{\omega x} S_{\omega x}}$ with $l_{EL} = W_s - 2\,W_w$, $S_{EL} = L_c\, d_W/2$, and $k_{EL} = k_a$. The resistance between E and H and E and B is also through an air gap. For the resistance between E and H and E and B, $l_{EH} = d_s - d_w + g$, $S_{EH} = L_c\, w_w/2$, and $k_{EH} = k_a$. The same values for the resistor can be used for the connection between S and L and L and T. Table 3.13 summaries these resistors.

For the winding corner elements (Fig. 3-18) we will have anisotropic properties since it will be thermally more conductive in the direction of the conductors than in other directions. The conductors are assumed to be in the direction of the z-path, which will eventually become our z-axis in our effective cuboid. The y-axis is assumed to be out of the page. The process of obtaining our effective corner element will be to "bend" it into a cuboid as shown in Fig. 3-18. Therein, the principal parameter to be determined is the effective length, l_e. Choosing $l_e = \pi * w/4$ will keep the

Table 3.13: Thermal resistances as one element to model the air interface

Element E		
$R_{EL} = \frac{W_s - 2\,W_w}{L_c\, d_W/2}$	$R_{EH} = \frac{2\,(d_s - d_w + g)}{h_{ca}\, w_w\, l_c}$	$R_{EB} = \frac{2\,(d_s - d_w)}{h_{ca}\, w_w\, l_c}$
Element L and O		
$R_{LT} = \frac{2\,(d_s - d_w + g)}{h_{ca}\, w_w\, l_c}$	$R_{LS} = \frac{2\,(d_s - d_w)}{h_{ca}\, w_w\, l_c}$	$R_{OP} = \frac{2\,(d_s + g)}{h_{ca}\, w_s\, l_c}$

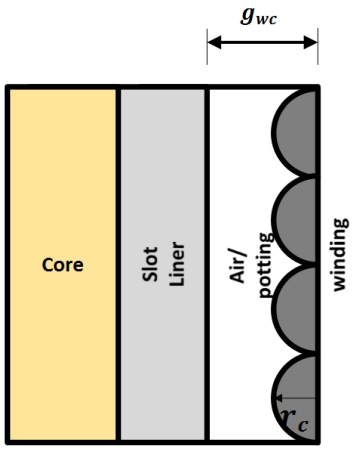


Figure 3-17: Core-winding interface

volume of the two regions the same, keep the area S_z, which is defined to be looking into the cross section along the z-path, the same, and keep S_y, the cross section looking into the elements from the y-axis, the same. The area looking into the direction of path x will not be the same, however. It is readily shown that $S_{or} = 2\,S_x$ This will affect how we connect the element to the other elements and ambient sources. In particular, since S_{or} is in contact with the ambient, it follows that both Sx surfaces (at x=0 and x=lx) should be connected to the ambient.

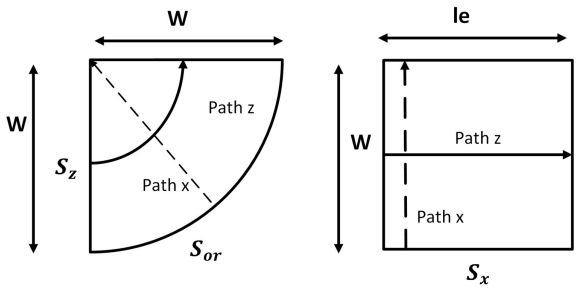


Figure 3-18: Anisotropic and effective corner element symbols.

For the winding elements of J, K, Q, M and N which represent the winding and are in front of elements D, E, L, F and R, we should note that these elements are anisotropic and their orientation is important. When homogenizing the winding, the direction of the conductors is taken (in a local sense) to be in the z-axis. In the case of element J, our local x- and z-axes are in the direction of the electromagnet z- and x-axes, respectively. In the case of element K, the situation is more subtle, because the conductors bend. At the 0x, 0y, and 0z nodes of element K, the alignment of the axes is as in element J. However, for the lx, ly, and lz nodes of element K, the local coordinate system axes have bent to match those of the system. All y-nodes of elements J and K have a thermal resistance to the ambient. The 0x node of element J and the 0x and lx nodes of element K also have a thermal resistance to ambient. All of these resistances are itemized in Table 3.12. In the case of element K, some explanation is in order. This element is bent as illustrated in Fig. 3-18. In order to achieve the same surface area to ambient in the x-direction in Fig. 3-18 as is presented by the area S_{or} in Fig. 3-18, both of the x-nodes have been connected to the ambient temperature.

A final point that merits comment is that the lx node of element J is connected to the 0z node of element D through R_{DJ}. It is important to remember that the coordinate system of element J has

been rotated. This thermal resistance may be calculated using (3.17), where $S_{cw} = w_c d_w = 2$ and h_{cw} is given by (3.18) with $g_{wc} = 0$ and h_{sl} and k_p being the heat transfer coefficient of the slot liner and thermal conductivity of air or the potting material, respectively. R_{DJ} and R_{MN} are equal.

Core losses and ohmic losses should be added to the cubic elements to find maximum winding and core temperature. Core losses include eddy current losses and hysteresis losses. Hysteresis losses can be found with modified Steinmetz equation for a nonsinusoidal waveform as (3.20) where ΔB is the difference between maximum and minimum flux density, B_b is considered to be equal to 1 T with f_b equal to 1 Hz, k_h, α and β are material properties.

$$P_h = k_h \left(\frac{f_{eq}}{f_b}\right)^{\alpha-1} \left(\frac{\Delta B}{2B_b}\right)^{\beta} \frac{f}{f_b} \tag{3.20}$$

Eddy current losses density can be found as $p = \frac{\sigma w^2}{12} \frac{1}{T} \int_0^T (\frac{dB}{dt})^2 \, dt$ where σ is conductivity of the magnetic material that is considered to be 50 MS/m and w is lamination size with the value of 0.8 mm considered here.

As a first step, one of the design points of Table 3.4 is considered here to find the optimal inductor size. An optimization is performed to find the inductor with minimum volume. The constraints are winding and core temperature, minimum inductance and the clearance between windings and the core. Design variables, input parameters and constraints are provided in Table 3.14 and 3.15.

Table 3.14: Converter ratings

Nominal power (hp)	25
Output RMS current (A)	22
Grid frequency (Hz)	60
Power factor	1
Grid voltage (V)	480
DC voltage (V)	750
Grid inductance (uH)	80
Converter inductance (uH)	407
Filter Capacitance (uF)	10
Switching frequency (kHz)	4
Modulation method	Space Vector Modulation

Table 3.15: Constraints and design variables

Heat transfer coefficient from core to air ($\frac{W}{m^2 K}$)	6500
Heat transfer coefficient from winding bundle to air ($\frac{W}{m^2 K}$)	6500
Core to core heat transfer coefficient ($\frac{W}{m^2 K}$)	2000
Ambient temperature (deg C)	25
Maximum winding temperature (deg C)	180
Distance from slot liner to winding bundle g_{wc} (mm)	0.5588
Wire insulation ratio to wire diameter	0.0389
Nomex and wrapper width around the coil (mm)	3.429
Bulge factor	0.1
Horizontal filling (coil width/ window area)	0.53
Stacking factor	0.95
Vertical margin between the coil and core (mm)	8.128
Design variables	
Type of core material	Hiperco50
Type of conductor material	Aluminium
Core width w_c (cm)	1
Wire gauge	17
Number of horizontal turns N_w	1
Number of vertical turns N_d	24
Core depth l_c (cm)	1

Chapter 4

Loss calculation

The difference between switching losses of SiC and Si is the most important factor that makes the usage of SiC switches at high switching frequency. The datasheet information for different types of modules is provided in chapter 7. Yet, it is important to calculate the conduction losses for all the modules and compare the total losses. The selection of modules for a specific converter is one of the design variables that will affect the converter performance. Therefore, in our optimization algorithm, the losses of each module must be calculated and compared with others. Calculation of losses through a simulation program is time consuming and integrating it with the whole optimization process can make the optimization impossible to do. In this work, it has been tried to find closed form expressions for losses in all types of converters and modulation algorithms.

In this chapter, the formulas for calculating losses for two-level and three-level converters will be provided and then methods for measuring switching losses and the effects of stray inductances and gate specifications on losses will be reviewed.

4.1 Loss calculation for two-level converters

In this section, loss calculation formulas for two-level conduction will be reviewed. Assuming a reference voltage value of $v_a = m_a\, sin(\theta)$ and current value of $i_a = \sqrt{2}\, I_{rms}\, sin(\theta - \Phi)$ the conduction duration of upper switch (d_{IGBT}) and conduction duration for the diode (d_{FWD}) are shown in (4.1).

$$\begin{aligned} d_{IGBT} &= \frac{1 + v_a}{2} \\ d_{FWD} &= \frac{1 - v_a}{2} \end{aligned} \tag{4.1}$$

The voltage drop across the switch is equal to $v_{IGBT} = V_0 + R_D\, i_c$. The average conduction losses of the switching can be found be integrating $i_c v_{IGBT}$ as (4.2) and finally the conduction losses can be derived as (4.3). With a similar process, the conduction losses of the diode can be derived as (4.4).

$$P_{cond,IGBT} = \frac{\omega}{2\pi} \int_{\phi}^{\pi+\phi} v_{IGBT}\, i_c\, d_{IGBT}\, dt = \frac{1}{2\pi} \int_{\phi}^{\phi+\pi} (V_0 + R_d\, i_c)\, i_c \frac{1 + m_a\, sin\theta}{2} d\theta \tag{4.2}$$

$$P_{cond,IGBT} = V_0\sqrt{2}\, I_{rms}\{\frac{1}{2\pi} + \frac{1}{8}m_a cos\phi\} + (\sqrt{2}I_{rms})^2\, R_{IGBT}\{\frac{1}{8} + \frac{1}{3\pi}m_a\, cos\phi\} \tag{4.3}$$

$$P_{cond,FWD} = V_0\sqrt{2}\, I_{rms}\{\frac{1}{2\pi} - \frac{1}{8}m_a cos\phi\} + (\sqrt{2}I_{rms})^2\, R_{FWD}\{\frac{1}{8} - \frac{1}{3\pi}m_a\, cos\phi\} \tag{4.4}$$

Switching energy losses for a specific module is given in datasheet for a rated voltage and current value ($V_{DC,r}$ and I_r). In each switching incident, this energy ($E_{r,IGBT}$) is dissipated. But as the current changes sinusoidally, the amount of dissipated energy will be different for each switching occurrence. Assuming that the switching energy is linearly dependent on voltage and current, switching energy can be scaled as (4.5) for switching instances.

$$E(i_c) = E_{r,IGBT}\, \frac{V_{DC}}{V_{DC,r}}\, \frac{i_c}{I_r} \tag{4.5}$$

For continuous switching with PWM, the average switching losses can be found by averaging all the dissipated switching energy (4.6) where N is equal to $\frac{1}{2}\frac{f_{sw}}{f_1}$. With N being a large number, $\frac{1}{T}\sum_{n=1}^{N} i_c(n) = \frac{f_{sw}}{2\pi}\int_0^{\pi}\sqrt{2}I_{rms}sin\theta d\theta$ and (4.6) can be simplified as (4.7).

$$P_{sw,IGBT} = \frac{1}{T}\sum_{n=1}^{N}\frac{V_{DC}}{V_{DC,r}}\frac{i_c(n)}{I_r} \tag{4.6}$$

$$P_{sw,IGBT} = E_{r,IGBT}\frac{V_{DC}}{V_{DC,r}}\frac{1}{I_r}\frac{\sqrt{2}I_{rms}}{\pi}f_{sw} \tag{4.7}$$

Switching losses for the diode is not linearly scaled with current. In (4.8), switching losses for a diode is derived. The relation losses and current values, $f(I_{rms}, I_r)$ can be approximated as (4.10).

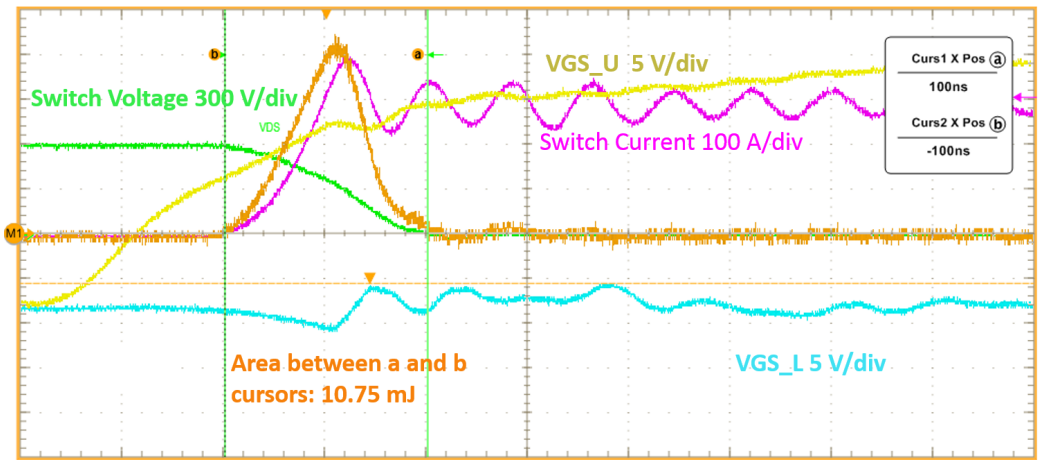
$$P_{sw,FWD} = E_{r,FWD}\frac{V_{DC}}{V_{DC,r}}\, f_{sw}\, f(I_{rms}, I_r) \tag{4.8}$$

$$f(I_{rms}, I_r) = \frac{\sqrt{2}\, I_{rms}}{\pi}\frac{1}{I_r} \tag{4.9}$$

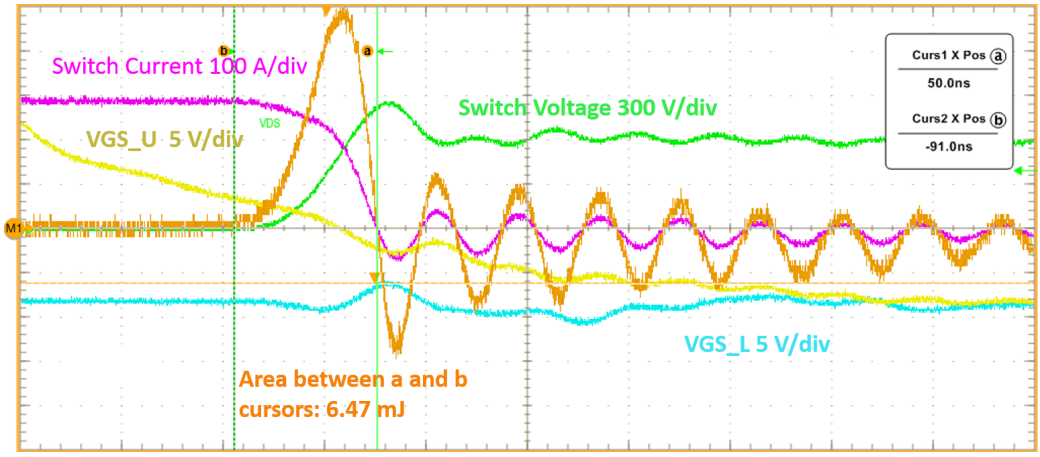
Although all the calculations were done for SPWM, it has been shown in [51] that average losses for space vector modulation is equal to corresponding SPWM values.

It should be noted that although switching losses values are mentioned in datasheet, it is dependent on bus bar layout design and stray inductances. Therefore it is necessary to measure the losses in the design using the known double pulse test. Fig. 4-1 shows the measured losses for CAS300M12BM2.

Closed-form expressions that are provided so far must be modified for SiC two-level converters because the MOSEFT channel can also conduct the current in reverse direction [52]. The third quadrant i-v characteristics for SiC modules are a combination of the Schottky diode and the MOSFET characteristics. The 3rd quadrant i-v characteristics can be found by numerically paralleling the channel i-v characteristics (similar to the first quadrant characterisitcs) and Schottky diode characteristics. The i-v characteristics for CAS300M12BM2 module it is shown in Fig. 4-2. Fig. 4-2(a) shows the IV characteristics from the CAS300M12BM2 datasheet and Fig. 4-2(b) shows the 3rd quadrant characteristics that is found by paralleling the 1st quadrant (Channel IV characteristics)



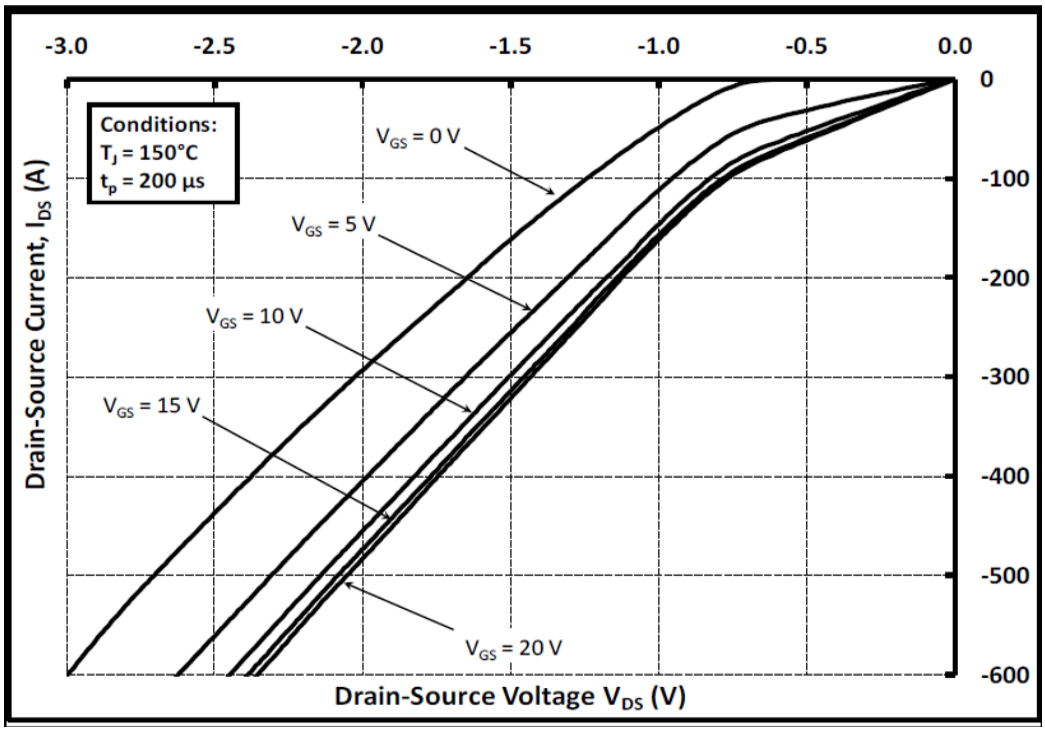
(a) Turn on



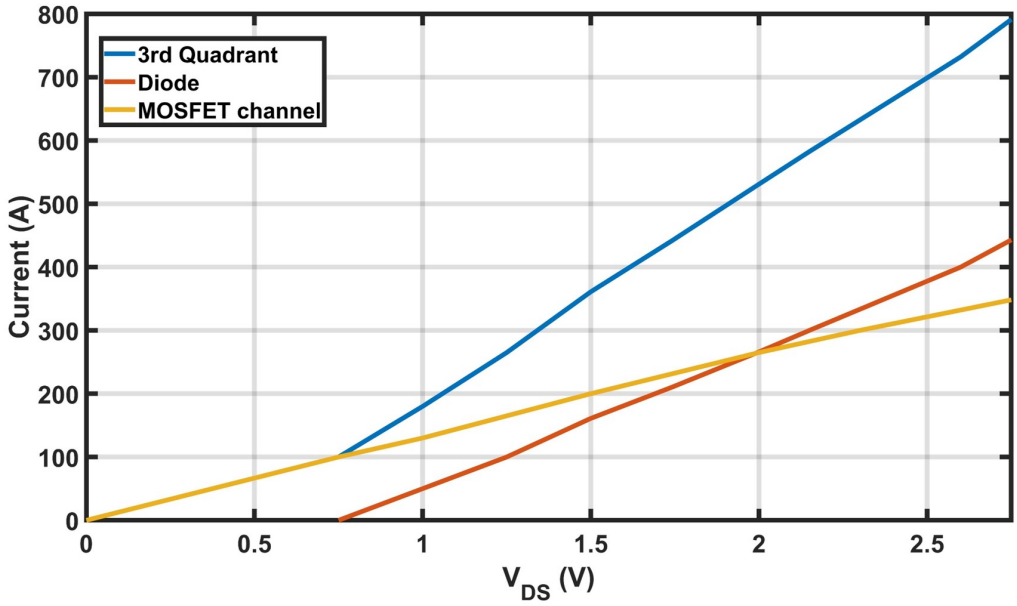
(b) Turn off

Figure 4-1: Double pulse measurement results for CAS300M12BM2 at 300 A and 600 V DC with gate resistance of 4.7 Ω

and Schottky diode IV characteristics.



(a) Datasheet 3rd quadrant IV characteristics of SiC MOSFET for $V_{GS} = 20\,V$ at 150 C



(b) Numerically calculated 3rd quadrant IV characteristics of SiC MOSFET for $V_{GS} = 20\,V$ at 150 C

Figure 4-2: IV characteristics of SiC module. The 3rd quadrant characteristics can be found by adding the currents of Schottky diode characteristics and MOSFET's first quadrant characteristics

A time based simulation was done to find the conduction losses in the third quadrant. The IV characteristics of any IGBT module in linear mode can be modeled by a resistance ($R_{CE,0}$) and a

voltage drop ($V_{CE,0}$) and the similar method can be used for diodes and MOSFET's first quadrant. However, at any instant that the reverse current is flowing through the switch, the amount of current that is flowing in the diode and MOSFET channel must be determined and based on that, the losses can be calculated. Table 4.1 shows the ratio between the channel current and total current and corresponding voltage drop.

Table 4.1: Channel current to total current ratio for a SiC MOSFET

Current ratio	Total Current (A)	Voltage drop (V)
1	0	0
1	100.7	0.724
0.787	157	0.902
0.733	187.6	1.005
0.656	239	1.155
0.631	267.6	1.247
0.587	319.9	1.396
0.562	366.1	1.54
0.522	455.9	1.793
0.509	509.6	1.954
0.487	585	2.166
0.474	642.2	2.339
0.466	696.7	2.5
0.459	735.2	2.609
0.447	784.3	2.729

The algorithm used for SiC MOSFET conduction loss calculation is shown in Fig. 4-3. In this algorithm, in positive output current direction, first quadrant IV characteristics is used to find the instantaneous losses. In reverse current direction, first the current is split into channel current and diode current. A piecewise linear function is used to estimate the current ratio between different current values of Table 4.1. The coefficients of this function is shown in Table 4.2 For example, for total current of $239 < i_{out} < 267$, $ratio_{MOS}$ is equal to $b_0 + b_1 * i_{out} = 0.871 - 0.898 * i_{out} * 10^3$. Table 4.2 also shows the values of resistance and voltage drop in different current values in the Schottky diode and the MOSFET channel that have been used in the algorithm presented in Fig. 4-3 for CAS300M12BM2. MOSFET voltage drop V_DS is assumed to be zero at all points.

Assuming unity power factor, in a half-bridge with Si IGBT modules, the upper IGBT switch only conducts in positive direction of current. But in a half-bridge with SiC modules the MOSFET conducts in both directions of current and therefore in the algorithm presented in Fig. 4-3 both directions of current must be considered.

Fig. 4-4 shows the losses in the SiC and IGBT module with and without considering the third quadrant IV characteristics for the operating condition of Table 4.3. SiC converter is operated at the PWM frequency of 12 kHz whereas the Si IGBT converter is run at 8 kHz due to IGBT junction temperature limit being exceeded at 186 A output current and 12 kHz PWM frequency. The upper MOSFET has conduction losses in the reverse direction of current as it shares the current with the parallel diode.

Fig. 4-5(a) shows the losses in the upper switch of one phase of a three-phase converter for the operating conditions of Table 4.3. The conduction losses are higher for higher fundamental frequencies in positive direction whereas it is lower for reverse current direction. The difference between the average losses in the upper switch in reverse current condition can be explained by

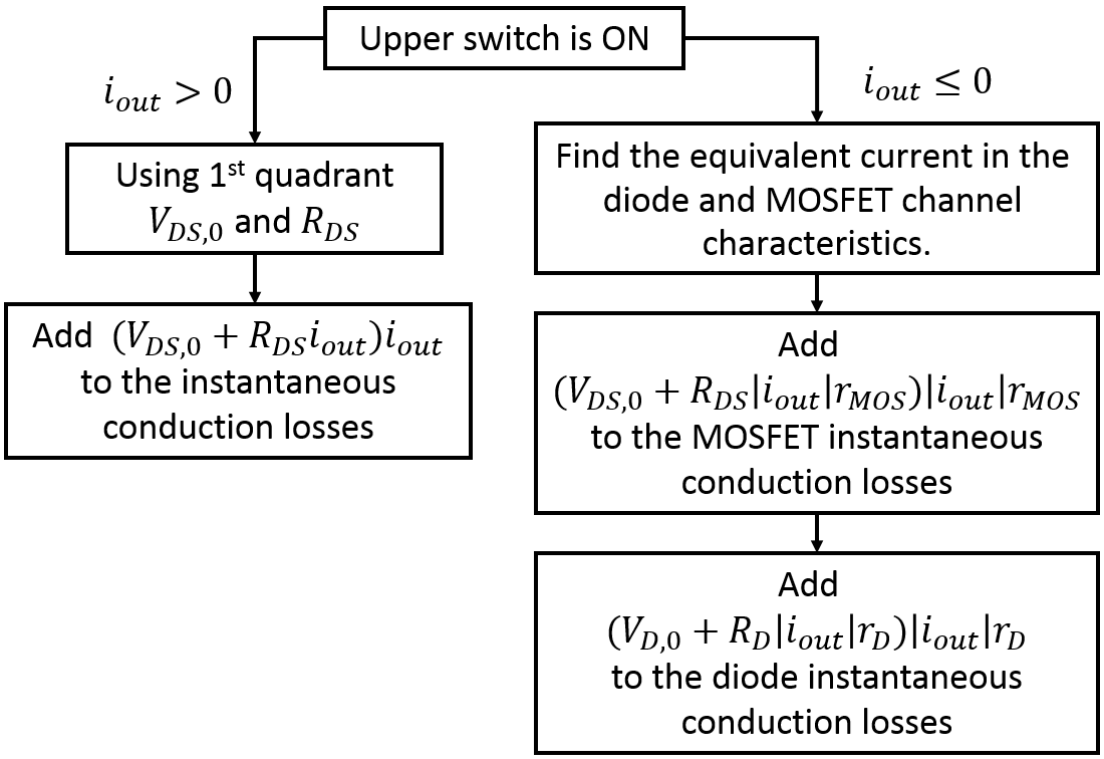


Figure 4-3: The algorithm for finding instantaneous conduction losses in the SiC MOSFET channel

Table 4.2: Current ratio linear function description and resistance values for SiC MOSFET

b_0	$b_1 * 10^3$	Total Current (A)	$R_D * 10^3$	V_D	$R_{DS} * 10^3$
0	0	0	0	0	0
1	0	100.7	0	NA	7.278
1.344	-3.543	157	5.558	0.717	7.344
1.064	-1.764	187.6	6.206	0.695	7.389
1.014	-1.495	239	4.662	0.772	7.736
0.871	-0.898	267.6	5.517	0.702	7.736
0.855	-0.838	319.9	4.482	0.804	7.87
0.759	-0.538	366.1	5.094	0.723	7.967
0.726	-0.448	455.9	4.383	0.837	7.868
0.628	-0.233	509.6	5.02	0.698	7.432
0.659	-0.295	585	4.252	0.89	8.373
0.612	-0.214	642.2	4.637	0.775	8.636
0.576	-0.158	696.7	4.648	0.771	8.102
0.59	-0.178	735.2	4.258	0.916	8.456
0.637	-0.242	784.3	3.362	1.272	9.129

Table 4.3: Sample operating condition

Output current (A)	186
Output frequency (Hz)	45
Power factor	0.63
DC voltage (V)	650
Operating mode	V/Hz
Modulation method	Space Vector Modulation

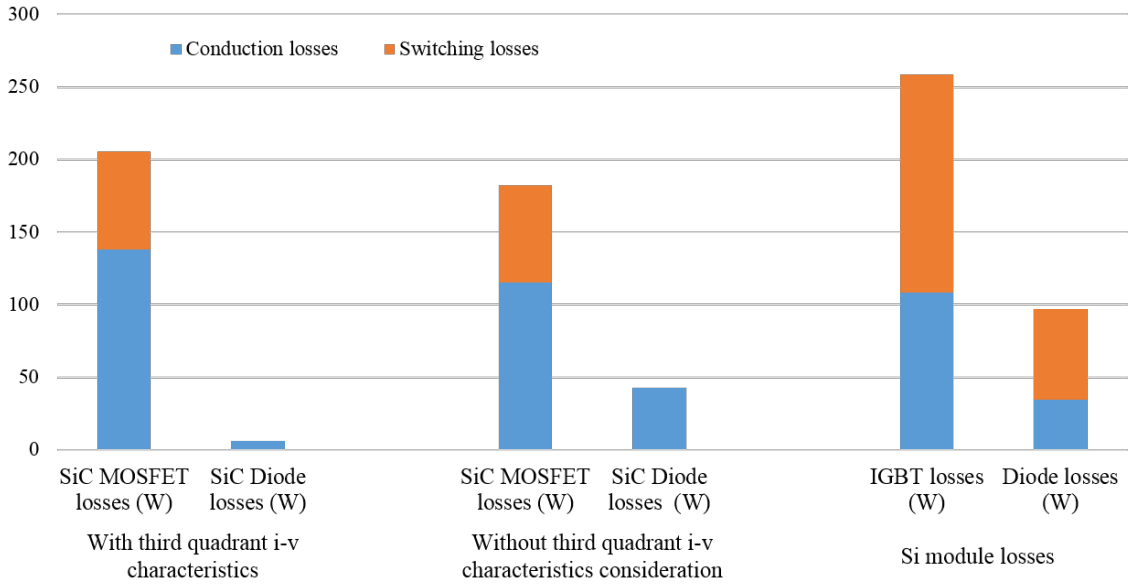
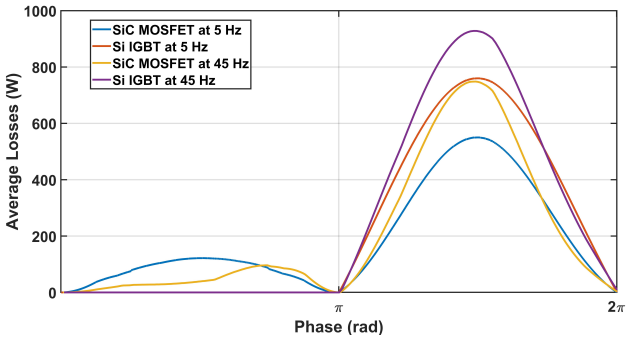
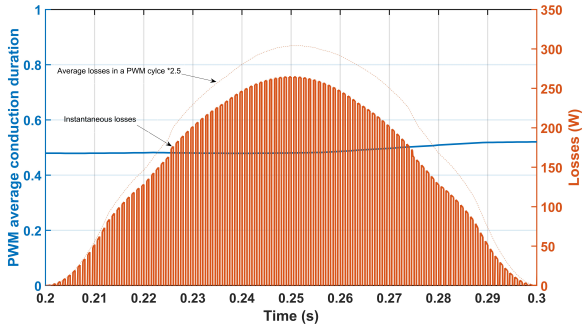


Figure 4-4: Losses for SiC MOSEFT and Si IGBT in operating conditions of Table 4.3

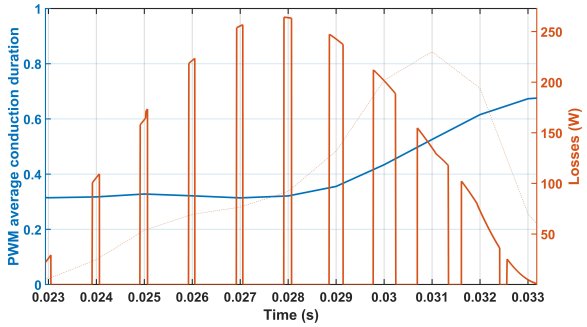
the change of conduction duration over time. Fig. 4-5(b) and 4-5(c) show the average conduction duration for the upper switch in the reverse current direction. Conduction duration is around 0.5 for low operating frequencies where as it changes with the operating frequency of 45 Hz. Switching frequency has been changed to 1 kHz to make the switching pulses more visible in this picture.



(a) Average losses in a PWM cycle for different fundamental frequencies. IGBT module is switched at 8 kHz



(b) Average conduction duration with switching frequency of 1 kHz and fundamental frequency of 5 Hz



(c) Average conduction duration with switching frequency of 1 kHz and fundamental frequency of 45 Hz

Figure 4-5: Losses and conduction duration for different fundamental frequencies and operating conditions of Table 4.3

4.2 Loss calculation for three-level converters

In this section,first closed form expressions for losses of NPC coverters will be derived. These expressions can only be used for carrier based modulation with zero common mode voltage added (SPWM). Ttype converter losses expressions are provided in [53]. Then, different modulation methods will be compared from different aspects. Modulation methods with neutral point balancing and loss reduction have different spectrum.

4.2.1 Conduction loss calculation

One leg of an NPC converter is shown in Fig. 4-6. With level shifted PWM, S1 conducts when the reference voltage is higher than both triangular waveforms. Fig. 4-7 shows the modulation and reference waveforms. Fig. 4-8 shows these waveforms in more details for an output voltage with output frequency of 60 Hz and modulation frequency of 15 kH with Ts as the switching period and T1 as the only time that S1 does not conduct. With the reference voltage being equal to $v_a = m_a sin(\theta)$, the conduction duration of the upper switch can be derived as $T_s m_a sin(\theta)$ and therefore S1 conduction losses can be derived as (4.10).

$$P_{cond,S1} = \frac{1}{2\pi}\int_{\phi}^{\pi}\left[V_0 + \sqrt{2}R_{IGBT}I_{rms}sin(\theta-\phi)\right] I_{rms}sin(\theta-\phi)\, m_a sin(\theta)d\theta = \frac{\sqrt{2}\, m_a\, I_{rms}}{12\pi}\{3V_0\big[(\pi-\phi)cos(\phi)+sin(\phi)\big] + 2\sqrt{2}I_{rms}\big[1+cos(\phi)\big]^2\} \tag{4.10}$$

Conduction duration for S2 is the duration for which the reference voltage is higher than the lower triangle waveform. For θ between ϕ and π, S2 is on all the time but for $\pi < \theta < \pi + \phi$ S2 is only on for $T_s(1 + v_a)$. Therefore conduction losses for S2 can be found from (4.11).

$$\begin{aligned} P_{cond,S2} &= \frac{1}{2\pi}\int_{\phi}^{\pi}\left[V_0 + \sqrt{2}R_{IGBT}I_{rms}sin(\theta-\phi)\right] I_{rms}sin(\theta-\phi)d\theta \\ &+ \frac{1}{2\pi}\int_{\pi}^{\pi+\phi}\left[V_0 + \sqrt{2}R_{IGBT}I_{rms}sin(\theta-\phi)\right] I_{rms}sin(\theta-\phi)(1+m_a\, sin(\theta))d\theta = \\ &\frac{\sqrt{2}I_{rms}}{12\pi}\{V_0\big[12+3m_a(\phi\, cos(\phi)-sin(\phi)\big] + R_{IGBT}\big[3\pi - 2m_a(1-cos(\phi))^2\big]\} \end{aligned} \tag{4.11}$$

Conduction duration for D1, D2, D3 and D4 is equal. D1 and D2 are only on when current is negative but positive rail voltage is used. D3 and D4 are on when current is positive and negative DC

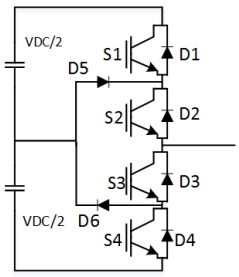


Figure 4-6: One leg of an NPC converter

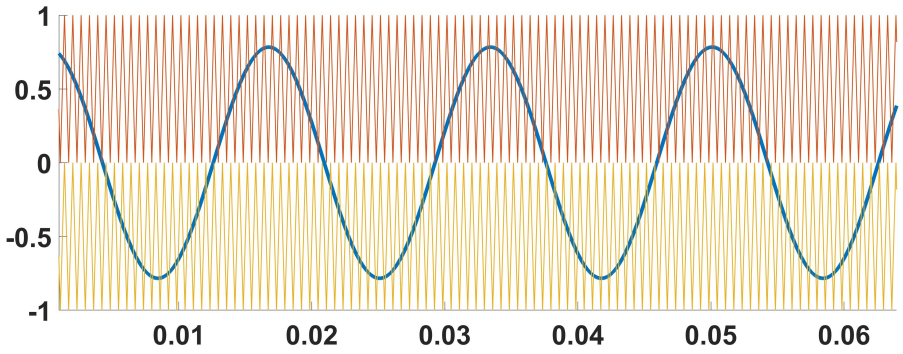


Figure 4-7: Triangular and reference voltage waveforms

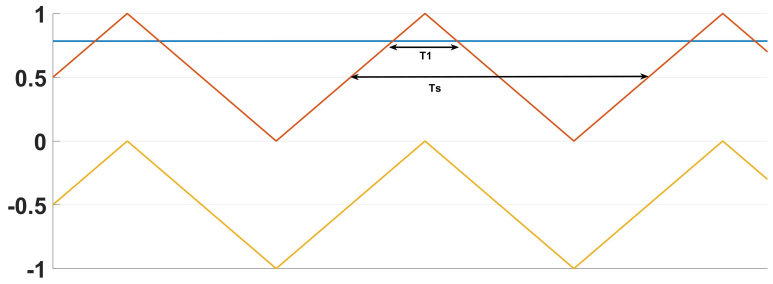


Figure 4-8: Conduction duration of S1

voltage is used. This time only happens for $\pi < \phi < \pi + \phi$ and for the duration of $-T_s\, m_a\, sin(\theta)$. The total losses are shown in (4.12).

$$\begin{aligned} P_{cond,D3} &= -\frac{1}{2\pi}\int_{\pi}^{\pi+\phi} \left[V_0 + \sqrt{2}R_{IGBT}I_{rms}sin(\theta-\phi)\right] I_{rms}sin(\theta-\phi)\, m_a sin(\theta) d\theta \\ &= \frac{\sqrt{2}I_{rms}m_a}{12\pi}\{3V_0\big[-\phi cos(\phi) + sin(\phi)\big] + 2\sqrt{2}r_{IGBT}I_{rms}\big[1-cos(\phi)\big]^2\} \end{aligned} \tag{4.12}$$

Diodes D5 is on when the current is positive and the mid point voltage is selected. When $\phi < \theta < \pi$, the conduction duration is equal to $T_s(1 - v_a)$. When $\pi < \theta < \pi + \phi$, the conduction duration is equal to $T_s(1 + v_a)$. For this period of time losses can be found as (4.13). Conduction losses for D5 and D6 are equal.

$$\begin{aligned} P_{cond,D5} &= \frac{1}{2\pi}\int_{\phi}^{\pi} \left[V_0 + \sqrt{2}R_{IGBT}I_{rms}sin(\theta-\phi)\right] I_{rms}sin(\theta-\phi)\,(1 - m_a sin(\theta)) d\theta + \\ &\frac{1}{2\pi}\int_{\pi}^{\pi+\phi} \left[V_0 + \sqrt{2}R_{IGBT}I_{rms}sin(\theta-\phi)\right] I_{rms}sin(\theta-\phi)\,(1 + m_a sin(\theta)) d\theta = \\ &\frac{\sqrt{2}I_{rms}}{12\pi}\{V_{D,0}\big[12 + 3m_a\big[(2\phi-\pi)cos(\phi) - 2sin(\phi)\big]\big] + \sqrt{2}R_D\big[3\pi - 4m_a(1+cos(\phi)^2)\big]\} \end{aligned} \tag{4.13}$$

4.2.2 Switching loss calculation

Switching in S1 occurs only on the positive side of current. Therefore base on (4.6), switching losses for S1 is derived in (4.14).

$$P_{sw,S1} = \frac{f_{sw}}{2\pi}\int_{\phi}^{\pi}\sqrt{2}I_{rms}sin\theta d\theta = \\ f_{sw}E_{sw}\frac{\sqrt{2}I_{rms}}{I_{ref}}\frac{V_{DC}}{V_{ref}}(\frac{1}{2\pi}\big[1+cos(\phi)\big]) \tag{4.14}$$

Switching in S2 happens when the current is positive and the voltage is switched between mid point voltage and negative DC. So for $\pi < \theta < \phi + \pi$, switching losses of S2 can be found as (4.15).

$$P_{sw,S2} = \frac{f_{sw}}{2\pi}\int_{\pi}^{\pi+\phi}\sqrt{2}I_{rms}sin\theta d\theta = \\ f_{sw}E_{sw}\frac{\sqrt{2}I_{rms}}{I_{ref}}\frac{V_{DC}}{V_{ref}}(\frac{1}{2\pi}\big[1-cos(\phi)\big]) \tag{4.15}$$

Reverse recovery happens in D4 when switching happens between negative voltage and neutral. This happens when $\pi < \phi < \pi + \phi$ and assuming a linear relation between dissipated energy and current for the diode, the switching losses can be derived as (4.16). Losses for D1 and D4 are equal. D2 and D3 experience no switching losses as the voltage across them is always zero clamping the connection point between the series switches to neutral voltage.

$$P_{sw,D4} = \frac{f_{sw}}{2\pi}\int_{\pi}^{\pi+\phi}\sqrt{2}I_{rms}sin\theta d\theta = \\ f_{sw}E_{sw}\frac{\sqrt{2}I_{rms}}{I_{ref}}\frac{V_{DC}}{V_{ref}}(\frac{1}{2\pi}\big[1-cos(\phi)\big]) \tag{4.16}$$

Diode D5 experiences reverse recovery when switching happens between mid point voltage and positive but switching from mid-point to negative does not make reverse recovery losses in the diode D5 because the voltage across it will be equal to zero in both switching states. If the relation between dissipated energy and current for the diode is linear the switching loss in the diode can be found from (4.17).

$$P_{sw,D5} = \frac{f_{sw}}{2\pi}\int_{\phi}^{\pi}\sqrt{2}I_{rms}sin\theta d\theta = \\ f_{sw}E_{sw}\frac{\sqrt{2}I_{rms}}{I_{ref}}\frac{V_{DC}}{V_{ref}}(\frac{1}{2\pi}\big[1-cos(\phi)\big]) \tag{4.17}$$

4.2.3 Comparison of different modulation methods

In this section, proposed modulation methods in the literature will be reviewed first. Then our proposed method for a balance between losses, THD and consequently converter side inductance and neutral point voltage will be provided. One of the disadvantages of three level converters is the potential of voltage imbalance between the upper and lower capacitor. There can be imbalance induced by imperfections in the converter or load; for example capacitance mismatch or unbalanced loads [54]. This can result in even order current harmonics and also it can cause capacitors or semiconductors failure. The other type of imbalance results from switching the NPC. Low power factor and high modulation index increases this effect more. However, since we are focusing on

active front end application, we can consider the unity power factor. Different solutions have been proposed for lowering the voltage unbalance. Some of methods proposed in the literature are more suitable for lower power factor applications and their performance in lowering unbalance is not good in high power factor applications. For example, [55] proposes injection of six harmonic to the common mode voltage that can be ineffective in balancing the voltage in high power factor applications. The method provided in [56] injects even harmonics in the AC side. This can results in higher THD and for the AFE application, a bigger converter side inductor will be required. Using redundant small vectors, is a another solution for reducing neutral point imbalance which is equivalent to injecting common mode voltage to the line to neutral output voltages as there is the relation between space vector modulation and carrier based modulation strategies is well known [56]. However, the common voltage function over time can be a function with discontinuous steps rather than a harmonic order of the fundamental frequency. Space vector modulation methods can be based on nearest three vector modulation or non nearest vector modulation. Non nearest vector modulation methods such as virtual vector modulation [57] can result in zero neutral point unbalance in any modulation index and power factor. In [58], a modulation method is proposed that is suitable for light load application and it is based on the measurements required in an electric starter generator. A modulation strategy that is based on non nearest vector modulation is proposed in [59]. This modulation method minimizes switching losses and finds the optimal switching sequence for minimum neutral point voltage imbalance. The disadvantage with all non nearest vector modulation methods is high distortion and resultant high THD values. This will affect the losses inside the converter side inductor in an AFE and can increase the current THD on the grid side. A nearest vector modulation method is proposed in [60]. This method minimizes neutral point voltage imbalance by using the redundancy in small vectors and the knowledge of the area of voltage vector. It also depends on calculating the minimum achievable neutral point unbalance based on the previous measurements.

In this section, two modulation methods are proposed that balance switching losses, THD and neutral point voltage unbalance and is based on nearest vector modulation. Short and medium vectors contribute to neutral point voltage unbalance. Fig. 4-9 shows the current direction from the short vector of PPO with the duration of dS1. Assuming a balanced three phase load, the voltage unbalance defined as the difference between upper and lower capacitor voltage can be calculated from (4.18) where C is the total DC bus capacitor value. Phase C current in this case is the neutral point current that contributes to the unbalance. Table 4.5 shows the current contributing to the voltage difference between upper and lower capacitor in an NPC converter for all short and medium vectors.

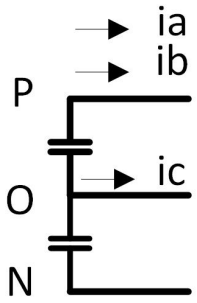


Figure 4-9: Current direction for the switching vector of PPO

$$\Delta V_{NP} = V_{upper} - V_{lower} = \frac{(i_c - i_a - i_b) * d_{S1} * f_{PWM}}{2C} = \frac{i_c\, d_{S1}\, f_{PWM}}{C} \tag{4.18}$$

Table 4.5 shows the current contributing to the voltage difference between upper and lower capacitor in an NPC converter.

Table 4.4: Neutral point current of short and medium switching vectors

Short vectors	Neutral point current
POO	$-i_a$
ONN	i_a
ONO	$-i_b$
POP	i_b
OON	$-i_c$
PPO	i_c
NOO	$-i_a$
OPP	i_a
OPO	$-i_b$
NON	i_b
OOP	$-i_c$
NNO	i_c
Medium vectors	**Neutral point current**
OPN	i_a
PON	i_b
NPO	i_c
ONP	i_a
NOP	i_b
PNO	i_c

In low modulation index, the redundancy of short vectors can be used to balance this voltage. However, in high modulation index which is the case for an AFE, short vectors are not capable of balancing the voltage in one switching cycle. In this work, there has been a set of rules made to limit the choice of switching sequences and short vector selection. The rules are as follow:

- The switching sequence must go from low to high in the first half of the switching cycle. For example, each phase can go from Negative DC voltage (N) to mid point (O) and then mid point (O) to Positive DC voltage (P)
- Switching between N and P with no intermediate state is not possible.
- Only total number of 6 switching can happen in one switching cycle.

Considering these rules, the possible switching sequences and vector selections will be limited. For the triangle areas shown in Fig. 4-10, the possible switching sequences are presented in Table 4.5.

In this work, two new modulation methods are analyzed to find the best approach for an AFE application. In the first method, number of switching events is limited to 4 and each switching cycle, the neural point voltage unbalance (ΔV_{NP}) and two of the phase currents are measured. For each

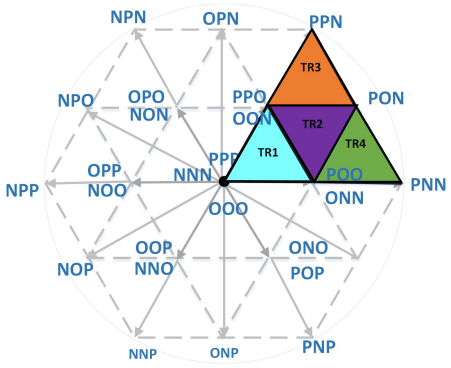


Figure 4-10: First 60 degrees of voltage in a three level converter space vector

Table 4.5: Possible switching vectors and sequences in the four triangle areas shown in Fig. 4-10

Triangle	Switching sequence	Total number of switching events
TR1	POO-PPO-PPP-PPO-POO	4
	OON-OOO-POO-PPO-POO-OOO-OON	6
	NNN-ONN-OON-ONN-NNN	4
TR2	PON-POO-PPO-POO-PON	4
	OON-PON-POO-PPO-POO-PON-OON	6
	ONN-OON-PON-OON-ONN	4
	OON-PON-POO-PON-OON	4
TR3	ONN-OON-PON-OON-ONN	4
	ONN-OON-PON-POO-PON-OON-ONN	6
	PON-POO-PPO-POO-PON	4
TR4	PNN-PON-POO-PON-PNN	4
	ONN-PNN-PON-POO-PON-PNN-ONN	6
	ONN-PNN-PON-PNN-ONN	4

triangle area, the neutral point voltage unbalance is predicted for the next switching cycle with all the possible switching sequences with four switching events. As it can be seen in Table 4.5, for each area there will be at most three possible switching sequences. At TR1, only one switching sequence will be possible. Because the two switching sequence cannot be followed by each other as it causes switching from N to P or vice versa. Between the sequences that clamp phase A to P and the sequence that clamps phase C to N, the first one will be always selected for this triangle area because it is compatible with DPWM. Therefore, this modulation method is not suitable for small modulation indexes. This algorithm is presented in Fig. 4-11.

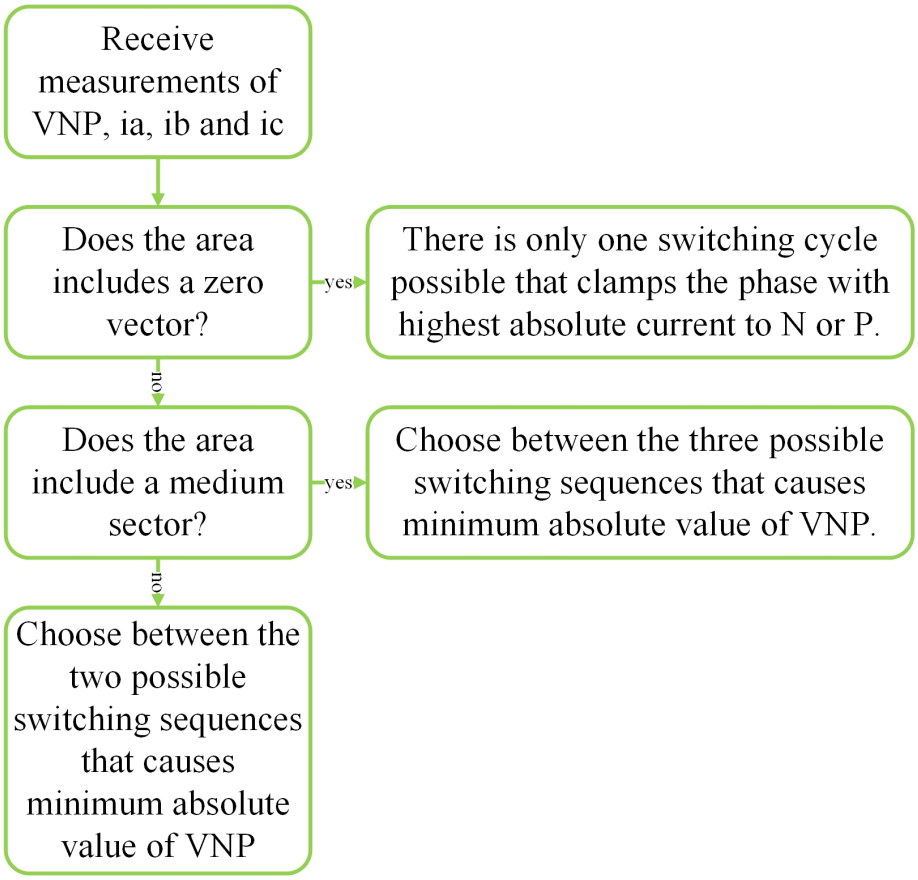


Figure 4-11: Proposed modulation algorithm for minimizing neutral point imbalance and switching losses

The other modulation method allows 6 switching events as well and provides more flexibility for adjusting the neutral point imbalance. In this modulation method, two redundant short vectors are used. Assuming the duty ration of a short vector is dS1, dS1 is divided to dS11 and dS12 to make the neural point voltage unbalance (ΔV_{NP}) equal to zero. If the short vectors are not capable of setting ΔV_{NP} to zero, the equation will result in negative duty ratio. The algorithm will set the duty ratio for that short vector to zero and the minimum possible absolute of ΔV_{NP} will be calculated. For TR3 and the switching sequence of ONN-OON-PON-POO-PON-OON-ONN, the equation for calculating the duty cycle distribution of POO and ONN is shown in (4.19). In this equation, $\Delta V_{NP,M}$ is the measured neutral point voltage imbalance, d_{S1} and d_{S2} are the duty ratios associated with the two short vectors and d_M is the middle vector duty ratio. The algorithm used for selecting the modulation sequences is shown in Fig. 4-12.

$$
\begin{aligned}
&d_{S11}\, i_a - i_a\, d_{S12} + i_b\, d_M - ic\, d_{S2} = \frac{-\Delta V_{NP,M}\, C}{f_{PWM}} \\
&d_{S11} + d_{S12} = d_{S1}
\end{aligned}
\tag{4.19}
$$

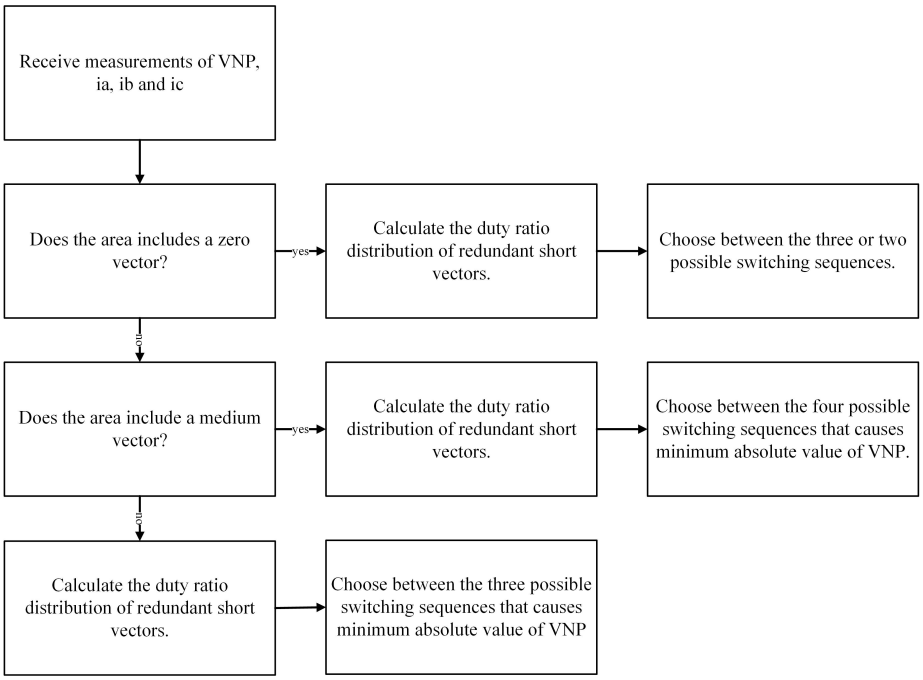


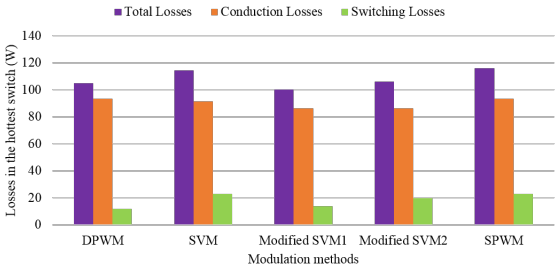
Figure 4-12: Proposed modulation algorithm for minimizing neutral point imbalance and switching losses. This method has higher switching losses compared to the method shown in 4-11

The methods provided so far have different amount of losses, THD and neutral point voltage imbalance. This comparison for the ratings provided in Table 4.6 is shown in Fig. 4-15. It can be seen that DPWM and SPWM cannot be used in NPC converters with small values of DC bus capacitors. The modified methods show less neutral point voltage unbalance compared to SVM while the losses are in the same range as SVM. Modified modulation methods are more applicable for converters with high switching frequency as they depend on the sampling of current and voltage. In order to avoid overrun of microprocessors, the update of rate of duty cycle of switches should be limited to one PWM cycle. The error in current and voltage measurements can be high in low PWM frequencies and therefore the predicted switching sequence can be non optimal in these methods. The performance of modified PWM method 1 is shown in Fig. 4-16. Values are in ratio to the maximum measured value. Maximum peak neutral point voltage unbalance happens at 4 kHz being equal to 60 V, maximum value of THD (%) happens in 4 kHz being equal to 4.55, maximum losses in one phase is at 32 kHz being equal to 834 (W) and maximum hottest switch losses happens at 32 kHz being equal to 148 (W). Peak neutral point voltage unbalance in SVM varies between 44 V and 40 V with switching frequency which compared to the modified modulation method, is not dependent on switching frequency.

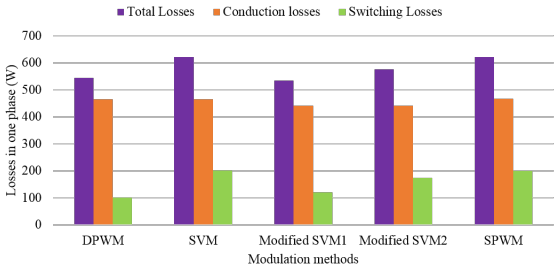
SiC two-level and Si three-level converters losses are compared for different switching frequencies in Fig. 4-17 for two converter ratings of Table 4.7. Losses in SiC two level converter hottest switch is higher compared to the Si three level one. The hottest switch in three level converter with 200 hp output is upper diode which changes to inner IGBT at the switching frequency of 18 KHz.

Table 4.6: Sample case converter ratings for comparison of different modulation techniques in a three-level converter

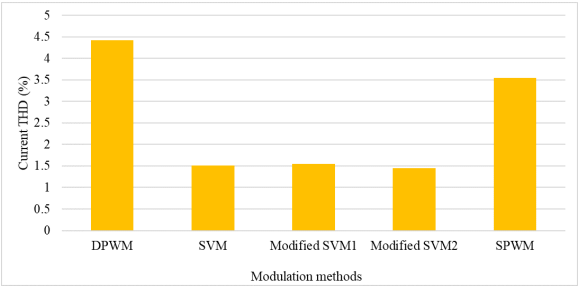
Parameters	Value
Nominal power (hp) for converter with 300 A module	200
Nominal power (hp) for converter with 300 A module	25
Output frequency (Hz)	60
Power factor	0.99
Grid voltage (V)	480
DC voltage (V)	650
Grid inductance (mH)	0.16
Switching frequency (kHz)	12
DC bus capacitor (μF) for converter with 300 A module	570
DC bus capacitor (μF) for converter with 50 A module	189
300 A, 600 V IGBT Power Module	FD300R06KE3
50 A, 600 V IGBT Power Module	F3L50R06W1E3B11



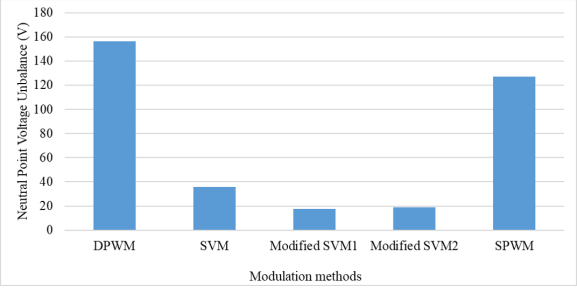
(a) Losses in the hottest switch in a phase



(b) Total Losses



(c) Current THD (%)



(d) Neutral point voltage unbalance (V)

Figure 4-13: Comparison of different modulation methods in a three-level converter running as an inverter with the operating condition of Table 4.6 with 300 A module

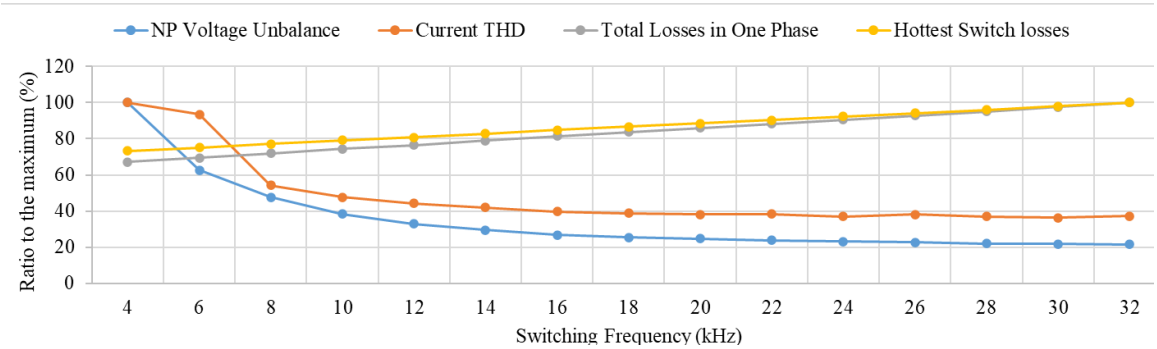
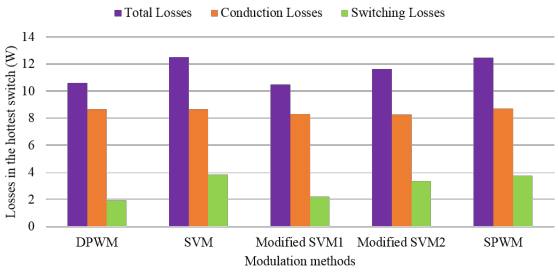
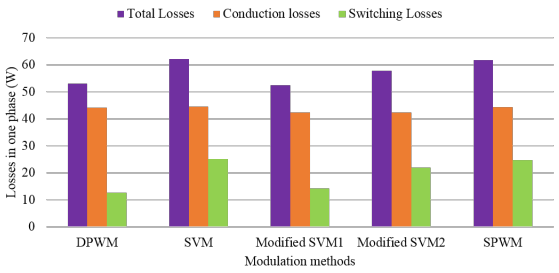


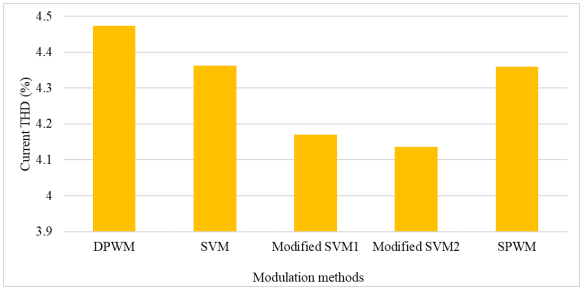
Figure 4-14: Performance of modified PWM method 1 in different switching frequencies and operating condition of Table 4.6 with 300 A module. Results are shown in ratio to the maximum measured value.



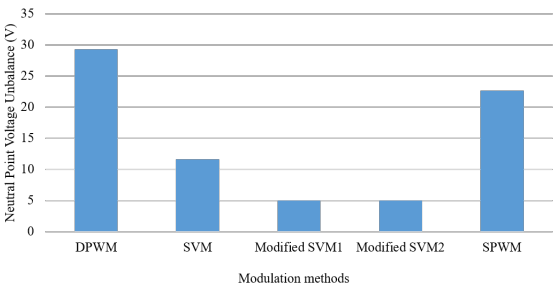
(a) Losses in the hottest switch in a phase



(b) Total Losses



(c) Current THD (%)



(d) Neutral point voltage unbalance (V)

Figure 4-15: Comparison of different modulation methods in a three-level converter running as an inverter with the operating condition of Table 4.6 with 50 A module

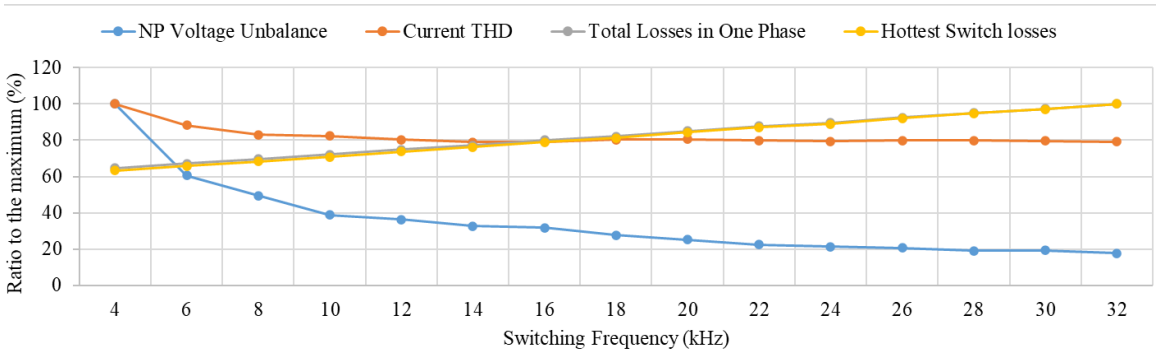
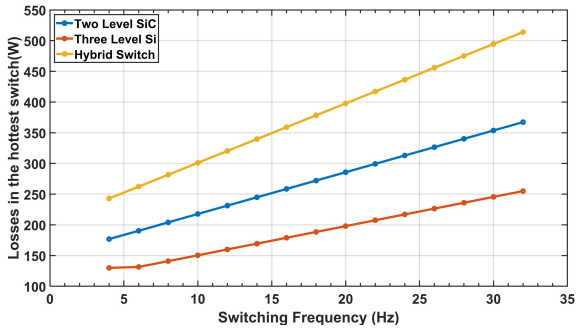


Figure 4-16: Performance of modified PWM method 1 in different switching frequencies and operating condition of Table 4.6 with 50 A module. Results are shown in ratio to the maximum measured value.

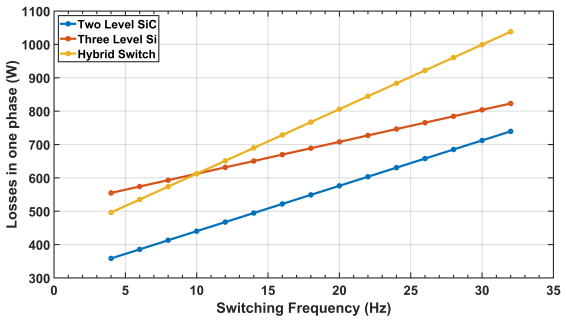
Dominant losses in upper diode is conduction losses whereas in IGBT it is switching losses. This results show that for 200 hp rating, it might be beneficial to use a hybrid module with SiC diodes in main switches to avoid reverse recovery losses. In 25 hp, the dominant factor in SiC converter total losses is conduction loss whereas in Si converter it is switching losses.

Table 4.7: Sample case converter ratings for comparison of losses in a three level and two level converter

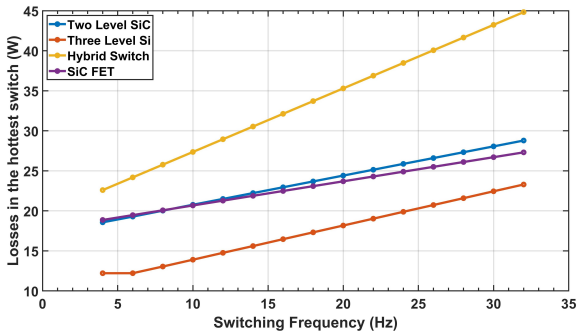
Converter 1 Parameters	Value
Nominal power (hp)	200
Output RMS current (A)	186
Output frequency (Hz)	60
Power factor	0.99
Modulation index	1
DC voltage (V)	650
Modulation Method	SVM
600 V IGBT Module	FD300R06KE3
1200 V SiC Module	CAS300M12BM2
1200 V Hybrid Power Module	SKiiP38GB12F4V19
Converter 2 Parameters	**Value**
Nominal power (hp)	25
Output RMS current (A)	22
Output frequency (Hz)	60
Power factor	0.99
Modulation index	1
DC voltage (V)	650
Modulation Method	SVM
600 V IGBT Module	F3L50R06W1E3
1200 V SiC MOSFET	CCS050M12CM2
1200 V Hybrid Power Module	SKiiP25AC12F4V19
1200 V SiC FET	UJ3C120040K3S



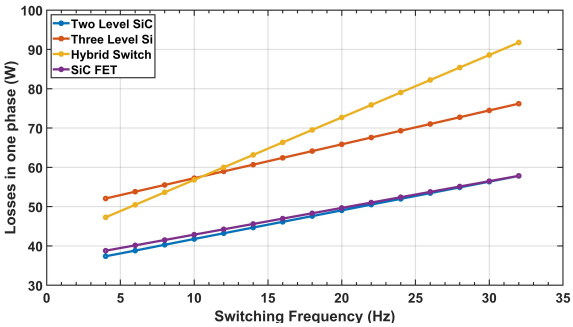
(a) Losses in the hottest switch in a phase with 300 A modules



(b) Total Losses of one phase with 300 A modules



(c) Losses in the hottest switch in a phase with 50 A modules



(d) Total Losses of one phase with 50 A modules

Figure 4-17: Comparison of losses in a SiC two-level and Si three-level converter for the operating condition of Table 4.7

4.3 Thermal characterization of SiC modules

Thermal transient models are provided in the datasheets. However, these models are not accurate as they do not consider the thermal impedance between diodes and MOSFET [61]. There are a lot of complicated networks proposed in the literature such as [62] and [63] for modeling the thermal behavior of IGBT modules. However, there are mostly difficult to be tuned to the measurements and being practically used. In this work, an impedance network is considered between the diode and MOSFET to find the junction temperatures for the 300 A SiC MOSFET module. A test setup with an open module and an IR camera is used to validate the thermal model. Thermocouples were used for measuring case temperature. IR cameras were used for junction temperature measurement because it is more reliable to measure the junction temperature using thermal cameras compared to mounting thermocouples on semiconductor dies. Installing thermocouples on the junction chips can damage the insulation and cause the failure of the module. As the module is rated at 1200 V, open module switches need gels to insulate the chips. The gel will add time delay to the measurements and therefore the measured temperature will be averaged over time. As a result, measurement of instantaneous peak temperature is impossible for AC operation using an IR camera. Therefore, it is necessary to run the inverter in different AC and DC conditions according to [64] to derive the thermal impedances. Different output frequencies must be tested to verify the thermal model. Also, to find the temperature swing in AC condition, it is necessary to run the inverter at DC conditions as well.

The test set up is shown in Fig. 4-18. The first step to find the thermal characteristics of the modules, is to run the double pulse test at the test setup for finding switching losses. The results for this test is different with the datasheet which can be explained from the fact that the stray inductances are higher in this setup due to the long distance between the open modules and the laminated DC bus bar. Although film capacitors have been used to lower the inductance from DC bus bar to the modules, the stray inductance still can be noticeable.

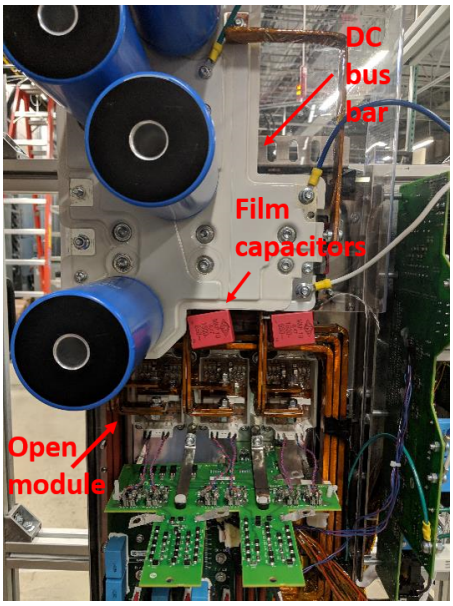


Figure 4-18: Test setup for deriving thermal models of the SiC module

An RC network along with a resistance between the diode junction and MOSFET losses has been considered. This thermal model is shown in Fig. 4-19. The equations that will determine

MOSFET and diode junction temperature are presented in (4.20). Only average diode losses and temperature is accounted for here. $T_{net}(t)$ represents the change of MOSFET junction temperature over time and includes a network of series RC network. Total losses of all switches that are mounted on the heat sink is P_{tot} and R_H is found from testing similar heat sinks with known modules and measuring the case temperature.

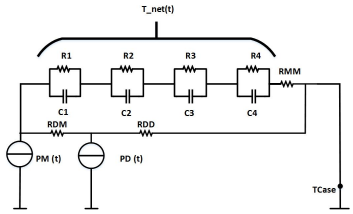


Figure 4-19: Thermal model considered for the SiC module

$$
\begin{aligned}
&T_{jM}(t) = T_{net}(t) + R_{MM}\,P_M(t) + R_{DM}\,P_D + T_{case}\\
&T_{net}(t) = T_1 + T_2 + T_3 + T_4\\
&C1\,\frac{dT_1}{dt} + \frac{T_1}{R1} = P_M(t)\\
&C2\,\frac{dT_2}{dt} + \frac{T_2}{R2} = P_M(t)\\
&C3\,\frac{dT_3}{dt} + \frac{T_3}{R3} = P_M(t)\\
&C4\,\frac{dT_4}{dt} + \frac{T_4}{R4} = P_M(t)\\
&T_{jD} = R_{DD}\,P_D + R_{DM}\,P_{M,av} + T_{case}\\
&T_{case} = R_H\,P_{tot}
\end{aligned}
\tag{4.20}
$$

The algorithm used here to find the thermal model parameters follows some rules that can be summarized as:

- The RC network used in this model should match with the transient thermal model presented in the datasheet. Multiple points from this transient model have been selected and presented in Table 4.8. These points are used to match with the calculated ones.
- The converter has been run in different AC conditions which the output fundamental frequency is varied. The average junction temperature is measured for both the diode and MOSFET ($\overline{T_{jM}}$ and $\overline{T_{jD}}$). The average calculated temperature for these operating conditions must match with measurements of Table 4.9.
- The converter is run at DC condition. In this condition, the average junction temperature is equal to maximum junction temperature. This measurement must match with the calculated values presented in Table 4.8 as well.

To minimize the error between measurements and calculation, genetic algorithm is used. Table 4.10 shows the optimization algorithm results.

4.4 Thermal performance comparison of three-level and two-level converters

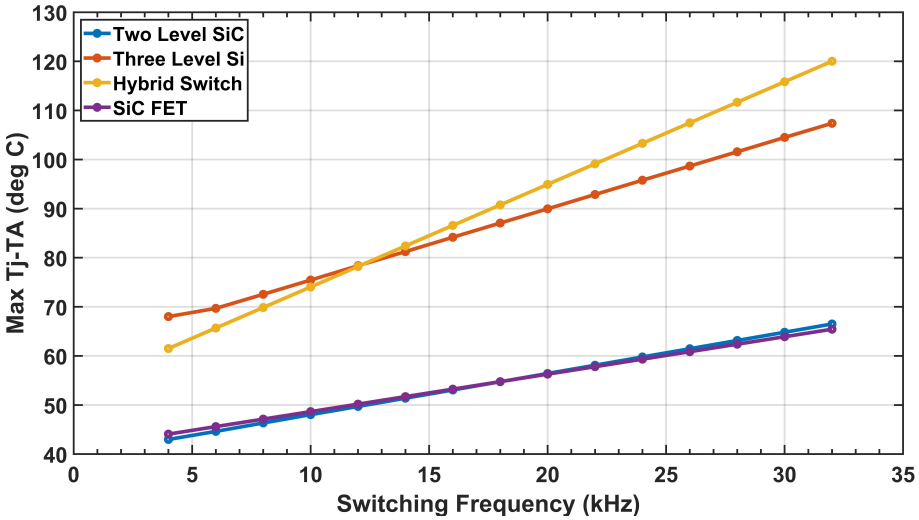
Fig. 4-20 shows the variation of maximum junction temperature versus frequency for the 200 hp converter of Table 4.7. It can be seen that the two level SiC converter is capable of working at high currents and high switching frequency. However, higher switching frequencies are needed in SiC two level converter for the same values of LCL filter in a three level converter. Based on Fig. 3-10 a 16 kHz SiC AFE converter with 22 A rated current needs a converter side inductance equivalent to an 8 kHz three level Si converter with the same current rating. The junction temperature of the modules are approximately equal for these two switchig frequencies. This can prove that a three level Si converter can have the same performance as a two level SiC converter. Table 4.11 summarizes this comparison.

Table 4.8: Data points derived from the transient thermal graph of CAS300M12BM2 datasheet

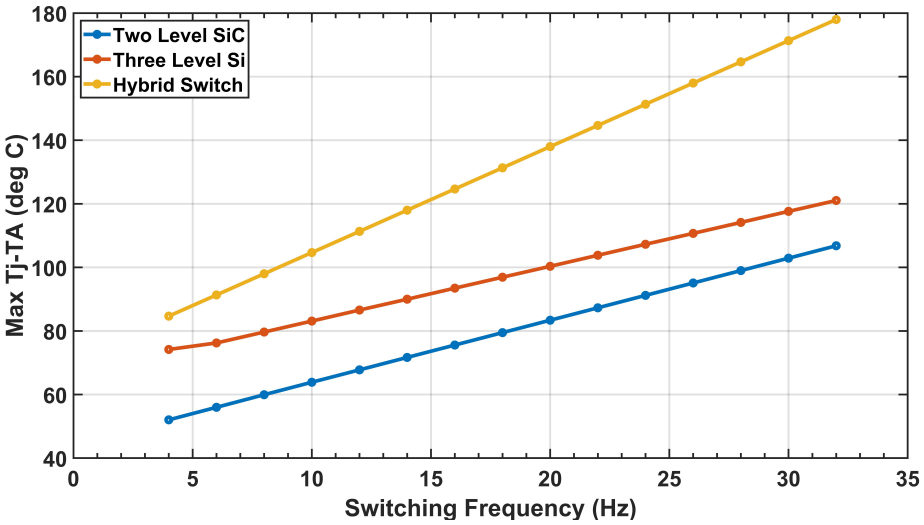
Time (s)	Impedance ($\frac{^\circ C}{W}$)
1e-6	80e-6
10e-6	550e-6
100e-6	2.5e-3
1e-3	8e-3
10e-3	27e-3
100e-3	53e-3
0.6	68e-3

Table 4.9: Measured junction temperature at different fundamental output frequencies, output current of 186 A, DC bus voltage of 650 V and power factor of 0.63. Normal space vector modulation is used.

f (Hz)	f_{sw} (kHz)	Measured $\overline{T_{jM}}(t) - T_{case}$ $^\circ C$	Measured $\overline{T_{jD}}(t) - T_{case}$ $^\circ C$
45	12	22.6	11.6
30	12	21.1	10.8
15	12	20.6	10.6
10	12	22	11.6
5	4	15.2	7.5
0	12	50	31.2



(a) Junction temperature rise to ambient temperature with 22 A output current



(b) Junction temperature rise to ambient temperature with 186 A output current

Figure 4-20: Maximum junction temperature for the two converters of Table 4.7

Table 4.10: Optimization algorithm results for deriving the transient thermal model of CAS300M12BM2 based on Fig. 4-19

R1	0.0252
R2	0.0008
R3	0.0349
R4	0.0071
C1	0.1764
C2	0.3638
C3	1.8911
C4	9.7110
R_{MD} ($\frac{^\circ C}{W}$)	0.0564
R_{MM}($\frac{^\circ C}{W}$)	6.2381e-08
R_{DD} ($\frac{^\circ C}{W}$)	0.0404

Table 4.11: Comparison of three-level and two-level converter losses and converter side inductance for a 480V, 22A AFE

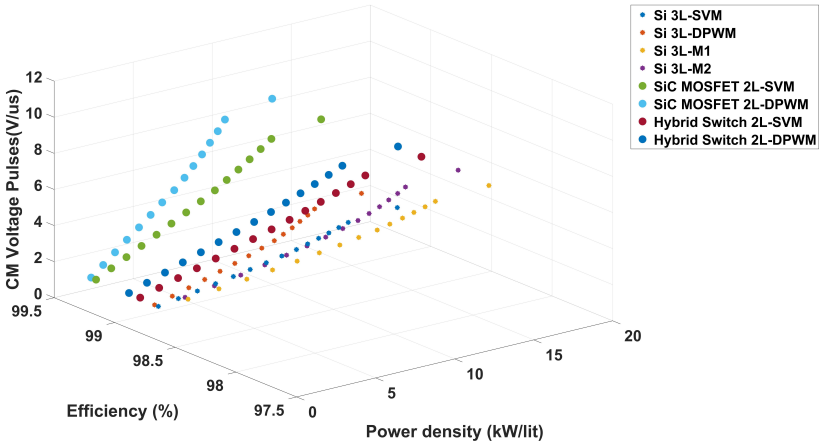
Module	fPWM	Levels	Maximum Tj-Tamb (C)	L_{conv} (%)
600 V F3L50R06W1E3-B11	8 kHz	3	72.5	2.5
1200 V CCS050M12CM2	16 kHz	2	53.1	2.5

4.5 Conclusion

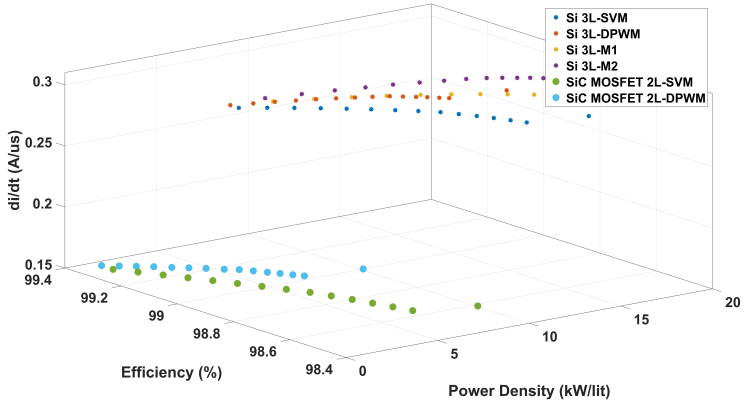
The optimization process of converters was broken into LCL filter size comparison and converter losses. Now, the results from these two blocks can now be integrated and an integrated and vigorous comparison is possible. Fig. 4-21 and 4-22 present the comparison results for a 25 hp and a 200 hp converter. Losses consist of inductor losses and switching and conduction losses. Volume and power density include the power module size, LCL filter size, heat sink, gate drives, precharge and protection circuit.

Common mode voltage pulses, dvdt and didt are presented as a guide for selecting between converters. However, the final EMI performance of the converter can be dependent on detailed design factors. Power density is higher for 200 hp designs. The three-level converter provides the highest power density whereas SiC two-level converters have the highest efficiency. Fig. 4-23 shows the comparison between calculated power density and inductors losses from [2] and this work results. Because of the optimized inductor design in this work, resulted power density is higher.

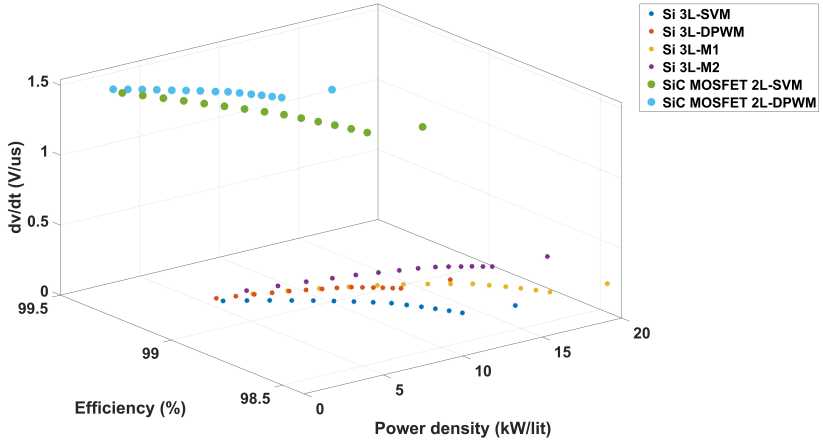
Table 4.12 shows the comparison between this work's results and literature. The references mentioned in this table are related to Power Factor Correction (PFC) converters which has an extra stage compared to AFE converters and are used for a power less than 1 kW.



(a) Common mode voltage steps comparison between different design space parameters

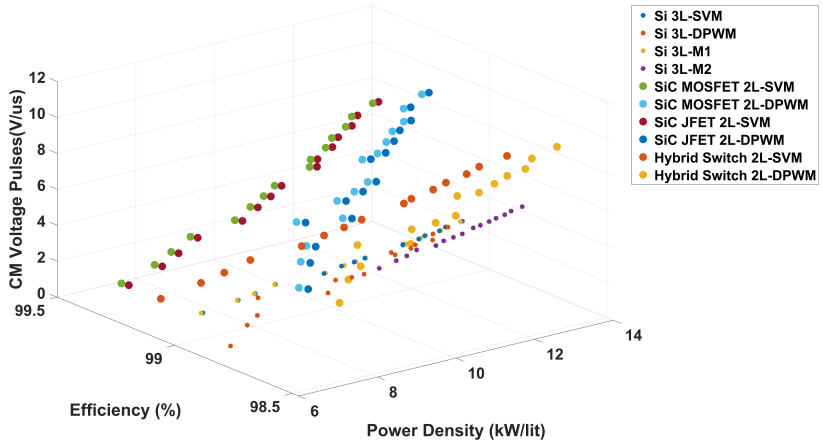


(b) di/dt comparison between different design space parameters

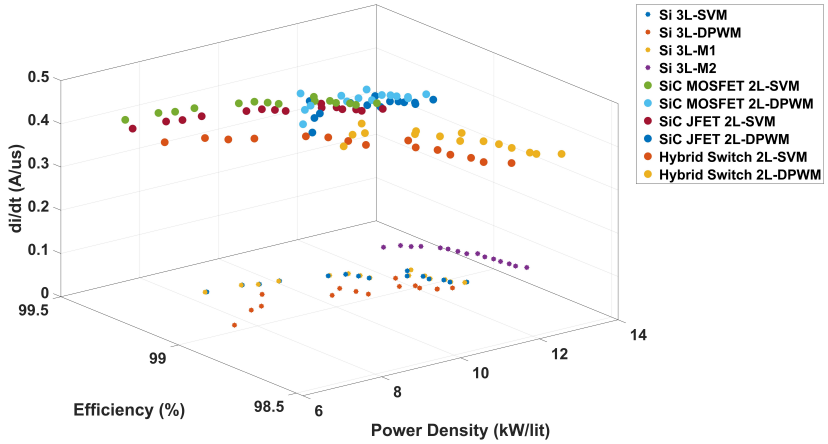


(c) dv/dt comparison between different design space parameters

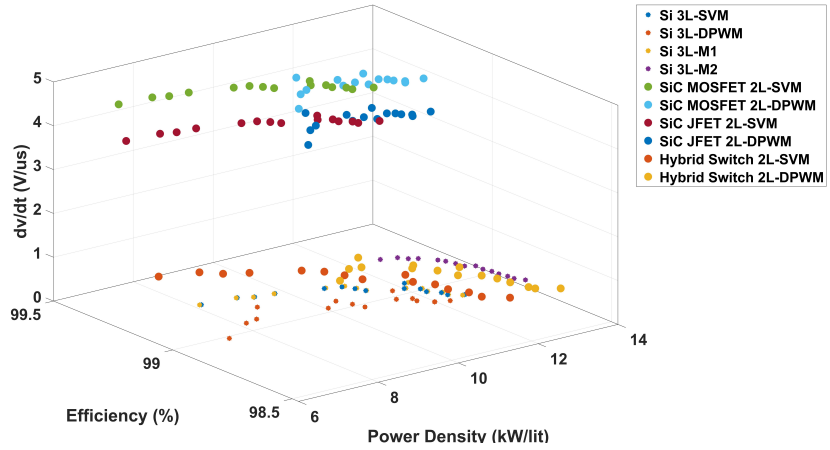
Figure 4-21: Final comparison between different topologies and semiconductor types from EMI performance standpoint for 200 hp design



(a) Common mode voltage steps comparison between different design space parameters



(b) di/dt comparison between different design space parameters



(c) dv/dt comparison between different design space parameters

Figure 4-22: Final comparison between different topologies and semiconductor types from EMI performance standpoint for 25 hp AFE design

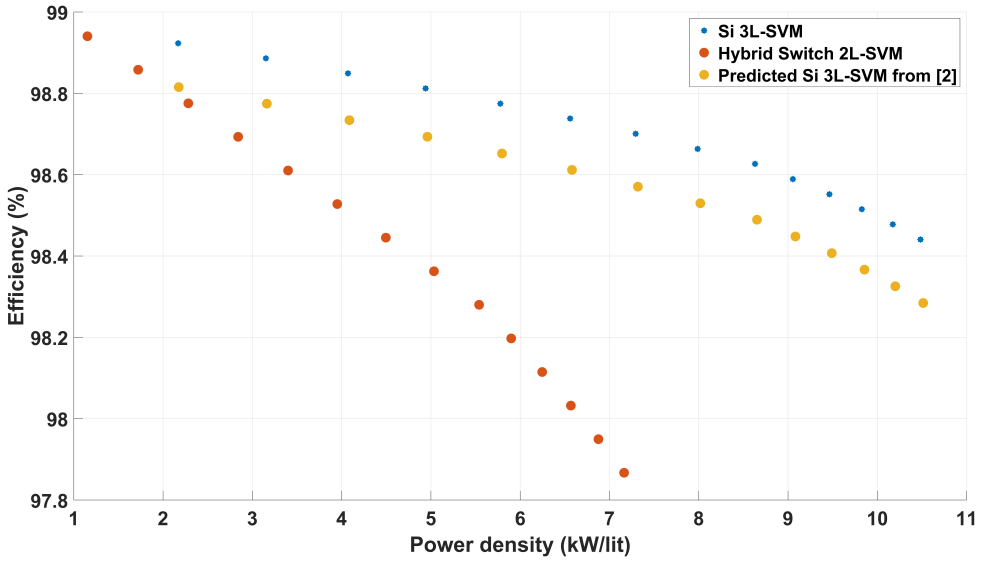


Figure 4-23: Comparison of the ratio between two-level and three-level converter power densities from and this work for the 200 hp converter

Table 4.12: Comparison of this work and previous works in the literature. The design in this work is based on an industrial products which have passed the required insulation and electrical safety tests; however, the rest of designs for PFC converters are new developed designs that have not been through standards tests.

References	Topology	Power (kW)	Effi-ciency	Power Density (kW/lit)	Includes EMI filter and energy buffer	Includes controller and heatsink
This work	Three-level NPC	154.21	98.71	16.20	No	Yes
This work	Three-level NPC	18.29	98.74	13.32	No	Yes
[65]	7L Flying capacitor	1.5	98.52 %	29.90	No	No
[66]	interleaved MHz triangular current mode totem-pole bridgeless	1.2	98.7%	13.42	No	No
[67]	interleaved boost	0.31	96.6%	5.79	Yes	Yes
[68]	triangular current mode totem-pole bridgeless	3	98.3%	5	Yes	Yes
[69]	diode-clamped 3-level boost	3	97.9 %	1.57	Yes	Yes

Chapter 5

Special applications of multilevel converters

In this chapter, a special application of three-level converters is investigated. Low speed operation of inverters can cause high maximum temperature that results in the necessity of over rating design of power modules. Operation of converters at low frequencies can have worse results than the DC output due to the high temperature ripple. Temperature ripple can stress the bond wires and chips. This chapter investigates the possibility of using three-level converters for lowering losses and distributing the losses between the power semiconductors. First, as an introduction, different modulation methods of three-level converters are reviewed. Then a new modulation method is proposed that can help mitigate the problems resulting from operation of drives in low output speed.

5.1 Modulation methods of three-level converters

Different modulation strategies for three-level converters including level shifted sinusoidal PWM and space vector based modulation (SVM) were introduced in Chapter 1. SPWM is easy to implement but it has inferior performance compared to SVM. SVM has more control freedom and is more suitable for high frequency applications. Fig. 5-9 shows the available space vectors of a three-level converter. These vectors are divided into three different types of zero, short, medium and long. Short and zero vectors have redundant switching states. The calculation of SVM duty cycle in this work is based on the g-h coordinate [70] and division of the space diagram to triangular divisions [1].

Selection of short vector can change the neutral point voltage, common mode (CM) voltage and losses. The steady state neutral point (NP) balance is essential in the operation of the converter. Therefore the primary goal is to keep the neutral point voltage as close as possible to the zero. This voltage is defined as the difference between the upper and lower capacitor voltages. Small vectors and medium voltages change the neutral point voltages. Focusing on the voltage vector of Fig. 5-9, Fig. 5-2 shows the effect of different possible short vectors on the NP voltage. For neutral point balancing one possible method can be alternating between the two possible short vectors in a switching cycle. For example if d_1 the switching duration for the first pair of short vectors (POO and OON), we can choose POO for $d_1\, T_s/2$ and OON for the other half of the duration. This way, the NP balances naturally but the main problem with this method is that the switching losses increases as the number of switching will increase. If we limit the number of switching states, obviously less switching will happen. The advantage of this method is that it does not need measurement of current and NP voltage. The other method is based on measuring the NP voltage and phase currents. If the

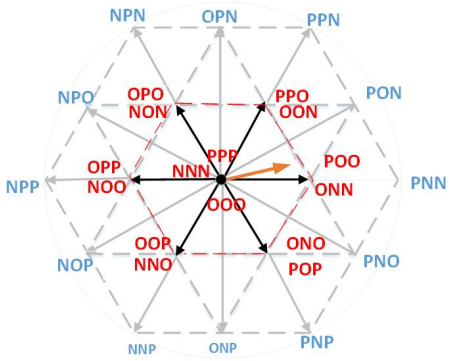
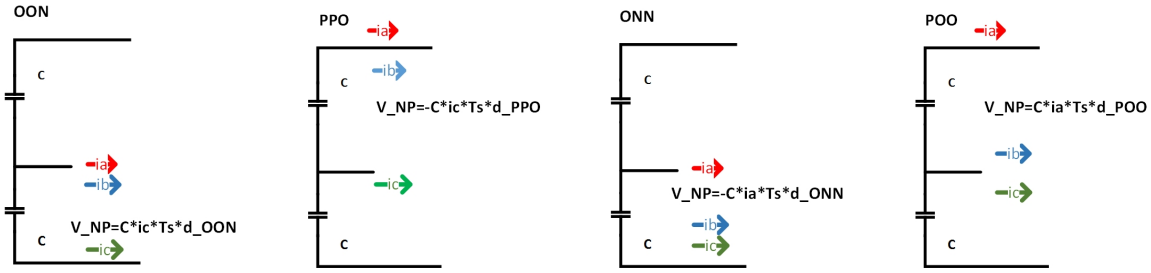


Figure 5-1: Space vector diagram for a three-level converter

NP voltage is negative, the switching states that will make it positive will be chosen.



(a) OON (b) PPO (c) ONN (d) POO

Figure 5-2: Short vector effects on NP

Losses can be affected by short and zero vectors. The selection and alignment of switching states in a switching period changes the losses significantly. In [1], in the sections with the possibility of two pairs of short vector selection (the stared area in Fig. 5-3), one of the short vectors is selected to balance the NP voltage and the other one is chosen for minimizing the losses. The sequence of different pulses is based on the previous pulse so that the transition from the previous pulse to the next one does not make extra losses. There are no specific rules given in [1] for selecting zero vector. However, two rules are necessary to follow in selection of switching states. First is that, two phases should not switch at the same time because it makes the dead time compensation complicated. Second, the transition in every phase should never be from positive to negative rail or vice versa. Considering these rules, the zero vector selection will be limited but still it needs more selection criteria to find the best modulation sequence. Losses can be lowered if switching is stopped for the phase with highest current. This method is discontinuous PWM where the phase with highest current is clamped to positive or negative voltage (nearest voltage value). For unity power factor, Fig. 5-4 shows the reference voltage value of the converter with sinusoidal PWM. It should be noted that DPWM is more effective for power factor values that are close to unity [1]. This idea can be used for choosing zero space vectors and basically for low modulation index values. This method which is modified method of [1] is referred as normal SVM in this work.

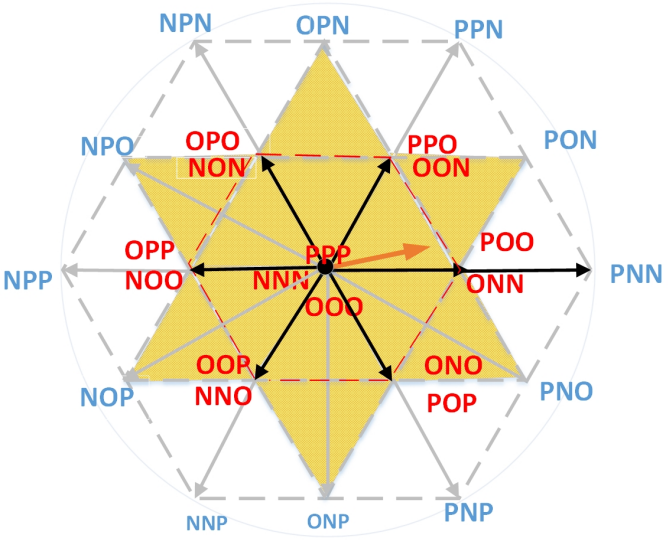


Figure 5-3: Space vector diagram for a three-level converter where sections with possibility of four short vector switching states are stared.

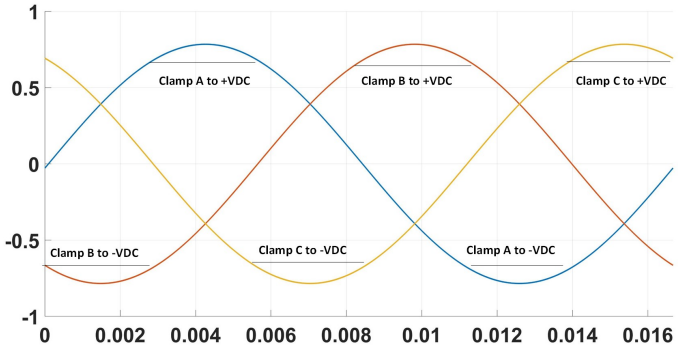


Figure 5-4: DPWM reference voltage with unity power factor

5.2 Thermal cycling of three-level inverters for low speed operation

Voltage-source inverters for AC motor drives have an inherent short-coming for generating full torque at low output frequency. Low output frequency means low modulation index and low motor speed in V/Hz operation. If the output fundamental time period is comparable to the time constants of power modules, there will be considerable swing in the junction temperature and the peak temperature will correspond to the peak power dissipation rather than the average. Peak junction temperature will limit the maximum output current whereas the swing in junction temperature (power cycling) will reduce the life of the power module [71].

Various solutions have been proposed to decrease the high junction temperature of low operation frequency. The most common one is dropping switching frequency which will reduce switching losses but it will remove all the benefits of high switching frequency causing audible noise from motors and motor ripple (especially motors designed for high PWM frequency). Control update rates are reduced as well (typically control runs at two times PWM frequency for synchronous sampling).

Reducing DC bus voltage at low speed is another option which can reduce the switching losses.

However, the bandwidth of control can be affected significantly as the DC bus has high capacitance and voltage takes a long time to change. Also, this method needs an AC/DC buck-boost converter and one stage of active front end or DC rectifier cannot be used for this method.

Modified PWM techniques can also solve the problem. A zero vector modulation method (ZVM) has been proposed in [72] where zero vectors are altered periodically to distribute the losses among the inverter switches in the phase leg carrying the largest current in a two level converter. This method will be analyzed in details in this paper.

Three level converters can also be used to improve the loss distribution between current carrying modules. In this paper, a modified modulation technique for three-level NPC converters are developed to reduce peak temperature and temperature swing of power modules at low output frequency.

The results of using the three level topology with this modulation method is compared with a two level SiC converter. It has been shown that three-level converter can help solving the temperature swing in low speed operation with similar results to the SiC converter.

5.3 Two-level converters and low speed operation

In ZVM, peak temperature reduction is achieved by trading-off conduction losses for switching losses; therefore, the effectiveness of the method depends on module type, switching frequency and operating frequency [29]. Temperature oscillations of an IGBT module (FF300R12KT3) and a SiC MOSFET (CAS300M12BM2) for the operating conditions of 16 kHz, 150 A, 650 V DC are presented in Fig. 5-5 and 5-6.

The transient thermal impedance of modules for power cycling has been used to find the temperature oscillations. The heat sink has been modeled as a thermal resistor with the value of 0.1845 $\frac{^\circ C}{W}$.

These models do not consider the coupling between diodes and modules and different modules and that can change the accuracy of temperature estimation [61]. In DC operation, the instantaneous losses are constant over time and therefore the junction temperature only depends on the thermal resistance of the module and no transient thermal model is needed. With increasing the output fundamental frequency from zero to 0.5 Hz, the junction temperature increases.

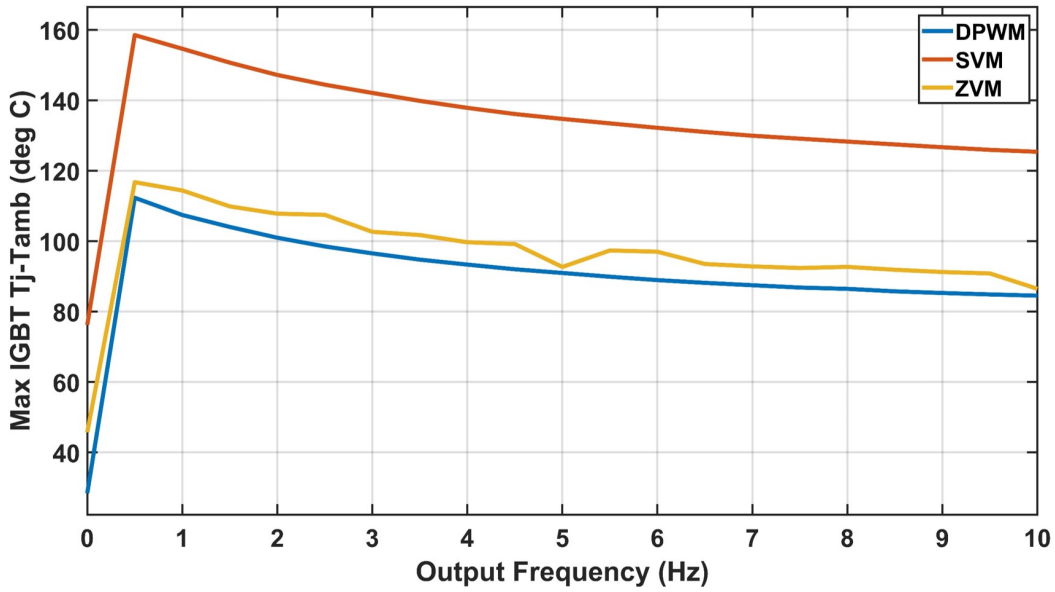
The longer fundamental period of 0.5 Hz compared to higher frequencies will cause the transient thermal model to respond to the peak instantaneous losses. In higher fundamental frequencies such as 45 Hz the peak junction temperature is more dependent on the average losses than instantaneous peak losses. Fig. 5-5 shows the variation of junction temperature based on output fundamental frequency. It can be seen that the peak junction temperature happens in 0.5 Hz fundamental frequency.

ZVM can reduce the maximum junction temperature in DC operation but for higher fundamental frequencies, is only effective for specific range of power factor values. As it can be seen in Fig. 5-6, ZVM is effective in the IGBT module for the power factor values smaller than 0.5 and in the SiC module it can be advantageous for power factors higher than 0.85.

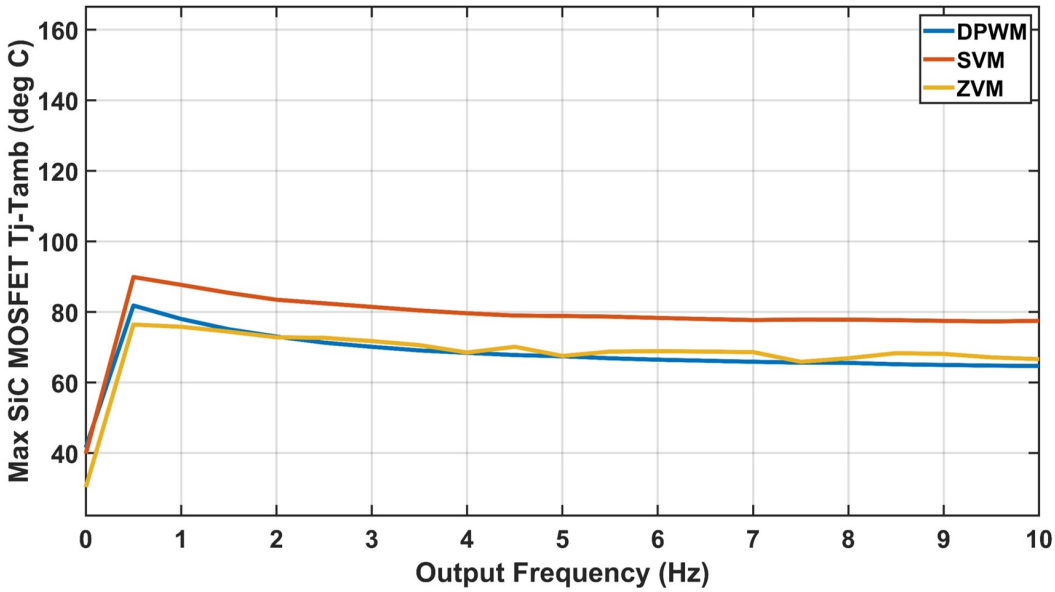
ZVM is more advantageous for modules with low switching losses as the comparison of Fig. 5-5(b) and 5-6(a) shows. ZVM increases the switching losses to lower the conduction losses in upper switch conduction. Therefore it is more effective in the SiC module because of lower switching losses in this type of switch.

The other important point about ZVM is that ZVM frequency must be selected based on the thermal time constants of the module. Fig. 5-7 shows the junction temperature variation with ZVM frequency change. The relation between ZVM frequency and junction temperature is not linear and therefore for each operating condition optimal ZVM frequency must be selected based on the module transient thermal model. It can be concluded that the maximum temperature values may not

improve noticeably using a ZVM method and the effectiveness of ZVM depends on various factors including output fundamental frequency and power factor.

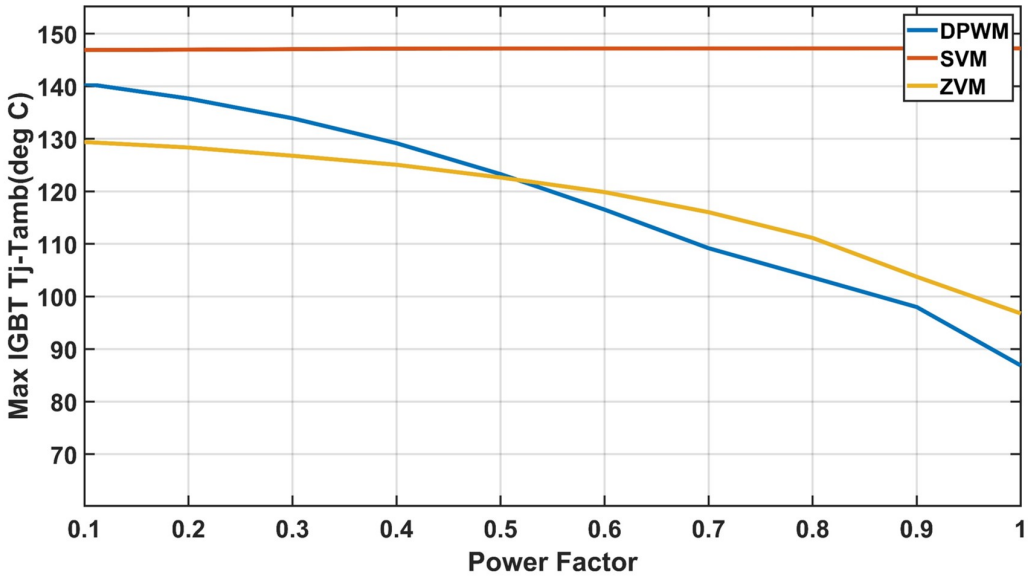


(a) Two-level Si converter maximum junction temperature

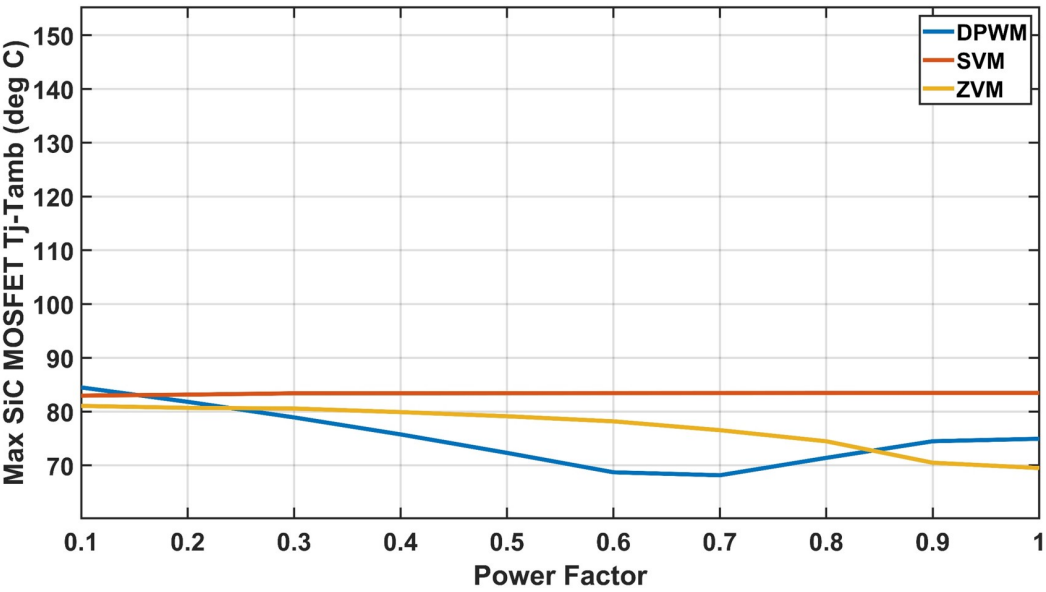


(b) Two-level SiC converter maximum junction temperature

Figure 5-5: Junction temperature variation for different modulation methods and output frequencies with $f_{ZVM} = 100\,Hz$. The fundamental frequency is changed in steps of 0.5 Hz.



(a) Maximum junction temperature variance for different power factor values in a two-level Si converter with 2 Hz fundamental frequency



(b) Maximum junction temperature variance for different power factor values in a two-level SiC converter with 2 Hz fundamental frequency

Figure 5-6: Junction temperature variation for different modulation methods and power factor values with $f_{ZVM} = 100\,Hz$

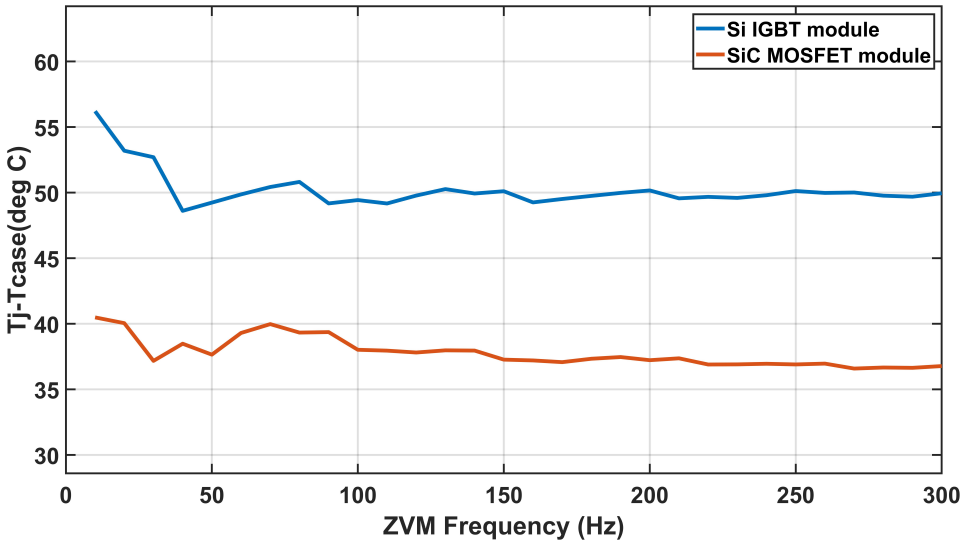


Figure 5-7: Junction temperature variation for a two-level converter with different ZVM frequencies and module types

5.4 Three-level converters and low speed operation

Three-level converters can be used for the loss distribution between the switches of a leg. Different modulation methods have been proposed in [72–75]. They can result in higher effective harmonic contents and therefore result in smaller filters. Yet, a general modulation method that can work for low speed operation and not just DC output voltage is missing. This modulation method needs to have halfwave symmetry and avoid switching of multiple phases at a time.

A modulation method for voltage-dip ride-through in grid-connected converters is introduced in [76] which removing of certain zero vector options has been proposed. The modulation methods are not half-wave symmetrical which will result in a poor harmonic performance. Also the paper concentrates on zero power factor which is not the case for inverter applications.

ZVM for three-level converters has been introduced in [74] where the three-level converter is switched like a two-level converter and redundant short vectors are not used so it is the same as ZVM introduced in [72].

A modulation scheme has been proposed in [75] where switching sequences are shown to vary conduction and switching losses to balance temperature. However switching of two phases at a time happen consecutively which can result in unpredictable states regarding dead-times .Also all the modulation schemes are designed for DC operation which does not happen in drives applications.

Considering the space vector diagram of a three-level converter, as the modulation index is very low in low speed in volt/hertz operation, the voltage will stay inside the circle that short vectors inscribe. For having lowest conduction losses the zero vector that transfers the current to the other switch in the leg can be used.

For example for $PF = 1$, the phase with highest current at -30° to 30° is phase A and in DPWM for lowest switching losses, this switch is clamped to $+VDC$ [1]. However, as d0 is almost 1 in low speed operation, for lowest conduction losses this phase can be clamped to $-VDC$ in a three-level converter for zero vector. The ZVM method actually uses this method where this act is done periodically. This modulation method is named M2 in this paper.

For avoiding switching losses, the phase with highest current can be clamped to O. For $0 <$

Table 5.1: Modulation schemes that can be used for $0 < \omega t < 30^\circ$ and unity power factor

Modulation methods	Upper Switch1		Upper Switch2	
	P_{Cond}	P_{SW}	P_{Cond}	P_{SW}
M1	*	0	*	0
M2	0	0	0	*
M3	0	0	*	0
M4	0	*	*	0

$\omega t < 30^\circ$ where the phase A current is at the highest of all phases current, Fig. 5-5 shows DPWM (Clamping phase A to $+VDC$ and all other possible modulation schemes.

To distribute losses equally in the switches of an NPC and also avoid the high peak temperature, two approaches can be taken. One can be calculating losses for all possible switching sequences of Fig. 5-8 and find the optimal one for a switching period and the other one can be finding losses for the whole 360° of conduction. Comparison of losses for one switching cycle is not based on constant current value for one fundamental frequency period but it does not result in the optimal losses values for the whole fundamental period.

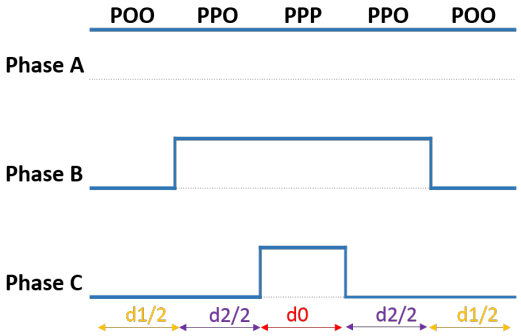
The fundamental frequency period can be simplified to calculate the losses in less than 360° of conduction and predicting it for the whole fundamental period. Assuming a power factor close to unity, the space vector diagram can be divided to the areas that the current is at its absolute maximum value following DPWM method. For example phase A has the highest absolute current value at $-30^\circ < \theta < 30^\circ$ and phase C has the highest absolute current value at $+30^\circ < \theta < 90^\circ$. If the algorithm for finding the switching sequence results in clamping phase A to +DC at $-30^\circ < \theta < 30^\circ$, it is reasonable to clamp phase C to -DC at $+30^\circ < \theta < 90^\circ$. To explain this better, assume number 1 is assigned to P (+DC), -1 is assigned to (-DC) and zero is equal to mid point (O). Summing these numbers possible options for each vector can vary from -3 to +3. For example, POO will be equal to +1 and NOO will be equal to -1. Multiplying the vector numbers found for $-30^\circ < \theta < 30^\circ$ by -1, can give the best vectors for $30^\circ < \theta < 90^\circ$. If M1 is chosen for $0 < \theta < 30^\circ$, then multiplying 1, 2 ,3, 2, 1 by -1 results in -3,-2, -1, -2, -3 for $30^\circ < \theta < 60^\circ$ which is equal to M2 and clamps phase C to -VDC.

With these simplifications, calculation of losses is only necessary for 60° of space vector diagram. But still loss calculation for each switching cycle for all possibilities in 60° of space vector diagram can be time consuming. For example for output frequency of 2 Hz and switching frequency of 12 kHz, 60° of conduction includes 1000 switching cycles and with 4 possible switching schemes, 4^{1000} possible switching sequences should be analyzed.

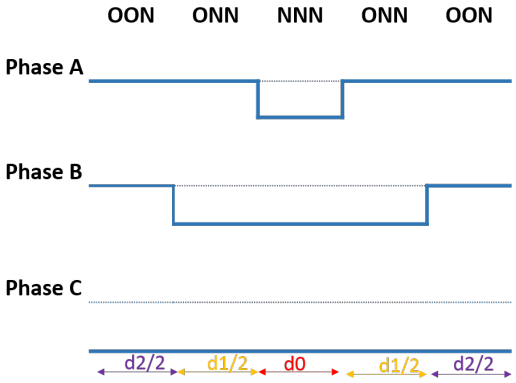
One other limitation that can lower the number of calculations is the transition between switching schemes. For example frequent transition between M1 and M2 is not possible because two phases will switch at the same time. Therefore between M1 and M2, M3 or M4 must be used.

In this work, each 60° has been divided to 4 segments as shown in Fig. 5-8 and average losses has been found for all modules and compared for all the options described in Fig. 5-8 using (5.1) and (5.2). Table 5.1 shows that which switch has losses in each modulation scheme. The losses are calculated based on having d0 equal to 1 and therefore neglecting conduction losses in dwelling time of d1 and d2.

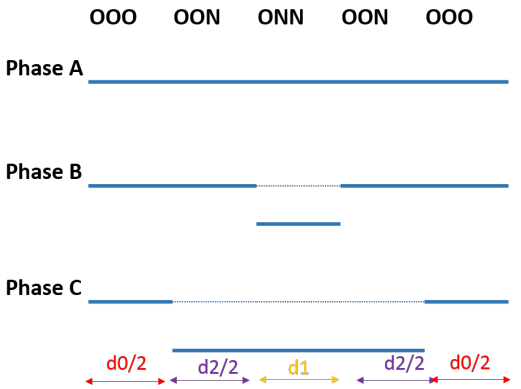
The losses is found for the whole operating period with the closed form expressions of (5.1) and (5.2). The sequences that result in a more balanced loss in all switches is selected as the final switching scheme. This algorithm is summarized in Fig. 5-10. This method needs the knowledge of the output current value and power factor beforehand. Yet, it is more flexible for different types of modules. This method is named optimal loss distribution.Table 5.2 shows the optimal switching



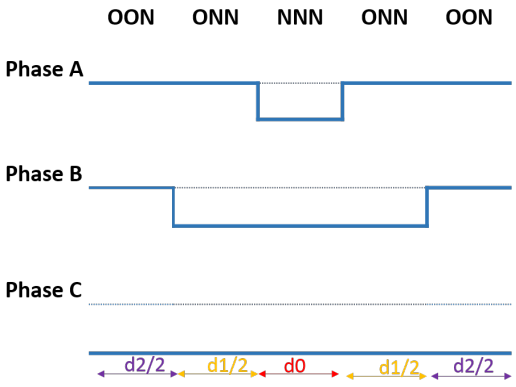
(a) Modulation method of M1 which is equivalent to DPWM (Clamping phase A to +VDC)



(b) Modulation scheme of M2 where the zero vector of NNN is used instead of PPP of DPWM



(c) Modulation method of M3 where phase A is clamped to O.



(d) Modulation method of M4 where phase C is clamped to O

Figure 5-8: Modulation schemes that can be used for $0 < \omega t < 30°$ and unity power factor

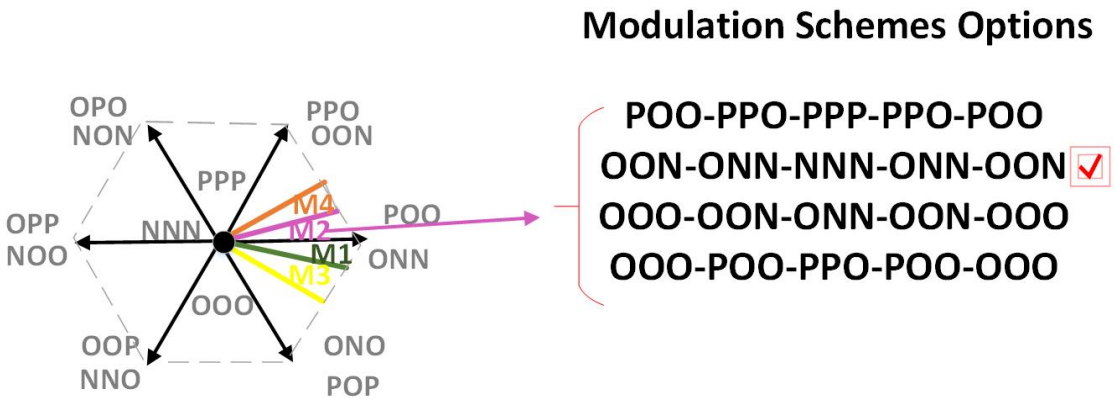


Figure 5-9: Mixture of all schemes modulation method where all the modulation options are used in the 60° of highest current period

sequence for each 15° of the conduction in space vector.

$$P_{cond,IGBT} = \frac{1}{2\pi}\int_0^{15^\circ} (V_{0,IGBT} + R_{ON}\, i)\, i\, d\theta \tag{5.1}$$

$$P_{sw,IGBT} = \frac{f_{PWM}}{2\pi}\int_0^{15^\circ} (E_{SW,ON} + E_{SW,OFF})\, \frac{V_{DC}}{V_{DC,r}}\, \frac{i}{I_r}\, d\theta \tag{5.2}$$

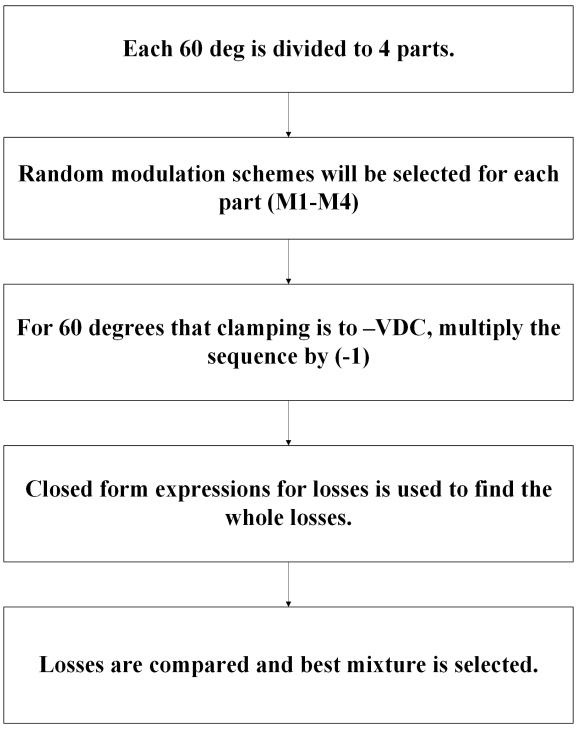


Figure 5-10: Algorithm for finding the switching sequence that results in the lowest average loss.

The other methods that has been tested in this, is the mixture of all the modulation schemes of Fig. 5-8 where for each 15° one of the four options is used for example M1-M2-M3-M4 for the whole 60° of conduction and this method is named mixture of all elements.

For one of the modules of show the power losses through upper switches for different modulation methods including level shifted sinusoidal PWM (SPWM) in an NPC converter. S2 is the the switch that has the highest peak losses.

Table 5.2: Optimal switching sequence for operating condition of and FD300R06KE3 IGBT module

conduction period	Switching sequence
$-90^\circ < \phi < -75^\circ$	-3, -2, -1, -2, -3
$-75^\circ < \phi < -60^\circ$	-3, -2, -1, -2, -3
$-60^\circ < \phi < -45^\circ$	-3, -2, -1, -2, -3
$-45^\circ < \phi < -30^\circ$	-2, -1, 0, -1, -2
$-30^\circ < \phi < -15^\circ$	1, 2, 3, 2, 1
$-15^\circ < \phi < 0^\circ$	1, 2, 3, 2, 1
$0^\circ < \phi < 15^\circ$	1, 2, 3, 2, 1
$15^\circ < \phi < 30^\circ$	0, 1, 2, 1, 0

Fig. 5-11 shows the maximum junction temperature of hottest switch (upper switches) for different modulation methods in an NPC converter with 600 V module of FD300R06KE3 and V/Hz operation in the conditions of 480 V, 2 Hz, 150 A, 16 kHz PWM frequency, power factor of 0.85, 9700 μF and 650 V DC voltage. The optimal modulation method shows the lowest maximum junction temperature.

The drawbacks of all the methods that were discussed is that they will change the neutral point voltage in three-level converters in steady state. The neutral point voltage balance is necessary to reduce the harmonics and to maintain proper function of the converter. The neutral point (NP) voltage balance for different modulation methods and the same operating conditions of Fig. 5-11 is shown in Table 5.4. It can be seen that although optimal loss distribution can result in lower junction temperature, it can cause high unbalance between the upper and lower DC bus capacitors in steady state.

Table 5.3: Steady state neutral point imbalance for different modulation methods with DC bus voltage of 650 V

Modulation method	Maximum Tj $^\circ C$	Maximum NP V (V)
DPWM	79.1	33.9
Optimal Modulation	73.5	36.1
Mixture of all schemes	82.3	38.7
SVM	85.8	3.7

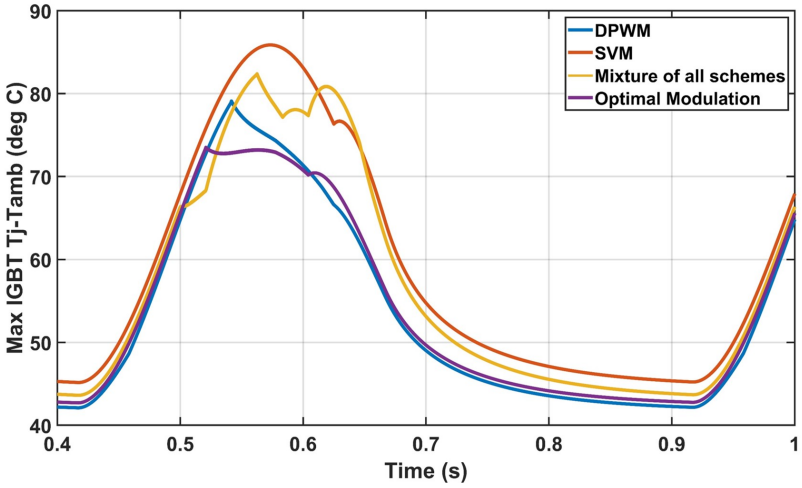


Figure 5-11: Junction temperature variation over time with different modulation methods with a 600 V switch (FD300R06KE3)

5.5 Modified methods for neutral point voltage balance

The disadvantage of all the methods that were proposed for lowering the peak junction temperature is that they will change the neutral point voltage in three-level converters. Unbalance in the neutral point voltage of a converter can cause higher THD values and losses.

It is necessary to modify the modulation schemes for neutral point voltage balance. Each of the short vectors changes the neutral point charge in a different direction [1].

Focusing on DPWM and for $0 < \omega t < 30°$ (assuming unity power factor) to avoid extra losses, two switching sequence of M1 and M3 can be used where the two subset of vectors are applied to balance the NP voltage and they smoothly connect with the succeeded vector sequence without switching two phases at a time. Altering between M1 and M3 should be done frequently. Here, a specific algorithm (5-12) has been used where the neutral voltage is measured and will affect the alteration between the two subsets. This algorithm is based on hysteresis control presented in [77].

A similar approach is implemented on the other methods to make the neutral point voltage oscillation as small as possible. 5.4 shows the neutral point voltage balance of the modified methods. Junction temperature for the hottest switches in different types of modulation methods is shown in 5-13. Mixture of all schemes is the most promising modulation scheme regarding balancing of losses and NP voltage.

Comparing 5.4 and 5.4 shows the effect of changing the switching sequence to balance the NP voltage. Temperature in the hottest switch is 37% increased to balance the NP voltage.

Table 5.4: Steady state neutral point imbalance for modified modulation methods

Modulation method	Maximum Tj $°C$	Maximum NP V (V)
DPWM	80.5	0.3
Optimal modulation	85.9	0.3
Mixture of all schemes	84.0	0.6

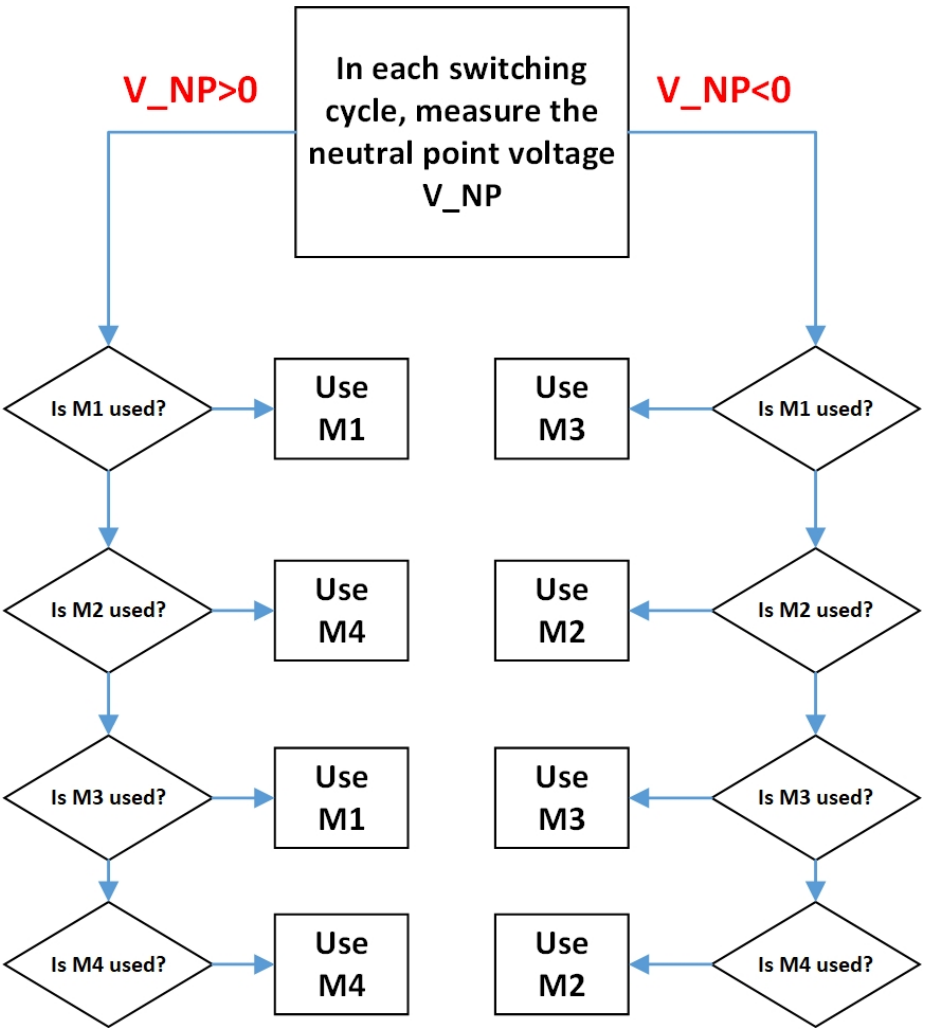


Figure 5-12: Algorithm for finding the switching sequence in modified modulation methods

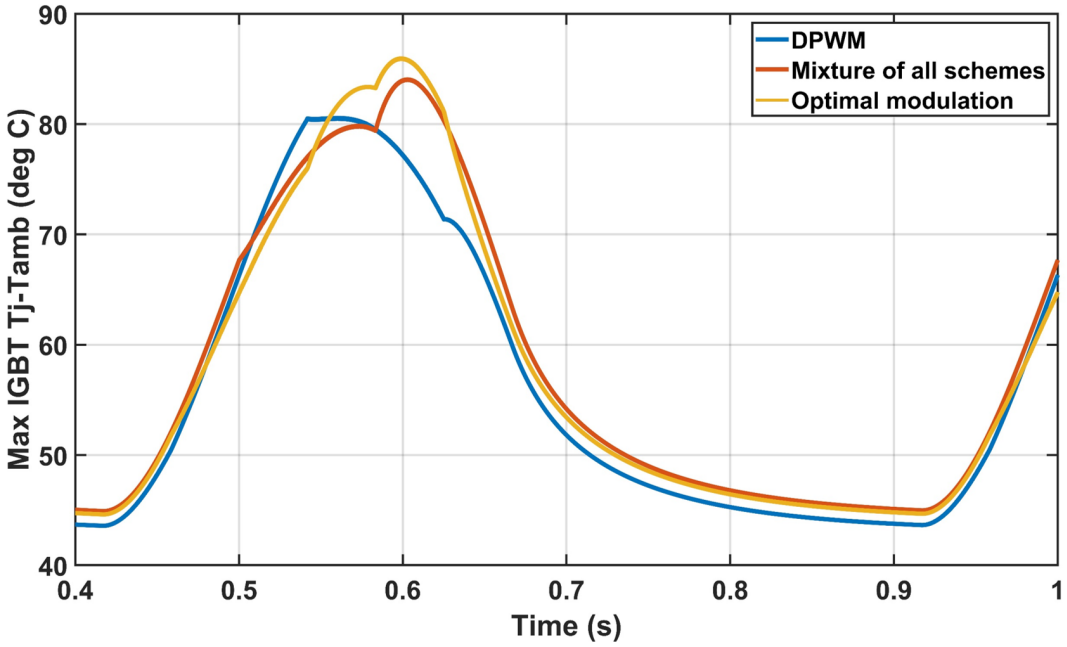


Figure 5-13: Junction temperature variation over time with different modified modulation methods with a 600 V switch (FD300R06KE3)

5.6 Implementation issues

The modulation methods that was proposed have different amount of required numerical calculations. Higher number of numerical calculations means a bigger and more costly microcontroller. Optimal modulation methods needs a full computation of losses in a fundamental period for any RMS current and power factor whereas the mixture of all modulation schemes does not need any calculations or current measurement and prediction.

Modification of modulation techniques requires either neutral point measurement feedback or knowledge of RMS current and power factor. Also it adds computation load to the system for conduct the algorithm of Fig. 5-12.

The other important issue that can cause problems in operation of converters in low speed operation with high switching frequency is dead time. A 480V, 186 A SiC inverter was run at 5 Hz output frequency. Fig. 5-15 shows the output current at different fundamental frequencies and it can be seen that the output current is distorted specially at higher switching frequencies. In higher switching frequencies, the dead time duration can be comparable to the duty cycle of the switch. Dead Time Compensation (DTC) is supposed to tackle this effect. The dead time compensation used in this inverter control is based on [78]. As this method and a lot of other similar dead time compensation algorithms [79] are based on current polarization, measurement errors, current ripples and discontinuous current conduction can disrupt the current spectrum. Assuming the current direction cannot be accurately detected for $-10 < Iout < 10$, for output frequency of 5 Hz and output current of 186 A, that means that the dead time compensation algorithm will result in arbitrary results for 2.4 ms although in the output frequency of 45 Hz that is reduced to 0.26 ms which is almost negligible. Deactivating dead time compensation can help solving this problem; however, the advantages of compensating dead time voltage loss or increase can be lost. Fig. 5-14 shows the output THD at different fundamental frequencies with and without dead time compensation. It can be seen that dead time compensation almost does not remove any of the harmonics in the voltage

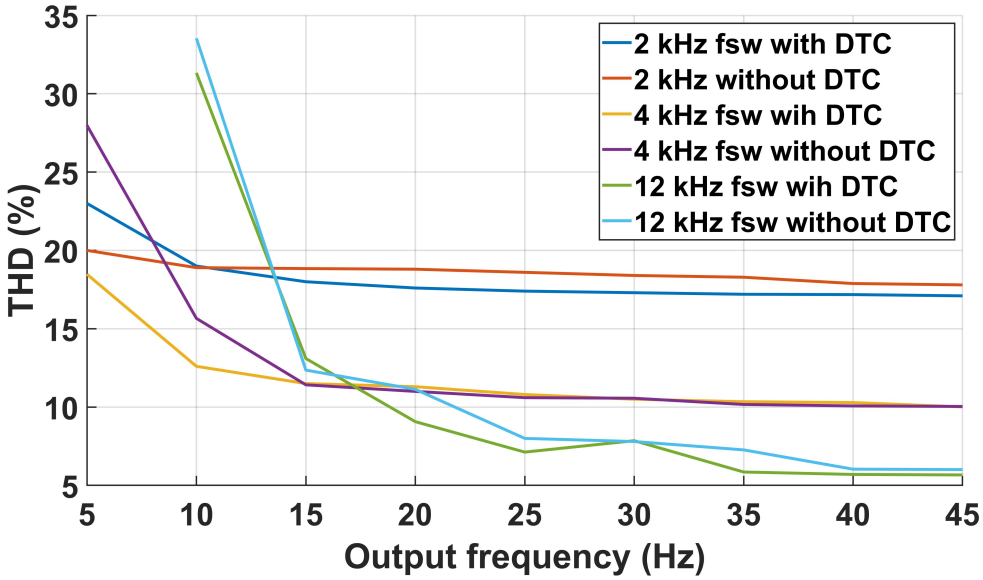


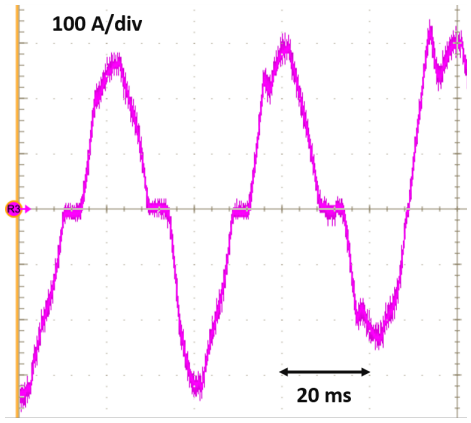
Figure 5-14: Current THD in different output frequencies

Table 5.5: The effect of output frequency on current THD

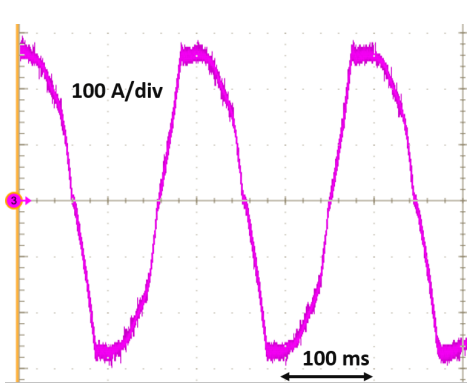
Fundamental Frequency (Hz)	Switching Frequency (kHz)	THD with dead time compensation (%)	THD without dead time compensation (%)
5	4 kHz	18	30
15	12 kHz	15	23
45	12 kHz	7	11

waveform at high switching frequencies.

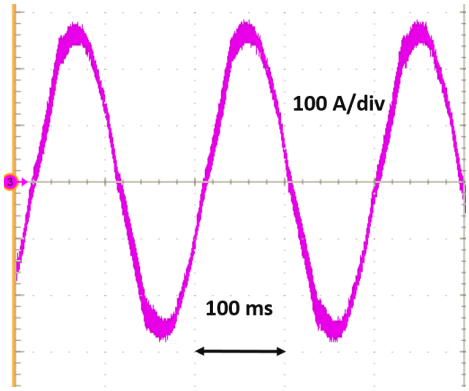
To decrease the effect of dead time on the output spectrum, the dead time was reduced from 2 μ s to 1 μ s. It is necessary to check the turn off time of the switch for different current conditions for this adjustment. The propagation delay of gate and control circuit needs to be counted in too.



(a) 10 Hz output current with 12 kHz of switching frequency



(b) 5 Hz output current with 4 kHz of switching frequency



(c) 5 Hz output current with 2 kHz of switching frequency

Figure 5-15: Low frequency output current distortion in high switching frequency

5.7 Conclusion

In this chapter different modulation techniques in a two-level converter have been compared. The effectiveness of current methods for peak junction temperature in different operating conditions has been analyzed. Three level converters are proposed to lower peak junction temperature more efficiently compared to two-level converters. An algorithm for finding the optimal modulation scheme for operation in low output frequency and high output power is proposed in three-level converters. The algorithm is used in a converter with 600 V IGBT modules. Then the neutral point voltage imbalance in steady state is analyzed and it is shown that the modified method can balance the neutral point balance with minimal negative effect on peak junction temperature.

Chapter 6

Implementation

In this chapter, details about implementation of the topologies that were introduced will be provided. The goal of building these converters is to verify filter sizing methods. First, the controller tuning methods are discusses and then designed boards and circuits are shown. Measurement results are provided at the end.

6.0.1 AFE Controller Design

The schematics for a two-level AFE is shown in Fig. 6-1. The closed-loop controller to regulate the DC bus voltage and rectifier line currents is presented in Fig. 6-2. $G_v(z)$, $G_q(z)$ and $G_d(z)$ are the PI controllers used for regulating DC voltage, q-axis and d-axis current.

The control-to-output transfer function for the q-axis current loop and voltage loop and d-axis current loop can be shown to be as (6.1). L, C and R are small signal DC voltage, filter inductor, DC link capacitor and load resistor respectively. i_q and i_d are small signal values of grid current with the direction shown in Fig. 6-1. V_{dc} is the small signal variation of DC voltage around the steady state operating point.

$$
\begin{aligned}
\frac{i_q(s)}{d_q(s)} &= \frac{-\frac{V_{dc}}{L}(s+\frac{1}{C\,R}) - \frac{3}{2}\frac{D_q\,I_q}{L\,C}}{s^2 + \frac{1}{C\,R}s + \frac{3\,D_q^2}{2L\,C}} \\
C_1 &= \frac{1}{1+\frac{s\,L}{V_{dc}G_q(s)}} \\
C_2 &= \frac{-\frac{D_q}{V_{dc}G_q(s)}}{1+\frac{sL}{V_{dc}G_q(s)}} \\
C_3 &= \frac{\frac{3}{2}(\frac{D_q + I_q\,G_q(s)}{C})}{s+\frac{1}{RC}} \\
C_4 &= \frac{-\frac{3}{2}\frac{I_q\,G_q(s)}{C}}{s+\frac{1}{RC}} \\
\frac{v_{dc}(s)}{i_q} &= \frac{C_1(s)C_3(s) + C_4(s)}{1 - C_2(s)\,C_3(s)}
\end{aligned}
\tag{6.1}
$$

A custom made control board which includes TI DSP TMS320F2812 is used to generate the PWM signals. This control board has the capability of measuring current, grid voltage and DC voltage. This DSP is inside a board capable of detecting short circuit and feeding measurements

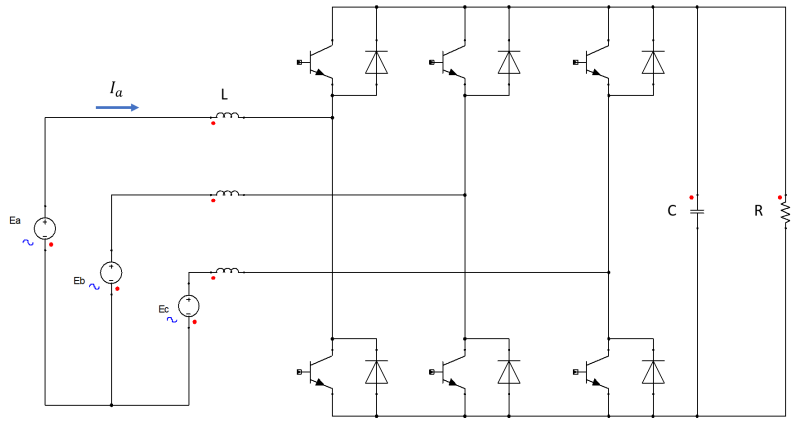


Figure 6-1: Two-level AFE schematics

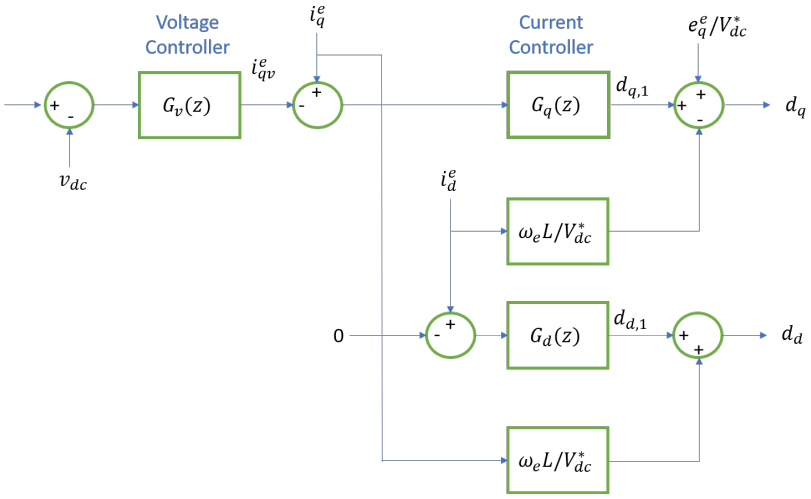


Figure 6-2: Closed-loop bus voltage and line current controller for active rectifier

from the grid and bus voltage named as General Purpose DSP (GPDSP) board. This board has been used for controlling inverters and AFE converters before [80, 81].

For the converter rating and specifications of Table 6.1, PI coneffcients of $G_v(s)$, $G_q(s)$ and $G_d(s)$ can be found as Table 6.2. PI controllers of $G_v(s)$, $G_q(s)$ and $G_d(s)$ for two operating conditions are presented in Fig. 6-3, 6-4 and 6-5.

Table 6.1: Converter ratings for testing the controller dynamics

Parameters	Value
Nominal power (hp)	40
Output frequency (Hz)	60
Grid voltage (V)	240
DC voltage (V)	400
Load resistance ($k\Omega$)	60
Grid inductance (mH)	1.2
Switching frequency (kHz)	4
DC bus capacitor (mF)	3
Phase margin (deg)	75
Bandwidth for $G_v(s)$ (Hz)	100
Bandwidth for $G_q(s)$ (Hz)	1000
Bandwidth for $G_d(s)$ (Hz)	1000

Table 6.2: Proportional and integrator gain coefficents for current and voltage controller of Table 6.1

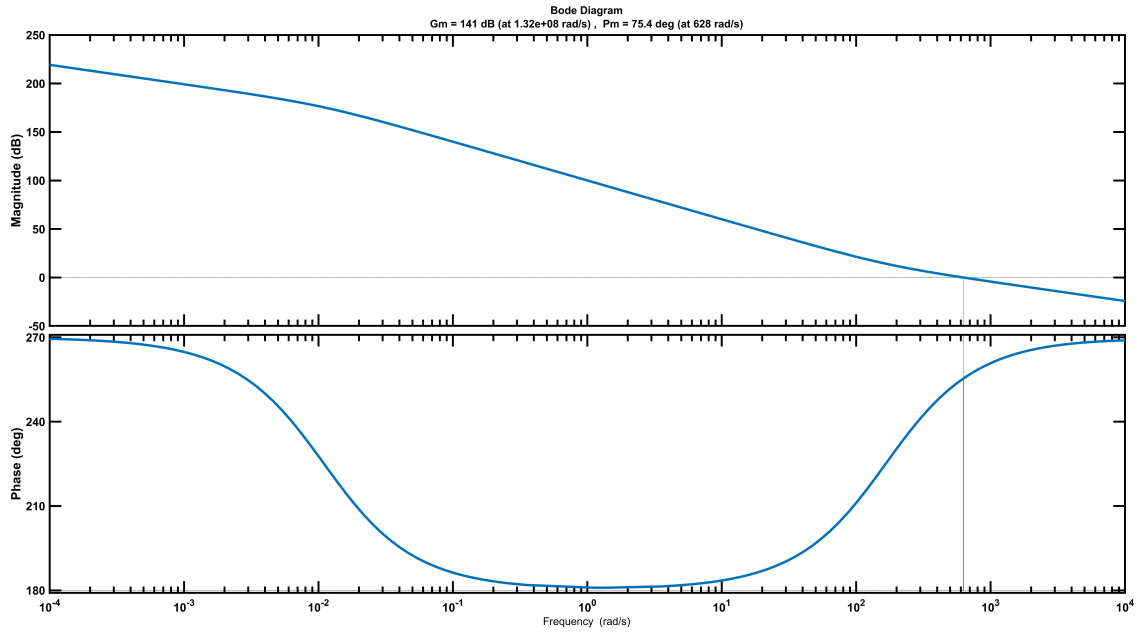
Parameters	Value
K_p of $G_v(s)$	2.5
K_i of $G_v(s)$	415
K_p of $G_q(s)$	0.0182
K_i of $G_q(s)$	30.57
K_p of $G_d(s)$	0.0163
K_i of $G_d(s)$	59.21

In order to run an AFE it is important to align the reference voltage with grid voltage using a PLL. Here a PLL with a the structure of Fig. 6-6 is used to align the two angles with setting the d axis component of grid voltage to zero. Fig. 6-7 shows the variation of angle with grid voltage. The yellow signal is grid voltage and the blue signal is set to have 0 value when the angle is less that 0.5 pu and to have value value of 1 when the angle is more than 0.5 pu.

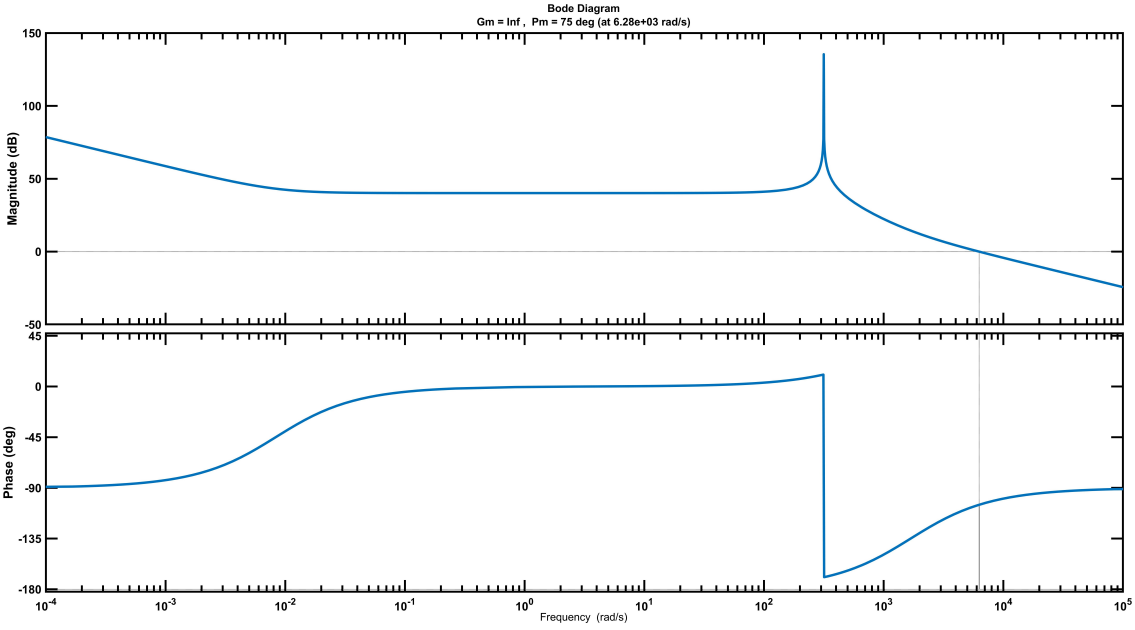
D and Q axis controllers are designed using fixed point tools of Simulink and support package of TI C2000 library. Fig. 6-8 shows the structure of the controllers. Anti wind up is used to avoid the constant increase of integrator terms and overflow of variables.

6.0.2 Test Setup

An evaluation board from Infineon (F3L030E07-F-W2-EVAL) is used to have a perfect gate drive design and make the comparison of losses possible. This board does not have DC bus capacitors. Each phase has a separate board and it is shown in Fig. 6-9. Having external capacitors makes the usage of film capacitors necessary.



(a) $G_v(s)$



(b) $G_q(s)$

Figure 6-3: Open loop transfer functions of $G_v(s)$ and $G_q(s)$ for load resistance of 60 $k\Omega$

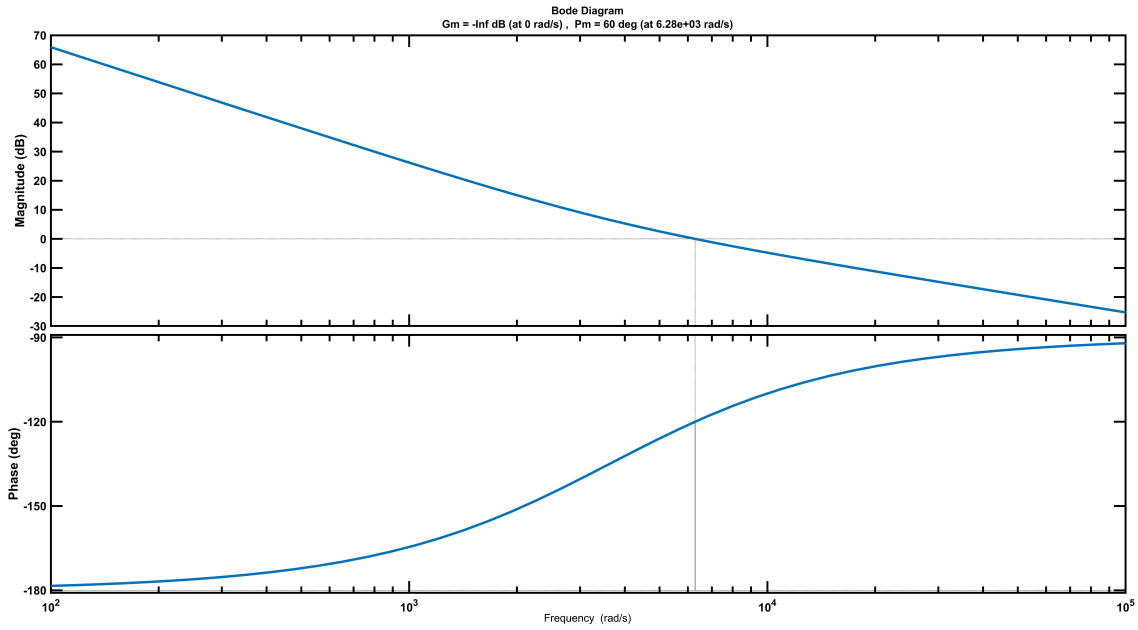


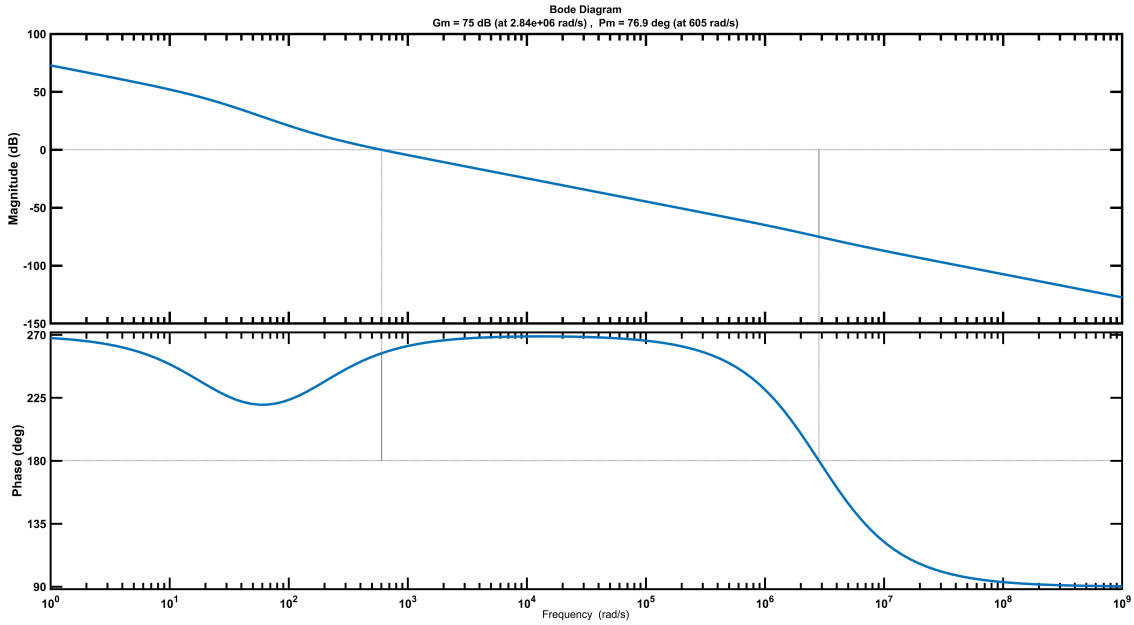
Figure 6-4: $G_d(s)$ for load resistance of 60 $k\Omega$ and 30 Ω

For AFE application, it is essential to measure the current value instantaneously to control the converter. So a current sensor circuit must be added. Also, the base plate's temperature can be measured from the evaluation board. In this board, thermistors, also known as NTC, are integrated as a temperature sensor. This thermistor is integrated to a circuit for getting a voltage signal showing the value of temperature. So all these items can be summarized as:

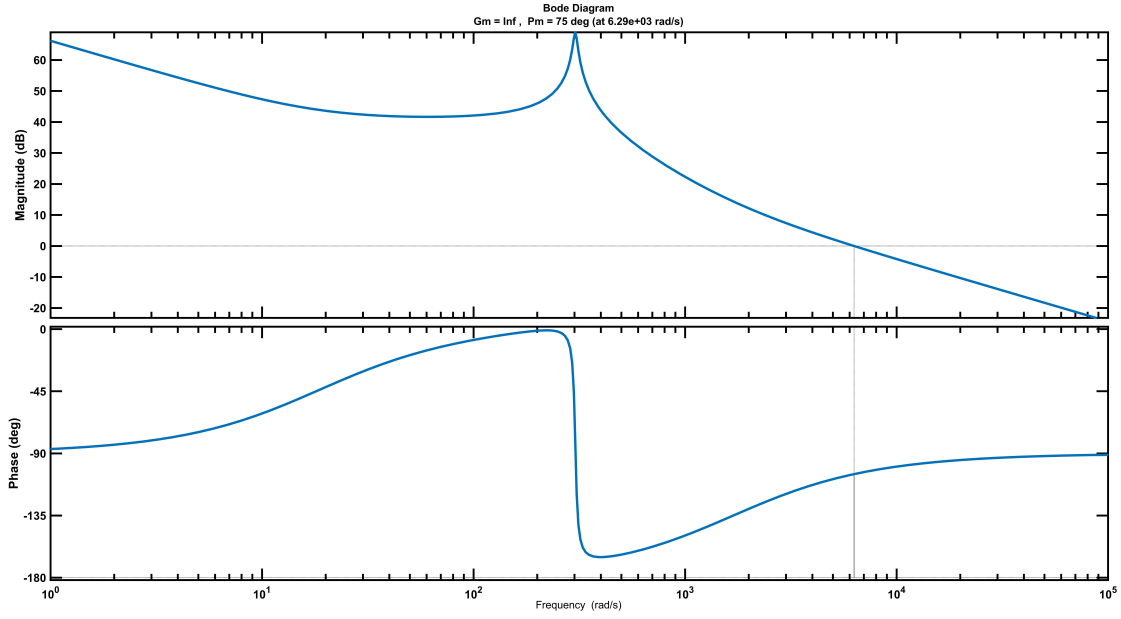
1. DC bus capacitors
2. Film capacitors
3. Current sensor
4. Current fault detection
5. Interface to the DSP board for PWM signals and pulse handling
6. Temperature measurement voltage division
7. Voltage measurement resistors

A custom board is designed to include the DC bus capacitors along with a resistor string to convert the DC voltage to lower voltage that can be sent to the GPDSP board. The layout and bare board of this design is shown in Fig. 6-10.

A second board is designed to measure current, detect short circuit and distribute the gate signals to the evaluation board. The layout schemes and bare board for this interface boards is shown in Fig. 6-11. The general scheme for connecting these boards together is presented in Fig. 6-12.



(a) $G_v(s)$



(b) $G_q(s)$

Figure 6-5: Open loop transfer functions of $G_v(s)$ and $G_q(s)$ for load resistance of 30 Ω

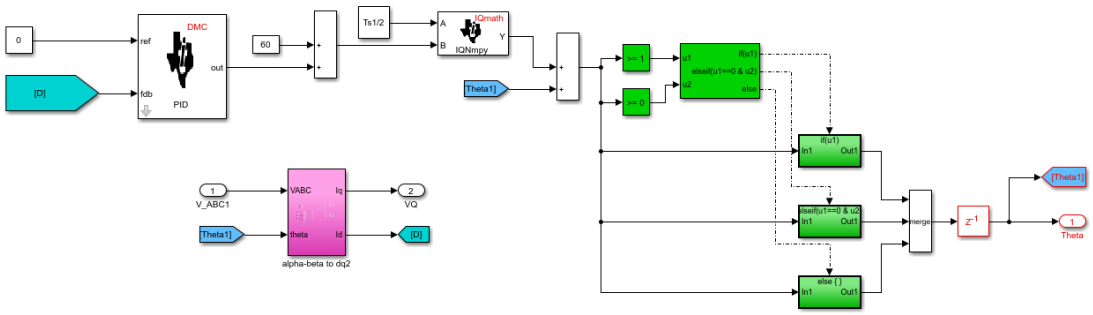


Figure 6-6: PLL controller structure to synchronise the reference voltage with grid voltage

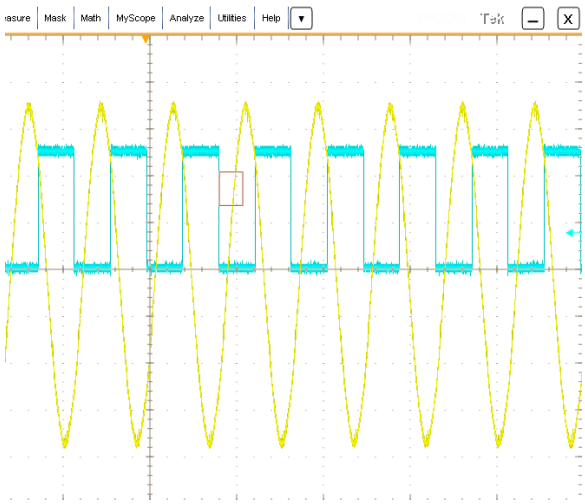


Figure 6-7: Reference angle of the controller in reference to grid voltage.

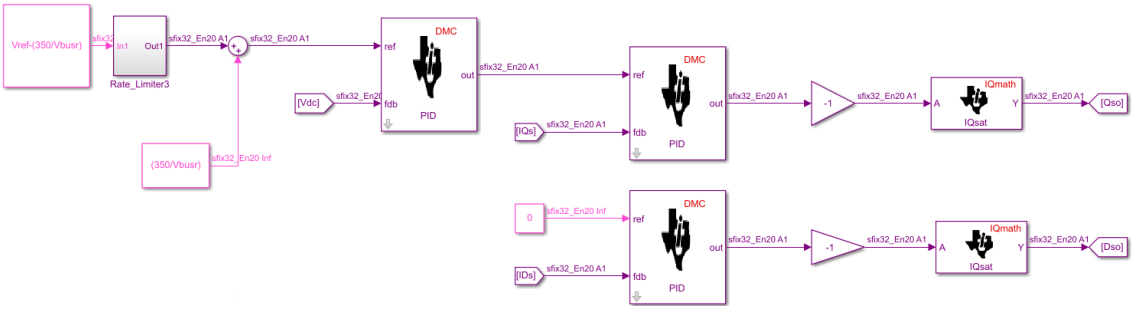


Figure 6-8: Reference angle of the controller in reference to grid voltage.

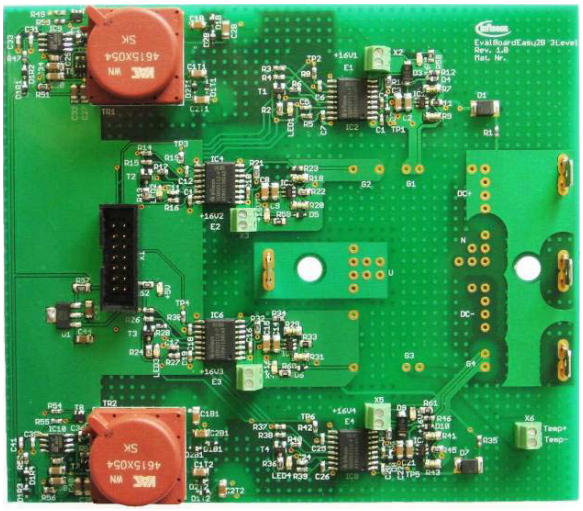
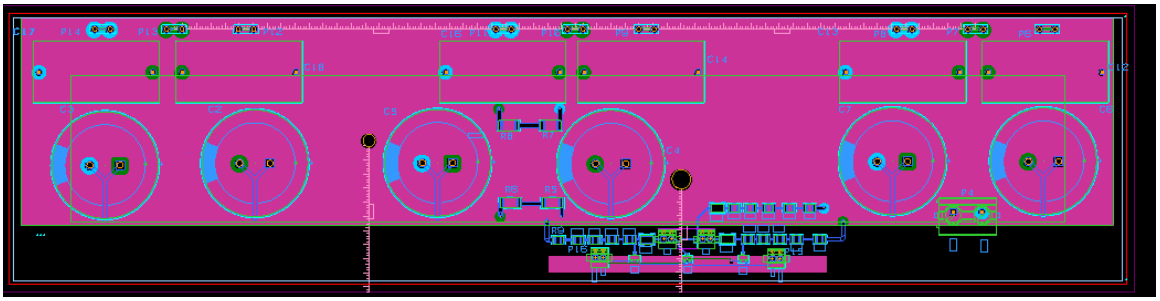
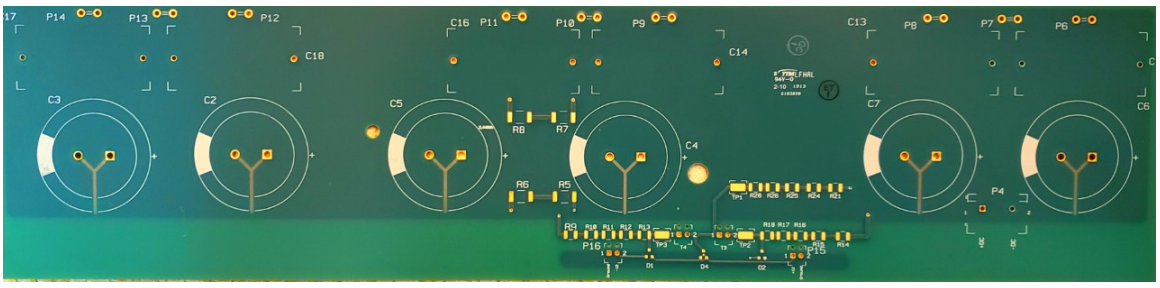


Figure 6-9: The evaluation board F3L030E07-F-W2-EVAL

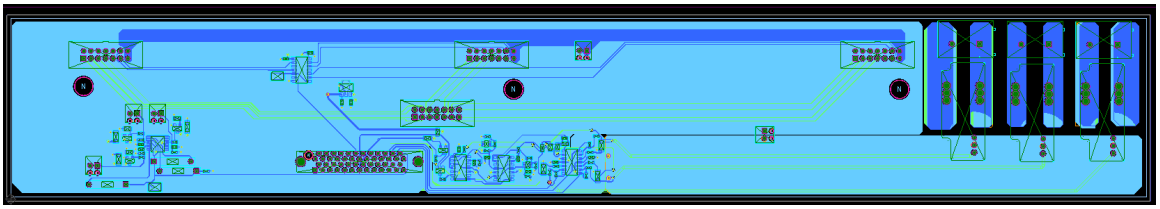


(a) Layout schematics

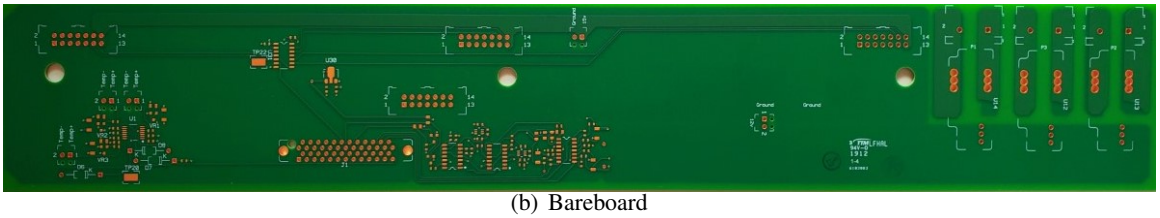


(b) Bare board

Figure 6-10: The board that includes the bus capacitors and measurement resistors



(a) Layout schematics



(b) Bareboard

Figure 6-11: Low voltage board for interfacing the GPDSP board and the evaluation board

6.0.3 Three-level Inverter Measurements

The three-level converter is configured for working as an inverter. A three-phase diode bridge is used to interface the inverter to the grid as shown in Fig. 6-13. A motor along with a dyne for applying torque is used to load the inverter. Fig. 6-14 shows the converter output current, DC voltage and line-line voltage for output frequency of 30 Hz and 10 Hz. The inverter is running in V/Hz mode. Low operating frequencies and therefore modulation indexes will result in two level modulation of the drive.

6.0.4 Two-level AFE Measurements

A two-level AFE is built using an AFE converter and an inverter to run the load as shown in Fig. 6-15. The goal from building this setup is to compare three-level and two-level converters current harmonics with the same switching frequency and filter. DC bus capacitors are precharged using a three-phase diode bridge. Inductor filter is 1.2 mH, grid voltage is 240 V and switching frequency is 4 kHz. Space vector modulation is used. Fig. 6-16 shows the output waveform of converters. The nameplate of the filtering inductor is shown in Fig. 6-17.

6.0.5 Three-level AFE Measurements

The setup presented in Fig. 6-13 is reconfigured to allow testing a three-level AFE converter. A similar load and inductor is used as the two-level converter. Fig. 6-13 shows the output waveform of converters.

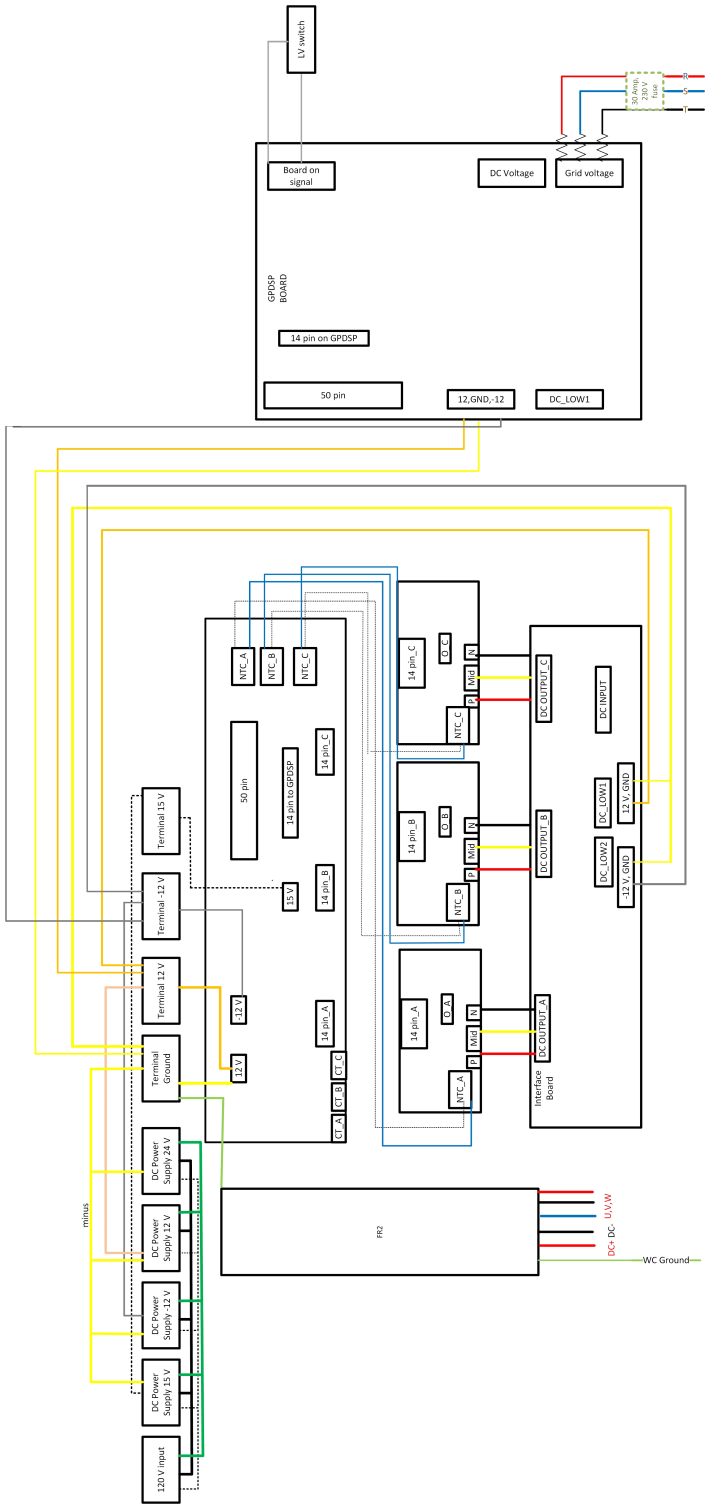


Figure 6-12: The parts on the custom boards to interface the DSP board to the evaluation board

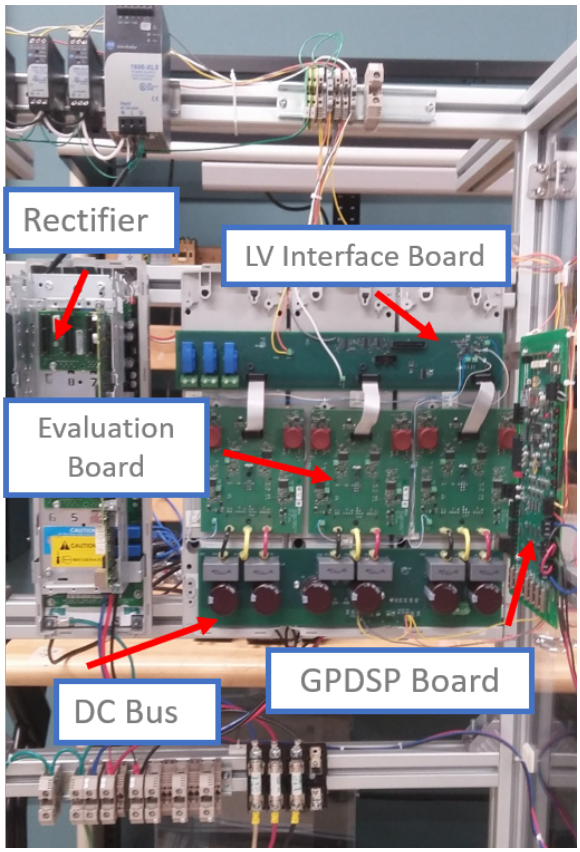
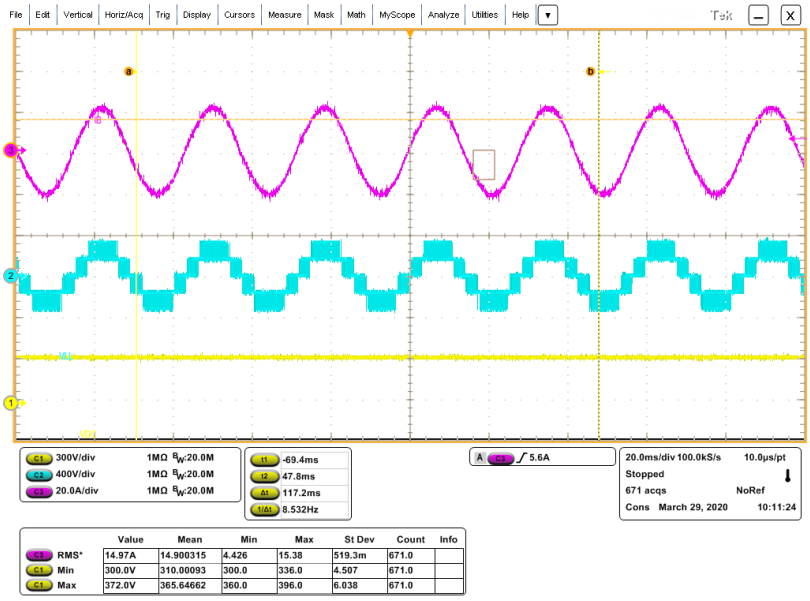
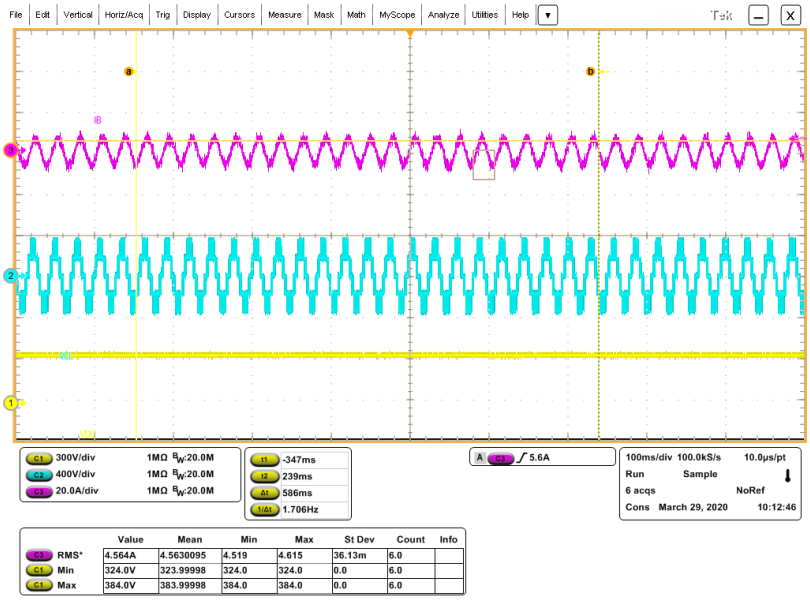


Figure 6-13: Three-level converter that is made with a controller board, an interface board, three phases of three-level modules, a rectifier and a bus bar board



(a) Modulation index of 0.9, operating frequency of 30 Hz and output current of 15 A



(b) Modulation index of 0.3, operating frequency of 10 Hz and output current of 4 A

Figure 6-14: Three-level inverter output. C3 is output current (A), C2 is line to line voltage (V) and C1 is the DC voltage (V). Grid voltage is 240 V and switching frequency is 4 kHz.

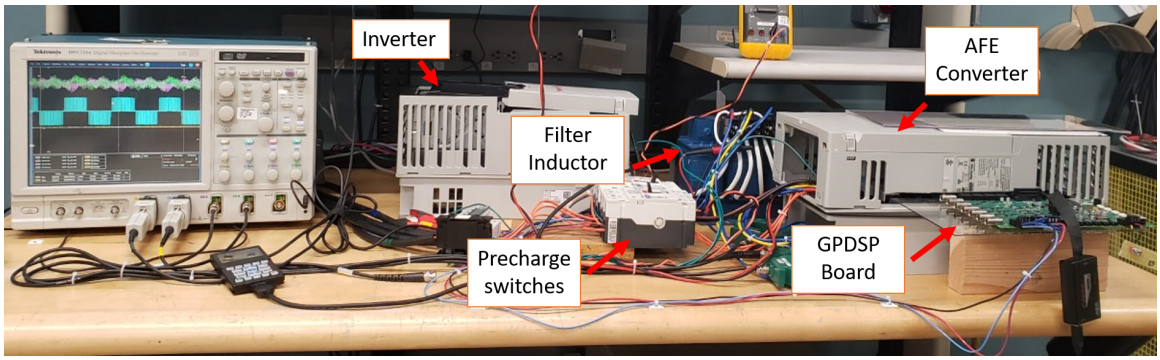
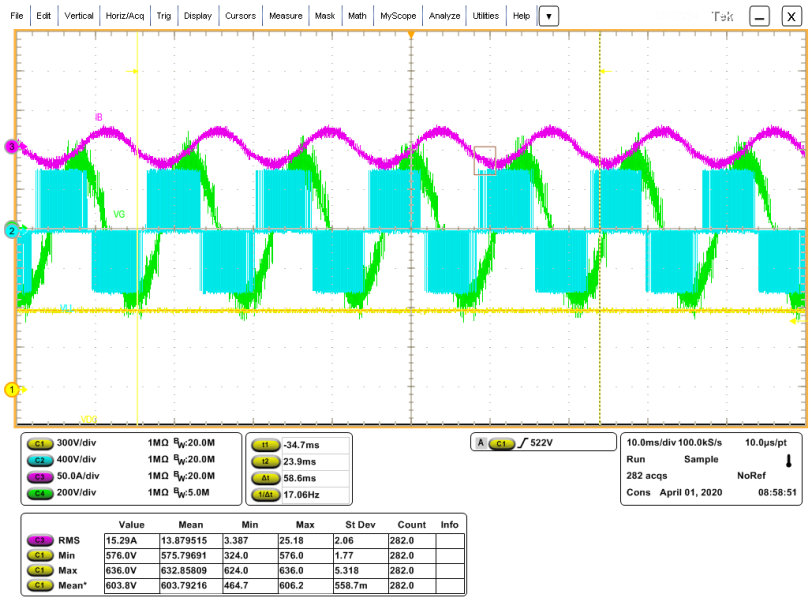


Figure 6-15: A two-level AFE integrated through the DC link with an inverter.

(a) Charging current for step voltage of 600 V



(b) Two-level AFE running with 15 A load

Figure 6-16: Two-level AFE output. C3 is output current (A), C2 is line to line voltage (V) and C1 is the DC voltage (V). Grid voltage is 240 V and switching frequency is 4 kHz.

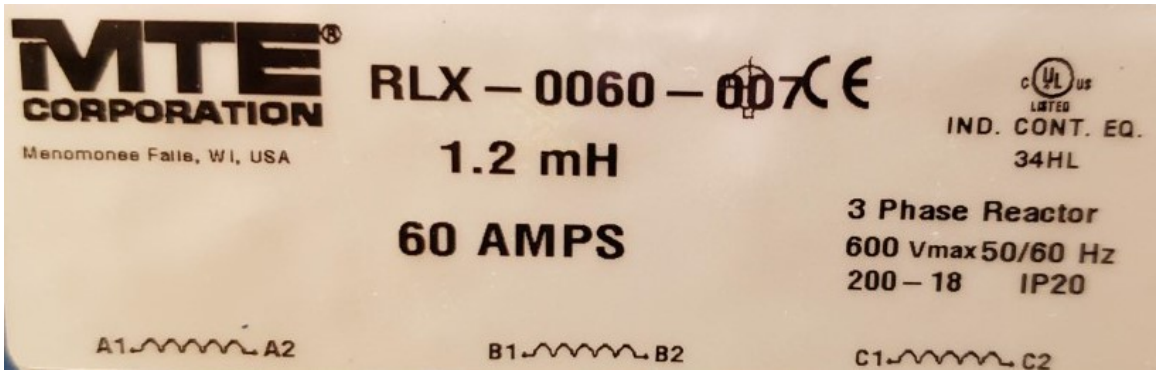
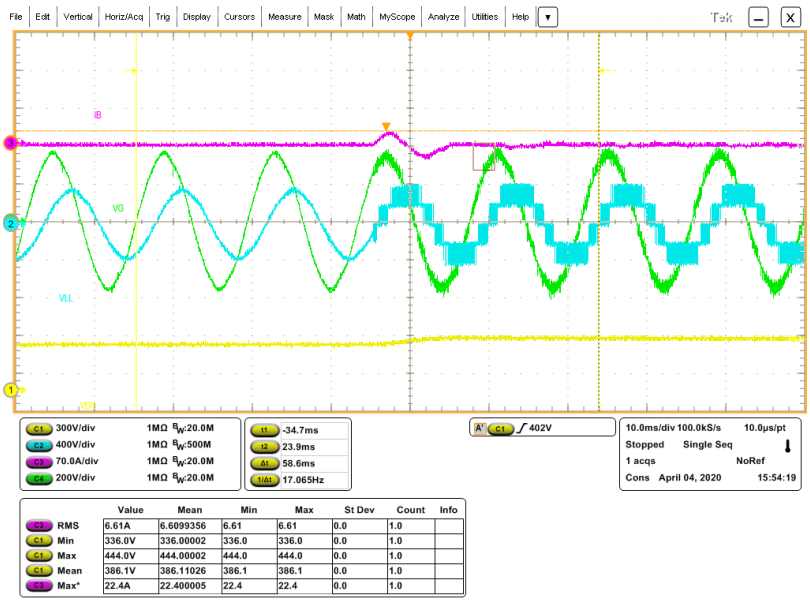
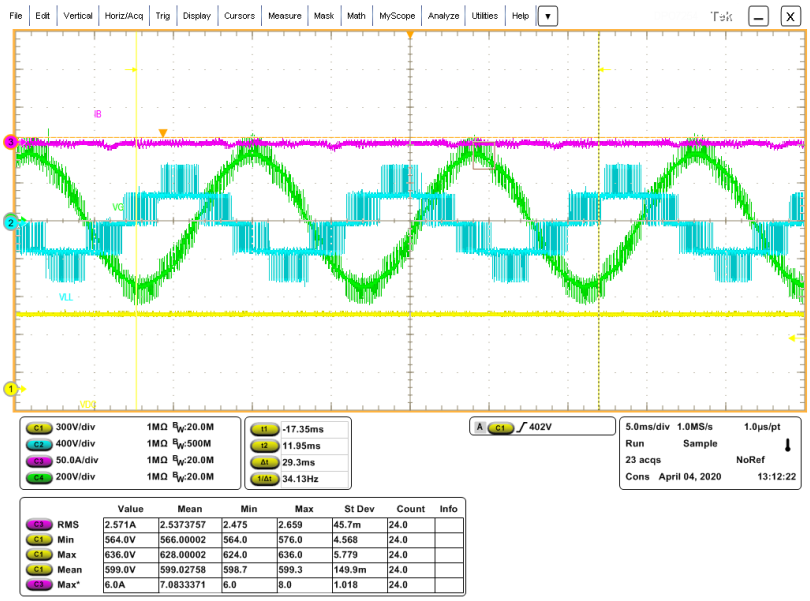


Figure 6-17: Nominal information of the three-phase inductor used in the test



(a) Charging current for step voltage of 600 V



(b) Three-level AFE running with no load

Figure 6-18: Two-level AFE output. C3 is output current (A), C2 is line to line voltage (V) and C1 is the DC voltage (V). Grid voltage is 240 V and switching frequency is 4 kHz.

Chapter 7

Summary and future work

This work investigates the design and optimization of the high power high frequency bidirectional 3-level power conversion system. It is a general purpose converter and the possible applications for the power conversion system includes renewable energy grid interface, energy storage system, motor drives and tractions, power supply for DC load and DC bus, energy control centers for smart grid and micro-grid. The key design challenges for the power conversion system are identified as high power density, high efficiency in a wide range of operating conditions, high reliability and good power quality.

To achieve the design objectives, a survey on the high power multilevel converter topologies and modulation strategies was done in chapter 1. The survey gives a detail classifications for the multilevel topologies and modulation strategies. The pros and cons for various multilevel converters and modulation schemes were discussed.

The comparison between different converter topologies is based on a general optimization algorithm with the objective functions of volume. In chapter 2, LCL filter design was performed considering thermal limitation. The novelty of this chapter was that the temperature limitation was incorporated into the optimization process as well.

Losses were calculated to compare different topologies and a thermal model was developed for SiC MOSFET power modules to predict the maximum junction temperature. Different modulation methods performance for the best performance including current THD, neutral point voltage balance and losses were compared in a three-level converter and a new modulation method was proposed to improve the performance of three-level converters.

Different topologies were compared for low speed operation as well. Three-level converter steps of voltage can be a helpful tool for overcoming high temperature ripples in converter. This can be of special application in traction motor converters.

Main contributions of this work can be summarized as:

1. Developing an optimization model for finding minimum weight converters
2. Proposing a new modulation method for balancing between neutral point voltage imbalance, THD and losses of three level converters
3. Derivation of a thermal model for SiC MOSFET power modules
4. Development of a low speed operation modulation strategy in the three-level converter to minimize the temperature ripple

As it was discussed SiC converters have the least amount of losses in different topologies and switch types. However, because of low turn on and off times, they can cause EMC issues. Future work will

include development of an active gate driver where different values of resistances will be in gate circuit based on the current level. This can reduce the EMC issues while increasing the losses at a minimal rate.

Low speed operation issues of converters were discussed in chapter 6. However, due to implementation challenges of low speed operation and dead time compensation methods, test results were not provided. Future work will include a dead time compensation method that is not based on current and can work for low speed, high frequency converters.

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Appendix A: Datasheet Properties of Power Modules

Table A.1: Comparison of datasheet parameters of different power modules

Si 1200 V module with 300 A current rating					
Module Name	Turn on switching energy (mJ)	Turn off switching energy (mJ)	Reverse recovery energy (mJ)	t_{off} (ns)	t_{on} (ns)
FF300R12KT3	25	37	26	680	215
1200 V module with 300 A current rating					
CAS300M12BM2	10.94	11.55	0	211	144
Hybrid 1200 V modules with 300 A current rating					
SKiiP38GB12F4V1	10	22	0	not given	not given
SiC 1200 V modules with 50 A current rating					
CCS050M12CM2	1.1	0.6	0	69	51
Hybrid 1200 V modules with 50 A current rating					
SKiiP25AC12F4V1	0.6	3.1	0	286	53
Si 600 V modules with 300 A current rating					
FF300R06KE3	3.3	12.5	7	600	190
Si 600 V modules with 50 A current rating					
F3L50R06W1E3-B11	0.4	1.6	1.5	295	42

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EDUCATION

University of Wisconsin-Milwaukee *2015 - 2020*
PhD in Electrical Engineering GPA: 4 out of 4
Department of Electrical Engineering
Thesis title: Three-level converters for low voltage high performance motor drives

Sharif University of Technology *2010-2012*
M.Sc in Electrical Engineering- Power Systems. GPA: 17.2 out of 20
Department of Electrical Engineering
Thesis title: Designing a 400 kV Compact Line for Iran Transmission Network

Sharif University of Technology *2005-2010*
B.Sc in Electrical Engineering- Power. GPA: 15.3 out of 20
Department of Electrical Engineering
Thesis title: Load Management Approaches by Demand Response

WORK EXPERIENCE

Rockwell Automation 2016-Present
Electrical Engineering Intern

Comparison of three level Si converters and two level SiC converters

- Designing a circuit to interface a three-level evaluation board to circuits needed to run the three-level converter as an Active Front End
- Designing the schematics and layout of the circuit using Mentor Graphics software
- Designing an LCL filter for the converter to face the grid considering thermal limitations and grid standards
- Designing a closed-loop control algorithm to run the converter as an AFE and inverter
- Implementing the controller on TI F2812 DSP

Developing a fixture for reliability testing of electrolytic capacitors
Rockwell Automation

- Simulating the test circuit in ANSYS Simplorer to validate the design
- Building the test fixture and testing high voltage (650 V) capacitors
- Estimating the MTBF of different capacitors

Building a platform for application of SiC MOSFET modules in 200 hp drives

- Characterizing SiC MOSFET modules from different vendors including running double pulse test, i-v curve derivation, reliability testing and open module thermal testing
- Investigating different short circuit detection methods
- Running the EMC tests and finding the optimal filters for complying with required standards
- Sizing the drive for starting a new product line at Rockwell Automation

Programming microcontrollers for fault handling

- Programming PIC microcontrollers to handle isolated analog signals and determine fault status
- Troubleshooting the PCB layout and finding layout issues

Building a common mode filter for reduction of SMPS EMI issues

- Sizing the parts for the specific requirements of SMPS EMI limits
- Testing the circuit at a 40 hp drive

University of Wisconsin- Milwaukee 2015-2018
Teaching and Research Assistant

Designing an optimal Multi Modular Converter (MMC) for shipboard applications
Numerical analyses of DC microgrid converters sizing and stability issues
Taught classes and labs of electromechanical conversion and power electronics

Power System Research Center of Tarbiat Modares University 2015
Research Assistant
Capacitor placement and reactive power control in transmission and mid-voltage network of Hormozgan (A regional electricity company)

- Simulating the power system network for different operating conditions to find the nodes with voltage dips
- Optimizing the placement for lowest cost and compatibility with grid standards

Developing a software tool for estimating the Average Variable Costs (AVC) of power plants
Power System Research Center of Tarbiat Modares University

- Programming curve fitting tools for economic models of power plants in C#
- Developing a graphic interface for receiving the data and showing the results graphically

Niroo Research Institute (NRI) of Iran's ministry of power 2010-2015
Research Assistant
Developing a planning module of SABA software

- *Developing an algorithm for placing normally open and normally close switches in distribution networks regarding cost and reliability metrics.*
- *Programming the algorithm in C# as a module of the new developed power system analysis and planning software (SABA)*

  Literature review about circuit breaker and instrument transformers Conducting a literature review bout circuit breakers and instrument transformers failure modes and required maintenance including investigation of related standards for a maintenance module in SABA software released by NRI

TECHNICAL STRENGTHS

- **Programming languages:** C, C++, Assembly (8085, 8086, 8051), Verilog
- **Algorithm development environment:** MATLAB
- **Electrical design and simulation tools:** ANSYS, PSCAD, DigSilent, ORCAD, SPICE, SIMULINK, COMSOL, ETAP and Mentor Graphics

PUBLICATIONS

- M. Karami and R. Tallam, "Thermal Characterization of SiC Modules for Variable Frequency Drives," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 4944-4949.

- X. Wang, M. Karami and R. M. Tallam, "Test Fixtures to Apply Variable DC Bias and AC Ripple Current for Reliability Testing of Electrolytic Capacitors," in IEEE Transactions on Industry Applications, vol. 55, no. 4, pp. 4073-4079, July-Aug. 2019.
- M. Karami, X. Wang and R. Tallam, "Test Fixture to Measure the Saturation Characteristics of Coupled Multi-Winding Inductors," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 4680-4687.
- M. Karami and R. M. Cuzner, "Optimal Control of Modular MultiLevel Converters (MMCs) for Minimum Storage Requirement," IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society, Washington, DC, 2018, pp. 3965-3972.
- M. Karami, R. Tallam and R. Cuzner, "Comparison of Three-Level and Two-Level Converters for AFE Application," 2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Atlanta, GA, 2018, pp. 264-270.
- X. Wang, M. Karami and R. M. Tallam, "Test fixture to apply DC bias and AC ripple current for reliability testing of electrolytic capacitors," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 2691-2695.
- S. Narasimhan, M. Karami, R. Tallam and M. Das, "Evaluation of SiC based inverter drives," 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Albuquerque, NM, 2017, pp. 1-8.
- M. Karami and R. M. Cuzner, "Optimal sizing of modular multi-level converters designed for shipboard applications," 2017 IEEE Electric Ship Technologies Symposium (ESTS), Arlington, VA, 2017, pp. 605-611.
- M. Karami and R. M. Cuzner, "A distributed controller for DC microgrids stability enhancement," 2016 IEEE International Conference on Renewable Energy Research and Applications (ICRERA), Birmingham, 2016, pp. 556-561.
- M. Karami, H. Seifi and M. Mohammadian, "Seamless control scheme for distributed energy resources in microgrids," in IET Generation, Transmission Distribution, vol. 10, no. 11, pp. 2756-2763, 4 8 2016.

TEACHING EXPERIENCES

- Power Electronics lecturer at University of Wisconsin-Milwaukee
- Relays and Protection lab lecturer at Sharif University of Technology (SUT)
- Electrical Circuits teaching assistant at SUT
- Electromechanical Energy Conversion lab assistant at UWM and SUT

HONORS AND AWARDS

- Winner of WiPDA conference 2018 student travel grant award, 2018
- Winner of three meritorious invention awards at Rockwell Automation
- Winner of 2019-20 UWM Graduate Student Excellence Fellowship (GSEF) awards
- Ranked 45th in Nationwide Universities Entrance Exam (Concour) for M.Sc. Program of Electrical Engineering, 2010.
- Ranked 103th in Nationwide Universities Entrance Exam (Concour) for B.Sc. Program (among more than 400,000 participants), 2005.
- Winner of several regional and state level rock climbing competitions

- First independent woman climber of Alam mountain's wall (the biggest climbing wall in Iran)

PROFESSIONAL SERVICES

- Reviewer for the 2016 IEEE Energy Conversion Congress and Exposition (ECCE 2016)
- Reviewer for 2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)
- Reviewer for 2017 IEEE Electric Ship Technologies Symposium (ESTS)
- Reviewer for 2019 IEEE Energy Conversion Congress and Exposition (ECCE 2019)

VOLUNTEER ACTIVITIES

- Organizer of meetup events for Adventure Rock climbing gym
- Technical leader of several mountaineering events at Sharif University of Technology Mountaineering Club
- Presented STEM career introductory sessions at different high schools