Hot-Substrate Deposition of Hole- and Electron-Transport Layers for Enhanced Performance in Perovskite Solar Cells

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Charge transport layers play an important role in determining the power conversion efficiencies (PCEs) of perovskite solar cells (PSCs). However, it has proven challenging to produce thin and compact charge transport layers via solution processing techniques. Herein, a hot substrate deposition method capable of improving the morphology of high-coverage hole-transport layers (HTLs) and electron-transport layers (ETLs) is reported. PSC devices using HTLs deposited on a hot substrate show improvement in the open-circuit voltage (V_{oc}) from 1.041 to 1.070 V and the PCE from 17.00% to 18.01%. The overall device performance is then further enhanced with the hot substrate deposition of ETLs as the V_{oc} and PCE reach 1.105 V and 19.16%, respectively. The improved performance can be explained by the decreased current leakage and series resistance, which are present in PSCs with rough and discontinuous HTLs and ETLs.

In recent years, organic–inorganic halide perovskite materials have continued to gain interest due to their facile material synthesis, deposition, and superior optoelectronic properties, such as high charge-carrier mobilities, strong absorption, long carrier recombination lifetimes, and long carrier diffusion lengths.[1–6] The certified power conversion efficiency (PCE) of perovskite solar cells (PSCs) has been rapidly boosted to 22.1% via systematically optimizing materials, interfaces, and processing methods,

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and the veil over the intrinsic mechanism is also gradually being lifted.[7–14] This process has revealed the important role of charge transport layers (CTLs) in the development of high performance PSCs.[15–18] The role of CTLs is to extract either holes or electrons, thus their energy levels affect both the ability for charge selection and the resulting open circuit voltage (V_{oc}) of PSCs, which has led to various efforts to tailor their energy levels.[19–22] In addition to the optimization of CTL energy levels, to avoid the issue of hot spots, an uniform morphology is quite important for highly efficient and large area PSCs.[23–25] In principle, there should be an optimal thickness for a given CTL due to the trade-off between their distinct functionalities. CTLs transport selected free charges to electrodes. Most of the conventional materials used for hole and electron transport layers, including organic and inorganic options, have much lower charge carrier mobilities than perovskites do; thus a thinner CTL is preferred to reduce the series resistance (R_s) in a device in efforts to attain higher fill factor (FF). Alternatively, CTLs help avoid charge leakage and reduce charge recombination by preventing direct contact between the metal electrode and perovskite films. In addition, CTLs prevent or slow the permeation of undesired species into perovskite, such as metal ions, oxygen, and moisture. Thus, a thicker CTL is preferable for this functionality. If a CTL is very rough, only some areas will be an optimal thickness, others may suffer from significant current leakage or a high series resistance. An increased current leakage in a device reduces the V_{oc} and a large R_s often results in a low FF.
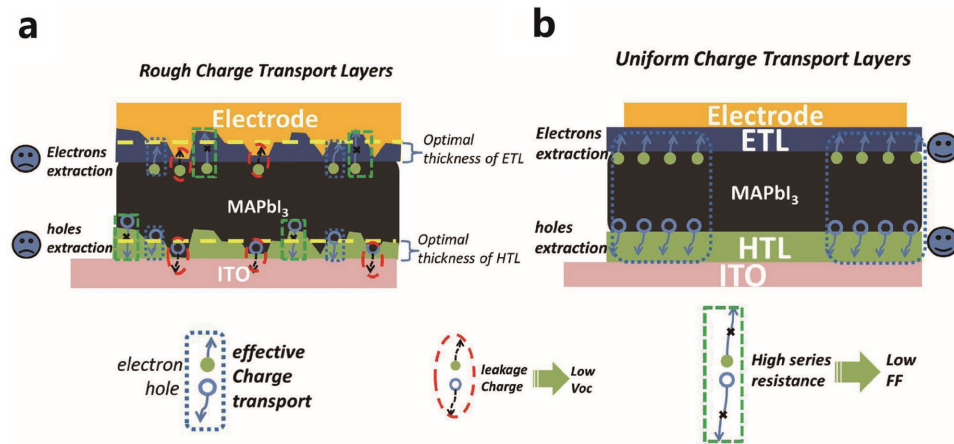
Herein, we report a simple hot substrate deposition method to improve the surface morphology of both the hole-transport layer (HTL) of poly(4-butylphenyl-diphenyl-amine) (PTPD) and the electron-transport layer (ETL) of phenyl-C61-butyric acid methyl ester (PCBM), as illustrated in **Scheme** 1b. The modified PTPD layer, with its higher coverage and flatness, combines advantages of an appropriate work function and nonwetting surface character, and the modified PCBM with higher uniformity and lower roughness contributes to less current leakage and low charge recombination. As a result of the improved PTPD, perovskite and PCBM layers, the PCEs of $CH_3NH_3PbI_3$ (MAPbI$_3$)-based PSCs increased from 17.00% to 19.16%.

Here we employ poly(3,4-ethylenedioxythiophene): poly(styrenesulphonate) (PEDOT:PSS) as the bottom HTL because of its high conductivity, high coverage, and excellent

Scheme 1. a) Charge transport in rough charge transport layers-based PSCs. b) Charge transport in PSCs based on charge transport layers with uniform thickness at optimal value.

smoothness as shown by the atomic force microscope (AFM) and scanning electron microscope (SEM) images in **Figure 1**a,d. However, the lower work function of the PEDOT:PSS relative to many other HTL materials limits the potential V_{oc} of devices as represented in Figure S4 in the Supporting Information. In addition, the hydrophilic surface of PEDOT:PSS tends to produce a perovskite active layer with smaller grain sizes. To overcome such limitations, we attempted to deposit PTPD on top of the PEDOT:PSS to create a hole transport bilayer PTPD/PEDOT:PSS. The PTPD/PEDOT:PSS HTL bilayer is capable of adjusting the work function and modifying the surface wetting character to improve device performance capability. As shown in Figure 1b,e, the PEDOT:PSS covered indium tin oxide (ITO) substrates on a room-temperature (RT) (PTPD/PEDOT:PSS-RT) was very rough and had a low coverage, which may be ascribed to the poor adhesion of PTPD to the PEDOT:PSS surface, and

self-aggregation of PTPD molecules during the film formation process. HTLs made from nonuniform and low coverage films may cause current leakage at regions where the HTL is too thin and a large R_s at regions where the HTL is too thick (illustrated by Scheme 1a). To mitigate this problem, we adopted a hot substrate deposition method, in which the substrates were preheated to a given temperature before the CTLs were deposited. As the result in Figure 1c,f shows, the PTPD film deposited on the PEDOT:PSS substrate that was heated to 90 °C (PTPD/PEDOT:PSS-90 °C) exhibited better coverage and smaller surface roughness compared with the room-temperature sample (PTPD/PEDOT:PSS-RT). The hot substrate may induce better adhesion between the PTPD and PEDOT:PSS surface because the quick drying of the solvent caused by the hot substrate provides less time for the self-organization of the PTPD, forcing the PTPD to quickly form a higher-quality film.
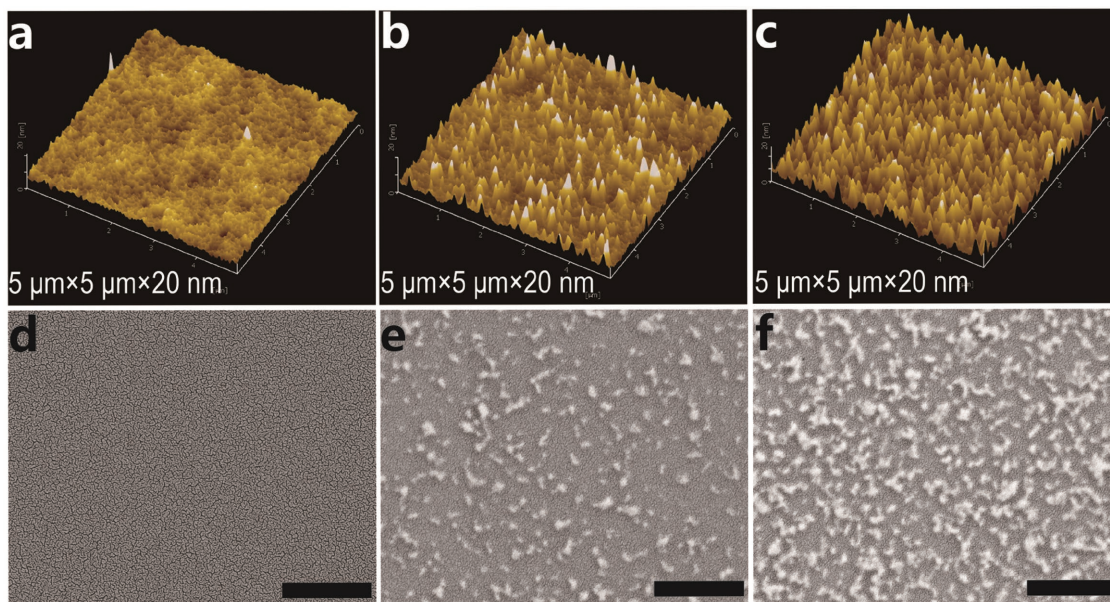

Figure 1. a–c) AFM images of the PEDOT:PSS, PTPD/PEDOT:PSS-RT (room temperature), and PTPD/PEDOT:PSS-90 °C (hot substrate, 90 °C), respectively, all of the scales are 5 µm × 5 µm × 20 nm. d–f) Top-view SEM images of the varied HTLs corresponding to (a–c), the scale bars are 1 µm.
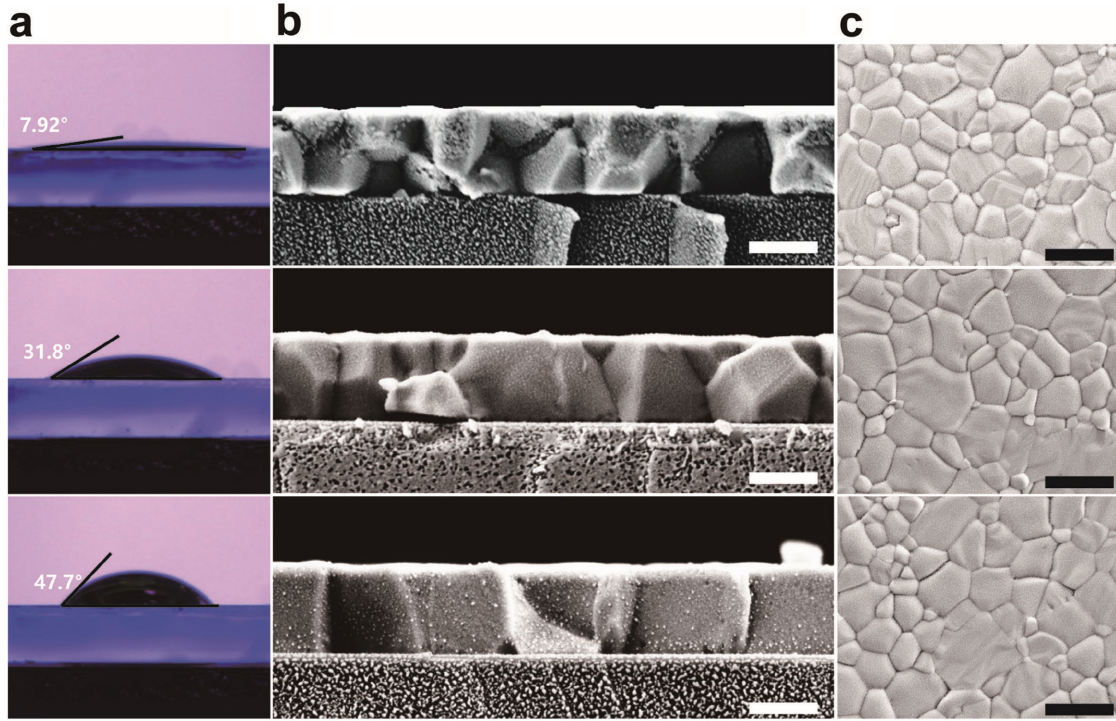
Figure 2. a) The contact angle of perovskite solution on varied HTLs of the PEDOT:PSS, PTPD/PEDOT:PSS-RT, and PTPD/PEDOT:PSS-90 °C, respectively, b) the cross section and c) the top-view SEM images of perovskite films deposited on the varied HTLs. Scale bars of (b) are 500 nm and of (c) are 1 μm.

It is interesting but not surprising that better coverage of PEDOT:PSS by PTPD would impact the MAPbI$_3$ layer deposited on it because the surface morphology of the HTL has been shown to impact MAPbI$_3$ grain formation, as we have previously demonstrated.[26] As shown in **Figure 2**a, the PEDOT:PSS film had a low contact angle of 7.92° to the perovskite precursor solution because the PSS ions of the PEDOT:PSS induce a hydrophilic surface. The PTPD/PEDOT:PSS-RT HTL had a much larger contact angle of 31.8° to the perovskite precursor solution due to the hydrophobic nature of the PTPD. PTPD/PEDOT:PSS-90 °C HTL had an even larger contact angle of 47.7° due to the improved coverage of PEDOT:PSS with PTPD. As shown in Figure 2c, the nonwetting character of the PTPD/PEDOT:PSS-90 °C HTL favors of the formation of larger perovskite grains. As shown in Figure S1 in the Supporting Information, the average sizes of the MAPbI$_3$ grain are 520 nm on PEDOT:PSS, 611 nm on PTPD/PEDOT:PSS-RT, and 658 nm on PTPD/PEDOT:PSS-90 °C, which is in good agreement with the results of a previous study.[26] Figure 2b shows the cross-sectional SEM images of MAPbI$_3$ films deposited on various HTLs. Most of the grain boundaries are perpendicular to the substrate for perovskite films deposited on a PTPD/PEDOT:PSS-90 °C HTL, which reduces the charge recombination by minimizing the grain boundaries area. On the contrary, the grain boundaries are far fewer perpendicularly distributed for perovskite films on PEDOT:PSS and PTPD/PEDOT:PSS-RT. This result would indicate that the hot substrate deposition method may favor vertical charge transport in the perovskite active layer.

To determine how the hot substrate deposition method will impact the performance of PSCs, we carefully studied the photovoltaic properties of PSCs based on various HTLs. First,

we optimized the concentration of PTPD and then fabricated PSCs based on the PEDOT:PSS and PTPD/PEDOT:PSS HTLs that had been deposited at various temperatures. The resulting current density–voltage (J–V) curves and corresponding photovoltaic parameters are shown in Figure S2 and Table S1 in the Supporting Information, **Figure 3**a, Figure S3 in the Supporting Information, and **Table 1**. The adopting of the PTPD/PEDOT:PSS HTL and increasing the substrate temperature improved the V_{oc} from 0.984 to 1.081 V. The variation of PCE followed a very similar trend and reached 18.01% efficiency for the optimized devices deposited on a substrate heated to 90 °C. To determine the origin of the improvement in the V_{oc} and PCE, we measured the work function of PEDOT:PSS, PTPD/PEDOT:PSS-RT, and PTPD/PEDOT:PSS-90 °C. As shown in Figure S4 in the Supporting Information, work function of the PTPD/PEDOT:PSS-RT film is −4.94 eV, which is higher than that of the PEDOT:PSS (−4.87 eV), while the PTPD/PEDOT:PSS-90 °C showed a slightly higher work function of −4.97 eV due to its better film coverage. Although there is not yet a clear correlation between the work function of charge selective layers and the V_{oc} in perovskite solar cells, but we speculate that a larger work function of PTPD/PEDOT:PSS that more closely matches with that of MAPbI$_3$ could increase V_{oc} of the devices by reducing energy loss and charge recombination.[27] However, the larger J_{sc} induced by employing the PTPD layer may due to the better film quality of the resulting perovskite layer (shown as Figure 2c). The rough surface of PTPD/PEDOT:PSS-RT layer may be the main reason for the decreased FF (73.86%). However, the better coverage and lower variation in layer thickness of the PTPD via hot substrate deposition successfully recovered the FF to 75.62% without diminishing the
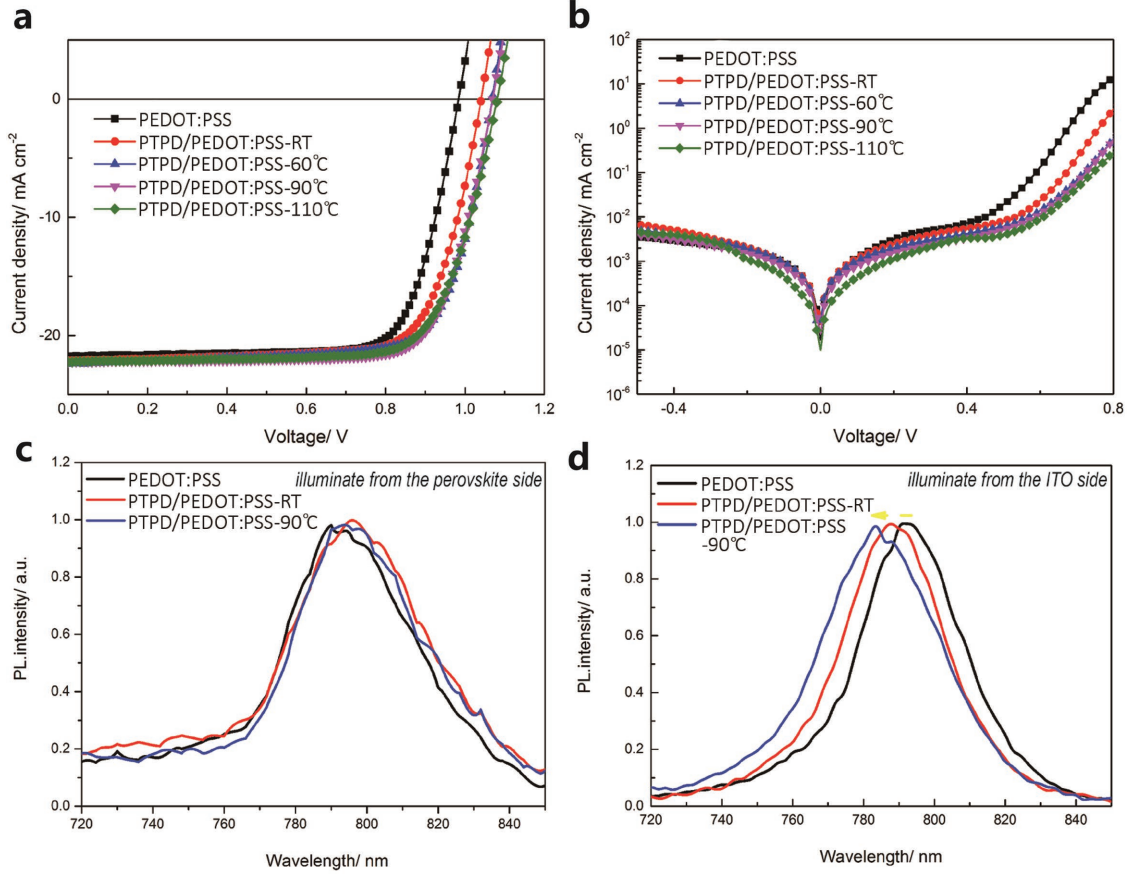
Figure 3. a) Current–voltage (J–V) curves under 100 mW cm^{-2} illumination with forward scan mode for devices based on varied HTLs of PEDOT:PSS and PTPD/PEDOT:PSS films deposited on substrates with different temperature (RT, 60, 90, and 110 °C), with an active area of 0.12 cm^2 at forward scanning rate of 0.05 V s^{-1}, b) J–V curves for devices based on varied HTLs under dark condition, the PL spectra for perovskite samples deposited varied substrates, with 532 nm green laser as excitation source from c) the perovskite side and d) from the ITO (HTL) side.

Table 1. Photovoltaic parameters of PSCs using varied HTLs and PCBM ETLs modified via the hot-substrate deposition strategy. All the devices were measured under the same conditions.

	PCE [%]	V_{oc} [V]	J_{sc} [mA cm^{-2}]	FF [%]
PEDOT:PSS[a]	16.20	0.984	21.78	75.62
PTPD/PEDOT:PSS-RT	17.00	1.041	22.12	73.86
PTPD/PEDOT:PSS-60 °C	17.64	1.069	22.36	73.80
PTPD/PEDOT:PSS-90 °C	18.01	1.070	22.25	75.62
PTPD/PEDOT:PSS-110 °C	17.68	1.081	22.23	73.56
PCBM-94 °C[b]	17.17	1.022	22.27	75.61
PCBM-82 °C[b]	18.19	1.086	22.63	74.00
PCBM-62 °C[b]	18.62	1.099	22.94	73.82
PCBM-Rt[b]	18.01	1.070	22.25	75.62
PCBM-62 °C-best cell[b]	19.16	1.105	22.80	76.05

[a]All of the photovoltaic parameters of PSCs (active area = 0.12 cm^2) were measured under a one sun simulated solar irradiation (AM 1.5, 100 mW cm^{-2}) with forward scanning of 0.05 V s^{-1}; [b]PSCs with varied PCBM ETLs are based on the same HTLs of PTPD/PEDOT:PSS-90 °C.

V_{oc} or J_{sc}. Because hot substrate deposition has reduced the number of regions with high series resistance, the resulting average thickness may be closer to that of an optimized thickness.

The dark current of the devices shown in Figure 3b reveals the other function of the PTPD layer, i.e., leakage current reduction. The use of PTPD layers, particularly those deposited onto hot substrates, reduces the current leakage and increases the diode rectification ratio, which may be explained by the higher work function, better coverage by PTPD, and suppressed recombination in perovskite films with larger grains.[28,29] As shown in Figure 3c, the photoluminescence (PL) peaks of the perovskite films deposited on various HTL substrates illuminated from the perovskite side have the same PL peak at 792 nm. However, when illuminating from the HTL side, the PL peak of perovskite on PTPD/PEDOT:PSS-90 °C HTL exhibits a blueshift from 788 to 784 nm compared to perovskite on PTPD/PEDOT:PSS-RT HTL (Figure 3d), which is very similar to the phenomenon previously reported by Shao et al.[17] The blueshift in the PL of the perovskite layer can be attributed to the decrease either in trap states at the HTL/perovskite interface or in perovskite grains/boundaries near the HTL.

In typical p–i–n planar structure PSCs, PCBM is a popular ETL that has the multifunctional purpose of electron extraction and grain boundary passivation.[17,30,31] Therefore, improving the quality of the PCBM layer and its interface with perovskite layer is an attractive approach to further increase the performance of PSCs. Here, we found that the hot substrate deposition strategy was also effective in improving the quality of the PCBM layers. PCBM ETLs deposited on the perovskite substrates at various temperature (RT, 62, 82, and 94 °C) were used to fabricate devices. We began to measure the temperature of the perovskite-based substrates preheated to 110 °C as soon as they were transferred onto the spin coater. Because the room temperature in the glovebox was constant and there was no strong airflow, we can be sure of the real temperature of the substrates according to the cooling time (5 s (94 °C), 15 s (82 °C), 35 s (62 °C), 300 s (22 °C)). We then quickly casted 20 µL of PCBM solution onto the substrate at various cooling times (temperatures) during spinning to form various PCBM ETLs. Their $J–V$ curves and photovoltaic parameters are shown in **Figure 4**a and Table 1, respectively. Both the V_{oc} and PCE

presented a trend of first improving and then decreasing with the continual increase of substrate temperature. The device with PCBM-62 °C gave the highest V_{oc} of 1.099 V and PCE of 18.62% compared with the device with PCBM ETL deposited at RT. The variation in the $J–V$ curves measured in the dark shown in Figure 4b, elucidate an opposite tendency of the efficiency results. The lowest dark current resulted from the PCBM-62 °C ETL, which can be attributed to the higher coverage and improved uniformity of the PCBM films on the perovskite layer. We also studied the influence of the ETLs' thickness on the performance of PSCs by utilizing PCBM solutions with different concentrations from 10 to 35 mg mL^{-1}, and depositing them on perovskite substrates at both RT and 62 °C. The result is shown in Figure S5 in the Supporting Information: the V_{oc}, FF, and PCE of the PCBM-RT-based PSCs clearly diminished with the decreased thickness of PCBM. However, the PCBM-62 °C-based PSCs performed much better with the thinner PCBM films. This may have occurred because even with a thinner layers, the hot substrate strategy is useful in the production of PCBM ETLs with higher coverage and improved
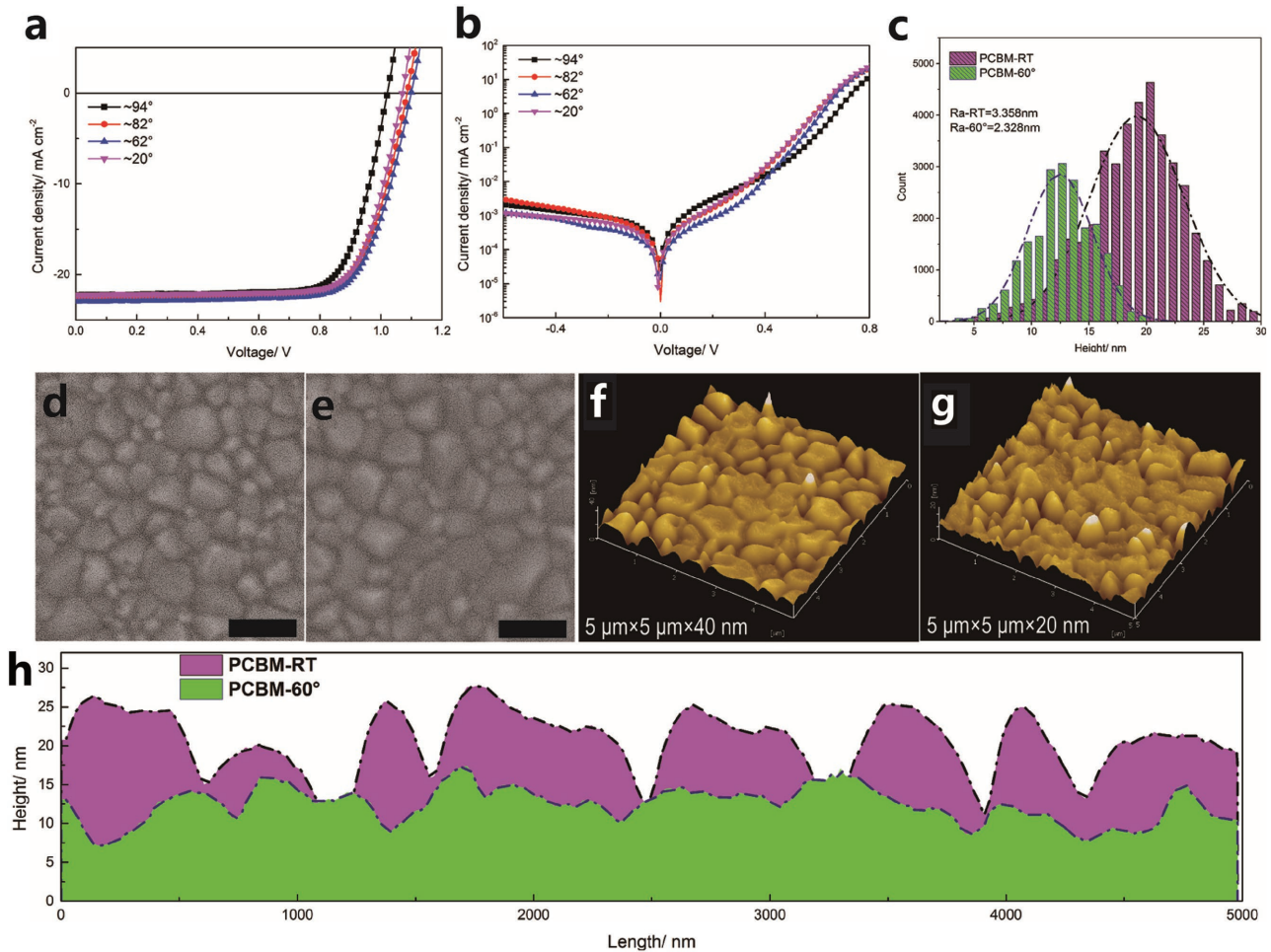

Figure 4. $J–V$ curves of devices a) under 100 mW cm^{-2} illumination and b) under dark condition with forward scan mode based on PCBM ETLs deposited under different temperature heated substrates, with an active area of 0.12 cm^2 at a scan rate of 0.05 V s^{-1}, c) the surface height data distributions of PCBM-RT and PCBM-62 °C ETL, respectively. d,e) Top-view SEM images of PCBM-RT and PCBM-62 °C ETL, the scale bars are 1 µm. f,g) The AFM surface images of PCBM-RT and PCBM-62 °C ETL, the scales are 5 µm × 5 µm × 40 nm and 5 µm × 5 µm × 20 nm, respectively. h) Cross-section height distributions of PCBM-RT and PCBM-62 °C ETL, respectively.

uniformity. We also utilized both SEM and AFM to observe the surface morphologies of the PCBM layers deposited on perovskite substrates at RT and 62 °C as shown in Figure 4d–f. There are many deep valleys on the PCBM-RT ETL surface, whereas the PCBM-62 °C ETL exhibits a smoother surface morphology. Their distribution of surface heights illustrated in Figure 4c show that PCBM-62 °C has a narrower height distribution and lower roughness (Ra-62 °C = 2.328 nm), compared with PCBM-RT ETL (Ra-RT = 3.358 nm). The cross-section height distributions of the samples shown in Figure 4h directly proved that hot-substrate deposition is capable of producing a much smoother ETL surface. Our strategy induced the formation of higher quality PCBM ETLs with more desirable morphology, which can be attributed to the hot substrate speeding the drying process of solvent in order to avoid the aggregation of PCBM molecules.

Finally, we fabricated PSCs by utilizing the optimized hot substrate deposition method to modify both the HTL and ETL. As shown in **Figure 5**a, the carefully optimized device obtained a peak efficiency of 19.16% in the forward scan and 19.38% in the reverse scan, indicative of negligible hysteresis. Also, the incident photon-to-electron conversion efficiency (IPCE), shown in Figure 5b, is favorably high for wavelengths from 300 to 800 nm. The corresponding integrated J_{sc} is 22.5 mA cm^{-2} which is in good agreement with the results of the J–V curve, as shown in Figure 5a. Figure 5c illustrates the steady-state photocurrent output of the PSC device at the maximum power point (0.90 V)

while being illuminated for 150 s, which shows a stable current density of 21.13 mA cm^{-2} with a resulting PCE of 19.02%. Moreover, 40 devices were fabricated and characterized to study the reproducibility of the device fabrication process (shown in Figure 5d). As a result, we achieved an average V_{oc} of 1.078 V (s.d. = ± 0.013 V) and PCE of 18.31% (s.d. = ± 0.53%), implying excellent reproducibility using this method.

We demonstrated that the use of a hot substrate deposition is an effective avenue for modification of both the PTPD/PEDOT:PSS HTL and the PCBM ETL in p–i–n planar PSCs. After a simple optimization via this method, the V_{oc} and PCE were enhanced from 1.041 to 1.105 V and from 17.00 to 19.16%, respectively. With a careful and systematic study, we found that the hot substrate deposition contributes to the high coverage and low roughness of PTPD/PEDOT:PSS HTL, which can effectively mitigate the high regional series resistance and the overall lower FF. The modified HTL favors the formation of a higher quality perovskite film with larger grains, which indicates less charge recombination at the grain boundaries. Alternatively, hot substrate deposition method assists the formation of higher quality PCBM ETLs with improved adhesion to the perovskite surface and a more favorable surface morphology. Due to the modification of the HTL and ETL via the hot substrate deposition, the resulting enhancement of the V_{oc} and PCE of the device is evident. Thus, we believe that this strategy can be a promising and reliable approach for improving the overall performance of PSCs.
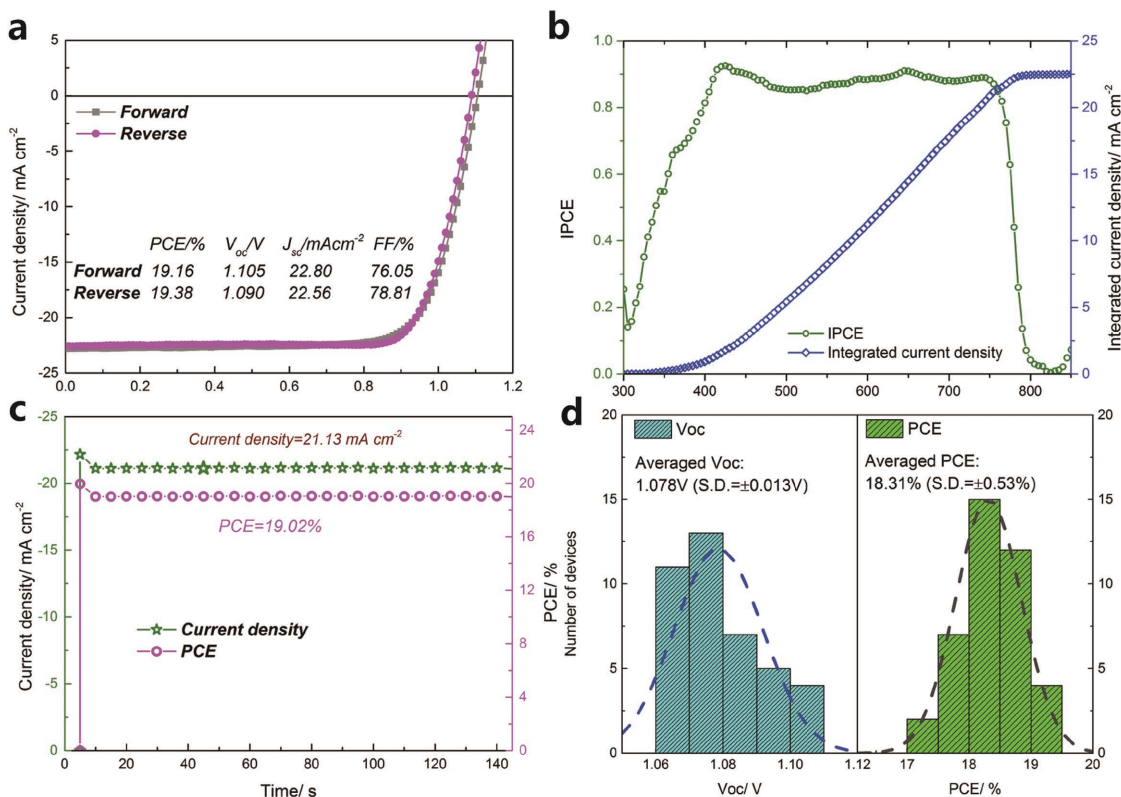

Figure 5. a) J–V curves under 100 mW cm^{-2} illumination with both reverse and forward scan for the best-performing device based on HTL and PCBM-62 °C, with an active area of 0.12 cm^2 at a scan rate of 0.05 V s^{-1}, b) the IPCE spectrum of the best-performed PSC of (a) and the corresponding integrated J_{sc}, c) the stead state current output at the point of maximum power output (0.90 V) of the best-performing device, d) the conversion efficiency distribution profiles of 40 devices based on modified HTL and ETL via hot-substrate deposition strategy.

Experimental Section

Materials: Isopropyl alcohol (IPA) (99.5%, Sigma-Aldrich), *N,N*-dimethyl formamide (DMF) (99.5%, Sigma-Aldrich), dimethylsulfoxide (DMSO) (99.5%, Sigma-Aldrich), 2-butanol (99.5%, Sigma-Aldrich), chlorobenzene (CB) (99.5%, Sigma-Aldrich), ethanol (99.5%, Sigma-Aldrich), PbI_2 (99.999%, Alfa Aesar), PEDOT:PSS (Germany, Heraeus, Clevios PVP AI 4083), [6,6]-phenyl-C_{61}-butyric acid methyl ester ($PC_{61}BM$), and 4,7-diphenyl-1,10-phenanthroline (Bphen) (Taiwan, Nichem Fine Technology Co. Ltd.) were used. CH_3NH_3I (MAI) was typically synthesized using a published method in the literature.[32]

Device Fabrication: Solar cells with the ITO/PEDOT:PSS/PTPD/$MAPbI_3$/PCBM/Bphen/Al planar device structure were used. Before device fabrication, the ITO glass substrates were cleaned with water, acetone, and IPA in sequence. The ITO glass was illuminated under the UV cleaner for 15 min; then, PEDOT:PSS was spin coated on the substrate at a rotation speed of 3000 rpm for 35 s, followed by thermal annealing at 120 °C for 15 min. The perovskite precursor solution was prepared by mixing 922 mg PbI_2 and 349.8 mg MAI in a 1 mL DMF and DMSO mixed solvent (vol/vol = 9:1). The perovskite films were deposited on HTL substrates heated to various temperatures (RT (≈20 °C), 60, 90, and 110 °C) via spin coating at 6000 rpm for 30 s. Then 220 µL of 2-butanol was used as the antisolvent and was casted on the perovskite film at the 9th second during the spin-coating process (in an N_2-filled glovebox). The perovskite films were immediately transferred onto a hotplate at 110 °C for 1 min before being washed by another 220 µL of 2-butanol to remove the extra MAI. Then, the perovskite films were annealed at 100 °C for 15 min (in ambient air) and then under DMSO vapor at 100 °C for 15 min with a Petri dish covering them.[33] The PCBM ETL was deposited by spin coating the solution of 20 mg mL^{-1} of PCBM in chlorobenzene at 2500 rpm for 30 s on the perovskite substrate at different temperatures (RT (≈20 °C), 62, 82, and 94 °C). The substrate temperature was controlled by transferring the 110 °C preheated perovskite substrates to the spin coater for different cooling times (5 s (94 °C), 15 s (82 °C), 35 s (62 °C), 300 s (22 °C: ≈RT)). The actual temperature of the substrate was measured using an IR temperature thermoscope. All of the perovskite substrates were preheated at 100 °C for 3 min, and their temperatures for the next deposition were controlled according to when they were removed from the hot plate. A 0.7 mg mL^{-1} Bphen solution in ethanol was then spin coated at 4000 rpm for 30 s. Finally, a 100 nm Al electrode was deposited via thermal evaporation through a metal mask. The active device area was set as 0.12 cm^2 by the overlapping area between the top Al cathode and bottom ITO anode.

Film and Device Characterization: The simulated solar irradiation (AM 1.5, 100 mW cm^{-2}) was provided via a sun simulator (Zolix Sirius-SS). The typical current–voltage characteristics of the devices were measured using a Keithley 2400 source meter by reverse scanning from 1.2 to –0.5 V or forward scanning from –0.5 to 1.2 V at a scanning speed of 0.05 V s^{-1}. The output of the light source was adjusted using a calibrated silicon photodiode (ABET technology). The IPCE spectra were measured using a power source (Zolix Sirius-SS) with a monochromator (Zolix Omni-λ) and a source meter (Keithley 2400). The device area (0.12 cm^2) was determined by the overlap of the cathode and anode. Scanning electron microscopy (SEM) images of the films were obtained with a Zeiss Supra 55 microscope. The PL lifetime distribution was measured using the DCS 120 with an excitation laser of 600 nm (40 mHz, laser facula diameter: ≈10 µm).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Conflict of Interest

The authors declare no conflict of interest.

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