LOW TOTAL HARMONIC DISTORTION (THD) RESONANT CONVERTER FOR COOKER MAGNETRON POWER SUPPLY

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Western Carolina University in partial fulfillment of the
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By

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ABSTRACT

LOW TOTAL HARMONIC DISTORTION (THD) RESONANT CONVERTER FOR COOKER MAGNETRON POWER SUPPLY

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The traditional cooker magnetron power supply consists industrial frequency transformer, which is bulky, inefficient and with high harmonics distortion. There are numerous researchers who investigates magnetron power supply design with soft switching converter, in order to reduce weight and improve efficiency [7–10]. However, no investigation currently exists on harmonic distortion of traditional magnetron power supply, and very little research or analysis is done on harmonic distortion of new type of magnetron power supply. This project aims to investigate harmonic distortion of traditional magnetron power supply in the first phase. In the second phase, a novel design of high frequency and low harmonic distortion magnetron power supply is targeted.

CHAPTER 1: INTRODUCTION

1.1 Traditional Microwave Oven

In 1945, an engineer in Raytheon Percy Spencer discovered that the magnetron built in the war period can be a promising application for heating food [11], and then Raytheon invented the first commercially available microwave oven [12]. The most important component in microwave oven is the magnetron which works as the source of microwave power. The advent of the microwave oven makes the magnetron well-known and popular

1.1.1 Magnetron Characteristics

Figure 1.1 is a picture taken from a 2008 Emerson microwave oven, which shows the structure of the magnetron for microwave oven. The internal construction of the magnetron includes a cylindrical cathode and an anode on a larger concentric circle, permanent magnet axially produces the magnetic field to accelerate electrons [13]. At start-up stage, the cathode filament is heated until the filament temperature rises up to the critical value, then the filament begins to emit electrons. Within the magnetic fluxes produced by two ring magnets, the accelerated electrons make the anode cavities resonate and radiate microwaves [14].

Figure 1.2 represents the voltage vs. current characteristics of the magnetron. The magnetron has very high resistance when operates in non-oscillating range, and low resistance when operating in the oscillating range which is shown in Figure 1.2. When the voltage applied between the anode and the cathode exceeds 3.6 kV, the magnetron anode current starts to increase rapidly. However, when the voltage is lower than 3.6 kV [15], the resistance between anode and cathode is very high which is considered as ’OFF’ state.

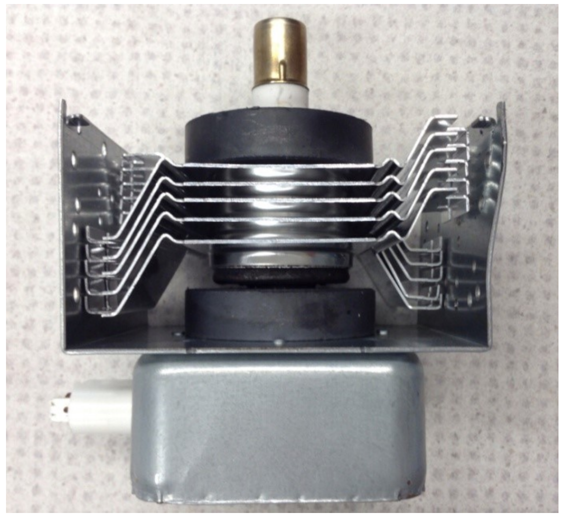


Figure 1.1: Magnetron Structure

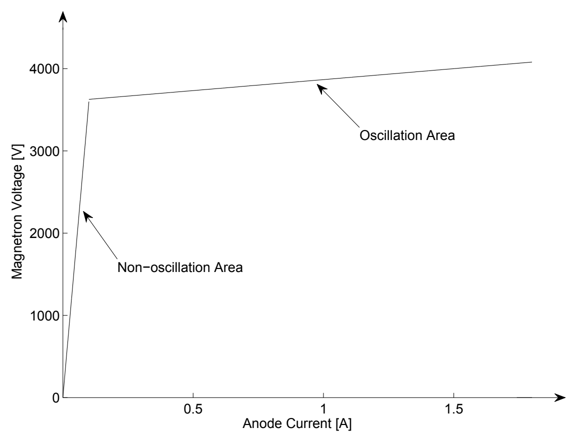


Figure 1.2: Magnetron Voltage and Current

1.1.2 Traditional Power Supply of the Magnetron in Microwave Oven

The mainstream microwave ovens on the market are supplied by a traditional power supply which is shown in Figure 1.3 and Figure 1.4. The picture in Figure 1.3 is a traditional magnetron power supply taken from a 2008 made Galanz microwave oven. The circuit diagram of the traditional power supply is shown in Figure 1.4.

As shown in Figure 1.4, the magnetron power supply is fabricated by a line-frequency transformer, a capacitor and a diode. The 120V-60Hz line voltage is boosted by a line-frequency transformer. The output voltage of the transformer is rectified by a half-wave rectifier which is composed of a capacitor and a diode.

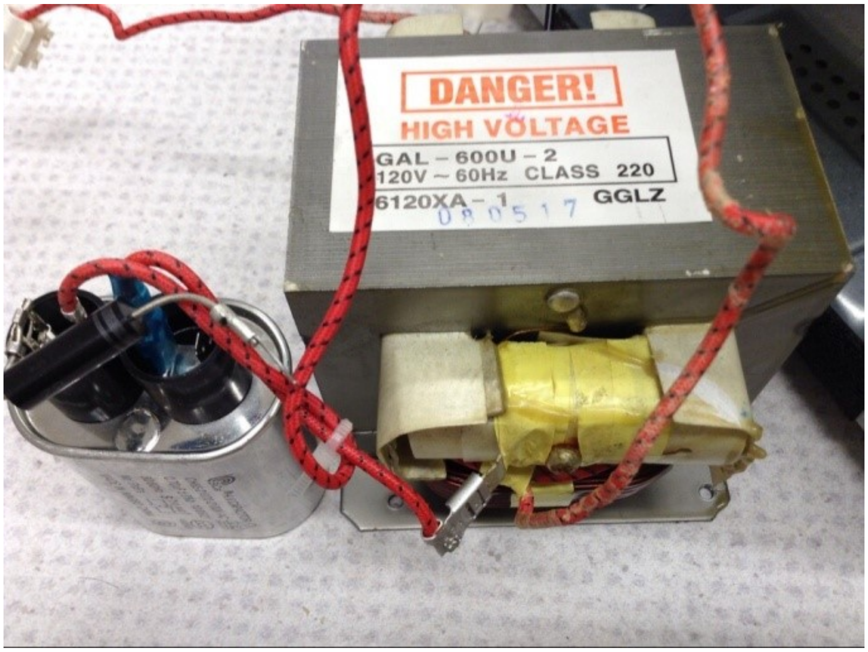


Figure 1.3: The Picture of Traditional Magnetron Power Supply

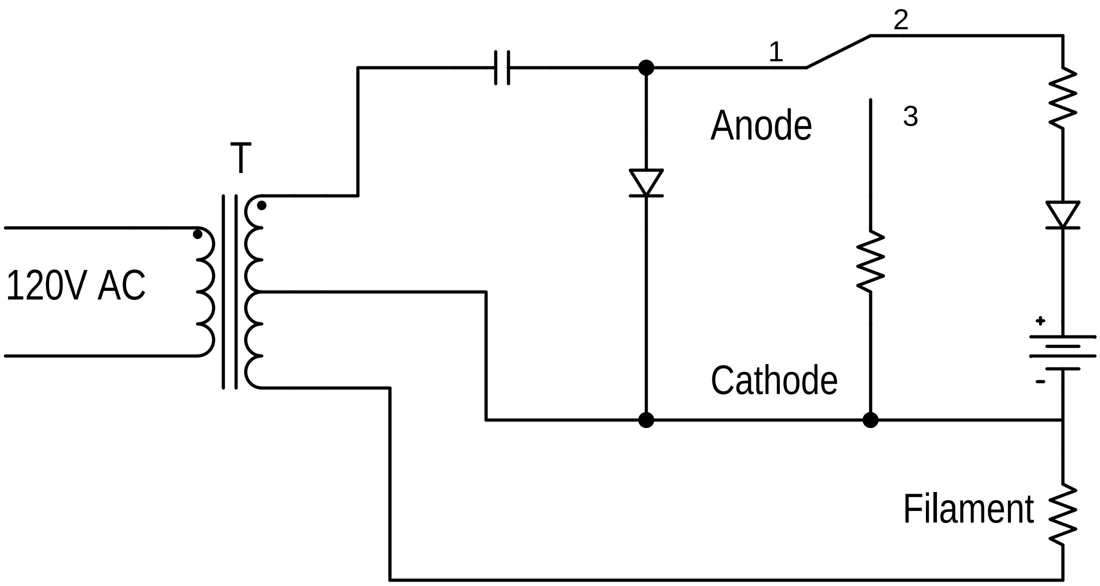


Figure 1.4: A Circuit Diagram of Traditional Magnetron Power Supply

1.1.3 Advantages and Disadvantages of the Traditional Power Supply

The traditional magnetron power supply has many advantages. The circuit of the power supply is very simple as shown in Figure 1.4, which means the power supply can be cheap and reliable. Therefore this kind microwave oven lasts for decades and can keeps its popular.

However, there are also several significant drawbacks with traditional microwave ovens:

First, the current distortion is significant [16]. The lab test was performed on a 2008 made Emerson microwave oven as shown in the Table 1.1 and Figure 1.5. The total harmonic distortion (THD) can be calculated using:

$$THD = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + I_5^2 + K}}{I_1} \tag{1.1}$$

where I_n is the nth harmonic of the power supply current. K is a sum of all the other higher order harmonics. In this experiment, THD was shown to be 42.92% with K set to zero. In this experiment K was not zero and increased the THD to approximately 45%. That means the MW oven wastes 45% of the consumed energy. This level of THD in current can result in undesired effects in the power grid. At the same time, when the oven is turned on, creating many harmonics, it will make the current through the grid *dirty*, which will have deleterious effects on other equipment connected within the same power grid.

Table 1.1: Harmonic Results from Lab Test

Order / Value	I_1	I_2	I_3	I_4	I_5
Decibels (dBA)	57.5	33.0	50.0	24.0	35.0
Scaled Current (A)	749.0	44.0	316.0	16.0	36.0

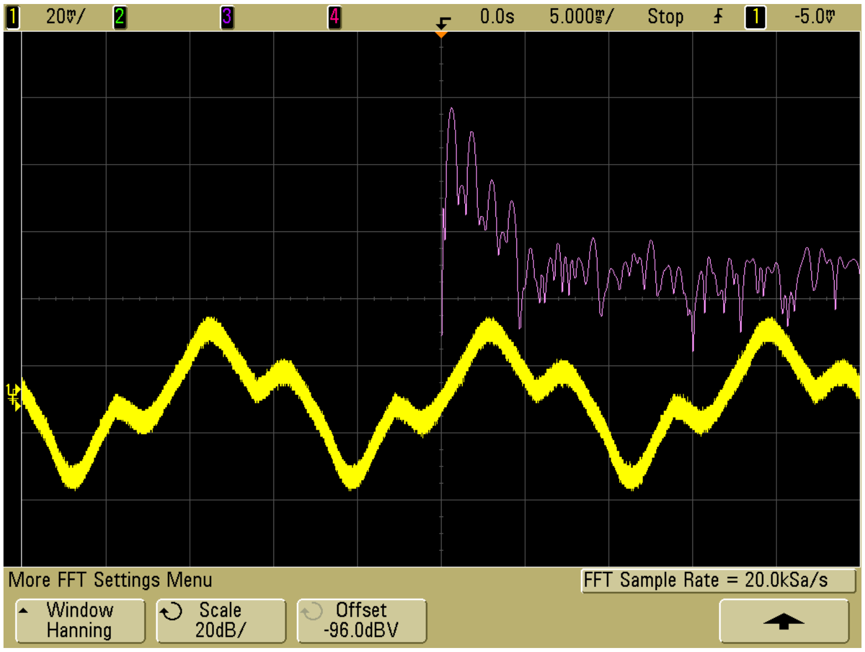


Figure 1.5: Input Current of MW (Microwave) Oven and Its Fast Fourier Transform

Secondly, when the user adjusts the output power, the power supply repeatedly turns on and off to control the total amount of output energy [8]. Continuous adjustment of power is not possible. Since the adjustment is not continuous, there will be numerous current shocks on the magnetron and transformer.

Thirdly, the traditional power supply system is very bulky. The weight of the transformer and capacitor in the Figure 1.3 is about 3kg.

Fourthly, the traditional power supply system creats significant audible noise. Since the current has a fundamental frequency of 60 Hz, it produces a physical resonance which is in the human-audible sound range.

1.2 A New Magnetron Power Supply

To improve the efficiency and reduce the weight and volume of the magnetron power supply, switching mode magnetron power supplies are introduced. The output voltage of the power supply is up to 4kV. For hard-switching converters, the current and voltage spikes cause much switching noise and high switching loss. To solve the problem of noise and reduce the switching loss, soft-switching resonant converters are developed [17].

1.2.1 LLC (Inductor-Inductor-Capacitor) Resonant Converter

The LLC resonant converter is a type of series-parallel converter. LLC resonant converters combine characteristics from series converters and parallel converters. When the load or input voltage have wide variations, it is easy to adjust the output power by changing the switching frequency. It can achieve zero voltage switching (ZVS) across the operational range. Figure 1.6 shows the LLC resonant network. Another advantage of the LLC topology is that the two inductors in the resonant network shown in Figure 1.6 can be integrated into the transformer, including the leakage inductance Lr and magnetizing inductance Lm [2].

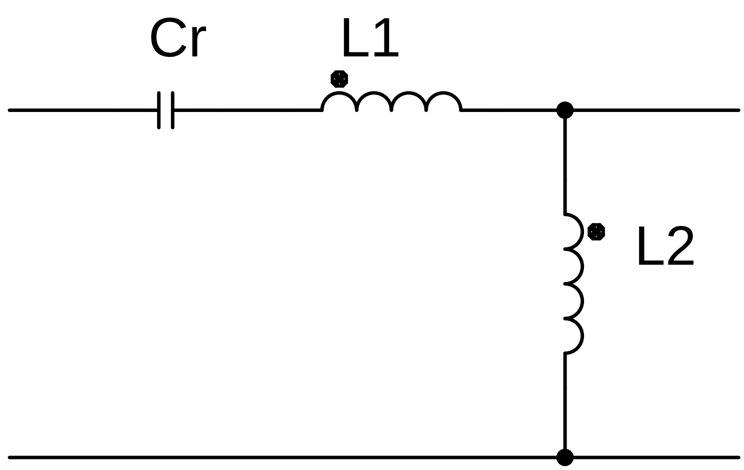


Figure 1.6: LLC Resonant Network

1.2.2 A New Magnetron Power Supply Based on LLC Resonant Converter

Figure 1.7 is the simplified main circuit of the proposed power supply system with resonant circuit. This design is a modification from LLC converters which often are used to increase power efficiency in many appliances [10, 15]. In this study, the LLC network will be used to boost the voltage rather than being used as a voltage step-down application. In this figure, a high frequency resonant circuit will be applied before the transformer in the power supply system. This resonant power supply is composed of an input rectifier bridge, switching bridge, resonant circuit, transformer and output rectifier.

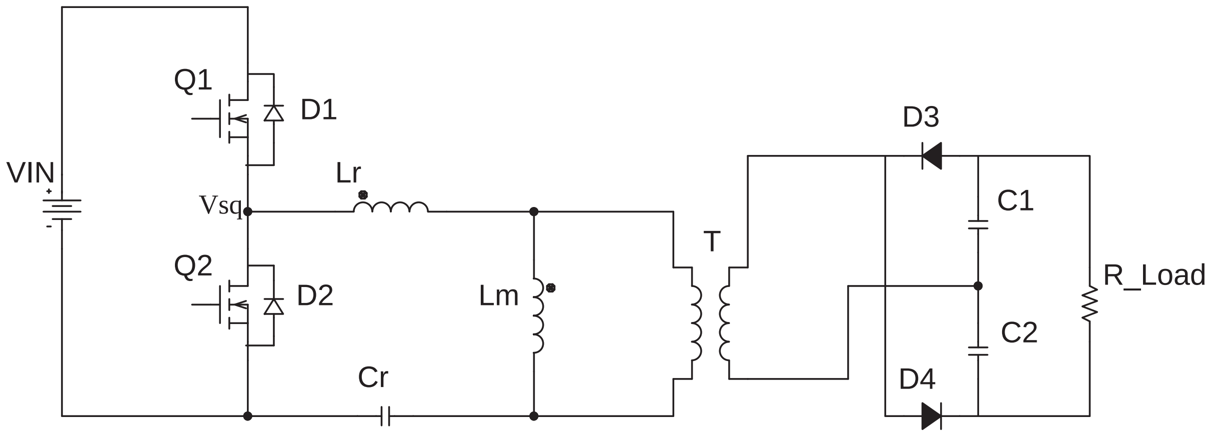


Figure 1.7: Simplified Main Circuit

The power supply system with resonant circuit in this research will have some main advantages as compared to traditional power supply.

Firstly, the resonant frequency can be up to 150 kHz which is much higher than 60 Hz in the traditional power supply system. Also, the output voltage can be adjusted to keep steady when the input sinusoidal voltage goes down periodically. Therefore the large capacitor can be replaced by a much smaller one. The smaller capacitor will result in a much smaller phase shift between voltage and current.

Secondly, the output power can be adjusted continuously, as opposed to a pulse output, because the voltage gain of the resonant circuit can be changed by changing the frequency of the switching signal on the IGBT (Insulated-gate Bipolar Transistor) device. [18, 19]

Thirdly, the IGBT devices in the switching bridge chop up the input line frequency voltage to be a much higher frequency voltage. Higher frequency voltages require a small-volume transformer if the same power is needed to be transferred. The output voltage filter capacitor can be much smaller too. So, the weight of the power supply system with resonant circuit may be significantly reduced.

Fourthly, as noted above, the frequency of the current is larger than 20 kHz which is beyond the range of human hearing. The noise of the traditional MW oven should disappear.

1.3 Other Studies on LLC Resonant Based Magnetron Power Supplies

The LLC resonant based magnetron power supply has been studied in one published paper [15]. The math derivations for the LLC converter with a voltage doubling rectifier is not completely correct in this paper. The IGBTs are adopted as switches in the LLC resonant converter, therefore the operation frequency range is around 30 kHz. The switching mode power supply with 1000 Watts output, the total harmonic distortion (THD) is not discussed in this paper or compared with the traditional Microwave oven. No investigations on the power efficiency and closed loop control methods are discussed in this paper.

In this thesis, switching devices will be replaced by MOSFETs with higher switching frequency which can help LLC resonant converters reach to a higher efficiency [2]. The total harmonic distortion (THD) will be investigated deeply and compared with traditional power supply, as well as the power efficiency and closed loop control methods.

CHAPTER 2: LLC BASED MAIN CIRCUIT ANALYSIS

2.1 Topology Selection

As analyzed in the last chapter, to reduce the weight of the transformer, improving the switching frequency decreases the size of passive components. However, a high switching frequency on power devices results in a large switching loss. Therefore the resonant and soft switching technique is a good choice. The soft switching technique improves the power density and efficiency.

Resonant converters, which have been investigated in-depth in the 1980s [20, 21], can achieve very low loss even when the resonant converter operates at a very high switching frequency. There are three typical resonant topologies, Series Resonant Converter (SRC), Parallel Resonant Converter (PRC) and Series-Parallel Resonant Converter (SPRC).

2.1.1 Series Resonant Converter (SRC)

The circuit diagram of the SRC network is shown in Figure 2.1. The SRC network is a series combination of an inductor and a capacitor. The load is a voltage dividing part connected in series with the SRC network. Changing the input frequency will change the impedance of the SRC network, and then consequentially change the load voltage. Since the load is connected in series with the network, the output voltage gain is always less than or equal to 1.

The AC voltage gain characteristic plot is shown in Figure 2.2. The SRC has three main weaknesses. Firstly, the range of output voltage is limited. The output voltage of the power supply used to power the magnetron needs to have a broad range in order to change the output microwave power. Secondly, it can be seen from the Figure 2.2 that at light load, the switching frequency needs to be very high to keep the output voltage regulated. Theoretically, the switching frequency has to be infinite at zero load. Thirdly, in this topology, the SRC network stores a lot of energy, especially with a light load. The large inrush turn-off current on the switch is also a big challenge.

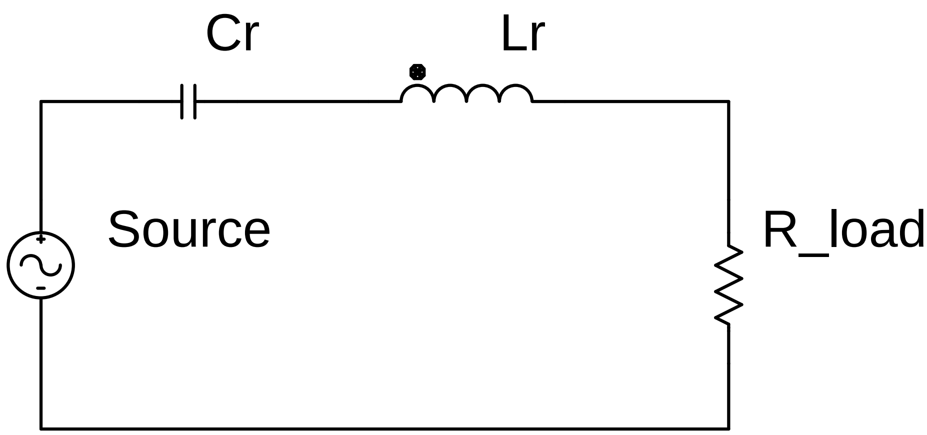


Figure 2.1: Series Resonant Converter

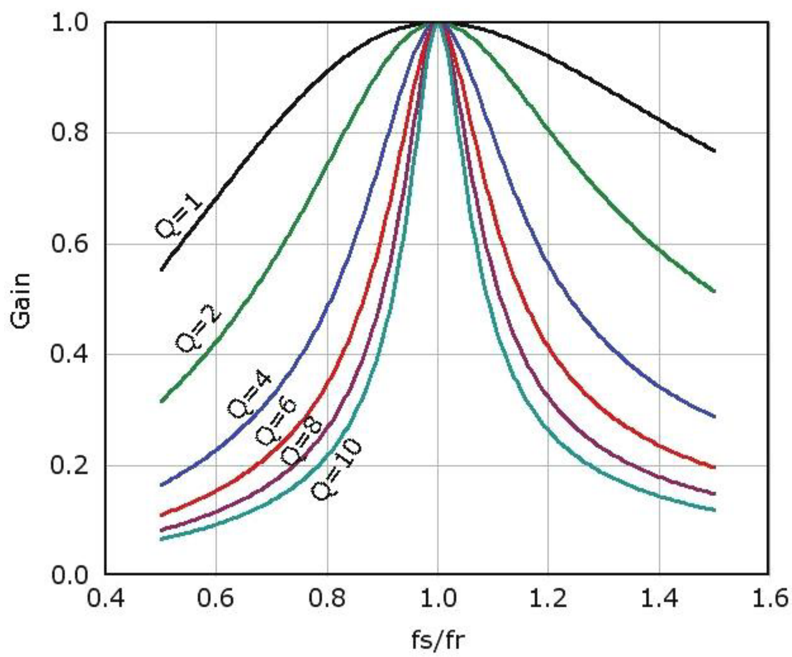


Figure 2.2: SRC Voltage Gain [1]

2.1.2 Parallel Resonant Converter (PRC)

The circuit diagram of the PRC network is shown in Figure 2.3.For the PRC, the resonant tank is in series, similar to the SRC. The difference from the SRC is that the load is in parallel with the resonant capacitor. The voltage gain characteristic plot is shown in Figure 2.4. The operation area is much smaller comparing with the SRC. Similar to the SRC, the operation area of Zero Voltage Switching is also on the right side of the resonant frequency (The ZVS operation area will be discussed later).

The load is in parallel with the capacitor. Since the impedance of the resonant tank is small [22], a big challenge is that the circulating current is very large at light load. Due to the PC board trace resistance, the efficiency of the converter is too low to be used on a high power application like the Microwave Oven. Similar to the SRC, the turn-off current through the switch is also very large at light load. Since the SRC and PRC both only have one resonance, they require a wide frequency shift in order to accommodate input and load variations.

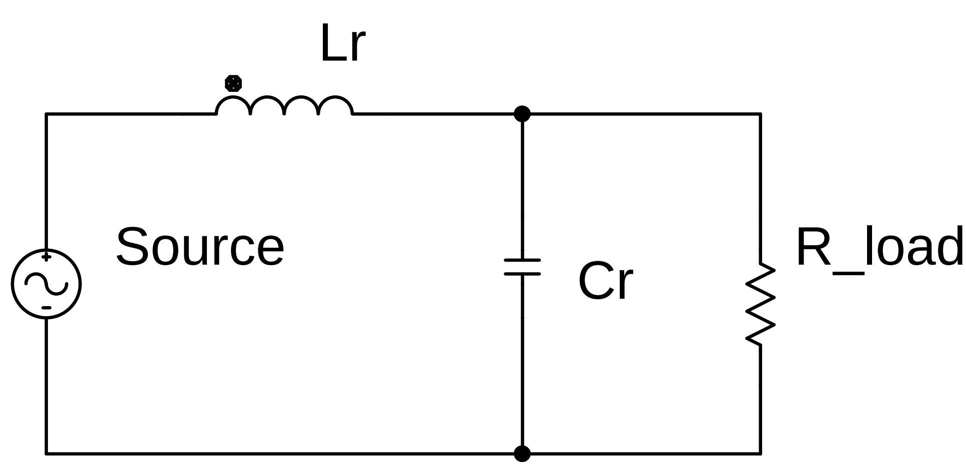


Figure 2.3: Parallel Resonant Converter

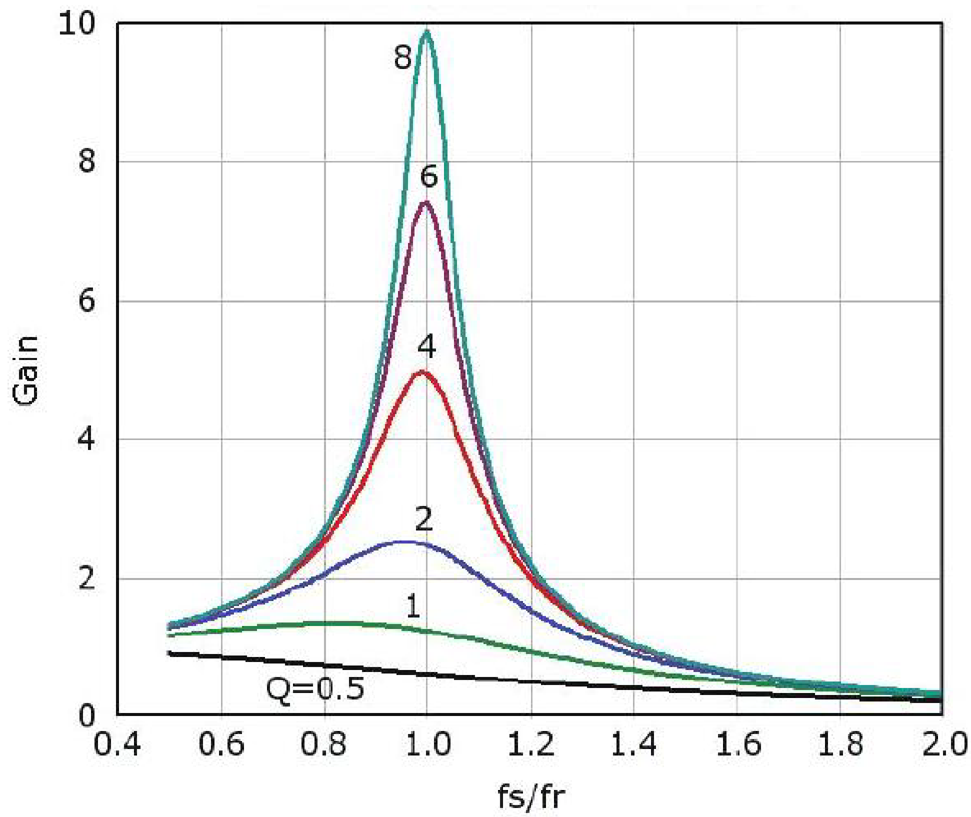


Figure 2.4: PRC Voltage Gain [1]

2.1.3 Series-Parallel Resonant Converter (SPRC)

The typical Series-Parallel Resonant network is shown in Figure 2.5, and is also known as the LCC resonant converter. It combines advantages from both the SRC and PRC. In the normal operation region, the circulating energy is much smaller compared with the SRC and PRC [19]. As shown in Figure 2.6, the operation region is still to the right side of the resonant frequency. Similarly to the SRC and PRC, it has a big problem dealing with input voltage variation. The conduction and switching losses will increase at high input voltage, which is fairly similar to PWM converter.

Changing the LCC resonant network to an LLC resonant network will shift the resonant frequency and will solve the problem of circulating energy [2]. The LLC network is shown in Figure 2.7. There are many advantages of the LLC resonant converter. For example, comparing with the LCC topology which needs two independent capacitors that are expensive and increasing the size of the system, the two inductors of the LLC topology can be integrated into a transformer

[2]. This creates a very desirable result in which the ZVS operation can be completed over the entire operating range. As shown in Figure 2.8, the LLC can regulate the output voltage under wide variations of input voltage and load without changing the range of frequency. The LLC converter is a suitable topology for power adapters with high efficiency, providing a high and nearly constant efficiency throughout the complete load and input voltage range [23].

From the above discussion, the LLC topology will be adopted for this research as the topology of the magnetron power supply, since it can achieve soft-switching, while maintaining great efficiency.

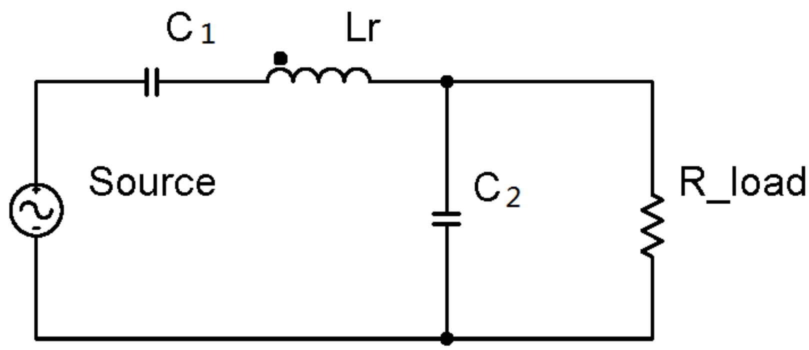


Figure 2.5: LCC Series-Parallel Resonant Converter

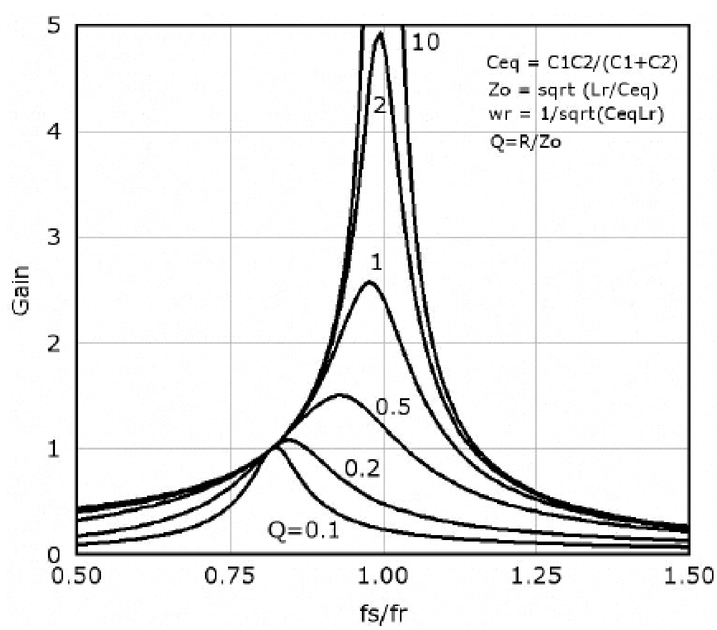


Figure 2.6: LCC Resonant Converter Voltage Gain [1]

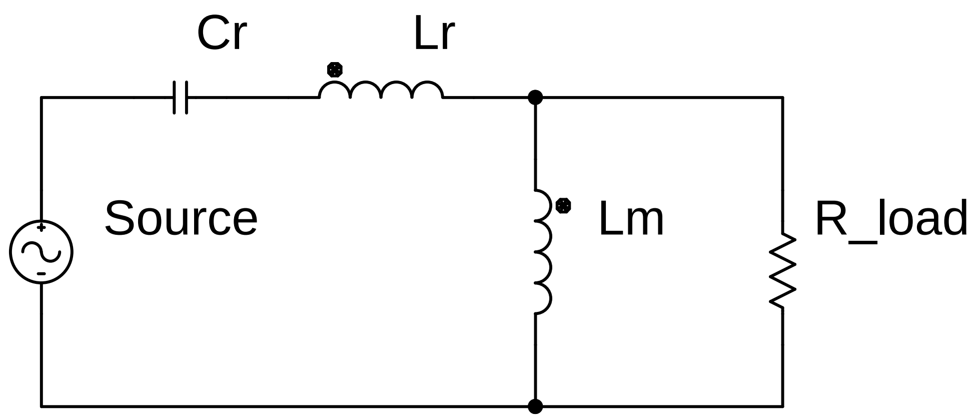


Figure 2.7: LLC Series-Parallel Resonant Converter

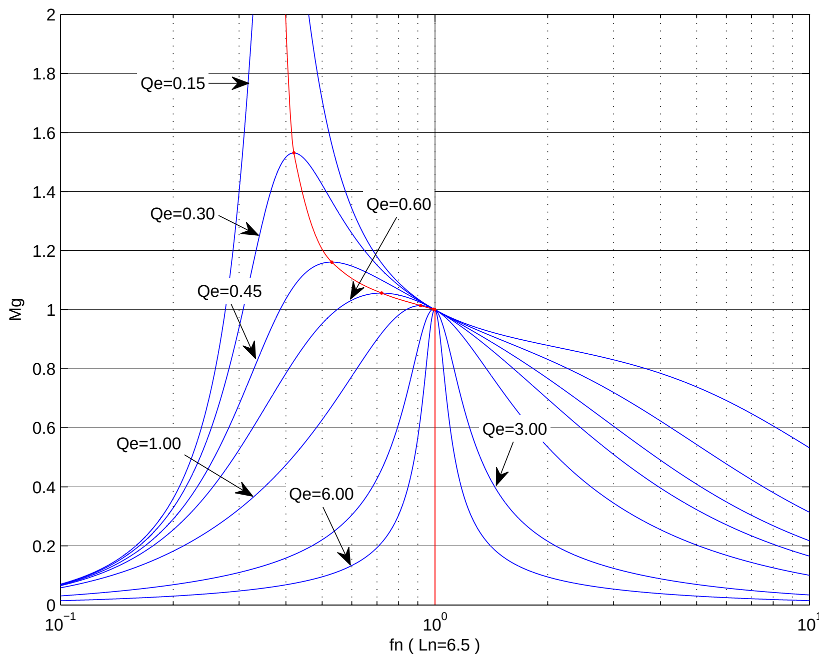


Figure 2.8: LLC Resonant Converter Voltage Gain

2.2 Mathematical Derivation of Main Circuit Voltage Gain

The main circuit of the power supply is derived from the normal LLC topology. A voltage doubler is adopted as the output network, in order to get a higher output voltage. Normally the LLC topology is used on the voltage step-down application, but the power supply needs to boost the voltage in the proposed approach.

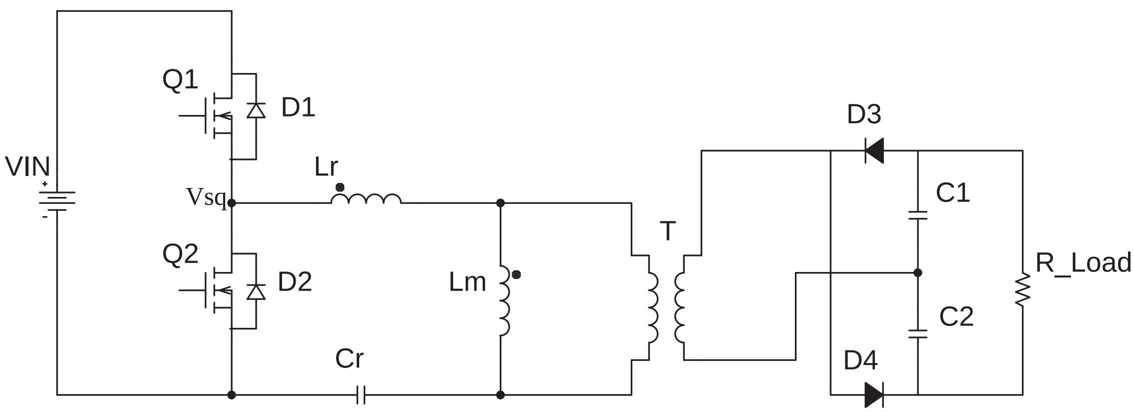


Figure 2.9: LLC Based Main Circuit

In the Figure 2.9, the DC (Direct Current) rail voltage Vin is the input voltage applied on the switching bridge. Q1 and Q2 are both high speed MOSFETs. In this application, they conduct alternately on a 50% duty cycle. L_r and C_r are part of the resonant network. In the actual circuit, L_r and L_m are integrated into the transformer as the leakage inductance and magnetizing inductance to reduce space and cost of extra components. A step-up transformer is connected to the resonant network. On the secondary side of the transformer, a rectifier doubles the voltage to satisfy the requirement of 4000V delivered to the magnetron. R_{Load} represents the magnetron's impedance. As shown in Figure 2.15, V_{sq} is the switching node voltage which alternates between zero and Vin. The math derivation of the main circuit model is based on the First Harmonics Analysis (FHA) [24]. The following mathmatical analysis does not consider any loss elements. The FHA method extracts the fundamental harmonic of the square wave as an approximation.

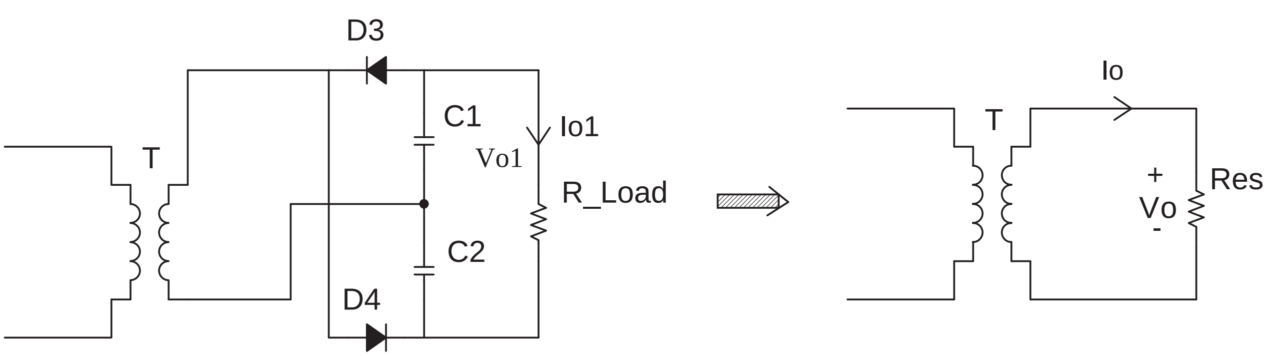


Figure 2.10: Secondary Side Equivalent

The equivalent resistance referred to the transformer secondary side R_{es} is shown in the Figure 2.10. R_{es} can be calculated using the Ohm's law as follows:

$$V_o = \frac{1}{2} V_{o1} \tag{2.1}$$

$$I_o = 2 * I_{o1} \tag{2.2}$$

$$R_{es} = \frac{V_o}{I_o} \tag{2.3}$$

$$R_{Load} = \frac{V_{o1}}{I_{o1}} \tag{2.4}$$

$$R_{es} = \frac{\frac{1}{2} V_{o1}}{2 I_{o1}} = \frac{1}{4} R_{Load} \tag{2.5}$$

The LLC resonant network has two resonant frequencies:

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2.6}$$

$$f_p = \frac{1}{2\pi\sqrt{(L_r + L_m) C_r}} \tag{2.7}$$

From the LLC based main circuit which is shown in Figure 2.9, by replacing the switching node with a square wave voltage source V_{ge}, and referring the secondary side resistance R_{es} to the primary side resistance R_e, the equivalent main circuit is obtained as Figure 2.11.

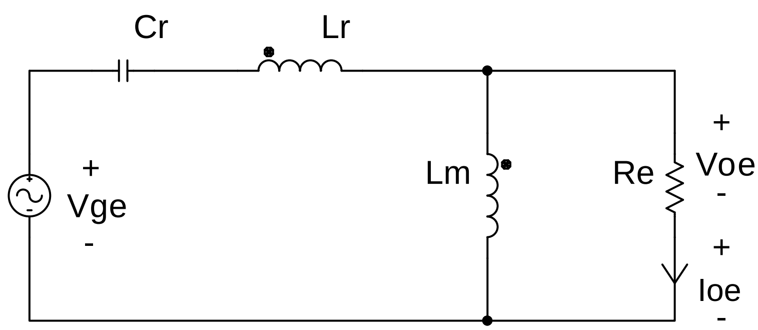


Figure 2.11: Equivalent Main Circuit

The switching bridge divides the DC input voltage into a square wave voltage, the Fourier transform of the periodic square wave is:

$$x(t) = \frac{4}{\pi} (cos(\omega t) - \frac{1}{3} cos(3\omega t) + \frac{1}{5} cos(5\omega t) - |...|) \tag{2.8}$$

The DC input voltage V_{IN} is applied on the resonant network for each half cycle. Therefore the voltage source V_{ge} is a square wave which can be decomposed as:

$$V_{ge}(t) = \frac{1}{2}\frac{4}{\pi}V_{IN}sin(\omega t) \tag{2.9}$$

$$V_{ge} = RMS(V_{ge}(t)) = \frac{\sqrt{2}}{\pi}V_{IN} \tag{2.10}$$

The fundamental harmonic of the output voltage V_{oe}:

$$V_{oe}(t) = \frac{4}{\pi}nV_{o}sin(\omega t - \phi_1) \tag{2.11}$$

$$V_{oe} = RMS(V_{oe}(t)) = \frac{2\sqrt{2}}{\pi}nV_o \tag{2.12}$$

The equivalent output current I_{oe} is derived as:

$$V_{oe}I_{oe} = V_oI_o \tag{2.13}$$

$$I_{oe} = \frac{\pi}{2\sqrt{2}}\frac{1}{n}I_o \tag{2.14}$$

The equivalent load resistance R_e is derived as:

$$R_e = \frac{V_{oe}}{I_{oe}} = \frac{8n^2}{\pi^2}R_{es} \tag{2.15}$$

$$R_{es} = \frac{1}{4}R_{Load} \tag{2.16}$$

$$R_e = \frac{2n^2}{\pi^2}R_{load} \tag{2.17}$$

Reactances of L_r, L_m and C_r:

$$X_{C_r} = \frac{1}{\omega C_r}, \quad X_{L_r} = \omega L_r, \quad X_{L_m} = \omega L_m \tag{2.18}$$

The resonant frequency f_o is determined by:

$$2\pi f_o L_r = \frac{1}{2\pi f_o C_r} \tag{2.19}$$

The magnetizing current I_m:

$$I_m = \frac{V_{oe}}{\omega L_m} = \frac{2\sqrt{2}}{\pi}\frac{nV_o}{\omega L_m} \tag{2.20}$$

The circulating current in the resonant network I_r:

$$I_r = \sqrt{I_m^2 + I_{oe}^2} \tag{2.21}$$

The Voltage gain of this main circuit M_g is calculated by using the voltage division method:

$$M_g = \frac{V_{oe}}{V_{ge}} = \frac{jX_{L_m}||R_e}{(jX_{L_m}||R_e) + j(X_{L_r} - X_{C_r})} \tag{2.22}$$

The voltage gain M_g can be normalized as:

$$L_n = L_m/L_r, \quad Q_e = \sqrt{L_r/C_r}/R_e \tag{2.23}$$

$$M_g = \frac{L_n f_n^2}{[(L_n+1)f_n^2 - 1] + j[(f_n^2-1)f_n Q_e L_n]} \tag{2.24}$$

The relationship between the input and output voltage can be expressed as:

$$V_o = M_g(f_n, L_n, Q_e)\frac{1}{n}\frac{V_{IN}}{2} \tag{2.25}$$

2.3 Analysis of Main Circuit

In this section, the characteristics of the main circuit are discussed, including the utilization of the voltage gain, the resonant converter operation and the zero-voltage switching (ZVS).

2.3.1 Voltage Gain Analysis

The expression of voltage gain M_g has been derived. After the normalization, there are three elements involved, Q_e,L_n and f_n. As suggested from the a TI handbook [2], the inductance ratio, $L_n = L_m/L_r$ is normally in the range from 3 to 7. In this application, L_n is set as 6.5; the reason will be explained later. Fixing the parameter L_n makes the voltage gain vs. frequency plot to be much more straightforward. The plot of M_g vs. normalized frequency f_n is shown in Figure 2.12.

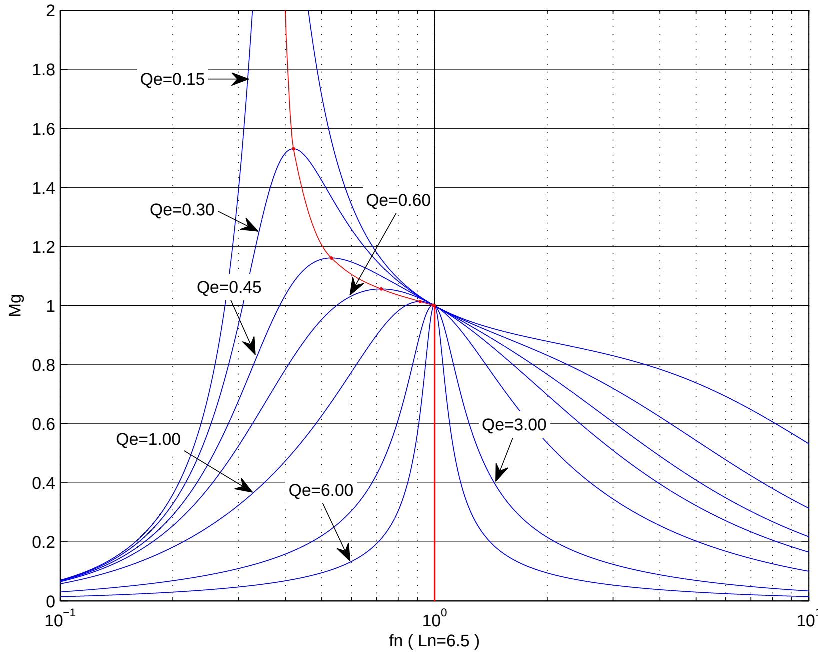


Figure 2.12: M_g vs. L_n (L_n =6.5)

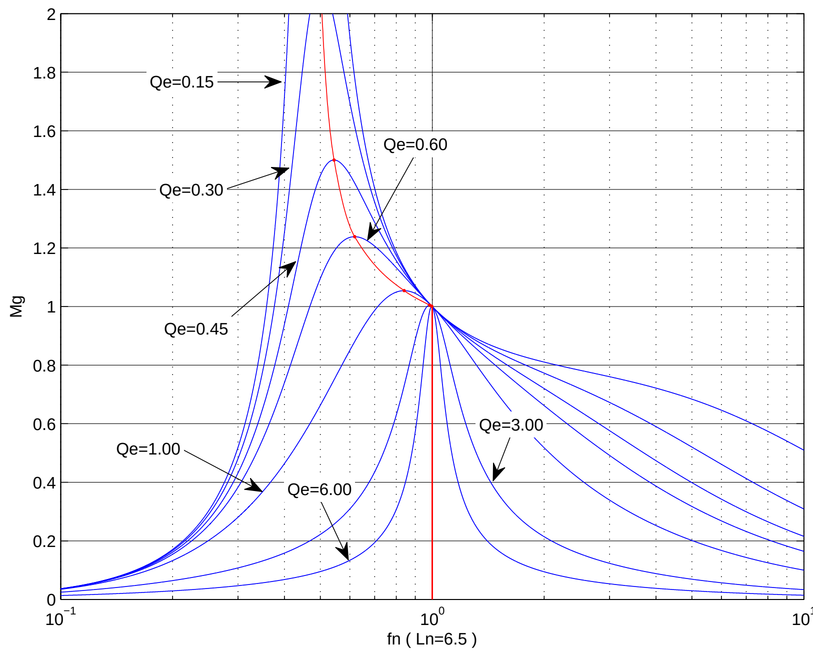


Figure 2.13: M_g vs. L_n (L_n =3.5)

With a given L_n and Q_e, M_g presents a convex curve shape, and the operation region is recommended to be in the vicinity of the network's resonant frequency. As shown in Figure 2.12

and Figure 2.13, L_n has been given as 6.5 and 3.5. Q_e is a function of the load and the parameters of network. M_g presents a family of curves regarding to the change of L_n and Q_e. Every curve goes through a same point (L_n, M_g=1). The voltage drop across L_r and C_r is zero at f_n=1, since X_{L_r}-X_{C_r} =0 at the resonant frequency point. Therefore the input voltage is applied directly on the load with a unity voltage gain.

When the Q_e is fixed, such as Q_e=0.5 shown in Figure 2.12 and Figure 2.13, decreasing L_n lifts the voltage gain and shrinks the curve. Since the voltage gain is lifted, this results in a better operation frequency band. In other words, it is easier to get an output voltage without shifting the operation frequency too much. For example, in Figure 2.12, the operating frequency range is widest for M_g between 1.1 and 1.4. However, a larger L_n results in a overall higher voltage gain and a higher start-current through the resonant network which might be beyond the current limitation of power devices.

The quality factor of the resonant network Q_e is described in Equation 2.23. In the real design, both L_r and C_r are fixed, and Q_e is only decided by the load. Increasing the load R_e will increase the effect of L_m, since R_e and L_m are parallel, and the distance between the two resonant frequency points will be increased. As observed in Figure 2.12, changing the load R_e from 0 to ∞, the corresponding peak voltage gain moves from unity to ∞.

From the above analysis, there are many considerations during the design process. The combination of f_n, Q_e and the shifting operation frequency makes the parameter selection full of compromises.

2.3.2 Operation at the Resonant Point ($f_n = 1$)

The typical waveforms on different parts of an LLC resonant converter at the resonant frequency ($f_n = 1$) are illustrated in Figure 2.15. In Figure 2.14, a capacitor C_T is added to be parallel with Q_2 comparing to Figure 2.9(There is also a capacitor C_T is parallel with Q_1). C_T is an equivalent capacitor which contains the switch's output capacitance (Coss) and stray capacitance(Cstray).

C_T needs to be considered during the transition between two switches.

$$C_T = Coss + Cstray \tag{2.26}$$

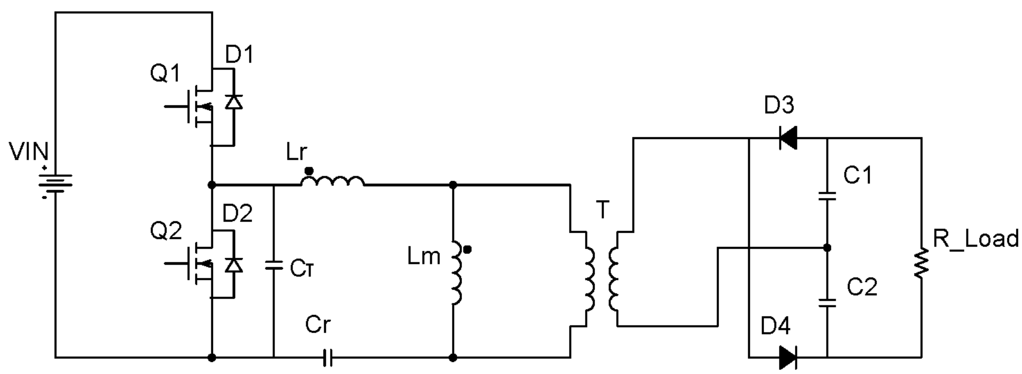


Figure 2.14: Main Circuit with Stray Capacitance

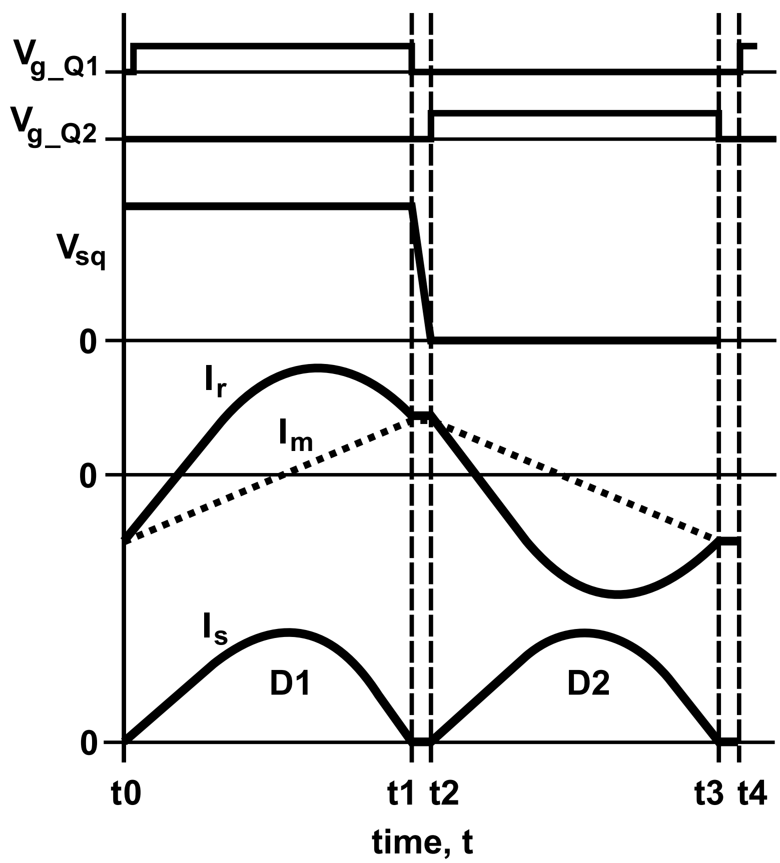


Figure 2.15: Operation of LLC Resonant Converter at f_0 [2]

When the LLC resonant converter operates at the resonant point ($f_n = 1$), a whole operation cycle contains four stages which is shown in Figure 2.15. V_{sq} is the switching node voltage. The analysis of one whole operation cycle is stated as below:

$t_0 \sim t_1$: At t_0, the switch Q1 turns on. C_T has been fully charged, and the switch node voltage is equal to the input voltage. I_r=I_m<0 at t=t_0. Both I_r and I_m increase after t_0, from negative to positive. I_r is always larger than I_m during this stage, a positive current presents on the transformer's primary side. The diode D_4 is forward biased, and charges C_2. At this stage, the voltage on the magnetizing inductor L_m is clamped by the output voltage, thus L_m doesn't resonate with L_r and C_r.

$t_1 \sim t_2$: At t_1, the switch Q_1 turns off. C_T starts to discharge at t1 until the voltage on C_T decreases to zero. In other words, the switch node voltage equals to zero. $I_r = I_m > 0$ at $t = t_1$. I_r is still positive after Q_1 is turned off. I_r can't flow back to input voltage source, instead circulating in the resonant network. A positive current flows through the diode D_2, the voltage on Q_2 is zero and Q_2 is ready for ZVS conduction. At t_1, $(I_r - I_m)$ is zero which means there is no current flowing through the transformer's primary side. Lm participates into the resonant network. The resonant period becomes much larger, so that I_r and I_m decrease very slow during $t_1 \sim t_2$.

$t_2 \sim t_3$: At t_2, the switch Q_2 is softly turned on. C_T has been fully discharged, the switch node voltage is zero. $I_r = I_m > 0$ at $t = t_2$, and then both I_r and I_m begin to decrease from positive to negative along the resonant sinusoidal current wave. I_m is always larger than I_r, thus a negative current presents on the transformer's primary side. The diode D_3 is forward biased, and charges C_1 during this stage. The same as in the first stage $t_0 \sim t_1$, the voltage on L_m is clamped by the output voltage, and the resonant network only contains L_r and C_r.

$t_3 \sim t_4$: At t_3, the switch Q_2 turns off. I_r is negative and starts to charge C_T. The switch node voltage rises from zero to input voltage. The negative current I_r can't circulate in the resonant network, instead flowing back to the input voltage source through the switch Q_1. The negative current flows through the diode D_1, the voltage on Q_1 is zero and Q_1 is ready for ZVS conduction. The same as in $t_1 \sim t_2$, L_m resonating with L_r and C_r results in a much longer resonant period.

2.3.3 Zero-Voltage Switching (ZVS)

Soft-switching is a major benefit of the LLC converter topology which significantly reduces switching loss. ZVS occurs when a switch device, such as a MOSFET,which turns on only when the drain-source voltage V_{DS} is reduced to zero [25]. In this research, the way to achieve zero V_{DS} is to force a reversal current flowing through the MOSFET's body diode when a positive gate signal is applied.

As analyzed before, such as in $t_1 \sim t_2$ stage shown in Figure 2.15, because the switch Q_1 turns off, the positive current keeps flowing, and makes the diode D_2 forward biased and prepares conditions needed for achieving ZVS. After Q_1 turns off, the current I_r remains positive for a while and then decreases to be negative. In other words, the current I_r lags the voltage applied on the resonant network which can be observed in Figure 2.15. The condition required to achieve lagging current is to make sure the input impedance, Z_{in} (shown in Figure 2.15) is inductive.

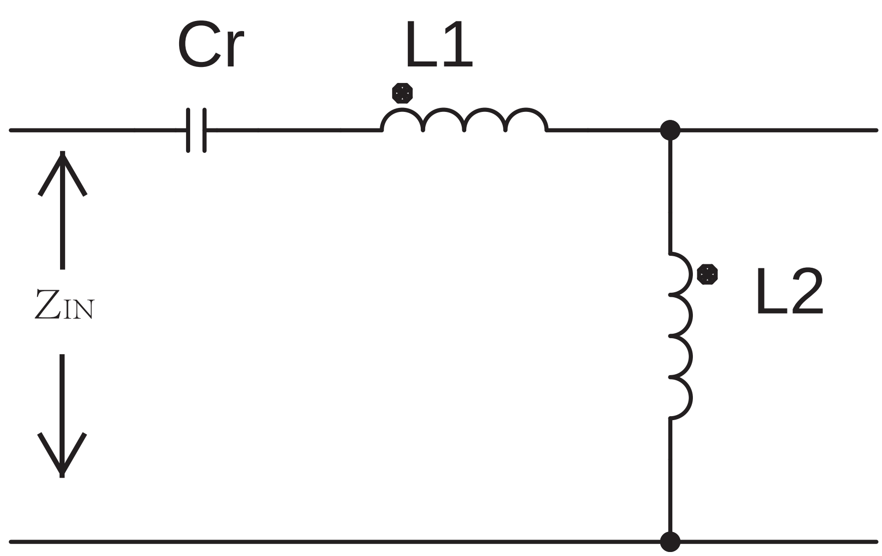


Figure 2.16: LLC Network Input Impedance

Zin can be expressed in a polar form:

$$Z_{IN} = |Z_{IN}|e^{j\theta} \tag{2.27}$$

θ is the phase angle between I_r and the input voltage. When $\theta > 0$, the input impedance Z_{IN} is inductive. As discussed before, the angle between I_r and V_{IN} is a function of switching frequency. As shown in Figure 2.12, each gain peak point corresponds to $\theta = 0$. These peak points are connected by a red line in the Figure 2.12. A higher frequency results in a larger impedance presented on L_r, but a smaller impedance on C_r. Therefore the right side of the red line represents the inductive region. To achieve ZVS, the operation region has to be in the inductive region.

The equivalent capacitor C_T which is parallel to the switch Q_2 cannot be ignored. The energy stored in this capacitor determines the achievement of ZVS. Such as in the stage $t_3 \sim t_4$, after Q_2 turns off, the negative I_r starts to charge C_T. Only when C_T is fully charged, I_r begins to flow through the diode D_1. Therefore the negative flowing energy in the resonant network needs to be large enough to make sure C_T can be fully charged during $t_3 \sim t_4$.

2.4 Design Implementation

The converter's electrical specifications in this thesis are given as follows:

- Input voltage: 97 to 118 VDC
- Rated output power: 1000 W
- Output voltage: 4000 VDC
- Rated output current: 0.25 A
- Output voltage line regulation: <= 5%
- Efficiency (V_{IN}=108 V and I=0.25 A) >= 90%
- Switching frequency (normal operation): 60 to 140 kHz

The input voltage is a 10% fluctuation from the nominal 108 V rectified grid voltage.

Design Steps:

1. Determine the Transformer Turns Ratio (n)

The theoretical turns ratio is computed as:

$$n = (VIN/2)/(V_o/2) = (108/2)/(4000/2) = 0.027 \approx 0.025(1:40) \tag{2.28}$$

From the reference [26], the industry adjusted turns ratio is computed as:

$$n1 = n\sqrt{L_m/(L_m + L_r)} = 0.027\sqrt{6.5/(6.5+1)} = 0.025 \tag{2.29}$$

2. Determine the voltage gain from the DC rail to the normalized secondary voltage (M_g_min and M_g_max):

$$M_g\_min = nVo\_min/Vin\_max = n[4000(1-5\%)]/[108(1+10\%)] = 0.80 \tag{2.30}$$

$$M_g\_max = nVo\_max/Vin\_min = n[4000(1+5\%)]/[108(1-10\%)] = 1.08 \tag{2.31}$$

To implement a 10% safety margin for an overload current capability of 110%, M_g_max is adjusted from 1.08 to 1.08*110% = 1.19.

3. Calculate the equivalent load resistance (R_e)

$$R_e = 2 * n^2/(\pi^2) * R_L = 2 * 0.027^2/(\pi^2) * 16000 = 2.36\Omega \tag{2.32}$$

4. Select the L_n and Q_e

Based on the Spice simulation in Chapter 4, L_n and Q_e are selected as 6.5 and 0.4. From Figure 2.12, the corresponding peak of the voltage gain M_g is 1.25, which satifies the required M_g maximum of 1.19.

5. Calculate Resonant Circuit Parameters

The resonant parameters, C_r, L_r and L_m, are determined by Equations 2.19 and 2.23. A switching frequency of 80 kHz is selected as the series resonant frequency f_o.

$$C_r = \frac{1}{2 * 2\pi * Q_e * f_o * R_e} = \frac{1}{2 * 2\pi * 0.4 * 80kHz * 2.36} = 2.1\mu F \tag{2.33}$$

$$L_r = \frac{1}{(2\pi * f_o)^2 * C_r} = \frac{1}{(2\pi * 80kHz)^2 * 2.1\mu F} = 1.88\mu H \tag{2.34}$$

$$L_m = L_n * L_r = 1.88\mu H * 6.5 = 12.27\mu H \tag{2.35}$$

CHAPTER 3: HARDWARE DESIGN

In this Chapter, transformer design, component selection, MOSFET driver IC and protection circuit will be discussed in detail. The signal processor is selected as TI 2000 DSP controller.

3.1 Integration Transformer Design

As discussed in Chapter 2.3, the LLC resonant topology has many advantages. One of these advantages is that the LLC contains two inductors which can be integrated into the transformer. Therefore this study will use the existing inductors in the transformer as part of LLC implementation. Thus the leakage inductance and magnetizing inductance of the transformer can be effectively utilized.

The transformer is a device which can provide energy storage and delivery, current filtering and electrical isolation. To achieve high power density of the power supply, the transformer design is one of the most key elements. There are many ways to reduce the loss and improve the power density. Magnetic integration is one of the methods that has been studied recently, and applied into real products [27]. The transformer design will be shown as following step by step.

3.1.1 The List of Transformer Parameters

$Input:$	$54V, 20A$
$Output1:$	$2000V, 0.5A$
$Output2:$	$7V, 0.5A$
$Topology:$	$Half-Bridge$
$Switching\ Freq:$	$80kHz$
$Max\ Core\ Loss(Pclim):$	$2.0W$

3.1.2 Core Selection

Ferrite cores are the most often used in switched mode power supply design. The relative permeability μr of ferrite is between 1500-3000. Ferrite materials are popular because of their lower cost and lower loss as compared with powdered metal materials; Ferrite materials have the disadvantage of a lower saturation flux, however in high frequency applications, the required saturation flux density is usually very low. In this thesis, Mn-Zn ferrites are chosen as the core material. TDK Corporation provides a list of large size Mn-Zn ferrites for high power [3]. Ferrite PC40 from TDK is selected as the core material. Figure 3.1 gives the key characteristics of PC40, and core loss vs. temperature characteristics is shown Figure 3.1.

Initial permeability μi	Curie temperature Tc (°C)	Saturation magnetic flux density Bs (mT) H=1194A/m		Remanent flux density Br (mT) H=1194A/m	Coercive force Hc (A/m) H=1194A/m	Core loss Pcv (kW/m^3) B=200mT			Electrical resistivity ρ (Ω • m)	Approximate density dapp (kg/m^3) ×10^3	Thermal expansion coefficient α (1/K) ×10^{-6}	Thermal conductivity κ (W/mK)	Specific heat Cp (J/kg • K)	Bending strength δb3 (N/m^2) ×10^7	Young's modulus E (N/m^2) ×10^{11}	Magnetostriction λs ×10^{-6}
						25kHz		100kHz								
23°C		23°C	100°C	23°C	23°C	90°C	100°C	100°C								
2300	>200	500	380	125	15	64	70	420	6.5	4.8	12	5	600	9	1.2	–0.6

Figure 3.1: PC40 Material Characteristics [3].

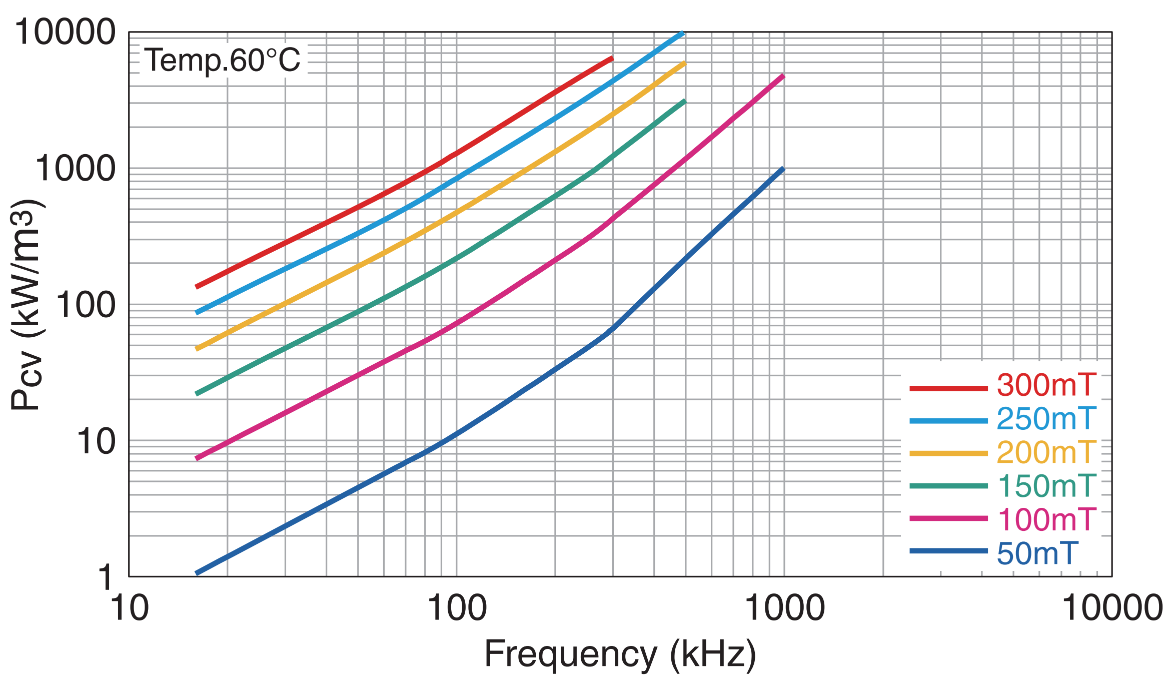


Figure 3.2: PC40 Core Loss vs. Freq at 60 Hz [3].

There are many ways to estimate the size of the core. The Area Product ('AP') method is adopted in this transformer design [26]. The following formula gives an estimation of the area product required:

$$AP = A_W A_E = \frac{P_O}{K \bigtriangleup B \, f_0} \tag{3.1}$$

where:

$$\begin{aligned}
Po &= Power\ Output\ in\ Watts \\
\Delta B &= Flux\ Density\ Swing\ (Per\ Cycle), Tesla \\
f_0 &= Main\ Operating\ Frequency\ in\ Hz \\
K &= 0.014 (Forward\ converter) \\
&= 0.017 (Bridge, Half Bridge)
\end{aligned}$$

A diagram of the EE core is shown below in Figure 3.3. EE cores are less expensive, and have the advantage of a simple bobbin winding. In this thesis, the EE shape will be adopted as the core shape.

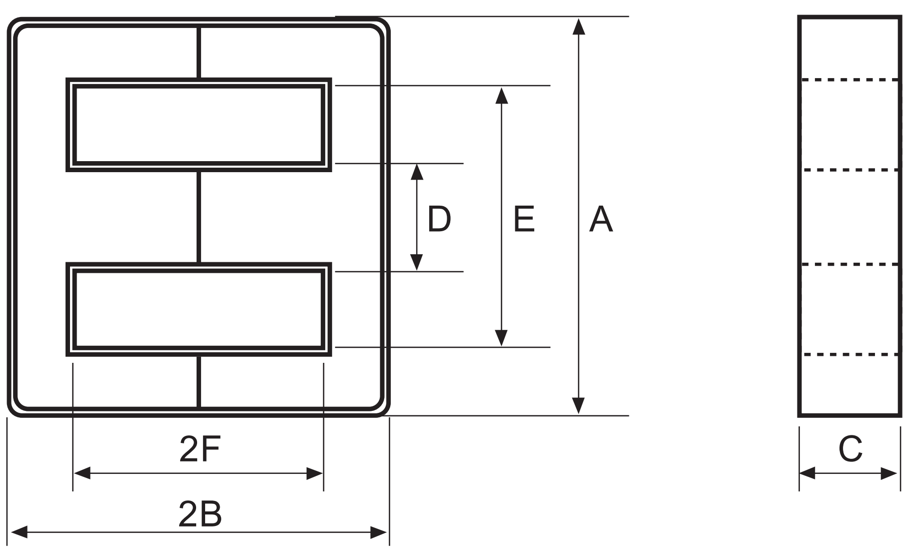


Figure 3.3: EE Core Diagram [4]

According to the Equation 3.1, the minimum required area product can be calculated by specifying the required output power:

$$AP = \frac{1000}{0.017 * 0.26 * 80} = 39,993.0\ cm^4 \tag{3.2}$$

The core size is selected as EE42/21/15, which has an area product as 49484 cm^4 and satisfies the area product requirement [4].

3.1.3 Loss Limited Flux Swing

The core loss is mainly determined by the frequency and the flux swing. The operation frequency is 80 kHz. The core loss per cm^3 is required to find the maximum flux swing. The core loss per cm^3 is calculated as:

$$\frac{Pclim}{Ve} = \frac{2\ W}{17.3\ cm^3} = 115.6\ mw/cm^3 \tag{3.3}$$

At the operating frequency, the peak flux density is found in the core loss curve. Doubling the peak to obtain the peak flux density swing $\triangle B$(At 115.6 mw/cm^3 and 80 kHz):

$$\triangle B = 2 * 130\ mT = 0.26\ Tesla \tag{3.4}$$

3.1.4 Primary and Secondary Turns Calculation

Using Faraday's Law, the number of primary turns $N1$ is calculated as:

$$N1 = \int Edt/\triangle\,\phi = Vin * Ts \tag{3.5}$$

$$N1 = \frac{n_a V_o'}{fs\ \triangle B\ Ae} = \frac{0.025 * 2000}{80k * 0.26 * 178 * 10^{-6}} = 6.75 \tag{3.6}$$

Rounding $N1$ to an integer, thus $N1 = 7$. Recalculate the flux swing and core loss at 7 turns:

$$\triangle\ B(7turns) = 0.26T * \frac{6.75}{7} = 0.25\ Tesla \tag{3.7}$$

From the core loss curve, the core loss at the amplitude of 0.25T/2 is $110mW/cm^3 * Ve$:

$$Core\ Loss(real) = 110 * 17.3\ mW = 1.9\ Watts \tag{3.8}$$

The numbers of secondary turns $N2$ and $N3$:

$$N2 = \frac{N1}{n_a} = \frac{7}{0.025} = 280 \tag{3.9}$$

$$N3 = 1 \tag{3.10}$$

3.1.5 Define the Winding Structure

The skin depth, D_{pen}, is the distance from the conductor surface to where the current density is 37% of the surface current density. The nominal depth of penetration for a conductor can be calculated using page 58 of [28]:

$$Dpen = \sqrt{\frac{\rho}{\pi\mu_0\mu_r f}} = \frac{7.6}{\sqrt{80k}} = 0.269mm \tag{3.11}$$

Where:

$$\rho\ is\ the\ resistivity\ at\ 100°C\ in\ \Omega - m$$

$$\rho = 2.3 * 10^{-8}\ \Omega - m for copper$$

$$f\ is\ the\ frequency\ in\ Hz$$

$$\mu\ is\ the\ absolute\ magnetic\ permeability\ of\ the\ conductor$$

$$The\ absolute\ magnetic\ permeability\ \mu = \mu_0 * \mu_r$$

$$\mu_0 = 4\pi x 10^{-7} H/m$$

According to US wire gauge table, a radius of $0.21mm$ is selected as $Dpen$, In order to reduce the AC resistance, the wire radius must be less than the calculated skin depth D_{pen}. According to US wire size table, a value of 0.21 mm is selected as the wire radius. The cross-sectional area A_w of the conductor is:

$$A_w = \pi * Dpen^2 = \pi * 0.21^2 = 0.138\ mm^2 \tag{3.12}$$

The cross-sectional area of AWG 26 wire is 0.138 mm^2 which satisfies the penetration requirement. Therefore AWG 26 wire is selected as the winding wire on both sides of the transformer. The recommendation of the maximum RMS current operated in copper wire I_{dc} is $450A/cm^2$

limited by heat dissipation. The RMS current flows in the primary side I_p and in the secondary side I_s are:

$$Ip = 1000W * 110\%/54V = 20.4A \tag{3.13}$$

$$Is = 1000W * 110\%/2000V = 0.55A \tag{3.14}$$

For the primary side and secondary side, the required total cross-sectional areas A_{p_Total} and A_{s_Total} are calculated as:

$$A_{p\_Total} = \frac{I_p}{I_{dc}} = 4.8\ mm^2 \tag{3.15}$$

$$A_{s\_Total} = \frac{I_s}{I_{dc}} = 0.129\ mm^2 \tag{3.16}$$

To avoid the high AC resistance while handling large currents, many wires will be twisted in parallel for each turn. The required parallel numbers in each turn of $N1$,$N2$,$N3$ are calculated by dividing the total cross-sectional area by the cross-sectional area of AWG 26 wire. Therefore the $N1$, $N2$ and $N3$ windings will have 40,1 and 6 individually wires, respectively within each winding. The resulting winding structure is shown in Figure 3.4:

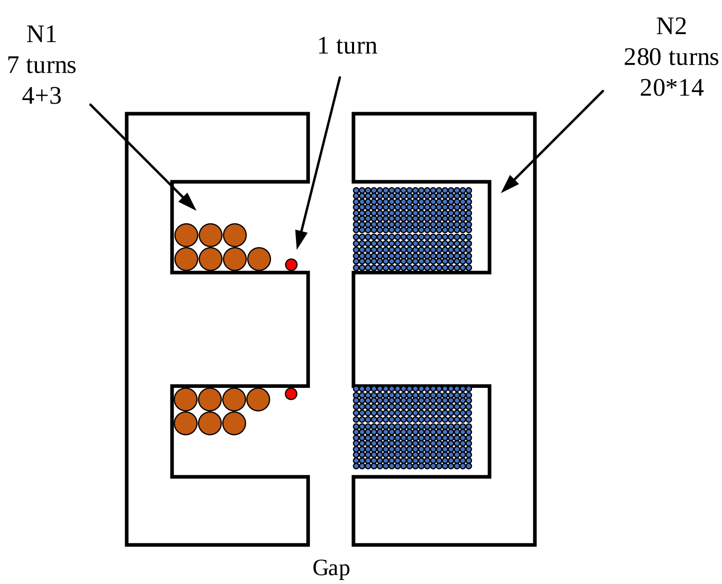


Figure 3.4: The Transformer Winding Structure.

3.1.6 The Real Designed Transformer

The transformer is custom made in *Xingchuangli,Ltd* in GuangDong, China. The pictures are followed as in Figure 3.5:

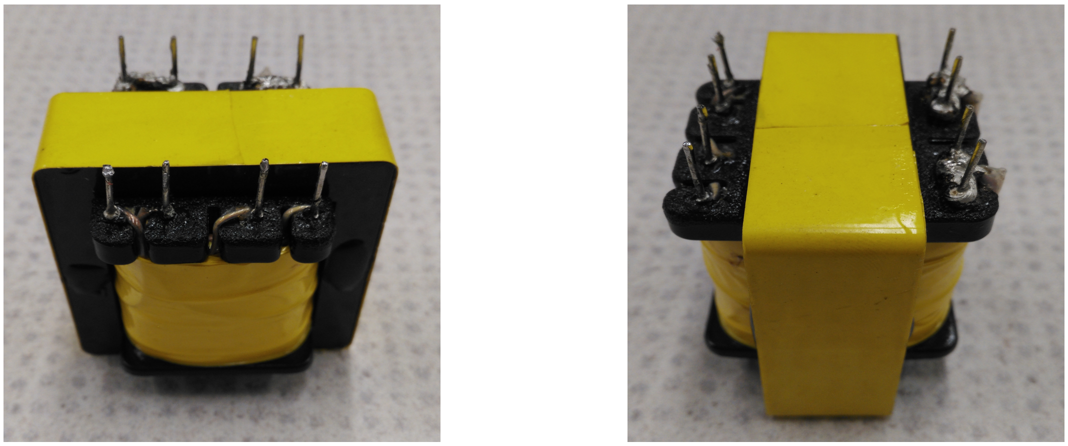


Figure 3.5: The Real Transformer.

The leakage inductance Lr and the magnetizing inductance L_m of the transformer is tested on a bench LCR meter. By applying signals with different frequencies, the following table is obtained:

Table 3.1: Lr and Lm Test Results

Freq(kHz)	0.1	1	10	100	200
Lr (μH)	28.6	3.2	2.7	2.6	2.7
Lm (μH)	9,400	5,700	99.5	14.7	-24.3

As seen from Table 3.1, the L_r and L_m at 100 kHz are 2.6μH and 14.7μH,respectively. The ratio $Ln = Lm/Lr = 5.65$

3.2 EMI Filter, Input Rectifier and Output Rectifier Design

In this section, the input and output configurations will be discussed in detail.

3.2.1 EMI Filter

The function of the EMI (Electromagnetic Interference) filter that will be installed at the AC input is to reduce high frequency noise that may cause interference with other devices. There are two main sources of noise that need to be eliminated. These are common mode noise and differential mode noise. An EMI filter normally consists of capacitors and inductors, therefore the EMI filter is bi-directional and passive. The EMI filter is shown in Figure 3.6. The EMI filter includes a protection fuse, common mode choke, and filtering capacitor.

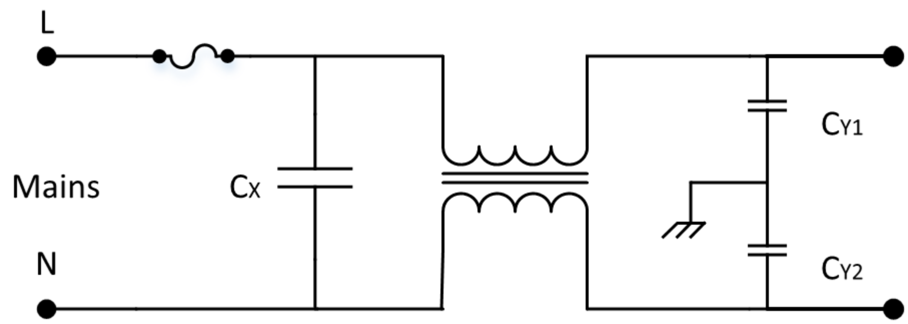


Figure 3.6: EMI Filter

Since the circuit must accommodate a 10 ampere line current, a 20 ampere fuse is selected to provide short circuit protection. Two inductors with the same number of turns and the opposite direction are wound on the same ferrite core. These two inductors and the core form a common mode choke. The common mode choke can reduce the common mode noise. Because the common mode signal has the same direction, this builds two identical magnetic fields in the ferrite core that will be added together to form a large magnetic field. The magnetic field increases the impedance in the path of common mode noise. For the normal line current flow through the common mode choke, there is no effect because two magnetic fields with the opposite direction cancel each other.

The capacitors including C_x, C_{Y1} and C_{Y2} can provide a low impedance path to divert the high frequency input noise, either into the ground, or into the power source. The capacitor C_x installed between two input lines can absorb the noise between two lines which is known as differential mode noise. C_{Y1} and C_{Y2}, which are both connected to the ground, can be used to eliminate the noise between line and the ground.

3.2.2 Input Rectifier

The power source of the resonant converter is the general-purpose alternating-current (AC) power supply, which is 120 volts AC in United States. The 120 volts will be rectified by a four-diode bridge, and followed by an L-C filter in order to smooth the sinusoidal waves especially at the case of a light load. As shown in the Figure 3.7, the inductor L and the capacitor C form a low pass filter which sets a cut-off frequency point, and only allows low frequencies to pass. The values of the inductor and the capacitor are selected as 2 mH and $5uF$. The cut-off frequency $f_c$can be calculated as:

$$f_c = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2 * \pi * \sqrt{2mH * 5\mu F}} = 1591.5Hz \tag{3.17}$$

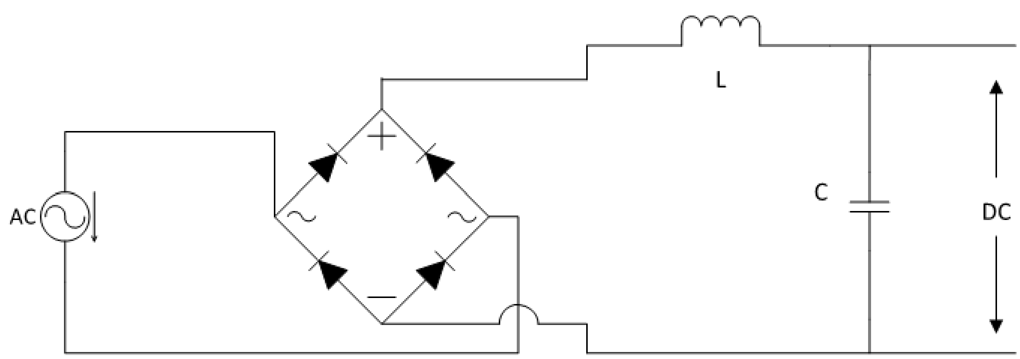


Figure 3.7: Input Filter

3.2.3 Output Rectifier

The circuit is designed to provide an output voltage as high as 4000 Volts. The high voltage is a big challenge for designing the transformer with the concern of electricity isolation. A voltage doubler is adopted as the output rectifier which is shown in Figure 3.8, in order to reduce the output voltage of the secondary side of the transformer. A high voltage, fast recovery diode is required as the rectifier diode. In this design, the low loss diode UX-F5B with a peak reverse voltage of 8 kV is chosen. The value of the output filter capacitor can be estimated assuming a 10% voltage drop is allowed. The average output voltage is 4000 V, and the current is equal to P/V_{out}=0.25 A. The equation of the capacitor charging balance is:

$$\triangle V * C = I * t \tag{3.18}$$

$\triangle V = 4000/2 * 10\% = 200V$. t is the half switching cycle($f_o = 80kHz$),$t = 6.25\mu s$. Then the capacitance is calculated as:

$$C = \frac{6.25\mu s * 0.25A}{200V} = 7.8nF \tag{3.19}$$

A 10nF film capacitor with a 3000 volt rating is selected as the output filter capacitor.

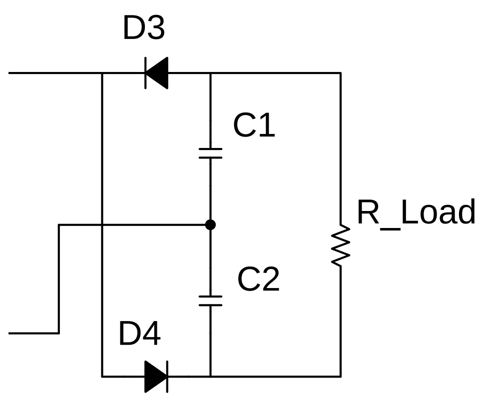


Figure 3.8: Output Rectifier

3.3 Main Circuit Design

The main circuit design includes the design of MOSFET bridge, resonant network and their component selection.

3.3.1 MOSFET Bridge Selection, Loss Calculation, Heat Sink Selection

a).MOSFET Bridge selection:

The most important parameters for MOSFET selection include Drain-Source Breakdown Voltage (V_{DS}), Continuous Drain Current (I_D), Drain-Source On-State Resistance (R_{DS}(on)), Total Gate Charge (Q_g) and Rise time (t_r). The MOSFET bridge and LLC network is shown in Figure 3.9.

The maximum voltage applied across Q_1 is V_{rec} when Q_2 is on. V_{rec} is the RMS value of the rectified grid voltage which is around 108 V. The current, $I_{DS(on)}$, flowing through the MOSFET (Q_1 or Q_2) is equal to the circulating current, I_r, in the resonant network. I_r is derived as the Equation 2.21. Referring back to the equivalent main circuit in Figure 2.11, based upon the calculation of L_m, L_r in Equations 2.35 and 2.34. I_m and I_{oe} can be calculated using Equations 3.21 and 3.22:

$$I_m = \frac{2\sqrt{2} * n * V_o}{\pi * \omega * L_m} = \frac{2\sqrt{2} * 0.025 * 2000V}{\pi * 2\pi * 80kHz * 12.27\mu F} = 7.3A \tag{3.20}$$

$$I_{oe} = \frac{\pi * I_o}{(2\sqrt{2} * n)} = \frac{\pi * 0.25A}{(2\sqrt{2} * 0.025)} = 22.2A \tag{3.21}$$

Thus,

$$I_r = I_{DS(on)} = \sqrt{I_m^2 + I_{oe}^2} = \sqrt{7.3A^2 + 22.2A^2} = 23.4A \tag{3.22}$$

The peak value of I_r is:

$$I_{r\_peak} = I_r * \sqrt{2} = 33.0A \tag{3.23}$$

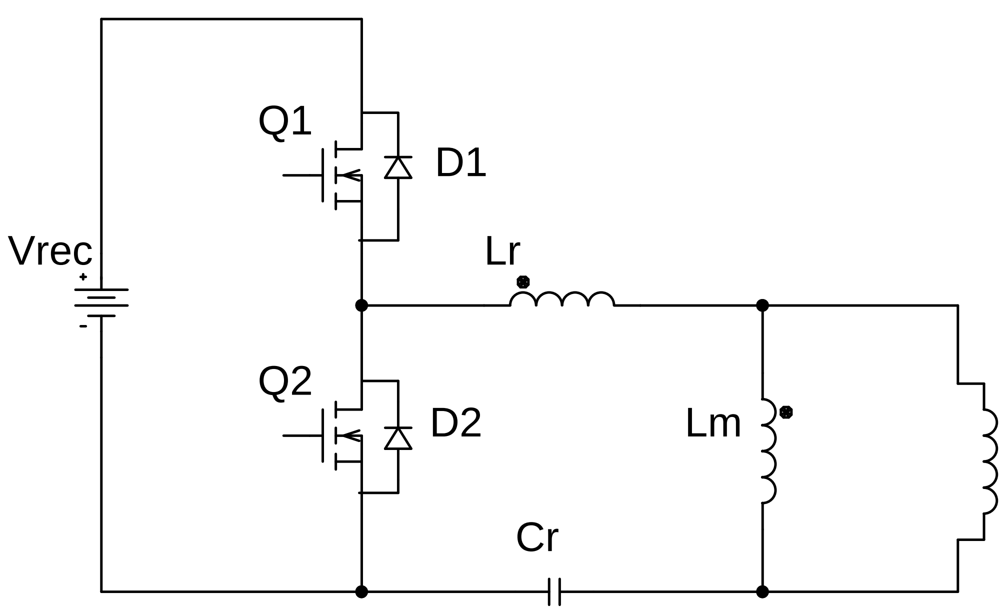


Figure 3.9: MOSFET Bridge and LLC network

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$(Drain-Source voltage)	650	V
$R_{DS(on)}$@ $T_{j,125^oC}$ (Drain-Source on-state resistance)	85	mΩ
Qg(Gate charge total)	170	nC
V_{DF}(Diode forward voltage)	0.9	V
I_D (Continuous drain current)@150	49.0	A
I_{DSS}(Zero gate voltage drain current)	10	µA
Eoss@100V (Coss stored energy)	7.2	µJ
Ptot (Maximum power dissipation)	481	W
tr(Switching rise time)	27	ns
tf(Switching fall time)	5	ns
td(off)(Turn-off delay time)	90	ns

Table 3.2: Key Performance Parameters of the IPW60R041P6

The model IPW60R041P6 MOSFET which is from Infineon $CoolMOS^{TM}P6$ series is selected. Table 3.2 lists some key performance parameters of this MOSFET model. b).MOSFET loss calculation:

The calculation of power loss in the MOSFET is critical for choosing or designing a heat sink, and also for evaluating the power efficiency of the power supply. There are many factors contributing to the power loss in the MOSFET. The power loss can be categorized into three types of loss, quiescent loss, switching loss, diode loss.

Quiescent loss includes the conduction loss (Pon) during the on-state and the cut-off loss ($Poff$) during the off-state. Pon is dissipated by the resistive element $R_{DS(on)}$. The conduction loss Pon at 125°C junction temperature is calculated as:

$$P_{on} = I^2_{DS(on)} * R_{DS(on)}/2 = 23.4^2 * (0.085\Omega)/2 = 23.27\ Watts \tag{3.24}$$

The reason for dividing by 2 in the formula for P_{on} is that the two MOSFETs conduct alternatively with a 50% duty cycle. The cut-off loss P_{off} is caused by the leakage current when the MOSFET is off.

$$P_{off} = V_{DS(off)} * I_{DSS}/2 = 108 * 10 * 10^{-6}/2 = 0.00\ Watts \tag{3.25}$$

$V_{DS(off)}$ is the voltage applied to the MOSFET when it is off. $V_{DS(off)}$ is equals to V_{rec} shown in Figure 3.9. $Poff$ is negligible comparing to Pon.

The contributions to switching loss include the energy lost during turn-on transition $Poff\_on$, the energy lost during turn-off transition Pon_off, and the energy P_{DS} used to charge drain-source capacitance (also referred to as output capacitance, Coss). As discussed in Chapter 2.3.2, the body diode is forward biased when the switch is turning on. Therefore there is no crossover loss due to the fact that the voltage drop between source and drain is 0V during the turn-on transition. Thus,

$$Poff\_on = 0 \tag{3.26}$$

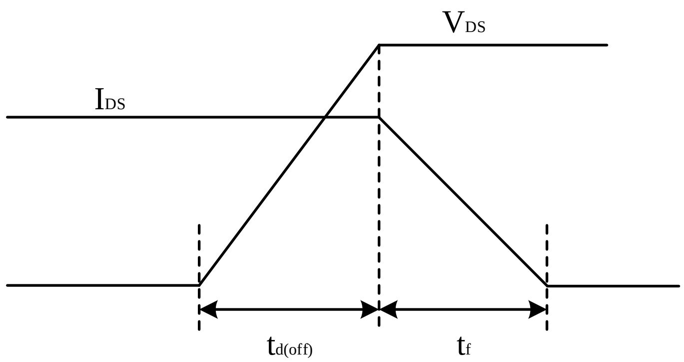


Figure 3.10: Turn-off Transition Waveform

Turn-off transition P_{on_off} is still existing. The turn-off transition waveform in the worst case is shown as Figure 3.10 The lost energy is the total crossover product area which can be calculated as:

$$Pon\_off = 1/2 * V_{DS} * I_{DS(on)} * [td(off) + tf] * fs \tag{3.27}$$

$$= 1/2 * 108V * 23.4A * (90+5)ns * 80kHz = 9.60\ Watts \tag{3.28}$$

The energy for one charging of Coss under a specific V_{DS} (400V) value is given in IPW60R041P6 datasheet as Eoss, and is shown in Table 3.2. P_{DS} is calculated as:

$$P_{DS} = Eoss * fs = 7.2 * 10^{-6} j * 80kHz/s = 0.58\ Watts \tag{3.29}$$

Diode loss includes the forward conduction loss Pd_f and the reverse recovery loss Pd_re. Pd_f is calculated as:

$$Pd\_f = 1/2 * I_F * V_{DF} * t_x * fs = 1/2 * 23.4 * 0.9 * 0.01 = 0.11\ Watts \tag{3.30}$$

As discussed in Chapter 2.3.2, the diode conducts only during the transition between two MOSFETS. IF is the resonant current flowing through the diode during the transition time. The transition time (deadband time) is less than 1% of the switching cycle. In the transition period, the resonant current is approximately set as $\frac{1}{2}I_r$. The conduction time tx in one duty cycle multiplied with the frequency f_s is the total conduction time in one switching cycle. Pd_re is zero. As discussed in Chapter 3.2, the body diode D_2 of MOSFET Q_2 starts to conduct after Q_1 is off at t1, then Q_2 turns on at t2, the current flowing through D_2 diverts into Q_2 because of the low on-resistance in Q_2. Since Q_2 already conducted before D_2 is reversed, the reversed voltage applied on D_2 is zero. Therefore there is no reverse recovery loss on D_2. The analysis is the same on the body diode D_1.

The summation of losses analyzed above will give the total dissipation, P_D, in the MOSFET:

$$\begin{aligned} P_D &= Pon + Poff + Poff\_on + Pon_off + P_{DS} + Pd\_f + Pd\_re \\ &= 23.27 + 0.00 + 0 + 9.60 + 0.58 + 0.11 + 0.00 = 33.56\ Watts \end{aligned} \tag{3.31}$$

c).MOSFET Heating Sink Selection:

The typical equation used for calculation of the MOSFET dissipation is shown as below:

$$\theta_{JA} = (T_J - T_A)/P_D \tag{3.32}$$

Where:

θ_{JA}=thermal resistance

T_J = junction temperature

T_A = ambient temperature

P_D = power dissipation

θ_{JA} consists of three separate thermal resistances in series. One is the thermal resistance inside the device, between the junction and the its case, called θ_{JC}. Another is the resistance of the silicon grease used between the MOSFET case and the heat sink, called θ_{CS}. The last one is the thermal resistance of the heat sink, called θ_{SA} [29]. The total thermal resistance is:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \tag{3.33}$$

Rearranging two Equations 3.32 and 3.33:

$$\theta_{SA} = (T_J - T_A)/P_D - \theta_{JC} - \theta_{CS} \tag{3.34}$$

Based on the datasheet specifications of the device and the actual operation conditions, the maximum junction temperature $T_J = 150^oC$. The ambient temperature T_A is set as 50^oC. P_D has been already calculated as 33.56 Watts. From the datasheet, the thermal resistance of silicon grease θ_{CS} is 0.1^oC/Watt, and the junction-case thermal resistance is 0.26 ^oC/Watt. Thus the thermal resistance θ_{SA} should be at most:

$$\theta_{SA} = (150^oC - 50^oC)/33.56W - 0.1^oC/W - 0.26^oC/W = 2.62^oC/W \tag{3.35}$$

The heat sink is selected as 52980X model provided by Aavid Thermalloy. The dissipation features are shown in Figure 3.11 [30]. Based on the Figure 3.11, to acquire a low enough thermal resistance, a cooling fan will be added in the practical design. Because a high air velocity results in a lower thermal resistance.

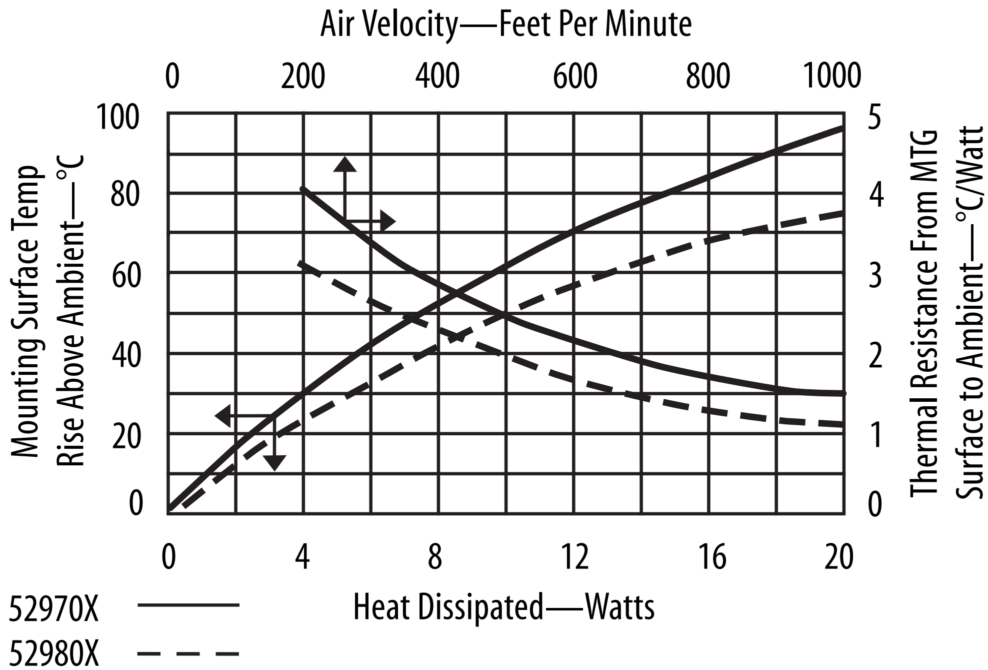


Figure 3.11: Heating Sink Dissipation Features

3.4 Resonant Network

The resonant network contains three components as shown in Figure 3.12. The leakage inductor L_r and the magnetizing inductor L_m are both discussed in Chapter 2.4. L_r and L_m are integrated into the transformer when it's designed. As shown in the Table 3.1, the values of L_r and L_m produced favorable test results.

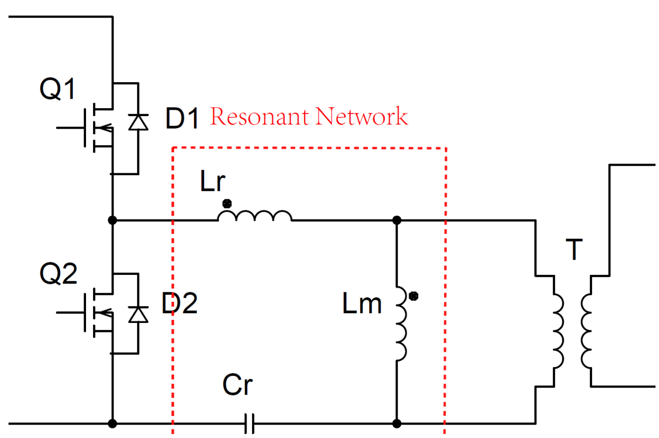


Figure 3.12: Resonant Network

The selection of the resonant capacitor ($2.2\mu F$) consists of determining the voltage applied across the capacitor and the capacitance value. A power film capacitor is selected, since it has a high power rating. The voltage on the resonant capacitor is obtained from the PSpice simulation, which is shown in Figure 3.13. The voltage is a DC voltage with sinusoidal fluctuations. The RMS value of the voltage is around 55 V. B32523 Model from EPCOS is designed for automotive industry use. B32523 Model has a permissible 250 V DC voltage which satisfies the requirement.

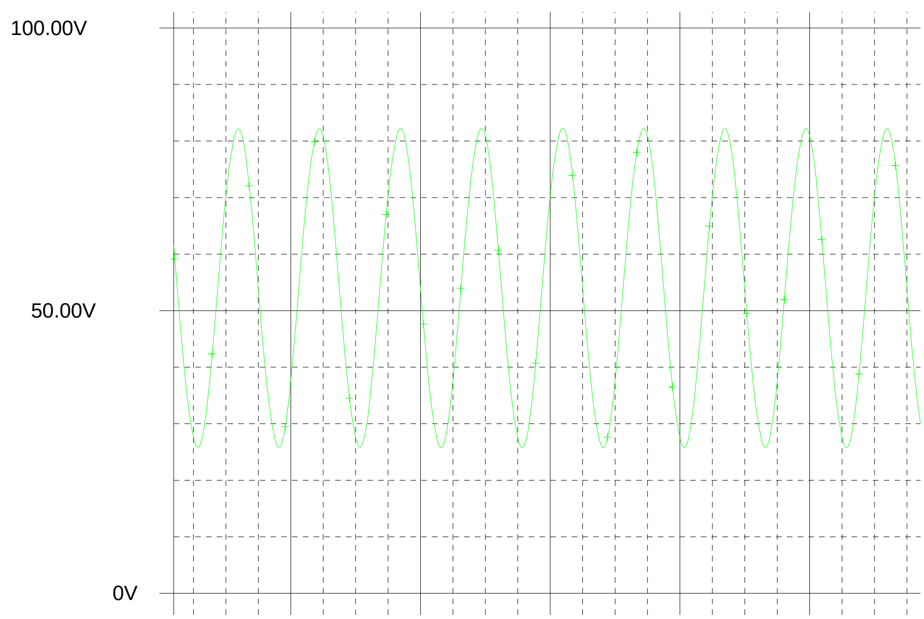


Figure 3.13: Voltage on the Resonant Capacitor Cr

3.5 Driver Circuit Design

The driver circuit for the MOSFET is critical for the success of the circuit design. In this section, the driver IC selection and the detailed turning on and off process will be discussed.

3.5.1 Driver IC Selection

The goal of the driver circuit design is to turn on and turn off the MOSFET fast and accurately. The equivalent circuit of the MOSFET is shown in Figure 3.14. The MOSFET contains a body diode and three parasitic capacitors, Cgs, Cgd and Cds.

Where:

Cgs = capacitance between gate and source

Cgd = capacitance between drain and gate

Cds = capacitance between drain and source

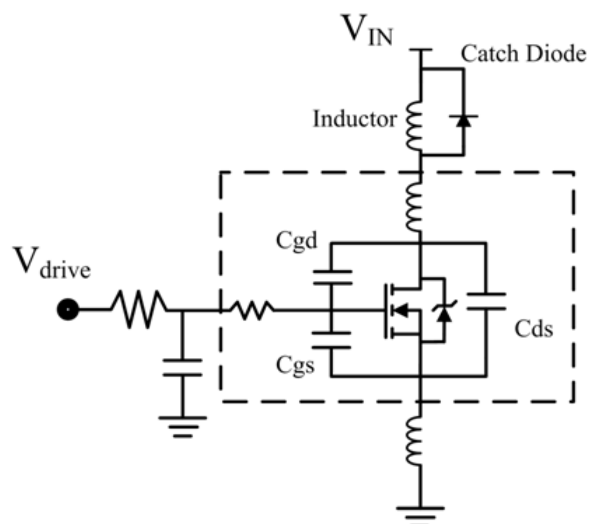


Figure 3.14: Parasite Capacitance in the MOSFET

During the turn on process, the capacitance Cgs first begins to charge until arriving at the plateau of the curve shown in Figure 3.15. The MOSFET starts to turns on at the gate plateau voltage which is around 6.1 V. Technically the rise time tr of the turn-on process is the period from the starting point to the plateau voltage (Miller Plateau). However, to turn on the MOSFET completely, the gate current has to fill the total charge Qg shown in Table 3.1.

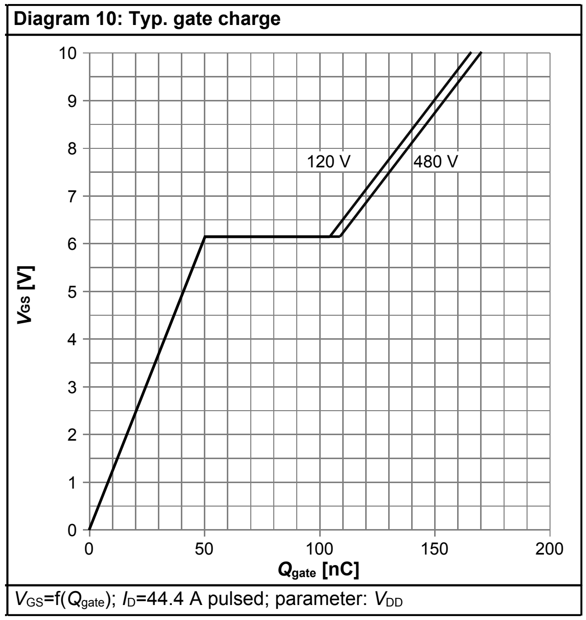


Figure 3.15: Typical Gate Charge Diagram [5]

The rise time tr of the turn on transition is 27 ns. From the datasheet, tr is tested under a very large gate charging current which is around 7.6 A. During the rise time, the total gate charge equals to 27*7.6 = 205 nC. The total charge given in Table 3.1 is 170 nC. It is hard to get a driver IC with a 7.6 A charging current. Finally the model 2EDL23N06PJ from Infineon is selected, which has a maximum charging current of 2.3 A,is selected as the driver IC. The charging time tr (rise time) can be approximately calculated as:

$$tr = Qg/2.3A = 170nc/2.3A = 74ns \tag{3.36}$$

3.5.2 Charging and Discharging Path

The charging and discharging paths for both MOSFETs are the same, and are highlighted in the red box as shown in Figure 3.16 below. The internal gate resistance of the MOSFET is 1 Ω. The resistance RLIN1 for the charging path is calculated as:

$$RLIN1 = Vg/2.3A - 1\Omega = 5.5\Omega. \tag{3.37}$$

Where Vg is the voltage supply for the driver IC which is equal to 15 V, and Vg is applied directly on the gate charging path. RLIN1 is selected as a 6 Ω resistor.

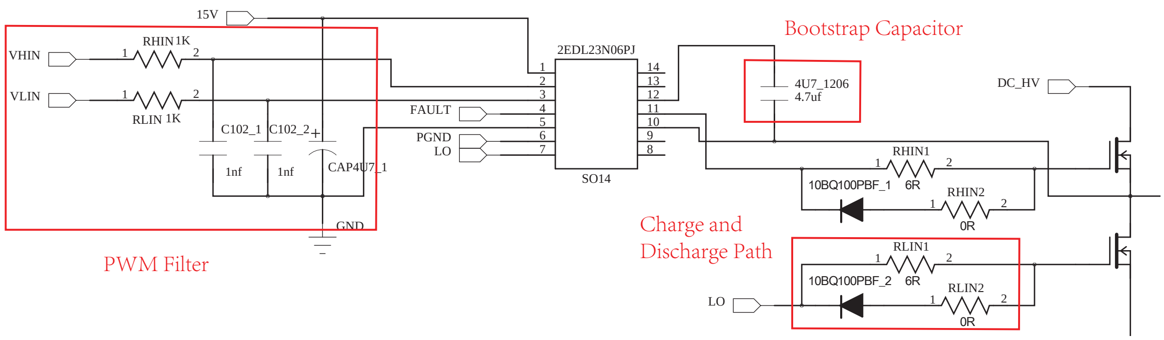


Figure 3.16: MOSFET Driver Circuit

As for the discharging path, the resistance along the path should be as small as possible to reduce the turn-off loss. Therefore a zero resistance will be ideal. Because of the 1 Ω internal gate resistance, the total discharging resistance is 1 Ω. Vgs is fully charged to be Vg here. The peak discharging current will be Vgs/1 Ω =15 A. A 15 A repetitive surge current is a huge challenge for the discharging diode. A high performance Schottky rectifier diode 10BQ100PBF from VISHAY is selected. 10BQ100PBF is compatible with the high frequency operation. It can take a continuous current of 1A, and a 38 A surge current.

3.5.3 Bootstrap Capacitor Calculation

The driver for the low side MOSFET (Q_2) is fairly straightforward, only a 15 V voltage applied on the gate charge path is required. However the high side MOSFET (Q_1) needs some special techniques to guarantee a +15 V difference. The bootstrap circuit is utilized in the high side gate driver to provide the +15 V difference. The MOSFET driver with bootstrap circuit is shown in Figure 3.17 [6]. When the low side MOSFET is turned on and the high side MOSFET is turned off, the Vs is pulled down to the ground. The bootstrap capacitor, C_{BOOT}, is charged through the bootstrap resistor, R_{BOOT}, and bootstrap diode, D_{BOOT}. When the low side MOSFET is turned off, the V_{BS} floats and the bootstrap diode is reversely biased.

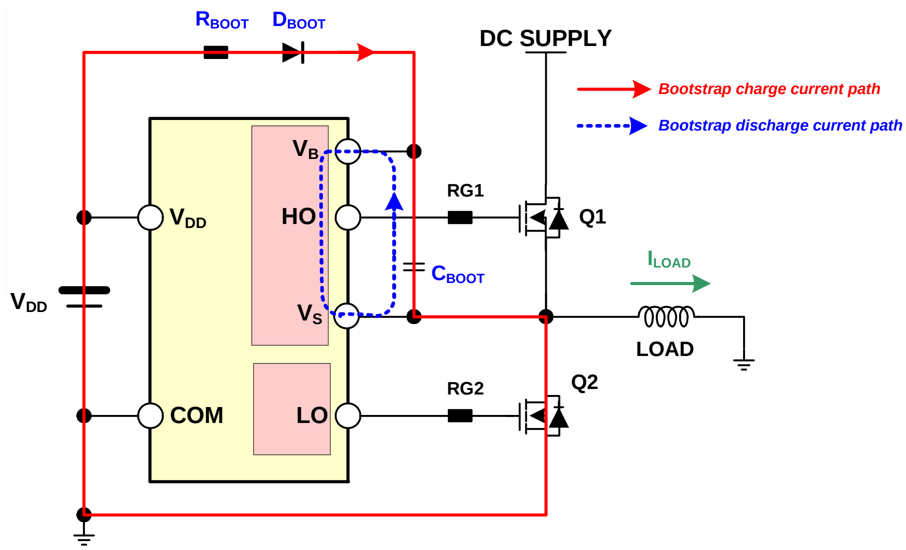


Figure 3.17: Bootstrap Power Supply Circuit [6]

The bootstrap capacitor is charged during each switching cycle. Theoretically the voltage V_{BS} across the bootstrap capacitor, C_{BOOT}, can be charged to:

$$V_{BS} = V_{DD} - VD_{BOOT} - VDS = 15V - 1.2V - 0.2V = 13.6V \tag{3.38}$$

The voltage drop on R_{BOOT} can be ignored because it is very small. The value of the bootstrap capacitance is determined by the maximum allowable voltage drop on V_{BS}. Assuming the permissible maximum bootstrap voltage fluctuation, $\triangle V_{BS}$, is 0.5 V. The maximum tolerance of the bootstrap voltage fluctuation is about 1.5 V. Therefore a 0.5 V design specification provides a 1V margin. The bootstrap capacitance is calculated as [5]:

$$C_{BOOT} = (i_{QBS} * tp + Qgs)/(\triangle V_{BS}) * 1.5 \tag{3.39}$$

where i_{QBS} is the quiescent current of the high side section, tp is the switching period. Comparing with the total charge Qg for the super junction capacitance in this MOSFET model, $i_{QBS} * tp$ can be ignored. Therefore the bootstrap capacitance is:

$$C_{BOOT} = Qgs/\triangle V_{BS} * 1.5 = 170nC/(0.5V) * 1.5 = 127.5nF \tag{3.40}$$

In the practical design, there are two special considerations on the bootstrap capacitor. The current drawn from the bootstrap capacitor is a large pulse current. Therefore the ESR

(Equivalent Series Resistance) of the capacitance has to be very small. Otherwise the losses can result in a lower capacitor lifetime. The layout rule of the bootstrap capacitor is that it must be placed as close as possible to the driver IC. Otherwise, the voltage spikes caused by parasitic resistors and inductors may trigger the undervoltage lockout threshold of the driver IC.

a).Investigation of the Voltage Drop along the Bootstrap Charging Path

As shown in the Equation 3.38, the value of V_{BS} is supposed to be around 13.6 V with a small periodical fluctuation. This voltage drop along the bootstrap charging path was measured in the lab. The V_{BS} shown in Figure 3.18 demonstrates the Equation 3.38 for a switching frequency of 100 kHz. However when the switching frequency is raised to 500 kHz from 100 kHz, the VBS becomes 10.0 V which is shown in Figure 3.19.

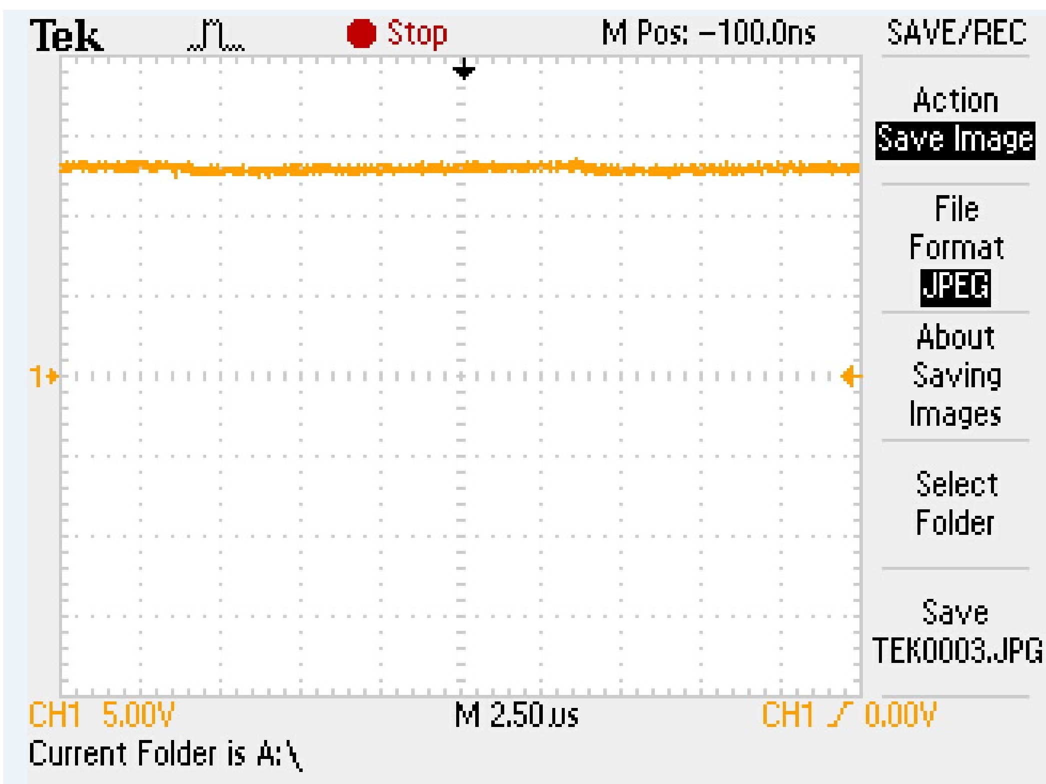


Figure 3.18: V_{BS} under 100 kHz Switching Frequency

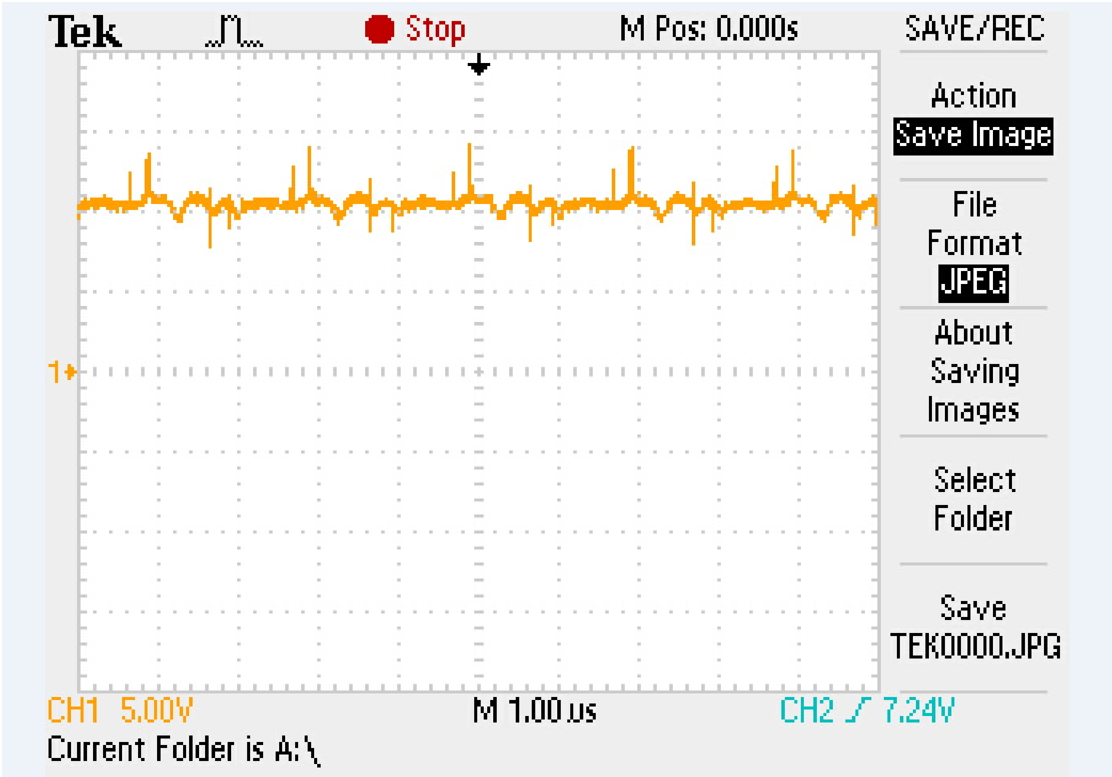


Figure 3.19: V_{BS} under 500 kHz Switching Frequency

There are two possible explanations. One is a small switching period results in a non-saturation on-state of the MOSFET. According to the Equation 3.38, a non-saturation on-state means a higher V_{DS} value, thus the V_{BS} is lower than 13.6 V. However the voltage drop on MOSFET was also measured in the lab, and the resulting V_{DS} was almost zero during the on-state. Thus this explanation is not valid.

The other reason is the high switching frequency causes a big recovery loss on the bootstrap diode, D_{BOOT}. The bootstrap diode, D_{BOOT}, is integrated into the driver IC. The performance of the bootstrap diode under a high frequency is doubtable. Therefore paralleling a high performance diode with the existing diode might be a good solution.

3.5.4 PWM (Pulse Width Modulation) Signal Filtering

The PWM signal block is shown in Figure 3.16, which consists of a resistor and a capacitor (RC filter) for each PWM signal. VHIN and VLIN are two PWM signals from DSP controller. The IO ports of this controller can provide 3.3V PWM signals with a maximum current of 4mA. The RC filter resistances, RHIN and RLIN, can be calculated as:

$$RHIN = RLIN = 3.3V/4mA = 825\Omega \tag{3.41}$$

In the real design, the value of RHIN and RLIN are chosen as 1 kΩ. The RC filter and its magnitude bode plot are shown in Figure 3.20. The $-3dB$ cut off frequency needs to be higher than the frequency of PWM signal. The 500 kHz PWM signal is the highest frequency that will be used during the soft-start period. Therefore the cut off frequency f_c can be set as 600 kHz. Based on the voltage division rule, the expression of a $-3dB$ output magnitude decrease can be written as:

$$-3dB = 20 * log(\frac{1/(2\pi * fc * C)}{(R + 1/(2\pi * fc * C))}) \tag{3.42}$$

$$C = 0.11nF \tag{3.43}$$

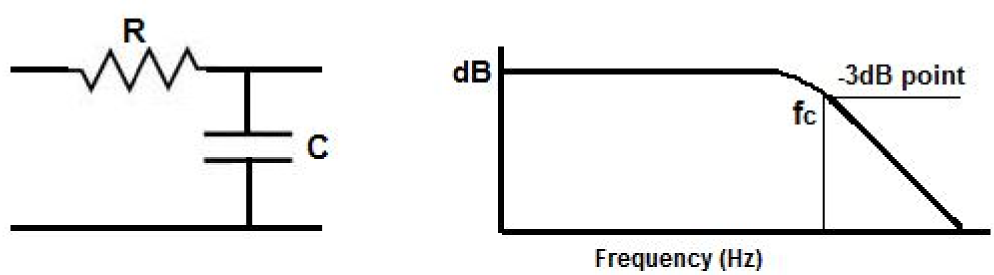


Figure 3.20: RC Low Pass Filter

3.6 Protection and Feedback

There are four parts of design in this section, MOSFET current sensing, input current sensing, input voltage sensing and fault management. The first two parts are design to protect the short circuit and restart. The other two are design to acquire the parameters used in the feedback control.

3.6.1 Detect the Short Circuit Condition

There is a mechanism in the driver IC model 2EDL23N06PJ to prevent overcurrent (short circuit). The voltage drop between the pins, PGND and GND, can be sent to a comparator with a threshold of 0.46 V. If the voltage drop is larger than 0.46 V, then the comparator will be triggered and the protection is activated to stop all the PWMs signals for a $230\mu s$ period. During the protection period, a $230\mu s$ fault signal will be shown on the pin of /FLT.

The voltage drop between PGND and GND needs to be created when the short circuit is happened. As shown in Figure 3.9, the circulating resonant current flows through MOSFET during the whole switching cycle. Therefore the overcurrent sensor can be connected in series with the source terminal of the MOSFET. The overcurrent sensor is shown in the red box in Figure 3.16.

As calculated in the Equation 3.23, the peak circulating current is 33.0 A. The definition of the overcurrent value under the short circuit condition is critical. It can't be too large, thus some large currents caused by short circuit might be omitted. It also can't be too small, that the protection can be triggered by the start currents or the noises. Therefore a three times of the peak circulating current is selected as the overcurrent limitation. The resistance of the current sensor can be calculated as:

$$0.46V/(3*33.0A) = 4.6m\Omega \tag{3.44}$$

This resistor has to be a special made resistor for power electronics current sensing. The LRMA series resistors from TT Electronics is selected. The LRMA series resistors have precise resistance, a high power rating, and a low thermal EMF (Electromotive Force).

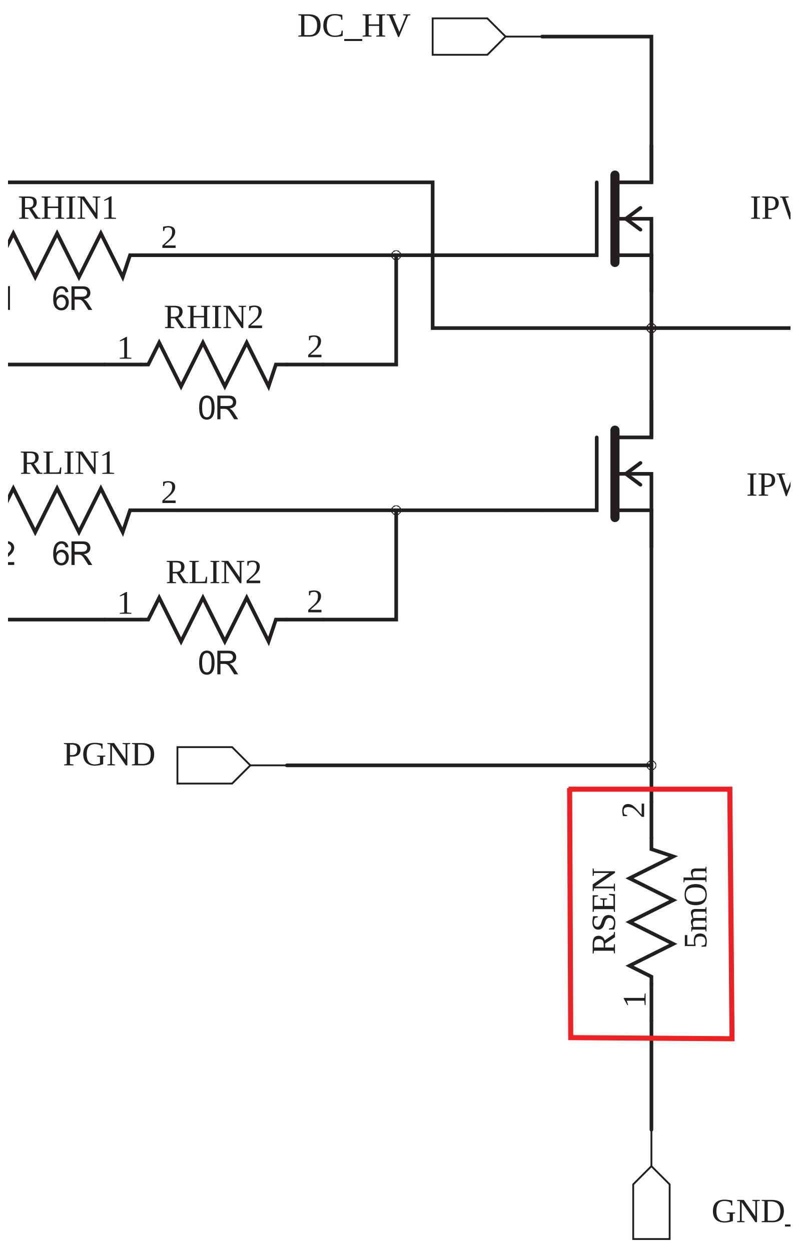


Figure 3.21: Over Current Sensor

3.6.2 Fault Indication and Restart

The /FLT pin will activate under the occurring of the under-voltage protection or the overcurrent protection. The fault indication signal from /FLT lasts only 230μs. The driver IC will restart to work after the 230μs activation. If the problems in the circuit are not properly solved, the driver IC will keep going into the fault condition and restart. Finally the repetitive overcurrent or under-voltage conditions probably will damage the MOSFETs or driver IC itself.

The fault signal has to be detected and sent to the DSP controller. Then the DSP controller can prohibit all the PWM signals until the circuit problems are found and solved. A flip-flop circuit is shown as below. When the /FLT pin is activated, the zero fault voltage will be locked and a red LED will be lighted. At the same time, the DSP captures the falling edge of the fault signal and stops all PWM outputs. A reset signal will be sent to the flip-flop to circuit to clear the fault condition.

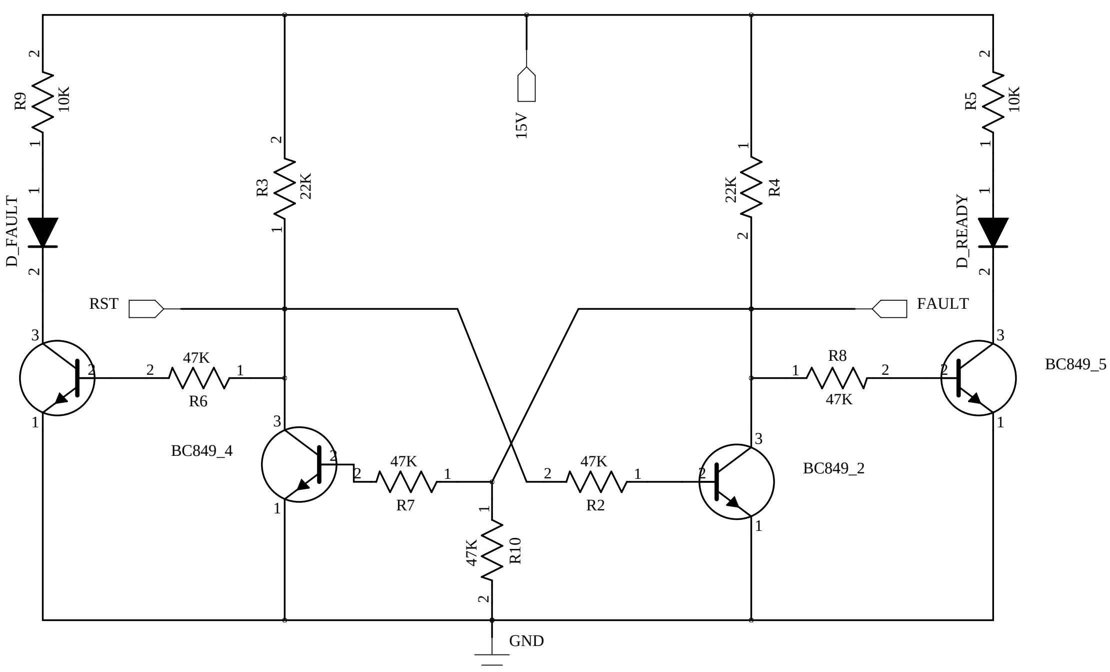


Figure 3.22: Flip-Flop Circuit for Fault Indication and Restart

3.6.3 Input Current and Zero-crossing Point of Input Voltage

As analyzed in the Chapter 2.3.1, the output voltage of the resonant power supply can be adjusted by changing the switching frequency. The LC filter after the rectified bridge is far away from filtering the sinusoidal voltage into a DC voltage. Therefore the DC rectified voltage is actually an approximate positive semi-sine.

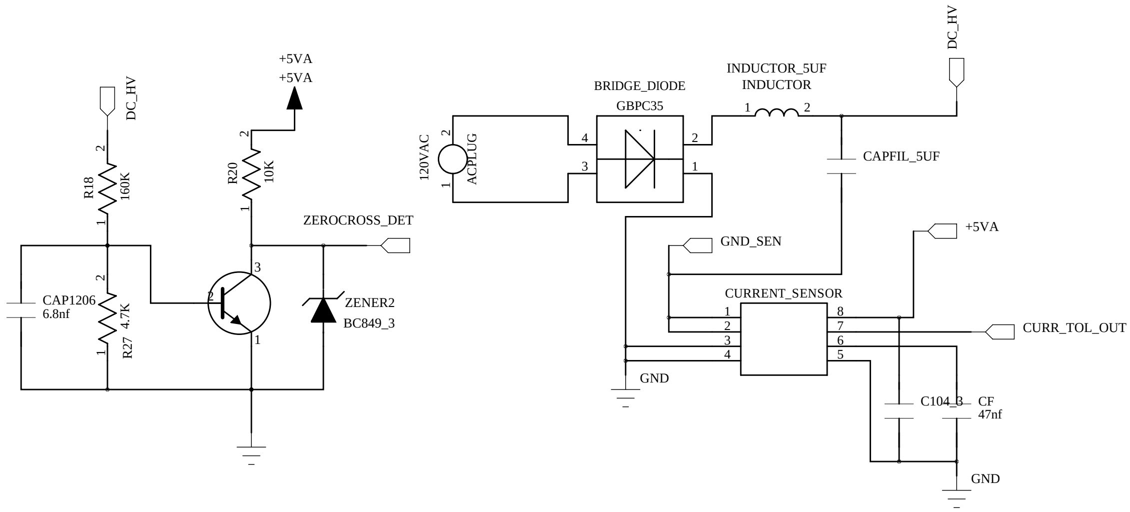


Figure 3.23: Input Voltage Zero Cross Detection and Input Current Sensor

To acquire a more flat output voltage applied on the magnetron, the voltage gain of the resonant converter needs to be adjusted along with the positive semi-sine input voltage. The synchronous control point for every cycle of the positive semi-sine wave can be selected as the zero-crossing point of the positive semi-sine wave. The zero-crossing detection circuit is shown in Figure 3.23. A voltage divider is used to obtain the rectified voltage. When the voltage is approaching the bottom of the positive semi-sine wave, the output of the amplifier will be flipped. A small capacitor is installed for filtering the possible noises, in case of the false triggering. The passing frequency band of this filtering capacitor needs to include the frequency of the semi-sine wave.

The RMS current also need to be acquired to be used in the calculation of the input power. There are two ways to detect the input current. One is to insert a small precision resistor. The other method is to adopt a hall effect linear current sensor. A small precision resistor is cheap, but it needs a amplifying circuit to enlarge the signal. The input current is large, thus a considerable power will be dissipated in the resistor. Finally the hall effect chip ACS711 model from Allegro is adopted as the current sensor.

3.7 Layout of PCB (Printed Circuit Board)

The considerations of designing the high power PCB and electromagnetic interference (EMI) are discussed in this section.

3.7.1 PCB Copper Calculations

Due to the high current in the resonant tank and the MOSFET bridge, the PCB thickness and the trace width need to be calculated in case of over temperature or even damage. According to the standard IPC-2221 (Generic Standard on the Printed Circuit Board Design) [31], the trace width is calculated as following. First, the Area is calculated:

$$Area(mils^2) = \left(\frac{Current(A)}{k * \left(Temp\_Rise(^oC)\right)^b}\right)^{(1/c)} \tag{3.45}$$

Then, the width is calculated:

$$Width(mils) = \frac{Area(mils^2)}{(Thickness(oz) * 1.378(mils/oz)} \tag{3.46}$$

For IPC-2221 external layers: k = 0.048, b = 0.44, c = 0.725. where k, b, and c are constants obtained from IPC-2221 curves. To reduce the trace width as much as possible, a PCB copper plate with 3 oz thickness is selected. Bringing the 3 oz thickness into the formula above, and set the allowable temperature rise as 10^oC. The width trace is calculated as 305 mils.

3.7.2 EMI Suppression

The PCB layout of the transformer primary side is shown in Figure 3.24. The left area of the primary side is the mixed signal processing part (the low power area), and the right area is the high power side. The switching MOSFET can generate a high electromagnetic noise which might be interfered with the low voltage side. The PWM signal in the low voltage area is very sensitive, any pollutions can results in the wrong conduction on the MOSFETs which might burn the MOSFETs. The low voltage side also has communication with the DSP controller, any noises might hurt the DSP controller as well.

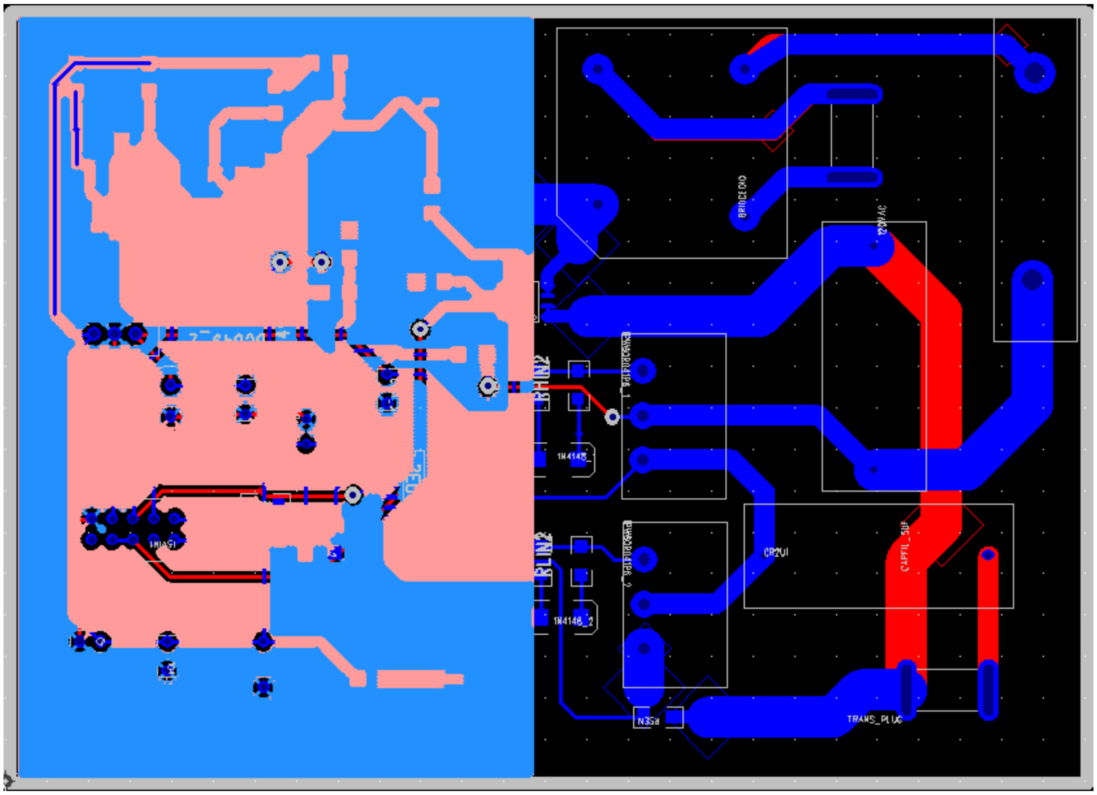


Figure 3.24: PCB Layout

As shown in the Figure 3.24, the low power and the high power side are separated on the PCB. There is only one connection point at the border between these two areas. Also to protect the low power side from the electromagnetic noise, the ground flooding on the both side of the low power area is implemented.

CHAPTER 4: SIMULATION AND EXPERIMENT

4.1 Simulation Results Discussion

The LLC based main circuit in Figure 2.9 is simulated in Pspice environment. A transient analysis based circuit is built in Pspice as shown in Figure 4.1. The DC input voltage of the MOSFET bridge is set as 108 V which is equal to the filtered rectified voltage of the AC main in United States. In the simulation diagram, TR1 is a transformer model with two secondary outputs. The secondary output between pin 3 and pin 4 is for delivering the energy to the rectifier diode. The other output between oins 10 and 11 is for driving the filament of the Microwave Oven.

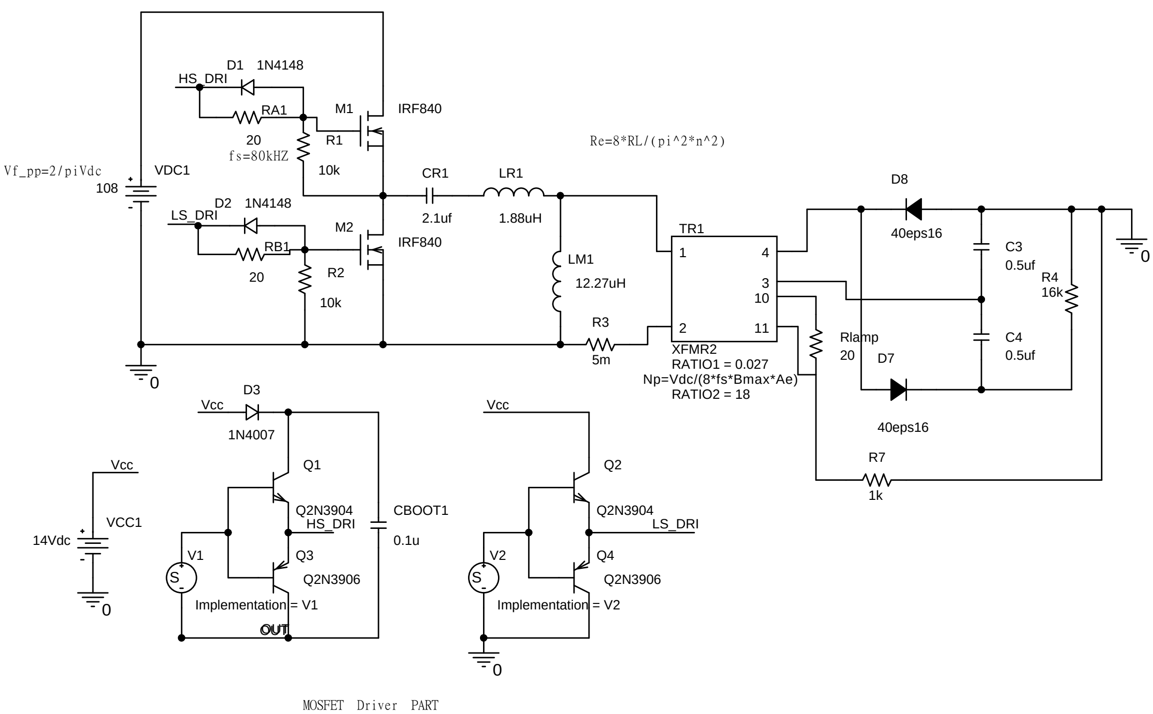


Figure 4.1: Simulation Diagram of the Main Circuit in Pspice

4.1.1 The Simulation of the Operation of the Resonant Network

The operation of the resonant network has been discussed in detail in subsection 2.3.2. As shown in the Figure 2.15. The simulation results of currents I_r, I_m and I_s are all shown in Figure 4.3. The resonant current I_r is a sinusoidal wave, the magnetizing current I_m is a linear increasing or decreasing current and doesn't resonate with L_r and C_r. Because the voltage on L_m is clamped by the secondary output voltage (constant voltage). The current I_s which is delivered to the secondary side is the difference between I_r and I_m.

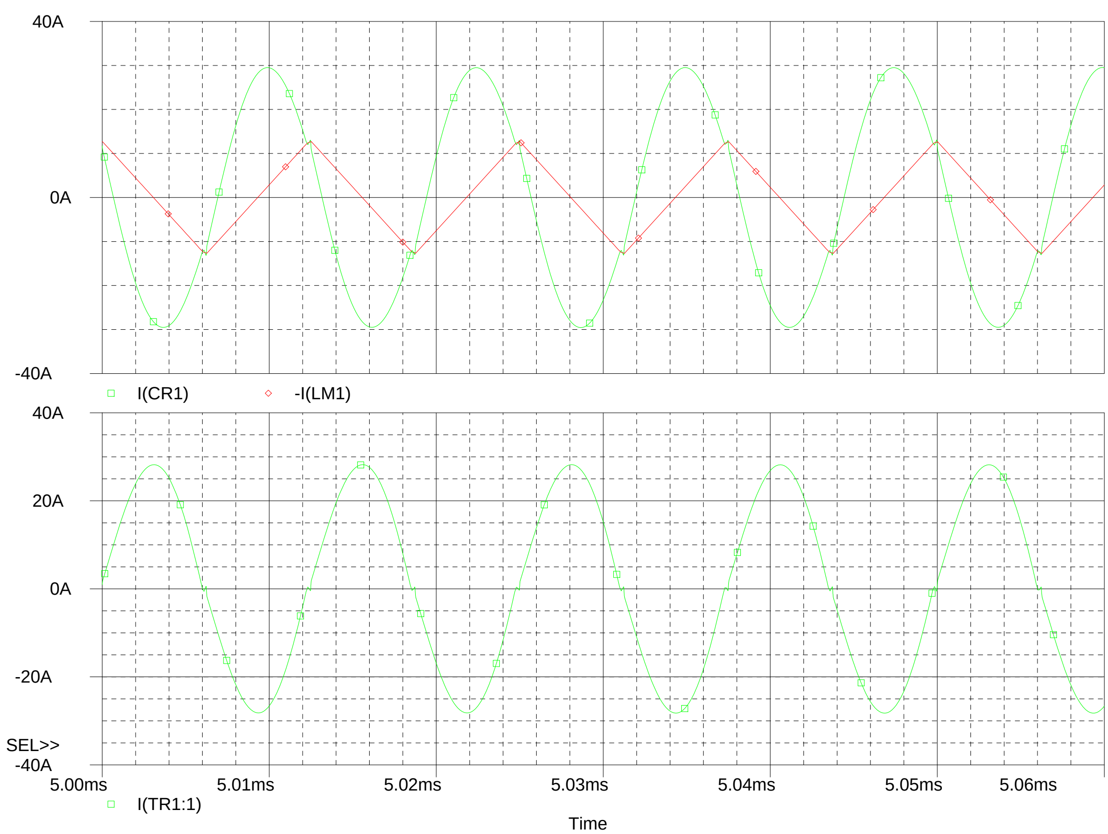


Figure 4.2: Simulation of the Operation of the Resonant Network

4.1.2 The Simulation of the Operation of the Resonant Network

The operation of the resonant network has been discussed in detail in Chapter 2.3.2. As shown in the Figure 2.15. The simulation results of currents I_r, I_m and I_s are all shown in Figure 4.3. The resonant current Ir is a sinusoidal wave, the magnetizing current I_m is a linear increasing or decreasing current and doesn't resonate with L_r and C_r. Because the voltage on L_m is clamped by the secondary output voltage (constant voltage). The current Is which is delivered to the secondary side is the difference between I_r and I_m.

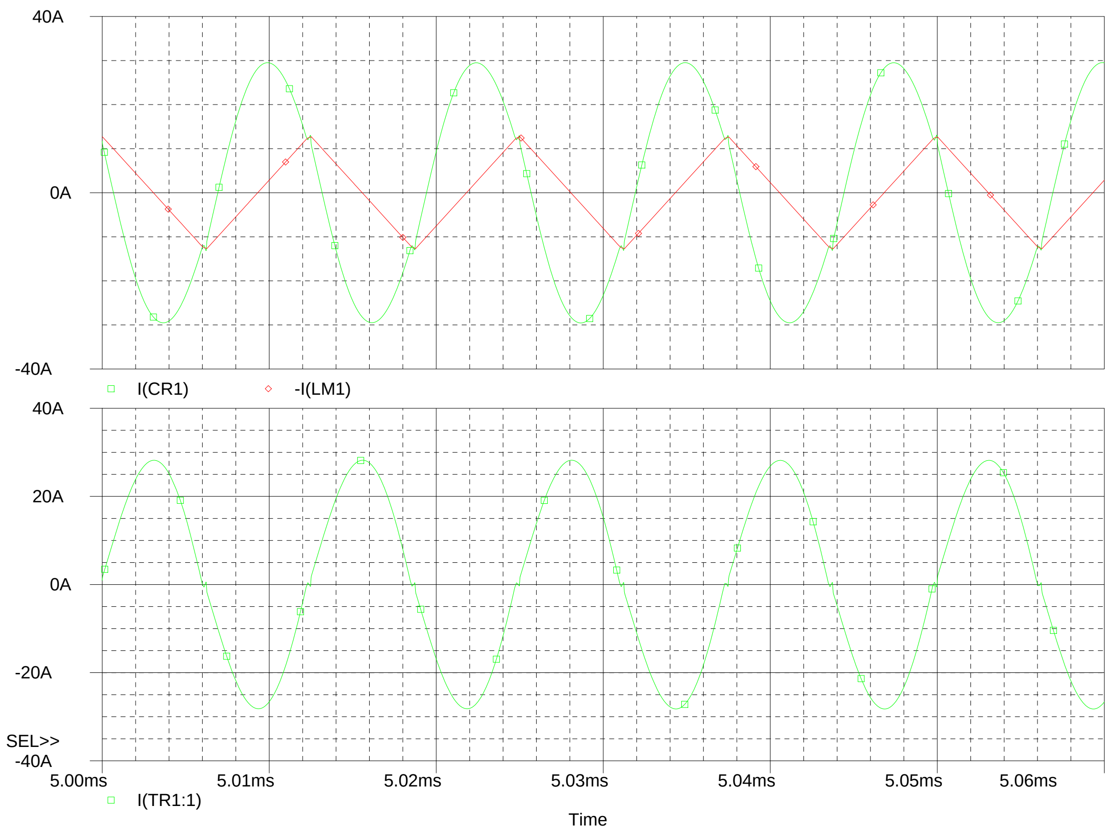
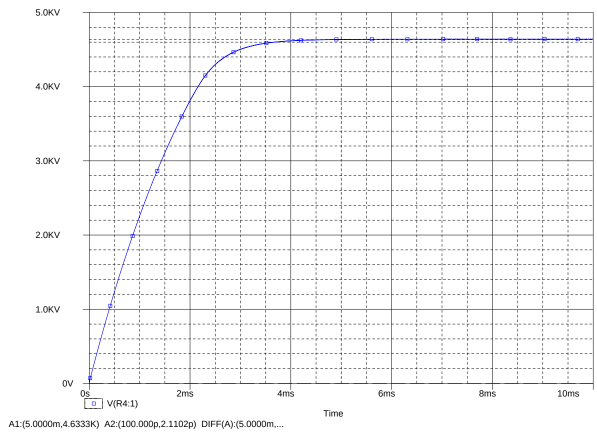


Figure 4.3: Simulation of the Operation of the Resonant Network

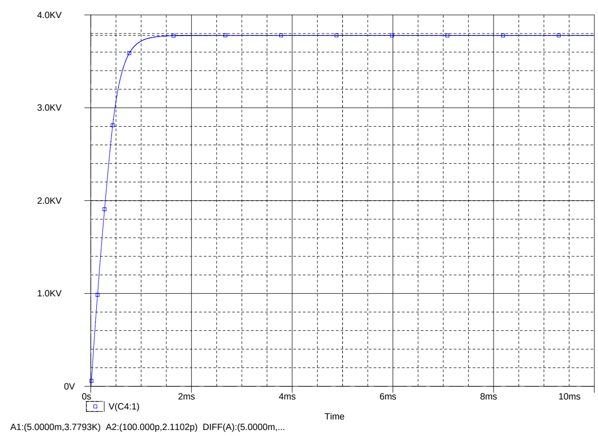
4.1.3 The Output Voltages at Different Switching Frequencies

As analyzed in the Chapter 2.3.1, the voltage gain M_g changes as a function of switching frequency as shown in Figure 2.12. The curves of M_g under different Q_e all have a peak value. In Section 2.4, Q_e of 0.4 is selected for this design. The maximum voltage gain M_g=1.25 is produced when the switching frequency is approximately $0.6 * f_o$.

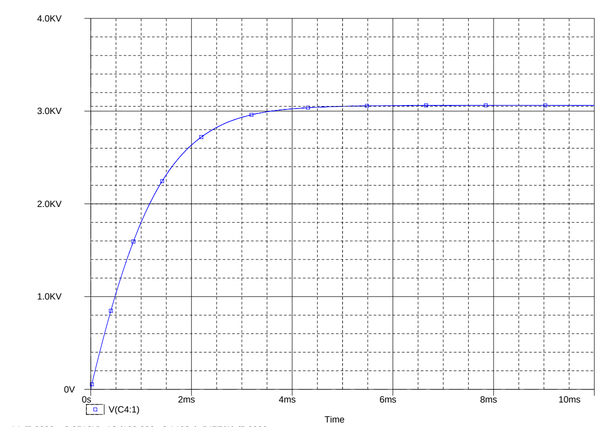
When the switching frequency increases beyond $0.6 * f_o$, the voltage gain M_g decreases and the power delivered also decreases. Therefore adjusting the power level of the microwave oven can be achieved by adjusting the switching frequency beyond $0.6 * f_o$. Three switching frequencies ($0.625 * f_o$, f_o and $1.667 * f_o$) are simulated in Pspice. The simulated output voltage as a function of time is shown in Figure 4.4 for each of the three selected switching frequencies. One will notice that the steady state output voltage decreases with increasing switching frequency: 4700 V at 0.625 f_o, 3980 V at f_o, and 2950 V at 1.667 f_o.



(a) $f_n = 0.625 f_o$

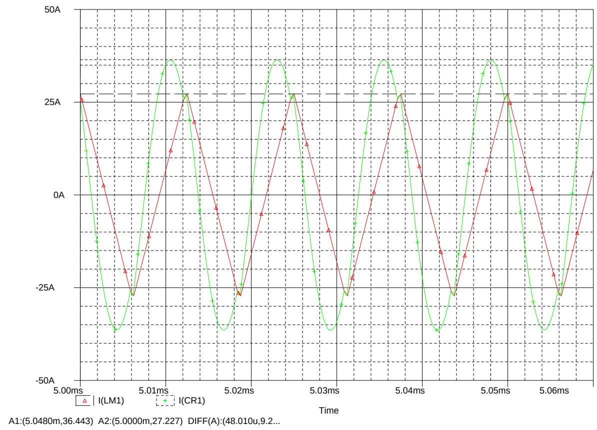


(b) $f_n = f_o$

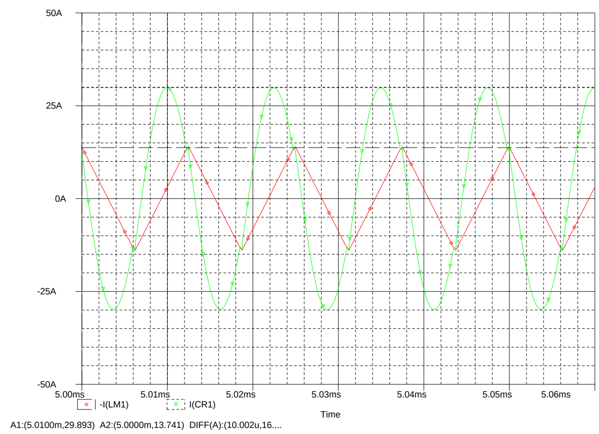


(c) $f_n = 1.667 f_o$

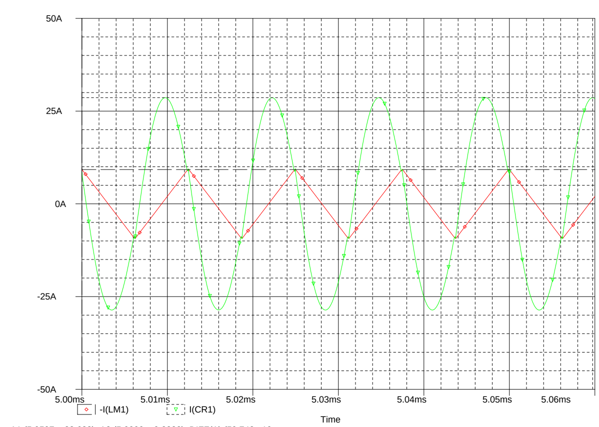
Figure 4.4: Output Voltages under Different Switching Frequencies



(a) $L_n = 3$



(b) $L_n = 6$



(c) $L_n = 9$

Figure 4.5: Resonant Current I_r and Magnetizing Current I_m under Different L_n

4.1.4 The Resonant Currents Under Different Inductor Ratio L_n (L_m/L_r)

L_n is defined as the ratio between L_m and L_r in Equation 2.23. L_n is a critical parameter to determine the operation of the resonant converter. During the exploration using the simulation, a problem emerged. The peak of the current I_m is too large and almost equals to the peak of the current Ir when L_n is small. That means a substantial current flows through the magnetizing inductor which will cause a lot of loss.

Increasing the magnetizing inductance can reduce the current I_m. Because the slope of the I_m vs. time is inversely proportional to the magnetizing inductance L_m. Therefore a larger L_m (also means a larger L_n) will reduce the peak of the current I_m substantially. The resonant current I_r and the magnetizing current I_m are simulated under three different L_n. They are shown in Figure 4.5.

4.1.5 Soft Switching Realization

As discussed in subsection 2.3.3, the zero-voltage switching (ZVS) during the MOSFET turn-on transition is one of the benefit of using the LLC resonant topology. The ZVS MOSFET turn-on transition is shown in Figure 4.6. Before the MOSFET Q2 is turned on, the voltage drop of Q2 has already reduced to 0 (closely) because of the conduction of the MOSFET body diode.

Soft switching is also realized on the secondary rectifier diodes. The current flowing in the rectifier diodes is the current difference between I_r and I_m. As observed in Figure 2.15, I_r and I_m has an intersection period. This intersection period is the transition between two PWM signals. The diode current I_d is zero during the intersection period. As shown in Figure 4.7, the diode current is reduced to zero before it turns off. This is called zero-current switching (ZCS) which reduces the switching loss substantially.

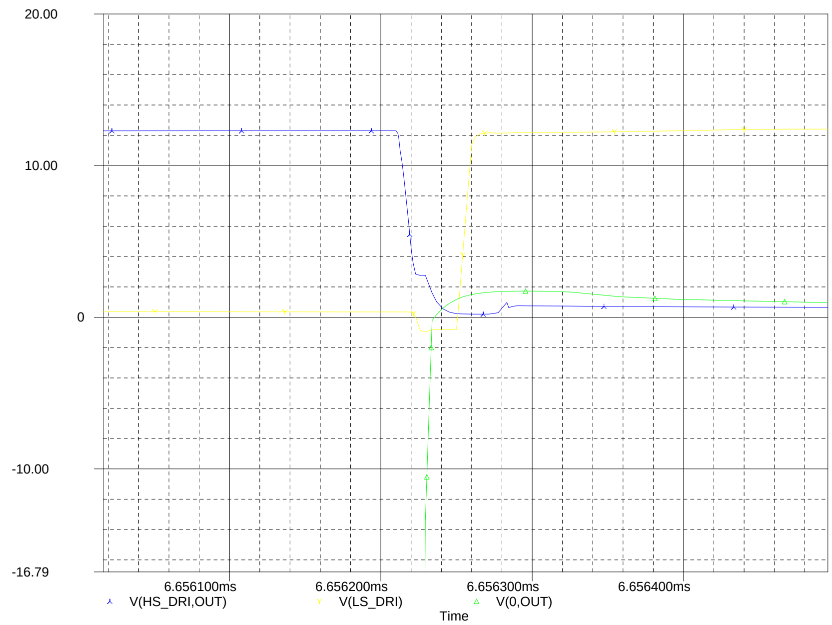


Figure 4.6: MOSFET(Q2) Turn on at Zero Voltage

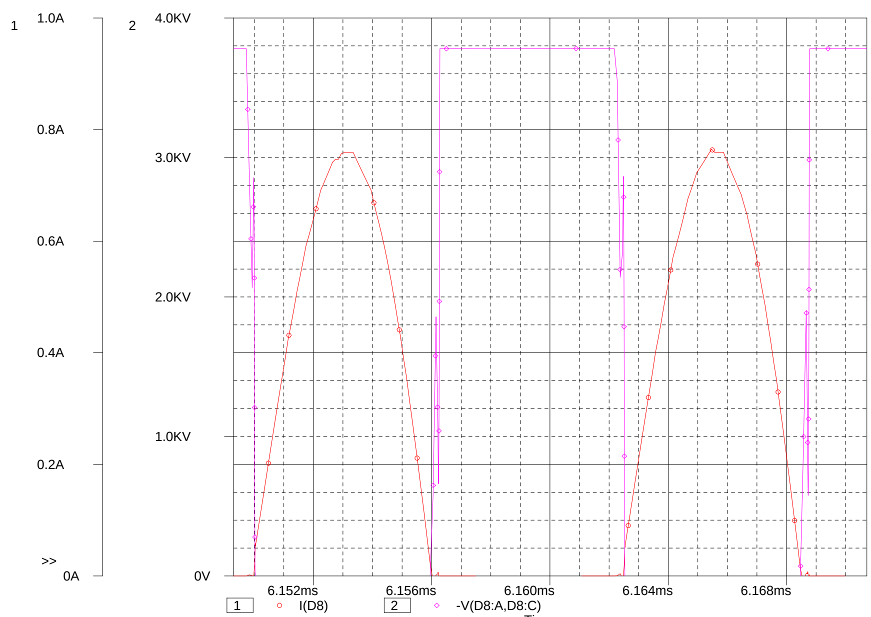
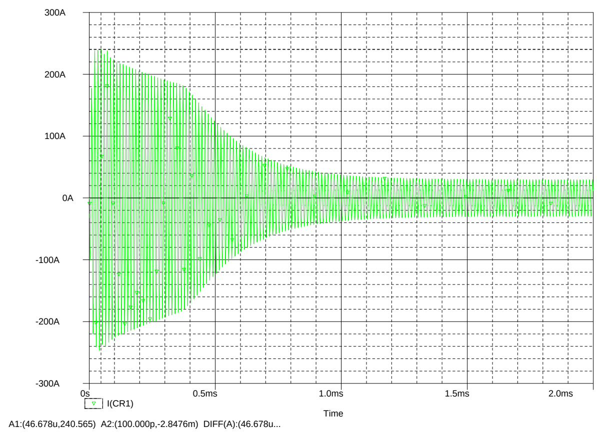


Figure 4.7: Rectifier Diode(D3) Turn off at Zero Current

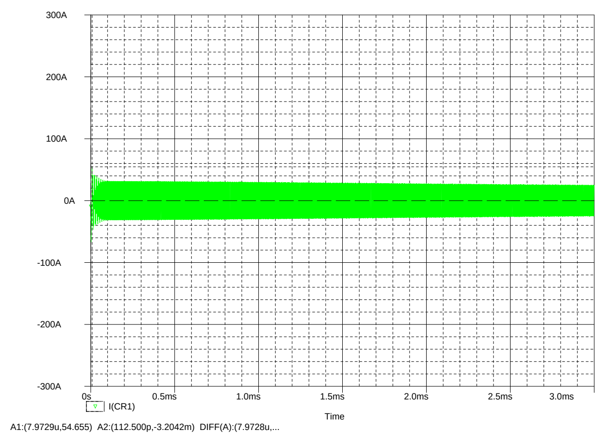
4.1.6 Soft Start

Due to the large resonant capacitance, filtering capacitance and parasitic capacitance, the start-up current can be huge. The huge start-up current of the resonant converter can damage the devices and produce a large scale EMI.

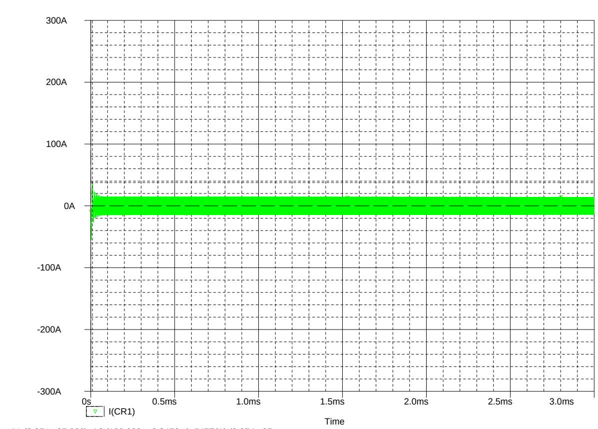
As analyzed in Chapter 2, the voltage gain M_g has a much smaller value under a high switching frequency which is shown in Figure 2.12. Based on this characteristic, the start-up current can be controlled by using a high frequency PWM to obtain a low output voltage. Thus the start-up current can be smaller. A DSP can be used to produce a high switching frequency during startup and the design switching frequency during steady state operation. The simulations of the start-up current under different frequencies are shown in Figure 4.8.



(a) $f_s = 80kHz$



(b) $f_s = 250kHz$



(c) $f_s = 500kHz$

Figure 4.8: Start Resonant Current under Different Frequencies

4.2 Experiment Results Discussion

The experiment tested is implemented based on the designed Prototype which is shown in the Figure 4.9. The complete circuit was tested using a low voltage power supply and a resistive load. A 6 V DC voltage was adopted as the input of the MOSFET bridge. The circuit was not tested at full voltage(and full load) due to a failure in the input full wave rectifier. The two complementary PWM signals from the DSP are shown in the Figure 4.10. There is a 100 ns dead time between the turn-on statuses of two MOSFETs.

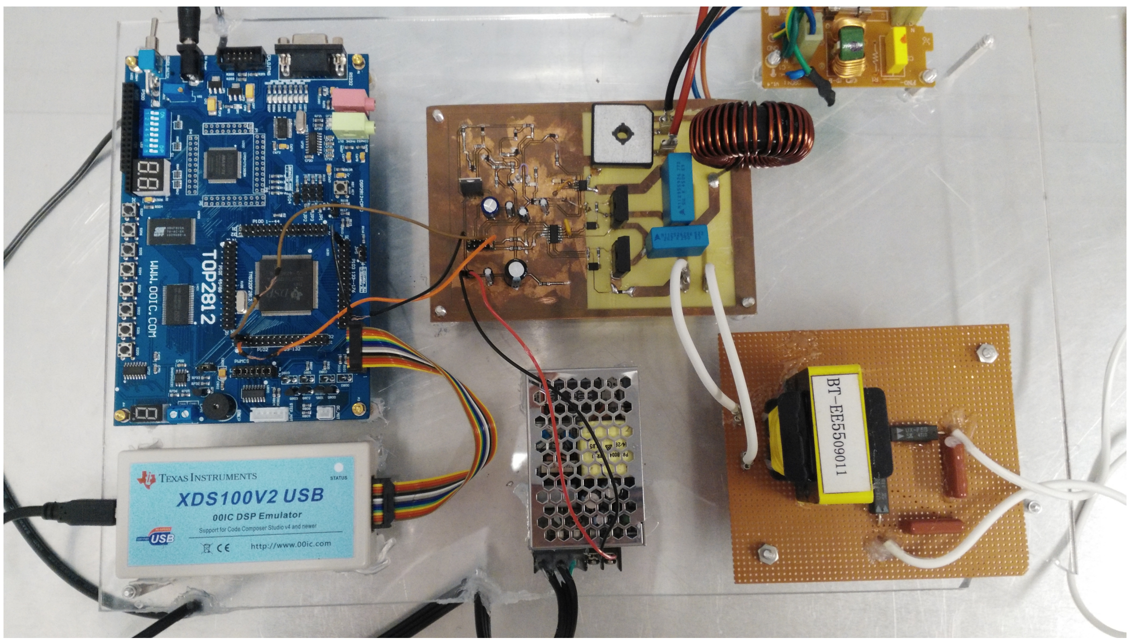


Figure 4.9: Picture of the System Prototype

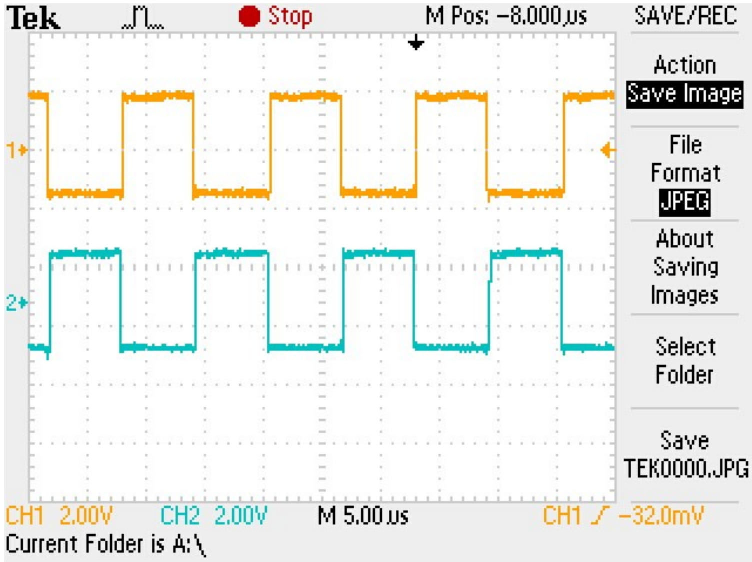


Figure 4.10: Two Complementary PWM Signals from DSP

The two complementary PWM signals are amplified by the driver IC, and the voltage of the turn-on stage is increased to 13.6 V which is shown in Figure 4.11 in order to drive the gates of the MOSFETs. The MOSFET switching waveform (channel 1) is shown in Figure 4.12,.

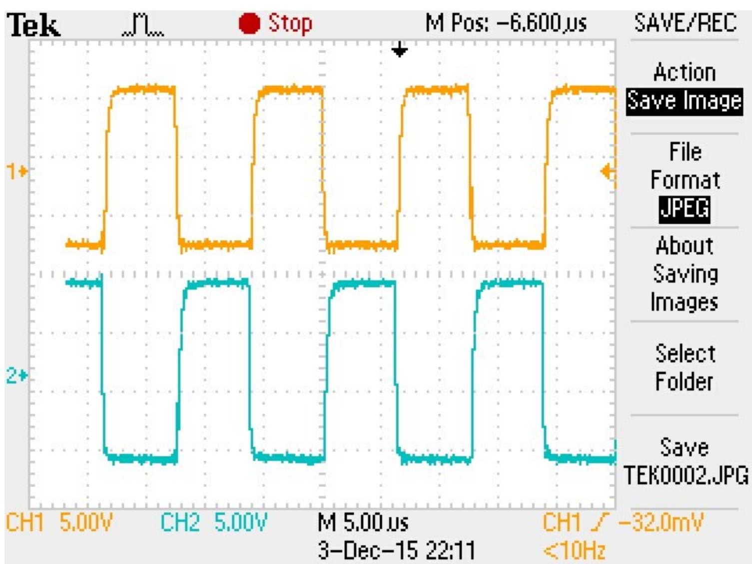


Figure 4.11: Two Complementary PWM Signals from Driver IC

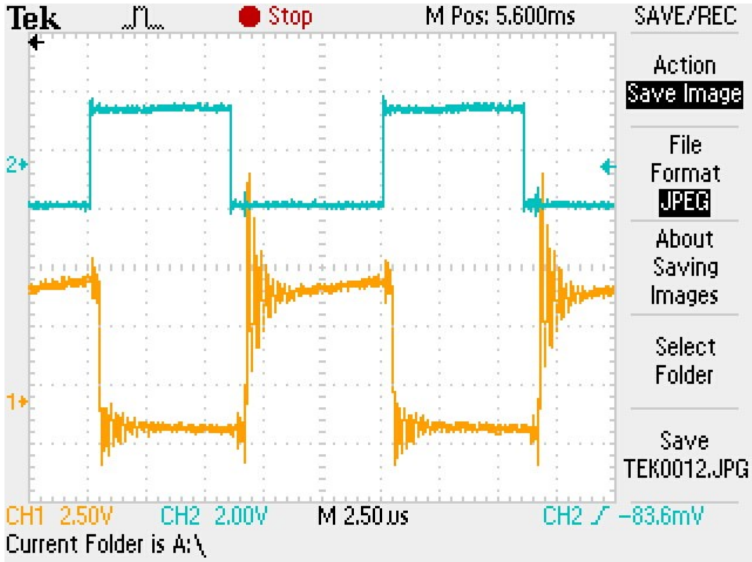


Figure 4.12: MOSFET Switching Waveform

The two MOSFETs alternatively conducts. The DC voltage applied on the MOSFET bridge is chopped into a square wave which has a frequency the same as the switching frequency. As shown in the Figure 2.11, the voltage of the primary side of the transformer is close to the square Vge, because the voltage drop on the C_r and L_r is close to 0V around the switching frequency f_o. The voltage on the secondary side of the transformer is also a square wave due to the clamping of the output capacitors. The voltage on the secondary side of the transformer is measured as in Figure 4.13. The peak to peak secondary voltage is about 150 volts as shown in Figure 4.13. The input voltage from the MOSFETs is about 6 volts, which gives a voltage gain of about 25 for this low voltage test.

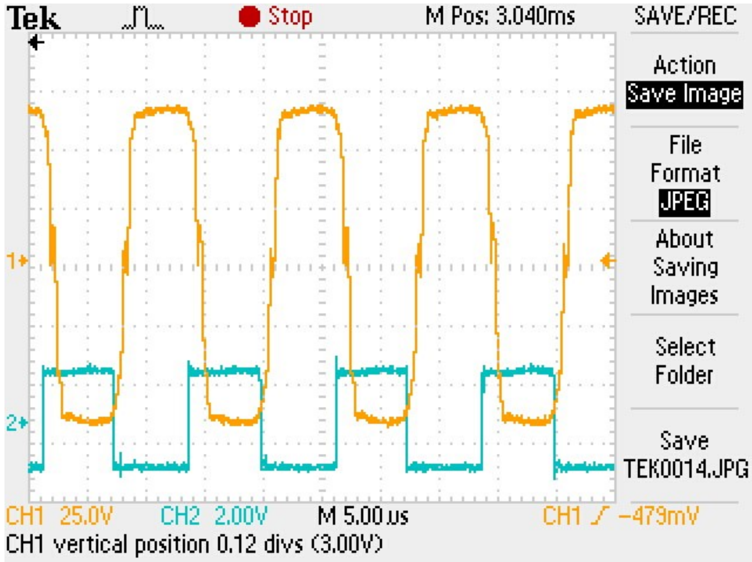


Figure 4.13: The Voltage on the Secondary Side of the Transformer(yellow);PWM signal (blue)

Finally the square wave output voltage of the secondary side of the transformer is doubled by the half-wave voltage doubler and filtered by the capacitor. The output voltage is a DC voltage which will be applied on the testing load. The output voltage on the load is shown in Figure 4.14.The volts per division in Figure 4.14 is 50 V.

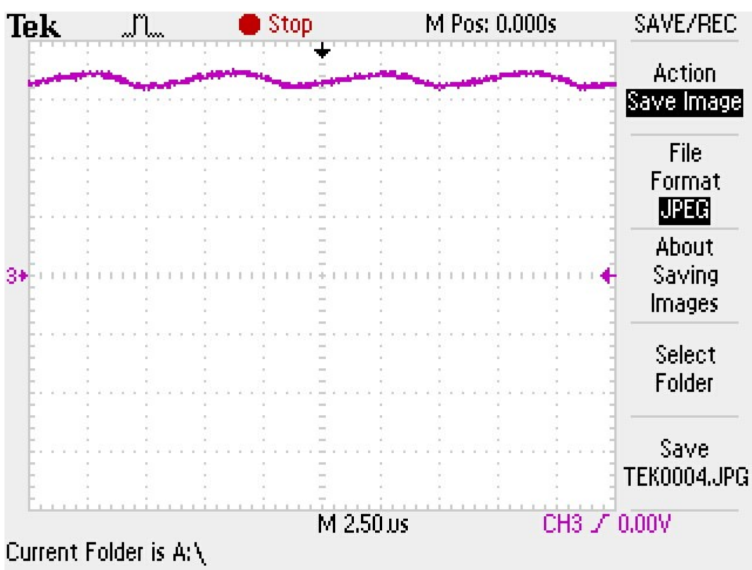


Figure 4.14: DC Output Voltage

The design specify a voltage gain of 40 from the input to the load. However the voltage gain from the input to the load is around 25. The voltage gain is much lower than expectation because of the voltage drop on the MOSFETs and the transformer core. When the input voltage is improved to the 108 V nominal rectified grid voltage, the effects of the the voltage drop on the MOSFETs and the transformer core can be ignored.

CHAPTER 5: CONCLUSION AND FUTURE WORK

This thesis designed a soft switching power supply forg magnetrons. The design includes the theoretical analysis, math derivation, simulation and hardware implementation.The soft switching power supply adopted a LLC based main circuit. The main circuit is analyzed step by step to show how the resonant network works. The mathematical derivation of the voltage gain gave a good guidance on analysis. The open-loop main circuit was simulated by Pspice.All the analyses are verified by the simulation results.

The main part of this thesis is the hardware design and implementation. The hardward design includes the integrated transformer design, inductor design, driver circuit, mixed-signal circuit,and firmware debugging. The integrated transformer had a good performance under lab testing. The switching bridge and the resonant network both worked as expected under the control of the driver circuit and mixed-signal circuit.

Future work includes: *(1)* test and debug the main circuit under full load condition, *(2)* refine the control firmware to obtain a precise control which can track the fluctuation of the input grid voltage, *(3)* Compare the design in this thesis to the switching power supply with PFC(Power Factor Correction), to see whether the effects of reducing THD is obvious or not.

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