BEHAVIORAL MODELING OF ZINC-OXIDE, THIN-FILM, FIELD-EFFECT TRANSISTORS AND THE DESIGN OF PIXEL DRIVER, ANALOG AMPLIFIER, AND LOW-NOISE RF AMPLIFIER CIRCUITS

by

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ABSTRACT

LEROY ALFRED CALDER III. Behavioral modeling of zinc-oxide, thin-film, field-effect transistors and the design of pixel driver, analog amplifier, and low-noise RF amplifier circuits. (Under the direction of DR. DAVID M. BINKLEY)

Zinc-oxide (ZnO) is of great interest due to transparent properties, high breakdown voltages, and low cost. Behavioral modeling is presented in this dissertation to model ZnO thin-film field-effect transistor (FET) drain current versus gate-source overdrive voltage. Initial findings show that in “strong inversion,” saturation, the drain current equation reveals a quartic-law dependency on gate-source overdrive voltage instead of square-law dependency seen in complementary metal-oxide semiconductor (CMOS) with no mobility reduction effects. This is postulated to result from the ZnO mobility showing a square-law increase with gate-source overdrive voltage. A “strong inversion,” saturation model having ±1.6% deviation from measured data is created in verilog-A to simulate and design circuits. Circuits include a fabricated and measured pixel driver circuit sinking 28 μA of current while only having a gate area of 20 μm^2. This ZnO thin-film FET pixel driver is believed to have the highest current density reported at the time of this writing. Also, the first known ZnO thin-film FET analog amplifier is analytically designed for a gain of 3 V/V at 10 kHz while drawing only 8 μA of supply current. Finally, the first known ZnO thin-film FET low-noise RF amplifier is designed, utilizing scattering parameters measured at the Air Force Research Laboratory on a device with minimum channel length of 1.25 μm. This amplifier has a small-signal gain of 12.6 dB at 13.56 MHz, and a current drain of 268.4 mA at a drain voltage of 13 V.

DEDICATION

This work is dedicated to my wife, Heather. She has been my source of hope, my source of inspiration, and my constant supporter throughout this process. No matter how frustrated or discouraged I might have become, she has always been there to show me the love and confidence of a true best friend. This work would not have been possible otherwise.

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Leroy Alfred 'Alan' Calder, III

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LIST OF ABBREVIATIONS

ZnO	Zinc-Oxide
FET	Field-Effect Transistor
GaAs	Gallium-Arsenide
CMOS	Complementary Metal-Oxide Semiconductor
IC	Integrated Circuit
eV	Electron-Volt
ITO	Indium Tin Oxide
LCD	Liquid Crystal Display
PDP	Plasma Display Panel
OLED	Organic Light Emitting Display
RF	Radio Frequency
LNA	Low-Noise Amplifier
ADS	Advanced Design System
AFRL	Air Force Research Laboratory
GaN	Gallium-Nitride
SiO_2	Silicon Dioxide
PECVD	Plasma-Enhanced Chemical Vapor Deposition
MOSFET	Metal-Oxide Semiconductor FET
DC	Direct Current
AC	Alternating Current

VNA	Vector Network Analyzer
TV	Television
LED	Light Emitting Diode
ESD	Electro-Static Discharge
FIB	Focused Ion Beam
MAG	Maximum Available Gain

CHAPTER 1: INTRODUCTION

1.1 Opportunities for Zinc-Oxide Thin-Film FET Circuits

Zinc-oxide (ZnO) is relatively new to the semiconductor industry. Zinc-oxide was used for centuries as part of various metallurgical activities and has found its most recent uses in applications such as rubber manufacturing, cement processing, and most commonly as a barrier cream used for nappy rash or diaper rash [1]. Recently, ZnO has found another use in the electronics industry for thin-film transistors. In this chapter, three distinct reasons are presented for use of this new material in electrical engineering and materials communities.

The primary motivation of any new technology is the economic impact. If a material is too cost prohibitive or too difficult to repeatedly manufacture, then it is unlikely to find funding to pursue research further. ZnO is an abundant material, found all over the world [2], and is less costly to fabricate in a low temperature process on various substrates such as amorphous glasses and plastics [3]. Also, when dealing with integrated electronics, ZnO thin-film field-effect transistors (FETs) are used in conjunction with gallium arsenide (GaAs) or silicon CMOS (complementary metal-oxide semiconductor) integrated circuits (IC's) easily at the module level.

The most recent area to use ZnO thin-film FETs is pixel selection and driver circuits [2]. ZnO is a II-VI compound semiconductor with a wide direct bandgap of 3.35 electron

volts (eV) [3]. Because of this wide band gap property, which results in transparency, ZnO thin-film FETs have found acceptance in the area of display electronics. ZnO is a viable alternative to the more expensive indium tin oxide (ITO), which is found in most commercial liquid crystal displays (LCD's), plasma display panels (PDP's), and organic light-emitting displays (OLED's) [4]. Due to its transparency, ZnO is able to overcome issues of size associated with most pixel driver circuits. Pixel driver circuits must be kept small in order to allow the pixel unobstructed access to the front of the display. Since ZnO thin-film FETs allow light to pass through them, larger ZnO transistors are used that are nearly the size of the pixel with very little loss of lumen performance within the display [5]. In addition to the ability to create more vivid pixels, the ZnO thin-film FET is a voltage controlled device, with little current leakage. Low current leakage translates into efficient pixel driver circuits that do not dissipate much current in the off state.

Finally, a large focus of this dissertation is in the area of military and consumer electronics using ZnO thin-film FETs. In addition to pixel driver circuits, an analog amplifier and a radio frequency (RF) low-noise amplifier (LNA) are designed. As previously mentioned, the ZnO thin-film FET has a large band gap of 3.35 eV. Advantages associated with wide band gaps include: high breakdown voltages, ability to sustain large electric fields, lower electronic noise, and high temperature and high power operation [6]. For these reasons, there is motivation to begin an investigation into applications for analog and RF electronics that would be beneficial to the military and consumer electronics community. An analog differential amplifier is designed to show micro-power performance and predictable gain for an all-NFET style operational

amplifier. In addition, the RF performance of the ZnO thin-film FET is demonstrated with a low-noise RF amplifier with high current density (335.5 μA/μm), which translates to high power density [2]. The low-noise RF amplifier is designed in Agilent Advanced Design System® (ADS) using two-port measured scattering parameters (S-parameters) on a ZnO thin-film FET, with a gate-oxide thickness of 22 nm and a gate length of 1.25 μm.

In conclusion, several factors are presented that have motivated the research in circuit design and fabrication of ZnO thin-film FETs for use in multiple applications. These applications are cost-effective pixel driver circuits, analog amplifiers, and low-noise RF amplifiers. As the technology improves, there are opportunities for numerous other circuit designs to develop which may benefit both consumer and military applications.

1.2 Research Contributions

The following are the novel research contributions of this dissertation:

1. A ZnO thin-film FET behavioral drain current and capacitance model to allow for hand design and simulation of circuit performance in the Cadence design suite. This drain current shows a fourth order dependency on gate-source overdrive voltage for “strong inversion,” saturation, operation. The quartic-law behavioral model accurately tracks the measured performance to within ±1.6%. This quartic-law operation is in contrast to square-law operation for traditional bulk CMOS, without mobility reduction effects. Modeling is performed on the mobility that shows a square-law increase with gate-source overdrive voltage,

which is considered a possible source of the drain current quartic-law "strong inversion," saturation operation. Also, for the "strong inversion," non-saturation or ohmic operation, the drain current shows a gate-source overdrive voltage raised to the 2.3 power instead of unity as expected in bulk CMOS. The models are evaluated using Air Force Research Laboratory ZnO thin-film FETs having a minimal channel length of 2 μm and a gate-oxide thickness of 30 nm. These FETs are also used for the design of pixel drivers and analog amplifier circuits.

2. A fabricated pixel driver, which can sink 28 μA while having a gate area of only 20 μm^2. This pixel driver is believed to be the smallest published with high current density (14.5 μA/μm) at a low drain voltage of 2 V. This performance matches the drain current model of Chapter 3 and gives confidence for future pixel driver designs. Performance is confirmed with verilog-A simulation in the Cadence design suite.
3. A ZnO thin-film FET analog amplifier is analytically designed utilizing the behavioral model of Chapter 3. It is believed to be the first ZnO thin-film FET analog amplifier to be designed. The amplifier is designed to have a gain of 3 V/V at 10 kHz, with rail voltages of ± 5 V and a total current consumption of 8 μA.
4. A low-noise RF amplifier is designed from scattering parameters measured at the Air Force Research Laboratory for ZnO thin-film FETs having a gate length of 1.25 μm and a gate-oxide thickness of 22 nm. This design achieves 12.6 dB of gain while having less than 16.5 dB of input return loss, less than 13.7 dB of

output return loss and less than 16 dB of reverse isolation in a 50 Ω system. The amplifier is designed for the RFID tag frequency of 13.56 MHz.

1.3 Dissertation Organization

Chapter 2 gives an overview of the ZnO thin-film FET. Fabricated device layers are discussed in order to describe the operation and fabrication of the Air Force Research Laboratory (AFRL) devices used in this research. Chapter 3 describes the methodology used to extract model parameters for the ZnO thin-film FET drain current model. Model parameters are then used to create a full behavioral model of the drain current and capacitances of a ZnO thin-film FET with a gate oxide thickness of 30 nm and a gate length of 2 µm. In Chapter 4, a ZnO pixel driver circuit is designed and discussed. Measured data is collected and compared with the modeled and simulated results to show accuracy of the modeling equations. Chapter 5 presents a micro-power differential amplifier utilizing an all-NFET architecture. Design and simulation of the amplifier is discussed as it relates to the model and simulation data. Chapter 6 gives the design of a low-noise RF amplifier. Measured scattering parameters are used to simulate and design the amplifier using the newest ZnO thin-film FET technology from AFRL having 1.25 µm gate length and a gate oxide thickness of 22 nm. Finally, Chapter 7 concludes the dissertation with an overall summary and discussion of novel information discovered through this research. This chapter concludes with proposed future research for ZnO thin-film FETs. Finally, Appendix A includes the verilog-A program used to implement the ZnO thin-film FET behavioral model in the Cadence design suite with the Spectre® simulator.

CHAPTER 2: OPERATION OF THE ZNO THIN-FILM FET

2.1 ZnO Thin-Film FET

In Chapter 1, a brief introduction of the advantages of ZnO was presented. Chapter 2 explores the fabrication of ZnO thin-film FETs, specifically Air Force Research Laboratory (AFRL) devices used in this research.

ZnO thin-film FETs have become of great interest in the electronics field due to their many advantages, such as high temperature, high power operation, and similarity in many ways to gallium-nitride (GaN) [7]. Another characteristic that is advantageous for electronic applications is the high current on/off ratio, currently greater than 10^{12} [8]. Design of the transistors, including oxide thickness, and width and length of the channel, is very important in determining the on/off ratio, which is most important for low-leakage switching. In (2.1), a relationship is given in [9] that allows for the design of a general leakage current approximation for a ZnO thin-film FET:

$$I_{DS\,off} = \frac{\sigma W \tau}{L} V_{DS} \tag{2.1}$$

Here σ is the electrical conductivity, τ is the thickness of the channel layer, W and L are the respective width and length of the conduction channel, and V_{DS} is the source-drain voltage [8]. From (2.1) it is apparent that channel thickness, width, and length must be optimized in order to provide the desired off current performance for a given source-drain voltage. Low leakage is primarily the result of the low conductivity of native ZnO.

Another advantage of the ZnO thin-film FET is the ability to have high output resistance when operating in saturation where $V_{DS} > V_{DS,sat}$, the drain current saturation voltage [10]. It is desirable to have high output resistance in amplifier configurations to maximize small-signal resistances and voltage gain.

Finally, as with GaN, ZnO thin-film FETs do not yet have a stable p-type FET available for complementary logic circuits. This is due to low solubility of p-type dopants and their compensation by abundant n-type impurities [11]. Previous work in [12], however, shows that a p-type material may be grown, thereby allowing for very low-power complementary logic circuits in the future. This would of course hinge upon a p-type process becoming stable for production process fabrication.

2.2 ZnO Thin-Film FET Operation

The understanding of possible ZnO thin-film FET accumulation operation is not conclusive. There are several theories, including the grain boundary theory, the Fermi level theory, and the ionized impurity scattering mechanism theory.

The most popular theory to date is the grain boundary theory. Due to the polycrystalline nature of ZnO channels, it is theorized that as the gate-source voltage increases, the potential of free carrier charge with respect to fixed charge increases. This increase of free carrier charge also increases the charge density of the induced free carrier, resulting in reduction of the potential barrier at the grain boundaries [13]. This is the first theory to be proposed and is still quite popular in the ZnO literature.

The second theory involves the Fermi level and carrier concentration. In [5] researchers propose that the interface states pin the Fermi level near the conduction

band, which creates an accumulation layer, at a sufficient gate-source voltage. That accumulation layer then requires a gate-source voltage below zero in order to fully turn off the device.

The last theory involves the ionized impurity scattering mechanism, which may be responsible for the accumulation operation. In [4] an experiment was conducted in which gallium was added to a ZnO channel under the assumption that the grain size would decrease and therefore would also decrease the mobility in reference to a native ZnO channel. However, this resulted in little change to the mobility and led the researchers to infer that ionized impurity scattering was responsible rather than the dominant grain-boundary mechanism theory.

2.3 Air-Force Research Laboratory Devices

Devices used in this work are fabricated at the Air Force Research Laboratory (AFRL) at Wright-Patterson Air Force base. An introduction to the fabrication layers of the AFRL ZnO thin-film FET is given, followed by the fabrication process parameters.

The AFRL ZnO thin-film FET fabrication layers are shown in Figure 2.1. Note that this FET design has the gate buried under the channel versus a top gate design.

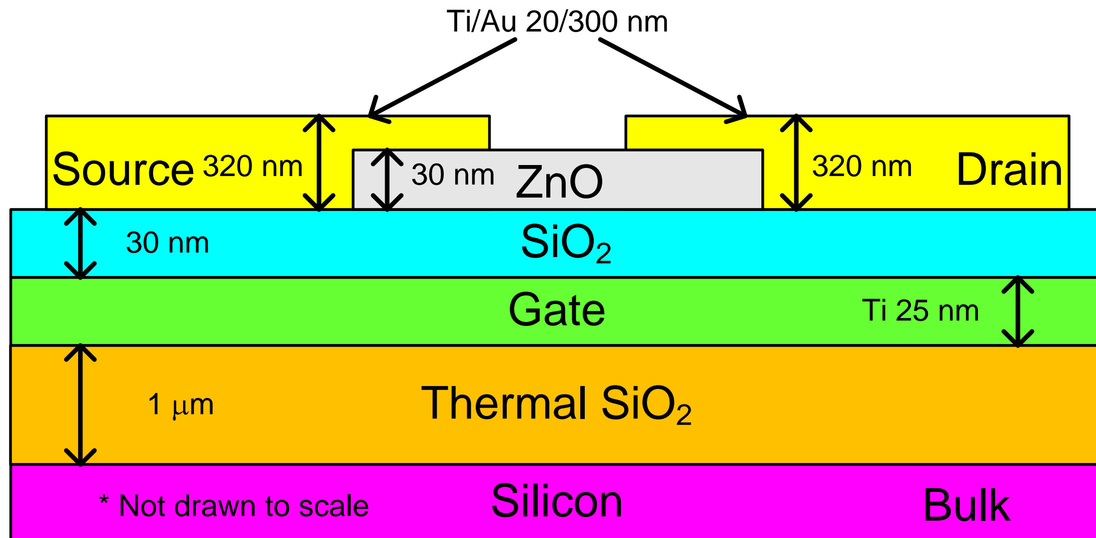

Figure 2.1. Air Force Research Laboratory ZnO thin-film FET fabrication layers (not drawn to scale) [8].

The AFRL devices are fabricated on thermally grown SiO_2-covered silicon wafers [8]. ZnO films were deposited using pulsed laser deposition. The substrate is heated to 350 degrees Celsius while being rotated during deposition [8]. The bottom gate is made of titanium and is 25 nm thick. The drain and source are made of titanium/gold layers of 20 nm and 300 nm, respectively. The SiO_2 gate insulator is deposited using plasma-enhanced chemical vapor deposition (PECVD) to a thickness of 30 nm [8]. All annealing is done at 400 degrees Celsius. The process is outlined in Table 2.1, which lists the equipment used to complete the given step.

Measurements are taken using scattering parameters (S-parameters) to find the frequency limitations of the transistors at 2 µm gate lengths. The f_T and f_{max} are measured to be 400 MHz and 500 MHz respectively [8]. It is estimated that when the process goes to a 1 µm gate length, f_T and f_{max} will increase into the low GHz range.

Table 2.1. Process steps and measurements for Air Force Research Laboratory ZnO thin-film FETs [8].

Step Descriptor	Equipment	Comments
Intial wafer	NA	SiO_2-covered silicon wafers
ZnO film deposition	Neocera Pioneer 180	Pulsed laser deposition (PLD) with Krypton-Flouride (KrF) laser
Chamber base pressure	chamber	4 x 10^{-8} torr with O_2 background gas during deposition to 150 mtorr
Substrate temp at deposition	backside heater	350 degrees Celsius (rotated during deposition)
Gate	NA	titanium gate at 25 nm thick
Gate insulator	PECVD	30 nm thick SiO_2
Annealing	NA	Class 100 clean room with 400 degrees Celsius for 10 minutes after deposition and before source/drain contact fabrication
DC characterization	Agilent 4156C Precision Semiconductor Parameter Analyzer	All dc curves taken on devices with an L = 2 μm
f_T and f_{max}	HP8751A Network Analyzer	S-parameters used to determine S_{21}

In conclusion, the ZnO thin-film FET fabrication process steps are presented. Each layer of the fabricated device is described and dimensions are given as these differ from standard silicon CMOS devices. The AFRL ZnO thin-film FETs discussed here are used exclusively in the remainder of this dissertation.

CHAPTER 3: BEHAVIORAL MODELING OF ZNO THIN-FILM FETS

This chapter describes the behavioral modeling of ZnO thin-film FETs. Behavioral models are created to describe the drain current operation, low frequency small-signal operation to include capacitance, and the RF small-signal model. Derivations and theory are used to describe how the models are created and assumptions used.

3.1 DC Device Modeling

3.1.1 Derivation of the M value

M_{nonsat}, is the gate-source effective voltage power law exponent for drain current in the non-saturation region. It is determined with data from the ZnO thin-film FET in the deep ohmic region, or non-saturation region defined $V_{DS} << V_{DS,sat}$. The non-saturation data is collected with a voltage on the drain of 0.1 V. M_{sat}, is the gate-source effective voltage power law exponent for the drain current in the "strong inversion," saturation region of operation. It is determined using the saturation region, defined as $V_{DS} \geq V_{DS,sat}$. The "strong inversion" region is defined as $V_{GS} - V_T > V_{EFFSI,onset}$, where $V_{GS} - V_T$ is the effective voltage, and $V_{EFFSI,\text{ onset}}$ is 0.5 V as observed from drain-current power law behavior versus gate-source voltage as seen later in Figure 3.1.

Before modeling ZnO thin-film FETs, a brief review of the drain-current equation for bulk CMOS is given from [14] in (3.1) for strong inversion ($V_{GS} - V_T > 0.25$ V), saturation ($V_{DS} \geq V_{DS,sat}$) operation. Here the drain current is given by

$$I_D = \frac{1}{2} \cdot \mu \cdot C'_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_{GS} - V_T)^2 \quad (3.1)$$

where μ is the field-effect mobility, C'_{ox} is the gate capacitance per unit area, W is the width of the gate, and L is the length of the gate. In saturation, ($V_{DS} \geq V_{DS,sat}$), neglecting drain-source conductance, g_{ds}, effects, the drain current of a general power-law device can be expressed as

$$I_D = \left(\frac{W}{L}\right) \cdot k'_{satSI} \cdot (V_{GS} - V_T)^{M_{sat}} \quad (3.2)$$

where

$$k'_{satSI} = constant \quad (3.3)$$

The transconductance g_m is found from (3.2) as

$$g_m = \frac{\delta I_D}{\delta V_{GS}} = \frac{\delta I_D}{\delta (V_{GS} - V_T)} = M_{sat} \cdot \left(\frac{W}{L}\right) \cdot k'_{satSI} \cdot (V_{GS} - V_T)^{M_{sat}-1} \quad (3.4)$$

Also from equations (3.4) and (3.2) the transconductance efficiency is calculated as

$$\frac{g_m}{I_D} = \frac{M_{sat} \cdot \left(\frac{W}{L}\right) \cdot k'_{satSI} \cdot (V_{GS} - V_T)^{M_{sat}-1}}{\left(\frac{W}{L}\right) \cdot k'_{satSI} \cdot (V_{GS} - V_T)^{M_{sat}}} = \frac{M_{sat}}{V_{GS} - V_T} \quad (3.5)$$

The transconductance can also be expressed as

$$g_m = \frac{g_m}{I_D} \cdot I_D = \frac{M_{sat} \cdot I_D}{V_{GS} - V_T} \quad (3.6)$$

Solving (3.2), for $V_{GS} - V_T$ gives

$$(V_{GS} - V_T)^{M_{sat}} = \frac{I_D}{\left(\frac{W}{L}\right) \cdot k'_{satSI}} \tag{3.7}$$

where

$$V_{GS} - V_T = \left(\frac{I_D}{\left(\frac{W}{L}\right) \cdot k'_{satSI}}\right)^{\frac{1}{M_{sat}}} \tag{3.8}$$

Substituting (3.8) into (3.6), gives another expression for the transconductance efficiency, given by

$$\frac{g_m}{I_D} = \frac{M_{sat}}{\left(\frac{I_D}{\left(\frac{W}{L}\right) \cdot k'_{satSI}}\right)^{\frac{1}{M_{sat}}}} \tag{3.9}$$

Equation (3.9) shows that $\frac{g_m}{I_D}$ is inversely proportional to the drain current raised to the *$1/M_{sat}$* power, or

$$\frac{g_m}{I_D} \propto \frac{1}{(I_D)^{\frac{1}{M_{sat}}}} \tag{3.10}$$

Equation (3.2) shows the drain current is proportional to $V_{GS} - V_T$ raised to the M_{sat} power, or

$$I_D \propto (V_{GS} - V_T)^{M_{sat}} \tag{3.11}$$

Equation (3.11) shows that $V_{GS} - V_T$ is proportional to the drain current raised to the $\frac{1}{M_{sat}}$ power, or

$$(I_D)^{\frac{1}{M_{sat}}} \propto V_{GS} \tag{3.12}$$

As seen in (3.12), M_{sat} may be extracted from measured data using $(I_D)^{\frac{1}{M_{sat}}}$ as the y-axis and V_{GS} as the x-axis. When the M_{sat} value models the performance correctly, it fits a straight line for "strong inversion," saturation operation. Assumptions are made that this performance characteristic carries over into non-saturation as well, but for a different power-law exponential, M_{nonsat}. In the following sections, M_{sat} and M_{nonsat} curve fitting is shown in a graphical format for both saturated and non-saturated conditions.

3.1.2 Saturation Region Modeling

To extract M_{sat}, the following conditions were used: V_{DS} = 2 V and V_{GS} = 0.5 V to 2.5 V, where $V_{DS} \geq V_{DS,SAT} \approx V_{GS} - V_T$.

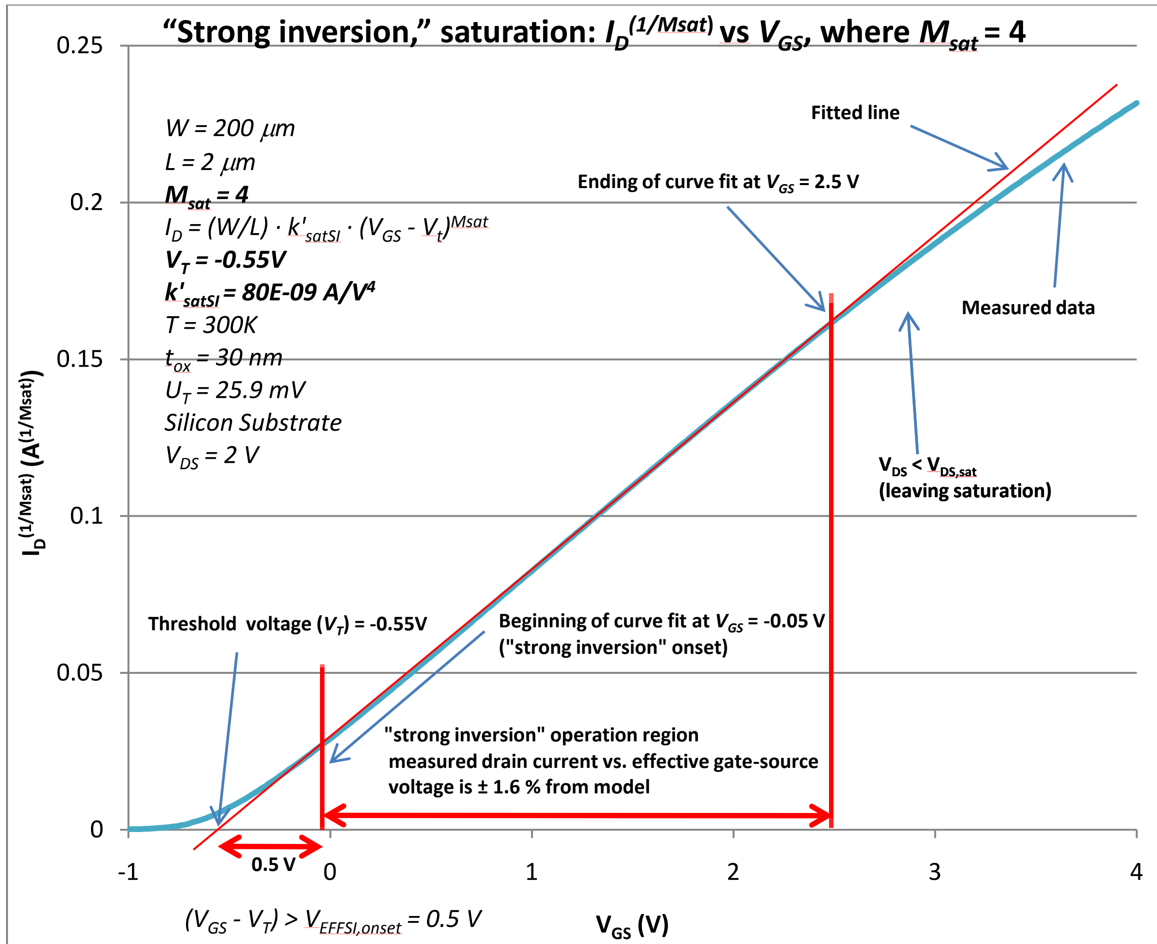

Figure 3.1. Measured and modeled drain current versus gate-source voltage for "strong inversion," saturation region of operation for M_{sat} = 4, V_{DS} = 2 V. Curve fit is within ±1.6% of measured drain current for V_{GS} = -0.05 V to 2.5 V.

In Figure 3.1, the line drawn on the curve fits measured drain current within ±1.6% for an M_{sat} value of 4.

Performance data of AFRL ZnO thin-film FET devices show that mobility increases as V_{GS} increases while V_{DS} is held constant. For an L = 2 µm device, using a polynomial curve fit on the extracted data from [15], a mobility slope greater that unity is observed. As shown in Figure 3.2, the "strong inversion" region of operation curve fit reveals that mobility increases as the square of V_{GS} - V_T.

The mobility data in Figure 3.2 is taken with a drain voltage of 0.5 V. This puts the transistor in the ohmic region ($V_{DS} < V_{DS,sat}$). For purposes of initial modeling, this ohmic region mobility is used in the saturation region. The mobility shows a square-law operation with V_{GS} - V_T and, when multiplied by a square-law FET model of (3.1) gives a consistent quartic law operation for the device drain current versus V_{GS} - V_T shown in Figure 3.1.

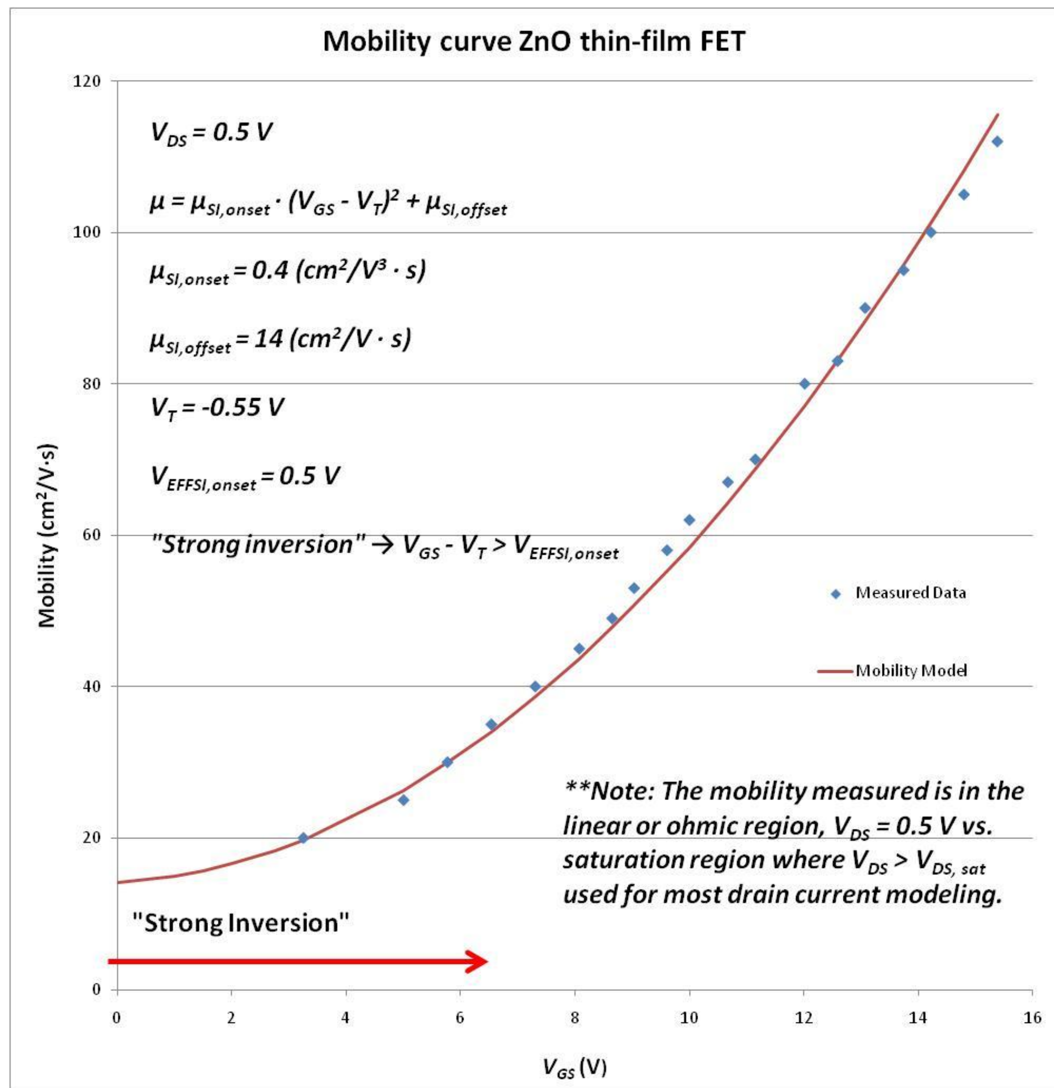

Figure 3.2. Measured and modeled ZnO thin-film FET mobility versus gate-source voltage at V_{DS} = 0.5 V.

The mobility has a square law operation with respect to V_{EFF} = V_{GS} - V_T. The mobility can be modeled by

$$\mu = \mu_{SI,onset}\left[\frac{cm^2}{V^3 \cdot s}\right](V_{GS} - V_T)^2 + \mu_{SI,offset}\left[\frac{cm^2}{V \cdot s}\right] \tag{3.13}$$

In the mobility fitting of Figure 3.2, $\mu_{SI,onset}$ is 0.4$\left[\frac{cm^2}{V^3 \cdot s}\right]$, $\mu_{SI,offset}$ is 14 $\left[\frac{cm^2}{V \cdot s}\right]$, and V_T is -0.55 V. Based on a threshold voltage of -0.55 V, the "strong inversion" onset is believed to occur at 0.5 V effective voltage, (V_{GS} - V_T). Equation (3.14) gives the "strong inversion" onset voltage as

$$V_{EFFSI,onset} = V_{GS} - V_T = -0.05\ V - (-0.55\ V) = 0.5\ V \tag{3.14}$$

For ZnO thin-film FET "weak inversion," saturation region modeling, the bulk CMOS weak inversion, saturation region equation in (3.15) from [14] is used as an initial model.

$$I_D(WI) = 2 \cdot n \cdot \mu \cdot C'_{ox} \cdot U_T^2 \cdot \left(\frac{W}{L}\right) \cdot \left(e^{\frac{V_{GS} - V_T}{n \cdot U_T}}\right) \tag{3.15}$$

From this relationship in bulk CMOS, a similar drain current model is derived for ZnO thin-film FETs, where "weak inversion" is defined as $V_{GS} - V_T < V_{EFFWI}$ = -0.13 V. The "weak inversion," saturation drain current is modeled as

$$I_D(WI) = k'_{satWI} \cdot \left(\frac{W}{L}\right) \cdot \left(e^{\frac{V_{GS} - V_T}{n \cdot U_T}}\right) \tag{3.16}$$

where k'_{satWI} is used as the constant value for “weak inversion,” saturation operation as shown in Figure 3.3.

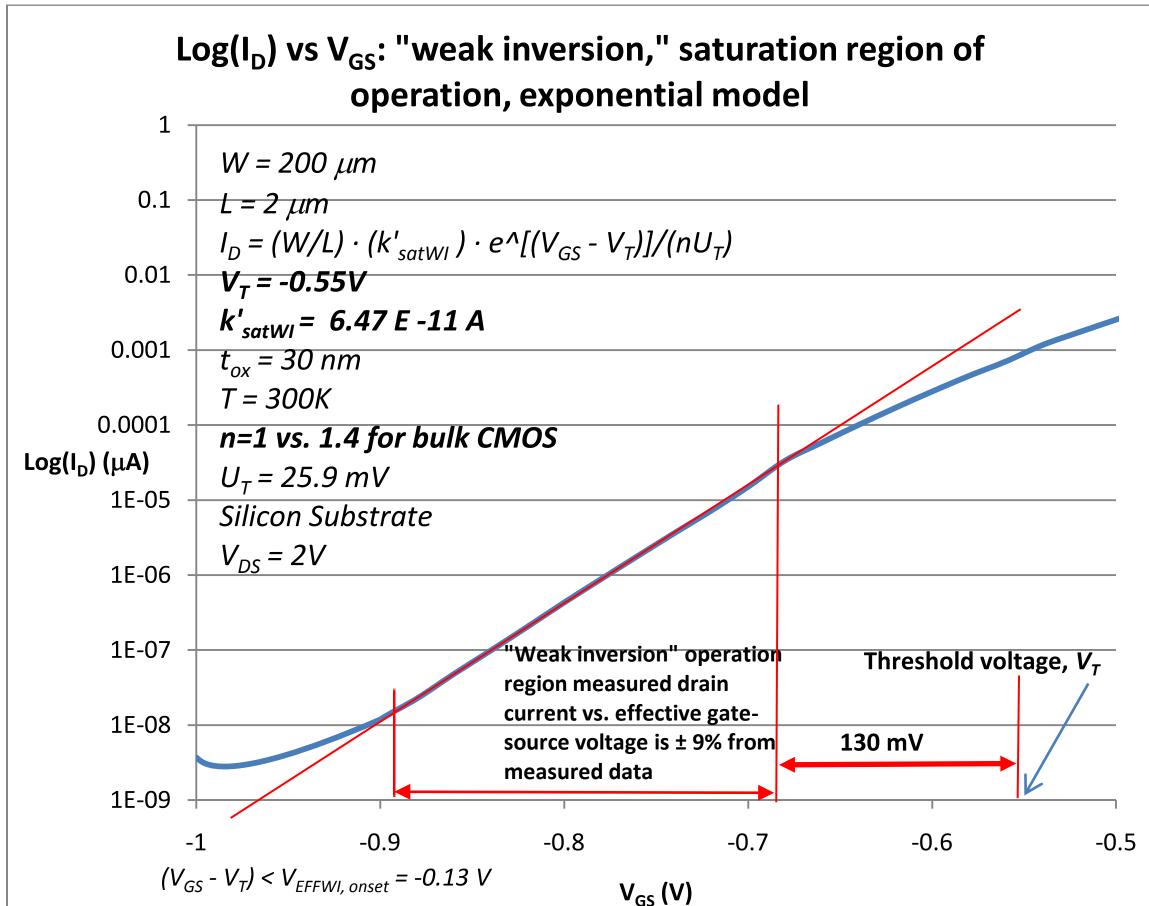

Figure 3.3. Measured and modeled drain current versus gate-source voltage for “weak inversion,” saturation region with V_{DS} = 2 V. Drain current on a log scale reveals fitted exponential performance within ± 9% of measured data.

Figure 3.4 shows drain current from the “weak” to “strong inversion” regions of operation. Interestingly, the “weak inversion” and the “strong inversion” models track measured data within ±1.6% for “strong inversion,” and within ±9% for “weak inversion.” However, between, in “moderate inversion,” both models fail to predict drain current, just as for bulk CMOS.

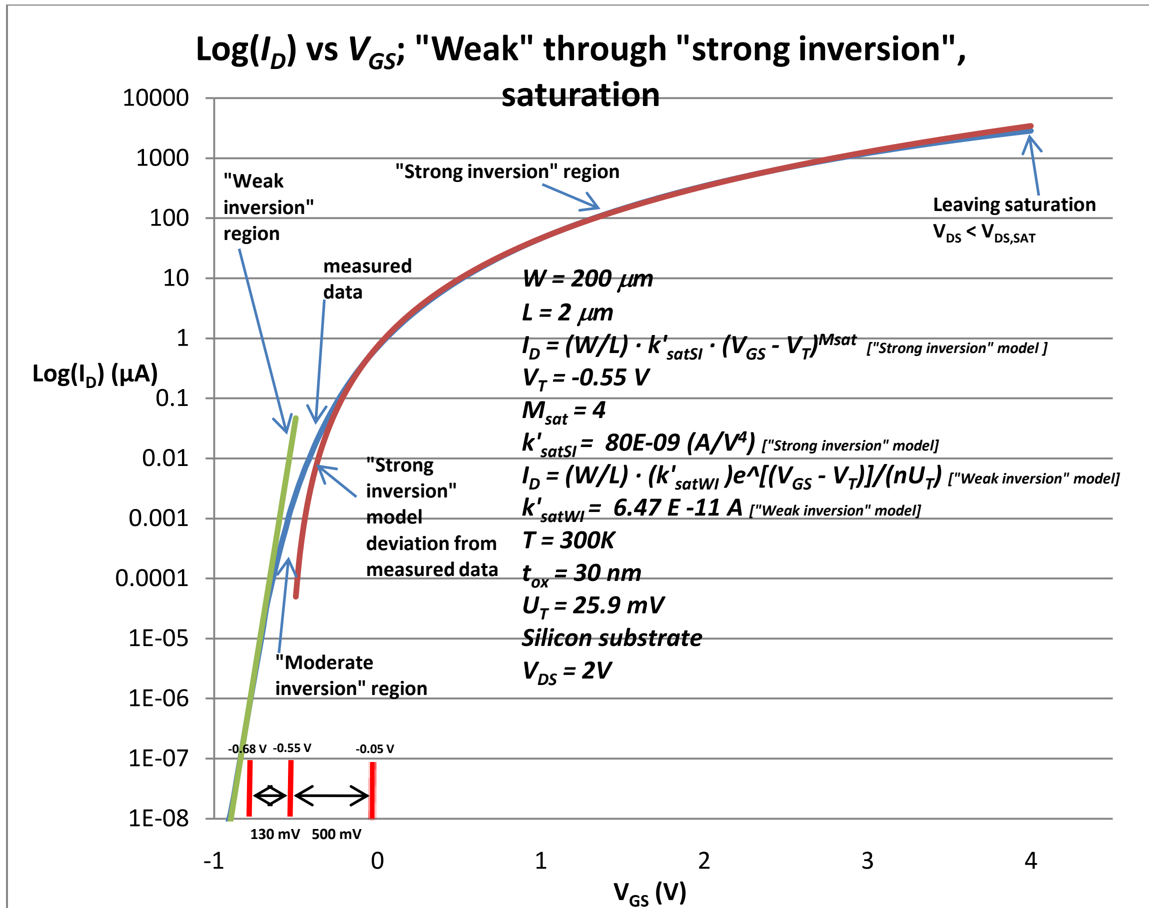

Figure 3.4. Measured and modeled ZnO thin-film FET drain current versus gate-source voltage from "weak" through "strong inversion."

3.1.3 Non-saturation Region Modeling

Equation (3.17) gives the drain current for bulk CMOS strong inversion ($V_{GS} - V_T >$ ~ 0.25 V), non-saturation ($V_{DS} < V_{DS,sat}$) operation [16] as

$$I_D = \mu \cdot C'_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_{GS} - V_T) \tag{3.17}$$

Here the overdrive voltage ($V_{GS} - V_T$) is raised to unity, as compared to being squared for the saturation ($V_{DS} > V_{DS,sat}$) region of operation. When referring back to the generic device equation form of (3.2), for ZnO thin-film FETs. M_{nonsat}, or the drain current power

law exponent for the non-saturation region, is extracted at 2.3, and V_T is extracted at 0.1 V. It is interesting to note that a value of M_{nonsat} = 2.3 gives a good fit, as shown in Figure 3.5, but based on the square-law characteristics of the mobility described in Chapter 2, one would assume that M_{nonsat} = 3. This suggests that more research into the device physics is required for a better understanding of ZnO thin-film FET drain current modeling. For the extraction of M_{nonsat}, shown in Figure 3.5, V_{DS} = 0.1 V, V_{GS} = 1 V to 5 V, and therefore, $V_{DS} \ll V_{DS,SAT}$.

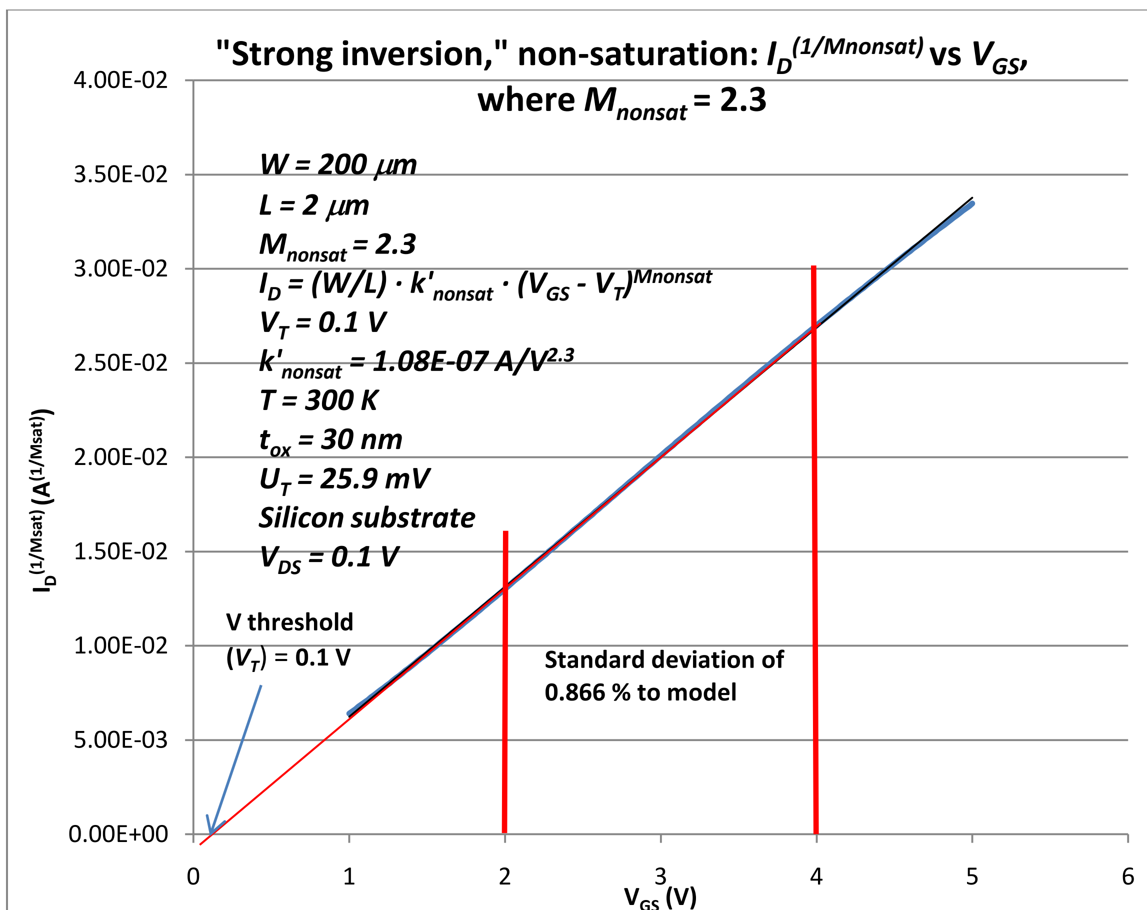

Figure 3.5. Measured and model drain current versus gate-source voltage for non-saturation region of operation with M_{nonsat} = 2.3 and V_{DS} = 0.1V. Curve fit is within ± 0.866% with measured data for V_{GS} = 2 V to 4 V.

3.2 AC Device Modeling

As with all transistors, one important aspect of modeling is the small-signal model. Small-signal analysis allows for gain calculations as well as output impedance calculations, which is very beneficial when doing power transfer efficiency calculations and RF matching.

As with bulk CMOS, in the small-signal model of Figure 3.7, the G, D, and S are correspond to the gate, drain and source, respectively. The transconductance [17], denoted as g_m is calculated for bulk CMOS in strong inversion, saturation as

$$g_m = \frac{2 \cdot I_D}{V_{GS} - V_T} \tag{3.18}$$

For the ZnO thin-film FET, measured data reveals that the transconductance is actually somewhat higher than that predicted by (3.18). Instead of multiplying the drain current by 2, the ZnO thin-film FET model multiplies the drain current by 4 using the extracted value of M_{sat} = 4. The transconductance is repeated from (3.6)

$$g_m = \frac{M_{sat} \cdot I_D}{V_{GS} - V_T} = \frac{4 \cdot I_D}{V_{GS} - V_T} \tag{3.19}$$

Another component is the output resistance of the device, also known as the drain-source resistance r_{ds}. As seen in [18], the output resistance is often modeled using an Early voltage, V_A, and the drain current I_D. This gives [18]

$$r_{ds} = \frac{1}{g_{ds}} = \frac{V_A + V_{DS}}{I_D} \approx \frac{V_A}{I_D} \tag{3.20}$$

Where the Early voltage V_A is represented as the inverse of the channel-length modulation factor λ as

$$V_A = \frac{1}{\lambda} \tag{3.21}$$

A graphical representation of how the Early voltage is extracted from drain current versus V_{DS} curve trace data is shown in Figure 3.6 according to [18]. Using the I_D versus V_{DS} curves of multiple V_{GS} values, a continuation line may be drawn from the saturation region portions of the curve to intersect the x-axis at a point known to be the negative of the Early voltage. The slope of those continuation lines is also known as the output impedance, r_{ds}.

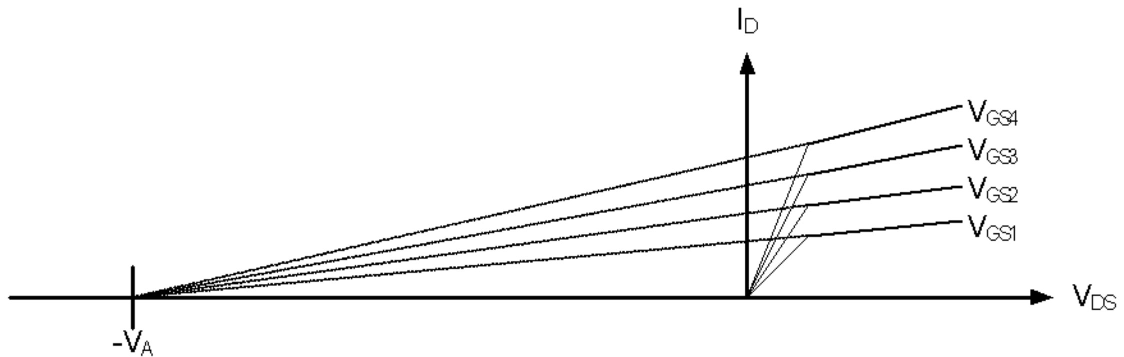

Figure 3.6. The graphical method of extracting the Early voltage.

For the purposes of this dissertation, the Early voltage is extracted to be 20 V for L = 2 μm AFRL devices as referenced from [15].

Another important part of any AC small-signal model is the capacitances associated with the transistor, required to ascertain the frequency response of the device. It also becomes important when preparing for circuit design, which is the purpose of this work.

Figure 3.7 gives a small-signal model for ZnO thin-film FETs. As part of the bottom-gate configuration, a gate-body overlap capacitor is modeled.

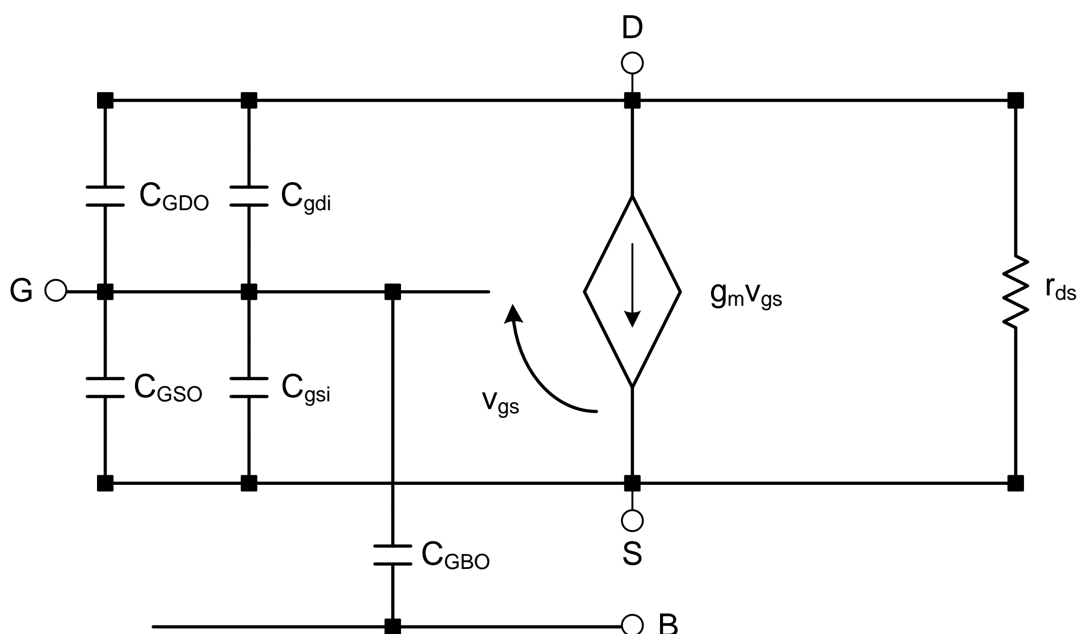

Figure 3.7. Small-signal model for the ZnO thin-film FET including capacitances as adapted from [19, p. 98].

Figure 3.8 gives a picture of where each capacitance forms with each layer of fabrication. The gate-drain intrinsic capacitor, C_{gdi}, is listed, but is considered to be 0 as the model is for saturation conditions where the drain is assumed pinched off.

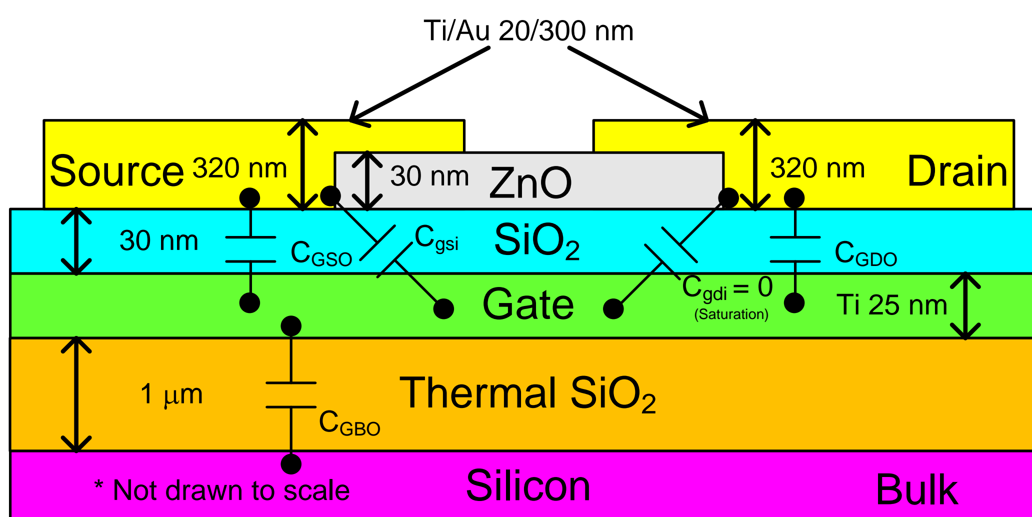

Figure 3.8. Fabrication layers with capacitances drawn for illustration of Figure 3.7 [8].

The first capacitance that is crucial for calculation is known as the gate oxide capacitance per unit area, C'_{ox} [19, p. 41]. C'_{ox} is calculated in (3.22), which includes a convenient expression from [19, p. 41].

$$C'_{ox} = \frac{\varepsilon_{SiO_2}}{t_{ox}} = \frac{34.5\ fF}{\mu m^2}\left(\frac{1\ nm}{30\ nm}\right) = 1.15\ \frac{fF}{\mu m^2} \tag{3.22}$$

Here ε_{SiO_2} is the permittivity of silicon-dioxide which is used as the gate-oxide and t_{ox} is the thickness of the gate oxide, which is 30 nm for the AFRL ZnO thin-film FETs used in this research.

The total gate-oxide capacitance, C_{GOX} is given by

$$C_{GOX} = W \cdot L \cdot C'_{ox} \tag{3.23}$$

Assumptions are made in this modeling that intrinsic capacitance values are similar to that of bulk CMOS operating in strong inversion, saturation. In (3.24), the intrinsic gate-source capacitance is given for a ZnO thin-film FET in "strong inversion," saturation.

$$C_{gsi} \approx \left({}^{2}/_{3}\right) \cdot W \cdot L \cdot C'_{ox} \tag{3.24}$$

The intrinsic gate-drain capacitance is assumed zero due to operation in the saturation region where the drain is pinched off [16]. There is no gate to bulk intrinsic capacitance assumed for the devices.

In (3.25), the gate-drain overlap capacitance is calculated, followed by the gate-source overlap capacitance in (3.26) and the gate-body overlap capacitance in (3.27). The gate-body overlap capacitance is included in this work due to the bottom-gate fabrication shown in Figure 3.8. The overlap capacitances are given by

$$C_{GDO} = A_D \cdot C'_{ox} \tag{3.25}$$

$$C_{GSO} = A_S \cdot C'_{ox} \tag{3.26}$$

$$C_{GBO} = W \cdot L \cdot C'_{oxsub} \tag{3.27}$$

where
$$C'_{oxsub} = \frac{\varepsilon_{SiO_2}}{t_{ox}} = \frac{34.5\ fF}{\mu m^2}\left(\frac{1\ nm}{1000\ nm}\right) = 34.5\ \cdot 10^{-3}\ \frac{fF}{\mu m^2} \tag{3.28}$$

A_D is the area under the drain, A_S is the area under the source, and C'_{oxsub} is the capacitance per unit area of the gate with respect to the substrate. In the calculation of C'_{oxsub} value, an oxide thickness (t_{ox}) of 1 μm or 1000 nm is used as seen in Figure 3.8.

Table 3.1. Example set of ZnO thin-film FET small-signal parameter values.

Transistors	**Symbol**	**Unit**	**Value**
Example	I_D	μA	19.53
Example	V_{GS}	V	0.7
Example	V_T	V	-0.55
Example	V_{EFF}	V	1.25
Example	W	μm	200
Example	L	μm	2
Example	k'	A/V^4	80E-09
Example	n		1
Example	V_A	V	20
Example	g_m	μS	62.5
Example	r_{ds}	MΩ	1.02
Example	t_{ox}	nm	30
Example	t_{oxsub}	nm	1000
Example	C'_{ox}	$fF/\mu m^2$	1.15
Example	C'_{oxsub}	$fF/\mu m^2$	0.035
Example	C_{GOX}	fF	460
Example	C_{gsi}	fF	306.67
Example	C_{GDO}	fF	690
Example	C_{GSO}	fF	690
Example	C_{GBO}	fF	3.45

Table 3.1 gives an example set of values for the small-signal analysis of a ZnO thin-film-FET utilizing the equations for the entire Section 3.2 of this Chapter.

It is important to note that the extrinsic overlap capacitances for this device are actually much larger than the intrinsic capacitances, therefore dominating the frequency response in circuit applications. The drain and source dimensions are 200 µm by 3 µm to give an area of 600 μm^2.

3.3 RF Device Modeling

In preparation for any radio frequency (RF) design, probe testing is typically done on the wafer of the transistors before dicing and packaging. During that wafer probing, scattering parameters (S-parameters) are taken that allow the designer to understand how the device operates at high frequencies (RF frequencies). These scattering parameters are a measurement of how an applied voltage signal is either reflected (S_{11} and S_{22}) or passed through the device (S_{21} and S_{12}). The S_{11} parameter is the ratio of the reflected to incident voltage on port 1 of the device. The S_{22} is the same definition, but on port 2 of the device. The S_{21} parameter is known as the forward gain or ratio of port 2 output voltage to port 1 input voltage. The S_{12} is known as the reverse isolation of the device or ratio of port 1 voltage resulting from an applied voltage on port 2. In most RF devices it is undesirable for the output port to couple a signal to the input port. That is why the S_{12} measurement is made.

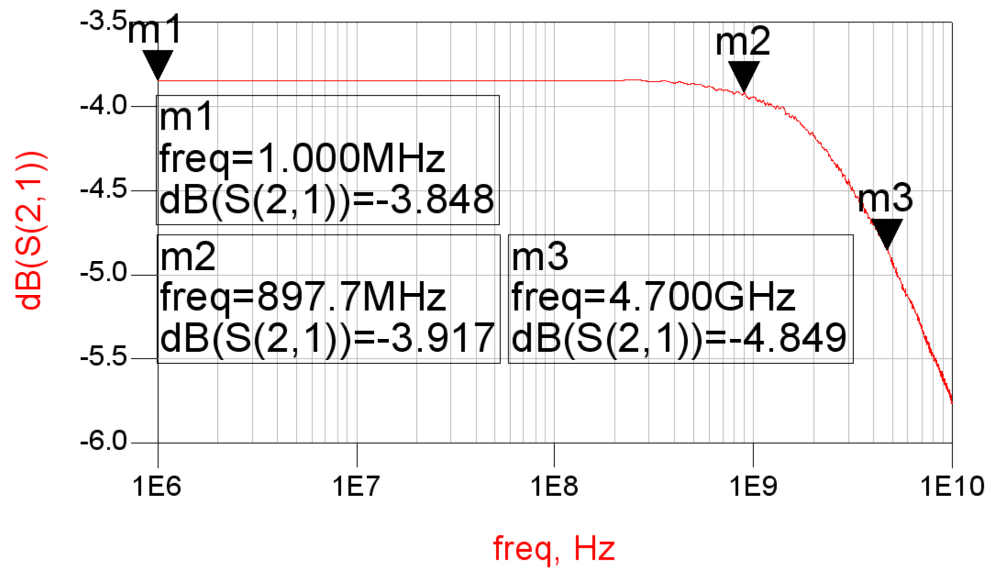

Figure 3.9. Non-matched S_{21} showing the intrinsic gain flatness of the ZnO thin-film FET.

For the AFRL RF ZnO thin-film FETs, a base measurement was taken at the AFRL using a probe station and a vector network analyzer (VNA). For a single transistor, with 50 ohms being presented to the gate and drain of the FET the following S-parameters were taken and used to create an RF model of operation for the device. The AFRL ZnO thin-film FET used for RF S-parameter measurements had a W = 100 µm, L = 1.25 µm, I_D = 33.55 mA, V_{DS} = 13 V, V_{GS} = 9.5 V, and a t_{ox} = 22 nm.

Notice the forward gain shown by S_{21} in Figure 3.9 of the device is less than 0 dB, which likely means that both the input and output of the device prefer to see impedances other than 50 ohms at the present biasing levels. In this case, the device was measured with 50 ohm probes. Three frequencies are marked for example

purposes. A low frequency value of 1 MHz to show the highest gain of the unmatched device, a recorded frequency of 897.7 MHz, a common cellular frequency, and a 1 dB roll-off frequency of 4.7 GHz, which shows the likely limit of usable bandwidth from a theoretical perspective. Once the device is matched for a lower frequency, this frequency will typically provide far more loss from the filtering attributes of the matching network.

A Smith chart is a useful tool for converting values such as voltage reflections, (S_{11} and S_{22}), to real and imaginary impedance values if the characteristic impedance (Z_o) is known. In Figure 3.10, the input impedance is given on a Smith chart by plotting the reflection data and converting to an impedance, Z_o = 50 Ω system at the required frequency of design. The Smith chart is a graphical representation of both real and imaginary impedance values of an RF system. All input impedances are seen to have a large amount of capacitance with a series resistive component. This large capacitive value will require inductance as part of a matching network to convert the input impedance of the ZnO thin-film FET toward the characteristic impedance for maximum power transfer.

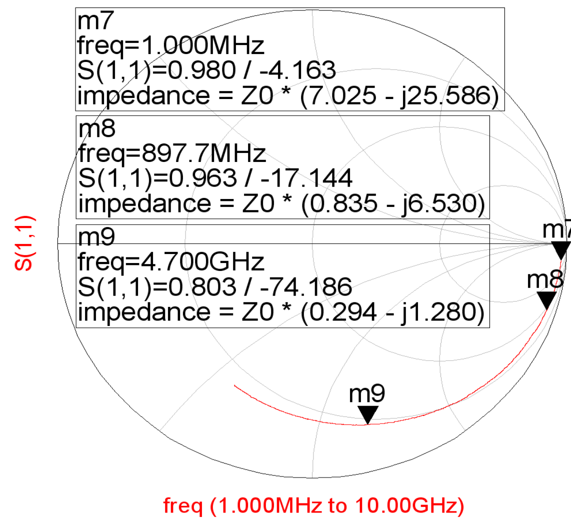

Figure 3.10. Input impedance sweep of the device to show the impedance of the gate at varying frequencies.

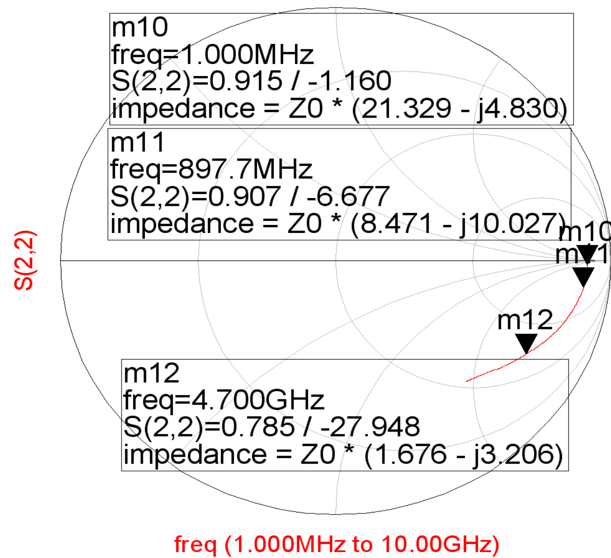

Figure 3.11. Output impedance sweep on the drain of the ZnO thin-film FET to show the drain impedance at given frequencies.

Figure 3.11 shows the output impedance sweep at the drain of the device. This measurement is very useful in determining how a device is matched for different applications. For RF amplifiers such as low noise amplifier’s (LNA’s) or gain blocks operating at very low power, the output is matched to 50 ohms as needed to achieve the proper noise figure or gain. In the case of a power amplifier, however, the output is purposefully matched away from 50 ohms in an attempt to succeed in some tradeoff of efficiency and output power, or in the case of a linear power amplifier, the tradeoff would be linearity and efficiency. In whatever application it may be, the output impedance sweep is instrumental in assisting the RF engineer in the creation of an output matching network to efficiently transfer power to the load.

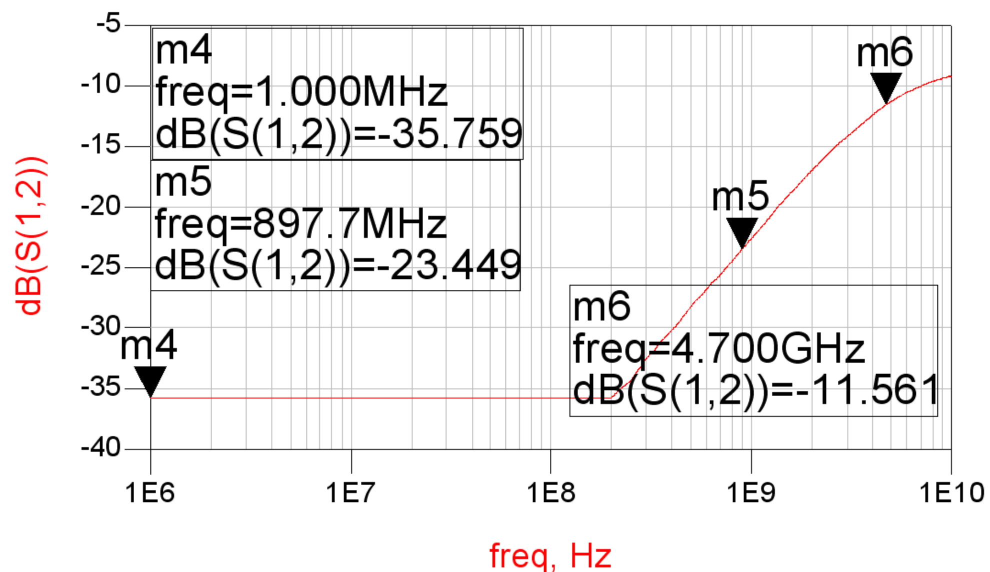

Figure 3.12. S_{12} showing the reverse isolation of the ZnO thin-film FET.

Most RF amplifiers must be designed to attenuate unwanted signals at the output port to the input port. For this reason, the S_{12} plot shown in Figure 3.12 is created to check for any unintended reverse amplification.

From the previous S-parameter measurements from an actual ZnO thin-film FET, a lumped-element RF device model was created using Agilent ADS software. Figure 3.13 shows this model.

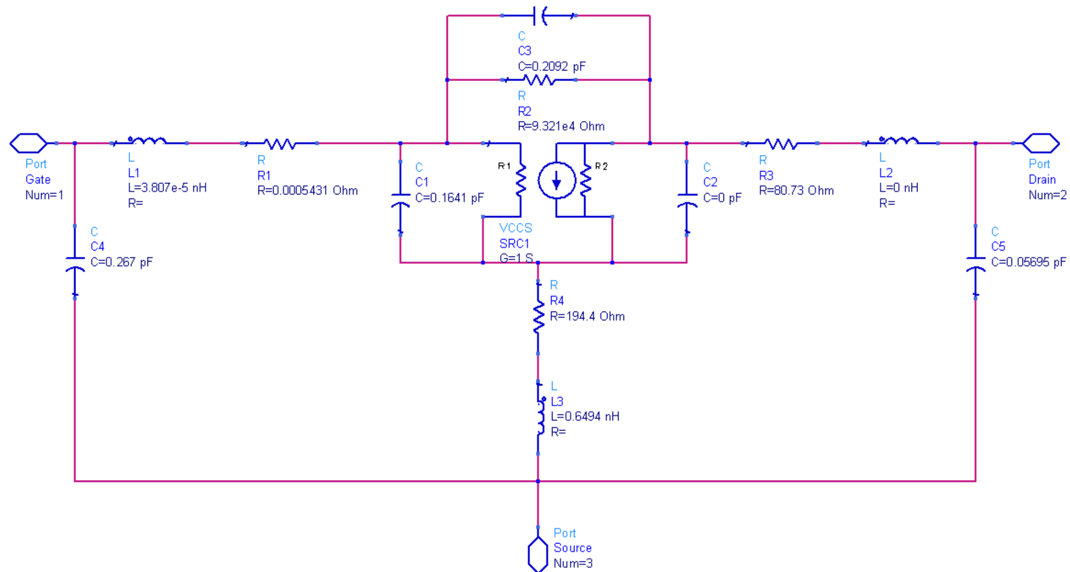

Figure 3.13. Lumped-element RF model for ZnO thin-film FET from S-parameter measurements [2].

CHAPTER 4: DESIGN AND EVALUATION OF A ZNO THIN-FILM FET PIXEL DRIVER

This chapter utilizes the modeling of Chapter 3 to design pixel driver circuits with ZnO thin-film FETs. For the design of the pixel driver circuit, test transistors were laid out separately from the circuit in order to take I-V curves to confirm the models used in the design of the circuit.

4.1 ZnO Thin-Film FET Modeling Extraction

For this AFRL fabrication run, a process shift occurred that causes the previous model parameters used to design the circuits from Chapter 3 to be incorrect for this run. The extracted "strong inversion," saturation threshold voltage shifted to a value of -3.4 V from a previous value of -0.55 V. This shift in V_T has effects on the pixel driver design, and a re-evaluation of the design biasing was performed to achieve the desired current sourcing capabilities.

Figure 4.1 shows how this threshold voltage was extracted as performed in Chapter 3. From this extraction, the threshold voltage is then used to extract the k'_{satSI} constant. It is interesting to note that although a process shift occurred, the M_{sat} value remained 4.

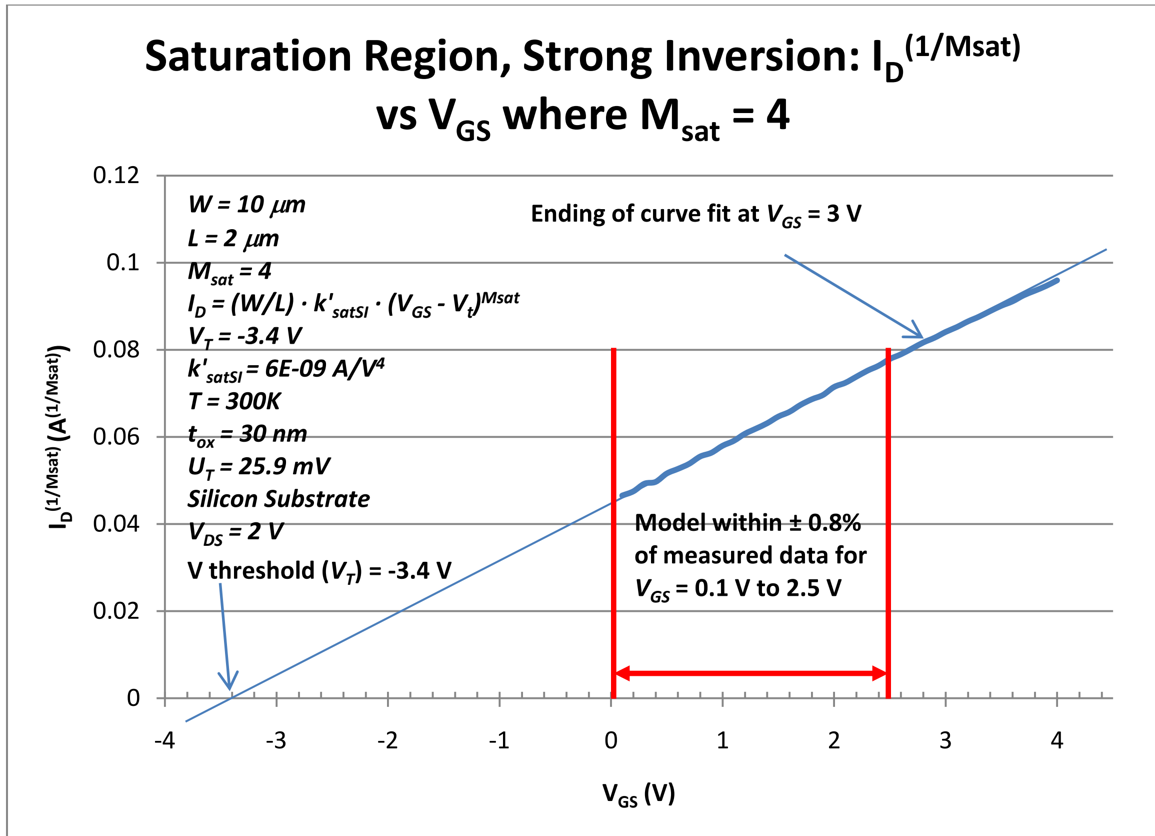

Figure 4.1. Threshold voltage and current constant extraction for ZnO thin-film FETs used in fabricated pixel drivers.

After completion of the V_T and k'_{satSI} extraction in Figure 4.1, a comparison is created in Figure 4.2 that shows the accuracy of the updated model parameters. Also, the deviation from the previous model is plotted to display the V_T shift that occurred. As observed, the extraction of V_T = -3.4 V and k'_{satSI} = 6 x 10^{-9} A/V^4 for the pixel driver run gives considerably different modeling compared to V_T = -0.55 V and k'_{satSI} = 80 x 10^{-9} A/V^4 extracted for a previous run in Figure 3.1. Such a large shift in those two parameters could be a result of damage done to the pixel driver transistors at some time after leaving AFRL.

From the new and complete model of the single ZnO thin-film FET in Figure 4.2, analysis of the pixel driver circuit allows for a closer approximation of the series on resistance in the series switch.

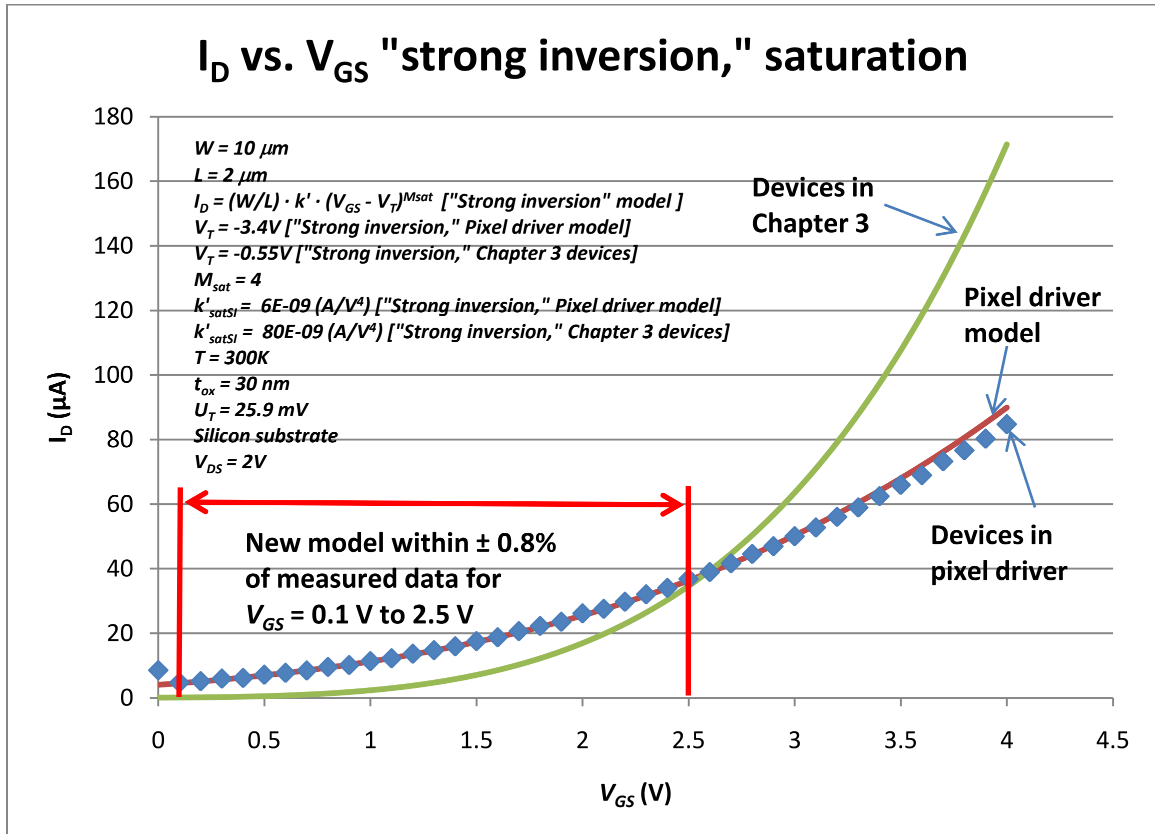

Figure 4.2. Analysis of the deviation from Chapter 3 model parameters and updated model parameters for fabricated ZnO thin-film FET pixel driver.

4.2 Applications of ZnO Thin-Film FET Pixel Drivers

The liquid crystal display (LCD) is a mainstay in both portable and large electronics. This leads to numerous branches of research looking for more efficient and effective ways to increase contrast ratios, pixel brightness, and longevity of displays. These displays are located in certain items such as LCD televisions (TVs) and portable displays for smart phones. Due to the latest advances in light emitting diode (LED)

technology, a new LED known as an organic LED (OLED) is a very popular choice for many manufacturers of displays. However, because of the nature of the OLED, its pixel brightness is directly controlled by the amount of current that is passed through it [20]. This requires a pixel driver transistor that has both the capability to deliver the required current and not block the light being emitted by the display. Currently, amorphous silicon driver circuits are used to provide the current to drive OLED displays. Since amorphous silicon transistors are not transparent, they need to be made small with high voltages to enable the correct amount of current drive [5].

A natural solution for the need of high current and high transparency is the ZnO thin-film FET. The ZnO thin-film FET has high mobility, high transparency in the visible wavelength of light, and most importantly, is very compatible with inexpensive plastic substrates [12]. With the transparent nature of the ZnO thin-film FET, it is possible to use a larger FET than with amorphous silicon transistors to provide the same amount of current drive [5]. This allows for lower voltage rails, which leads to less total power consumption.

4.3 Circuit Description

Two ZnO thin-film FET pixel driver configurations are selected and fabricated. For the purposes of this dissertation, they are named the single-transistor and selectable pixel driver.

The simplest of the two circuit configurations is the single-transistor pixel driver with schematic shown in Figure 4.3. As the name states, the single-transistor pixel driver contains only one ZnO thin-film FET and drives the OLED without additional circuitry.

This is the simplest solution and has the advantage of increased contrast ratio because of the smaller size from fewer transistors in the driver circuit allowing for smaller pixels. It also will have a higher yield than a circuit with more transistors [20].

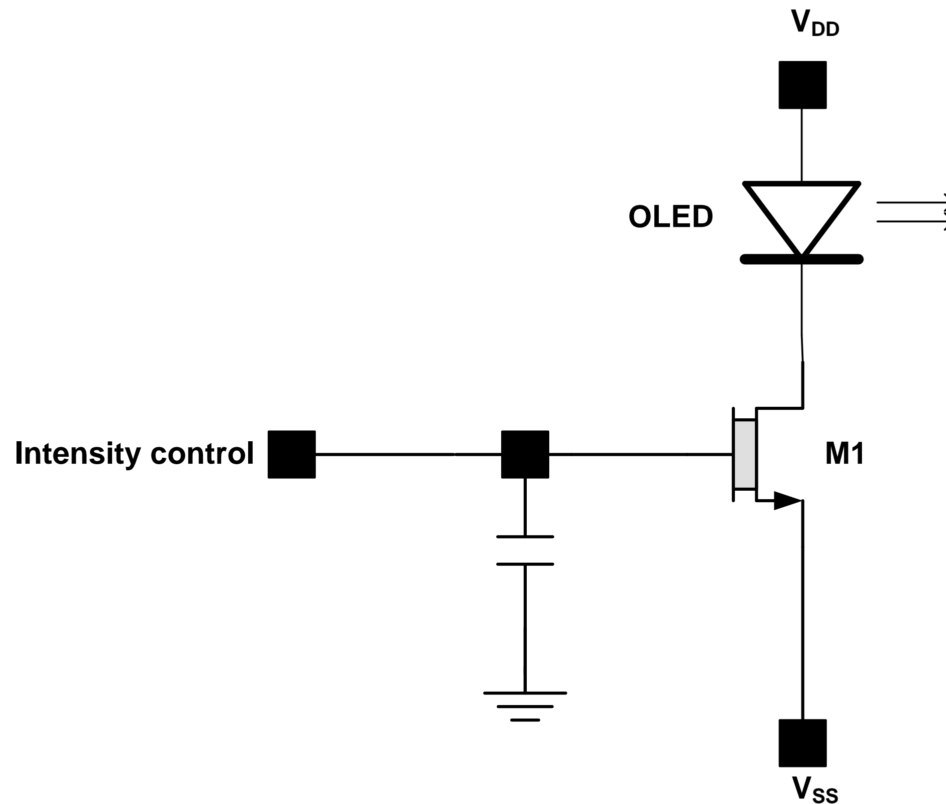

Figure 4.3. Single-transistor ZnO thin-film FET pixel driver schematic.

Slightly more complex is the selectable pixel driver shown in Figure 4.4. The selectable pixel driver has an additional series switch that allows the selection of the pixel driver for such applications as a multiplexed control line scheme as presented in [21].

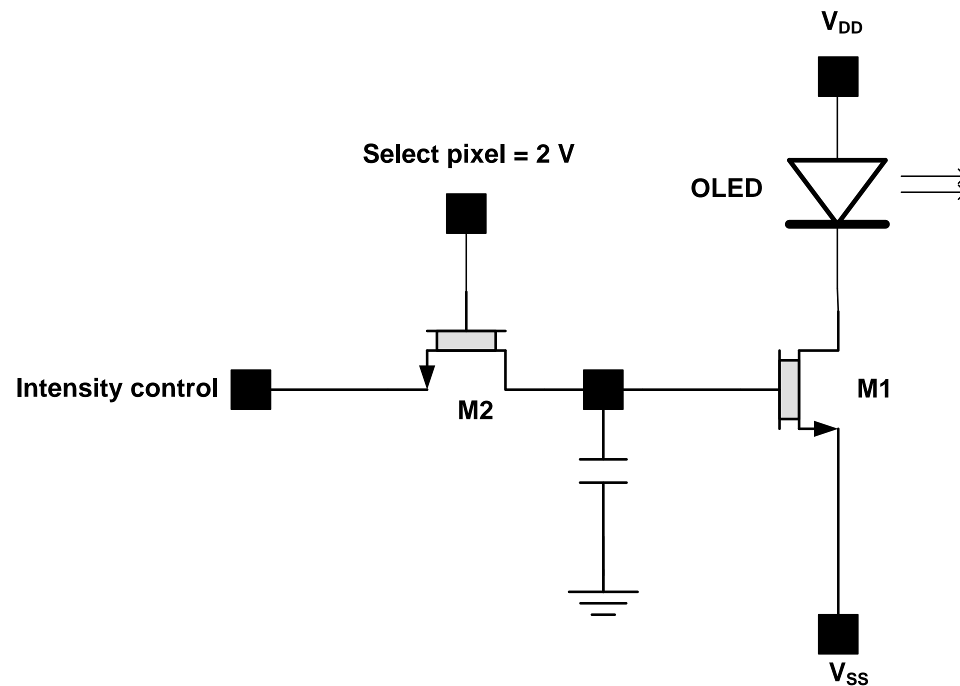

Figure 4.4. Selectable ZnO thin-film FET pixel driver schematic.

For both the single-transistor and selectable pixel driver, a capacitor is used in the end application to hold a charge on the gate of the driver transistor in order to hold the control voltage, (the intensity voltage shown in Figures 4.3 and 4.4) during the frame delay [22].

4.4 Analysis and Design

The design of the single-transistor pixel driver circuit is presented first. The selectable pixel driver is then presented, building upon the single pixel driver design. Using (3.2) to find the drain current, a device size of 10 µm wide by 2 µm long is selected to provide a total gate area of 20 μm^2. As of this writing, the smallest operational ZnO pixel driver transistor gate area is 100 μm^2 [13]. Once the size is selected, proper voltage biasing is required to ensure appropriate current capability to drive the OLED. In this

design, V_{DS} = 2 V and V_{GS} = 2V are used to provide 28 μA to the OLED by using the modeling equations of Chapter 3, with the model parameters extracted in Figure 4.1. The 28 μA value came from the need to supply current to a 20 μm x 20 μm OLED pixel. Since the average current necessary to produce a bright display is approximately 10 mA/cm^2 [20], a steady current of 0.04 μA is required. If it is assumed that there are 400 address lines and only one line is active at any one given time, the current needed is 16 μA (400 · 0.04 μA), to make a pixel shine brightly during the entire duty cycle. Margin is added due to the infancy of this process in case the mobility is less than originally expected. Figure 4.5 gives a schematic diagram of the single transistor pixel driver with bias and sizing details.

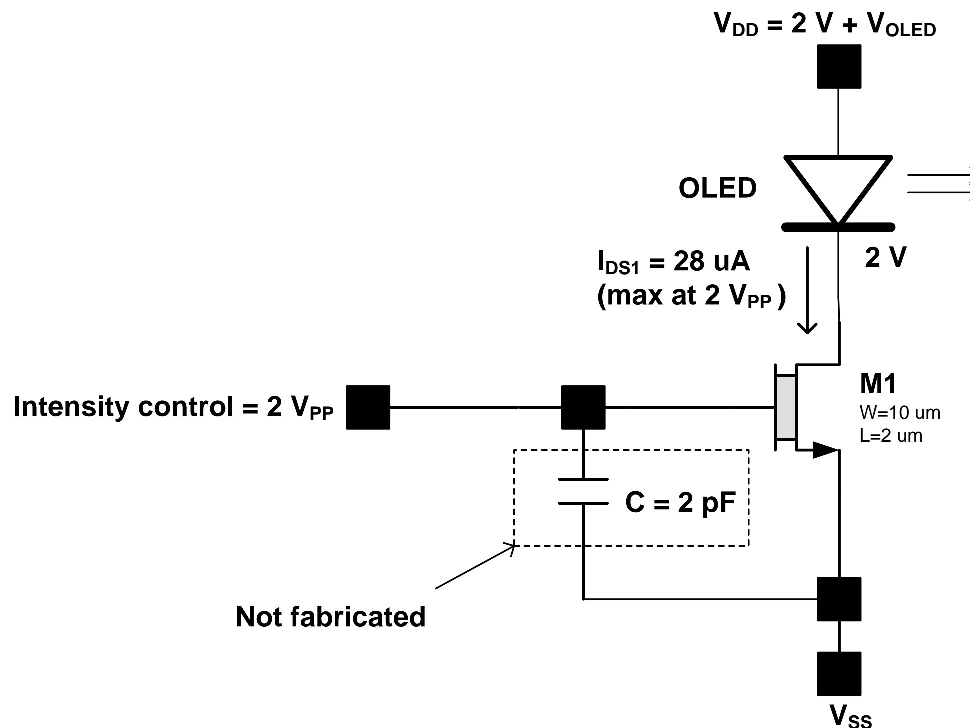

Figure 4.5. Single-transistor ZnO thin-film FET pixel driver designed for a 20 μm x 20 μm OLED pixel.

From the single-pixel design, the selectable pixel driver adds the series ZnO thin-film FET switch that is used for a matrix-style display to select the pixel from a multiplexed controller. The selectable pixel driver schematic is shown in Figure 4.6.

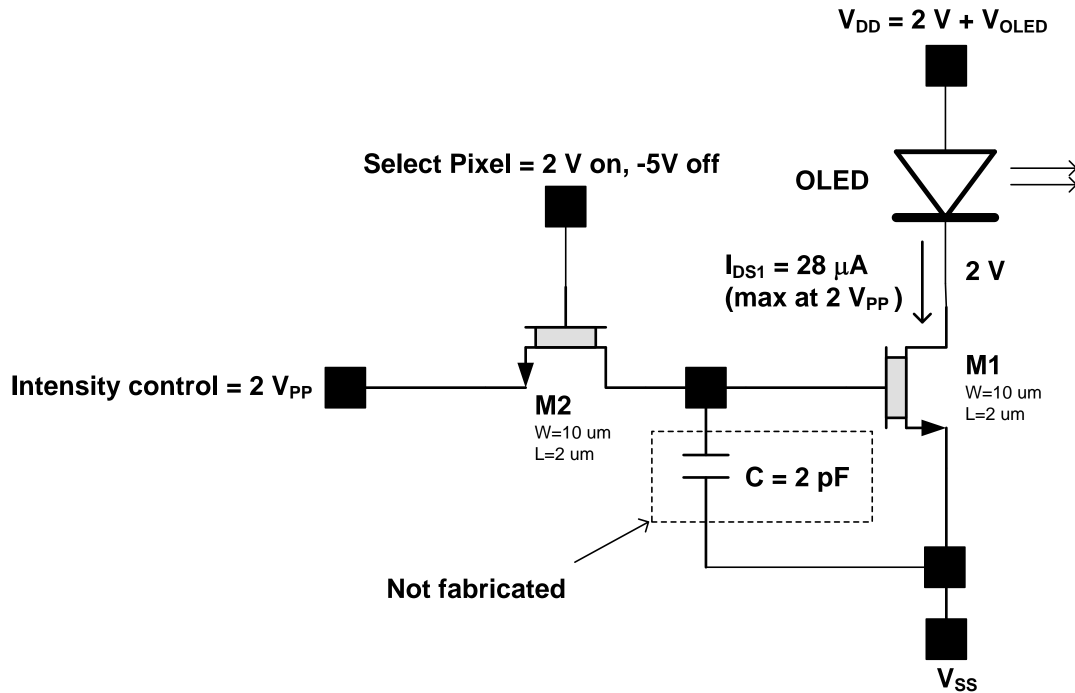

Figure 4.6. Selectable ZnO thin-film FET pixel driver designed for a 20 µm x 20 µm OLED pixel.

In Figure 4.6, the current flow seen through device M2 is assumed to be very small (only M1 gate leakage and capacitor leakage). Therefore the circuits of Figure 4.5 and 4.6 for both circuits perform identically because of identical gate voltage passing to the gate of M1 for both circuits. All calculations take into account that the actual supply voltage will need to be higher than 2 V above the voltage drop across the OLED. For display purposes, the gate capacitor is in the schematic at 2 pF, but it is not fabricated in the prototypes evaluated.

4.5 Design Simulations

Preparing for design simulations, the modeling from Chapter 3 with the modeling parameters of Figure 4.1 are used for both the single-transistor and selectable pixel driver circuits. For each circuit, both a spreadsheet mathematical model and a verilog-A model are created and used to guide the design efforts. The verilog-A model found in Appendix A, is simulated in the Cadence design suite.

For each of the circuits, (3.2) is used with k'_{satSI} = 6E-09 A/V^4 and a threshold voltage V_T = -3.4 V to complete the model variables. As mentioned, the sizing of M1 is W = 10 µm and L = 2 µm as also shown in Figure 4.1.

Figures 4.7 and 4.8 show the simulated drive current performance from a spreadsheet mathematical model and a verilog-A model, respectively, for the single-transistor pixel driver. In Figures 4.7 and 4.8, the ZnO thin-film FET is capable of delivering much more current than the required 28 µA. For both the spreadsheet and verilog-A model, greater than 160 µA is achievable for an intensity voltage of 5 V if required by a specific OLED.

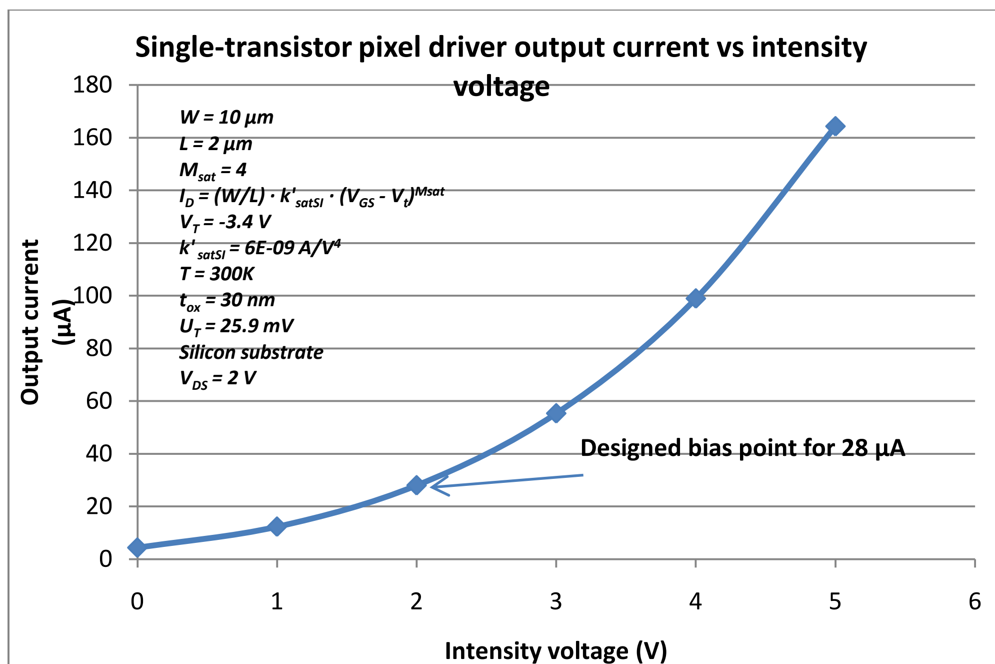

Figure 4.7. Spreadsheet drive current model data for single-transistor ZnO thin-film FET pixel driver design.

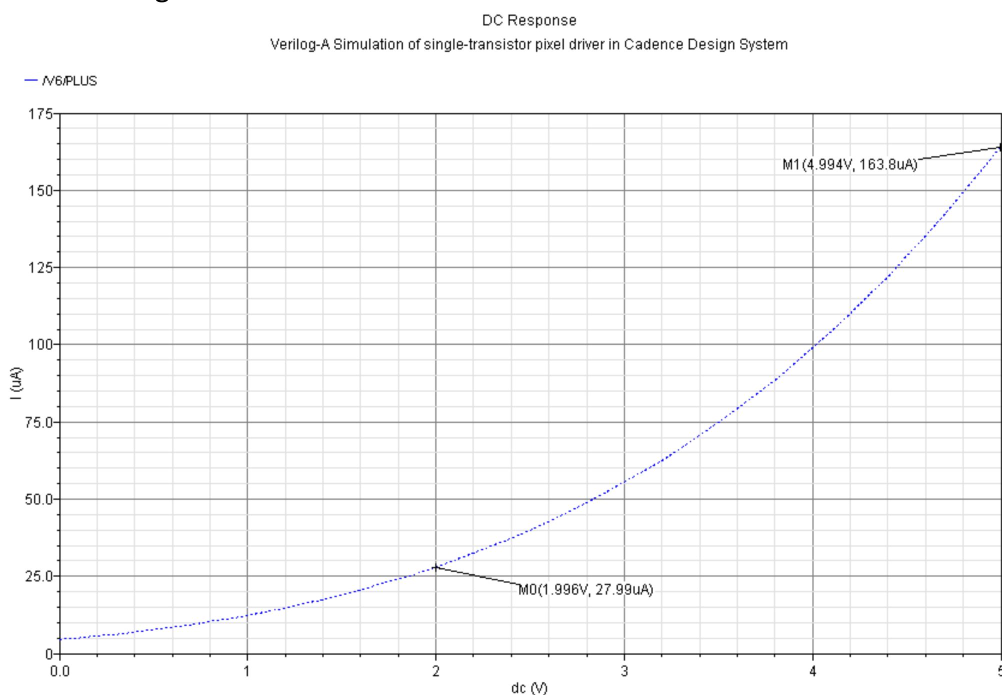

Figure 4.8. Verilog-A drive current model data for single-transistor ZnO thin-film FET pixel driver design.

Figures 4.9 and 4.10 show the spreadsheet and verilog-A drive current model data for the selectable pixel driver circuit design. This model includes the unexpected loss observed with the series select switch (M2) used in a matrix display control configuration. The drain-source (switch) resistance is calculated from the non-saturation drain current given in Figure 3.5 and the operating V_{GS} of 0.4 V for M2 from measured data. A voltage drop across M2 is proof of gate leakage in M1, which may support the assumption of damage in the pixel driver transistors. The switch resistance is

$$r_{ds} = \frac{1}{k'_{nonsat} \cdot \left(\frac{W}{L}\right) \cdot (V_{GS} - V_T)^{m_{nonsat}}} \tag{4.1}$$

$$= \frac{1}{\left(1.08\,E - 07\ (A/V^{2.3})\right) \cdot \left(\frac{10\ \mu m}{2\ \mu m}\right) \cdot (0.4\,V - 0.1V)^{2.3}} = 29.53\ M\Omega$$

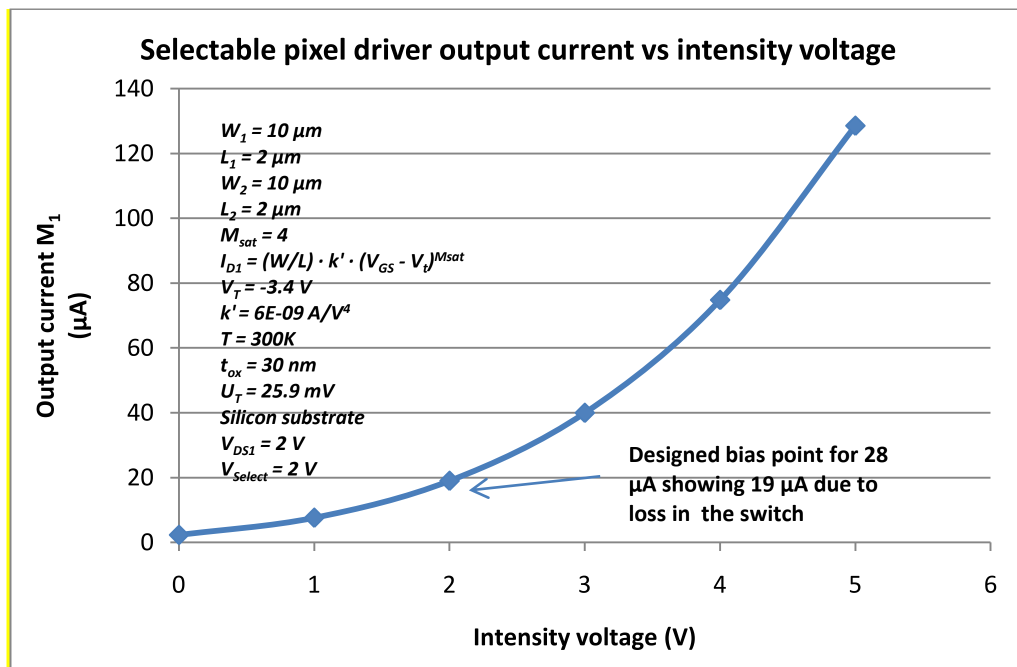

Figure 4.9. Spreadsheet drive current model data for selectable ZnO thin-film FET pixel driver design.

In the spreadsheet model used for Figure 4.9, the observed series switch loss must be included for accuracy. From the single-transistor pixel driver, the output current drops from 28 μA to 19 μA since the intensity voltage is dropped across the series switch. As a result, with the highest intensity voltage of 5V, the selectable pixel driver gives a current output just below 130 μA, which is 30 μA below the single-pixel driver circuit in Figure 4.7. According to the verilog-A simulation results shown in Figure 4.10, at an intensity voltage of 5 V, the switch loss is actually higher resulting in 86 μA, which is far below that of the spreadsheet model across the M2 switch. Experimental measurements showed a voltage drop across the M2 switch indicating current into the gate of M1. This performance is not completely understood and is modeled with a simple resistive divider for the verilog-A model and a 0.4 V drop in the spreadsheet model. The verilog-A model is adjusted with the resistive divider to model measured performance at the designed biasing. If the verilog-A simulations are done with only a series switch, then the performance is identical to the single-transistor verilog-A simulation. No gate leakage is expected since no gate leakage modeling is included in the verilog-A model. As previously mentioned, this measurement of gate leakage may be the result of damage to the device.

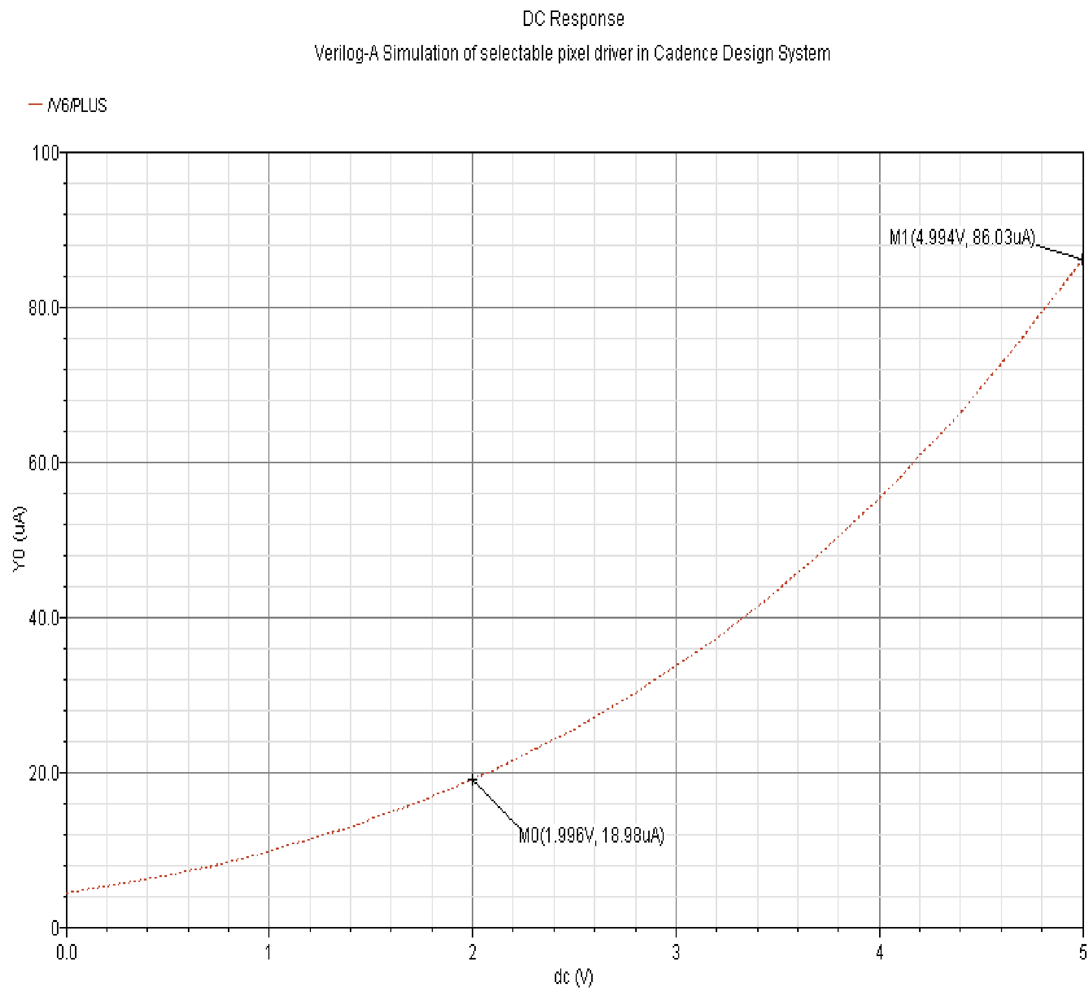

Figure 4.10. Verilog-A drive current model data for selectable ZnO thin-film FET pixel driver design.

4.6 Experimental Evaluation

Photomicrographs of the final fabricated pixel driver circuits are shown in Figures 4.11 and 4.12. Figure 4.11 shows the single-transistor pixel driver, and Figure 4.12 shows the selectable pixel driver. Both were fabricated at the Air Force Research Laboratory (AFRL).

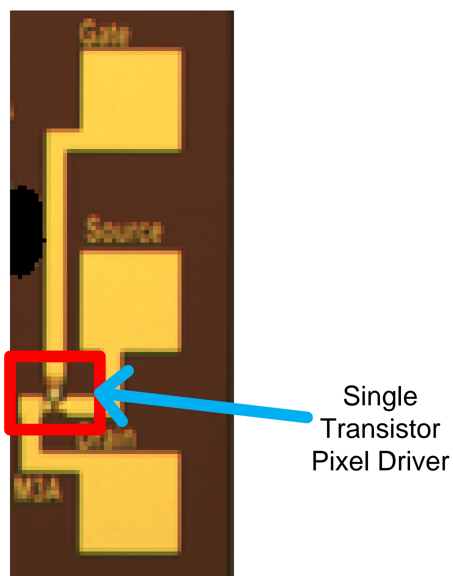

Figure 4.11. Photomicrograph of fabricated single-transistor ZnO thin-film FET pixel driver circuit.

Figure 4.12. Photomicrograph of fabricated selectable ZnO thin-film FET pixel driver circuit.

Testing of each circuit consisted of essentially an identical setup. The only difference being the additional power supply required to drive the pixel select input on the selectable pixel driver circuit. Each test setup is shown in Figures 4.13 and 4.14 for the single transistor pixel driver and selectable pixel driver, respectively.

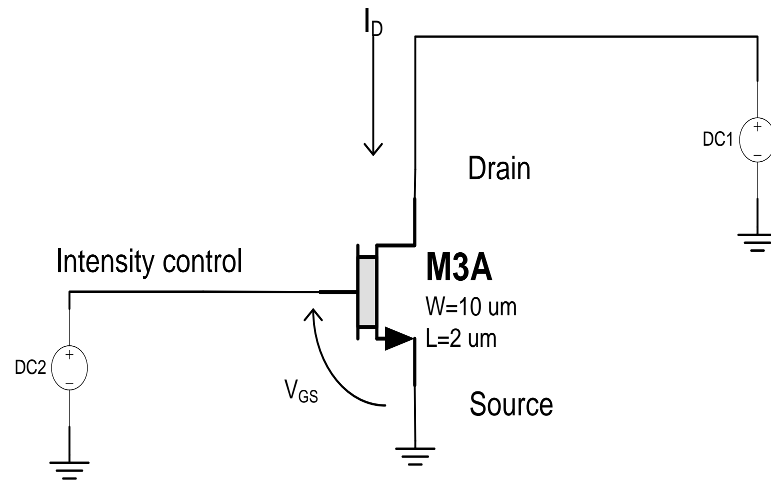

Figure 4.13. Single-transistor ZnO thin-film FET pixel driver test circuit.

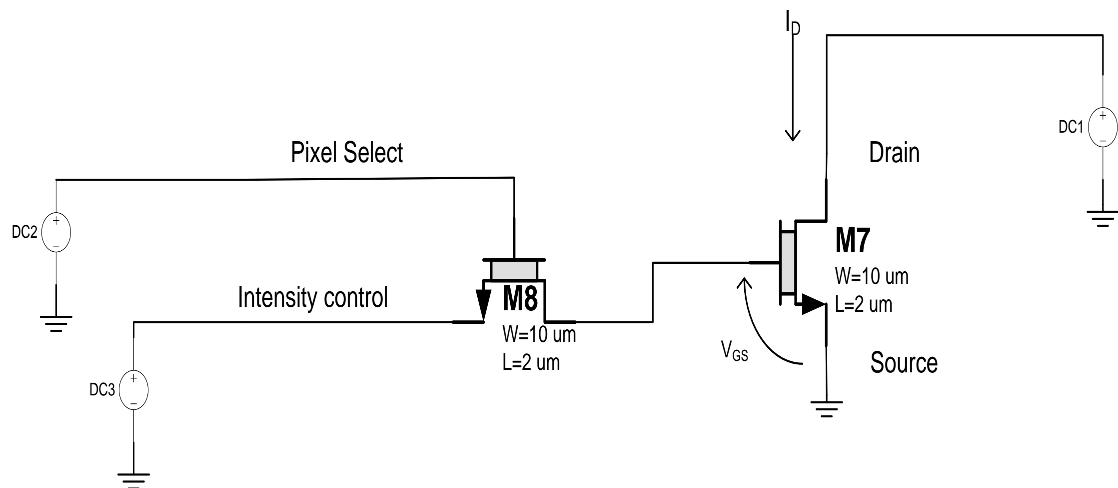

Figure 4.14. Selectable ZnO thin-film FET pixel driver test circuit.

Figures 4.15 and 4.16 show the measured drive current for the ZnO thin-film FET pixel driver circuits.

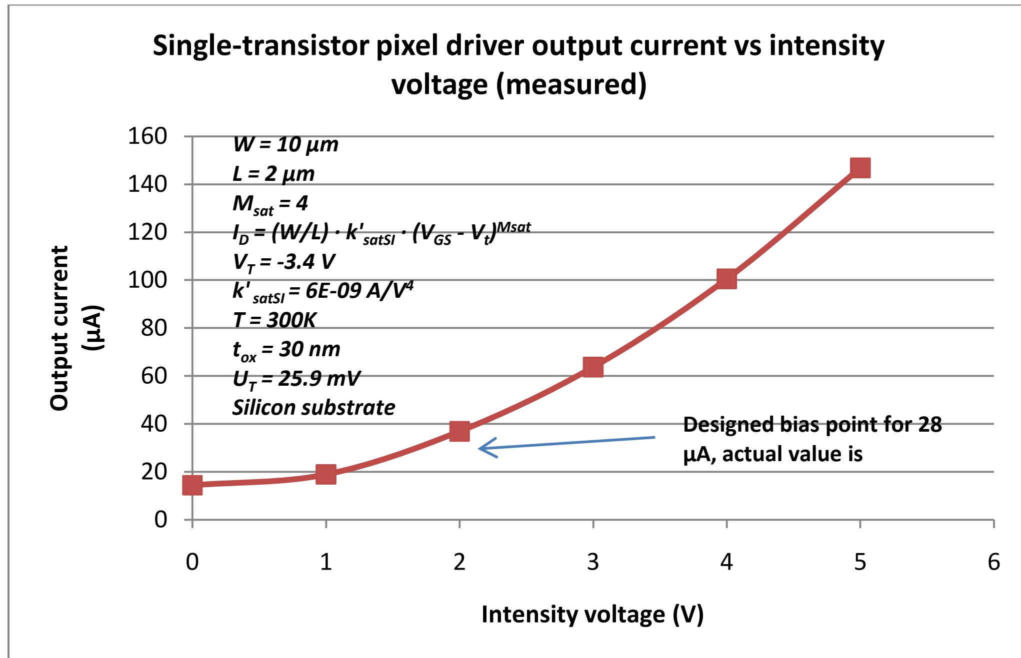

Figure 4.15. Measured data for single-transistor ZnO thin-film FET pixel driver design.

As seen in Figure 4.15, the actual current delivered at the designed operating bias point is 37 µA compared to 28 µA predicted by the modeling in Figure 4.7.

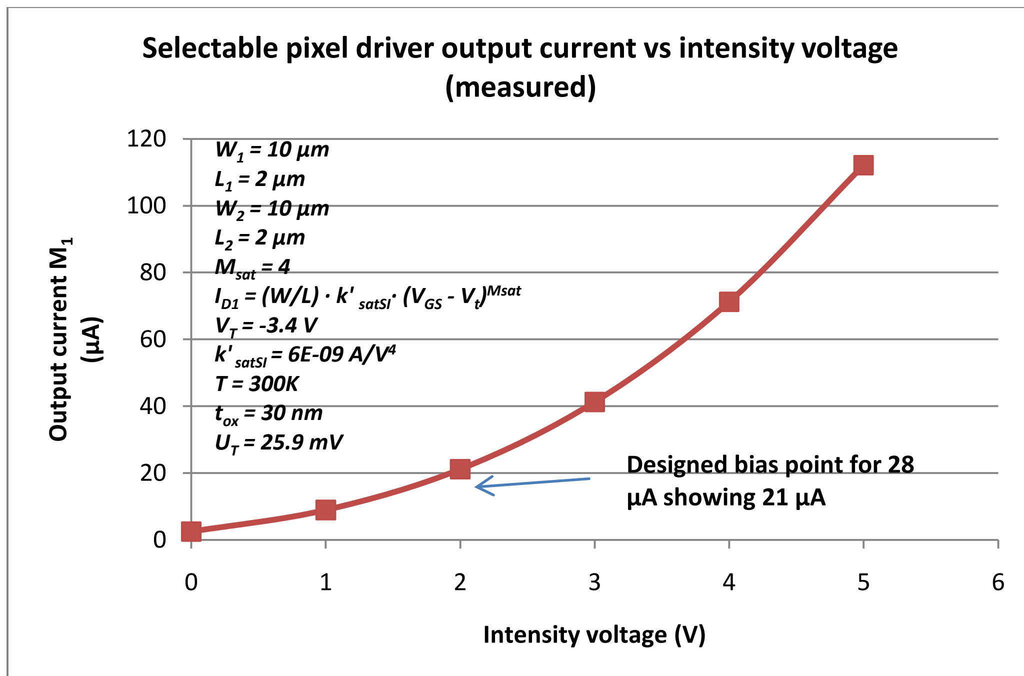

Figure 4.16. Measured data for selectable ZnO thin-film FET pixel driver design.

As with the drive current in Figure 4.15, the measured drive current in Figure 4.16 deviates from the modeled values, but this time in the opposite direction with a lower than expected measured output current of 21 µA compared to 28 µA predicted by the modeling. The measured device current at 21 µA compared to 37 µA for the single-transistor design suggests significant voltage drop across the M2 switch.

4.7 Comparison of Modeled and Measured Results

In this section, both measured and modeled performance of the single-transistor pixel driver and the selectable pixel driver are presented. Figure 4.17 compares the measured and modeled current of the single-transistor pixel driver. In Figure 4.17 the modeled current clearly follows the same shape and trend as the measured current, but the measured current is above the modeled current for intensity voltages below 4 V.

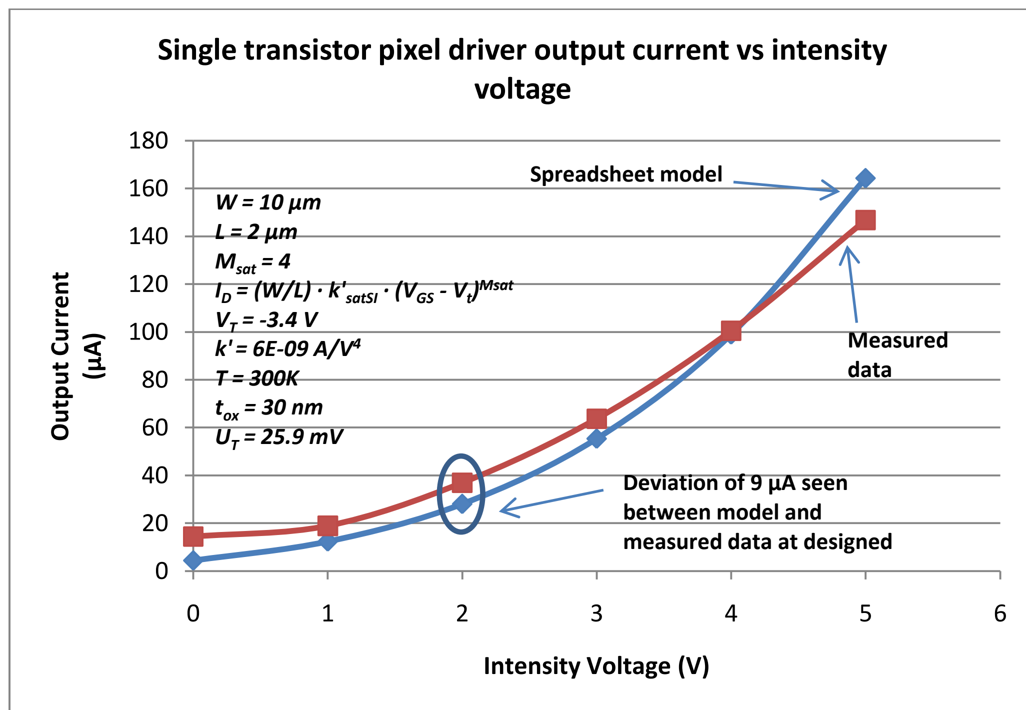

Figure 4.17. Measured and modeled drive current for the single-transistor ZnO thin-film FET pixel driver circuit.

Figure 4.18 compares the measured and modeled current of the selectable pixel driver. Here, the increase in measured current compared to modeled current is partially compensated by switch losses mentioned earlier.

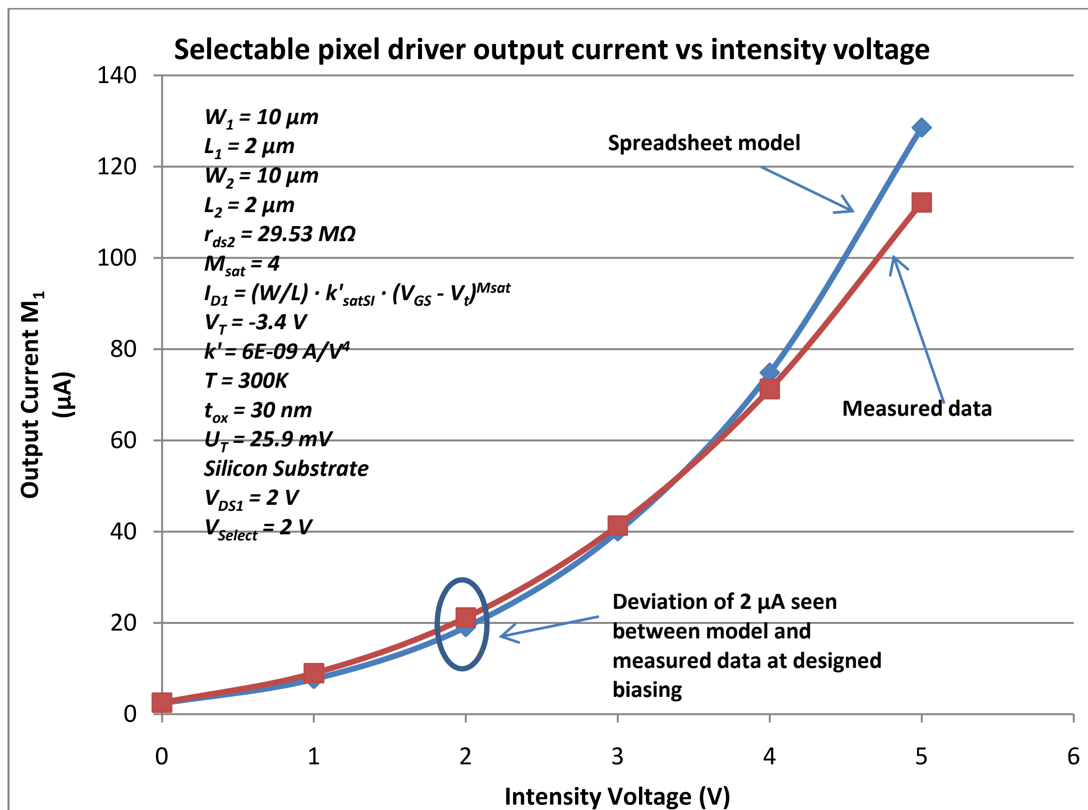

Figure 4.18. Measured and modeled drive current for the selectable ZnO thin-film FET pixel driver circuit.

4.8 Summary and Conclusions

The pixel driver circuit designs are not novel in nature, but do display improved current density over previously published work. Their performance is compared to previously published results in Table 4.1.

Table 4.1. Comparison of current density (I_D/W) between this work and previous publications.

	W	L	V_D	V_{GS}	I_D	Current Density
	(µm)	(µm)	(V)	(V)	(µA)	(µA/µm)
Single transistor pixel driver "this work"	10	2	2	2	37	3.7
Selectable pixel driver "this work"	10	2	2	2	21	2.1
D. Redinger, et. al. [5]	1000	10	5	??	5	0.005
T. Hirao, et. al. [13]	10	10	10	40	129	12.9
Single transistor pixel driver (max) "this work"	10	2	2	5	145	14.5

Note that the pixel drivers presented here achieve comparable current density as reported in [13], but at V_{GS} = 5 V compared to V_{GS} = 40 V in [13]. One point that requires emphasis is that the measured pixel driver circuits were measured with a much smaller k'_{satSI} (13.3 times smaller) than their predecessors measured at the AFRL in Chapter 3. However, the V_T is also shifted to a -3.4 V from a 0.5 V expectation during design. The parameter changes could translate into even higher current density if fabricated as designed. The change in current density is shown in

$$Current\ density\ change = \left(\frac{V_{GS(pixel)} - V_{T(pixel)}}{V_{GS(AFRL)} - V_{T(AFRL)}}\right)^4 \cdot \left(\frac{k'_{satSI(pixel)}}{k'_{satSI(AFRL)}}\right) \tag{4.2}$$

$$= \left(\frac{5\ V - (-3.4\ V)}{5\ V - 0.5}\right)^4 \cdot \left(\frac{6\ x\ 10^{-9}\ A/V^4}{80\ x\ 10^{-9}\ A/V^4}\right) = \ 9\%\ change$$

which results in an expected 9% increase in current density if fabricated as designed. Because of the measured M1 gate leakage, threshold voltage shift, and k'_{satSI} shift, a second fabrication is planned. The second fabrication will further investigate the current density of the ZnO thin film FET pixel driver circuits.

In conclusion, two separate pixel driver circuits using ZnO thin-film FETs were designed, fabricated, and evaluated show an appropriate application for the technology. The ZnO thin-film FET is shown to provide an appropriate amount of current for an OLED or other display pixel for use in TV displays and portable hand-held device displays. In the future, with more stable processes, ZnO thin-film FETs should be replacements for the amorphous silicon thin-film transistors as display drivers for the information and entertainment display markets.

CHAPTER 5: DESIGN OF A ZNO THIN-FILM FET ANALOG AMPLIFIER

In this chapter, an analog amplifier is designed to demonstrate the amplification capabilities of an all-NFET amplifier circuit made with ZnO thin-film FETs. This design is calculated based upon the modeling work completed in Chapter 3. The capacitive modeling work is used to simulate frequency response of the ZnO thin-film FET analog amplifier. The initial amplifier design was done by advisor, Dr. David Binkley.

5.1 Circuit Description and Transistor Parameters

This section describes the analog amplifier architecture and gives some insight on the design process. Figure 5.1 shows the all-NFET analog amplifier design used for this research. The two active load transistors, M3 and M4, are wired with a diode connection in order to maintain saturation operation, where $V_{DS} = V_{GS} > V_{DS,sat}$. The differential pair, M1 and M2, is biased to maintain a certain level of transconductance for a designed small-signal gain. The current mirror, M5 and M6, is set for a 1 to 1 ratio, for easier fabrication and measurement. Also, with a 1 to 1 ratio in the current source, $I_{BIAS} = I_{DSS}$, and $I_{DSS} = I_{DS1} + I_{DS2}$.

The entire circuit is designed for fully differential operation and dual rail voltages, $V_{DD} = -V_{SS}$ for less biasing circuitry on the input gates of the differential pair. The ground or 0 V bias voltage on the input differential pair allows for easy measurements.

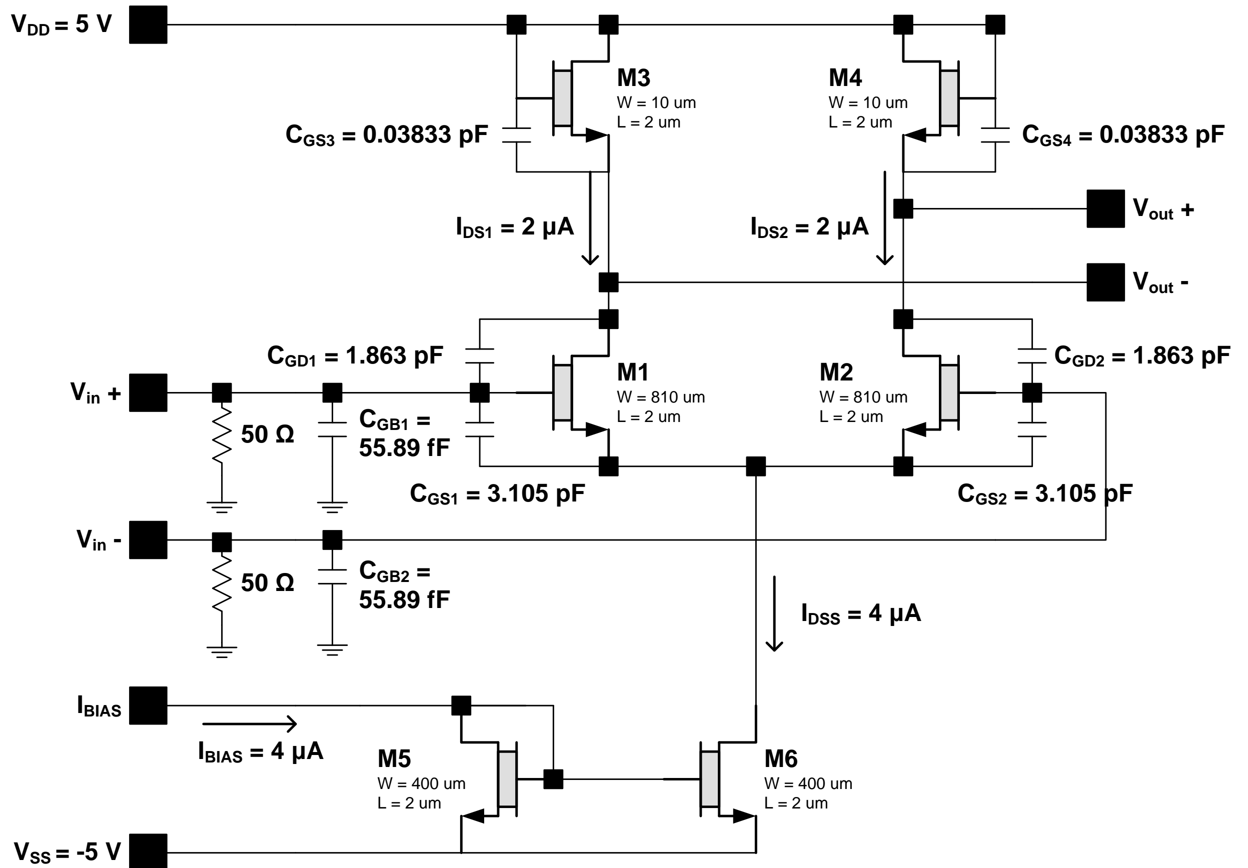

Figure 5.1. Schematic of ZnO thin-film FET analog amplifier.

In Figure 5.1, ZnO thin-film FET sizing, currents, and capacitances are given for the amplifier. Section 5.2 will describe the entire design process including design equations and assumptions made for a robust design. This design process will include sizing and calculations.

Tables 5.1, 5.2, and 5.3 give the calculated transistor parameters for the ZnO thin-film FET analog amplifier shown in Figure 5.1. The k'_{satSI} extracted from Figure 3.1 is used for all design calculations.

Table 5.1. Differential input pair M1 and M2 transistor parameters for ZnO thin-film FET analog amplifier.

Transistors	**Symbol**	**Unit**	**Value**
M1, M2	I_D	µA	2
M1, M2	V_{GS}	V	1.45
M1, M2	V_T	V	0.5*
M1, M2	V_{EFF}	V	0.95
M1, M2	W	µm	810
M1, M2	L	µm	2
M1, M2	k'_{satSI}	A/V^4	80E-09**
M1, M2	n		1
M1, M2	V_A	V	20
M1, M2	g_m	µS	16
M1, M2	r_{ds}	MΩ	10
M1, M2	t_{ox}	nm	30
M1, M2	t_{oxsub}	nm	1000
M1, M2	C'_{ox}	$fF/\mu m^2$	1.15
M1, M2	C'_{oxsub}	$fF/\mu m^2$	0.035
M1, M2	C_{GOX}	fF	1863
M1, M2	C_{gsi}	fF	1242
M1, M2	C_{GDO}	fF	1863
M1, M2	C_{GSO}	fF	1863
M1, M2	C_{GBO}	fF	55.89
M1, M2	C_{GD}	pF	1.86
M1, M2	C_{GS}	pF	3.11

* Actual V_T when fabricated was -3.4 V.

** Actual k'_{satSI} when fabricated was 6 x 10^{-9} A/V^4.

Table 5.2. Diode-connected active loads M3 and M4 transistor parameters for ZnO thin-film FET analog amplifier.

Transistors	Symbol	Unit	Value
M3, M4	I_D	μA	2
M3, M4	V_{GS}	V	3.36
M3, M4	V_T	V	0.5*
M3, M4	V_{EFF}	V	2.86
M3, M4	W	μm	10
M3, M4	L	μm	2
M3, M4	k'_{satSI}	A/V^4	80E-09**
M3, M4	n		1
M3, M4	V_A	V	20
M3, M4	g_m	μS	5.3333
M3, M4	r_{ds}	MΩ	10
M3, M4	t_{ox}	nm	30
M3, M4	t_{oxsub}	nm	1000
M3, M4	C'_{ox}	fF/μm^2	1.15
M3, M4	C'_{oxsub}	fF/μm^2	0.035
M3, M4	C_{GOX}	fF	23
M3, M4	C_{gsi}	fF	15.33
M3, M4	C_{GDO}	fF	23
M3, M4	C_{GSO}	fF	23
M3, M4	C_{GBO}	fF	0.69
M3, M4	C_{GD}	pF	0.023
M3, M4	C_{GS}	pF	0.038

* Actual V_T when fabricated was -3.4 V.

** Actual k'_{satSI} when fabricated was 6×10^{-9} A/V^4.

Tables 5.1, 5.2, and 5.3 all include a unitless value *n* known as the substrate factor. *n* is near the ideal value of 1, which is linked to the “weak inversion” slope shown

in Figure 3.3 for the ZnO thin-film FETs indicating little substrate effect. n is also used in various other models such as the EKV model used for MOSFETs [19, p. 41].

Table 5.3. Current mirror M5 and M6 transistor parameters for ZnO thin-film FET analog amplifier.

Transistors	Symbol	Unit	Value
M5, M6	I_D	µA	4
M5, M6	V_{GS}	V	1.85
M5, M6	V_T	V	0.5*
M5, M6	V_{EFF}	V	1.35
M5, M6	W	µm	400
M5, M6	L	µm	2
M5, M6	k'_{satSI}	A/V^4	80E-09**
M5, M6	n		1
M5, M6	V_A	V	20
M5, M6	g_m	µS	22.86
M5, M6	r_{ds}	MΩ	5
M5, M6	t_{ox}	nm	30
M5, M6	t_{oxsub}	nm	1000
M5, M6	C'_{ox}	$fF/\mu m^2$	1.15
M5, M6	C'_{oxsub}	$fF/\mu m^2$	0.035
M5, M6	C_{GOX}	fF	920
M5, M6	C_{gsi}	fF	613.33
M5, M6	C_{GDO}	fF	920
M5, M6	C_{GSO}	fF	920
M5, M6	C_{GBO}	fF	27.6
M5, M6	C_{GD}	pF	0.92
M5, M6	C_{GS}	pF	1.53

* Actual V_T when fabricated was -3.4 V.

** Actual k'_{satSI} when fabricated was 6×10^{-9} A/V^4.

5.2 Analysis and Design

When designing an analog amplifier, certain initial design decisions are made. Performance aspects such as current consumption, gain, and transistor sizing are typically the first decisions made.

For current consumption, 2 µA per differential half-circuit was selected. The differential half circuit current causes the entire ZnO thin-film FET analog amplifier to draw a total of 8 µA with 4 µA for the differential pair circuitry and 4 µA for the current mirror bias reference current. The current mirror bias reference current draws 4 µA due to the 1 to 1 ratio of the current mirror.

Next, in the design decision-making process is selecting the gain. Based on [23], the voltage gain of an all-NFET analog amplifier having diode-connected loads is low but well controlled due to the low output resistance presented by the loads. As such, a gain of 3 V/V was chosen since the ratio of transconductances of *M1* to *M3* will permit this gain.

The final step in any analog amplifier design is the sizing of the transistors. This was done following circuit analysis of the amplifier. Referencing Figure 5.1, the differential gain relationship is given in (5.1) and shows the differential voltage gain for the amplifier is

$$A_V = \frac{g_{m1}}{g_{m3} + g_{ds1} + g_{ds3}} \cong \frac{g_{m1}}{g_{m3}} \qquad (5.1)$$

Since $g_{ds1} \ll g_{m3}$ and $g_{ds3} \ll g_{m3}$, (5.1) allows for a simplified gain equation. From (3.6), the transistor transconductances are given by

$$g_{m1} = \frac{M_{sat} \cdot I_{D1}}{V_{EFF1}} = \frac{4 \cdot 2\ \mu A}{0.95\ V} = 7.07\ \mu S \tag{5.2}$$

$$g_{m3} = \frac{M_{sat} \cdot I_{D3}}{V_{EFF3}} = \frac{4 \cdot 2\ \mu A}{2.85\ V} = 2.8\ \mu S \tag{5.3}$$

where $M_{sat} = 4$ is the power-law factor extracted in Figure 3.1 for ZnO thin-film FETs. The gate-source overdrive voltage is $V_{EFF} = V_{GS} - V_T$. Substituting (5.2) and (5.3) into (5.1) reveals the final differential voltage gain equation used for design of the ZnO thin-film FET analog amplifier as

$$A_V \approx \frac{V_{EFF3}}{V_{EFF1}} \tag{5.4}$$

The approximate voltage gain (it is approximate because g_{ds1} and g_{ds3} have been neglected) is set by the ratio of transconductances or V_{EFF} voltages as

$$A_V \approx \frac{g_{m1}}{g_{m3}} = \frac{V_{EFF3}}{V_{EFF1}} = \frac{2.85\ V}{0.95\ V} = 3\ V/V \tag{5.5}$$

From (3.2), the transistor shape factor is

$$\frac{W}{L} = \frac{I_D}{k'_{satSI} \cdot (V_{EFF})^{M_{sat}}} \tag{5.6}$$

For equal I_D, k'_{satSI}, and $M_{sat} = 4$ values, this gives

$$\frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1} = \left(\frac{V_{EFF1}}{V_{EFF3}}\right)^{M_{sat}} = \left(\frac{0.95}{2.85}\right)^4 = \frac{1}{81} \tag{5.7}$$

Equation (5.7) describes the ratio of shape factors (*W*/*L*) for transistors M1 and M3 in order to obtain the desired V_{EFF} voltages. Transistor M1 will have a shape factor 81 times larger than that of M3 to obtain the desired V_{EFF} values and voltage gain of 3 V/V.

Assuming that the smallest transistor capable of fabrication is a 10 µm/2 µm (*W*/*L*) device, then M3 is sized at 10 µm/2 µm. Multiplying M3's width by the scaling factor of 81, M1 is then sized at 810 µm/2 µm device.

Solving equation (3.2) for the M5 and M6 current mirror V_{EFF5} gives

$$V_{EFF5} = \left[\frac{I_{D5}}{k' \cdot \left(\frac{W}{L}\right)_5}\right]^{\left(\frac{1}{M_{sat}}\right)} = 1.35\ V \tag{5.8}$$

Given that the sizing for M5 and M6 is 400 µm/2 µm, chosen at about one-half the shape factor of M1 and M2, and the drain current is 4 µA, V_{EFF5} is calculated at 1.35 V. For the intended M1, M2 threshold voltage of 0.5 V, $V_{GS5} = V_{T5} + V_{EFF5}$ = 0.5 V +1.35 V = 1.85 V.

5.3 Design Simulations

Simulation in the Cadence design suite using the behavioral model developed in Section 3.1 was attempted. However, due to the inability of the Cadence design suite used to converge with more than one verilog-A model in a given schematic, the DC

biasing op points were incorrect. It was then not possible to perform computer simulations for the amplifier.

5.4 Summary and Conclusions

In conclusion, a ZnO thin-film FET analog amplifier was designed having a voltage gain of 3 V/V. A threshold voltage of 0.5 V was expected, and a positive threshold voltage is required to keep the M3 and M4 diode-connected active loads in saturation. Unfortunately, as described in section 4.1, the threshold voltage for the AFRL prototypes was incorrect at V_T = -3.4 V. This rendered the M3 and M4 diode-connected loads inoperable. However, because of the good fit of "strong inversion," saturation drain current modeling described in Section 3.1, there is considerable confidence it is very likely the amplifier will work as designed with a correct, positive threshold voltage. A second fabrication of the amplifier is planned for the future.

CHAPTER 6: DESIGN OF A ZNO THIN-FILM FET LOW-NOISE RF AMPLIFIER

In this chapter, a ZnO thin-film FET low-noise RF amplifier (LNA) is designed through simulation using the Agilent Advanced Design System® (ADS). Using a set of measured S-parameters provided by AFRL on a prototype ZnO thin-film FET, simulation and analysis are completed on a prototype low-noise RF amplifier. Analysis into stability, gain, and frequency response is completed in an effort to ascertain the usefulness of this transistor for possible RF applications in civilian and military circuitry.

The LNA is designed to meet a forward gain of 12 dB, an input return loss of -12 dB, an output return loss of -12 dB, and a reverse isolation of -15 dB. The LNA design is to show unconditionally stability at 13.56 MHz in a 50 Ω system.

The transistor of this design has a gate length of 1.25 µm, instead of the 2 µm previously used throughout this dissertation. This device also has a gate-oxide thickness (t_{ox}) of 22 nm, in contrast to the t_{ox} of 30 nm for previous devices. In addition, using measured drain current from AFRL, a k'_{satSI} value of 63.92 x 10^{-9} A/V^4 is extracted using the method shown in Figure 3.1. This is compared to initial measured AFRL devices with a k'_{satSI} of 80 x 10^{-9} A/V^4 in Chapter 3, and fabricated test devices for the pixel driver and analog amplifier with a k'_{satSI} of 6 x 10^{-9} A/V^4 in Chapters 4 and 5, respectively.

6.1 Circuit Description

This section describes the architecture of the ZnO thin-film FET RF LNA, and gives a brief description of the design process. Figure 6.1 shows the schematic diagram of a single transistor LNA designed with a common-source configuration for maximum gain. An input series capacitor, C_1, for matching and DC blocking is used in conjunction with a shunt inductor, L_1, to provide gate biasing and continue the input matching circuit. The source inductor, L_S, is used to improve stability by providing non-resistive impedance and source degeneration for the ZnO thin-film FET. The output match consists of a shunt inductor, L_2, for matching and also to couple drain voltage to the ZnO thin-film FET. This inductor is followed by a series capacitor, C_2, which provides DC blocking and completes the matching circuit for the output. In addition, RF bypass capacitors are placed on the DC voltage nodes in order to bypass any RF frequency to ground and prevent coupling into the power supplies. The bypass capacitor values of 0.27 µF with a 0402 package have a self resonant frequency of 13 MHz, which is ideal for the operating frequency of 13.56 MHz.

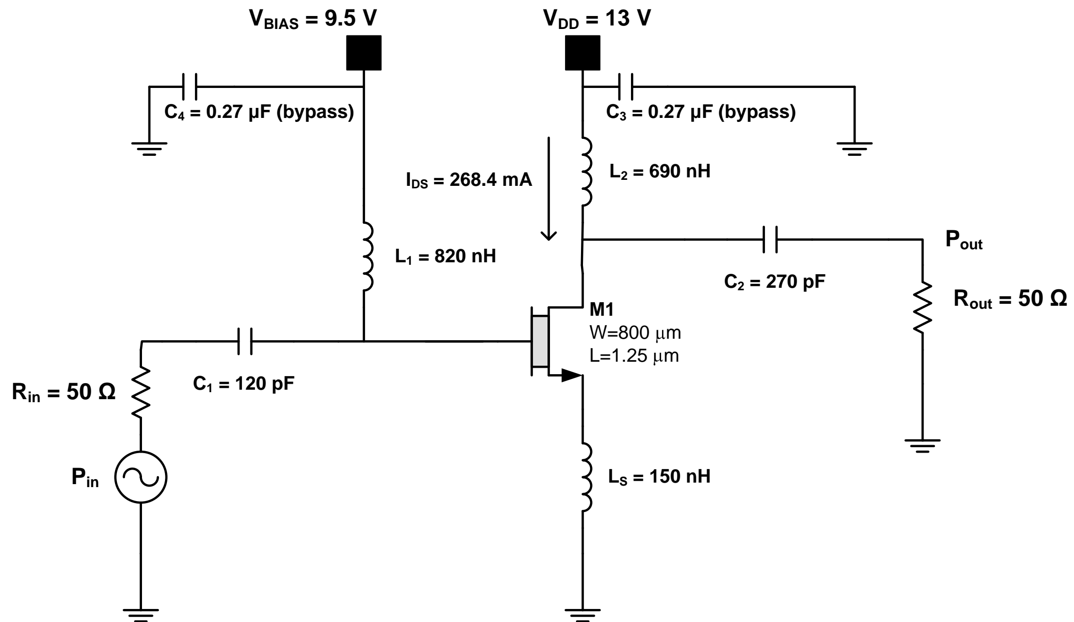

Figure 6.1. ZnO thin-film FET low-noise amplifier including input and output matching networks and source degeneration inductance for stability.

Each component of the amplifier is used in the Agilent Advanced Design System (ADS) along with S-parameters for a transistor M1. The transistor S-parameters were measured on a wafer probing station by the AFRL. Because these parameters were measured, accurate simulations results are expected.

From (3.2), I_D = 268.4 mA, W = 800 µm, L = 1.25 µm, V_{GS} = 9.5 V, V_T = 0.5 V, and k'_{satSI} = 63.92 x 10-9 A/V^4 is extracted as shown below

$$I_D = \left(\frac{W}{L}\right) \cdot k'_{satSI} \cdot (V_{GS} - V_T)^{M_{sat}} = \tag{6.1}$$

$$\left(\frac{800\ \mu m}{1.25\ \mu m}\right) \cdot 63.92\ E^{-9} \left(\frac{A}{V^4}\right) \cdot (9.5\ V - 0.5\ V)^4 = 268.4\ mA$$

The next section describes the S-parameter design of the amplifier.

6.2 Analysis and Design

When designing an RF LNA, there are several considerations that must be made before beginning an actual design. The very first of these decisions is usually an appropriate transistor to use for the application required. In this instance, the transistor was the deciding factor for the application. A ZnO thin-film FET was desired for use to show possible applications. Due to the AFRL measured unity-gain bandwidth of 950 MHz [2] for the ZnO thin-film FET, the LNA was designed to be used for the 13.56 MHz industrial, scientific, and medical (ISM) frequency band. A higher frequency could have been used, but a lower frequency was chosen to meet the gain specification of 12 dB. In this case, the application is for an RFID tag and/or tag reader.

The next step once a transistor has been selected is to analyze the transistor for stability. The standard practice of measuring stability is to use the S-parameters extracted for the transistor and make an initial assessment using the Rollett Stability Factor, *K*, the intermediate quantity *Δ* [24]. The intermediate quantity *Δ* and Rollett Stability Factor *K* are given by

$$\Delta = (S_{11} \cdot S_{22}) - (S_{12} \cdot S_{21}) \tag{6.2}$$

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 \cdot |S_{21}| \cdot |S_{12}|} \tag{6.3}$$

Knowing the Rollett stability factor K and Δ, an initial observation of stability is determined. If $K > 1$ and $|\Delta| < 1$, then the transistor is said to be unconditionally stable, which means that no matter what impedance is connected to the input or output of the transistor, it will not go into oscillation. Otherwise, it is known as potentially stable [25], which requires further analysis of the transistor.

If a transistor is potentially stable, according to the Rollett stability factor, K, further analysis is required to determine stability limitations. These stability limitations are best analyzed through the use of stability circles that are plotted directly onto a Smith chart. The Smith chart is a graphical tool used to plot impedances and admittances and is very useful in RF design. From [26], stability circles are first calculated from (6.4) – (6.7). Equations (6.4) and (6.5) show the calculation for the radius and stability of the input or source stability circle, respectively.

$$r_s = \left| \frac{S_{12} \cdot S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \tag{6.4}$$

$$c_s = \frac{(S_{11} - \Delta \cdot S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \tag{6.5}$$

Here the * operator indicates the complex conjugate of the value. A complex conjugate is the opposite imaginary operator in a complex number containing both real and imaginary values. When plotted, (6.4) and (6.5) create a circle on the Smith chart that shows an area of instability if an impedance of that region is presented to the input of the transistor.

Equations (6.6) and (6.7) present the equations needed to create the output stability circle.

$$r_L = \left|\frac{S_{12} \cdot S_{21}}{|S_{22}|^2 - |\Delta|^2}\right| \tag{6.6}$$

$$c_L = \frac{(S_{22} - \Delta \cdot S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \tag{6.7}$$

As in the case of the input stability circle, the plot shows the area of impedances that, if presented to the output of the transistor, would result in instability. Therefore, it is very useful to know what areas on the input and output of the device would result in unstable operation.

Once the values are plotted for both input and output stability circles, some alternative methods are employed to make the transistor unconditionally stable. Usually these alternative means tend to reduce gain or add noise, but are required if unconditional stability is desired.

If a transistor is considered potentially stable by the input and output stability circles, then design methods are employed to change the S-parameters of the transistor and thereby create a stable transistor. The three most popular methods of creating stability in a transistor are listed below:

1) Adding an input resistor.
2) Adding an output resistor.
3) Adding a series inductor to the source (in a common-source configuration).

In the case of an LNA design, neither 1 nor 2 are desirable due to the additional thermal noise that a resistor would add to a signal path, with 1 being the least desirable due to the noise being amplified from the input. This then leaves option 3.

The addition of a series source inductor assists in the cancellation of reactance on the gate of the transistor caused by capacitance between the gate and source of the transistor [27]. This cancellation then provides a pure resistance at the gate to the signal source and assists in the stability of the entire device. As quoted from [24], “The actual output impedance of a transistor is dependent upon the source impedance that the transistor ‘sees’. Conversely, the actual input impedance of the transistor is dependent upon the load impedance that the transistor ‘sees’.” If this is true, then once the inductor is added to the transistor to improve stability, the conjugate matching technique is used for maximum gain, starting with the output and then followed by the input match.

Once a suitable source inductor value is selected that moves the stability circles outside the Smith chart (i.e. a resistive component that is greater than infinity or less than 0), then a check of maximum available gain (MAG) is calculated for perfect conjugate matching conditions [24]. Therefore, a ceiling is set on the amount of gain available in the design. To calculate MAG, first an intermediate value in (6.8) is required to do the completed MAG calculation in (6.9) [24]. These values are given below as

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \qquad (6.8)$$

$$MAG = 10log\frac{|S_{21}|}{|S_{12}|} + 10log\left|K \pm \sqrt{K^2 - 1}\right| \tag{6.9}$$

where B is an intermediate value used to determine the ± value. If B is +, the – sign is used in (6.8), otherwise it would be the opposite. K is the Rollett stability factor from (6.3).

Once the MAG value is calculated, then an absolute maximum obtainable gain for the transistor is known. Typically, including the loss of the input and output matches, the achievable gain is 2 dB below the MAG. Now that the transistor is unconditionally stable with the source inductor, it is now possible to use conjugate matching on the input and output for maximum gain. Numerous materials are available for matching tutorials, so the process will not be duplicated in this work. One good example of conjugate matching for an RF amplifier is found in [28].

6.3 Design Simulations

This section goes through the complete design and simulation process as required to design a ZnO thin-film FET LNA. First, the transistor is checked for stability, then made stable. The MAG is calculated and gain goals are set for the design. Once design goals are created, then matching and bias circuits are designed and simulated for accuracy. Trade-off design goals will be made in order to meet pre-selected specifications of the design. These were given at the beginning of the chapter.

The method employed to model the ZnO thin-film FET is known as the s-parameter model. Measurements were taken by AFRL at the substrate level using an RF probe station and a vector network analyzer (VNA) to record the measurements. The

VNA then saves those measurements from the input and output ports into a two-port s-parameter file, also known as an S2P file. This S2P file is imported into Agilent ADS as a model block and connections are made in order to simulate the S-parameters as a linear model block. Agilent ADS is used to simulate the S2P file with calculation blocks present to make certain initial calculations. In this instance, multiple blocks are placed in parallel to simulate a larger ZnO thin-film FET device than was measured. This method by industry standard practice is considered acceptable up until approximately 1 GHz. After 1 GHz, parasitics are no longer properly modeled by placing the s-parameter blocks in parallel, and a new measurement of the required transistor must be made. In the case of this design, the operating frequency is 13.56 MHz, so the parallel s-parameter method is sufficiently accurate.

The parallel model creates an 800 μm/1.25 μm ZnO thin-film FET from a 100 μm/1.25 μm FET measured in the lab. This configuration simulates a ZnO thin-film FET interdigitized with 8 fingers.

The first characteristic that requires calculation by ADS is the Rollet stability factor K, and the intermediate value Δ. They are each plotted on the same graph and are shown in Figure 6.2.

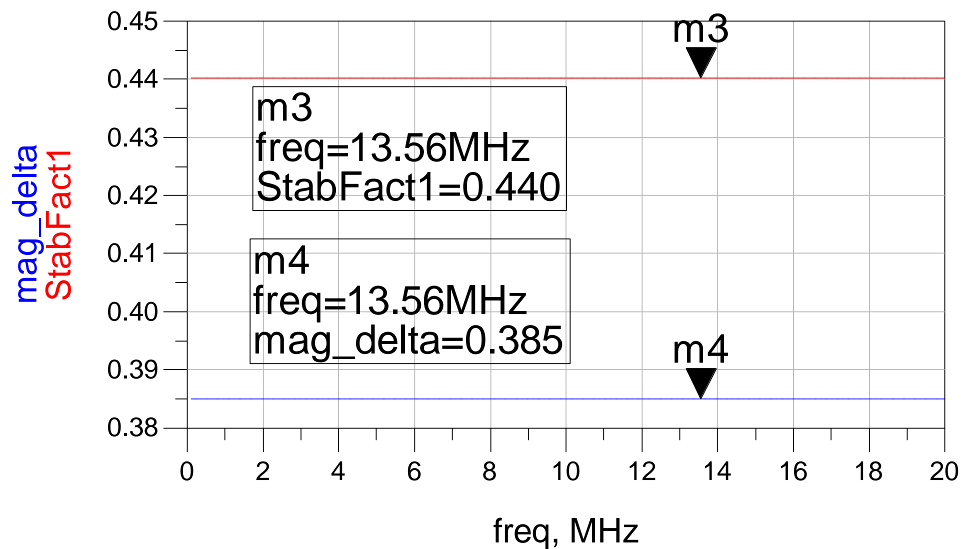

Figure 6.2. Rollett stability factor *K*, as StabFact1. Also mag_delta is plotted which has previously been symbolized by *Δ*.

From Figure 6.2, K is not greater than 1, so the ZnO thin-film FET at the current biasing conditions is not unconditionally stable. However, *Δ* is less than 1 as desired for stability, which means that the ZnO thin-film FET is potentially stable and requires further analysis to ascertain usable stability.

Stability circle calculations are the next step in determining stability for a transistor. Using Smith chart plots, and the source and load stability circle functions of Agilent ADS, stability circles for the source and load are plotted in Figures 6.3 and 6.4.

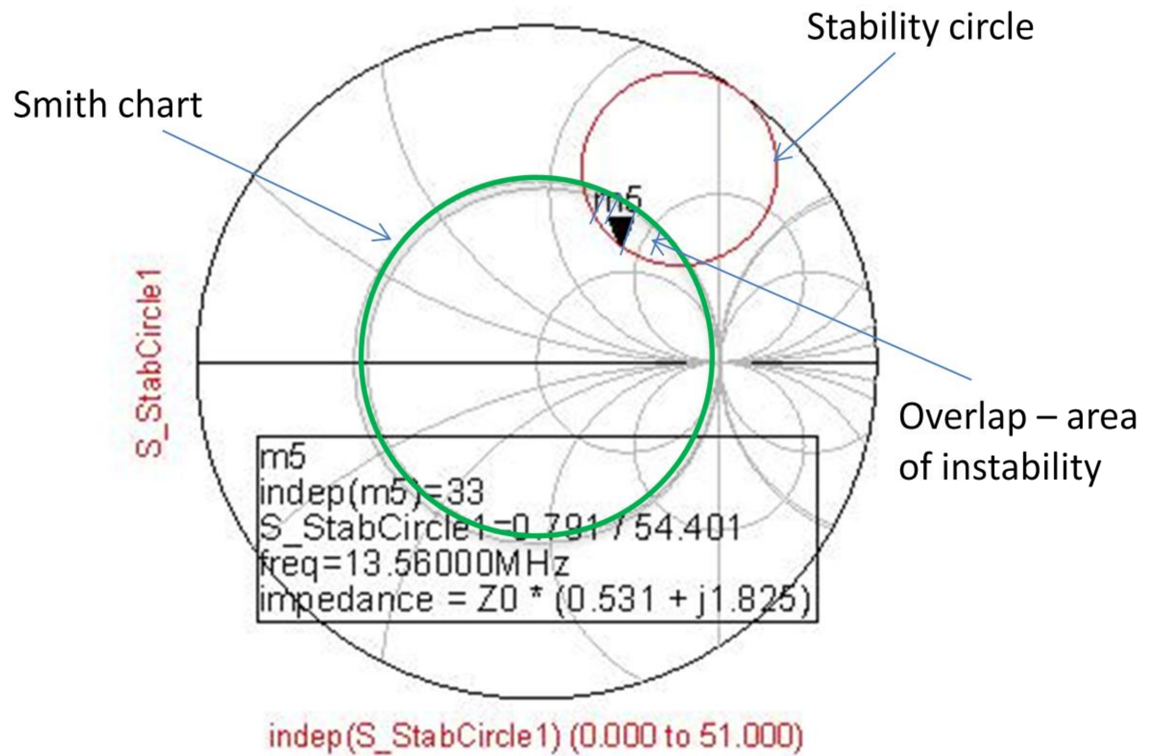

Figure 6.3. Source stability circle at 13.56 MHz showing operation within the real portion of the Smith chart at 13.56 MHz.

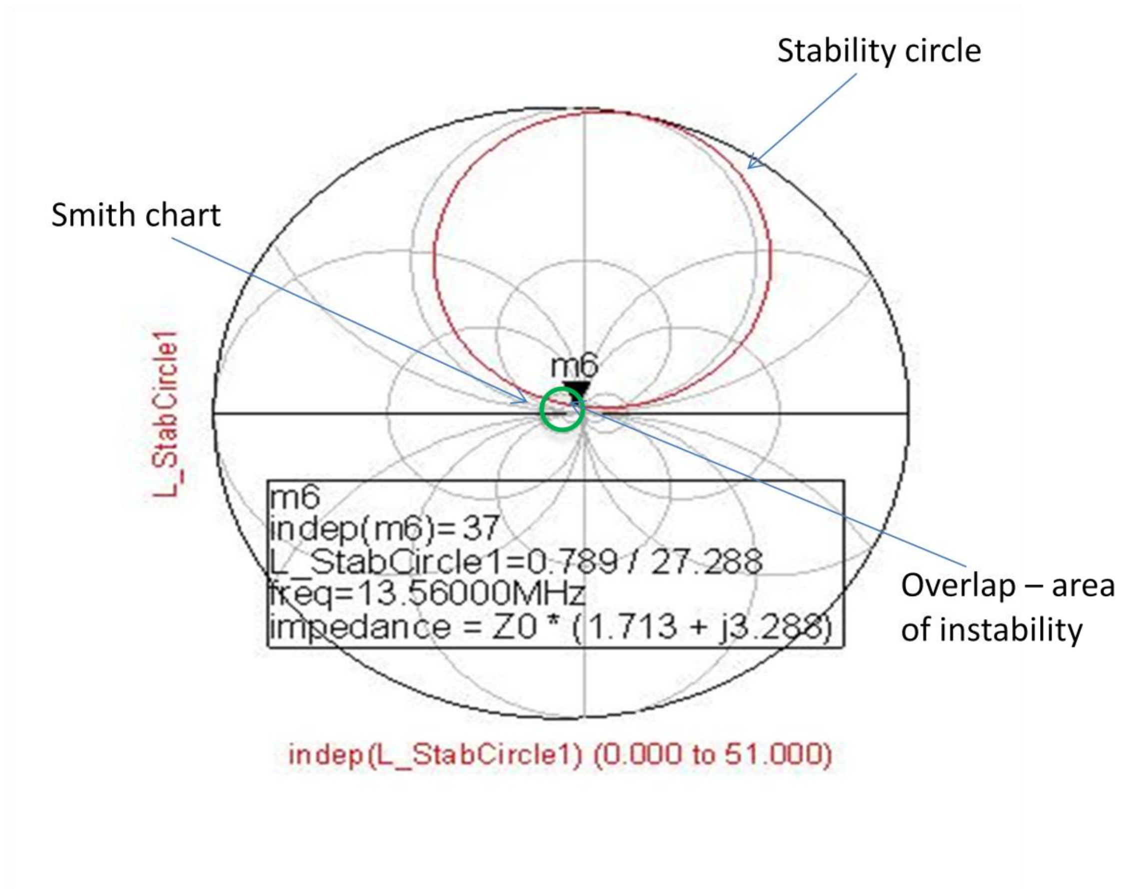

Figure 6.4. Load stability circle showing operation within the real part of the Smith chart at 13.56 MHz.

From the two stability circle plots, it is evident that the ZnO thin-film FET is potentially stable and not unconditionally stable. This is because there is aregion of overlap between the stability circles and the real portion of the Smith chart. Therefore, a stability technique must be used in order to use the ZnO thin-film FET. Looking at Figure 6.1, a series source inductor of 150 nH is placed at the source of the ZnO thin-film FET in order to cancel the reactive portion of the gate to source capacitance and cause the stability of the transistor to improve to an unconditionally stable condition. Once the 150 nH inductor is included in the simulation, the stability analysis is iteratively

accomplished until a satisfactory level of the Rollett stability factor and stability circles are achieved. Figure 6.5 reveals the Rollett stability factor, *K*, and the mag_delta after the 150 nH stabilization inductor is included. Each are considered to meet requirements for unconditional stability because the StabFact, or K is greater than 1, and the mag_delta, or Δ is less than 1. Therefore, it is now unconditionally stable and conjugate matching may be performed on the input and output of the LNA.

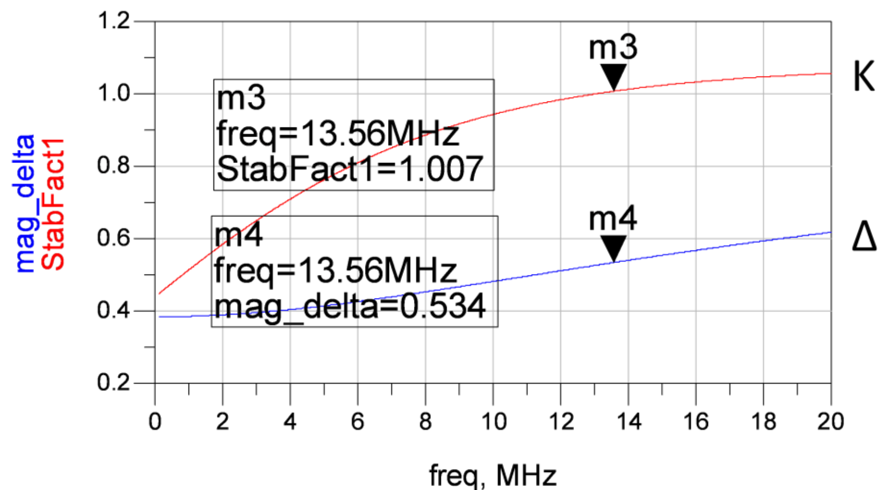

Figure 6.5. Rollett stability factor, *K*, as StabFact1. Also mag_delta is plotted which has previously been symbolized by *Δ*. Each are considered unconditionally stable.

Now that stability is confirmed both using the Rollett stability factor, K, it is time to check the MAG or maximum achievable gain to set gain expectations in the final design. Figure 6.8 gives the calculated MAG with a 150 nH inductor included with the original s-parameter model.

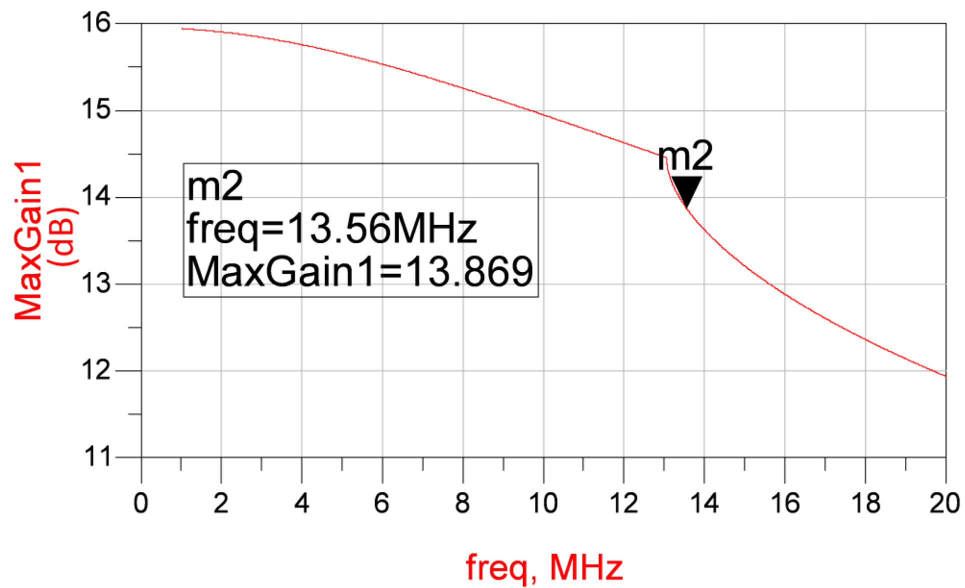

Figure 6.6. MAG or maximum available gain with the 150 nH source inductor present.

From Figure 6.6 an absolute max gain value of 13.9 dB is found as a ceiling for gain performance. This value is calculated considering a perfect transfer of power by a lossless conjugate match on the input and output of the ZnO thin-film FET at 13.56 MHz. Given this ceiling of gain performance, a gain of 12 dB is set as the goal of the completed design.

Now that a performance goal is set for the LNA, S-parameters of the ZnO thin-film FET including the source inductor are plotted to give a starting point for the design. Figure 6.7 shows all four S-parameters without input and output matching.

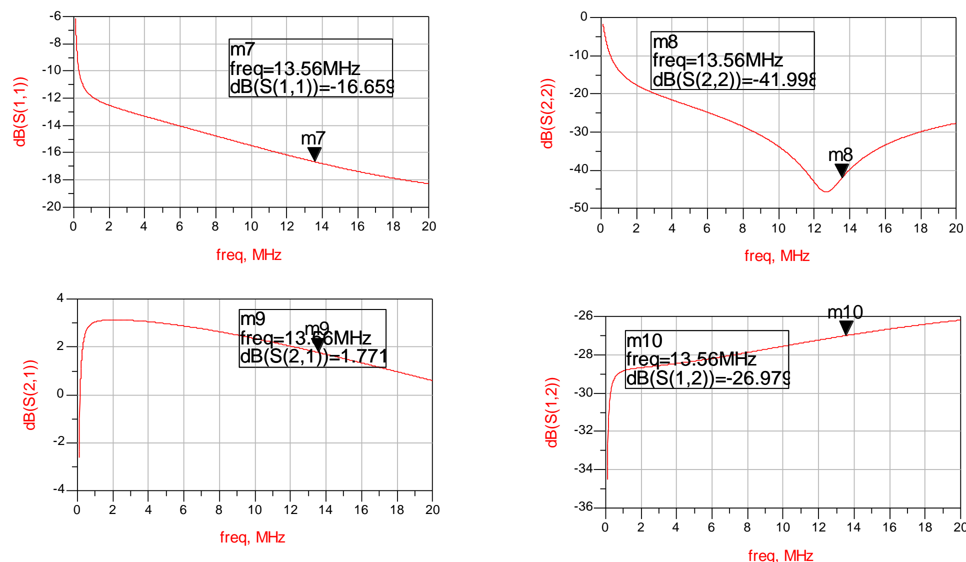

Figure 6.7. S-parameters of the unmatched ZnO thin-film FET including stability source inductor.

Analyzing M1 with source inductor but without input and output conjugate matching, the input return loss (S_{11}) is simulated at -16.7 dB, an acceptable return loss in most design applications. Typically -12 dB is considered an acceptable return loss and will be the upper threshold design goal. The output return loss (S_{22}) is simulated at -42 dB, which is far greater than expected in any design. The design goal in this circuit will be -12 dB. Reverse isolation (S_{12}) is simulated to be -27 dB and is always designed to be the minimum amount possible to prevent output loading from affecting the input match of the LNA. Finally, the forward gain (S_{21}) is simulated to be 1.8 dB, which is unacceptably low for this design. The present design requires that input and output conjugate matches be designed in order to have maximum achievable gain.

As shown in Figure 6.1, a conjugate matching network with a series capacitor *C_1* and shunt inductor *L_1* provide the input match. Also shown in Figure 6.1, the output match, with a shunt inductor *L_2* is followed by a series capacitor *C_2*. Each match is used for a dual purpose, both for RF matching and biasing for the ZnO thin-film FET. The input match is created using a series 120 pF capacitor *C_1* for matching and DC blocking. The input matching 820 nH inductor *L_1* is used for matching and for biasing the gate with a DC voltage. The output match consists of a shunt 690 nH inductor *L_2* that provides the drain voltage and matching. Also included in the output match is a series 270 pF capacitor *C_2* that provides matching and DC blocking on the output. Figure 6.8 gives a Smith chart plot of the input and output matching impedances with the matching components present.

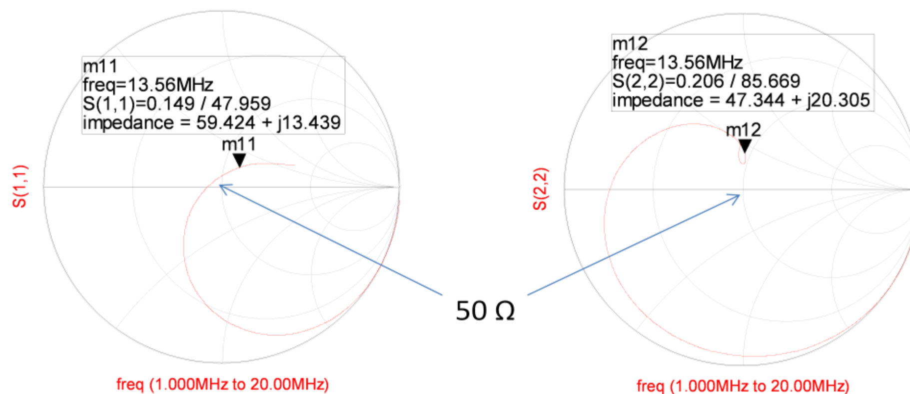

Figure 6.8. ADS Smith chart plots of input and output impedance in order to show conjugate matches.

In each plot, the goal is to have the markers on 50 Ω, or the center of the Smith chart. The closer to 50 Ω, the lower return loss since less voltage is being reflected back to the generator. As with most designs, some trade-offs must take place to achieve the design goals on all parameters. In this case, to prevent either input return loss or output return loss from going out of specification, a compromise impedance is maintained for each to achieve acceptable performance Z_{in} = 59.4 + j13.4 Ω, and Z_{out} = 47.3 + j20.3 Ω at 13.56 MHz. Figure 6.9 gives a final illustration of the S-parameter plots with full matching circuitry finalized.

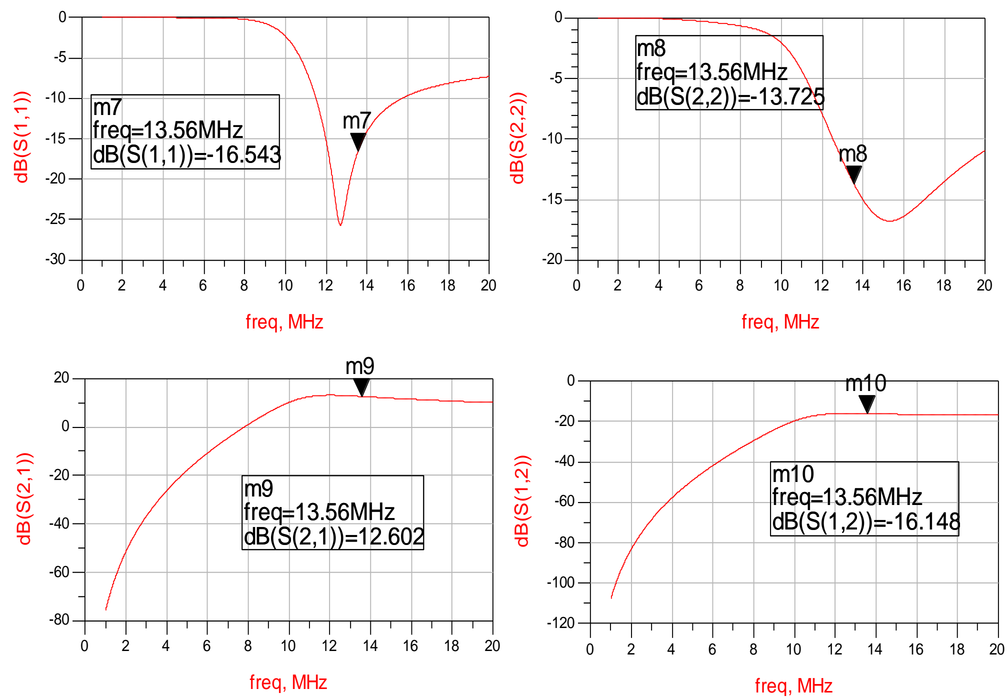

Figure 6.9. Simulated S-parameters of complete, matched ZnO thin-film FET LNA.

For the entire amplifier in a 50 Ω system, the forward gain (S_{21}) is simulated at 12.6 dB. The input return loss (S_{11}) is simulated at -16.5 dB with the output return loss (S_{22}) simulated at -13.7 dB. Reverse isolation (S_{12}) is simulatd at -16.1 dB. This is a reasonable value to isolate output loading effects from pulling the input match.

6.4 Summary and Conclusions

In conclusion, a ZnO thin-film FET LNA was designed and simulated for the 13.56 MHz ISM frequency band for application in RFID tags and tag reading devices. From drain current information for the s-parameter file a 100 µm/1.25 µm device draws 33.55 mA of current. This corresponds an amplifier having a current draw of 268.4 mA for 8 paralleled 100 µm/1.25 µm devices, which is quite excessive for the application. This does, however show a high current density of 335.5 µA/µm. Future designs may be able to improve current consumption by raising the characteristic impedance of the system to greater than 50 Ω. This would increase gain by allowing a larger output impedance with lower current consumption.

At a gate voltage of 9.5 V and drain voltage of 13 V, the ZnO thin-film FET operates at high voltages as required to increase the mobility as shown in Figure 3.2. Such high voltage operation is typical of current generation AFRL ZnO thin-film FETs. Achieving higher mobility at reduced values of V_{GS} would increase the performance of this technology for integrated circuit design.

CHAPTER 7: SUMMARY AND CONCLUSIONS

7.1 Summary and Conclusions of Work

This dissertation described the ZnO thin-film FET, its modeling and the design of pixel driver, analog amplifier, and RF amplifier circuits.

The following are the novel research contributions of this dissertation:

1. A ZnO thin-film FET behavioral drain current and capacitance model to allow for hand design and simulation of circuit performance in the Cadence design suite. This drain current shows a fourth order dependency on gate-source overdrive voltage for “strong inversion,” saturation, operation. The quartic-law behavioral model accurately tracks the measured performance to within ±1.6%. This quartic-law operation is in contrast to square-law operation for traditional bulk CMOS, without mobility reduction effects. Modeling is performed on the mobility that shows a square-law increase with gate-source overdrive voltage, which is considered a possible source of the drain current quartic-law “strong inversion,” saturation operation. Also, for the “strong inversion,” non-saturation or ohmic operation, the drain current shows a gate-source overdrive voltage raised to the 2.3 power instead of unity as expected in bulk CMOS. The models are evaluated using Air Force Research Laboratory ZnO thin-film FETs having a

minimal channel length of 2 μm and a gate-oxide thickness of 30 nm. These FETs are also used for the design of pixel drivers and analog amplifier circuits.

2. A fabricated pixel driver, which can sink 28 μA while having a gate area of only 20 μm^2. This pixel driver is believed to be the smallest published with high current density (14.5 μA/μm) at a low drain voltage of 2 V. This performance matches the drain current model of Chapter 3 and gives confidence for future pixel driver designs. Performance is confirmed with verilog-A simulation in the Cadence design suite.
3. A ZnO thin-film FET analog amplifier is analytically designed utilizing the behavioral model of Chapter 3. It is believed to be the first ZnO thin-film FET analog amplifier to be designed. The amplifier is designed to have a gain of 3 V/V at 10 kHz, with rail voltages of ± 5 V and a total current consumption of 8 μA.
4. A low-noise RF amplifier is designed from scattering parameters measured at the Air Force Research Laboratory for ZnO thin-film FETs having a gate length of 1.25 μm and a gate-oxide thickness of 22 nm. This design achieves 12.6 dB of gain while having less than 16.5 dB of input return loss, less than 13.7 dB of output return loss and less than 16 dB of reverse isolation in a 50 Ω system. The amplifier is designed for the RFID tag frequency of 13.56 MHz.

Planned publications from this work are as follows:

1. *IEEE Transactions on Electron Devices*, "Behavioral drain-current modeling of the ZnO thin-film FET."

2. *IEEE Transactions on Electron Devices*, "Design and evaluation of a ZnO thin-film FET pixel driver circuit."
3. *IEEE Transactions on Electron Devices*, "A ZnO thin-film FET RF low-noise amplifier design for RFID applications using measured S-parameters."
4. *IEEE Electron Device Letters*, "A ZnO thin-film FET analog amplifier."

7.2 Proposed Future Work

The first step toward future work would include evaluating multiple test transistors in varying sizes to confirm the existing modeling equations and to adjust them if needed. This would verify the modeling of the k'_{satSI} value as the shape factor (W/L) is scaled for various test transistors. Once multiple test transistors are measured and modeled, then new circuits could be fabricated to retest the models.

As described in this research, recent fabricated devices had a threshold voltage of -3.4 V compared to an expected value of + 0.5 V. In addition, k'_{satSI} was 13.3 times lower than designed and gate leakage was measured. Due to these unexpected parameter shifts, a second fabrication of the pixel driver circuit is planned. Also, because of the fabricated circuits had a threshold voltage of -3.4 V, the analog amplifier was not operational. Another analog amplifier should be fabricated to have a positive threshold voltage in order to fully test the first Zno thin-film FET analog amplifier.

Next, the designed LNA should be fabricated and housed in a package for placement onto an evaluation board. Noise measurements should be made on the ZnO thin-film FET LNA in order to develop noise models for analog and RF simulation. Using noise models would allow for prediction of the noise figure (NF) in simulations for

further LNA designs. Once NF measurements are made, input third order intercept point (IIP3) measurements should be collected to determine the input dynamic range of such an amplifier.

After the LNA of this dissertation is built, a second LNA should be designed with a characteristic impedance higher than 50 Ω to assist with gain while presumably lowering drain current consumption.

In addition to more model test data, further work should be done to investigate the conditions by which the mobility holds a square-law behavior with the gate-source overdrive voltage. This square-law operation is a significantly novel characteristic of the ZnO thin-film FET and should be explored more thoroughly in order to have more accurate models for circuit design.

Once investigation into mobility is complete, the next step is to develop a MOS continuous current model equation to account for transitions from "weak" to "strong inversion" operation for the ZnO thin-film FET. This transition region, known as the "moderate inversion" region between the "weak inversion" and "strong inversion" regions, could be modeled as motivated by the EKV MOS model. "Moderate inversion" modeling could facilitate micro-power, low frequency designs.

Finally, with the similarities of the band gap between ZnO and GaN (both near 3.4 eV), it is appropriate to make plans for power amplifier development. Perhaps adjustments are needed for certain peak power values, but the high breakdown voltage of ZnO thin-film FETs does lend itself to power amplifier design. Initially, linear power amplifiers should be attempted so that the one dB compression point (P1dB) and output

third-order intercept points (OIP3) are measured. If P1dB and OIP3 are competitive to existing GaN or GaAs process characteristics, then ZnO may deserve further study for RF power amplifier research.

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APPENDIX A: VERILOG-A MODEL

```
// VerilogA for ZnO_Dissertation, ZnO_FET_10_2, veriloga

`include "discipline.h"
`include "constants.h"

// Began February 25, 2009 Completed January 10, 2010
// Alan Calder
// This model is to describe a Zinc-Oxide Thin-Film Transistor
// Simple model, "Strong Inversion", Saturation operation
// Drain-Source Current model equation
// VerilogA for ZnO_Dissertation

`include "discipline.h"
`include "constants.h"

module ZnO_FET_10_2 (D, G, S);

        inout D, G, S;
        electrical D, G, S;

        parameter real Vth = -3.4; // Threshold voltage strong inversion
        parameter real k = 6e-09; // Constant for device equation
        parameter real W = 10e-06; // Width of device
        parameter real L = 2e-06; // Length of device

        //
        // visible variables
        //
        real Ids, Vgs, Vds, Veff;

analog begin

        Vgs = V(G, S);
        Vds = V(D, S);

// Define Veff as the Gate-Source voltage - threshold voltage

        Veff = Vgs - Vth;

// Define the Drain-Source current equation
```

```
        Ids = (W/L)*k*(Veff*Veff*Veff*Veff)*(1 + 0.05*Vds);

        I(D, S) <+ Ids;

        end

endmodule
```