A Biofuel-Cell-Based Energy Harvester With 86% Peak Efficiency and 0.25-V Minimum Input Voltage Using Source-Adaptive MPPT

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***Abstract*— This article presents an efficient cold-starting energy harvester system, fabricated in 65-nm CMOS. The proposed harvester uses no external electrical components and is compatible with biofuel-cell (BFC) voltage and power ranges. A power-efficient system architecture is proposed to keep the internal circuitry operating at 0.4 V while regulating the output voltage at 1 V using switched-capacitor dc–dc converters and a hysteretic controller. A startup enhancement block is presented to facilitate cold startup with any arbitrary input voltage. A real-time on-chip 2-D maximum power point tracking with source degradation tracing is also implemented to maintain power efficiency maximized over time. The system performs cold startup with a minimum input voltage of 0.39 V and continues its operation if the input voltage degrades to as low as 0.25 V. Peak power efficiency of 86% is achieved at 0.39 V of input voltage and 1.34 μW of output power with 220 nW of average power consumption of the chip. The end-to-end power efficiency is kept above 70% for a wide range of loading powers from 1 to 12 μW. The chip is integrated with a pair of lactate BFC electrodes with 2 mm of diameter on a prototype-printed circuit board (PCB). Integrated operation of the chip with the electrodes and a lactate solution is demonstrated.**

***Index Terms*— Biofuel-cell (BFC), CMOS, cold startup, dc–dc voltage converter, energy harvester, health monitoring, power management, source-adaptive maximum power point tracking (MPPT), wearable sensor.**

I. Introduction

RECENT advances in low-power electronics have paved the way for a wide range of wearable and implantable biomedical devices for health monitoring and fitness applications. Integration of such millimeter-scale devices on biocompatible platforms shows great potentials for real-time biochemical sensing [1]–[6]. Many personalized monitoring biodevices are designed to perform multiple tasks, such as on-demand wake-up, multiplexed sensing, data processing, and wireless data transmission. These power-demanding operations are performed continuously or periodically over long durations, which set challenging requirements for the energy sources and the overall power efficiency of the system [7].

Batteries have been the primary solution for many biochemical sensing systems; however, their limited capacities prevent long-term operations [8]–[10]. This is more pronounced when devices are miniaturized, and batteries must fit into smaller form factors. To tackle these challenges, prototypes with near-field wireless power delivery have been recently demonstrated for both implantable and wearable devices [11]–[14], yet their applications are limited since wireless power transmitters suffer from limited tissue depth penetration and need to be always in proximity of the sensor.

Other potential energy sources for biodevices include human body heat through thermoelectric generators (TEGs), body motion via piezoelectric cells, and the sunlight with photovoltaic cells (PVCs). However, they all fail to provide adequate power for local signal processing and wireless data transmission due to their low-power densities [15], [16]. Off-chip storage elements could be utilized to periodically store and then deliver energy, but they increase the overall size of the system and would not allow continuous operation.

Biofuel cells (BFCs) are promising alternatives to other forms of energy sources because of the versatile presence of biofuels and their superior energy density. Biofluids such as sweat, blood, basal tear, and saliva could serve as sustainable energy sources for the next generation of integrated biodevices [17], [18]. Glucose and lactate are fundamental energy containing substances, which are found in abundance in biofluids. Lactate, as the main metabolic product of both muscle and brain exertion, is found in sweat at tens of millimolar levels [19], [20].

Enzymatic BFCs act as biocatalysts to transform the bioenergy into electricity [21], [22]. They provide power densities at an approximately 1–40 μW/mm^2 range [23]. For small surface areas, it is crucial to design energy harvesters with high efficiencies at microwatt input power levels. It is also important to note that the open-circuit (OC) voltage levels of the recently developed BFCs nonpredictably range from 0.3 to 0.6 V, and the energy harvester system needs to convert the voltage to higher levels as required by most sensors. The OC voltage is mainly set by the electrode design, the materials on the cathode, and even the packaging of the enzymes on the

Manuscript received June 4, 2020; revised August 14, 2020 and September 28, 2020; accepted October 22, 2020. This article was approved by Associate Editor Qun Jane Gu. *(Corresponding author: Arian Hashemi Talkhooncheh.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2020.303549.

Digital Object Identifier 10.1109/JSSC.2020.3035491

electrodes. Moreover, as power extraction continues, biofuels degrade over time and the system should track these changes to efficiently continue the operation. In fact, the available input voltage of the BFC at the maximum power point (MPP), which is always lower than the OC voltage, decreases as the BFC or the solution concentration degrades [23].

Previous integrated sensors using BFCs as their energy sources have utilized either extensive off-chip circuitry, with numerous BFC electrodes to supply all modules [23], or bulky off-chip electrical capacitors (1 μF and 1 $\times$ 0.5 mm^2) for energy storage because of the limited power and OC voltage [24]. Other energy harvesting systems developed for Internet of Things (IoT) applications either use external electrical components [25]–[30], or suffer from loading condition dependencies [31], limited voltage requirements [32]–[34], and non-optimal power efficiencies at few-microwatt loading conditions [35]–[37].

This article presents a cold-starting energy harvester in 65-nm CMOS with source degradation tracing and automatic MPP tracking (MPPT) to address these BFC energy extraction challenges. A combination of two dc–dc voltage boost and buck converters with a hysteretic regulation approach is proposed to achieve 86% peak efficiency at 0.39 V of input voltage and 1.34 μW of output power. The chip uses no off-chip components, except for two BFC electrodes, developed using cross-dimensional nanomaterial integration, that utilizes lactate and oxygen as the fuel sources. Finally, energy extraction and power delivery from a lactate solution is demonstrated using the proposed integrated biodevice. The fully integrated CMOS chip allows for easy integration with any compatible energy source, as well as larger health-monitoring devices, such as smart watches and skin patches. Moreover, the overall fabrication cost is reduced due to minimized component count and in the final product.

This article is organized as follows. In Section II, the proposed system architecture is presented, and its advantages are described. Section III provides the system-level analysis of a generic harvester system and extends it to the proposed architecture. All major system building blocks and their interconnections are described in detail in Section IV. Section V elaborates the operation of the MPPT and presents the algorithm used to perform source degradation tracing. The experimental results of the energy harvester chip and its integration with the BFCs are provided in Section VI. Finally, Section VII summarizes this article with performance comparisons and conclusions.

II. Proposed System Architecture

State-of-the-art BFCs provide power densities in a range of 1–40 μW/mm^2 of the electrode area. To design a compact device with a single pair of BFC electrodes with 2 mm of diameter, the energy harvester should dissipate fewer than 1 μW on average for a reasonable end-to-end power efficiency. It is also very important that the system wakes up immediately whenever the source power is available, and energy extraction should start immediately without any external trigger. In addition, to make the harvester system compatible with standard

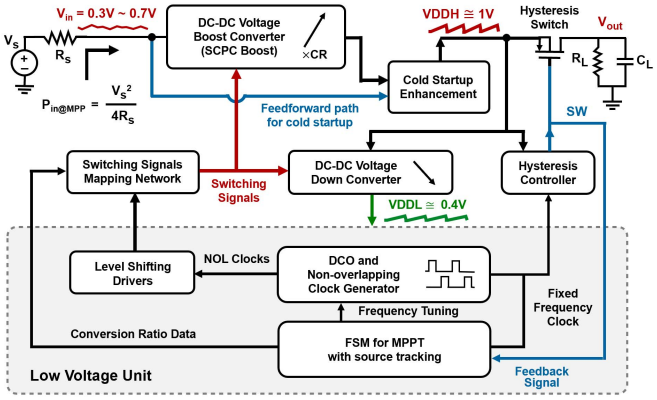


Fig. 1. Top level block diagram of the proposed energy harvester system.

on-chip CMOS sensors, we intend to regulate the boosted voltage at nominal supply values (0.9–1.2 V).

For major improvements in the overall power efficiency of the energy harvester systems, the system architecture design should be prioritized over block-level optimizations. The internal supply voltage seems to be the main bottleneck of the overall internal power consumption. In fact, the internal circuitry could be designed to operate with a lower supply to save power. It is well known that the supply voltage has a quadratic relationship with the dynamic power and a linear relationship with the static power of the digital circuitry [38]. The proposed system architecture is designed to be supplied by the lowest reliable voltage that the 65-nm CMOS technology permits. Although most designed blocks operate successfully with 0.25 V, the internal supply is set to 0.4 V. This voltage was chosen based on reliable operation of the logic core of the system.

A major challenge is that the internal supply voltage also needs to be regulated. Since the lower boundary value of the BFC OC voltage (0.3 V) is lower than the targeted internal voltage supply (0.4 V), it would not be reliable to directly downconvert and regulate the BFC voltage to supply the internals. In this article a system-level solution is proposed to address these challenges and to achieve superior power efficiency.

The proposed top-level block diagram of the energy harvester is shown in Fig. 1. It consists of a reconfigurable switched-capacitor power converter (SCPC) in parallel with a feedforward path for cold startup that is initially used to bypass this block. A cold startup enhancement block receives the available voltages from these two paths and delivers the highest available voltage to the internal circuitry. A dual-path dc–dc voltage down converter provides voltage supply to the low-voltage unit (shaded with gray in Fig. 1), which includes a digitally controlled oscillator (DCO) for the boost SCPC, a non-overlapping (NOL) clock generator, a finite-state-machine (FSM) for MPPT, and two ring oscillators with fixed frequencies for the FSM and the buck SCPC in the voltage down converter block. Clocking signals are generated at the low-voltage level (VDDL) and shifted up to the main supply voltage (VDDH) by a group of level shifters. These clock signals are fed to a mapping network, which redirects

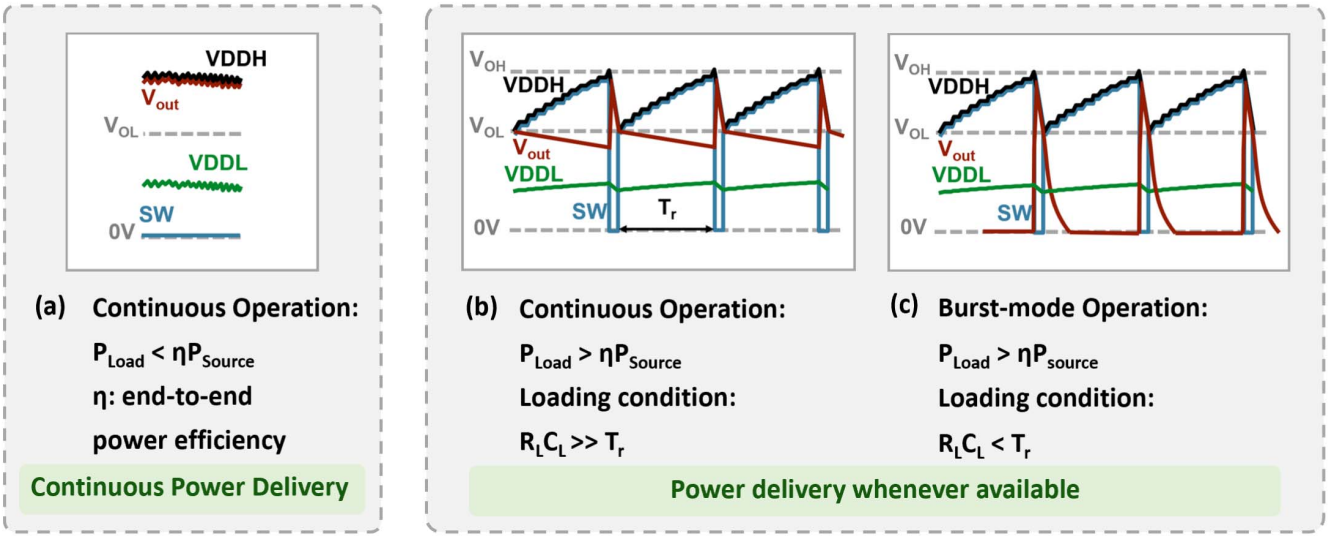


Fig. 2. Various loading conditions depending on the application. (a) Continuous power delivery (high-power sources or low-power sensors). (b) and (c) Periodic power delivery (for energy-storing/wakeup-enabled sensors with high power requirements).

and distributes them to corresponding switches in the boost and the buck SCPCs. The switching network is designed based on a combinational logic FSM and is controlled by a conversion ratio (CR) set by the MPPT FSM dynamically. At the same time, the boosted voltage (VDDH) is regulated by a hysteretic controller between two programmable thresholds (V_{OH} and V_{OL}), which could be set according to the load requirements. The proposed architecture ensures that the system performs a cold startup with a minimum input voltage of 0.39 V and continues operation when it degrades to as low as 0.25 V over time. Details of the cold startup and the operation of the building blocks with low-voltage supplies are provided in Section IV. The reason that the voltage up converter and voltage down converter stages are not combined is their different roles in the architecture. In fact, the boost stage provides an arbitrary gain over time for MPPT, which makes its internal stages to have arbitrary voltage levels. The buck stage, however, receives and downconverts the regulated voltage for the internals. Another benefit of cascading the down converter stage is the reduction of the ripples at VDDH by the gain of the down-conversion at the VDDL node. Utilizing the proposed two-stage topology is more power efficient only if the cascading losses are minimized and the overall power efficiency is better than having the internals supplied by the boosted voltage (0.9–1.2 V). A power analysis based on measurements is provided in Section VI to further demonstrate the benefits of the proposed system architecture.

The regulating switch on the right side of Fig. 1 is designed to remain on if the loading demand is less than the deliverable power. In this case, the short-wave (SW) signal remains at the ground level (the switch is operated with an inverted logic and turns on when the SW signal is low). VDDH, hence, V_{out} would rise and saturate above the targeted values for regulation at the MPP and the load will be continuously powered. Then depending on the application, the gain CR or the switching frequency (f_{S1}) of the boost SCPC could be changed to move away from the MPP for de-stressing the BFC

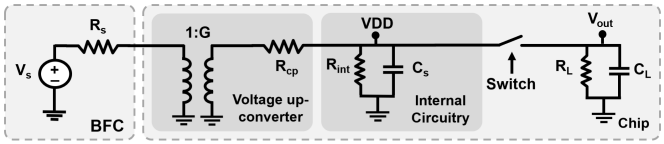


Fig. 3. Simplified circuit model of a generic energy harvester system.

and improving its lifetime. This scenario is shown in Fig. 2(a). In the opposite case, in Fig. 2(b), when the loading demand is higher, the switch performs a hysteretic control to keep VDDH between two programed thresholds (V_{OH} and V_{OL}). The circuit charges up an on-chip storage capacitor (C_{st}), until VDDH reaches V_{OH}. Then the switch turns on to deliver power to the load, until VDDH drops to V_{OL}, and then turns off to recharge the capacitor. In this case, the charging time (T_r) is smaller than the load *RC* time constant (applicable to sensors with a storage capacitor). Hence, V_{out} would remain high even when the switch is off, and we would again have a continuous sensing operation. In the third case, in Fig. 2(c), the situation is similar, except that the *RC* time constant of the load is lower than T_r. Therefore, V_{out} drops to zero whenever the switch is off. This is applicable to sensors with a burst-mode (wakeup-enabled) operation, where sensing continues whenever power becomes available.

To show the advantages of the proposed architecture compared to the previous designs, a system-level analysis of a generic energy harvester and its extension to the proposed system are discussed next.

III. Harvester System Modeling and Analysis

In this section, a simplified circuit model is provided to analyze the nonlinear characteristics of a generic harvester system. By the pseudo-static assumption, a general-purpose energy harvester could be modeled as a voltage boost converter in series with a switch that connects the output of the harvester to the load, as shown in Fig. 3. Depending on the application

and the chosen architecture, this switch could always be kept closed, or designed to operate periodically to regulate the output voltage (load regulation). The inefficiencies of the system are modeled by a series resistance R_{CP}, causing a voltage drop after boosting, and a parallel resistance R_{int}, accounting for internal power consumption. Furthermore, a storage capacitor C_{st} is in parallel with R_{int} to support power delivery to both internal circuits and the load. R_{CP} and R_{int} would consist of both constant and dynamic portions depending on the architecture. A few examples of dynamic variables are the CR, switching frequencies, switching transistors widths, and the supply voltage. We have provided generic circuit models for the energy source (a voltage source V_S in series with resistance R_S) and the load (R_L in parallel with C_L) to extend our analysis for various sources and loading conditions. All these four variables could change over time (for example, to mimic source degradation in a BFC or a stand-by mode in a sensor). We define $P_{in,MPP}$ as the maximum transferable power from the source of energy to the system. According to the theorem of maximum power transfer, $P_{in,MPP}$ is calculated as

$$P_{in,MPP} = \frac{V_S^2}{4R_S}. \tag{1}$$

We also define P_{out} as the average of delivered power to the load, which could be written as

$$P_{out} = \frac{V_{out}^2}{R_L}. \tag{2}$$

We now consider the following conditions of operation for further analysis.

A. Continuous Power Delivery (Switch Always ON)

In this case, no output voltage (or load) regulation is performed and the power is constantly delivered to the load. This would be applicable to cases with powerful sources or less demanding loads. Depending on the loading conditions and the available power, the output voltage (V_{out} = VDD) would settle to an arbitrary value. With a given V_S, R_S, R_{CP}, and R_{int}, V_{out} is derived by the following equation:

$$V_{out} = V_S\left(\frac{R'_L \times G}{R'_L + R_{CP} + R_S \times G^2}\right) \tag{3}$$

where $R'_L = (R_{int}||R_L)$. The end-to-end power efficiency would also be calculated as

$$\eta_{out} = \frac{4R_S G^2}{R_L}\left(\frac{R'_L}{R'_L + R_{CP} + R_S \times G^2}\right)^2. \tag{4}$$

This shows that the boost converter gain G and the load resistance R_L could be tuned to satisfy the load voltage requirements. However, if the maximum power efficiency is intended, R_L will be the only factor that sets V_{out}. A simulated plot is provided in Fig. 4(a) to show the generic nonlinearities of (3) and (4). By maximizing the power efficiency with respect to G, we would have

$$\eta_{out,MPP} = \left(\frac{R'_L}{R'_L + R_{CP}}\right)\left(\frac{R_{int}}{R_{int} + R_L}\right). \tag{5}$$

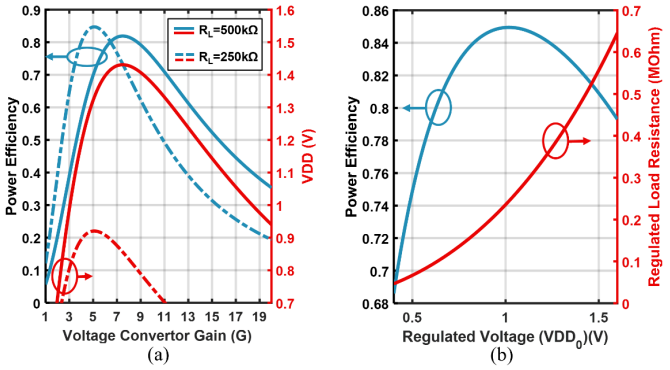


Fig. 4. Generic nonlinear system characteristics for (a) continuous power delivery (switch always on) and (b) load regulation (VDD regulation).

This maximum happens at

$$G_{MPP} = \sqrt{\frac{R'_L + R_{CP}}{R_S}} \tag{6}$$

and the output voltage is then set to

$$V_{out,MPP} = \frac{G_{MPP} \times V_S}{2}\left(\frac{R'_L}{R'_L + R_{CP}}\right). \tag{7}$$

Equation (7) shows that R_L sets $V_{out,MPP}$, which is not desired. Although, if the source is powerful enough to remove the need of MPPT, the gain G could be tuned away from the MPP to set V_{out} independent of R_L.

B. Load Regulation (VDD Regulation)

In this case, the switch is used to regulate VDD at a target value required by the load. This scenario is considered when the output power delivery is lower than the loading demand, even at the MPP. The switch turns on only when power is available, while keeping VDD above V_{OL} and below V_{OH} (hysteretic control). With the pseudo-static assumption, we can assume VDD is set to an average (VDD_0) by replacing the load and the switch with a new averaged load resistor R_{Lav}. This resistance depends on the switch toggling rate, which keeps VDD at VDD_0. By rewriting the equations, the power efficiency at MPP is derived as

$$\eta_{out,MPP} = \frac{2}{1 + \sqrt{1 + \left(\frac{R_{CP}}{R_S}\right)\left(\frac{V_S}{VDD_0}\right)^2}} - \frac{4R_S \times VDD_0^2}{R_{int} \times V_S^2}. \tag{8}$$

The first term in (8) is the overall efficiency of the transferred power to the right side of the voltage booster and the second term is the power penalty of the internal circuits. At this maximum, the voltage gain (G_{MPP}) is

$$G_{MPP} = \sqrt{\frac{R'_{Lav} + R_{CP}}{R_S}} = \frac{VDD_0}{V_S} + \sqrt{\left(\frac{VDD_0}{V_S}\right)^2 + \frac{R_{CP}}{R_S}} \tag{9}$$

where $R'_{Lav} = (R_{int}||R_{Lav})$ and R_{Lav} can be calculated by

$$R_{Lav} = \frac{R_{int}}{\sqrt{1 + \left(\frac{R_{int}}{R_{CP}}\right)}}. \tag{10}$$

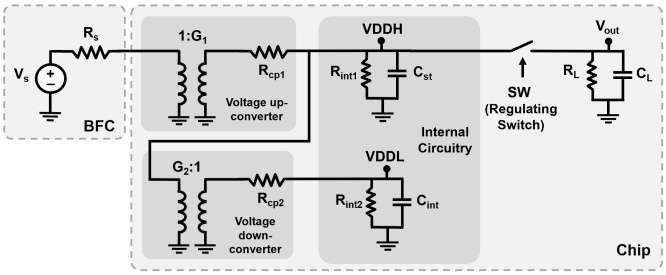


Fig. 5. Simplified circuit model of the proposed energy harvester system.

Fig. 4(b) shows simulated trends of R_{Lav} and power efficiency $\eta_{\mathrm{out,MPP}}$ versus VDD_0. It is worth noting that in this scenario, the power efficiency at MPP depends on VDD_0. If the supply requirement for a sensor is different than the maximum point of this curve, then extra power is burned internally. This inefficiency is due to a resistance mismatch between R_{Lav} and the rest of the circuit (even at the MPP). Another noticeable observation is that R_{Lav} is independent of R_{L}, which is desired in designing an energy harvester without taking loading conditions into account.

The simplified circuit model of the proposed energy harvester system is shown in Fig. 5. Using a secondary voltage converter, the boosted and regulated voltage (VDDH) is converted down (VDDL) to supply the internal circuits. A switched capacitor structure is used for both voltage converters to achieve superior voltage conversion efficiency. Capacitors can be designed precisely in CMOS processes, which help with accurate system-level modeling. While inductor-based voltage converters also provide a similar performance, it is desirable to avoid using bulky off-chip or area consuming on-chip inductors. The reconfigurable boost SCPC allows for having independent control over the gain (G_1) and the switching frequency (f_{S1}). Another SCPC with a fixed gain (G_2) and a fixed switching frequency (f_{S2}) is used to downconvert the voltage at steady state. VDDL is chosen to be 0.4 V to ensure reliable internal operations, therefore, G_2 is set to 2.5. The resistors R_{CP1} and R_{CP2} in Fig. 5 are inversely proportional to their corresponding flying capacitors and switching frequencies (f_{S1} and f_{S2}). Finally, R_{int1} and R_{int2} are resistors that account for both dynamic and leakage power.

The model provided in Fig. 5 would be more power efficient at steady state compared to traditional architectures that do not downconvert the internal voltage supply. However, this would hold true only when all circuit blocks are operating at the steady state, which will not be the case during the startup. At startup, neither of the SCPCs are functioning since the clock is not generated yet. Hence, there will be numerous challenges to be addressed to perform cold startup. These challenges will be studied and addressed in Sections IV and V.

IV. Design and Analysis of Main Building Blocks

In this section, critical building blocks of the proposed energy harvester system are discussed in more detail.

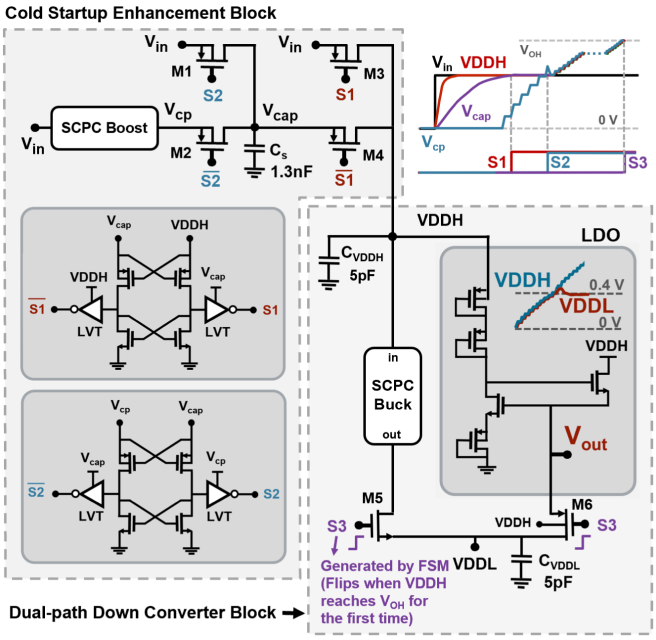


Fig. 6. Cold startup enhancement and the dual path down converter blocks.

A. Cold Startup Enhancement Block

The cold startup sequence is first explained in this section, and circuit details are presented next. Initially, when the BFC is connected to the chip, the feedforward path bypasses the boost SCPC (since no clock signal is available). This voltage path is then shorten through the cold startup enhancement block and the buck SCPC. Hence, the available voltage is delivered to the internal circuitry with minimized drop to maximize the chances of starting the low-voltage unit. The DCO and the FSM start operating, and the clock signals are sent to the level shifters. Through the mapping network, the clocking signals are delivered to both SCPCs. When voltage boosting starts, the FSM choses the boost SCPC over the feedforward path to use the increased supply for VDDH. At the same time, the buck SCPC keeps VDDL at 0.4 V. When VDDH reaches the voltage thresholds, the regulating switch starts delivering power to the load and the chip operates according to one of the three loading conditions mentioned in Section III in Fig. 2. The feedforward path is not directly connected to the low-voltage unit since the OC voltage of the BFC (V_{S}) is nonpredictable. If V_{S} is larger than 0.4 V, then the internal circuitry would burn excessive power, which would either shorten the lifetime of the BFC [17], [21], [23] or prevent the system to transit from cold startup to the steady state (because of excessive voltage drop across R_{S}). In fact, the dc–dc voltage down converter block ensures that VDDL never exceeds 0.4 V even if the source voltage is higher.

The cold startup enhancement block, shown in Fig. 6, consists of four low-V_{th} (LVT) PMOS switches to initially isolate VDDH from the output of the boost SCPC (V_{cp}) and the V_{cap} node with a 1.3-nF storage capacitor (C_{st}). These switches are controlled by two latch-based comparators that dynamically compare VDDH to V_{cap} and V_{cap} to V_{cp}, respectively. At startup, signals S1 and S2, as shown in Fig. 6,

are both zero so that the VDDH node is first pulled up to V_{in} by M3 and isolated from V_{cap} by M4 (V_{in} is the node after the source resistance R_S). Therefore, the SCPC is bypassed and the internal blocks start operating. At the same time, the storage capacitor C_{st} is being charged by V_{in} through M1, while V_{cp} is boosted by the SCPC. Once V_{cap} reaches V_{in} and V_{cp} reaches V_{cap}, S1 and S2 are toggled to ensure a smooth supply transition from V_{in} to V_{cp} for the VDDH node as soon as the boost SCPC and C_s are ready.

B. Dual-Path Down Converter Block

The dual-path down converter block works closely with the cold startup enhancement block. The first sub-block in the dual-path down converter is a low-dropout (LDO) voltage regulator. As shown in Fig. 6, the LDO can be modeled as a controlled high-pass filter, in which the output (VDDL) initially follows the input voltage (VDDH) and then gets regulated at 0.4 V. This block is used at startup, as soon as VDDH is pulled up to V_{in}, to deliver the initially available voltage to the internal circuitry in the low-voltage unit. The LDO is mainly designed to not rely on clocking signals at startup. Hence, the output of the LDO is shorted to VDDL through M6 with signal S3 which is initially zero.

The first critical sub-blocks that should start functioning with VDDL are the oscillators that start both SCPCs. As soon as these oscillators start, the level shifters convert the clocking signals levels to VDDH (which is equal to V_{in} at that moment). The clocking signals are then sent to both SCPCs through the switch mapping network. The settings of the mapping network are pre-programed to set the boost SCPC to a CR of 6, even before the FSM starts the MPPT. This CR_0 was chosen based on simulations in Section II as the closest initial guess to the correct CR for MPPT. Furthermore, this CR_0 ensures that VDDH reaches V_{OH} even though it might not be the optimum CR at steady state.

When the boost SCPC is clocked, VDDH starts rising above V_S. Since a similar architecture is used for all oscillators, they would start oscillating simultaneously. Therefore, while VDDH is being boosted, the FSM starts tracking it and the buck SCPC downconverts VDDH. The output of the buck SCPC is, however, isolated from the VDDL node initially through M5 and with signal S3, which is generated by the FSM. When VDDH reaches V_{OH} for the first time, the FSM toggles S3 to switch the down-conversion path from the LDO to the more power-efficient buck SCPC. The buck SCPC continuously multiples VDDH by 2/5 through cascading a standard $\times 1/5$ voltage divider with a voltage doubler.

The metal-insulator-metal (MIM) storage capacitor C_{st} is chosen to be larger than 1 nF, based on the requirements of a previously designed on-chip sensor in [11]. The size of C_{st} was limited by the chip area and was set to 1.3 nF. This relatively large on-chip capacitance also helps reducing the switching clock ripples at the VDDH node to lower than 5 mV. The ripple at VDDL due to the ripple at VDDH is also decreased by a factor of 0.4, which reduces the clocking ripples to lower than 2 mV. The additional ripples due to the DCO, the NOL clock generator, the MPPT FSM, and level shifters are negligible at the VDDL node. In fact, the 5-pF capacitor at the VDDL node (C_{VDDL}) is mainly chosen such that the transition from the LDO to the buck converter is smooth. The 5-pF capacitor at the VDDH node (C_{VDDH}) has only a role at startup when the boost SCPC is bypassed. It is chosen to be 5 pF to match C_{VDDL} such that when the LDO is effectively shorten (when VDDH $<$ 0.4 V), there will be minimized charge sharing losses between C_{VDDL} and C_{VDDH}.

C. Low-Voltage Digitally Controlled Oscillator (DCO)

The digitally controlled ring oscillator, shown in Fig. 7(a), operates at a minimum of 0.25-V supply voltage and provides clocking signals to the boost SCPC through the NOL clock generator, level shifters, and then the switch mapping network. It consists of two thyristor-based delay cells followed by an inverter buffer. In each delay cell, as depicted in Fig. 7(a), transistors M1 and M4 first reset the block with a pulse signal at their gates. Subsequently, the drain voltages of M2 and M3 start accumulating/dissipating charge through the sub-threshold leakage current paths that M1 and M4 provide. The outputs then switch through the positive feedback loop that is formed by M2 and M3. The duration of this transition (hence, the frequency of the oscillator) is adjusted by the binary-weighted branches of sub-threshold transistors. These branches provide leakage current paths driven by signals D0 through D3, which are controlled by the FSM. Minimum-size LVT transistors are chosen for M1 and M4 to minimize the overall power consumption while providing enough leakage current. M2 and M3 mainly operate in sub-threshold and are high-$V_{(th)}$ (HVT) to be more robust across process corners. It should be noted that the frequency tuning range would be lower than the theoretical $16\times$ with 4 control bits. There are several nonidealities in the design that should be considered. One major contribution to this nonlinearity is from the switch transistors (controlled by D0 through D3 in Fig. 7(a). Even when all switches are off, all branches would still contribute to the overall leakage current. Moreover, the control paths impose additional capacitance to the OUT_bar node in Fig. 7(a). The total capacitance at this node changes as the control bits are altered, which results in a change in charging/discharging time. In addition, increasing the number of the branches would eventually result in frequency saturation. This is primarily due to transistor M1 in Fig. 7(a) becoming the bottleneck of the leakage current. This could be improved by increasing the size of M1 (and M4), with a tradeoff for more power consumption and oscillation failure at lower supply voltages. In this work, since the lowest possible operating supply (0.25 V) is of main concern, the dimensions of M1 and M4 were minimized, which eventually resulted in a lower frequency tuning range. The outputs of this ring oscillator are two complementary impulse trains, the width of which are defined by the delays that the inverter buffers generate. To get clean clock signals with 50% duty cycles, both outputs are passed through two T-flip-flops. The thyristor-based delay elements burn less power than conventional inverter-based delay cells. The main reason is that the inputs of the thyristor-based cells toggle

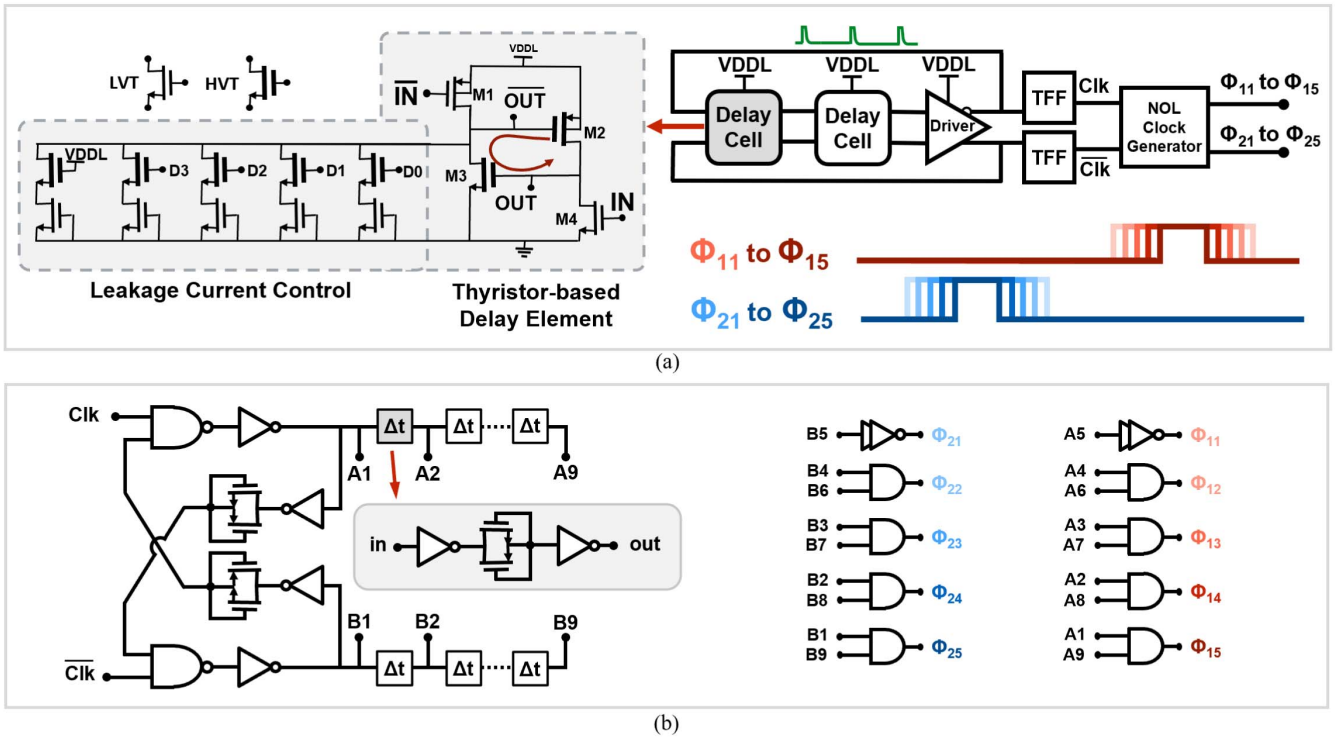


Fig. 7. (a) Schematics of the digitally controlled oscillator followed by the NOL clock generator. (b) Schematics of the NOL clock generator.

much faster than their outputs, hence, the short-circuit current is significantly reduced. Moreover, the thyristor-based delay cells are inherently slow (in contrast with inverters), due to their operation based on leakage current, which makes them excellent candidates for low-frequency oscillators.

The schematics of the NOL clock generator are shown in Fig. 7(b). All transistors used in this block are LVT to make sure the transitions are as fast as possible even at very low-voltage supplies. Any slow transitions in the waveforms would result in overlapping signals, which would decrease the boost/buck SCPC efficiency significantly and even preventing the harvester from performing cold startup.

D. Switched-Capacitor DC–DC Boost Converter

The boost SCPC consists of four stages of interleaved voltage doublers, each performing a $\times$ 1, +1, or $\times$2 operation. With this arrangement, all integer CRs (CR, which is equivalent to the gain G_1 in Section III) from 1 through 16 except for 11, 13, 14, and 15 are achievable. Fig. 8(a) shows the details of each stage. PMOS and NMOS transistors are used for both the high-side and the low-side switches for a minimal ON-resistance, especially when the switching signals have lower swings at startup. PMOS switches are avoided for ground connection of bottom plates of the flying capacitors since they provide a shorted path from V_{in} to the ground at startup. Each transistor is sized individually for an optimum ON-resistance, gate capacitance, and isolation (when turned off).

For an efficient performance, the switches of the SCPC should always be driven with VDDH-level clock signals. This is critical especially when a switch connects the output of a stage to the input of the next. Maximized gate voltages would bring switches to deep ON-/OFF-states to reduce voltage drops and leakage currents. It is also important to determine the order of level-shifting and distributing the clocking signals. The switch mapping network consists of fundamental logic gates that form a combinational logic FSM. Hence, its average dynamic power consumption scales quadratically with its supply voltage. It might seem reasonable to put the mapping network first, followed by the level shifters; however, the necessary number of level shifters would increase from 10 to 54 for the boost SCPC and 88 for the buck SCPC. A power optimization analysis is performed to choose the appropriate placement order of the level shifters and the mapping network. Considering the total number of SCPC switches and the average activity factor of all mapping network circuitry (which depends on the chosen CR), placing the level shifters first saves power by 40% [Fig. 8(b)].

E. Level Shifters

The level shifters are used to convert the voltage levels of several logic and clock signals from VDDL to VDDH, while maintaining the timing margins of the NOL clocks. The proposed level shifter circuit is shown in Fig. 8(c). At startup, when both VDDH and VDDL are below V_S, the input signal is passed through the LVT inverter path followed by the LVT buffer, since no level shifting is required, and transitions should be as sharp as possible. In fact, VDDH is initially pulled up to V_S and is then boosted toward V_{OH}, while the LDO and the buck SCPC keep VDDL at around 0.4 V.

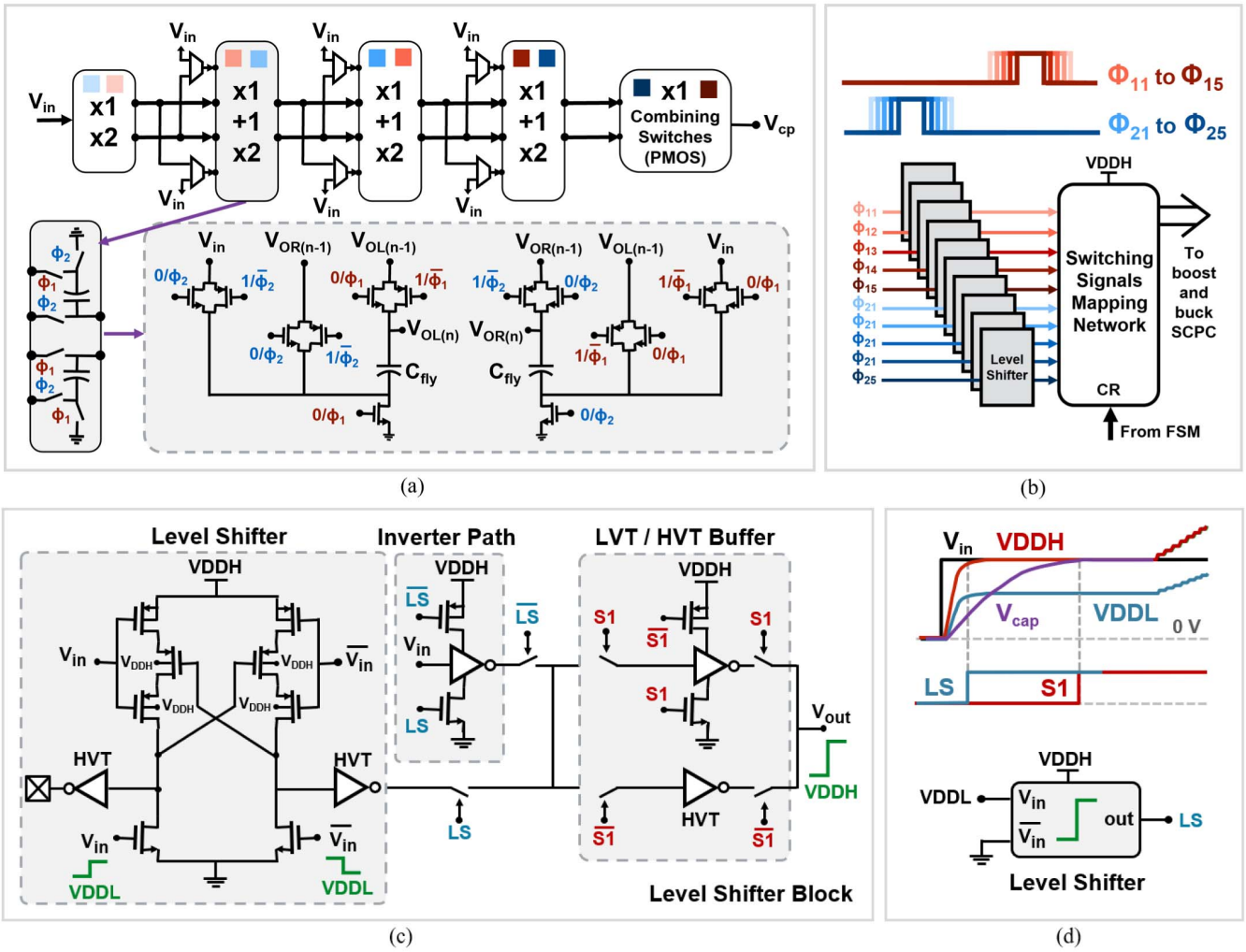


Fig. 8. (a) Schematics of the reconfigurable switched-capacitor power converter (boost). (b) Arrangement of the level shifters and the switch mapping network. (c) Schematics of the dual-path level shifters. (d) Generation of the LS signal through an identical level shifter with its input connected to VDDL. Signal S1 is generated by the comparison of VDDH and V_{cap} through a latched comparator.

This transition separates VDDL from VDDH gradually. It is desirable to choose the level shifter path over the inverter path as soon as a significant difference is detected between VDDL and VDDH. The level-shifter select (LS) signal in Fig. 8(c) is toggled to choose the level shifter over the LVT inverter path when this difference is detected. The details of generating the LS signal is discussed next.

The level shifter sub-block consists of a stacked and cross-coupled structure to enhance the gain. This architecture ensures that the level-shifting operation is feasible under all combinations of VDDL and VDDH from 0.4 to 1 V. For voltages below 0.4 V, due to its stacked structure, the level shifter will have a dead zone, in which the level shifting fails even if there is a difference between VDDL and VDDH. To tackle this challenge and change the path from the inverter to the level shifter at a correct moment, an identical level shifter with a fixed input of VDDL and a supply of VDDH is used to generate the LS signal for all other level shifter blocks [Fig. 8(d)]. A high output of this block ensures that all other level shifters will be ready to convert a signal with the current VDDL amplitude to VDDH.

As VDDH increases further, an HVT buffer is selected over the LVT buffer to prevent excessive dynamic short currents during each transition. Static power would also be slightly improved since subthreshold leakage currents of HVT transistors are smaller. The transition to the HVT buffer is made by the S1 signal generated by the latched comparator, comparing VDDH and V_S. It is worth noting that the toggling order of the LS and S1 signals could be exchanged according to different BFC OC voltages; however, the transition timings of the NOL clock signals will be maintained.

F. Hysteretic Controller

The hysteretic controller [Fig. 9(a)] consists of two clocked comparators that compare VDDH to V_{OH} and V_{OL}. Since V_{OH} and V_{OL} are not physically available to be compared to VDDH, an indirect comparison is performed. VDDH is divided by two separate voltage divider ladders to VDDH/d_1 and VDDH/d_2 as shown in Fig. 9(a). These ladders are programmable and are initially set to 2 and 11/6, respectively. Two comparators are used to compare VDDH/d_1 and VDDH/d_2 to a bandgap

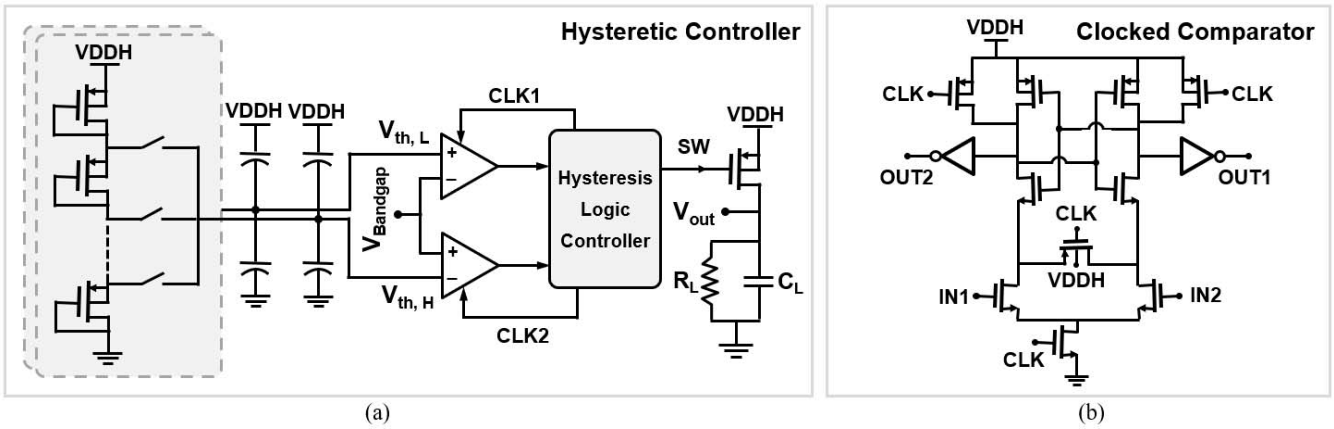


Fig. 9. (a) Hysteretic controller schematic. (b) Schematic of the clocked comparators used in the hysteretic controller.

voltage reference ($V_{\text{ref}} = 0.55$ V), which effectively makes the controller compare VDDH to $V_{\text{OH}} = d_1 \times V_{\text{ref}}$ and $V_{\text{OL}} = d_2 \times V_{\text{ref}}$. Depending on the loading conditions, VDDH is either kept between V_{OH} and V_{OL} or gets saturated (above V_{OL}). In this work, the ladders are designed to provide flexibility for choosing V_{OH} and V_{OL} with the minimum separation of 0.1 V for demonstration purposes. In general, this distance could be arbitrarily reduced and entirely set by the load requirements without compromising the harvesting efficiency. In fact, the separation of V_{OL} and V_{OH} could be reduced such that after each clock cycle, the boosted voltage is instantly delivered to the load (similar to [35]). However, in case the load is capacitive, there will be a significant drop in VDDH whenever the power is delivered to the load, due to charge sharing between the load capacitance and the internal storage capacitor of the harvester. Increasing the ripple of the VDDH node provides the advantage of tolerating these voltage drops to prevent the harvester from failure. It should be noted that the ripple on the V_{out} node is of our main concern, and not the VDDH node. In fact, V_{out} is the actual node that supplies the loads. As we recall from Fig. 2, depending on the loading conditions, along with the settings for VDDH ripple, the ripple of the V_{out} node could be entirely different.

A hysteretic controller logic block, which is another sequential logic FSM that is synthesized with HVT transistors, is used to receive inputs from both comparators to toggle the SW signal. The SW signal controls the hysteretic PMOS switch that connects the VDDH node to the load (V_{out}). The schematic of the clocked comparator is shown in Fig. 9(b). The frequency of the clock that enables the comparators should be sufficiently high such that they respond quickly when VDDH crosses V_{OH} or V_{OL}. To set the correct frequency for the comparators, two extreme cases should be taken into account; when the source is too powerful such that after each clock cycle, VDDH rises above V_{OH} from V_{OL} (at steady state), and when the load is too demanding such that when the hysteretic switch turns on, VDDH drops instantly below V_{OL}. In this design, the same clock frequency of the main MPPT FSM is used for the comparators.

V. MPPT and Source Degradation Tracing

The MPPT controller is an FSM synthesized with HVT transistors supplied by VDDL to reduce the dynamic and leakage power consumption. When the BFC becomes available, the input voltage is delivered to the low-voltage unit, including the MPPT FSM and its fixed-frequency clock generator. Following the first clock signal, a power-on-reset circuitry resets the FSM and all variables in the FSM are initialized. As shown in Fig. 10(a), the algorithm initially assumes the pre-programed CR of $\text{CR}_0 = 6$ and the lowest bit configuration (0000) for the DCO to prepare the SCPC to charge VDDH toward V_{OH}. Once VDDH approaches V_{OH} for the first time, the FSM switches the down conversion path from the LDO to the buck SCPC. If VDDH does not reach V_{OH} (if CR_0 is too high/low), a linear search for CR is performed until the first crossing occurs. The 2-D MPPT then starts by minimizing the storage capacitor charging time from V_{OL} to $V_{\text{OH}}(T_r)$ with a linear search for the optimum CR (coarse tuning) followed by the switching frequency (fine tuning). After finding the optimum CR and frequency, the circuit goes into the "Source Tracing" state. In this state, CR and the frequency will remain locked and T_r is continuously monitored to detect a noticeable change compared to the locked value ($T_{r,\text{Lock}}$). A dynamic threshold is introduced in the algorithm to always compare the latest T_r to $T_{r,\text{Lock}}/4$ (for detecting a 25% change). This threshold is set to ignore small changes in T_r which might be due to temperature fluctuations and/or other external perturbations. If a change is detected in T_r, which is presumably due to source degradation, the circuit will repeat the MPPT, starting from the latest locked CR and the minimum frequency. With this algorithm, any increase in the input power will also be detected (if more biofuel becomes available). In general, the number of clock cycles to lock to the new MPP depends on the locked CR (CR_{Lock}) and on how large the change is. In the case of BFCs, which degradation occurs gradually over a few minutes under heavy use, or several hours when occasionally used [23], the new CR would be either one step lower or higher than the locked CR. The new locked frequency could be different than the locked frequency by a maximum of 15 steps.

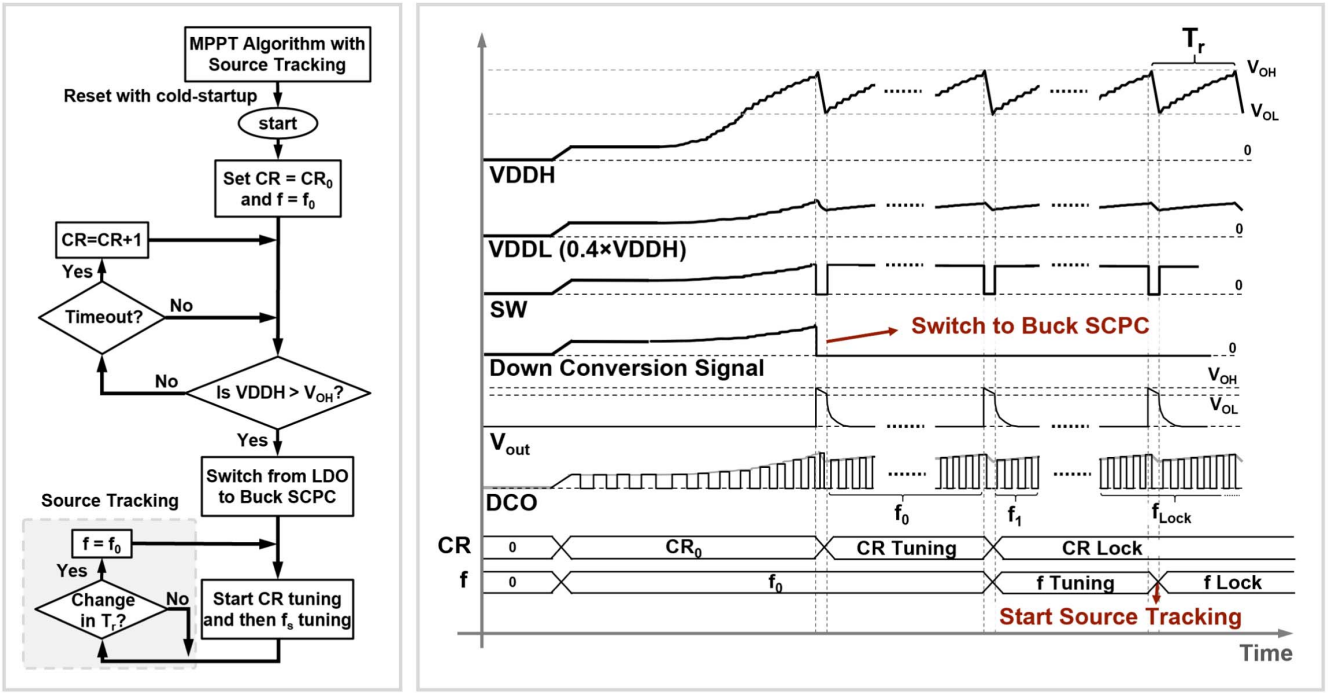


Fig. 10. (a) Flowchart of the proposed MPPT algorithm with source degradation tracing capability. (b) Timing diagrams of the important nodes of the harvester system while MPPT is being performed.

This results in a worst case of 20 tuning cycles, including the change detection. The total time of the re-tuning also depends on the distance of $V_{\rm OL}$ and $V_{\rm OH}$. For a 0.1-V ripple target, it would take approximately 4 ms for a worst-case scenario re-tuning, which is significantly shorter than the rate of BFC degradation.

Since VDDL is just the down-converted version of VDDH (at steady state), we would see a variation at VDDL with the amount of $(V_{\rm OH}-V_{\rm OL})\times 0.4$. As a result, the frequency of the DCO increases gradually as VDDL rises by approximately 60 mV during each cycle. However, since T_r is compared to the locked $T_{r,\rm Lock}$ by counting the clock cycles, rather than by measuring the actual time passed, this effect is canceled out. In fact, the source power determines how many cycles (and not how much time) it takes for VDDH to rise from $V_{\rm OL}$ to $V_{\rm OH}$.

VI. Measurement Results

The energy harvester chip is fabricated in a 65-nm CMOS process. The circuit performs cold startup and automatic MPPT with an input OC voltage of at least 0.39 V and an average input power ($P_{\rm in}$, defined as the maximum deliverable power) of 1.56 μW, as shown in Fig. 11(a). Peak power efficiency of 86% is achieved with 220 nW of internal power consumption.

Three more experiments are shown in Fig. 11. In one case [Fig. 11(b)], the input voltage is first decreased from 0.6 to 0.5 V to mimic a degradation in the BFC energy source while delivering power to an internal 60-kΩ test resistor. As shown in Fig. 11(b), the system first detects a change in the rise time of VDDH. Then the CR value and the switching frequency are modified to find and lock onto

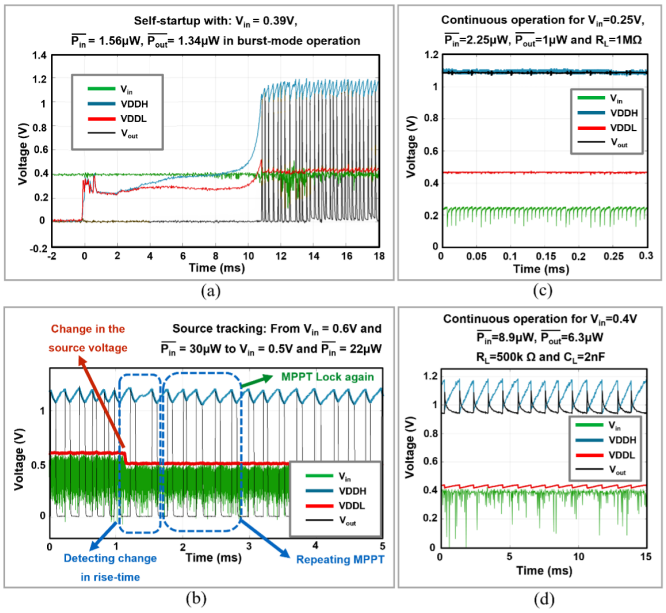


Fig. 11. Measurement results. (a) Cold startup in burst-mode sensing. (b) Source-adaptive MPPT. Continuous supply for $V_{\rm out}$ (c) when $P_{\rm Load} > P_{\rm out}$ and (d) when $P_{\rm Load} < P_{\rm out}$.

the new MPP. The chip has responded and locked onto the new MPP after a total of seven cycles, which has approximately taken 2 ms to demonstrate almost instant adaptation to source degradation. The loading condition for this case is set to mimic power-demanding burst-mode-operated sensors. In another case in Fig. 11(c), the output power is comparable to the loading condition (1 MΩ external resistor). The input

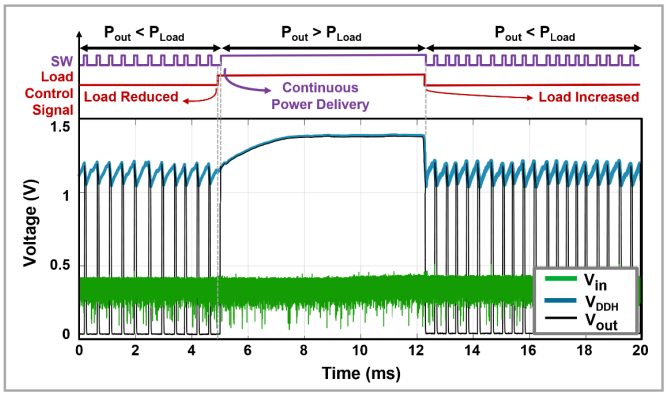


Fig. 12. Measurement results: transitions of different power delivery modes when load is changed over time ($P_{\text{Load}} > P_{\text{out}}$ to $P_{\text{Load}} < P_{\text{out}}$ and vice versa.

OC voltage is decreased to 0.25 V after MPPT lock and the average input power is set to 2.25 μW, while V_{out} settles to 1.01 V. In the last case [Fig. 11(d)], a continuous mode operation for a capacitive load is demonstrated, in which the instantaneous P_{Load} is more than P_{out}. VDDH is still regulated while V_{out} remains above 0.9 V.

In Fig. 12, another test case is shown to demonstrate the switching between power delivery modes. The system is initially locked at the MPP for an internal 60 kΩ test resistor with an input voltage of 0.4 V and input power of 12 μW. The load is then changed to an external 1-MΩ resistor. Since P_{out} becomes greater than P_{Load}, the power is continuously delivered to the load and the output voltage settles at 1.4 V until the load is changed back to the internal test resistor.

In an *in vitro* experiment, a pair of BFCs with a 2-mm diameter, similar to [23] is used to extract energy in a 20 mM lactate solution [Fig. 13(a)]. The OC voltage is initially 0.56 V with approximately 5.9 μW of average input power. The circuit performs cold startup and locks at the MPP with 3.1 μW of average power delivered to an internal 60-kΩ test resistor. The OC voltage degrades to 0.39 V after 10 min and then to 0.25 V after 30 min, while the chip continues its operation [Fig. 13(b) and (c)]. After 30 min, the system stops operating since the input voltage decreases below 0.25 V. In this case, the lifetime of the continuous operation could be improved using a more concentrated solution or larger electrodes.

The die micrograph and the printed circuit board (PCB) are shown in Fig. 14. The chip and the wire-bonds are encapsulated with polydimethylsiloxane (PDMS) to avoid short circuit connections when dipped into the lactate solution. A power efficiency plot for a V_S of 0.3 and 0.39 V at steady state is provided in Fig. 15(a). This plot shows a reliable operation over a wide range of output power. The end-to-end power efficiency is kept above 70% for loading powers from 1 to 12 μW, which verifies the compatibility of the energy harvester chip with BFC power levels. At higher average output power levels, a decrease in efficiency is observed, which is due to a transition to the continuous power delivery mode and an increase in VDDH (hence VDDL). This increase results in excessive internal power consumption and non-optimal overall efficiency. In Fig. 15(b), measured results for power

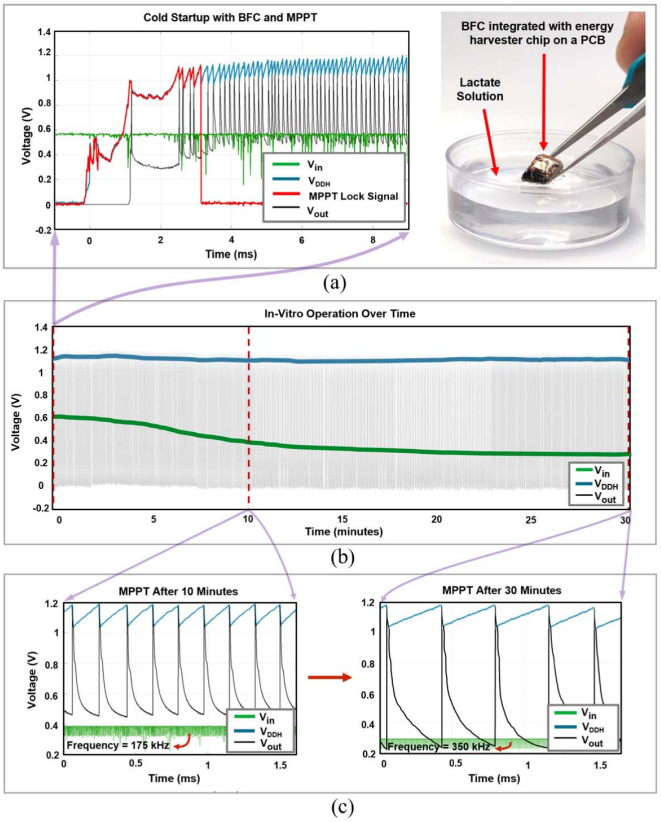


Fig. 13. (a) *In vitro* measurement test setup with lactate BFC, demonstrating cold startup and MPPT. (b) Harvesting operation with tracing the source OC voltage degradation from 0.56 to 0.25 V over 30 min. (c) MPPT lock after 10 and 30 min.

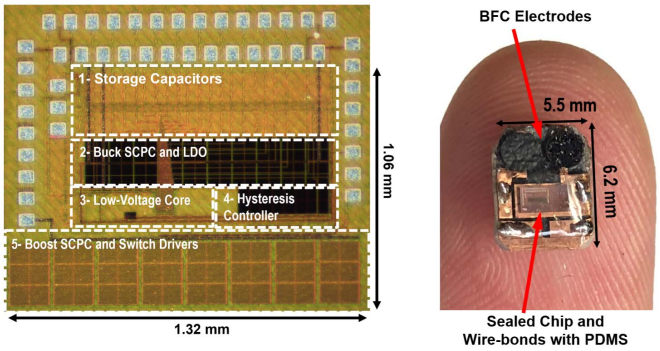


Fig. 14. 65-nm CMOS chip micrograph and the PCB with BFC and the chip.

efficiency versus various loading condition ratios are provided. The results show a flat efficiency response, which verifies that the performance is independent of loading conditions due to load regulation at higher loading ratios.

A power breakdown for the internal circuitry is provided in Fig. 16, for a 220-nW total average power consumption at the peak efficiency. A major portion of the power is consumed by the level shifters, which in fact, indicates that the total power consumption would have increased significantly, if the internal voltage supply had not been down-converted. In fact, the total internal power consumption is estimated to increase

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	JSSC'18 [24]	VLSI'15 [25]	JSSC'15 [26]	JSSC'18 [27]	JSSC'16 [31]	JSSC'18 [32]	TCAS-I'18 [35]	This Work
Technology	65 nm	0.18 µm	0.18 µm	28 nm	0.18 µm	65 nm	0.18 µm	65 nm
Fully Integrated	External Cap	External Inductor	10 µH Inductor	10 µH Inductor	Yes	Yes	Yes	Yes
Source Type	BFC	Solar Cell	PV	PV / TEG / BFC / Battery	TEG / PV	TEG / PV	PV	BFC
Topology	Duty-cycled	Inductive Buck/Boost	Inductive Buck/Boost	Inductive Buck/Boost	Boost SCPC	Boost SCPC	Boost SCPC	Boost + Buck SCPC
MPPT	Matched resisor	Manual	Yes	2D	2D	3D	2D	2D
Output Voltage (V)	0.3	1	1V, 1.8V and 3V	0.4 - 1.4	3.3	1	1.2 - 1.8	0.9 – 1.5
Input Voltage Range (V)	0.3 - 0.5	0.14 – 0.62	1	0.2 – 0.5	0.45 - 3	0.35 - 1	0.5 - 1.8	0.25 - 1
Min Cold startup (V)	0.3	0.33	No cold startup	Yes	2.1	0.35	0.72	0.39
Frequency Range	100 Hz	N/A	10 kHz	< 500 kHz	27 kHz – 1 MHz	19 kHz – 16 MHz	25 kHz – 1 MHz	100 kHz – 2 MHz
Throughput Power (µW)	400 – 800	10nW - 1µW	1mW – 10mW	1µW – 60mW	< 50	0.1 – 300	5.9 – 35.1	1 – 100
Peak Efficiency	N/A	84% @ 0.62V and P_{in}=1µW	83% @ 100µW	89% @ 20mW	81% @ 1.2V and 16µW	88% @ 0.85V and 200µA	72% @ 1.2V and 35µW	86% @ 0.39V and 1.34µW
Efficiency at BFC-level source power				76% @ 1µW	42% @ 0.6V and 1µW	70% @ 0.5V and 5µA	66% @ 0.9V and 6µW	80.4% @ 0.4V and 5.5µW
Chip Active area (mm²)	0.58*	9	4.62	0.5	2.89*	0.54	0.55	1.4

* Estimated from provided figures

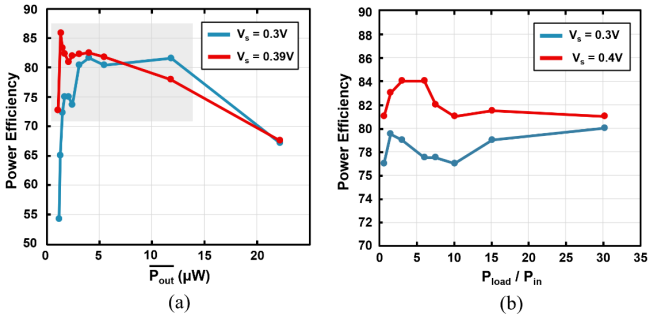
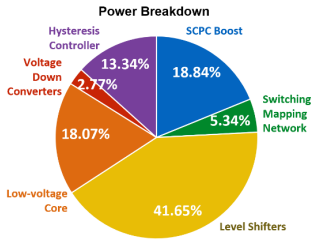


Fig. 15. (a) Measured efficiency plots of the energy harvester. (b) Measured power efficiency versus loading condition ratio.



- **Total internal power consumption at steady state: 220nW**
- **Estimated total power without voltage down-conversion: 370nW**
- **68% improvement in internal power consumption**

Fig. 16. Simulated power breakdown of the internal circuitry.

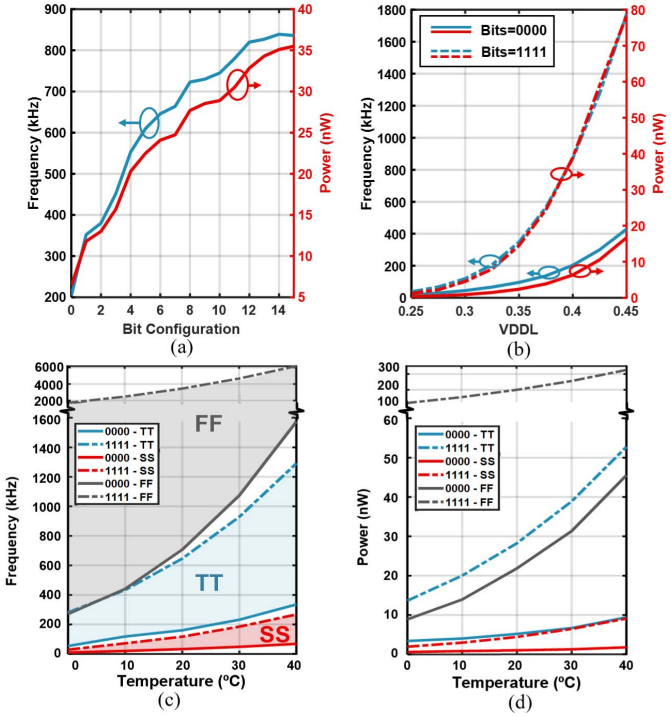


Fig. 17. (a) Measured DCO frequency and power consumption versus configuration bits. (b) Simulated frequency and power consumption of the DCO versus supply voltage for the lowest and highest bit configurations. (c) Simulated process and temperature variations for DCO frequency at bit configurations of 0000 and 1111. (d) Simulated process and temperature variations for DCO power consumption at bit configurations of 0000 and 1111.

by 68%, considering the power scaling of the low-voltage core for both dynamic and leakage power.

In Fig. 17(a), the measured frequencies and power consumptions of the DCO are provided at a 0.4 V supply for all configuration bits. The frequency range is measured to be approximately 600 kHz with highest at 836 kHz while dissipating 35.5 nW of power. In Fig. 17(b), simulated power consumption and frequency range of the DCO are provided when the voltage supply (VDDL) is swept from 0.25 to 0.45 V. The DCO stops oscillating at 0.25 V with lowest configuration bits, which can be improved by making the leakage current paths stronger at the lowest bit configuration. Fig. 17(c) and (d) shows process and temperature variation effects on the DCO frequency and power consumption at 0.4-V supply. The shaded areas in Fig. 17(c) show the covered frequency ranges by the DCO at each process

corner. For a more robust performance across process corners, the number of control bits could be extended to increase the overlap of the shaded areas. Furthermore, LVT transistors could be replaced with HVT with the tradeoff of oscillation failure at lower supplies.

VII. Conclusion

In this article, we present an energy harvester chip that performs cold startup with a minimum input voltage of 0.39 V utilizing a startup enhancement block. As the operation continues, the system can trace input voltage changes to as low as 0.25 V. Table I shows the overall performance of the energy harvester system in comparison with the prior art. The energy harvester chip achieves a superior efficiency with less than 0.4 V of input voltage and 5.5 μW of average output power.

Acknowledgment

The authors would like to thank the contributions of S. Sharma, S. Shah, and F. Aghlmand from Mixed-mode Integrated Circuits and Systems (MICS) Laboratory, California Institute of Technology (Caltech) and Caltech High-speed Integrated Circuits (CHIC) Laboratory, Caltech, members for their help with prototype printed circuit board (PCB) fabrication; and Muse Semiconductor for chip fabrication.

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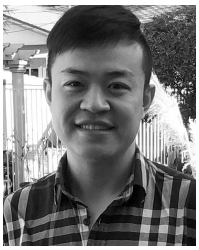

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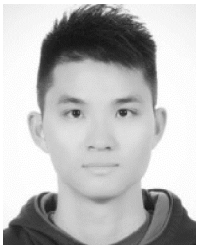

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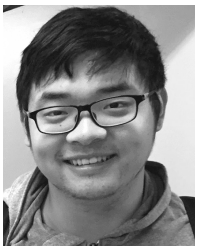

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