Multilayered Heater Nanocryotron: A Superconducting-Nanowire-Based Thermal Switch

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We demonstrate a multilayer nanoscale cryogenic heater-based switch (M-hTron) that uses a normal-metal heater overlapping a thin-film superconductor separated by a thin insulating layer. The M-hTron eliminates leakage current found in three-terminal superconducting switches and applies heat locally to the superconductor, reducing the energy required to switch the device. Modeling using the energy-balance equations and the acoustic mismatch model demonstrates reasonable agreement with experiment. The M-hTron is a promising device for digital superconducting electronics that require high fan-out and offers the possibility of enhancing readout for superconducting-nanowire single-photon detectors.

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I. INTRODUCTION

High-speed low-power nanoscale superconducting switches are essential for realizing superconducting electronic circuits. In recent years, there have been many attempts to develop electrothermal superconducting switches based on the destruction of superconductivity in a current-carrying nanowire, which leads to an impedance change to drive a load. One of these approaches uses a superconducting three-terminal device called a nanocryotron (nTron) [1–4]. In an nTron, a narrow nanowire, known as the gate, is connected to a wider superconducting nanowire, termed the channel, through a small constriction. Upon applying a current that exceeds its switching current to the gate, the constriction switches from the superconducting state to the resistive state. The normal domain quickly expands, suppressing superconductivity across the entire cross section of the channel and diverts the current in the channel to the load.

These devices have been successful in demonstrating fast nanoscale superconducting switches and have the advantage of a simple planar structure which is monolithically fabricated using a single thin layer of a superconducting film. However, they face significant challenges related to sneak current and low fan-out. In electrical circuits, sneak current is defined as any undesired leakage current that flows through unselected gates. Sneak currents have adverse impacts on power consumption and the reliability of electronic circuits.

Recently, a device based on nanowires has been developed that has no path for leakage current and uses thermal coupling to achieve switching behavior in the superconducting channel. This device, called the planar heater-nanocryotron (P-hTron) [5], is a thermal cryotron and is composed of a superconducting-nanowire channel that is galvanically isolated from an adjacent gate nanowire that serves as a heater. When the gate is biased with a current higher than its switching current, it becomes resistive and generates Joule heat, which raises the temperature of the channel and eventually makes it resistive. Because the heater is electrically isolated from the channel, the leakage-current problem of the nTron is eliminated. Similar to nTrons, the zero-resistance state and the high-resistance state can be considered the "1" and "0," respectively, for digital logic. In another thermal-coupling approach, a large-area normal-metal heater overlaps a meandered thin-film superconductor while being separated by a thin

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dielectric [6]. While this approach enables interfacing with high impedance loads, the device requires heating several square microns of superconductor and has only been demonstrated at approximately 1 K operating temperatures, limiting the switching speed of the device.

In this work, we study another type of hTron switch where the heater is placed on top of the superconducting channel and is electrically isolated from the channel by depositing a thin layer of an oxide film between the heater and the channel. We call this type of switch a multilayer hTron (M-hTron). The heater in an M-hTron is made of a normal metal that allows suppression of the critical current in the channel in a controllable manner. In M-hTron devices, the heater crosses over the superconducting channel; as a result, the heating in the channel is more uniform and local when compared to the P-hTron, where the heating gradually decreases across the width of the channel. This feature has the potential to increase the thermal coupling efficiency of M-hTrons and allows them to have a higher fan-out than P-hTrons. In this paper, we only present work on M-hTrons and, for simplicity, we refer to them as hTrons.

II. DEVICE FABRICATION

In the following section, we discuss the fabrication process of hTron devices. A multistep electron-beam lithography (EBL) process is used in combination with dry etching and lift-off processes to fabricate the hTron devices, as outlined in Fig. 1. In the first step, a 20-nm-thick NbN superconducting film is deposited by a reactive dc-magnetron sputter process on a sapphire (Al_2O_3) substrate. Then, 50-nm-thick Au marks are defined by a lift-off process on the NbN film using EBL at 100 kV. In the next EBL step, the superconducting channel is patterned on positive-tone electron-beam resist (ZEP 520A). The exposed resist is first developed in hexyl acetate at 0°C, is then dipped in IPA, and is blow-dried with N_2. The NbN layer not covered by the resist layer is then etched in CF_4 plasma at 50 W. To prevent the resist mask layer from overheating and hardening during the etching process, we perform the etching process in three steps, allowing the resist layer to be cool down for 2 min after 3 min of CF_4 etching. The resist layer is then ashed in oxygen plasma (100 W for 25 s) and removed by submerging the sample in Microposit Remover 1165 (N-Methyl-2-pyrrolidone) heated at 60°C. In the last EBL step, the heater element is defined on the top of the superconducting-nanowire channels using a lift-off process. In this step, we first deposit a 25-nm-thick layer of SiO_2 using an e-beam evaporation technique. Here, the SiO_2 film is used as an insulating layer to make sure that there is no electrical contact between the heater and the superconducting channel. Following the evaporation of the SiO_2 layer, a 30-nm-thick layer of Ti is evaporated. The lift-off is then performed in Microposit Remover 1165 at 60°C.

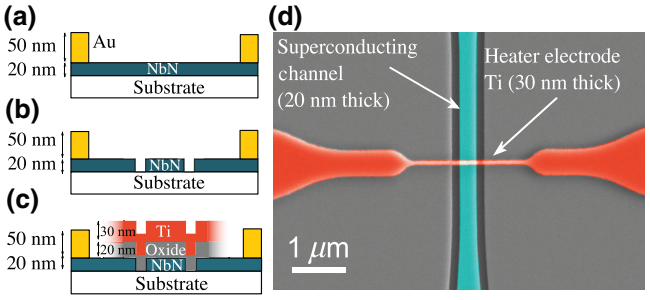

FIG. 1. A cross-section view of the fabrication process. After deposition of the NbN film, (a) Au marks are defined on a 20-nm-thick NbN film using a lift-off process. (b) The superconducting channel is then patterned on the NbN film using EBL and an RIE process with CF_4 gas. (c) A heater made of a 30-nm-thick Ti layer is defined on the top of superconducting channel. A 25-nm-thick layer of SiO_2 film is employed as a dielectric layer, isolating the heater and the channel. (d) A false-color SEM image of the final hTron device with the NbN channel shown in blue and the Ti heater shown in red.

The high-yield fabrication and reproducible results are closely associated with the quality of the interfaces as well as the oxide layer. For this reason, we fine tune every step of the nanofabrication processes to get high-quality interfaces between different layers and also make sure that we have a pinhole-free dielectric between the heater and superconducting channel. Figure 1(d) shows a colorized scanning-electron-microscope (SEM) image of a fabricated hTron device.

III. THEORY AND SIMULATION

To characterize the heat transfer in hTron devices, we formulate and solve heat-transfer equations in various device geometries. Several fundamental energy-relaxation processes governed by electron-electron (*e*-*e*), electron-phonon (*e*-ph), phonon-electron (ph-*e*), and phonon-phonon (ph-ph) interactions contribute to the heat transport in nanoscale devices at cryogenic temperatures. While, in general, these interactions can lead to complex dynamics, to simplify our approach, we neglect the details of nonequilibrium electron and phonon distributions in favor of the quasiequilibrium two-temperature model.

Heat transfer within the Ti heater is modeled using

$$C_e(T_e)\frac{\partial T_e}{\partial t} = -\Sigma_{e\text{-ph}}\left(T_e^5 - T_{\text{ph}}^5\right) + \nabla\kappa_e(T_e)\nabla T_e + \vec{j}\cdot\vec{E} \tag{1}$$

and

$$C_{\text{ph}}(T_{\text{ph}})\frac{\partial T_{\text{ph}}}{\partial t} = \Sigma_{e\text{-ph}}\left(T_e^5 - T_{\text{ph}}^5\right) + \nabla\kappa_{\text{ph}}(T_{\text{ph}})\nabla T_{\text{ph}}, \tag{2}$$

which form the basic two-temperature equations for the bulk of a normal metal. In Eqs. (1) and (2), T_e is the electron temperature, $T_{\rm ph}$ is the phonon temperature, C_e is the electron heat capacity, $\Sigma_{e\text{-ph}}$ describes the electron-phonon coupling strength, κ_e is the electron thermal conductivity, $\vec{j} = \sigma\vec{E}$ is the current density, σ is the conductivity, $\vec{E}$ is the electric field, $C_{\rm ph}$ is the phonon heat capacity, and $\kappa_{\rm ph}$ is the phonon thermal conductivity. Note that the temperature dependencies of the heat capacities and thermal conductivities are included in this formulation. The SiO_2 spacer layer is treated in a similar way to Eq. (2) but with electron-phonon interactions neglected and the heat capacity defined according the Debye model. The description of the superconductor system follows the approach of Vodolazov [7] using Eqs. (30)–(32) therein, under the simplifying assumption that the magnitude of the superconducting order parameter is equal to its equilibrium value for the current value of the electron temperature $\Delta(t) = \Delta_{\rm BCS}[T_e(t)]$. Furthermore, we use the phenomenological approach of Ref. [8] to describe the current distribution in the superconductor and Joule heating. While this neglects the details of vortex formation and motion, which could be captured by a time-dependent Ginzburg-Landau (TDGL) approach, the computational complexity of solving the TDGL equations makes them impractical for calculations of large three-dimensional (3D) geometries over many nanosecond time scales. The phenomenological approach has been demonstrated to capture the main electrothermal physics of superconducting nanowires [9–11], which is the regime of interest in the current study.

A constricted region is included in the model by defining a length of 40 nm where the switching current is given by a fit to the experimentally measured switching current. Elsewhere in the NbN channel, the switching current is given by the theoretical depairing current, which is approximated using the Bardeen temperature dependence and the zero-temperature value calculated from the Usadel equations [12].

Heat fluxes at the interfaces between materials are determined using the acoustic mismatch model (AMM), following the approach of Kaplan [13], leading to boundary conditions of the form

$$\kappa_1(T_1)\nabla_\perp T_1 = -\frac{G_{12}}{4}\left(T_1^4 - T_2^4\right), \tag{3}$$

where T_1 and T_2 are the local phonon temperatures of the two materials at the interface, $\kappa_1(T_1)$ is the local phonon thermal conductivity at the interface, $\nabla_\perp$ indicates the outward gradient in the direction normal to the interface and G_{12} describes the boundary conductance. Interfaces with the vacuum are assumed to be perfectly insulating and the substrate is assumed to remain fixed at the bath temperature ($T_{\rm sub}$). A block diagram of this thermal system is shown in Fig. 2. Additional details and simulation parameters can be found in Appendix A.

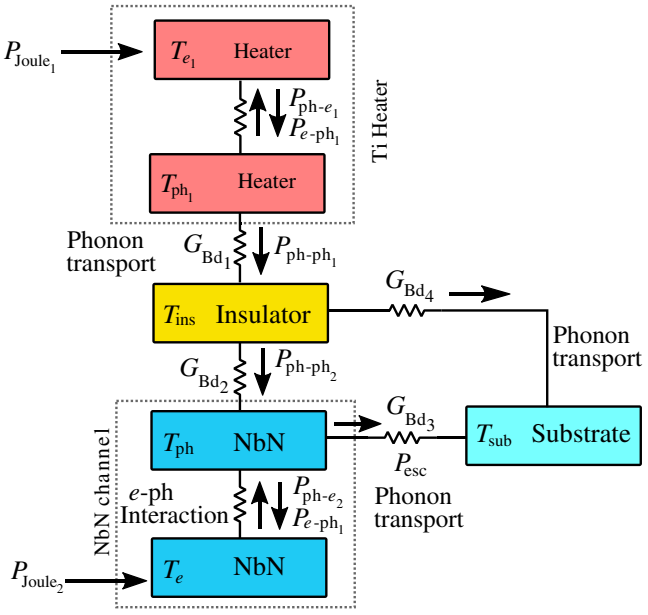

FIG. 2. The block diagram of the electrothermal model. The electron and phonon systems of the Ti heater and NbN channel are coupled by electron-phonon interactions. Each of these electron systems can be heated through Joule dissipation. The phonon systems of the heater, insulator, and channel are coupled by boundary resistances. The insulator and channel are also coupled by boundary resistances to the substrate, which remains at a fixed temperature.

In the model, two current sources determine the bias conditions of the hTron, as shown schematically in Fig. 3(a). A time-dependent current source [$I_H(t)$] governs the current flow in the heater. The superconducting channel is electrically connected in series with an inductor (L) and the combined inductor and channel are connected in parallel with a load resistor (R_L). This circuit is driven by the bias-current source ($I_{\rm Ch}$).

The nonlinear set of coupled partial differential equations is solved in a 3D geometry using the finite-element method. The geometry of the simulated system matches the experimentally fabricated devices. In the simulation domain, the insulator and heater cross perpendicular to the superconducting channel, as shown in Fig. 1(d), and maintain the topography of the step edge at the channel as shown in Fig. 1(c). Maintenance of this step edge necessitates the use of a 3D finite-element solver. In the 3D geometry, interfaces of the channel, dielectric, or heater that are not in contact with each other or the substrate are assumed to be perfectly insulating.

During operation, as current passes through the heater, Joule heating first heats the electron system of the Ti. This heat couples to the phonon system and couples to the phonons of the dielectric spacer. Eventually, this heat is coupled to the phonon system of the superconductor and, through electron-phonon interactions, to the electron

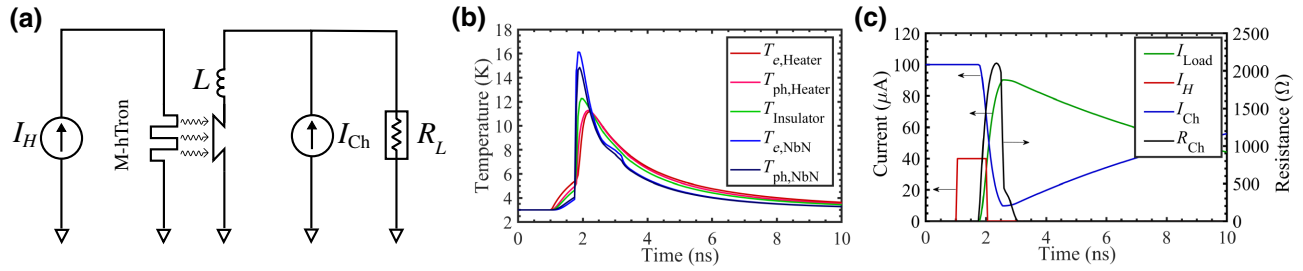

FIG. 3. (a) The schematic circuit for simulating hTron performance. The heater current source I_H dissipates energy in the hTron resistor, increasing the temperature of the superconducting channel. When this heat drives the hTron channel to the normal state, the appearance of a finite resistance diverts current to the load, modeled as a 50Ω resistor. The time-dependent (b) temperature response and (c) electrical response of the hTron. Once the heater current activates, the temperature of the system increases. Thermal boundary resistances and heat capacities lead to a lag between when the NbN temperature increases compared to the heater. Once the NbN electron temperature exceeds the current-dependent critical temperature, the channel switches to the normal state and the Joule heat from the NbN rapidly increases the temperature of the device. The heater width is 500 nm, the channel width is 600 nm, the heater current is a 1-ns-long 40 μA pulse, the channel bias current is 100 μA, and the substrate temperature is 3 K.

system, which suppresses superconductivity. When the temperature of the superconductor surpasses the current-dependent critical temperature of the superconductor, the superconductor switches to the normal state and Joule heating expands the normal domain along the length of the channel. Figure 3(b) shows an example simulation of the time evolution of the temperature of the system for a 1-ns current pulse in the heater. The delay caused by heat passing through the multiple thermal boundary resistances and due to the heat capacities of these layers causes a lag between the onset of current in the heater and the formation of resistance in the superconducting channel, as seen in Fig. 3(c). The reset properties of the superconducting channel are determined by the series inductance and load seen by the device and the duration of the current pulse through the heater. For short pulsed heat sources, self-resetting can be achieved through proper selection of the L/R_L time constant or biasing of the device below the retrapping current.

IV. EXPERIMENT

A schematic representation of the experimental setup for characterizing the hTron devices is shown in Fig. 4(a). The unfamiliar schematic symbol represents the hTron device. The bias current through the superconducting channel is provided by an arbitrary waveform generator (Keysight 33622A) and a room-temperature resistor, R_{bias}, connected in series with the channel of the hTron. The current flow in the channel is determined by measuring the voltage drop across the known R_{bias} using an oscilloscope (LeCroy WaveRunner 620zi) and applying Ohm's law. The gate

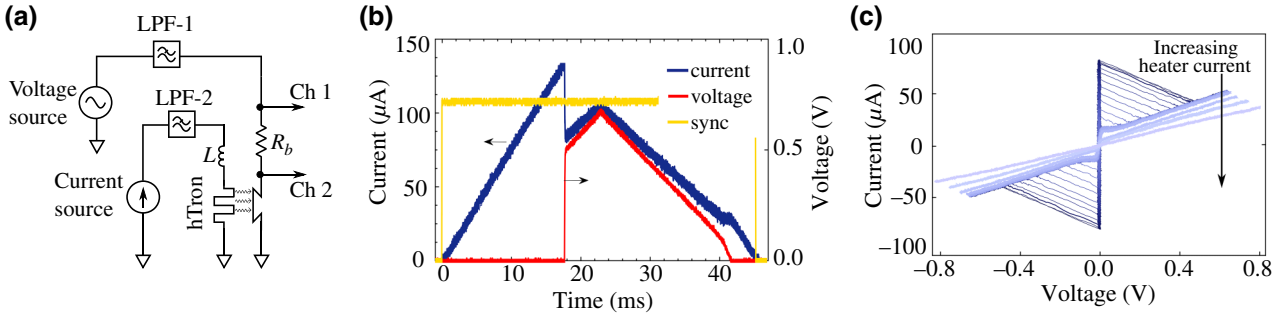

FIG. 4. (a) The schematic circuit diagram of the measurement setup for characterizing hTron devices. The device is held at the base temperature in a cryostat. The arbitrary-waveform generator (Keysight 33622A) in series with a bias resistor, R_{bias}, and a low-pass filter are used to bias the superconducting channel. The current signal from a low-noise current source (Yokogawa GS200) is sent to the heater. (b) Example data traces from the acquisition procedure. The blue line is the applied bias current to the superconducting channel and is calculated by measuring the potential difference across the bias resistor, R_{bias}. The red line shows the voltage across the channel. The output voltage appears on the oscilloscope (LeCroy 610ZI) once the bias current exceeds the switching-current value of the channel. The time difference between the sync signal of the AWG (yellow) and the switching time (red) can be translated to the switching current through knowledge of the ramping slope of the input current. The heater is biased at a fixed current value during this measurement. (c) The I-V characteristics of a hTron for different values of the heater current. The channel-switching current decreases as the heater current increases.

of the hTron is biased by a low-noise dc current source (Yokogawa GS200) in series with a low-pass filter (BLP-1.9+, dc, −1.9 MHz). Figure 4(b) shows the time trace of the current and voltage signals of the hTron recorded with the oscilloscope when there is no current applied to the gate port. All characterizations are conducted in a well-shielded closed-loop cryostat with a base temperature of 3 K. The current-voltage (I-V) characteristics of the hTron device as a function of the gate current, I_g, are shown in Fig. 4(c). This device is made of a 20-nm-thick NbN film and has a channel width of 600 nm. The switching current, I_c, of this hTron when there is no current applied to the gate is about 120 μA.

Figure 5(a) shows the switching current and retrapping current (I_r) of the channel as a function of the gate current for the same hTron device with a channel width of 600 nm. It can be seen that for $I_c > I_r$, the retrapping behavior and the retrapping current are not substantially modulated by the applied gate current. However, once the switching current is reduced to the retrapping current due to increasing gate current, the I-V curve for the channel does not have a hysteretic behavior during the transition from the superconducting state to the normal state and therefore the switching and retrapping currents are suppressed together as the gate current increases. In Fig. 5(b), we present the measured I_c and I_r as a function of the device temperature for the same hTron with zero gate current.

We compare these results to the predictions of the electrothermal model of the hTron under steady-state operation in Fig. 5(a), finding reasonable agreement between the model and experiment. To define the switching current of the constricted region of the superconducting channel, we fit the experimentally measured temperature-dependent switching current using the function $I_c = 126.6\left[1-(T/T_c)^3\right]^{2.1}$ μA, shown in Fig. 5(b). All other material and interface properties are estimated from literature values or measured experimentally and these details can be found in Appendix A. In this steady-state measurement, the relationship between the heater current and the switching current originates from an increase in the channel temperature due to a balance between the Joule heating of the heater and the thermal boundary resistance between the channel and the substrate. When diffusion is neglected, this takes the analytical form described in Appendix B by Eq. (B6).

We further investigate the influence of the superconducting channel width and gate width on the performance of hTron devices. In the first experiment, we fabricate several hTron devices with channel widths varying from 600 nm to 9600 nm, with the heater width fixed at 500 nm. Figure 6(a) shows the normalized switching current as a function of the heater current for hTron devices with widths of 600 nm, 3200 nm, and 9600 nm. At low heater currents, the switching current of the hTrons with wide channels shows a plateau, which means that the heater current does not modulate the switching current of the channel. This plateau can be explained if the location within the channel that causes switching, either due to a constriction or from current crowding at the bends of the wire, is not located directly underneath the heater. In this case, with small increases in temperature from the heater, the switching current is still limited by the constriction outside the heater region and the device switching current will not be modulated. Only when the temperature of the channel underneath the heater increases to the point where this section of the channel becomes the weakest current carrying region will further increases in the heater current reduce the channel switching current. This experiment demonstrates that the amount of

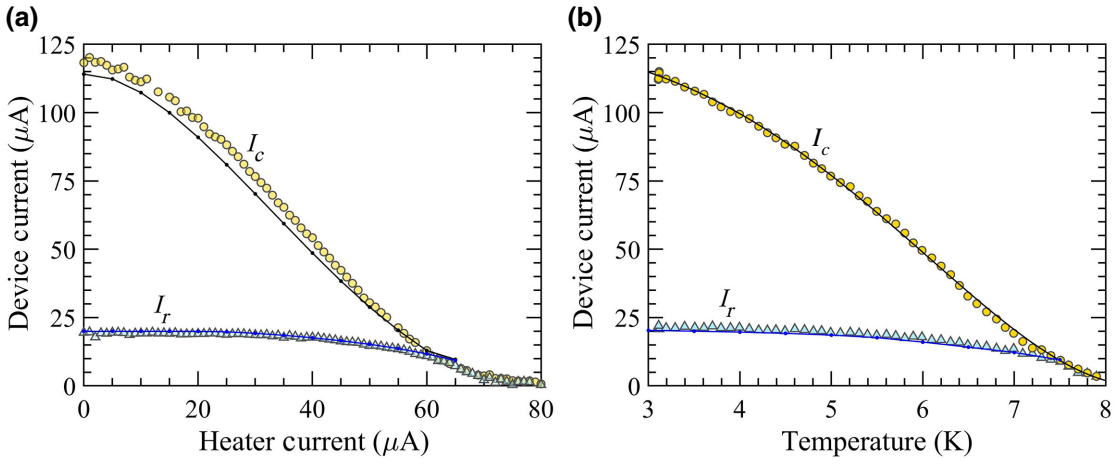

FIG. 5. The switching current (yellow circles) and the retrapping current (blue triangles) of a hTron with a channel width of 600 nm and a heater width of 500 nm as a function of (a) the heater current and (b) the temperature. The model predictions of the switching current (black line) and the retrapping current (blue line) are shown for comparison. The temperature-dependent switching current of the model is a fit to experiment.

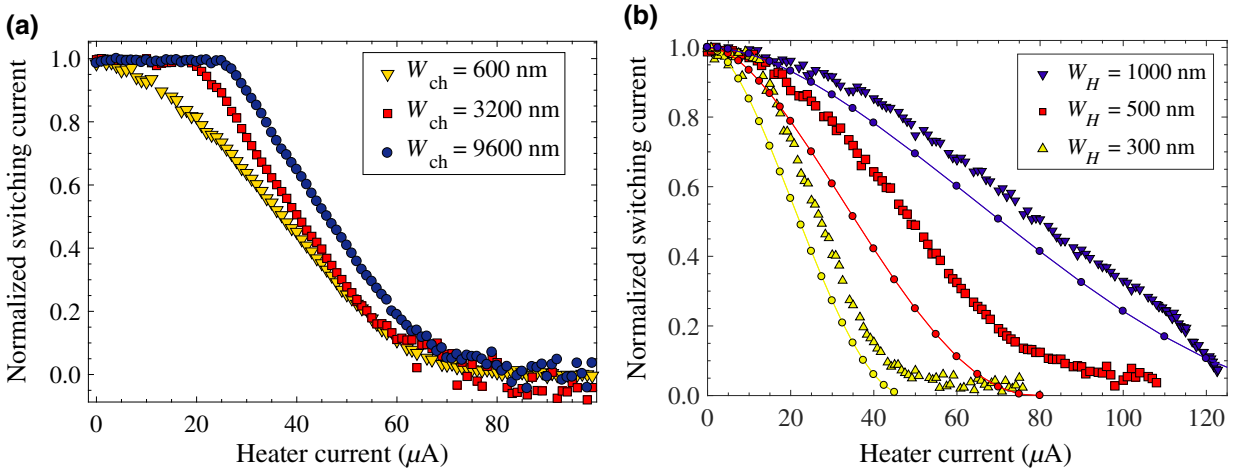

FIG. 6. (a) The normalized switching current of hTrons with channel widths of 600 nm, 3200 nm, and 9600 nm as a function of the heater current. The width of the heater is kept at 500 nm for these devices. (b) The normalized switching current of hTrons (symbols) with heater widths of 300 nm, 500 nm, and 1000 nm as a function of the heater current. The channel width is kept at 200 nm for these devices. Predictions from the electrothermal model (lines) are shown for comparison.

current required to suppress the switching current of each device is only slightly higher for the 9.6-μm-wide channel when compared to the 600-nm-wide one. From that, we can infer that the heater generates a very local region of increased temperature in the superconductor and that the heating power deposited per unit length is not a strong function of the channel width.

Additional devices are fabricated that probe the impact of the heater width on the switching behavior of the hTron devices. We fabricate a number of hTron devices with channel widths of 600 nm and heater widths varying from 300 nm to 1 μm. The normalized switching current of these hTrons as a function of their heater current is shown in Fig. 6(b). At a specific current, the deposited energy (as Joule heating) is the highest for the hTron with the narrowest heater width. This is expected, since the narrow heater geometry leads to a higher resistance and a higher current density within the heater.

V. FUTURE APPLICATIONS

There are several applications where introduction of the hTron offers the possibility of performance benefits over traditional techniques involving Josephson junctions and other types of superconducting switches. The hTron offers several advantages including high gain, no leakage current between the gate and channel, the ability to drive high-impedance loads, the possibility of large fan-out, and robustness to magnetic fields [1–5]. These properties make hTron devices an excellent choice that can provide the necessary on-chip platform to interface superconducting circuits involving superconducting single-flux quantum (SFQ) electronics to room-temperature control systems.

In one application, we use hTrons to build a scalable superconducting memory cell [14]. The schematic of an hTron-based memory cell is depicted in Fig. 7 and consists of two hTrons in parallel, making a superconducting loop. This memory cell stores bits "0" and "1" in the form of a clockwise or counterclockwise persistent current in the loop, respectively. Since there is no Ohmic loss in the superconducting loop, the state of the memory is secured and requires no refresh operation. For this loop to act as a memory, two main conditions need to be satisfied. First, the switching current of one of the hTrons must be smaller than that of the other one ($I_{c1} < I_{c2}$). Second, the inductance of the part of the loop with a smaller switching current must be lower than that of the other part ($L_1 < L_2$). For details of the memory-cell operation, see Ref. [14]. The memory cell based on the multilayer hTron is more scalable than that based on the planar hTron [5]. While the planar cell requires only a single layer for solitary devices, scaling requires compact via interconnects between thin superconducting films, while the multilayer approach does not require any vias. Furthermore, the minimum feature size of the planar cell is smaller than that of the multilayer cell, making yield over a large area more difficult.

The hTron also shows promise as a preamplifier for superconducting nanowire single-photon detector (SNSPD) readout. When operated in this configuration, the heater element of the hTron would act as the load of an SNSPD circuit while the channel of the hTron carries current that is diverted into a traditional rf amplifier as shown in Fig. 8(a). The hTron could be capable of increasing the amount of current diverted into the amplifier, which can increase the signal-to-noise ratio of the electrical pulse and reduce the noise contribution to timing jitter.

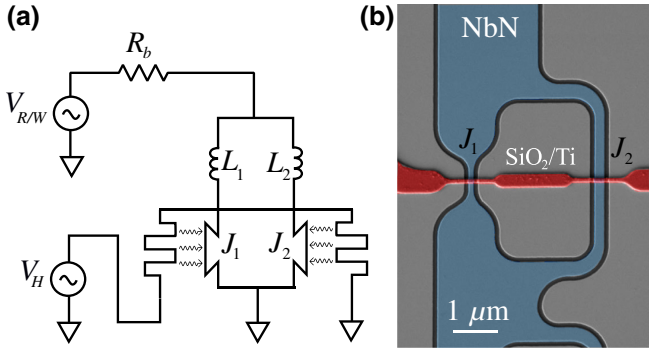

FIG. 7. (a) The schematic circuit presentation of a memory cell using two hTrons in parallel. The cell has a narrow constriction on one side and a wider constriction on the other. The heater is used as the cell-select port by lowering the switching current of both hTrons. This memory cell requires only one port to perform read-write operations and stores information in the form of the persistent loop current. (b) A false-color SEM image of a memory cell using hTrons, where blue indicates the superconductor while red indicates the heater.

The use of the hTron for this application is simulated using the same material parameters as used throughout this work for a channel width of 1 μm. As shown in Fig. 8(b), when a 300-nm-wide heater is used, a current amplification factor of 7 can be achieved for a current pulse resembling the output of an SNSPD with a bias current of 25 μA and a kinetic inductance of approximately 660 nH. Optimization of the material properties and device geometry can improve this value and reduce the amount of bias current and SNSPD inductance required to switch the hTron channel. In practice, the amplification factor that can be attained is limited by the reset dynamics of the SNSPD. Due to the finite resistance of the normal domain generated during photon detection (typically a few kilo-ohms), the heater resistance must be a small fraction of the normal domain resistance in order to ensure shunting of current from the nanowire during photon detection. Furthermore, the heater resistance contributes to determining the electrical reset of the SNSPD ($\tau_{\text{Reset}} = L_k/R_H$), and too large a resistance may induce latching [10]. Here, L_k is the kinetic inductance of the SNSPD and R_H is the heater resistance, which acts as the load impedance of the device. When operating an hTron as an SNSPD preamplifier, one must also consider the implications of signal-propagation delay and thermal-coupling jitter on the timing performance of the hTron. Experimental characterization of these effects is needed to fully evaluate the benefits of using an hTron for SNSPD signal amplification.

It is well known that shunted superconducting nanowires can be operated in an electrothermal relaxation-oscillation regime [10,15–17], where the feedback from the circuit causes the nanowire to regularly switch from the superconducting to the normal state. It is only recently that experimental work has demonstrated that these devices exhibit frequency lock-in to a driving microwave signal [18]. The local heating generated by the hTron means that the relaxation oscillation can be locally tuned and this enables the operation of many such devices on a single chip. To demonstrate this principle, we simulate the electrothermal response of a hTron with a 10Ω shunt resistor for different values of the heater current. As seen in Fig. 9, the response frequency can be tuned dramatically, demonstrating the promise of the hTron as a tunable relaxation oscillator.

VI. DISCUSSION

The combination of theoretical and experimental investigation provides considerable insight into the operation of hTron devices. When considering the results of the model,

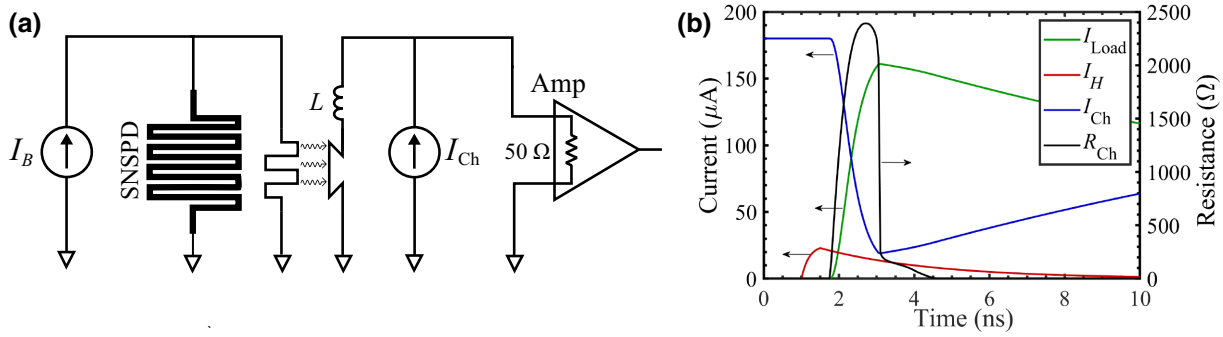

FIG. 8. (a) The schematic circuit for using the hTron as a preamplifier for SNSPD readout. The heater resistor of the hTron acts as the load resistor of the SNSPD. When the hTron switches, the channel current is diverted into an rf amplifier. (b) The simulated hTron response when operated as an SNSPD preamplifier. The channel width is 1000 nm, the heater width is 300 nm, and the channel bias current is 180 μA. The total resistance of the heater, including contacts, is 220Ω and the series inductance of the hTron channel is 1 μH. The red curve indicates the heater current and represents an SNSPD-like pulse, the blue curve shows the current through the hTron channel, and the green curve shows the current diverted to the 50Ω load of the hTron channel. The black curve shows the channel resistance. The simulated device achieves a current gain of 7.

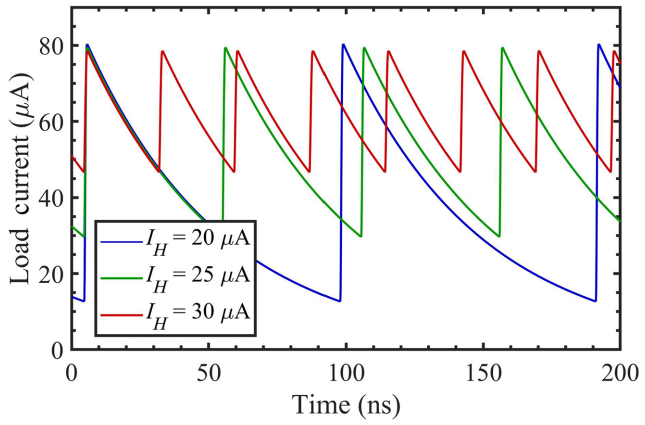

FIG. 9. The simulated hTron response when operated as a tunable oscillator. The channel width is 600 nm, the heater width is 300 nm, and the channel bias current is 90 μA. The total resistance of the heater, including contacts, is 220Ω and the series inductance of the hTron channel is 500 nH. The load resistor is 10Ω. The blue, green, and red curves show the current through the load resistor for heater currents of 20 μA, 25 μA, and 30 μA, respectively. As the heater current increases, the oscillation frequency increases.

it is important to emphasize that the only free parameters used in the fitting procedure are used to define the temperature-dependent switching current, which is directly extracted from experiment. The heater-current dependence of the switching and retrapping current is primarily influenced by the thermal boundary conductance of the interfaces, which is extracted from literature values of material properties and the AMM, which is not used as a fitting parameter. Given the uncertainty in properties such as the interface boundary resistance and the diffusion coefficient, the fitting between experiment and model shown in Fig. 5(a) is surprising. A better fit to the experimental switching current as a function of the heater current can be achieved by making a correction to the interface resistance between the NbN and the sapphire but our goal is to demonstrate the qualitative accuracy of the model and its usefulness as a design tool, not to attempt to extract an estimate of the boundary resistance.

Proper design requires a thorough understanding of the effects of heater and channel width on device performance. When considering the channel width, it can be recognized from Fig. 6(a) that as the channel width increases, a plateau region forms in the switching current at low heater currents. This means that for low heater currents, the increase in temperature caused by the heater does not impact the switching current of the channel, in contrast to the expectations based on the model. One possible explanation is that the superconductivity of the channel is suppressed somewhere outside of the region directly beneath the heater, so that local heating of the channel in this area does not initially affect the switching current. Eventually, sufficient heat is dissipated by the heater to increase the local temperature of the channel, so that switching is caused in the region directly beneath the heater and the switching current decreases with an increased heater current, as expected. With proper design and improvements in fabrication, this plateau is expected to be eliminated.

Similar arguments can be used to understand the impact of the heater width on the device performance shown in Fig. 6(b). For a given heater current, as the heater width is reduced, the current density increases, leading to more dissipation per unit area. Therefore, a smaller heater current is required to achieve the same amount of Joule heating per unit area. If plotted as the heater current density rather than heater current, the curves from the three devices do not directly overlap as might be expected but they are reasonably close given fabrication nonuniformity. The model predictions for the switching currents of these devices underestimate the heater current required to suppress superconductivity in the channel. There are several explanations for this discrepancy. Apart from the previously stated concerns of uncertainties in the boundary-resistance parameters for the interfaces, the temperature-dependent switching current is not calibrated and is assumed to have the same temperature dependence as the device shown in Fig. 5. Furthermore, the sheet resistance of the Ti heater is not measured for this fabrication run. A slightly thicker Ti heater due to deposition uncertainty would lead to lower current densities for a given bias current and shift the model predictions to higher heater currents, leading to better agreement with experiment.

The design and fabrication of the hTron is not restricted to the Ti and NbN material systems for the heater and channel, respectively. Depending on the application, there can be advantages to using a lower-T_c superconductor. For a given size of channel, a lower-T_c material will require less energy to break superconductivity, increasing the sensitivity of the hTron. This can be particularly important for applications where only a small amount of heater current is available to drive the channel normal, such as SNSPD readout. The heater material must be chosen to achieve an appropriate load for the circuit that drives the hTron. To match to a 50-Ω transmission line, a lower-resistivity material such as Au-Pd might be needed in order to maintain a narrow heater geometry across the channel. Attention must also be paid to the acoustic properties of these materials. In order to maximize the heat transfer from the heater to the channel and thus to maximize device sensitivity, an ideal heater material would be acoustically matched to the dielectric and the dielectric would be matched to the channel. The channel would be poorly matched to the substrate in order to trap the energy coupled from the heater. When thermal coupling from the heater is poor, additional energy is lost through diffusion in the heater leads, which reduces the device efficiency. The channel geometry must also be optimized to match the

requirements of the load it is intended to drive. For a given material, by using a thinner channel, the sheet resistance increases, which increases the impedance of the channel in the normal state, but this also decreases the critical current of the device. Similarly, a narrower channel has a higher normal resistance and requires less energy to switch but it also has smaller critical current.

Optimization of these devices requires balancing all of these device properties while considering the constraints on the maximum acceptable heater resistance and the load that the hTron must drive. While certain approximations can simplify this analysis (see Appendix B), the optimization problem is generally nontrivial. While the time-dependent validity of the model is not verified experimentally, the steady-state performance is sufficient to estimate the approximate amount of heat needed to switch the superconducting channel. Overall, the model described here can be used to judge the feasibility of hTrons for particular applications and optimize device performance once the material and interface properties are sufficiently well characterized.

As a final consideration, the cryogenic environment can play an important role in hTron performance. All of the measurements performed in this work are made with the device exposed to vacuum. If used in a wet system, the interface between the heater and liquid helium acts as an additional dissipation channel and lowers the efficiency of the heater by allowing thermal energy to couple to the helium rather than the channel. Similarly, if a passivation layer is used to protect the top surface of the entire device, heat can diffuse in all directions through the passivation layer rather than being directed preferentially to the channel. For optimal performance, the heater material should be chosen such that passivation is not necessary to prevent degradation over time.

VII. CONCLUSION

As cryocooler technology continues to improve and the use of superconducting detectors and circuits becomes more prevalent, there is an urgent need for improved superconducting electronics and switches to interface between dissimilar material systems. We successfully fabricate and test several multilayer thermal superconducting switches that locally transfer energy from a heater to a superconducting channel while maintaining electrical isolation. Crucially, electrical isolation eliminates the undesired sneak current present in nTrons and enables greater flexibility in the design of the impedance of both the gate and channel, as needed for high fan-out or interfacing with semiconductor electronics. This characteristics of hTrons make them ideal candidates for a number of applications ranging from amplifiers for SNSPD readout to digital electronics and memory devices.

The heat transfer in these devices is adequately described by the combination of the two-temperature and acoustic mismatch models solved over the 3D geometry of the device. Such a model can be used as a design tool to tailor hTron performance for specific applications. While an improved theoretical understanding of the nonequilibrium superconductivity and the thermal boundary resistances would aid in the quantitative design of hTrons, the current understanding of these devices is sufficient to position the hTron as an enabling technology for a variety of superconducting electronics applications.

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APPENDIX A: SIMULATION PARAMETERS

The model described in Sec. III requires knowledge or estimates of a variety of physical properties of the superconductor, heater, and dielectric materials. Given that many of these parameters are difficult to measure experimentally, we use a combination of literature estimates and measured quantities in our modeling.

The thickness of the titanium heater is estimated to be 30 nm based on the deposition time and rate, the sheet resistance is measured to be $24.8\Omega/\square$, and the electron thermal conductivity is modeled according to the Wiedemann-Franz relation. The electron heat capacity is estimated as $C_{e,\mathrm{Ti}}(T_{e,\mathrm{Ti}}) = \gamma_{\mathrm{Ti}} T_{e,\mathrm{Ti}}$, with $\gamma_{\mathrm{Ti}} = 320\ \mathrm{J/m^3K^2}$ [19]. The titanium phonon system is treated using the Debye model with $C_{\mathrm{ph,Ti}}(T_{\mathrm{ph,Ti}}) = \alpha_{\mathrm{Ti}} T_{\mathrm{ph,Ti}}^3$, in which $\alpha_{\mathrm{Ti}} = 2.47\ \mathrm{J/m^3K^4}$ [19]. The Ti phonon thermal conductivity is estimated as $\kappa_{\mathrm{ph,Ti}} = \alpha_{\mathrm{Ti}} D_{\mathrm{ph,Ti}} T_{\mathrm{ph,Ti}}^3$, with the phonon diffusion coefficient $D_{\mathrm{ph,Ti}} \sim 0.27\ \mathrm{cm^2/s}$, which represents the Casimir limit. The electron-phonon coupling constant is $\Sigma_{e\text{-ph,Ti}} = 1.3 \times 10^9\ \mathrm{W/m^3K^5}$ [20].

The heat capacity of the SiO_2 spacer is estimated using the Debye model. The SiO_2 thermal conductivity is estimated by extracting the bulk-phonon mean free path from bulk values of the thermal conductivity [21] and the Debye heat capacity [22], averaging this mean free path with a wavelength-independent lower bound equal to the film thickness and then using the kinetic relation to estimate the reduced thermal conductivity for a thin film [23].

The NbN film is 20 nm thick, based on the deposition time and rate, and the T_c value is 8.4 K, based on the temperature-dependent switching current. The sheet resistance for the simulations is estimated to be 470 $\Omega/\square$, based on the average I-V characteristics of measured devices at cryogenic temperatures and the geometry of the devices. The electron diffusion coefficient of NbN is approximated as 0.5 cm^2/s and the electron-phonon characteristic coupling time τ_0 is approximated to be 1000 ps (see Ref. [7]). These properties lead to an estimated zero-temperature depairing current of 237.4 μA [12] for the 600-nm-wide devices and the Bardeen temperature dependence is used at elevated temperatures to approximate the temperature-dependent depairing current. The switching current is approximated by $I_c = 126.6\left[1-(T/T_c)^3\right]^{2.1}\,\mu$A, which comes from fitting experimental measurements of the switching current for the 600-nm-wide channel device over the temperature range of interest (see Fig. 5). This represents the switching current of the device at the smallest constriction, which is assumed to be at the center of the nanowire for the 600-nm-wide channel device. Outside of this constricted area, the switching current is given by the temperature-dependent depairing current. These values lead to a constriction factor of approximately 0.58 ± 0.05 over the range of $0.4 \leq T/T_c \leq 0.8$, which is consistent with measurements of the switching current to depairing current ratio in thin NbN films [24]. It is important to note that the use of a constriction underneath the heater and a depairing current outside of the heater region is necessary to simultaneously reproduce the switching and retrapping characteristics of the device within the model. If the experimentally measured switching-current relation is used over the entire nanowire domain, the simulated retrapping current is significantly smaller than the experimentally measured results. For the NbN-phonon system, we use the Debye model and the average phonon sound velocity $v_{\mathrm{avg,NbN}} = 4912$ m/s, based on measurements of the elastic properties of the material [25], which lead to $C_{\mathrm{ph,NbN}}(T_{\mathrm{NbN}}) = \alpha_{\mathrm{NbN}} T^3_{\mathrm{ph,NbN}}$ with $\alpha_{\mathrm{NbN}} = 1.03\ \mathrm{J/m^3K^4}$. The phonon thermal conductivity is treated in the same way as the Ti heater, using the phonon diffusion coefficient $D_{\mathrm{ph,NbN}} \sim 0.33\ \mathrm{cm^2/s}$.

The thermal boundary conductance at each of the interfaces is calculated using the AMM following the approach detailed by Kaplan [13]. The relevant sound velocities and densities used for these calculations along with the boundary conductance parameters are listed in Table I.

The retrapping current simulations of Fig. 5 are performed with a time-dependent voltage source in series with the superconducting channel, the series inductor, and a 10 kΩ bias resistor. The supply voltage is slowly reduced, allowing an established hot spot to shrink to its minimum size before relaxing to the superconducting state. The retrapping current is evaluated as the minimum current that sustains a hot spot.

APPENDIX B: SIMPLIFIED MODEL

All of the simulation results shown above use the full 3D model described in the text. However, the implementation of such a model is computationally intensive and is often not necessary to gain useful information for making design decisions. The computational complexity of the model can be significantly simplified by reducing the model to a lower-dimensional form. In the limits of a wide superconducting channel, a wide heater, a thin heater, a thin dielectric spacer, and a thin channel, the system of equations can be expressed as a zero-dimensional (0D) set of coupled PDEs. While this neglects the effects of diffusion and cannot be used to describe the electrothermal evolution of the superconducting channel, it does provide a simple means of estimating the thermal dissipation required to achieve switching of the superconductor. For the heater, the reduced set of equations can be expressed as

$$C_{e,H}(T_{e,H})\frac{\partial T_{e,H}}{\partial t} = -\Sigma_{e\text{-ph},H}\left(T^5_{e,H} - T^5_{\mathrm{ph},H}\right) + \frac{I_H^2 \rho_H}{(w_H\, d_H)^2} \tag{B1}$$

TABLE I. The AMM parameters. For each material, v_l is the longitudinal sound velocity, v_t is the transverse sound velocity, and ϱ is the density.

Material 1	v_l (m/s)	v_t (m/s)	ϱ (g/m^3)	Material 2	v_l (m/s)	v_t (m/s)	ϱ (g/m^3)	G_{12} (W/m^{2}K^4)
NbN	7137	4459	8.25	Sapphire	10900	6450	3.98	516.2
NbN	7137	4459	8.25	SiO_2	5832	3712	2.2	738.1
SiO_2	5832	3712	2.2	Sapphire	10900	6450	3.98	452.5
Ti	6100	3120	4.50	SiO_2	5832	3712	2.2	1504

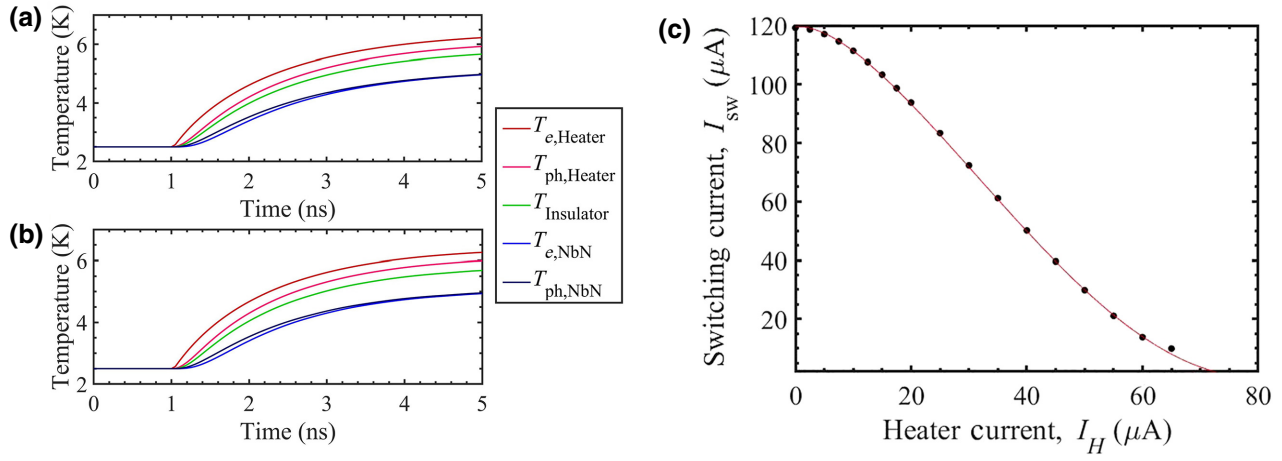

FIG. 10. A comparison of the transient response of the (a) zero-dimensional (0D) simplified model to the (b) full 3D model. A heater current of 30 μA turns on at a time of 1 ns. The channel width is 600 nm and the heater width is 500 nm. The temperatures of the 3D model are sampled at the center of the intersection of the heater and nanowire and at a depth of half the film thickness. There is good quantitative agreement between the simplified and full models. (c) A comparison of the simulated switching current for the full 3D model (circles) and the analytical expression given in Eq. (B6) (red line). The two models agree in this limit of a wide heater and a wide channel. The deviation in the switching current of the full model at the highest heater current is due to ambiguity in the definition of switching in this regime.

and

$$C_{\mathrm{ph},H}(T_{\mathrm{ph},H})\frac{\partial T_{\mathrm{ph},H}}{\partial t} = \Sigma_{e\text{-ph},H}\left(T_{e,H}^5 - T_{\mathrm{ph},H}^5\right) - \frac{G_{H-D}}{4d_H}\left(T_{\mathrm{ph},H}^4 - T_D^4\right), \quad \text{(B2)}$$

where $T_{e,H}$ is the heater electron temperature, $C_{e,H}$ is the electron heat capacity, $\Sigma_{e\text{-ph},H}$ is the heater electron-phonon coupling strength, I_H is the heater current, ρ_H is the heater resistivity, d_H is the heater thickness, w_H is the heater width, $T_{\mathrm{ph},H}$ is the heater phonon temperature, $C_{\mathrm{ph},H}$ is the phonon heat capacity, G_{H-D} is the heater-dielectric boundary conductance, and T_D is the dielectric temperature. The dielectric equation takes the form

$$C_{\mathrm{ph},D}(T_{\mathrm{ph},D})\frac{\partial T_{\mathrm{ph},D}}{\partial t} = \frac{G_{H-D}}{4d_D}\left(T_{\mathrm{ph},H}^4 - T_D^4\right) - \frac{G_{D-S}}{4d_D}\left(T_{\mathrm{ph},D}^4 - T_{\mathrm{ph},S}^4\right), \quad \text{(B3)}$$

where $C_{\mathrm{ph},D}$ is the dielectric heat capacity, d_D is the dielectric thickness, G_{D-S} is the dielectric-superconductor boundary conductance, and $T_{\mathrm{ph},S}$ is the channel superconductor phonon temperature. Finally, the reduced equations for the superconducting channel become

$$C_{e,S}(T_{e,S})\frac{\partial T_{e,S}}{\partial t} = -\Sigma_{e\text{-ph},S}\left(T_{e,S}^5 - T_{\mathrm{ph},S}^5\right) \quad \text{(B4)}$$

and

$$C_{\mathrm{ph},H}(T_{\mathrm{ph},H})\frac{\partial T_{\mathrm{ph},H}}{\partial t} = \Sigma_{e\text{-ph},S}\left(T_{e,S}^5 - T_{\mathrm{ph},S}^5\right) - \frac{G_{D-S}}{4d_S}\left(T_{\mathrm{ph},S}^4 - T_D^4\right) - \frac{G_{S\text{-Sub}}}{4d_S}\left(T_{\mathrm{ph},S}^4 - T_{\mathrm{Sub}}^4\right), \quad \text{(B5)}$$

where $T_{e,S}$ is the electron temperature of the channel, $C_{e,S}$ is the electron heat capacity, $\Sigma_{e\text{-ph},S}$ is the electron-phonon coupling constant, $C_{\mathrm{ph},H}$ is the phonon heat capacity, $G_{S\text{-Sub}}$ is the channel-substrate boundary conductance parameter, d_S is the channel thickness, and T_{sub} is the substrate temperature.

The full 3D simulation results are compared with the results of the simplified formulation of Eqs. (B1)–(B5) in Fig. 10 for the time-dependent temperature response of the system to a current pulse in the heater. There is only a small difference in the transient response of the system, which is attributed to the thermal conduction across the thicknesses of the films.

Within the simplified model, calculation of the steady-state thermal coupling from the heater to the superconducting channel can be reduced to the analytical expression

$$T_{e,S}(I_H) = \left[\frac{4\rho_{\square,H}}{G_{S\text{-sub}}}\left(\frac{I_H}{w_H}\right)^2 + T_{\mathrm{sub}}^4\right]^{1/4}, \quad \text{(B6)}$$

where $\rho_{\square,H}$ is the heater sheet resistance. The heating-induced switching current is found by inverting the temperature-dependent switching-current expression. A comparison with the full 3D model is shown in Fig. 10(c).

The reasonable success of the 0D model indicates that it is a useful tool for designing the thermal-coupling properties of hTron devices. However, a full model is needed in order to understand the more complex electrothermal coupling that occurs in superconducting circuits.

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