Perspectives on Formation and Properties of Semiconductor Interfaces

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Recent progress in experimentally and theoretically understanding interfaces at the atomic level suggest that ultimate electronic systems may one day be fabricated on a single integrated chip. If such elements as Si VLSI processors, GaAs/AlAs integrated optoelectronic IO devices, II-VI superlattice visible displays and high speed III-V processors are to be integrated, interface formation and *in situ* processing will be required at a level of sophistication well beyond what is available today. In this paper, we review recent developments in interface formation by both MOCVD and MBE. To illustrate the power of our diagnostic methods, the details of epitaxial interface formation on an atomic scale are reviewed for lattice matched systems (Ge/GaAs/AlAs) and epitaxial silicides ($Ni/Si_2/Si$) as well as oxidation of silicon to form Si/SiO_2 interfaces. New developments in using lattice mismatched superlattices with strained layers are discussed for CdTe/ZnTe. Additional complications of growing compound semiconductors on elemental substrates (e.g., anti-phase domains) are discussed for GaAs growth on Si(100).

The implications of these interface formation methods for understanding and controlling the physical properties of these material systems are also explored. A review of the current status of heterojunction band offsets is given. Emission and adsorption of light is discussed for lattice matched quantum well lasers and strained-layer superlattices for light sources and detectors. New developments in transport both parallel and perpendicular to the interface are explored with particular attention to new device structures employing layers of a few atomic dimensions for tunnel structures. It is shown that by understanding and controlling the formation of heterojunction and superlattice interfaces, novel device properties can be established to provide integrated device performance well beyond current capabilities. The opportunities for advances in this field are only just beginning to be realized.

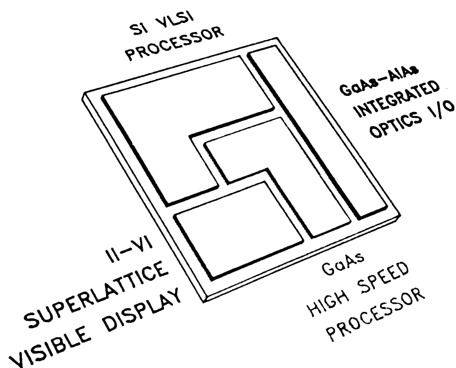

Fig. 1. Schematic representation of the ultimate electronic system. Combining interfaces from group IV, III-V, and II-VI interfaces on a single substrate requires advances in interface growth and *in situ* processing to achieve the advantageous performance of each of the device interfaces (e.g., visible light emission from II-VI's, high speed IO and processing from III-V's, and complex integrated electronics in Si).

1. INTRODUCTION

This paper is meant to take a broad overview of recent developments in understanding and controlling semiconductor interface formation. While presenting details at an atomic level, the intent is to provide insight into new ideas, trends, and opportunities for further research. References are given to work in the literature to provide entry to more

G. Le Lay et al. (eds.), *Semiconductor Interfaces*
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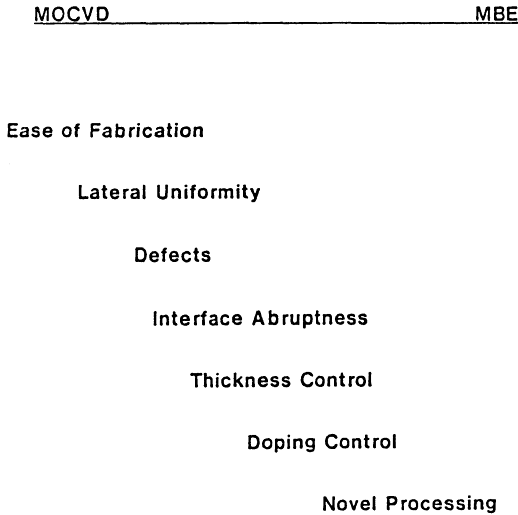


Fig. 2. Schematic comparison of advantages for MOCVD and MBE. A scale is depicted where a property such as ease of fabrication is an MOCVD advantage while at present novel *in situ* processing capabilities are a distinct advantage of MBE. Depending on the characteristic considered, either of the new epitaxial interface growth methods may be advantageous. For such areas as interface abruptness on an atomic scale, thickness control, defect formation, the two techniques are comparable. The challenge for future research is to improve the characteristics that are not well controlled (i.e., lateral film uniformity in MBE materials.

comprehensive treatment of the topics discussed. By presenting an overview of a broad range of recent developments, it is suggested that future advances will occur from extending knowledge in new areas such as strained-layer superlattices and combining them with the extraordinary atomic level tools developed in surface physics during the past 15 years.

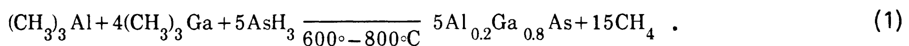
2. FORMATION

Recent developments in the preparation of complex semiconductor interfaces are due to the development of deposition methods capable of atomic level control. The new methods of molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD) result in layers of extraordinarily high quality at thicknesses down to interatomic dimensions. This is opening up applications involving new levels of integration which exploit new materials and device structures.

2.A. Growth Methods

2.A.1. Metal Organic Chemical Vapor Deposition (MOCVD)

While scientific understanding of the interface formation process by MOCVD is at a more primitive level than MBE, the flexibility and potential for large-scale manufacturing makes this an extraordinarily exciting interface formation methodology. MOCVD systems are composed of a series of valves and stainless steel gas lines which are controlled by highly sophisticated mass flow controllers. The basic chemical reactions occurring at the semiconductor surface are relatively straightforward. For example, when trimethylaluminum and gallium are combined in arsine at between 600° and 800°C, an AlGaAs alloy of composition is formed in proportion to the amounts of aluminum and gallium compounds with methane as a byproduct:



$$(CH_3)_3Al + 4(CH_3)_3Ga + 5AsH_3 \xrightarrow[600°-800°C]{} 5Al_{0.2}Ga_{0.8}As + 15CH_4 \quad . \tag{1}$$

Because this technique involves the combination of organic compounds, there are a myriad of potential sources for controlling the growth of semiconductors and forming *in situ* interfaces with other semiconductors as well as metals and insulators. [1]

For group III elements there are at least a dozen potential sources involving combinations of methyl (CH_3), ethyl (C_2H_5), and isobutyl (C_4H_9) with the appropriate metallic or hydrogenated metallic species of aluminum, gallium, indium, etc. For group V sources, arsine (AsH_3) and phosphine (PH_3) have traditionally been used because of their very high toxicity. Recent attempts have been made to substitute organic compounds involving methyl, ethyl, and isobutyl groups with the arsenic, phosphorus or antimony sources. One area of particular promise is the use of adducts. These are organic compounds which are combinations of triethyl or trimethyl radicals with both a group III and group V element (e.g. $(CH_3)_3Ga{\cdot}(CH_3)_3As$). Literally dozens of sources exist for doping III-V compounds both n and p type. Se, Te, Si, S, Sn, and Ge are all available for n-type dopants. Zn, Mg, Be, Cd, Si, and Ge can be employed for p-type doping (though under normal vapor growth conditions Si and Ge are n-type dopants). To create complex interfaces with other materials, sources for semi-insulating layers are possible with such compounds as $VO(OC_2H_5)_3$ and $(C_5H_5)_2$ Fe. Metal contacts can also be deposited by MOCVD using such organic sources as $C_7H_{13}O_2Au$ for depositing gold. Diffusion masks can be deposited in such forms as Si_3N_4 by reacting SiH_4 with NH_3.

With such great potential and myriad of variables, MOCVD reactors have become increasingly complex. At Xerox PARC, R. D. Burnham [1] began building his first reactor in 1979 with two inject lines. In 1982 a next generation system was built with three lines in order to grow controlled quantum well structures and allow atomic level planar doping of III-V compounds. The present state of the art is exemplified by a new six inject line reactor which became operational in December, 1986. These are used for a multiple chamber configuration where choices of gases can be changed to include the types of materials discussed in the last paragraph plus selective etchants. Such reactors involve computer control of the switching manifold with the potential for extensive *in situ* monitoring. In addition, *in situ* lateral modification of the layers is possible using laser assisted growth techniques as discussed in section 3.B.1 below.

The resulting MOCVD layers exhibit interface abruptness of one interatomic spacing [2]. The uniformity of such layers are as good as or better than similar structures fabricated by MBE, as shown by quantum well laser structures. [3] The result is a technique for formation of interfaces which offer advantages and disadvantages comparable to MBE.

2.A.2. Molecular Beam Epitaxy (MBE)

Molecular Beam Epitaxy offers an interface formation technique which is compatible with sophisticated methods for characterizing surface properties. Present state of the art involves combining multiple ultra-high vacuum chambers with sample transport and interlock mechanisms. In this way interfaces can be grown by MBE in one special purpose chamber, transferred to another chamber for characterizing the properties of the surface and subsurface regions, and ultimately transferred to chambers which measure the performance of interfaces in producing physical phenomena of interest (e.g., light emission, transport). An example of such a sophisticated multi-chamber system is shown in Fig. 3, [4].

A system constructed by Ross Bringans and Lars-Erik Swartz of Xerox PARC combines three chambers for MBE preparation, characterization and measurement of synchrotron radiation photoelectron spectroscopies (i.e., angle resolved valence electrons using UV and high resolution core levels using soft x-rays). [5]

The current state of the art in molecular beam epitaxial systems has been reviewed in these proceedings by Klaus Ploog. [6] Here we will review some of the understanding of MBE interface formation that can be obtained through the combination of synchrotron radiation with MBE growth during the initial stages of heterojunction formation. Because the valence band offset evolves during the first few monolayers of growth, it is vital to probe the detailed interatomic interactions during the initial stages of deposition. Using the core-level emission from both the substrate and the overlayer adatoms, both stoichiometric and chemical bonding information can be directly obtained for the interface species involved. The intensity of the emission from the 3d core levels can be analyzed directly to follow the characteristics of the interface formation. Taking

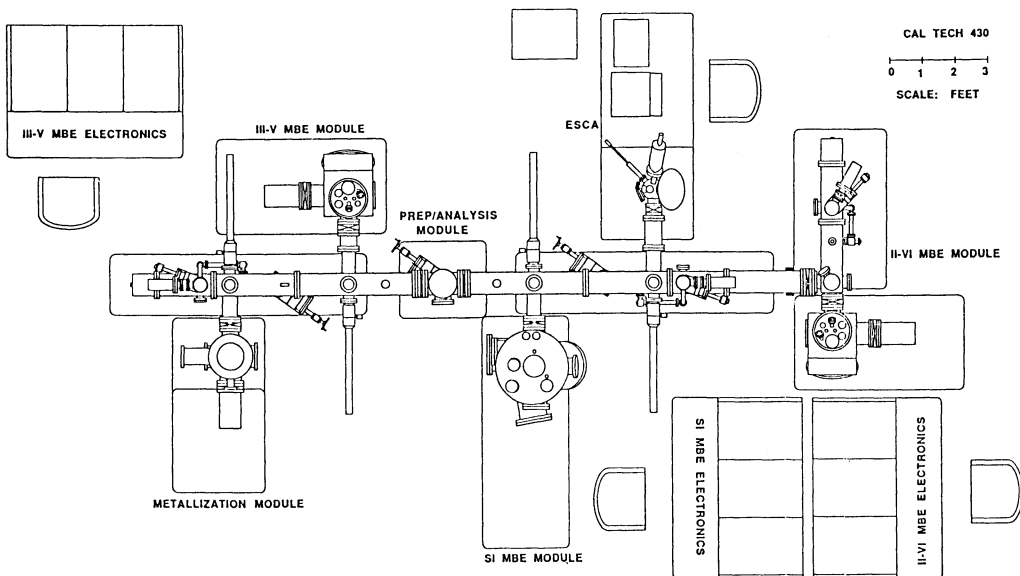


Fig. 3. Schematic diagram of the Caltech 430 MBE and analysis system manufactured by Physical Electronics, Inc. The system allows group IV, III-V, and II-VI MBE combined with a metalization module for sample contacts and silicide formation. Various *in situ* analysis techniques are possible including the ESCA facility shown in the diagram.

as an example the formation of the Ge interface with GaAs, we find that the thin film growth is dramatically different as a function of substrate temperature. [7] Normal photoemission analysis of core level intensity versus log of overlayer thickness, can distinguish abrupt epitaxial interface formation at 350°C from island formation at 22°C. [7] At lower temperatures much greater thicknesses are necessary to fully attenuate the substrate signal indicating island formation. At higher temperatures, interdiffusion occurs and the substrate constituents behave differently. Since in all cases the Ga substrate is known to be immobile, we have devised a novel method for analyzing core photoemission intensities. [8]

Figure 4 is a plot of the percentage of total 3d core photoemission intensity as a function of the percentage of the element which is stationary at the interface (i.e., Ga). In the ideal case shown by the dashed line, as the overlayer thickness increases (i.e., Ge), the substrate constituent signal would decrease to the origin (e.g., both Ga and As signals disappear at the same time). This is the case for 350°C Ge MBE growth on GaAs (110) [7]. In the case of GaAs (100) surfaces in Fig. 4, excess As evolves from the substrate to the top of the growing Ge film for all initial surface structures. This "stationary cation analysis" of core-level photoelectron spectra provides overviews for trends in the atomic level motion at interfaces during the initial stages of formation.

This result for Ge growth on (100) surfaces of GaAs demonstrates the importance of surface energy in determining the ultimate configuration of semiconductor interfaces. In another Ge MBE growth experiment involving (110) non-polar substrates, it was shown that even though AlAs is a more stable bulk semiconductor, the surface interactions were such that interdiffusion occurred even more abruptly than for GaAs. [9] Even though the enthalpy of AlAs is -28 kcal/mole compared to GaAs's enthalpy of -17 kcal/mole, deposition of Ge at between 325° and 350°C leads to out-diffusion of the substrate species from the non-polar (110) face <u>only</u> in the case of the AlAs. Thus bulk equilibrium thermodynamic quantities are not predictive of the surface and kinetic processes involved in MBE interface formation.

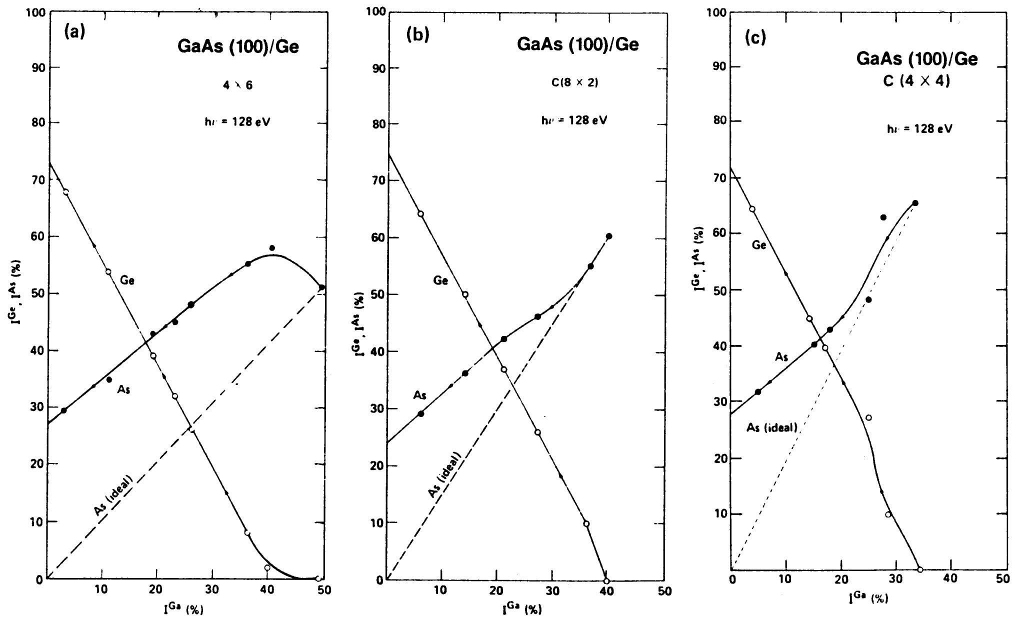


Fig. 4. Stationary cation analysis of core-level photoemission intensity to determine interface formation characteristics on an atomic scale for Ge deposited by MBE in *in situ* on GaAs (100) surfaces under epitaxial growth conditions [8]

2.A.3. Oxidation

No discussion of semiconductor interface formation and properties would be complete without consideration of the Si/SiO_2 interface. This gift of nature provides the physical properties allowing the marvels of the current electronics age. One of the striking features of this naturally occurring interface growth method is that the growth of the silicon dioxide/silicon interface proceeds in an atomically abrupt, planar manner. [10] Photoelectron spectroscopy has provided an extraordinarily valuable tool for characterizing this interface on an atomic scale. [11] Grunthaner et al. have used high resolution XPS techniques to identify the various bonding species of silicon with oxygen. Recently, they have extended this work using synchrotron radiation to vary the photon energy and obtain depth profiles of the oxide and substrate species. They have developed models for the bonding of silicon in its various charge states with oxygen across the (100) and (111) interfaces. By correlating core-level electron energy distributions at fixed photon energy with the photon energy variation of photoelectron yield at the silicon 2p threshold around 100 eV, we have been able to identify detailed formation mechanisms for SiO_2 and sub-oxide species of silicon at the interface. For the growth methods employed, we can develop the detailed atomic model for the interface which extends over one to two interatomic planes. [12,5]

Using such techniques, one can explore modifications in the growth procedures which may allow modification of interface defect formation, incorporation of foreign species to tailor electrical and transport properties, and ultimately achievement of multilayer silicon/SiO_2 structures for advanced three-dimensional devices.

2.B. Epitaxy

Having explored methods for forming semiconductor interfaces, we discuss the process of epitaxy in detail for both lattice matched and greatly lattice mismatched semiconductor interfaces.

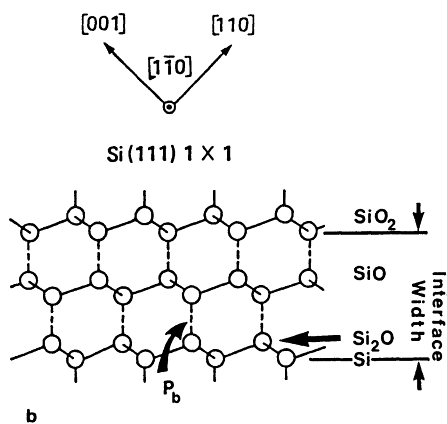


Fig. 5. Model for the interface width and species of silicon atoms surrounded by 4 silicons (Si),1 oxygen and 3 silicons (Si_2O), silicon with 2 oxygen and 2 silicon nearest neighbors (SiO), and fully oxidized SiO_2 (Silicon surrounded with four oxygen near neighbors). This result for (111) oxidation was determined using both the high resolution and tunable characteristics of soft X-ray synchrotron radiation in the 100 eV range for Si cleaved surfaces at elevated temperature. [12]

2.B.1. Lattice Matched Interfaces

2.B.1.a. GaAs/Ge/AlAs

There are many examples of heterojunction interfaces grown by MBE displaying pathologically different properties depending on such parameters as growth sequence. [9] However, device properties that are extremely sensitive to band offsets indicate symmetric barrier formation for reciprocal growth conditions. [7,13] It is important to understand the details of the chemical and physical structure on an atomic scale in order to understand the physical origin of such variations in interface properties as well as to evaluate possible methods of providing property control through growth variation.

We must recognize that the free surfaces of compound semiconductors are extremely complex. For a particular crystallographic orientation, different surface superstructures having varying stoichiometries can drastically affect the initial atomic configuration and chemical composition that incident adatoms bond with. Further, as discussed above, outdiffusions can occur under ideal conditions based on the stabilization of the growing free surface. Detailed decompositions of photoemission core levels into surface and bulk contributions can be individually studied as sub-monolayer coverages of foreign adatoms are deposited. Detailed kinetics for interface formation and models for the ultimate interface [10] can be obtained from 3d core line shapes and intensity variations for Ga, As, and Ge with growth. [14,7,5,8] An example of such a result is given in Fig. 6.

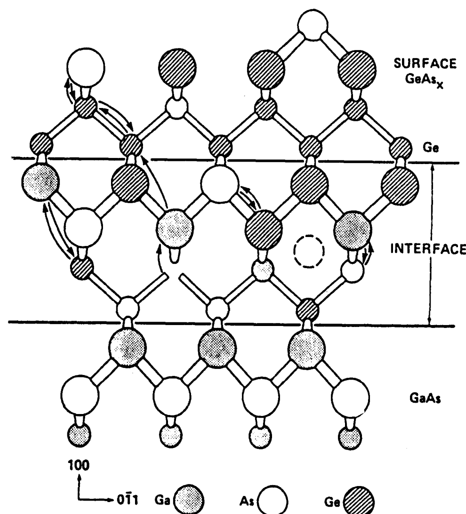


Fig. 6. Model for the GaAs (100)/Ge heterojunction grown by MBE at 340°C. The diagram shows some of the interatomic exchange processes that occur during MBE growth that lead to an atomically distributed (though otherwise abrupt) transition from one semiconductor to the other. This transition and the resulting complex structure at the interface will depend on the stoichiometry and structure of the initial GaAs surface because the growth process is dominated by physical and chemical forces which continually minimize the free surface energy. [10]

From such studies of epitaxial interface formation we conclude that metastable surface phases are driving forces that stabilize the ultimate interface atomic structure. Understanding the stable arsenic-terminated GeAs surface is as vital as having a model for the clean GaAs (100) starting surface. [15] This free energy driving force also means that the epitaxial overlayers are not necessarily characteristic of the bulk stoichiometric material. Detailed surface and interface physics and chemistry must be determined to understand formation of heterojunction interfaces.

2.B.1.b. $NiSi_2/Si$

Formation of lattice matched semiconductor interfaces is not limited to heterojunctions alone. One of the most exciting developments in this regard is the formation of insulator/semiconductor lattice-matched interfaces [16] and epitaxial metal/semiconductor interfaces [17,18]. Here we only briefly discuss the latter case as an example of exciting new directions in forming novel epitaxial interfaces.

The basic process of creating epitaxial Si/silicide structures involves (1) surface cleaning by argon ion bombardment and annealing, (2) deposition of a metal film onto the clean surface, and (3) formation of the silicide by solid phase reaction by annealing at elevated temperatures. Si MBE is much more difficult than GaAlAs MBE because of the higher substrate temperature required to achieve epitaxial growth. For example, *in situ* heating up to 1200°C while maintaining 10^{-9} torr UHV ambient is necessary for Si surface preparation. The result for Ni growth is the formation of atomically abrupt epitaxial $NiSi_2/Si$ interfaces. The $NiSi_2$ lattice matches Si and has two possible orientations relative to Si (111). (Type A interfaces have $NiSi_2$ aligned with the silicon lattice, while type B is the same structure rotated by 180°.) The important question is whether the properties of the abrupt interface depend on this different relative atomic orientation of the two lattice-matched materials.

To investigate this controversial question [17], photoresponse measurements using conventional fowler analysis have been combined with analysis of the forward I-V characteristics of the same Schottky barrier samples by Hauenstein et al. [18] The rotated type B interface is found to be a compound barrier of both high and low barrier height. The Schottky barrier height for Type B differs by nearly 200 meV from the $0.62 \pm .01$ eV value obtained for the type A interface. Understanding the origin of such differences in properties and their relation to interface formation is crucial for tailoring device properties. For example, in this current $NiSi_2/Si$ controversy, understanding of the origin and role of planar defects along the interface must be improved; simple misfit dislocations or clustering of the two different types of interfaces appear to be absent for this system. Understanding the nature of the defects and their formation process is an issue for surface and interface physicists.

2.B.2. Strained Layer Superlattices

It is often desirable to tailor properties of semiconductor interfaces independent of whether the new material to be grown matches the lattice structure of the semiconductor substrate. In the past, quaternary alloys of column III and column V elements would have had to be combined in order to create an alloy with optimal lattice match across a heterojunction interface. Examples include InGaAsP and InGaAlP to achieve a band gap greater than that of the GaAs substrate. By being able to grow thin layers of semiconductors, one can create superlattice structures which accommodate the strain caused by the mismatch in lattice constant for materials with otherwise desirable properties (e.g., band gap). In this section we explore the cases of II-VI materials and of compound semiconductor growth on elemental semiconductor substrates. Both are examples of new methods of forming semiconductor structures to tailor specific physical properties.

2.B.2.a. CdTe/ZnTe

Because of their larger band gaps, II-VI materials offer the possibility for creating structures that absorb and emit light in the visible region of the spectrum. The promise of these materials has not been realized to date because of the difficulties in producing

defect free structures and structures with controlled doping. With the advent of MOCVD and MBE, growth temperatures can be significantly lowered. For the zinc II-VI compounds, MOCVD growth temperatures are in the range of 350° to 400°C with MBE growths at 180°C compared to solution growth temperatures at 1600°C and even LPE at 800° to 850°C. This leads to better control of purity, layer structure, and dopant incorporation. By constructing structures of multiple layers of only tens of angstroms of thickness, one can in addition tune properties and utilize substrates compatible with other heterojunction combinations.

In a series of well-controlled MBE growths by Faurie and co-workers, Miles et al. have studied in detail the nature of the strain accommodation for II-VI growth on GaAs substrates and the resulting luminescent properties. [19] The superlattice structure studied is shown schematically in Fig. 7.

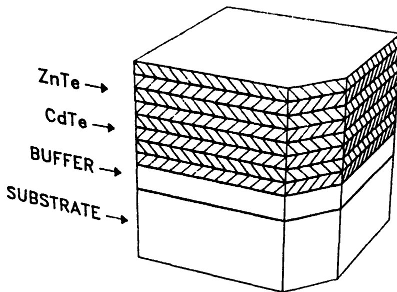


Fig. 7. Schematic diagram of ZnTe/CdTe superlattice structure grown on GaAs substrates with CdTe, ZnTe, and $Cd_{0.5}Zn_{0.5}Te$ buffer layers [19]

The bulk properties of CdTe and ZnTe show band gaps of 1.6 eV and 2.38 eV respectively and zinc blende lattice constants of 6.481 and 6.104 Å respectively. This corresponds to a lattice mismatch of 6.2%. The strained layer epitaxy for such highly mismatched pairs of materials can proceed in two ways. One, the overlayers can be unstrained with the lattice mismatch accommodated by dislocations at the interfaces between the materials (see Fig. 8a). Two, for layers below a critical thickness, the strain may be coherently accommodated by elastic deformation to a single lattice constant in the plane of growth. This results in alternate growth-direction expansion and contraction of consecutive layers, as dictated by a biaxial analogue of the Poisson ratio. The closer this in-plane lattice constant lies to the lattice constant which minimizes strain energy in the structure, the larger the "critical thickness" below which the structure is defect-free.

The best experimental way to resolve which of these strain accommodation mechanisms is operable for various layer thicknesses of CdTe/ZnTe, is through X-ray diffraction measurements. Through a measurement of superlattices of thicknesses in the range of 20 to 50 Å with approximately 200 periods each, Miles et al. studied the

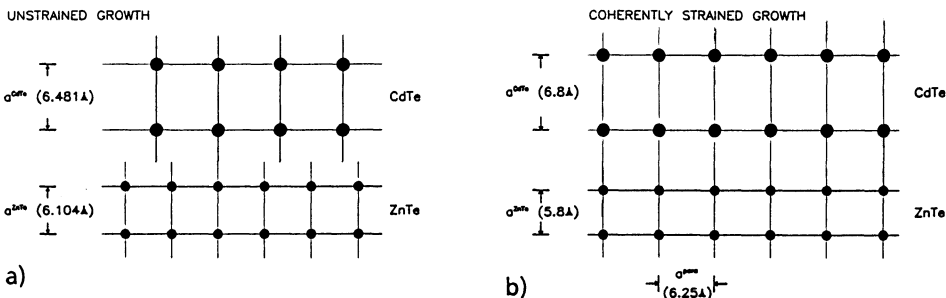


Fig. 8. Schematic representation of a) unstrained growth and b) coherently strained growth for ZnTe/CdTe superlattices [19]

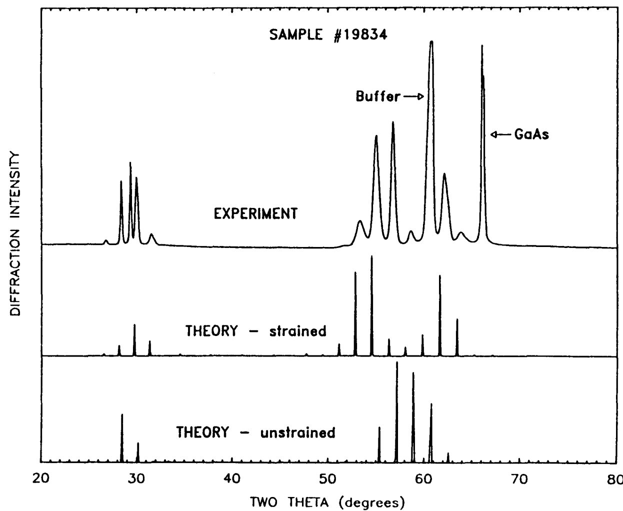


Fig. 9. X-ray diffraction measurements and kinematical model calculations for CeTe/ZnTe superlattices. [19]

contributions to structure from single superlattice cells and the effect of the superlattice periodicity. As summarized in Fig. 9, comparison of kinematical calculations with X-ray diffraction data suggests that the superlattices are highly strained with a structure close to that of a free-standing superlattice. Combining this data with TEM and in situ RHEED measurements has led to the conclusion that defects created at the buffer layer/superlattice interface do not propagate far into the superlattices, leaving high-quality structures away from this interface.

It is important to note also that such high quality superlattices exhibited strain accommodation independent of the composition of the buffer layer. It is believed that in these cases, creation of dislocations at the buffer layer to superlattice boundary accommodated the structural differences. As will be discussed in 3.B.2, the layers were quite uniform in thickness and exhibited intense luminescence compared to the equivalent II-VI alloy. Importantly, high quality II-VI superlattices could be grown for layer thicknesses exceeding the critical thickness predicted by standard theoretical approaches of Bean, Matthews and Van der Merwe [20]. This appears to be the result of a sudden jump of the in-plane lattice constant at the superlattice/buffer layer interface. Thus, although this lattice constant is not a parameter which can be adjusted at will in systems with this large a lattice mismatch, the choice of substrate appears to have little impact on the high quality of the superlattices. Understanding the detailed physical forces that define the critical thickness for such large mismatched superlattices is necessary if formation of such semiconductor interfaces is to be properly predicted and controlled.

2.B.2.b. GaAs/Si

Epitaxial interface formation of GaAs on Si offers major opportunities for merging the physical properties of silicon interfaces with those of III-V's, as well as providing cheap, durable, large area, and high thermal conductivity substrates. Problems in achieving this involve not only the large lattice mismatch of 4% but also the formation of antiphase domains within the compound semiconductor epitaxial layer. This latter problem occurs with growth on elemental substrates because of the absence of a preferential site for adsorption of the group III or group V element. One way suggested to avoid this situation is to use non-primitive crystallographic planes such as the Si (211) orientation. [21] The more technologically interesting result would be to employ the Si (100) surface because it is the orientation used for standard VLSI technologies.

Recently Aspnes and Ihm [22] have suggested a topological solution to the problem of GaAs growth on Si. Simply stated, if one can create steps that are two atoms in height, the Ga and As planes will interleave. This occurs because the first layer formed on Si will always be terminated by As due to the preferential energy of the arsenic terminated silicon surface. [15] Note that this is the same cause for As termination of the growing Ge surface in the III-V lattice-matched Ge/GaAs epitaxy discussed above. With steps in increments of two atomic heights, the terraces would be high enough to accommodate a layer of Ga plus As on top which is adjacent to As directly terminating Si on silicons on the neighboring plateau. Through a series of calculations of the energy of silicon atoms at step edges, Aspnes and Ihm have found that there is a net reduction of 0.04 eV per step atom through a π-bonded chain reconstruction. In addition, by having vicinal cuts in the (110) rather than (100) axis relative to the (100) surface normal, step terraces of retangular shape provide a favorable situation to accommodate low Ga or As surface mobility. Simple annealing for five minutes at 1000°C for such Si (100) substrates is found to eliminate all monoatomic steps. This provides a substrate for GaAs growth which should not produce antiphase domains. The sole origin of this effect appears to be thermodynamic driving forces caused by step atom reconstruction. [22] This new result for compound semiconductor growth on elemental semiconductor substrates deserves considerable effort by surface physicists to explore experimentally and theoretically the properties of steps.

3. PROPERTIES

Motivation for understanding the formation of semiconductor interfaces on an atomic scale is driven by the desire to tailor the properties of the resulting structures. In this section we explore both the parameters which determine properties of semiconductor interfaces as well as demonstrating new and exciting trends in properties of novel semiconductor interfaces.

3.A. Barrier Heights (Heterojunction)

The principal parameter determining semiconductor interface properties is the height of the electrostatic barrier at the interface. Whether these be epitaxial, amorphous, or interfaces created by doping variations in a single host material, changes in the potential within the semiconductor are responsible for the interesting physical properties.

3.A.1. Schottky Barriers and Ohmic Contacts

Much has been written about the controversies in understanding Schottky barrier heights. [23,24] Debate over the role of defects versus metal induced gap states (independent of what they are called!) seems to go on forever. The issues are important and perhaps some of the more subtle effects such as the differences in Type A and B interfaces of $NiSi_2$/Si will help to resolve these issues.

As will be shown for heterojunctions, Schottky barrier properties can be tailored. For example, Brillson has shown that metallic interlayers can cause metal/semiconductor interfaces to exhibit either rectifying or ohmic-current voltage characteristics depending on the thickness of the Al placed between Au and CdS. [26] See Fig. 10.

In discussing the formation of semiconductor interfaces, no consideration has been given to the problem of ohmic contacts. While major questions of the origin and theory for Schottky barriers remain (such as to explain the difference in type A versus type B $NiSi_2$/Si barrier heights), no comparable effort to understand and improve ohmic contacts exists. The metallurgy is quite complex [10] and epitaxial ohmic contact work is only just beginning [25].

3.A.2. Heterojunctions

There has been much recent discussion of the heterojunction band offset problem. [5,24] Here we provide a summary perspective on the current state of understanding.

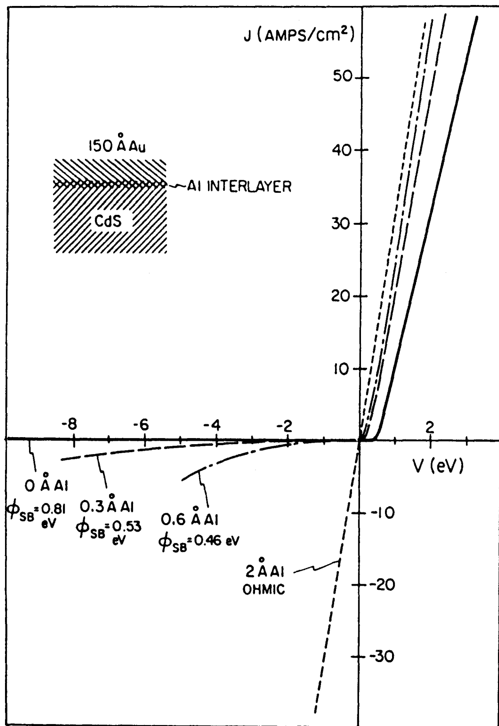


Fig. 10. Variation in Au/CdS interface properties by *in situ* deposition of submonolayer thicknesses of Al [27]

Recent work has firmly established that each heterojunction pair can have a single, unique band offset value independent of preparation details if the interfaces are formed in a controlled, ideal manner. For example, the crystallographic orientation, [8] the presence of large excess of a single constituent, [27] or the intentional deposition of a metal inner layer [28] do not change the value of the GaAs/Ge band offset. The controversey over possible violations of the commutative and transitive properties of band offsets has been resolved in favor of reciprocal interfaces which are clearly known to occur in real device structures. [29,30] Much of the discussion of tailoring intrinsic properties of interfaces is due to extrinsic effects in the formation of the heterojunction interface; for example, the use of cleaved surfaces and room temperature amorphous overlayers artificially causes variation as large as half the band gap compared to epitaxial crystalline layers on defect-free substrates. Even though charged levels of a single sign at the interface cannot pin the Fermi level [10,27], dipole layers created by intentional monolayer dopants of opposite sign intentionally deposited within at most a few atomic layers of each side of the interface can produce intentional potential changes. [31] It must be emphasized, however, that the properties of heterojunctions are controlled by band offsets with sensitivities down to meV. [32,5] While some of the most interesting theoretical advances have involved trying to find commonality between transition metal impurities, Schottky barrier heights, and heterojunction band offsets, [25] the general trends obtained by such theoretical approaches are only road maps for the experimentalist who must probe these interface properties to orders of magnitude better accuracy. The best "rule of thumb" for the band offset value of a new, unknown semiconductor/semiconductor pair is provided by the table of valence band edges of Margaritondo and co-workers. [33,15] However, caution must be used as inconsistencies are often found (e.g., ZnSe/SnTe), and the table values have evolved significantly over time (see for comparison ref. [33]).

Table 1. Positions of the band edges are given relative to the valence band edge of germanium. The difference between two terms gives a zeroth-order estimate of the discontinuity ΔE_V.

Energies of valence band edges

Semiconductor	**E_V (eV)**
Ge	-0.00
Si	-0.16
α-Sn	0.22
AlAs	-0.78
AlSb	-0.61
GaAs	-0.35
GaP	-0.89
GaSb	-0.21
InAs	-0.28
InP	-0.69
InSb	-0.09
CdS	-1.74
CdSe	-1.33
CdTe	-0.88
ZnSe	-1.40
ZnTe	-1.00
PbTe	-0.35
HgTe	-0.75
CuBr	-0.87
GaSe	-0.95
$CuInSe_2$	-0.33
$CuGaSe_2$	-0.62
$ZnSnP_2$	-0.48

3.B. Light Emission/Absorption

3.B.1. Quantum Well Lasers/Superlattice Luminescence

The ability to form heterojunctions having atomic scale interface abruptness has provided dramatic enhancements in the quality and properties of light-emitting devices. A number of excellent reviews have been published on the quantum size effect [34], quantum well lasers [35], and general reviews on new directions made possible by advances in MOCVD and MBE interface formation techniques [36]. The ability to control composition, interface abruptness, and complex structures of III-V alloys allows tailorability of opto-electronic properties.

One particular important recent advance involves impurity induced homogenation of superlattice regions at relatively low annealing temperatures. This promises to provide a new generation of novel opto-electronic properties. [37] Dramatic advances have been made in utilizing both n and p-type impurity dopants to cause homogenation of quantum well superlattice regions. [38] However, the detailed physical mechanism that causes impurities at lattice matched III-V heterojunction interfaces to produce massive interdiffusion some 400-^{o}500°C below normal pure superlattice interdiffusion temperatures is not understood and is little studied. [39]

As shown in Fig. 2, one of the distinct advantages of MBE is its ability to achieve *in situ* lateral modification of the atomic layer growth. One of the challenges for MOCVD is to develop ways to achieve such *in situ* processing of semiconductor interfaces. As shown schematically in Fig. 11, one method is to use focussed *ex situ* laser beams transmitted through the reactor so as to produce fine lines on the growing semiconductor interface. In this way, lasers can assist MOCVD, by local heating for device structure formation homogenizing alloys, by controlled photochemical etching, and by laterally defined deposition utilizing through photochemical and photothermal growth rate enhancements.

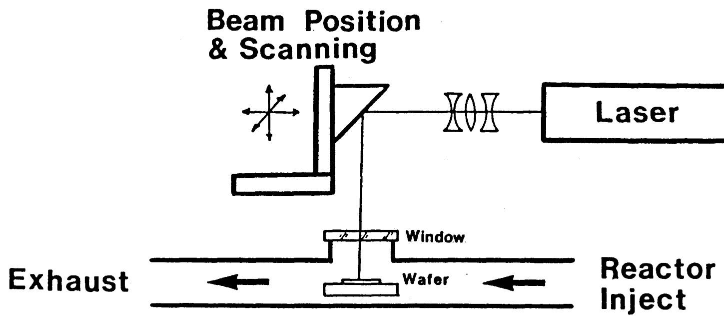


Fig. 11. Schematic diagram of a scanned laser system for *in situ* lateral structure processing of epitaxial layers grown by MOCVD.

The impurity-induced disordering effect smears the structure of superlattices with layers hundreds of angstroms in thickness. The region of homogenized alloy material has the composition of the average superlattice composition. The quality of the homogenized layer is equivalent in optical and electrical properties to that of the equivalent alloy layer grown directly by MOCVD. Thus, one can grow 2-D superlattice structures and then choose regions in which to locally induce homogenation of the lattice in order to create lateral regions of different optical and electrical characteristics. By choosing the proper impurity, one can also type convert to either n-type using silicon impurities or p-type by using zinc impurities. This provides a novel mechanism for creating regions of different indices of refraction laterally. In this way laser structures of enhanced capability can be produced.

The results described for impurity induced disordering have been nearly all the result of empirical studies. [38] Basic questions need to be resolved such as how the presence of the interfaces is important in promoting the impurity induced interaction in the superlattice. [39] Further questions of what range such forces may operate over (given that the effect has been seen for layers many hundreds of angstroms in thickness) present interesting challenges to the surface and interface scientist. Understanding and controlling this phenomenon promises to provide a new, powerful method for tailoring light emitting and detecting properties of semiconductor interfaces.

3.B.2. Strained-Layer Superlattices

The major advantage of creating strained-layer superlattices is to form interfaces among materials with desired properties where the structural parameters are incompatible. For the ZnTe/CdTe case described in 2.B.2.a, the band structure is shown in Fig. 12. Note that the valence bands include light and heavy hole contributions which are important in understanding the ultimate-superlattice optical properties. These superlattices exhibit intense luminescence compared to a rather weak and shifted broad luminescent intensity for the equivalent $Cd_xZn_{1-x}Te$ alloy. [19] The power of the strained layer superlattice idea is perhaps illustrated best by Fig. 13 where a k·p calculation for the contours of constant energy gap are shown as functions of the number of CdTe and ZnTe layers per superlattice period. A range of band gaps is achievable. Note also that because of the strain effects on the light hole valence states in ZnTe, the superlattice gap actually decreases as ZnTe layers are added for fixed thicknesses of CdTe layers. This "bowing" is an intriguing phenomenon that provides a region of relative stability for tailoring the optical properties of strained-layer superlattices.

For Ge/Si strained-layer superlattices, band offsets can be changed from mainly electron to mainly hole barriers depending on alloy composition and layer thickness as described by Bean [40]. The uniqueness of the optical properties of such Ge/Si superlattices has recently been demonstrated by Pearsall et al. [41] where new optical

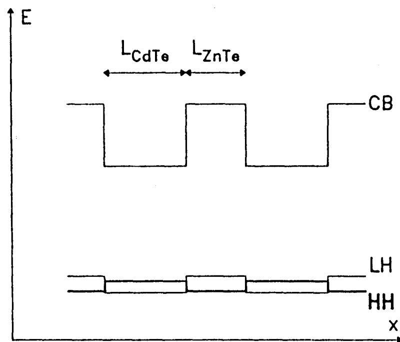


Fig. 12. Schematic band structure for the ZnTe/CdTe strained-layer superlattice

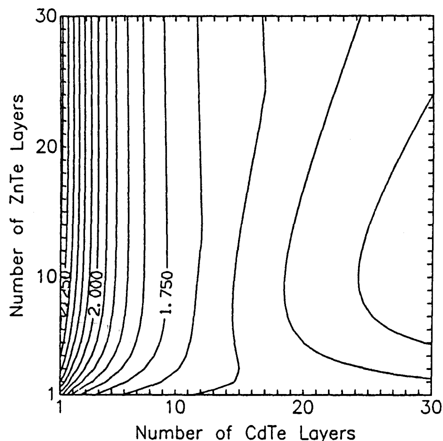


Fig. 13. Calculated superlattice band gaps with strain effects included. Contour interval is 50 meV. Calculations assumed the lattice constant of the free-standing superlattice. Note the shift to lower energies for high CdTe and low ZnTe content.

transitions were measured which are not present in Si, Ge, nor Si_xGe_{1-x} alloys. The tailoring of such superlattice structures offers the ability to vary optical properties of devices directly on Si substrates. With advances in these areas, the formation of opto-electronic circuits directly on Si substrates may be possible utilizing strictly group IV semiconductor interfaces.

3.C. Transport

With the ability to form interfaces with properties controlled to an atomic scale, one must understand the interactions of carriers being transported both parallel to such material transition regions as well as effects when they traverse across such abrupt boundaries. In this section, we note some of the considerations for the interactions of carriers near interfaces and suggest areas of great potential for novel interface properties.

3.C.1. Transport Parallel to Interfaces (High Electron Mobility Transistors)

The extraordinarily high mobilities for transport in the potential notch at heterojunction interface regions has received considerable attention. [42,33] Carrier interactions occur not only at the interface but across the interface for transport along interfaces. We must understand the extent of material transition regions, atomic scale interface composition, the formation of possible intrinsic clustering of atoms at interfaces, interface roughness, and long-range coulomb effects with dopants in layers near the interface. Note the fundamental role that the heterojunction band offset and doping play in determining the potential region in which carriers are transported.

3.C.2. Transport Perpendicular to Interfaces (Tunnel Structures)

With the ability to form interfaces of atomic abruptness, MBE and MOCVD are providing the ability to construct barriers of only 10-20 atomic layers in thickness. This creates the possibility for fabricating a series of heterojunction interfaces which can be used to control conduction via tunelling phenomena. Such structures can provide inherently high speed devices because of the rapid variation in current with voltage. There have been a number of major experimental programs begun to create negative differential

resistance using a GaAs quantum well separated by two thin GaAlAs barriers. Many device configurations are under active investigation with exciting results beginning to appear. [43]

Detailed understanding of the interaction of carriers through these interfaces is crucial to making progress with these structures. Tailorability will depend on the affect of modifications to interface chemical and physical structure on transport and energy loss phenomenon. Reports of large, reproducible interface phonon structures have been reported for I-V measurements. [44] Perhaps these tunnel structures offer one of the most challenging problems for surface and interface studies because of their extreme sensitivity to the details of the entire interface environment. Both theoretical and experimental probes will be necessary to increase knowledge of these structures.

4. CONCLUSIONS

Of all semiconductor interfaces, heterojunctions and superlattices provide some of the most exciting new opportunities. These man-made materials provide a broad range of new device structure possibilties. Tailorability can be achieved in systems that previously had been believed to be unsuitable for applications due to such effects as lattice mismatch induced strain. The key to realizing such promise is to increase our understanding of surfaces and interfaces. The advances in MOCVD and MBE provide new atomic level control of interface formation. Advances in achieving lateral modification of these atomically controlled layers offer ways of directly tuning device structures. To realize this potential both thermodynamic and kinetic effects during the growth of semiconductor interfaces must be understood better. In this way semiconductor interface properties become controllable. Band offsets (barrier heights in general) can be controlled and tuned to provide novel light emission, optical absorption, and carrier adsorption (parallel and perpendicular to interfaces). The opportunities in this field are truly exploding!

5. ACKNOWLEDGEMENTS

The portions of this paper reporting results from the Xerox photoemission research would not have been possible without major collaborative contributions from H. W. Sang, Jr., A. Katnani, P. Zurcher, P. Chiaradia, and J. C. McMenamin, Jr. Perspectives on MOCVD are due to the insight and technical contributions of R. D. Burnham (Amaco). We acknowledge the exciting contributions and advice of R. L. Thornton (Xerox) on impurity-induced disordering of superlattices. The work at Caltech on strained-layer superlattices could not have progressed without the generous assistance of M. B. Johnson and C. Y. Wu. Ted Woodward (Caltech) provided stimulating discussions and shared results on resonant tunnelling device structures prior to publication. The support from the Office of Naval Research (L. R. Cooper) and DARPA (R. Reynolds, S. Roosild, and J. Murphy) is greatfully acknowledged for both its financial contribution as well as the technical perspective provided by the individuals. We are grateful to D. E. Aspnes of Bellcore for generously providing a preprint of his GaAs/Si work prior to publication.

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