POLYTECHNIQUE MONTRÉAL

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Modeling of direct current grid equipment for the simulation and analysis of electromagnetic transients

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Thèse présentée en vue de l'obtention du diplôme de *Philosophiæ Doctor*

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Cette thèse intitulée:

Modeling of direct current grid equipment for the simulation and analysis of electromagnetic transients

présentée par **Anton STEPANOV**

en vue de l'obtention du diplôme de *Philosophiæ Doctor*

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DEDICATION

To the advancement of engineering, science, and engineering science.

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RÉSUMÉ

Les transmissions à base de courant continu sont capables de répondre mieux que les transmissions traditionnelles à base de courant alternatif aux enjeux de nos jours tels que l'intégration des énergies renouvelables, les difficultés avec l'installation des nouvelles lignes aériennes pour les raisons socio-environnementaux, la gestion des flux de puissance sur le réseau électrique. Ceci est grâce aux systèmes de contrôle performants et rapides, à un niveau de fiabilité accrue des composants utilisés, à l'efficacité énergétique des technologies de pointe, telles que les convertisseurs modulaires multiniveaux (Modular Multilevel Converter ou MMC en anglais). Ces avantages ont contribué à une croissance rapide du nombre de transmissions à courant continu à travers le monde dans les dernières années, avec les plans d'établir des réseaux multi-terminaux d'un niveau supérieur aux réseaux électriques traditionnels dans le but de les renforcer.

Les outils de simulation numériques sont nécessaires pour faciliter et accélérer la mise en œuvre de ce type de projets d'envergure. Ils permettent d'analyser et d'étudier les systèmes électriques de plus en plus complexes et par conséquent d'éviter les problèmes opérationnels, d'augmenter la fiabilité et l'efficacité des réseaux électriques. La complexité accrue des réseaux électriques modernes qui contiennent les composants à base de l'électronique de puissance tels que les liaisons à courant continu exige une recherche sur les outils de simulation et les modèles avancés.

Ainsi, cette thèse se focalise sur le développement d'un cadre pour les simulations précises et rapides des liaisons à courant continu. À la suite d'une revue de la littérature il est démontré que la modélisation des MMCs a un impact particulièrement important sur la précision et l'accélération des simulations et par conséquent une grande partie de cette thèse est dédiée aux différentes méthodes pour réduire le temps de simulation et améliorer la précision des résultats dans les études avec les MMCs.

Le cœur du sujet commence par la présentation de la modélisation des MMC hybrides et leurs systèmes de contrôle. Les modèles sont classés en quatre catégories selon le niveau de précision : le modèle détaillé permet de représenter les non-linéarités au niveau des composants semiconducteurs. Le modèle détaillé équivalent utilise les résistances variables pour représenter les semiconducteurs : une valeur faible pour l'état fermé et une grande valeur pour l'état ouvert. Dans le modèle équivalent d'un demi-bras tous les condensateurs dans chaque demi-bras sont supposés d'avoir la même tension, ce qui permet de les représenter par un seul condensateur et

ainsi de réduire considérablement la quantité de calculs à faire. Le modèle en valeur moyenne néglige la dynamique interne des condensateurs et est établi sur l'hypothèse que la tension de tous les condensateurs dans tous les demi-bras d'un convertisseur est identique et constante. Le système de contrôle typique basé sur les boucles en cascade est présenté. Ce système permet d'opérer le convertisseur dans des différentes conditions.

Il est démontré dans cette thèse que les transitoires au début des simulations peuvent être éliminés avec une initialisation précise des modèles du convertisseur MMC, ce qui permet de réduire considérablement le temps de simulation. L'algorithme itératif proposé permet de trouver le comportement en régime établi des variables importantes dans chaque demi-bras du MMC, à savoir la fonction de commutation et la somme des tensions de tous les condensateurs. Ces variables sont par la suite utilisées pour initialiser le système de contrôle et le circuit électrique du convertisseur. Selon les tests, une telle initialisation permet de sauver 50% voire même plus du temps de simulation.

L'autre approche étudiée pour accélérer les simulations est le passage entre les modèles du MMC avec les différents niveaux de détails durant les simulations. Il est proposé d'activer le modèle le moins détaillé et ainsi le plus rapide pendant les périodes quand les détails internes du convertisseur ne sont pas nécessaires. Tel est, par exemple, la période d'initialisation au début des simulations où toutes les variables n'ont pas encore atteint leurs valeurs en régime établi. Les modèles plus détaillés sont par la suite activés pour faire l'étude désirée. Les méthodes d'activation des modèles ainsi que deux nouveaux modèles en valeur moyenne sont développés pour permettre un passage fluide et sans à-coups entre les différents modèles du convertisseur. Dépendamment des conditions de simulation, cette méthode permet d'accélérer la simulation de 10 fois.

Tenant compte des avancements dans les technologies permettant de paralléliser les calculs, cette thèse propose aussi d'accélérer les calculs du modèle détaillé équivalent du MMC en les parallélisant sur les processeurs multicœurs. Les calculs des variables internes de chaque demi-bras sont lancés sur des fils d'exécution différents, ce qui permet de les exécuter en même temps. L'accélération des calculs due à la parallélisation dépend du nombre de sous-modules par demi-bras et du nombre de fils d'exécution. Le facteur d'accélération a la tendance de se stabiliser sur une valeur limite quand le nombre de fils d'exécution augmente à cause des différents calculs qui doivent se faire en série et ne peuvent donc pas être accélérés. Tels sont la résolution des systèmes

de contrôle, la résolution de la matrice de l'analyse nodale modifiée augmentée, ou encore la création et le management des fils d'exécution. La méthode proposée permet ainsi d'accélérer la simulation de 5 fois voire plus.

Cette thèse démontre aussi que le modèle équivalent d'un demi-bras peut générer ou consommer de la puissance active, ce qui n'est pas réaliste puisqu'il n'existe pas de sources ni de consommateurs importants de puissance à l'intérieur du convertisseur. L'origine de cette puissance fictive est attribuée à l'implémentation des équations du modèle en question qui sont résolues avec un pas de temps de retard par rapport aux autres équations électriques. Une formulation analytique décrivant la puissance fictive en fonction des paramètres du réseau est développée et quelques méthodes pour éliminer cette puissance sont proposées. Les avantages et les inconvénients de ces méthodes sont discutés et leurs performances sont comparées en régimes établi et transitoire.

ABSTRACT

Compared to the traditional alternating current technology-based electrical grids, High-Voltage Direct Current (HVDC) transmission systems can more effectively respond to the challenges of the modern power grid related to the integration of renewable energy sources, difficulty to install new overhead lines due to socio-environmental reasons, and power flow management. This is mainly due to high performance of control systems, fast response times, reliable components and energy efficiency of the state-of-the-art HVDC technologies of today, such as the Modular Multilevel Converter (MMC). These advantages have contributed to the rapid growth in the number of HVDC projects in recent years with plans of having overlay HVDC grids that can reinforce the existing electrical grids.

To facilitate and accelerate the implementation of large-scale HVDC projects, it is required to use numerical simulation tools. Such tools allow to perform advanced analysis of involved electrical systems for preventing operating problems, increasing robustness and efficiency in power grids. The increased level of complexity of modern power grids with power electronics-based components, such as HVDC, requires research on advanced simulation tools and models.

Therefore, this thesis aims to develop a framework allowing for accurate modeling and fast simulations of HVDC projects. After analysis of existing literature, the areas with high potential impact on accuracy and acceleration of electromagnetic transient simulations are found, and it is the modeling of MMCs that is considered in this thesis. Thus, a significant part of this thesis is dedicated to research on efficient modeling techniques that allow to reduce simulation time and improve accuracy for MMC-based HVDC systems.

The modeling aspects and control systems of hybrid MMCs are presented first. The MMC models used in electromagnetic transient simulations are grouped into four categories. The detailed model represents the nonlinear current-voltage characteristics of semiconductor switches. The detailed equivalent model represents the switches as two-value resistances: a small value for the closed state and a large value for the open state. The arm equivalent model assumes all capacitors in each arm have identical voltages, so a single equivalent capacitor is used to represent the whole arm, thus greatly reducing the computational burden of the model. The average value model neglects the inner dynamics of arm capacitors and is based on the assumption that all six of them share an

identical constant voltage. A typical cascade control system based on two feedback loops is described in this thesis. It allows to operate the converter in various conditions.

It is demonstrated in this thesis that it is possible to remove initialization transients at the startup of simulations with accurate initialization of MMC models, which allows to considerably reduce computing times. The proposed iterative algorithm finds the steady-state solutions for two important variables in each arm of the MMC, namely, the arm switching function and the total capacitor voltage. These variables are then used to initialize the electrical circuit and the control system of the converter. Based on presented test results, this technique allows to save more than 50% of computing time.

Another approach to accelerate simulations is the transitioning between MMC models with different levels of details during time-domain simulations. It is proposed to use the least detailed and therefore the fastest model during the periods where the internal details of the converter are not of interest. Such is, for example, the initialization transient period at the beginning of simulations. More detailed MMC models are activated to perform detailed computations. The time-domain activation methods of various MMC models as well as two novel average value models are developed, which allows for smooth transitions between the MMC models. Depending on the simulation case, the proposed new approach can accelerate the computations by a factor of 10.

Considering the advances in parallel computer architectures, it is proposed in this thesis to parallelize the internal calculations of the detailed equivalent model (DEM) on multi-core processors. The calculations of the internal variables for all MMC arms are performed at the same time-point on separate threads, which allows to accelerate simulations. The acceleration gains resulting from parallelization increase as the number of submodules in the MMC and the number of threads used for parallelization increase. However, the acceleration factor tends to saturate as the number of threads increases. This is due to the amount of calculations that must still be performed in series, such as the solution of control system equations and modified augmented nodal analysis equations. The creation and management of multiple threads at each time-point also contributes to the reduction of the acceleration factor. The test results demonstrate that the DEM parallelisation can accelerate the computations by more than 5 times.

This thesis also demonstrates that the arm equivalent model can generate or consume considerable amounts of active power, which is not realistic since the MMC does not have significant internal

loads or sources of active power. The origin of such spurious power is found to be in the implementation of model's equations that are solved with one time-step delay relatively to the rest of the electrical circuit. An analytical formulation of spurious power as a function of grid parameters is derived and several methods to eliminate it are proposed. The advantages and disadvantages of the solutions are discussed, and their performances are then compared in steady-state and transient simulations.

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LIST OF SYMBOLS AND ABBREVIATIONS

AC alternating current

AEM arm equivalent model

AVM average value model

CBA capacitor balancing algorithm

CCSC circulating current suppression controller

CPU central processing unit

DC direct current

DCCB direct current circuit breaker

DEM detailed equivalent model

DLL dynamic-link library

DM detailed model

EMF electromotive force

EMT electromagnetic transient

EMTP electromagnetic transient program

FB full bridge

FPGA field-programmable gate array

GPU graphics processing unit

HB half bridge

HPF high-pass filter

HVDC high voltage direct current

IGBT insulated-gate bipolar transistor

LCC line commutated converter

LPF low-pass filter

MMC modular multilevel converter

MNE main network equations

MTDC multiterminal direct current

MUX multiplexer

NLC nearest level control

PCC point of common coupling

PI proportional-integral

PLL phase locked loop

PR proportional-resonant

PS phase shift

p. u. per unit

PWM pulse width modulation

RMS root mean square

SM submodule

UFD ultrafast disconnector

VSC voltage source converter

XLPE cross-linked polyethylene

LIST OF APPENDICES

CHAPTER 1 INTRODUCTION

1.1 Context and motivation

Renewable energy integration projects [1-3] provide a timely response to the growing concerns in the modern world for ecology and dependence on fossil fuels. However, the sources of renewable energy are often distant from the consumption centers, so large amounts of electric power must be transported over long distances. At the same time, the massive integration of renewable energy sources and increasing sophistication of modern power grids can have adverse effects on power system stability and reliability, leading to power outages and cascading failures [4, 5].

In such situations, High-Voltage Direct Current (HVDC) links (see Figure 1.1) can provide significant advantages over traditional Alternating Current (AC) transmission systems. HVDC systems can connect asynchronous areas and have no limits on transmission length, they have high performance controls, make better use of materials (peak and RMS values for currents and voltages are the same) and depending on the length of the transmission their losses can be smaller [6-8]. Besides, electric power grid performances can be further improved by extending point-to-point HVDC links to multiterminal DC networks, making the grid even more flexible and secure [9-11].

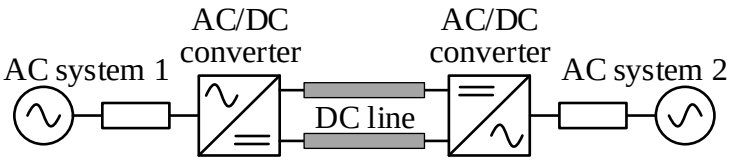


Figure 1.1 Typical point-to-point HVDC transmission

HVDC transmission projects require advanced analysis of performance in various operating modes and during transients due to the complexity of the equipment and high requirements in terms of stability, safety and reliability [12]. Therefore, computer simulations are performed at various stages of HVDC project lifetime: to determine component ratings and optimize equipment performance, to design control and protection systems, for prototyping and during factory acceptance tests, for maintenance and personnel training, for onsite event analysis [13-15]. To cover this multitude of applications, fast and accurate simulation tools are required. However, due to the complexity of modern power systems, detailed time-domain simulations are usually time-consuming [15-17]. Therefore, new methods must be researched to exploit different options for

reducing computing times and for improving simulation accuracy when dealing with HVDC transmission projects and grids.

1.2 Review of direct current grid equipment

Electric power transmission based on direct current (DC) has been established at the beginning of massive electrification in the nineteenth century. First HVDC projects, such as Lyon-Moutiers link built in France in 1906, used mechanical converters and therefore had limited practical application for large-scale power transmission [18]. It was not until the mid twentieth century that such transmissions began to be systematically used [8].

The main advantages of HVDC systems over conventional AC transmission include the ability to connect asynchronous areas, the absence of limitation on transmission distance which allows to use long submarine and underground cables, fast response times and high controllability of power transfer for improving the overall reliability of the electric system. The associated costs of complex components required for HVDC transmission could be covered by the reduction in the number of conductors, which makes HVDC systems also more economically beneficial over long distances. The break-even distance in cost for point-to-point transmissions is around 70 km for cables and 700 km for overhead lines but can vary depending on the voltage level [8, 19, 20].

The possibilities for multiterminal operation of HVDC systems have been researched since the early days of DC transmissions in 1960s, when the semiconductor technology was still maturing [21, 22]. The first multiterminal HVDC transmissions based on the Line Commutated Converter (LCC) technology [23] were proposed as an extension of two-terminal configurations to three terminals, where the third station would either be connected in parallel to the others, sharing the same DC voltage, or in series, sharing the same DC current [24]. Reportedly, the first multiterminal HVDC transmission was implemented in 1982, when the second bipole of the Nelson river HVDC system (Manitoba, Canada) was constructed in parallel to the first one [25-27]. Several years later, the first four terminal HVDC system was commissioned in Quebec [28, 29].

Several complications with such multiterminal configurations were reported compared to the point-to-point transmission systems: the need to operatively balance current references of all the stations, special circuit breakers for handling the faults on the DC side, high-level dispatching control, danger of overloading. To tackle such problems, some generic approaches allowing arbitrary

configurations for true multiterminal HVDC grid functionality were proposed [22, 23, 30]. However, LCC-based multiterminal DC (MTDC) grids have not found a wide application in electrical transmission systems.

HVDC grids based on the Voltage Source Converter (VSC) technology had been researched since early 1990s as means for replacing AC transmission and distribution systems. Due to their ability to supply passive networks they were supposed to be a promising candidate for urban distribution networks [9, 31, 32]. Today, VSC-HVDC systems are considered as the most appropriate option for the integration of large offshore wind farms, where power transmission requires long submarine cables. Besides, in such conditions an MTDC grid can smooth out the fluctuations of renewable energy production over a wide geographical area and improve reliability [31, 32].

Similar complications as with LCC-based multiterminal DC grids are encountered when a two-terminal VSC transmission is expanded to a multiterminal system: higher-level dispatch control is necessary, requiring reliable communication between the terminals. DC fault protection schemes and fast-acting DC circuit breakers are needed to maintain the DC grid in operation in case of a contingency. In addition, DC/DC converters may be necessary for more complex grids with different voltage levels [10, 31-34]. The first multiterminal VSC HVDC system was put in operation in 2013 in Nan'ao island in China to harness wind energy. It is based on Modular Multilevel Converter (MMC) technology [33, 35]. Today, this is one of the few operational multiterminal VSC HVDC systems.

As with AC networks, MTDC grids must possess various types of devices to be operational: AC/DC converters, DC transmission lines and cables, DC circuit breakers (DCCB), DC/DC converters, as well as appropriate control and protection systems [10, 36-38]. In this section, DC grid equipment is reviewed along with their modeling aspects. MMC modeling is discussed in a separate chapter, due to the large amount of information.

1.2.1 AC/DC converters

AC/DC converters can be considered as crucial elements in HVDC systems, allowing to interconnect the AC and DC parts of the electrical grid. Wide application of HVDC transmissions in the second half of the 20th century can be associated with the advances in power electronics, allowing for massive production of reliable silicon-based components [39, 40].

1.2.1.1 Line commutated converters

Historically, the application of power electronics in high-power HVDC technologies started with the thyristor-based line commutated converters, Figure 1.2. The basic principle of operation of LCCs consists in controlling the firing angle of the thyristors. The higher the angle, the lower the resulting DC voltage. Converter on one side of the transmission performs rectification and controls the transmitted power by adjusting the DC current i_{DC}. The other station acts as an inverter and usually controls the DC voltage v_{DC} [8, 41].

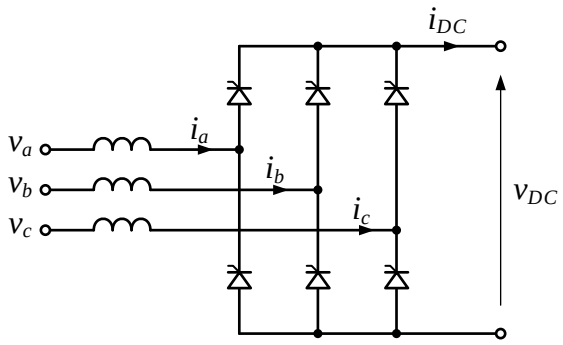


Figure 1.2 Thyristor-based line commutated converter

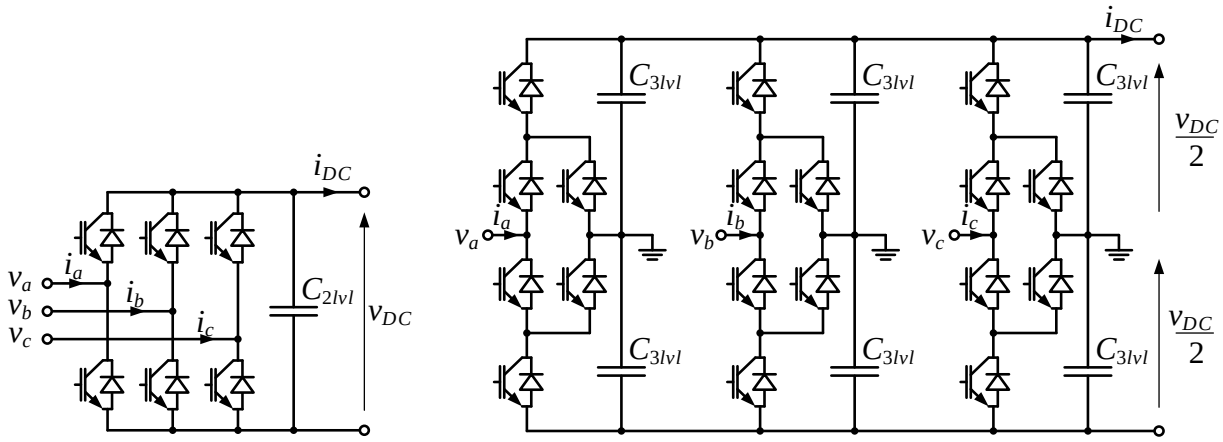
Main advantages of the LCC compared to other HVDC converters are relatively low losses and high power and voltage ratings. Important drawbacks of this technology are the high reactive power requirements, risks of inverter commutation failures, and high harmonic content of the AC side currents and DC voltage. Smoothing reactors, filters and a strong AC grid are needed to provide satisfactory operation [8, 19]. Also, the fact that the current direction cannot be rapidly reversed makes it difficult to construct a multiterminal DC grid [8, 19]. Most of the commissioned projects are thus point-to-point links or back-to-back systems. A multiterminal DC grid would require fast communication channels to properly dispatch scheduled power flows and to react to events and changes in the grid [42]. However, a few multiterminal projects have been commissioned and some are still in operation [25, 29, 35].

1.2.1.2 Voltage source converters

With the advent of fully controllable power electronic devices, i.e. devices that can be turned on and off depending on an external control signal, other AC/DC converter topologies emerged. Namely, the voltage source converters (see Figure 1.3). They first found their application in AC

motor drives, where smaller voltage and power ratings are required, as compared to HVDC technologies [40, 43, 44].

Various types of power electronic switches have been used, such as the Insulated Gate Bipolar Transistor (IGBT), gate-turn-off thyristor, metal-oxide semiconductor field effect transistors. In HVDC technologies, IGBTs are usually used. To achieve the required high voltage ratings, multiple IGBTs must be arranged in series [45].



a) two-level VSC b) three-level neutral point clamped VSC

Figure 1.3 Typical voltage source converter topologies

Classical two- and three-level VSCs are usually controlled using pulse-width modulation (PWM) techniques [45]. VSCs are more suitable for MTDC grid applications than LCCs, owing to their flexibility and rapidity, ability to operate in all four quadrants of the P-Q plane and with a quasi constant DC voltage. Moreover, VSCs are able to generate almost perfectly sinusoidal AC voltage waveforms and have black-start capability [46]. On the other hand, VSCs have higher losses compared to the LCCs [47]. They require high-frequency switching and filters to block the generated harmonics from propagating into the grid, although the harmonic content is lower than that of the LCC.

Since the development of VSC technology, increasing the number of voltage levels to generate smoother AC voltage waveforms was a questionable subject and converters with more than four levels were considered economically unfeasible due to the significant complexity of control and electrical circuits. Only two- and three-level VSCs have been practically used for high power HVDC transmissions until recently. Two configurations have been used for three-level converters:

diode-clamped and flying capacitors [44, 46, 48-50]. First real HVDC projects based on VSC technology were commissioned in the late 1990s and early 2000s [47, 49, 51-54].

1.2.1.3 Modular multilevel converters

Multilevel converters comprised of several identical modules with small voltage ratings have been researched for decreasing produced harmonics, switching frequencies and voltage gradients. This research started in the 1990s [55, 56]. A cascade structure of H-bridges with DC sources was introduced in 1996, which laid basis for what is now known as the MMC [57-59]. The MMCs were also first used for electric drives [60-62].

The advantages of MMC [63] technology include very low switching losses, high controllability, potential for DC fault current blocking and very low harmonic content. It can be possible to eliminate filters when the number of levels is sufficiently high. Modular structure allows for high scalability and improved reliability. Due to its advantages, the MMC is a cost-efficient and popular choice in modern HVDC projects. Several MMC-based HVDC projects have already been commissioned since 2010, including the Trans Bay Cable in America, INELFE in Europe and Nan'ao in China [15, 33, 64-68].

A typical MMC comprises six arms which are composed of valve (or arm) reactors L_{arm} and chains of series-connected submodules (SMs) which are essentially capacitors C_{SM} that can be either inserted into the current path or bypassed from it with the help of power electronic switches, Figure 1.4. In real projects, the number of SMs per arm N_{SM} can reach hundreds.

Until now, all commissioned projects included half-bridge SM-based MMCs and the Ultranet HVDC will be the first project to include the H-bridge submodules [69]. However, several different types of converters have been proposed in the literature, including the full-bridge (FB) SMs [70, 71], hybrid [72-74], and others [45, 75-77]. Hybrid MMCs, which combine the HB and FB-SMs in each arm, have the advantages of fault current blocking, DC voltage reversal, and overmodulation provided by the FB-SMs. At the same time, the installation costs compared to the FB-MMC-based systems are reduced due to HB-SM usage, which requires fewer IGBT switches. The number of FB-SMs in each arm (N_{FB}) in such hybrid MMCs is recommended to be above

70%. The number of HB-SMs (N_{HB}) is therefore below 30% [74]. SMs can have additional optional elements, such as the bypass thyristors, RC snubbers, discharge resistors.

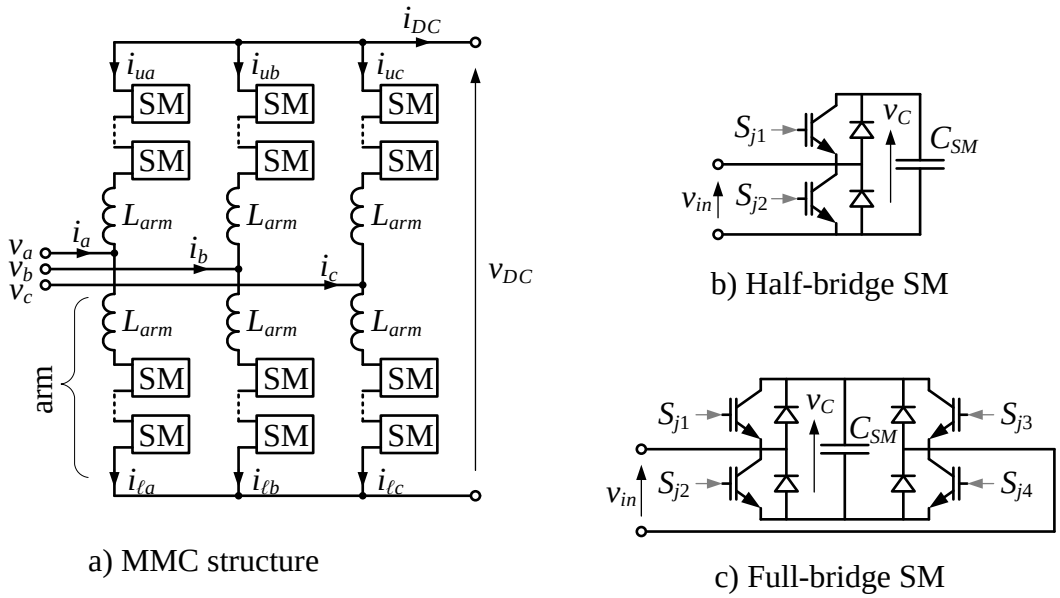


Figure 1.4 Modular multilevel converter

The desired AC voltage waveform is constructed by inserting the necessary number of SMs in each arm (assuming that the SM capacitor voltages are quasi-constant). Gating signals for the *j*-th HB-SM are defined as S_{j1} and S_{j2} for the upper and lower IGBTs, respectively. For the FB-SM, the gating signals are S_{j1}, S_{j2}, S_{j3}, and S_{j4}, as shown in Figure 1.4. Each IGBT can either be turned on ($S_{j1}=1$) or off ($S_{j1}=0$).

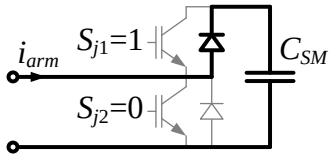
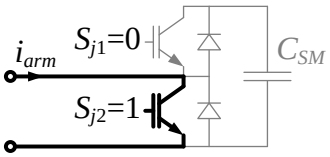
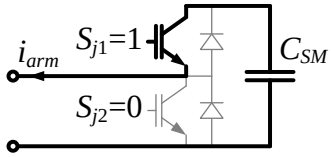
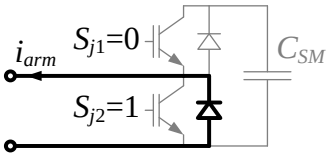
Several operating modes can be observed in HB- and FB-SMs:

- Short-circuit: both switches on at least one side are turned on (due to control misoperation for example).
- Abnormal discharge: due to discharging current, capacitor voltage reduces to zero.
- Normal: at each side one switch is turned on and the other is turned off.
- Blocked: both gating signals on at least one side are off.

In this list, HB-SMs are regarded as having only one side, FB-SMs have two sides. Among these operating modes, only the normal and blocked ones are usually of interest in grid-level studies.

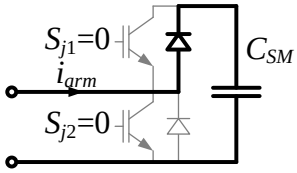
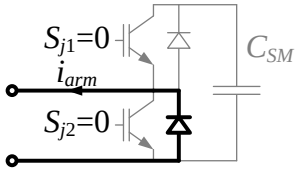
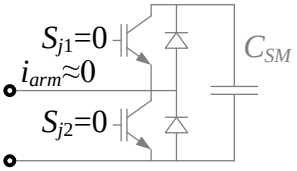
During normal operation, a HB-SM can either be positively inserted or bypassed. The FB-SMs can also be inserted negatively. When a SM is inserted, the arm current i_{arm} is passing through the SM capacitor. When the SM is bypassed, no current is flowing though the capacitor. The active elements in these conditions are defined by the arm current direction and IGBT switch states, as shown in Table 1.1 (solid black lines represent currently active elements). SM switching function S_j which represents the state of the j-th SM is introduced as: $S_j = 0$ for the bypass, $S_j = 1$ for the positive insertion, $S_j = -1$ for the negative insertion.

Table 1.1 Active elements in HB-SMs during normal operation

Arm current direction	**Inserted**	**Bypassed**
Positive arm current ($i_{arm} > 0$)		
Negative arm current ($i_{arm} < 0$)		

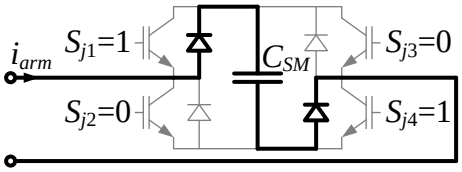
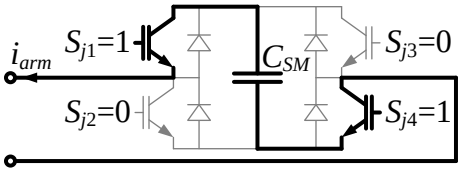
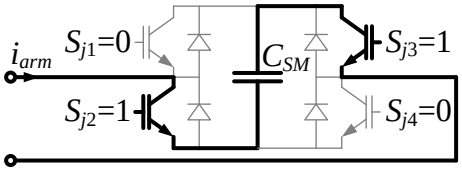
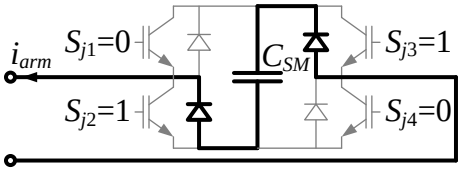
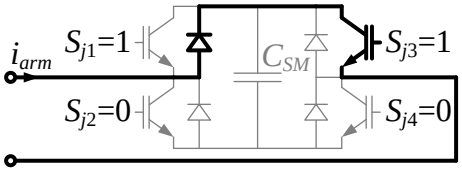
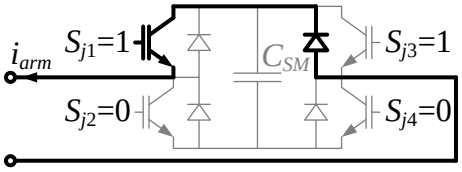
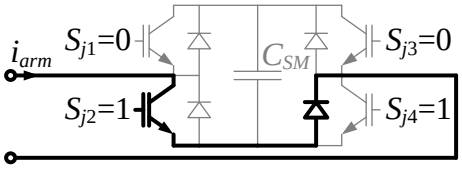
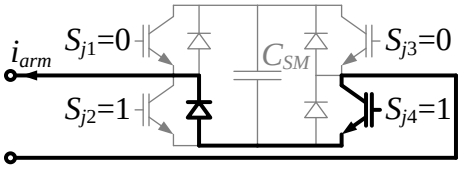
In the blocked mode, the active elements are defined by the arm current direction and capacitor voltage, Table 1.2. When the arm current is positive, SM capacitor is inserted; when the arm current is negative, the SM is bypassed and the voltage at its terminals is almost zero. High impedance state occurs when the voltage at the SM terminals is positive but is lower than the capacitor's voltage, so both diodes are negatively biased and therefore neither can pass current.

Table 1.2 Active elements in HB-SMs in blocked mode

Inserted ($i_{arm} > 0$, $v_{in} > v_C$)	**Bypassed** ($i_{arm} < 0$, $v_{in} < 0$)	**High impedance** ($0 < v_{in} < v_C$)
		

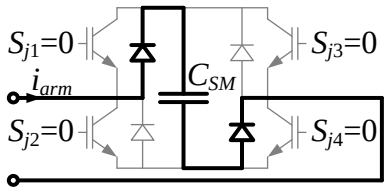
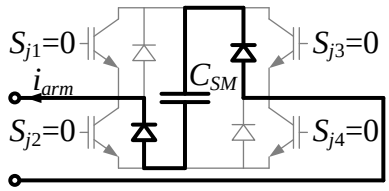
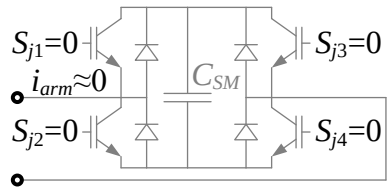
For a FB-SM to be inserted, the opposite IGBTs on the left and right side must be activated: S_{j1} with S_{j4} for the positive insertion (in this case the SM terminal voltage has the same polarity as the capacitor voltage) and S_{j2} with S_{j3} for the negative insertion (SM terminal voltage and capacitor voltage have opposite polarities). For the bypassed state, the same IGBTs on both sides must be activated: S_{j1} with S_{j3} or S_{j2} with S_{j4}, see Table 1.3.

Table 1.3 Active elements in FB-SMs during normal operation

Type	**Positive arm current ($i_{arm} > 0$)**	**Negative arm current ($i_{arm} < 0$)**
Positively inserted		
Negatively inserted		
Bypassed with upper switches		
Bypassed with lower switches		

When all IGBTs in a FB-SM are turned off, irrespective of the direction of the arm current, the SM capacitor is either always charging or is in the high-impedance state, Table 1.4. This provides the DC fault blocking capability. In the case when one IGBT is turned on, the SM is still considered blocked, but its behavior is similar to that of the HB-SM.

Table 1.4 Active elements in FB-SMs in blocked mode

Positively inserted ($i_{arm} > 0$, $v_{in} > v_C$)	**Negatively inserted** ($i_{arm} < 0$, $v_{in} < -v_C$)	**High impedance** ($-v_C < v_{in} < v_C$)
		

1.2.1.4 Modeling

AC/DC converter modeling has been a major research topic over the span of the last 60 years and many modeling aspects of LCCs and VSCs have been covered. In EMT-type studies, behavioral modeling approach is often used to represent the converters, which consists in replacing the internal details of complex nonlinear elements such as IGBT switches by simplified external characteristics such as the voltage-current curve [78]. This requires small simulation time-steps, nonlinear solvers, and, consequently, long computing times. Another option is to remove the internal details in IGBTs and use only ideal switch representation with a set of algebraic-differential equations for each configuration of the switches in the system [79-81]. However, this approach requires an initial analysis of the system and a large set of equations owing to the fact that each switch can be in two states, so the total number of configurations is 2^{ν} where ν is the number of switches. It is therefore hardly extensible and applicable to HVDC system studies. To reduce the computational burden and to remove the high-frequency switching details, average-value models are often used, where only the low-frequency components are represented using the voltage and current sources [82]. As a disadvantage, such an approach requires a preliminary steady-state analysis of the system to establish the steady-state behavior. As a more general approach, the power electronics switches are often conveniently represented using ideal switches in the modified augmented nodal analysis [83].

The structural complexity of the MMC is significantly higher than that of the LCC and conventional two- and three-level VSCs. Therefore, a lot of effort is put into efficient modeling of MMCs. Due to the significant amount of available information, modeling and control principles of the MMC are presented in a separate chapter (Chapter 2).

1.2.2 DC circuit breakers

Many authors point out that DCCBs are extremely important for reliable MTDC grid operation [84-86]. Instead of shutting the whole grid to clear a DC fault, DCCBs allow for uninterrupted operation of the grid by isolating only the faulty equipment. There are significant differences in DCCB operation compared to AC circuit breakers: DC fault current does not naturally cross zero, it exhibits high rate-of-rise and its value is high due to the smaller impedances of the DC transmission lines. To tackle these difficulties, new circuit breakers that can operate in such conditions have been proposed and demonstrated in literature. Such DCCBs are usually divided into three groups depending on the primary components used for the fault current interruption: mechanical, solid-state, and hybrid, combining mechanical and power electronics-based parts.

1.2.2.1 Mechanical

Several types of mechanical DCCB topologies are available [88, 89] and a mechanical DCCB based on a passive resonance circuit, is shown in Figure 1.5. It generates an oscillating current with the help of a pre-charged resonant branch $L_{res} - C_{res}$ which, superposed with the fault current, results in the zero crossing of the total current flowing through the mechanical switch SW [8, 87]. To bring the fault current to zero after the separation of SW contacts, an energy absorption branch R_{nonl} is placed in parallel. All mechanical DCCBs share the same main advantage: they have very low steady-state losses. However, such DCCBs are inherently slow due to the dynamics of the mechanical parts and require large-sized components. Besides, during commutation process, an electric arc is created between the contacts of the mechanical switch, which imposes thermal stress on the equipment.

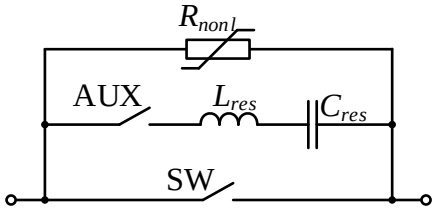


Figure 1.5 Resonant DC circuit breaker

1.2.2.2 Solid-state

Solid-state DCCBs (see Figure 1.6) are composed of power electronics switches connected in series, which results in rapid operation but significantly increases the steady-state conduction losses compared to mechanical DCCBs [90, 91]. Besides, fast commutating capabilities of solid-state DCCBs are infrequently used, which can be seen as an underusage of such an expensive equipment.

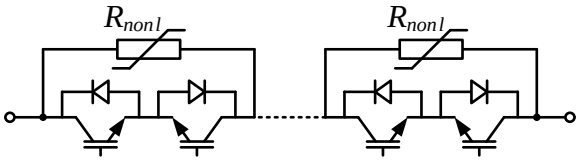


Figure 1.6 Solid-state DC circuit breaker

1.2.2.3 Hybrid

Hybrid DCCBs, Figure 1.7, are composed of three branches: mechanical, main switch, and energy dissipation branch [92-94]. In the normal conduction mode, the ultrafast disconnector (UFD) is closed and the DC current passes through the UFD and the commutation switch, which results in low steady-state losses. When the opening command is received, IGBTs of the commutation switch are turned off, which redirects the fault current to the main switch, where all IGBTs are in the conducting state. With no current flowing through, the UFD can separate its mechanical contacts without causing arcing. Finally, the IGBTs in the main switch are turned off and the fault current energy is dissipated in the energy absorption branch R_{nonl}. Hybrid DCCBs are commercially available and are planned to be installed in the Zhangbei project in China [95].

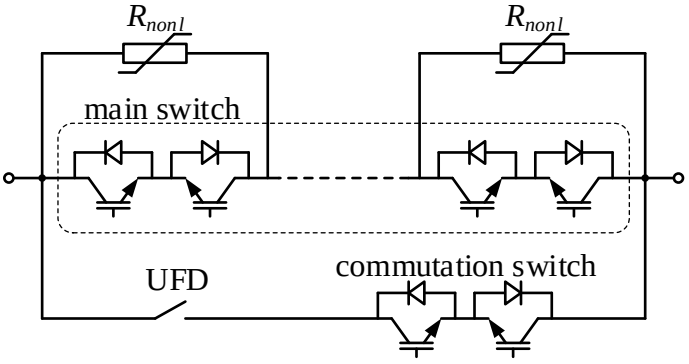


Figure 1.7 Hybrid DC circuit breaker

1.2.2.4 Modeling

Difficulties in modeling of mechanical DCCBs are related to the accurate representation of arcing [91, 96]. In hybrid DCCBs, arc representation is virtually unnecessary since the mechanical disconnector commutates small magnitude currents, which simplifies the modeling process [97]. Model details depend on the required EMT study type: for fault detection studies, modeling of the energy dissipation branch and a commutation delay are sufficient [98]. However, using ideal switches might give inaccurate results and therefore more detailed models are needed for accurate protection studies. Detailed modeling of DCCBs has been covered in literature [97, 99-101]. The residual mechanical switch and the fast disconnector of the DCCB can be represented with ideal switches with small residual current, the main and auxiliary IGBT switches can be modeled as variable resistances, and the surge arrester can be represented as a nonlinear resistance. As proposed in [99], a 'modular' approach could be used to create reusable modules for different branches. Internal control system and protection principles of DCCB are represented in [97]. Little information is available on the appropriate types of studies with models of different accuracy and influence of parameters [100].

1.2.3 DC/DC converters

DC/DC converters can have multiple uses in a DC grid. The converters with high stepping ratios can act as the traditional AC transformers in AC grids and would interconnect the parts of the DC grid with different nominal voltage levels. This can be used in offshore wind applications [102, 103]. Such converters can be based on front-to-front topology [104], which, similarly to a typical back-to-back HVDC configuration, includes two AC/DC converters but connected through the AC side, Figure 1.8. Both AC/DC converters actively participate in the control process, hence such configuration is called a dual active bridge (DAB). Voltage stepping and galvanic isolation between the two sides is provided by the transformer in the middle. The AC link does not have to operate at 50 or 60 Hz, its frequency can be increased significantly to reduce the size of the transformer.

For smaller transformation ratios, the DC/DC converters can act as power flow controllers [89] and divide a large DC grid into smaller areas for protection purposes [105]. Such converters can be based on various topologies and galvanic isolation may not always be present.

Until now, the DC/DC converters have been used only in low- and medium-voltage applications [106]. And although they are considered potentially useful in MTDC grids, high-power high-voltage DC/DC converters are yet to be seen in real HVDC projects.

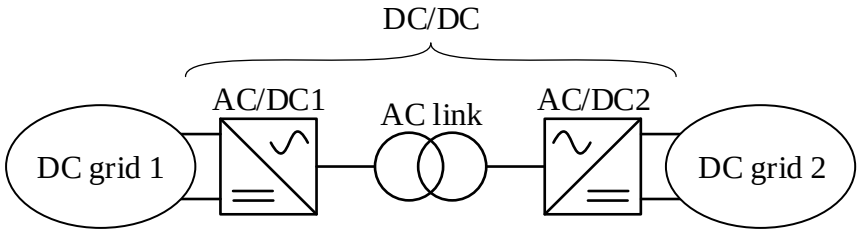


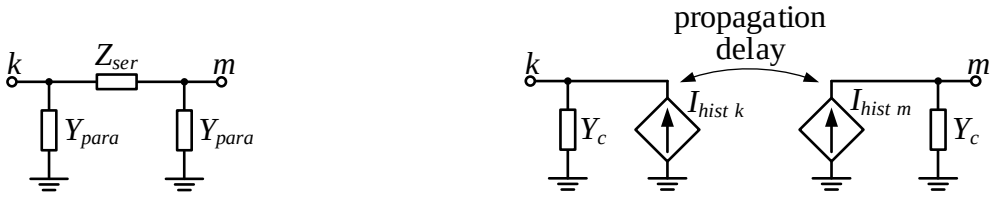
Figure 1.8 Front-to-front DC/DC converter

Modeling of the DC/DC converters has attracted some research interest [107-110]. In [111] converters are modeled as current sources in parallel with a capacitance, which is common for simplified AVMs of AC/DC converters. A common continuous MMC model is used in [109] for the DC/AC conversion stage and the simplified AVM model is used for the AC/DC rectification. However, the use of such simplified models can lead to incorrect results. A set of models with different levels of detail is established in [112] based on the MMC-DAB converter. The simplified linearized models were able to represent poorly damped modes otherwise only visible with the detailed models. Due to the higher frequencies of the AC link in the DC/DC converter, much smaller time-steps are necessary to accurately represent the transient phenomena. Transfer function representation is not suitable for such cases due to the one time-step delays introduced between the control and electrical system solutions if the time-step is not sufficiently small. A user-coded AVM including the control system equations is proposed in [110] as a solution to keep the desired accuracy at larger time-steps.

1.2.4 Lines and cables

Overhead lines, underground and submarine cables have been used in the HVDC transmissions. While overhead lines are usually more economically attractive, the final choice can be influenced by the cost of right-of-ways, landscape, esthetical, environmental, and ecological concerns [8, 89]. Cables used in the HVDC projects can have different types of insulation: mass-impregnated paper insulation, oil insulation, cross-linked polyethylene (XLPE). XLPE cables have been widely used in VSC-based transmissions. Current research focuses on the improvement of cable insulation [37].

Research on transmission line and cable modeling has attracted significant interest and many models with different accuracy levels have been developed in the literature, covering various possible operating conditions, study types, and frequency range phenomena. Line models are usually divided into two groups, as shown in Figure 1.9: lumped parameters, where a direct electrical connection exists between the two ends of the line, and distributed parameters, which can represent the travelling wave phenomena [113-115].



a) lumped parameters model b) distributed parameters model

Figure 1.9 Transmission line models

The latter group can further be subdivided into the constant and frequency dependent parameters. The choice of the model is usually associated with the frequency spectrum of the study: lumped parameter-type pi-sections are sufficiently accurate for low frequency studies, such as the DC or the fundamental frequency [116]. When faster transient processes are of interest, more detailed models that represent transmission delay provide better results. Current state-of-the-art model in terms of accuracy is the wideband or the universal line model [117], which represents the frequency dependence of line parameters and provides accurate results in a large frequency range, from DC to kHz and even MHz level. Its disadvantage is the high number of computations. Frequency-dependent models of cables is a challenging topic due to the complexity of the frequency dependence of cable parameters [118].

1.2.5 Conclusion

Different types of equipment are required for reliable operation of DC grids and many technological options are available for each type of equipment. Considering the recent advances is this area, it can be said that the modular multilevel converters are the most promising for future HVDC projects, being highly flexible in operation, reliable and energy-efficient. In meshed DC grids, the fault isolation can be provided by the hybrid DCCBs, that are currently introduced in actual projects.

It is important to maintain powerful EMT simulation tools to allow the engineers and researchers to perform different types of analysis on projected or existing HVDC systems. Considering various aspects of equipment modeling, it is the AC/DC converters, transmission lines and cables that receive the largest amount of attention from the researchers. This is due to various wideband phenomena that must be accurately represented and to high complexity of models and related control systems in the case of AC/DC converters. Research on modeling of other types of components, such as the DC/DC converters and DCCBs, is also active but to a lesser extent.

Considering the current state of development of DC grids, equipment modeling and potential impact, the following is concluded:

- The lack of real life HVDC projects involving DC/DC converters is a limiting factor, and that is why such converters are not researched in this thesis.
- Sufficiently advanced wideband line and cable models are currently available [117, 118] and will be reused in this thesis.
- The fact that DCCBs have already been introduced by manufacturers and are planned to be used in upcoming HVDC projects makes DCCB modeling another promising research topic. However, given the fact that several DCCB models are already available, [97-100] and the lesser importance of such models in HVDC transmissions, it was decided not to focus on this research topic.
- Therefore, this thesis will research primarily the modeling and simulation of MMCs, which are crucial for current and future HVDC transmission systems, to achieve better accuracy and reduce computing times.

The simulations in this thesis are performed in the EMTP software [83], but can be readily transposed into any other EMT-type simulation package.

1.3 Contributions

When dealing with computer simulations, accuracy and computing time are the two important aspects. This thesis attempts to cover both aspects by improving the modeling of MMCs for the simulation of HVDC systems and DC grids. Several methods to reduce computing times and improve accuracy are proposed. The contributions of this thesis are listed below.

1.3.1 Standalone MMC models

This thesis introduces two novel average value MMC models that do not require the separation of the AC and DC circuits, contrary to the existing average value models. This is useful for model relaxation in time domain simulations.

Two novel implementations of the arm equivalent model (AEM) using control system blocks are proposed. They allow to improve modeling accuracy.

An arm equivalent model of the hybrid MMC (Hybrid-AEM) is proposed, which closely replicates the behavior of more detailed models in terms of capacitor voltage dynamics. A block imitating the capacitor balancing algorithm (CBA) action in more detailed models is proposed for the Hybrid-AEM.

A memory pointer exchange scheme is developed for signal exchange between the detailed equivalent model and the CBA blocks, which allows to reduce the number of control signals managed by the EMT simulation software. Also, a new blocked mode algorithm is proposed.

1.3.2 Parallelization of the detailed equivalent model

A parallelization procedure for internal model calculations on multicore CPUs is proposed for the detailed equivalent model. It allows to significantly accelerate time-domain simulations by computing the model equations all at once instead of running them sequentially. The same approach is applied to the calculations of the capacitor balancing algorithm block.

1.3.3 Initialization of MMC models

A new initialization method for MMC models that include capacitor voltage dynamics is presented in the thesis. This method allows to calculate accurate initial values for all internal variables in the converter and its control system, and thus reducing computing times of EMT studies by eliminating the initialization transient at simulation startup. This method is also applicable to steady-state analysis of internal variables in MMCs.

1.3.4 MMC spurious power analysis

This thesis demonstrates that some MMC models can generate or consume considerable amounts of power which deteriorates simulation accuracy. The origin of such spurious power and its

quantification are demonstrated analytically for the AEM. Several solutions are proposed to eliminate the spurious power.

1.3.5 Adaptive MMC model

A model relaxation technique for MMCs is proposed in the thesis and methods for seamless transitions between various MMC models with different levels of detail are developed, including the appropriate control system blocks.

1.4 Thesis outline

This thesis contains the following seven chapters and two appendices.

Chapter 1 introduces the topic, available literature on the subject and the scope of research.

In chapter 2, hybrid MMC modeling and control techniques are presented.

Chapter 3 presents a novel initialization method for modular multilevel converter models.

Chapter 4 builds upon the initialization method presented in the previous chapter and proposes an adaptive modular multilevel converter model.

In chapter 5, a new parallelization technique for the detailed equivalent model is presented.

Chapter 6 demonstrates the analysis of the spurious power in the arm equivalent model of modular multilevel converter and proposes solutions for eliminating it.

Chapter 7 provides the summary of the thesis, conclusions, and recommendations for future work.

CHAPTER 2 MODULAR MULTILEVEL CONVERTER MODELS AND CONTROL

In EMT-type simulations it is common to use different models for the same simulated system. The choice of the model depends on the type of study and represents a compromise between tolerable computational burden and desired accuracy. As it has been outlined in Chapter 1, subsection 1.2.1.4, several electromagnetic transient models have been proposed for the conventional VSCs. Owing to the high complexity of the MMC, many MMC models with different levels of details have also been proposed for real-time and offline EMT simulations. Usually, four different types of models are used: the detailed model (DM), the detailed equivalent model (DEM), the arm equivalent model (AEM) and the average value model (AVM) [119]. These models and relationships between them are shown schematically in Figure 2.1 for the case of HB-SM based MMC. They will be discussed in detail further in this chapter.

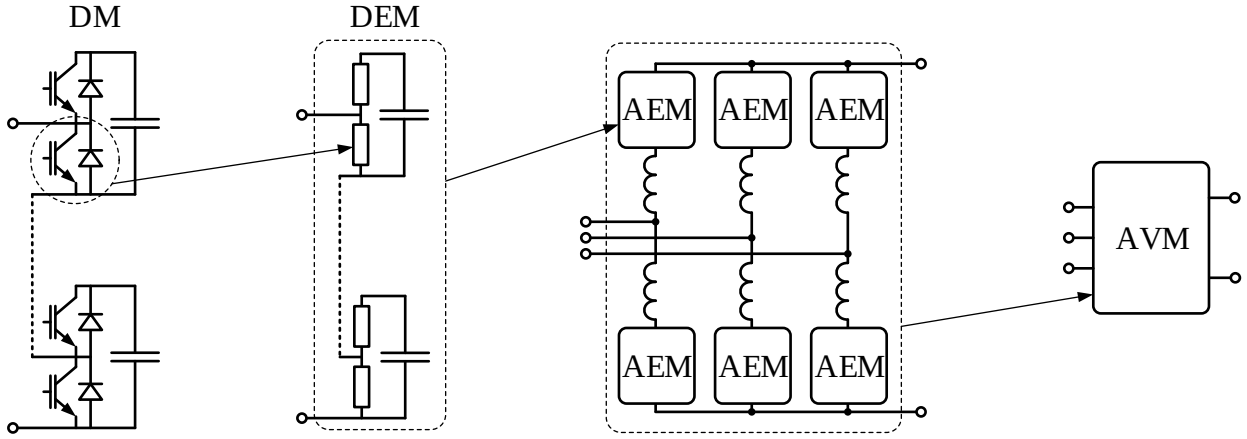


Figure 2.1 Overview of MMC models for EMT simulations

In this chapter, the hybrid MMC models that will be used in this thesis are presented. The concepts of the presented models for hybrid MMC are taken from existing literature on half-bridge MMCs and adapted to the hybrid configuration. The MMC control system presented in this chapter is based on the classical double feedback loop cascade structure [120].

In the following, lowercase letters represent variables, capital letters represent constants, and bold capital letters represent arrays of variables. By default, the time point at which any variable is taken is t. It will be omitted unless other instants are used.

2.1 Detailed model

The detailed model of the MMC includes the nonlinear IGBT v-i characteristics and offers the highest degree of precision in EMT studies [119]. Each SM capacitor C_{SM}, IGBT switches, and other elements, which can include RC snubbers (R_{snub} , C_{snub}), discharge resistors, bypass thyristors, etc. (see Figure 2.2), are represented and solved in the main network equations matrix. The DM can be used to validate simplified models, for SM-level studies and internal fault studies [89]. However, its application in grid studies is limited because of the high number of nonlinearities, internal nodes, and control signals, which makes simulations time-consuming. Such a model requires an EMT solver capable of efficiently simulating nonlinear elements, which is the case of EMTP.

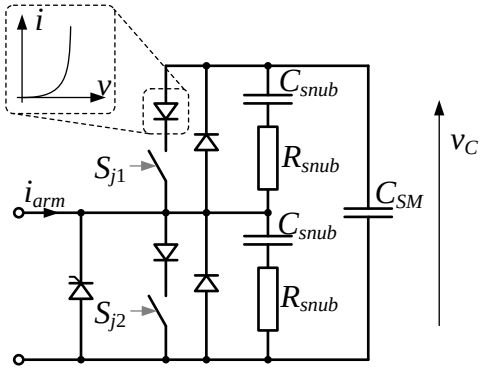


Figure 2.2 Detailed model of j-th HB-SM with snubbers

2.2 Detailed equivalent model

The detailed equivalent model represents the power switches (i.e. the IGBT and the antiparallel diode) as two-value resistances [119, 121]: the conducting switches have a low resistance R_{ON} (in the order of mΩ) whereas the turned off ones have a high resistance R_{OFF} (in the order of MΩ). In this model, all individual SM voltages and gating signals are available. The DEM is often implemented independently from the main EMT solver and is interfaced with it using a two-port Thevenin or Norton equivalent circuit [89].

2.2.1 SM equivalent circuit

Internally, each SM in the DEM implementation used in this thesis is represented by an equivalent circuit as in Figure 2.3. The SM capacitor C_{SM} is discretized using the trapezoidal integration rule, yielding a resistance and a history current source i_{hist} connected in parallel

$$C_{SM}\frac{dv_C}{dt} = i_C \tag{2.1}$$

$$\frac{v_C(t) - v_C(t-\Delta t)}{\Delta t} = \frac{i_C(t) + i_C(t-\Delta t)}{2\,C_{SM}} \tag{2.2}$$

$$i_C(t) = \frac{1}{R_C}v_C(t) - \left[\frac{1}{R_C}v_C(t-\Delta t) + i_C(t-\Delta t)\right] \tag{2.3}$$

$$i_{hist}(t) = \frac{1}{R_C}v_C(t-\Delta t) + i_C(t-\Delta t) \tag{2.4}$$

where $R_C = 0.5\Delta t / C_{SM}$ is the capacitor discretization resistance, v_C and i_C are the capacitor voltage and current respectively, and Δt is the numerical integration time-step.

a) HB-SM b) FB-SM

Figure 2.3 Detailed equivalent model of j-th SM

With Backward-Euler method using a halved time-step $\Delta t / 2$, the history current is calculated as

$$i_{hist}(t) = \frac{1}{R_C}v_C(t-\Delta t) \tag{2.5}$$

The resistance R_C obtained from the SM capacitor discretization is split into two parallel ones with the value of $2R_C$ to simplify the derivation of FB-SM equivalent circuit shown in Figure 2.4. With this, the FB-SM Thevenin equivalent circuit is calculated as:

$$R_k = 2\,R_C\;R_{j1} / \left[2\,R_C + R_{j1} + R_{j2}\right] \tag{2.6}$$

$$R_l = 2\,R_C\;R_{j2} / \left[2\,R_C + R_{j1} + R_{j2}\right] \tag{2.7}$$

$$R_m = 2\,R_C\;R_{j3} / \left[2\,R_C + R_{j3} + R_{j4}\right] \tag{2.8}$$

$$R_n = 2\,R_C\;R_{j4} / \left[2\,R_C + R_{j3} + R_{j4}\right] \tag{2.9}$$

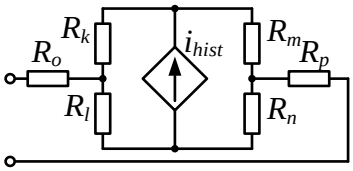
$$R_o = R_{j1}\;R_{j2} / \left[2\,R_C + R_{j1} + R_{j2}\right] \tag{2.10}$$

$$R_p = R_{j3}\;R_{j4} / \left[2\,R_C + R_{j3} + R_{j4}\right] \tag{2.11}$$

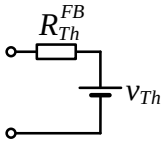
$$R_{Th}^{FB} = R_o + R_p + \frac{\left[R_k + R_m\right]\left[R_l + R_n\right]}{R_k + R_l + R_m + R_n} \tag{2.12}$$

$$k_{hist}^{FB} = \frac{R_l\;R_m - R_k\;R_n}{R_k + R_l + R_m + R_n} \tag{2.13}$$

$$v_{Th} = k_{hist}^{FB}\;i_{hist} \tag{2.14}$$



a) intermediate solution



b) final Thevenin circuit

Figure 2.4 FB-SM equivalent circuit derivation

The Thevenin equivalent is derived for HB-SMs as:

$$r_{Th}^{HB} = R_{j2}\,\frac{R_C + R_{j1}}{R_C + R_{j1} + R_{j2}} \tag{2.15}$$

$$k_{hist}^{HB} = \frac{R_C\;R_{j2}}{R_C + R_{j1} + R_{j2}} \tag{2.16}$$

$$v_{Th} = k_{hist}^{HB}\;i_{hist} \tag{2.17}$$

The values of R_{Th}^{FB}, R_{Th}^{HB}, k_{hist}^{FB}, and k_{hist}^{HB} may be precalculated for each possible combination of switch states and stored in memory for faster access.

2.2.2 Grouping

All SMs are connected in series, so the final Norton equivalent circuit of the arm is obtained as:

$$v_{Th}^{arm} = \sum_{j=1}^{N_{SM}} v_{Th\,j} = \sum_{j=1}^{N_{SM}} \left(k_{hist\,j}\; i_{hist\,j} \right) \tag{2.18}$$

$$y_{Nort} = \frac{1}{\sum_{j=1}^{N_{SM}} r_{Th\,j}} \tag{2.19}$$

$$i_{Nort} = y_{Nort}\; v_{Th}^{arm} \tag{2.20}$$

where N_{SM} is the number of SMs in the arm.

For all FB-SMs with the same states of switches, i.e. with the same values of R_{j1}, R_{j2}, R_{j3}, and R_{j4} (see Figure 2.3), equations (2.12) and (2.13) will give the same result, and only i_{hist} will change in (2.14). The same reasoning is applicable to the HB-SM equations (2.15)–(2.17). Therefore, instead of calculating the Thevenin equivalent circuits of each SM individually, the SMs with the same states of switches are grouped together to accelerate the simulation.

Grouping is performed in the following way: SM history currents are summed and the number of SMs in the group is calculated, which gives only one summation and one increment for each SM, which reduces the number of computations per time-step. The calculations for a group g with N_g SMs are as follows:

$$r_{Th}^{g} = \sum_{j=1}^{N_g} r_{Th\,j} = N_g\; r_{Th\,1} = N_g\; r_{Th\,2} = \ldots = N_g\; r_{Th\,N_g} \tag{2.21}$$

$$v_{Th}^{g} = k_{hist}^{g} \sum_{j=1}^{N_g} i_{hist\,j} \tag{2.22}$$

The Norton equivalent of the arm is obtained by combining all groups:

$$y_{Nort} = \frac{1}{\sum_{g} r_{Th}^{g}} \tag{2.23}$$

$$i_{Nort} = y_{Nort} \sum_{g} v_{Th}^{g} \tag{2.24}$$

2.2.3 Submodule states

As explained in Chapter 1, subsection 1.2.1.3, SMs can be in different operating states: normal, blocked, short-circuit, abnormal discharge. These states are used to assign the values of the power switch resistances in the DEM implementation used in this thesis. It can be argued that theoretically FB-SMs can be in more than one state at the same time. For example, short-circuited on one side and high-impedance blocked on the other. However, to simplify the treatment without seriously compromising the accuracy of the model, it is postulated that only one state is enough to correctly represent each SM. The following priority order is defined for the SM states (from highest to lowest): short-circuit, abnormal discharge, normal, blocked. So, if a FB-SM is short-circuited on one side and blocked on the other, it is the short-circuit state that takes precedence.

2.2.3.1 Short-circuit state

Several short-circuit states are possible for FB-SMs. However, a simplification can be made as to use only one, since in any of them the capacitor will be quickly discharged and there will be no significant contribution from the submodule to the arm equivalent.

Therefore, in HB- and FB-SMs all switches are activated when the short-circuit command is received. To avoid numerical oscillations in the capacitor voltage following a short-circuit, the model can request to switch to the Backward-Euler integration technique for the next time-point.

2.2.3.2 Abnormal discharge state

If the capacitor voltage reduces to zero due to discharging current and eventually becomes negative, all antiparallel diodes will start to conduct. To model this behavior, all power switch resistances are assigned the low resistance value R_{ON}. Another possibility could be to manually impose capacitor voltage to zero as soon as it discharges, however this makes the modeling approach less generic and therefore such an approach is not retained.

2.2.3.3 Normal state

In normal operation, FB-SMs can be either positively inserted ($S_{j1} = S_{j4} = 1$ and $S_{j2} = S_{j3} = 0$), negatively inserted ($S_{j1} = S_{j4} = 0$ and $S_{j2} = S_{j3} = 1$), or bypassed (either $S_{j1} = S_{j3} = 1$ and $S_{j2} = S_{j4} = 0$ or $S_{j1} = S_{j3} = 0$ and $S_{j2} = S_{j4} = 1$). SMs in these modes are grouped separately. The same is applicable for the two possible normal states of HB-SMs: inserted or bypassed.

2.2.3.4 Blocked state

The diodes are assigned the small resistance value R_{ON} when the voltage across them becomes positive and the high resistance value R_{OFF} when the current becomes negative, as fixed forward voltage drop on the diodes is neglected in this model. Since the switches are modeled as resistances, the following simplification is made: in blocked SMs, the states of freewheeling diodes are set by the arm current direction. This state must be treated last since the arm current direction is not known before the solution at the time-point t.

2.2.4 Blocked mode

In the blocked mode, SM insertion is determined by the arm current direction and capacitor voltage of each equivalent part (HB or FB). The proposed arm-level algorithm to solve the DEM circuit in these conditions is as follows:

1. get the arm voltage v_{arm} from the EMT solver.
2. assign the diode states according to i_{arm} direction at the previous time-point and recalculate i_{arm}. If the newly calculated i_{arm} direction matches the diode states, exit.
3. if not, assign the diode states using the opposite current direction and recalculate i_{arm}. If the new current direction matches the new diode states, exit.
4. if it is impossible to match the i_{arm} direction and the diode states, assign the high-impedance state and exit.

The steps of this algorithm are shown schematically in Figure 2.5 and the corresponding electrical circuits in case of an arm with one HB-SM and one FB-SM are shown in Figure 2.6 for each step of the algorithm.

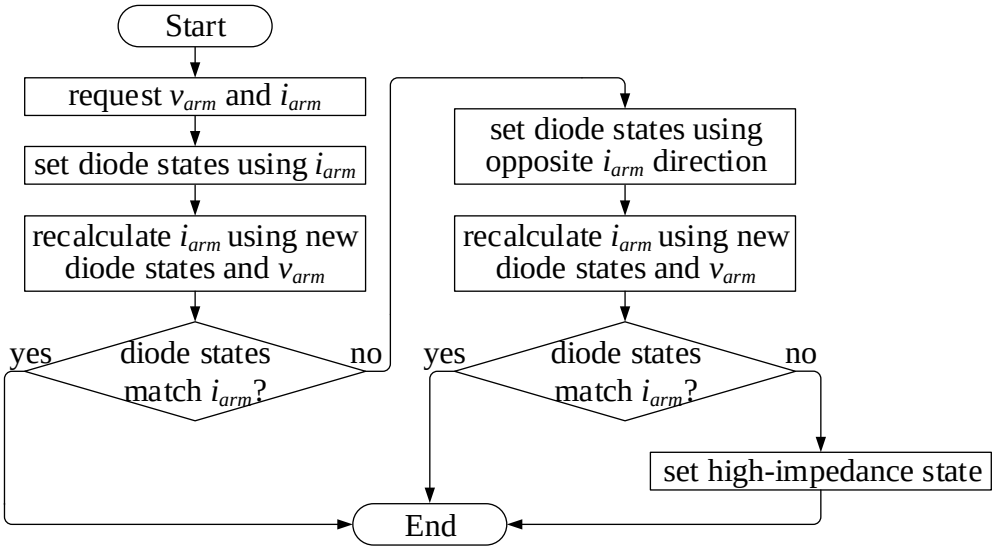
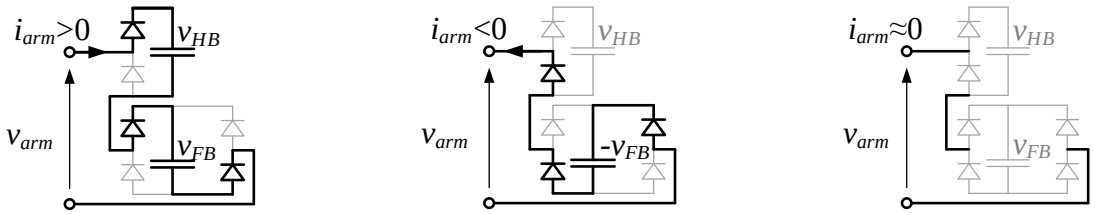


Figure 2.5 DEM blocked mode algorithm for one arm



a) with previous i_{arm} direction b) with opposite i_{arm} direction c) high-impedance mode

Figure 2.6 Blocked mode algorithm in case of positive arm current direction

2.2.5 Limitations of the blocked mode algorithm

Several assumptions are made in the blocked mode algorithm described above: first, it is supposed that all SMs in each arm change their conduction mode simultaneously, which is not entirely correct, since each SM has a different capacitor voltage, which might lead to some SMs being in the high impedance mode and some others being positively or negatively inserted. However, treating each SM as an independent nonlinear circuit would necessitate implementing a more

advanced algorithm which can considerably increase computational time. Besides, considering that often all SMs have rather similar voltages, this simplification does not produce significant errors.

Another source of errors is the assumption that the arm current only flows through the ON-state resistances and therefore has the same direction as the diode current. But when small time-steps and/or small values of OFF-state resistance are used, this assumption can be violated. For example, if a single HB-SM is considered with $R_{j1} = R_{ON}$ and $R_{j2} = R_{OFF}$, when the input voltage is located between the following boundaries with a positive i_{hist}, a violation can occur:

$$i_{hist}\ R_C \frac{R_{j2}}{R_C + R_{j1} + R_{j2}} < v_{arm} < i_{hist}\ R_C \tag{2.25}$$

In such a case, the current through the upper switch i_{Sj1} is

$$i_{Sj1} = \frac{i_{hist}\ R_C - v_{arm}}{R_{1j} + R_C} > 0 \tag{2.26}$$

The arm current is then equal to

$$\begin{aligned} i_{arm} &= -i_{Sj1} + i_{Sj2} = \frac{v_{arm} - i_{hist}\ R_C}{R_{j1} + R_C} + \frac{v_{arm}}{R_{j2}} = \frac{v_{arm}\left[R_{j1} + R_{j2} + R_C\right] - i_{hist}\ R_C\ R_{j2}}{\left[R_{j1} + R_C\right] R_{j2}} \\ &= \frac{R_{j1} + R_{j2} + R_C}{\left[R_{j1} + R_C\right] R_{j2}} \left[v_{arm} - i_{hist}\ R_C \frac{R_{j2}}{R_{j1} + R_{j2} + R_C} \right] > 0 \end{aligned} \tag{2.27}$$

In this case, the blocked mode algorithm concludes that the diode states are assigned correctly since the initial assumption and the result both indicate a positive arm current, but from (2.26) it is obvious that R_{j1} should have R_{OFF} value based on the direction of the current through the upper diode i_{Sj1}. This contradiction demonstrates that it is not enough to check only the arm current direction to confirm the validity of the assigned states, and additional validation must be performed that takes into account arm voltage. The validation can be based on the diode current direction as in (2.26). Another possibility is to use the equivalent SM resistance r_{eq}:

$$r_{eq} = \frac{v_{arm}}{i_{arm}} = \frac{v_{arm}\left[R_{j1} + R_C\right]R_{j2}}{v_{arm}\left[R_{j1} + R_{j2} + R_C\right] - i_{hist}\ R_C\ R_{j2}} = \\ = \frac{\left[R_{ON} + R_C\right]R_{OFF}}{R_{ON} + R_{OFF} + R_C - i_{hist}\ R_C\ R_{OFF} / v_{arm}} = R_{OFF}\ \frac{R_{ON} + R_C}{R_{ON} + R_C - R_{OFF}\left[\alpha - 1\right]} \tag{2.28}$$

where $\alpha = i_{hist}\ R_C / v_{arm}$.

The condition (2.25) can then be rewritten as

$$1 < \alpha < \left(1 + \frac{R_{ON} + R_C}{R_{OFF}}\right) \tag{2.29}$$

So, from (2.28) and (2.29) it can be concluded that the indicator for condition violation is:

$$\frac{v_{arm}}{i_{arm}} > R_{OFF} \tag{2.30}$$

Similar condition can be demonstrated for FB-SMs in blocked mode: if a SM is positively inserted, the same equation applies. If a FB-SM is negatively inserted, the equivalent resistance changes the sign.

Considering the assumption that all SMs have similar capacitor voltages (and therefore history currents), all SMs can be checked together for this condition violation:

$$\left(\left|\frac{v_{arm}}{i_{arm}\ N_{SM}}\right| > R_{OFF}\right) \Rightarrow \text{violation} \tag{2.31}$$

Another condition violation can occur when the bypassed mode is assigned using only the arm current direction. For the HB-SMs, it is the R_{j2} that is kept in the conducting state by the negative arm current while its own current is the opposite. In this case, it is enough to check the input voltage:

$$\left(v_{arm} > 0\right) \Rightarrow \text{violation} \tag{2.32}$$

For the bypassed FB-SMs that have one switch activated by the control system, the indicator of the violation is

$$\left(\left| \frac{\sum i_{hist}}{i_{arm}\, N_{SM}} \right| > \frac{R_{OFF}}{R_C} \left[1 + \frac{2\, R_C}{R_{ON} + R_{OFF}} \right] \right) \Rightarrow \text{violation} \tag{2.33}$$

Equations (2.31)–(2.33) allow to perform additional checks to make sure that the diode conduction states are accurately assigned. If any of the condition is violated at the steps 2 or 3 of the blocked mode algorithm (see subsection 2.2.4), the current step is invalidated, and the high impedance mode is assigned.

2.2.6 Iterative solution

During normal operation (i.e. no blocked and no discharged SMs), the Norton equivalent values (2.23) and (2.24) supplied to the EMT solver are uniquely defined by the control input and history currents. Since these values do not change until the next time-point, there is no need to iterate the electrical circuit solution because the DEM will always yield the same Norton equivalent. There is also no need to iterate when the blocked SMs are present if the arm current direction and the type of blocked mode do not change, since the same states will be assigned to the switches, thus producing the same Norton equivalent.

Iterations for the solution of the main network equations (MNE) are requested when the arm current changes its direction in the blocked mode, when the high impedance mode is activated or deactivated, and when SMs are discharged or start charging from the discharged state. If such conditions are detected in at least one arm, a request is sent to the EMT core to iterate the solution at the current time-point one more time. Iterations continue until the same current direction, blocked mode and discharged state are maintained for two consecutive iterations for all arms. Since there is no guarantee that this iterative process converges, a limit number of iterations per time-step is assigned (30 in this thesis). In the performed simulations, a stable solution is usually found in less than four iterations. The limit number of iterations could sometimes be reached in simulations with relatively large time-steps – in the order of 50 μs – if blocked FB-SMs have one of IGBTs still turned on and some of them are 'positively' blocked ($S_{j1} = 1,\ S_{j2} = S_{j3} = S_{j4} = 0$) while others are 'negatively' blocked ($S_{j1} = 0,\ S_{j2} = 1,\ S_{j3} = S_{j4} = 0$).

The algorithm for requesting the EMT software to iteratively resolve the MNE system at the current time-point is shown in Figure 2.7.

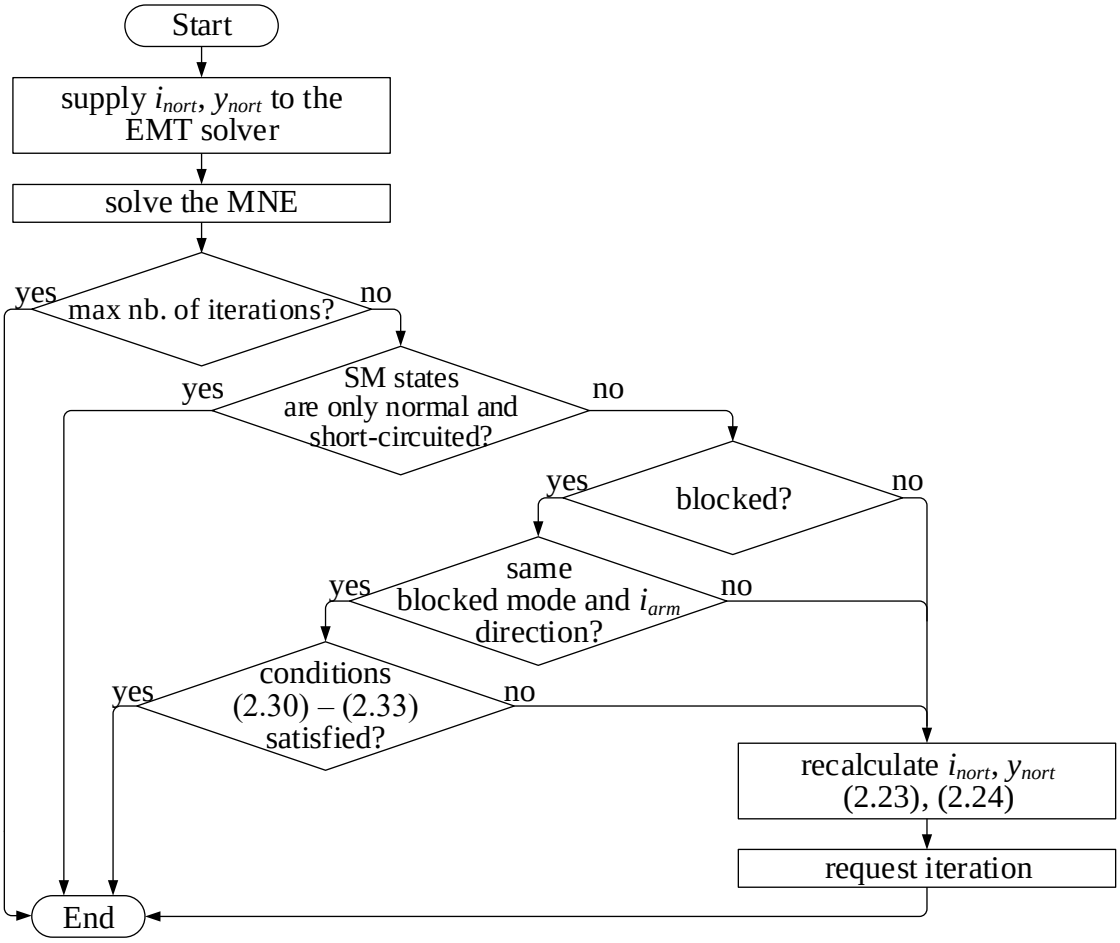


Figure 2.7 Iterative solution algorithm

2.3 Arm equivalent model

The arm equivalent model, Figure 2.8, assumes that all SM capacitors in each arm have identical voltages, so only one equivalent capacitor C_{arm} (2.35) is used to represent the whole arm [119, 122]. Grid studies and controller design can be performed [89]. The following variables are usually defined to build the AEM:

The arm switching function s_{arm} represents the state of the submodules in the whole arm. It is the proportion of the inserted SMs to the total number of SMs:

$$s_{arm} = \frac{1}{N_{SM}} \sum_{j=1}^{N_{SM}} S_j \tag{2.34}$$

The arm capacitor C_{arm}:

$$C_{arm} = C_{SM} / N_{SM} \tag{2.35}$$

The arm resistance R_{arm} represents the conduction losses of the converter considering that one IGBT is conducting in HB-SMs and two IGBTs conduct in FB-SMs:

$$R_{arm} = N_{HB}\, R_{ON} + 2N_{FB}\, R_{ON} \tag{2.36}$$

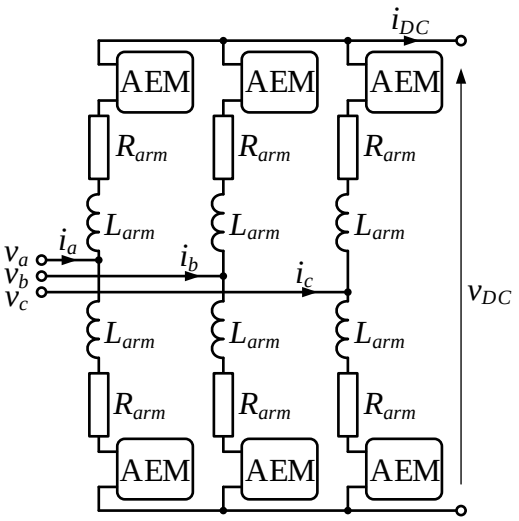
Since all SMs in each arm have identical voltages, the following equations for the normal operation mode can be written considering (2.34) and (2.35):

$$v_{arm} = s_{arm}\, v_{Ctot} \tag{2.37}$$

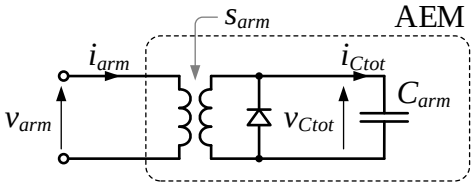
$$i_{Ctot} = s_{arm}\, i_{arm} \tag{2.38}$$

$$\frac{d}{dt} v_{Ctot} = \frac{i_{Ctot}}{C_{arm}} \tag{2.39}$$

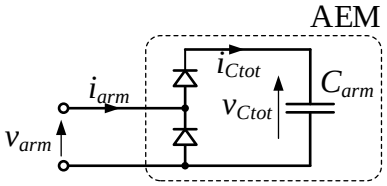
During normal operation, the arm switching function acts as a variable ideal transformer ratio between the arm capacitor and the rest of the circuit, which is schematically shown in Figure 2.8.b. When FB-SMs are used, the value of s_{arm} can become negative to represent negative insertion.



a) converter structure using the AEM



b) circuit for the normal operation

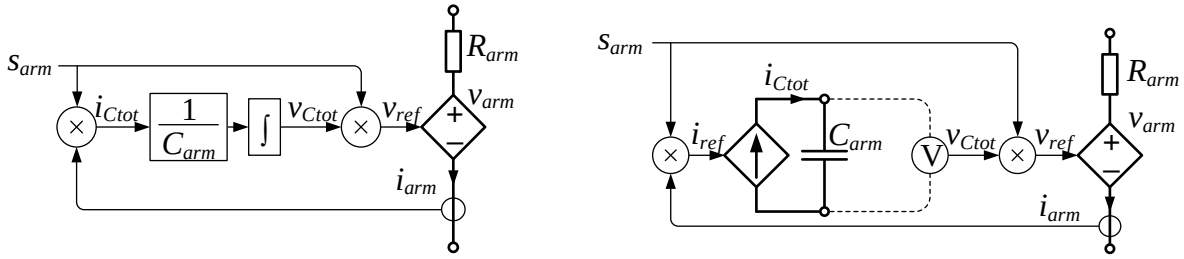


c) circuit for the blocked mode

Figure 2.8 Arm equivalent model of the HB MMC

Different implementations of the AEM exist [119, 123, 124]. The model equations (2.37)–(2.39) can be incorporated into the MNE matrix of the EMT-type simulation software and can be solved simultaneously with network equations.

Another possibility is to implement the model equations using the control diagram blocks of the EMT software, Figure 2.9 [125, 126]. In this case, the disadvantage is that the model equations are solved with a one time-step delay relatively to the rest of electrical network equations, which can result in the generation or consumption of the active power, as will be demonstrated in Chapter 6.



a) Classical-AEM-1 b) Classical-AEM-2

Figure 2.9 AEM implementations using control blocks

2.3.1 Hybrid-AEM

In this subsection, a Hybrid-AEM that comprises both HB- and FB-SMs is proposed. The HB and FB parts must be treated separately because their behavior differs in the blocked mode and when the SMs are to be inserted negatively (so only the FB-SMs can be inserted). The proposed Hybrid-AEM can operate in two states: active and high impedance. In the active operation state, the Thevenin equivalent circuits for each arm are found using the trapezoidal integration rule [123]. For the HB part:

$$r_{th\,HB} = R_{ON}\ N_{HB} + n_{HB}^2\ R_C / N_{HB} \tag{2.40}$$

$$v_{th\,HB} = n_{HB}\ \hat{v}_{HB} \tag{2.41}$$

For the FB part:

$$r_{th\,FB} = 2R_{ON}\ N_{FB} + n_{FB}^2\ R_C / N_{FB} \tag{2.42}$$

$$v_{th\,FB} = n_{FB}\ \hat{v}_{FB} \tag{2.43}$$

where $r_{th\,HB}$ and $r_{th\,FB}$ are the Thevenin equivalent resistances; $v_{th\,HB}$ and $v_{th\,FB}$ are the Thevenin equivalent voltages for the HB and FB parts, respectively; n_{HB} and n_{FB} are the number of HB- and FB-SMs to insert; $\hat{v}_{HB}$ and $\hat{v}_{FB}$ are the history voltages of HB and FB branches which are calculated at each time-point as:

$$\hat{v}_{HB} = v_{HB} + n_{HB}\, i_{arm}\, R_C\, N_{HB} \tag{2.44}$$

$$\hat{v}_{FB} = v_{FB} + n_{FB}\, i_{arm}\, R_C\, N_{FB} \tag{2.45}$$

where v_{HB} and v_{FB} are the voltages of HB and FB branches, respectively.

If the Hybrid-AEM is in the high impedance state (blocked mode), the Thevenin equivalent circuits are calculated as

$$r_{th\,HB} = R_{OFF}\, N_{HB} \tag{2.46}$$

$$r_{th\,FB} = 2\, R_{OFF}\, N_{FB} \tag{2.47}$$

$$v_{th\,HB} = v_{th\,FB} = 0 \tag{2.48}$$

The final Norton equivalent of the Hybrid-AEM that is supplied to the EMT solver is obtained from the series connection of the HB and FB Thevenin equivalents:

$$y_{Nort} = \frac{1}{r_{th\,HB} + r_{th\,FB}} \tag{2.49}$$

$$i_{Nort} = \frac{v_{th\,HB} + v_{th\,FB}}{r_{th\,HB} + r_{th\,FB}} \tag{2.50}$$

For the blocked mode, the approach from the DEM blocked mode is taken (see section 2.2.4) with all HB- and FB-SMs having identical voltage.

2.3.2 Pseudo-CBA

A Pseudo-CBA is proposed for the Hybrid-AEM in the normal operation mode to imitate realistic behavior of hybrid MMCs: the Pseudo-CBA defines n_{HB} and n_{FB} at each time-point based on the

total number of SMs to insert, the arm current direction, and the voltages of the HB and FB branches.

If n_{ref} is negative, only FB-SMs are inserted:

$$n_{HB} = 0 \tag{2.51}$$

$$n_{FB} = n_{ref} \tag{2.52}$$

Otherwise, the number of SMs to insert depends on v_{HB}, v_{FB}, n_{ref}, and i_{arm}. With the positive i_{arm} and $v_{HB} > v_{FB}$, as well as with the negative i_{arm} and $v_{HB} < v_{FB}$:

$$n_{HB} = \max\left(0, n_{ref} - N_{FB}\right) \tag{2.53}$$

$$n_{FB} = \min\left(n_{ref}, N_{FB}\right) \tag{2.54}$$

In other cases:

$$n_{HB} = \min\left(n_{ref}, N_{HB}\right) \tag{2.55}$$

$$n_{FB} = \max\left(0, n_{ref} - N_{HB}\right) \tag{2.56}$$

This algorithm is shown in Figure 2.10.

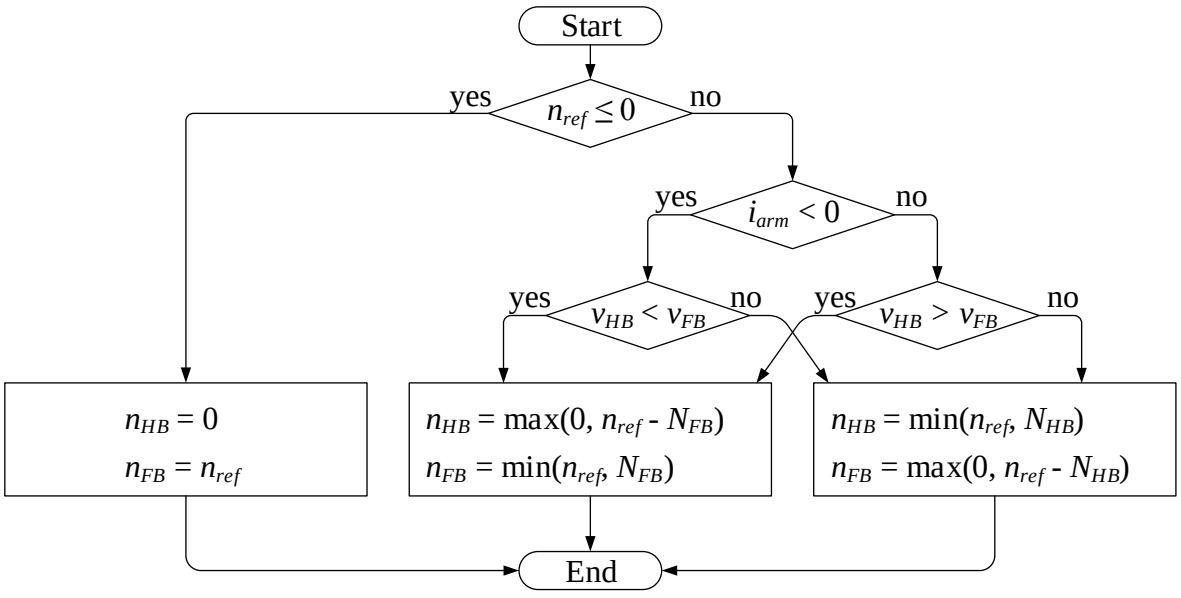


Figure 2.10 Pseudo-CBA algorithm

To make the Pseudo-CBA behavior resemble more the CBA block used with the DEM, a Δt delay is applied to the output signals n_{HB} and n_{FB} to emulate the time required for CBA computations.

2.4 Average value model

The average value model shown in Figure 2.11 typically comprises two parts, AC and DC, disconnected from each other. All SM capacitors of all arms are aggregated into a single DC side capacitor. Neither the voltage ripple nor the circulating current are present but the AC and DC currents and voltages in normal balanced operating conditions are accurate. As with the AEM, the AVM can also be implemented in different ways [113-120, 127, 128]. The conventional AVM is known to be inaccurate in blocked mode [119, 127].

The AVM is built upon the following phase equations in the normal balanced conditions, that allow to separate the AC and DC sides [129]:

$$v_m = \frac{v_{DC}}{2} - v_{up\,m} - R_{arm}\, i_{up\,m} - L_{arm}\, \frac{d}{dt} i_{up\,m} \tag{2.57}$$

$$v_m = -\frac{v_{DC}}{2} + v_{low\,m} + R_{arm}\, i_{low\,m} + L_{arm}\, \frac{d}{dt} i_{low\,m} \tag{2.58}$$

where $m = a,b,c$ is the phase; $i_{low\,m}$, $i_{up\,m}$, $v_{low\,m}$ and $v_{up\,m}$ are the lower and upper arm currents and voltages of the phase m, respectively.

By adding and subtracting (2.57) and (2.58), the AC and DC side equations are obtained:

$$0 = v_{DC} - \left[v_{low\,m} + v_{up\,m} \right] - R_{arm} \left[i_{low\,m} + i_{up\,m} \right] - L_{arm}\, \frac{d}{dt} \left[i_{low\,m} + i_{up\,m} \right] \tag{2.59}$$

$$v_m = \frac{v_{low\,m} - v_{up\,m}}{2} + R_{arm}\, \frac{i_{low\,m} - i_{up\,m}}{2} + L_{arm}\, \frac{d}{dt} \frac{i_{low\,m} - i_{up\,m}}{2} \tag{2.60}$$

The AC side currents and EMFs are defined as

$$i_m = i_{low\,m} - i_{up\,m} \tag{2.61}$$

$$e_m = \left[v_{low\,m} - v_{up\,m} \right] / 2 \tag{2.62}$$

Combining (2.60)–(2.62) results in the following AC side equation per phase:

$$v_m = \frac{R_{arm}}{2} i_m + \frac{L_{arm}}{2} \frac{d}{dt} i_m + e_m \tag{2.63}$$

The common mode voltage and current between the upper and lower arm of each phase are

$$e_{com\,m} = v_{low\,m} + v_{up\,m} \tag{2.64}$$

$$i_{com\,m} = \frac{i_{low\,m} + i_{up\,m}}{2} \tag{2.65}$$

This allows to obtain the following DC side equation per phase:

$$v_{DC} = 2\, R_{arm}\, i_{com\,m} + 2\, L_{arm} \frac{d}{dt} i_{com\,m} + e_{com\,m} \tag{2.66}$$

In normal operating conditions, the common mode current contains only the DC component: $i_{com\,a} = i_{com\,b} = i_{com\,c} = i_{DC}/3$. The common mode voltage is also considered identical in all phases $e_{com\,a} = e_{com\,b} = e_{com\,c} = e_{DC}$, so the following DC side equation can be obtained from (2.66):

$$v_{DC} = \frac{2}{3} R_{arm}\, i_{DC} + \frac{2}{3} L_{arm} \frac{d}{dt} i_{DC} + e_{DC} \tag{2.67}$$

Equations (2.63) and (2.67) govern the AC and the DC sides of the AVM.

To make the model complete, the capacitor dynamics must be accounted for. It is supposed that all arm capacitors have the same voltage defined as $v_{C\,AVM}$, which is assumed constant. In this case, all arm capacitors can be combined into one, C_{AVM}. So, considering (2.37), (2.63) and (2.67), the AC and DC side EMFs e_m and e_{DC} can be written as

$$e_m = v_{C\,AVM}\; s_{AC\,m} \tag{2.68}$$

$$e_{DC} = v_{C\,AVM}\; s_{DC} \tag{2.69}$$

where $s_{AC\,m}$ and s_{DC} are the AC and DC switching functions:

$$s_{AC\,m} = \frac{s_{low\,m} - s_{up\,m}}{2} \tag{2.70}$$

$$s_{DC} = s_{low\,m} + s_{up\,m} \tag{2.71}$$

The AC side switching functions $s_{AC\,m}$ are provided by the control system and are sinusoidally varying in steady-state conditions. The AC circuit contributions to the AVM capacitor current considering (2.38), (2.61), and (2.70) can be written as

$$i_{AVM\,AC} = \sum_{m} s_{AC\,m}\, i_m \tag{2.72}$$

As for the DC side, for the HB-based MMCs it is assumed that $s_{DC} = 1$, which is often realistic since it is common to have $< s_{low\,m} >=< s_{up\,m} >= 0.5$ (variables between "<" and ">" symbols denote period-average values). This results in the DC circuit of the AVM being directly connected to the equivalent capacitor C_{AVM}. In this case, the value of C_{AVM} can be calculated using the energy conservation principle so that the energy stored in the AVM capacitor E_{AVM} is equal to that in other models, for example in the AEM (E_{AEM}):

$$E_{AEM} \approx 6\,\frac{C_{arm}\, v_{DC}^2}{2} \tag{2.73}$$

$$E_{AVM} \approx \frac{C_{AVM}\, v_{DC}^2}{2} \tag{2.74}$$

So

$$C_{AVM} = 6C_{arm} \tag{2.75}$$

To represent the DC voltage reversal capability provided by the FB-SMs, the AVM capacitor cannot be directly connected to the DC circuit and the same approach as for the AC side can be used: the contribution of the DC circuit to the AVM capacitor is defined as

$$i_{AVM\,DC} = -s_{DC}\, i_{DC} \tag{2.76}$$

The maximum and minimum values of the arm switching functions are defined by the proportion of the FB-SMs in the arm:

$$-N_{FB} / N_{SM} \le s_{arm} \le 1 \tag{2.77}$$

Combining (2.70), (2.71), and (2.77) results in the following relationship between $s_{AC\,m}$ and s_{DC}:

$$\max\left(s_{AC}\right) - N_{FB} / N_{SM} \le \frac{s_{DC}}{2} \le 1 - \max\left(s_{AC}\right) \tag{2.78}$$

where $\max\left(s_{AC}\right)$ represents the amplitude of the sinusoidal signal s_{AC}.

If it is assumed that the AVM capacitor voltage is approximately equal to the nominal DC voltage of the converter V_{DC} and the AC voltage is also close to the nominal amplitude value per phase V_{AC}, the amplitude of s_{AC} can be approximated as $\max\left(s_{AC}\right) \approx V_{AC} / V_{DC}$. The limits for s_{DC} are

$$2\left[\frac{V_{AC}}{V_{DC}} - \frac{N_{FB}}{N_{SM}}\right] \le s_{DC} \le 2\left[1 - \frac{V_{AC}}{V_{DC}}\right] \tag{2.79}$$

The final electrical circuit of the Hybrid-AVM is shown in Figure 2.11.

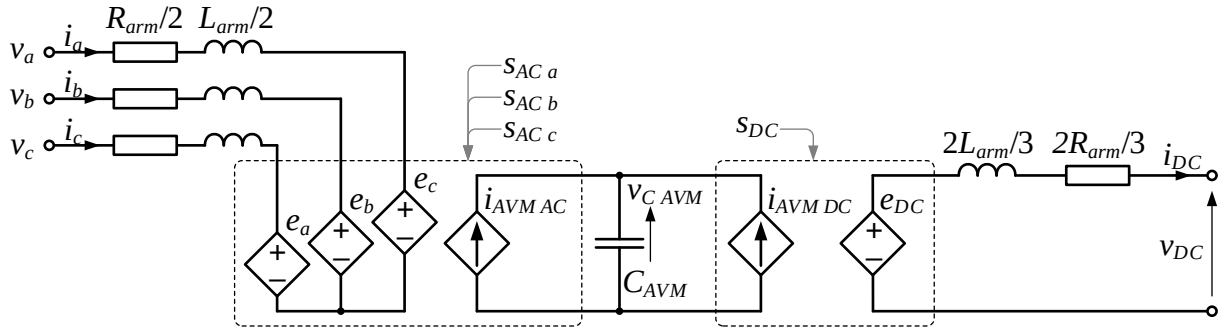


Figure 2.11 Hybrid-AVM for normal operation

In steady-state conditions, the AVM capacitor voltage must be constant, which means that

$$i_{AVM\,AC} = -i_{AVM\,DC} \tag{2.80}$$

The following equation may be then derived from (2.68), (2.69), (2.72), (2.76), and (2.80):

$$\frac{e_a\, i_a + e_c\, i_b + e_c\, i_c}{v_{C\,AVM}} = -\frac{e_{DC}\, i_{DC}}{v_{C\,AVM}} \tag{2.81}$$

This is the formulation of the power balance principle indicating that the power generated at the AC side p_{AC} is transferred to the DC side power p_{DC}:

$$p_{AC} = e_a\, i_a + e_c\, i_b + e_c\, i_c \tag{2.82}$$

$$p_{DC} = e_{DC}\, i_{AVM\,DC} \tag{2.83}$$

2.5 MMC control

In HVDC applications, the control system of grid-following MMC usually employs a cascade structure, as shown in Figure 2.12 [120]. Its main elements include a slower outer control loop, a faster inner control loop, a circulating current control, a phase locked loop (PLL) for grid synchronization, and a lower-level control that calculates the gating signals for the IGBTs in the converter. This section presents the control system suitable for unbalanced grid conditions, and the relevant control blocks are discussed in the next subsections, including sequence extraction, PLL, current control, active/reactive power and voltage regulation, reference distribution and DC side double line frequency ripple suppression. The energy balancing control [130, 131] which allows to keep the average values of arm capacitors equal is not considered in this thesis.

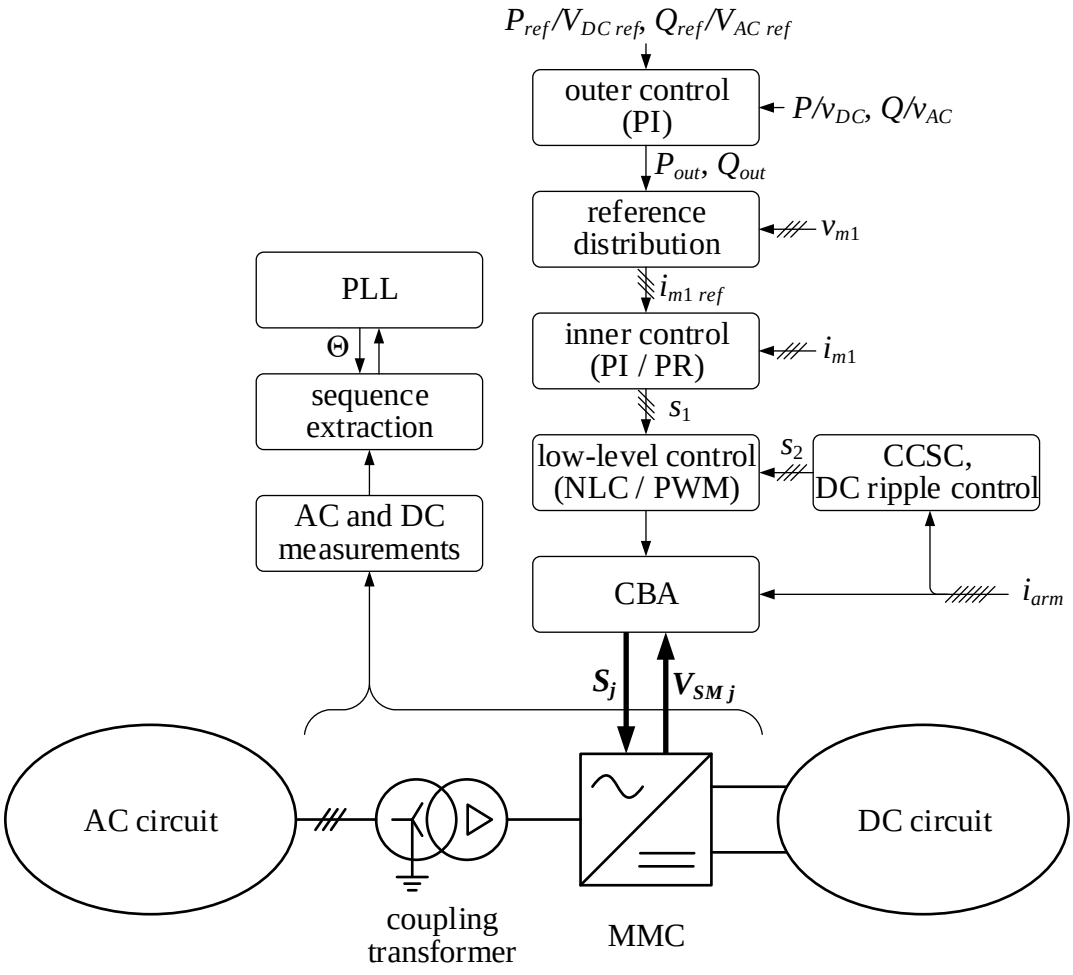


Figure 2.12 Schematic diagram of the control system

2.5.1 Sequence extraction

In MMCs, in addition to the fundamental frequency components, DC and second harmonic terms are often present in various signals, for example in arm switching functions and arm currents. Therefore, before extracting sequence components, the appropriate frequency components must first be separated from each other. This can be done by applying low-pass and notch filters tuned at the necessary frequency, Figure 2.13.

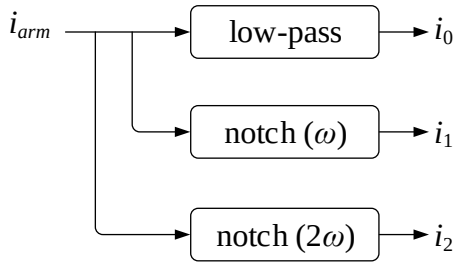


Figure 2.13 Extraction of the frequency components from the arm current

Another possibility for the extraction of harmonic components is as follows. Considering that during normal operation the fundamental frequency components i_1 are only present in the AC side currents and the DC i_0 and double line frequency i_2 components can only be found in the common mode current between the upper and lower arms, the following equations can be derived:

$$i_{m1} = i_{low\,m} - i_{up\,m} \tag{2.84}$$

$$i_{m0} + i_{m2} = \frac{i_{low\,m} + i_{up\,m}}{2} \tag{2.85}$$

In steady state, AC voltages and currents can be decomposed into the positive, negative and zero sequence components. In the following, AC side zero sequence is discarded due to the natural filtering provided by the delta-connected windings on the MMC side of the coupling transformer between the MMC and the AC grid.

Sinusoidal signals can be represented with rotating vectors in the complex plane with the amplitude, angle, and frequency equal to that of the sinusoidal signal. This is convenient when dealing with three-phase electrical networks. Fortescue transformation can be applied to a system of three rotating vectors $\bar{X}_a$, $\bar{X}_b$, and $\bar{X}_c$ to obtain sequence components:

$$\begin{pmatrix} \bar{X}^{+} \\ \bar{X}^{-} \\ \bar{X}^{z} \end{pmatrix} = \frac{1}{3}\begin{pmatrix} 1 & \gamma & \gamma^{2} \\ 1 & \gamma^{2} & \gamma \\ 1 & 1 & 1 \end{pmatrix}\begin{pmatrix} \bar{X}_{a} \\ \bar{X}_{b} \\ \bar{X}_{c} \end{pmatrix} \tag{2.86}$$

where $\gamma = e^{j2\pi/3}$ is the rotation operator; $\bar{X}^{+}$, $\bar{X}^{-}$, and $\bar{X}^{z}$ are the positive, negative, and zero sequence components.

In time domain, the procedure for obtaining sequence components differs because only the instantaneous values of sinusoidal signals are available. In such a case, Clarke's (2.87) and Park's (2.88) transformations can be applied:

$$\begin{pmatrix} x_{\alpha} \\ x_{\beta} \\ x_{z} \end{pmatrix} = \frac{1}{3}\begin{pmatrix} 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \\ 1 & 1 & 1 \end{pmatrix}\begin{pmatrix} x_{a} \\ x_{b} \\ x_{c} \end{pmatrix} \tag{2.87}$$

$$\begin{pmatrix} x_{d} \\ x_{q} \\ x_{z} \end{pmatrix} = \begin{pmatrix} \cos(\omega t + \Theta) & \sin(\omega t + \Theta) & 0 \\ -\sin(\omega t + \Theta) & \cos(\omega t + \Theta) & 0 \\ 0 & 0 & 1 \end{pmatrix}\begin{pmatrix} x_{\alpha} \\ x_{\beta} \\ x_{z} \end{pmatrix} \tag{2.88}$$

where $\omega t + \Theta$ is the angle of Park's transformation; x_{a}, x_{b}, and x_{c} are the sinusoidal signals for which the sequence components must be found.

For a generic three-phase system, the following α-β frame components can be found after applying Clarke's transformation:

$$\begin{pmatrix} x_{\alpha} \\ x_{\beta} \\ x_{z} \end{pmatrix} = \begin{pmatrix} X^{+}\cos(\omega t + \varphi^{+}) + X^{-}\cos(\omega t + \varphi^{-}) \\ X^{+}\sin(\omega t + \varphi^{+}) - X^{-}\sin(\omega t + \varphi^{-}) \\ X^{z}\cos(\omega t + \varphi^{z}) \end{pmatrix} \tag{2.89}$$

where X^{+}, X^{-}, and X^{z} denote the amplitudes of positive, negative and zero sequence components, respectively; φ^{+}, φ^{-}, and φ^{z} are the phase shifts of the corresponding sequence components.

Neglecting the zero sequence, if positive Park transformation ($\omega t + \Theta$) is applied to a system of three-phase signals, a combination of a constant term and a term oscillating at double line frequency (2ω) is obtained:

$$\begin{bmatrix} x_d^+ \\ x_q^+ \end{bmatrix} = X^+ \begin{bmatrix} \cos\left(\varphi^+ - \Theta\right) \\ \sin\left(\varphi^+ - \Theta\right) \end{bmatrix} + X^- \begin{bmatrix} \cos\left(-2\omega t - \varphi^- - \Theta\right) \\ \sin\left(-2\omega t - \varphi^- - \Theta\right) \end{bmatrix} \tag{2.90}$$

where x_d^+ and x_q^+ are the d and q projections in the positive d-q frame.

The constants represent the positive sequence component and the oscillating terms represent the negative sequence. The same is valid for the negative Park's transformation ($-\omega t - \Theta$):

$$\begin{bmatrix} x_d^- \\ x_q^- \end{bmatrix} = X^- \begin{bmatrix} \cos\left(\varphi^- - \Theta\right) \\ -\sin\left(\varphi^- - \Theta\right) \end{bmatrix} + X^+ \begin{bmatrix} \cos\left(2\omega t + \varphi^+ - \Theta\right) \\ \sin\left(2\omega t + \varphi^+ - \Theta\right) \end{bmatrix} \tag{2.91}$$

where x_d^- and x_q^- are the d and q projections in the negative d-q frame.

The above equations are used as a basis for the sequence extraction techniques for the AC side voltages and currents.

2.5.1.1 Decoupling by compensation

In (2.90) and (2.91), it can be observed that the amplitude of the oscillating terms in one equation is equal to the constant term in the other. Taking the positive sequence as an example, it is possible to eliminate the oscillations at -2ω in (2.90) in the following manner: at first, x_d^- and x_q^- in (2.91) are filtered with a low-pass filter (LPF) to obtain the constant part. Next, a double frequency Park's transformation ($2\omega t + 2\Theta$) is applied to the filtered signals to obtain the oscillating component of (2.90). Finally, the oscillating component is subtracted from (2.90) to get purely constant signals, as shown in Figure 2.14 [132]. The blocks $[\boldsymbol{C}]$ and $[\boldsymbol{P}]$ represent the Clarke's and Park's transformations, and the superscripts ±1 and ±2 correspond to the direct and inverse transformations at the line frequency and double line frequency, respectively.

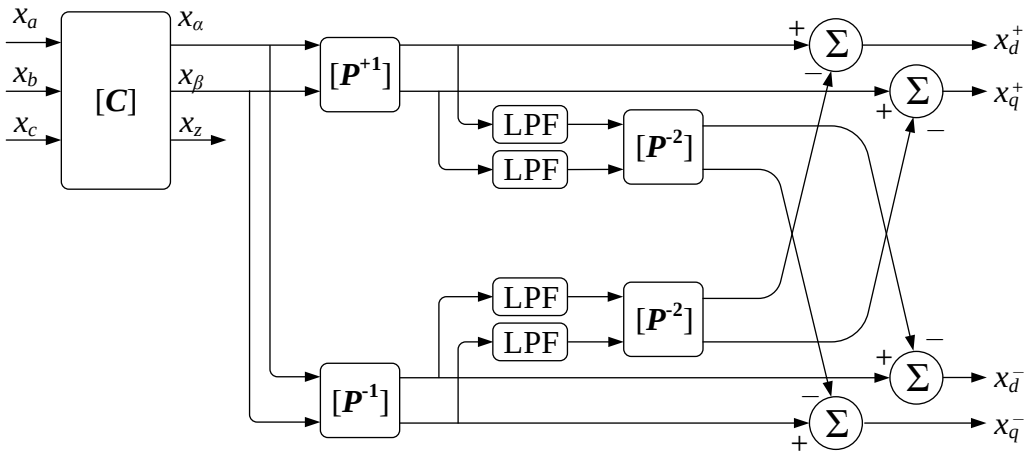


Figure 2.14 Sequence decoupling by compensation

2.5.1.2 Decoupling by delay

It is also possible to decouple the sequences in the stationary α-β frame knowing that in a steady state operation the following equations are true for positive and negative sequences:

$$x_\alpha^+(t) = -x_\beta^+(t - T/4) \tag{2.92}$$

$$x_\beta^+(t) = x_\alpha^+(t - T/4) \tag{2.93}$$

$$x_\alpha^-(t) = x_\beta^-(t - T/4) \tag{2.94}$$

$$x_\beta^-(t) = -x_\alpha^-(t - T/4) \tag{2.95}$$

where x_α^+, x_β^+, x_α^- and x_β^- are positive and negative sequence components in α-β frame, T is the period of the fundamental frequency. This gives the following decoupled terms [133]:

$$x_\alpha^+(t) = \left[x_\alpha(t) - x_\beta(t - T/4)\right]/2 \tag{2.96}$$

$$x_\beta^+(t) = \left[x_\beta(t) + x_\alpha(t - T/4)\right]/2 \tag{2.97}$$

$$x_\alpha^-(t) = \left[x_\alpha(t) + x_\beta(t - T/4)\right]/2 \tag{2.98}$$

$$x_\beta^-(t) = \left[x_\beta(t) - x_\alpha(t - T/4)\right]/2 \tag{2.99}$$

Park's transformations are then applied to the corresponding extracted sequences to obtain constant signals, Figure 2.15.

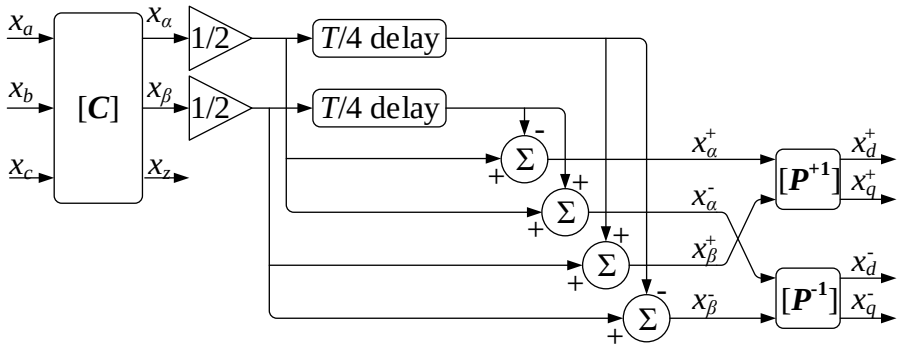


Figure 2.15 Sequence decoupling by delay

2.5.2 Grid synchronization

Synchronization with the AC grid in grid-following converters is performed with a phase-locked loop (PLL) which calculates the phase angle of the positive sequence grid voltage [132]. The PLL considered in this thesis is based on a feedback Proportional-Integral (PI) loop, which adjusts the angle of the Park's transformation to keep the q-axis voltage v_{q1}^+ equal to zero:

$$f_{PLL} = \frac{k_{I\,PLL} + s\,k_{P\,PLL}}{s}\left[0 - v_{q1}^+\right] \tag{2.100}$$

Under unbalanced conditions, double line frequency oscillations in (2.90) propagate into the PLL loop through the feedback variable v_q and consequently into the rest of the control system through the Park's transformation angle. To avoid such negative effects, the feedback variable is averaged over one period, which eliminates the oscillations, Figure 2.16.

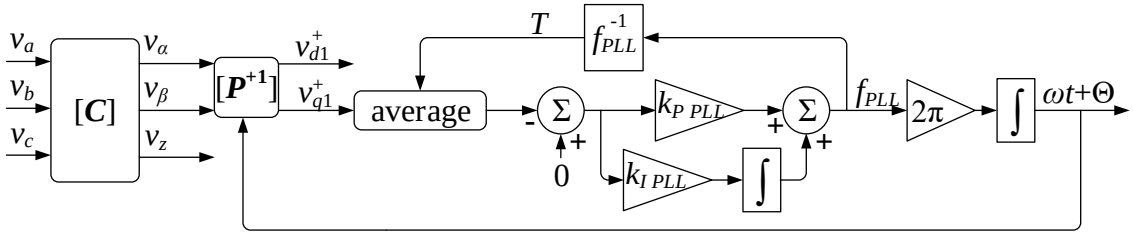


Figure 2.16 PLL diagram

2.5.3 Outer control

The outer loop in VSC-type converters is used to control the active (P) and reactive (Q) powers at the PCC, and AC (v_{AC}) and DC (v_{DC}) voltage magnitudes. Active power and DC voltage are associated with the active current channel whereas reactive power and AC voltage magnitude correspond to the reactive current channel. Active and reactive channels are treated independently. PI controllers are typically used to keep the controlled variables equal to the reference values. The outputs of the outer control loop P_{out} and Q_{out} are used as references for the inner loop which controls the AC side currents [120, 134]. The control diagram of the outer control loop is shown in Figure 2.17. The multiplexer MUX allows to select the desired control objective for each channel, active and reactive.

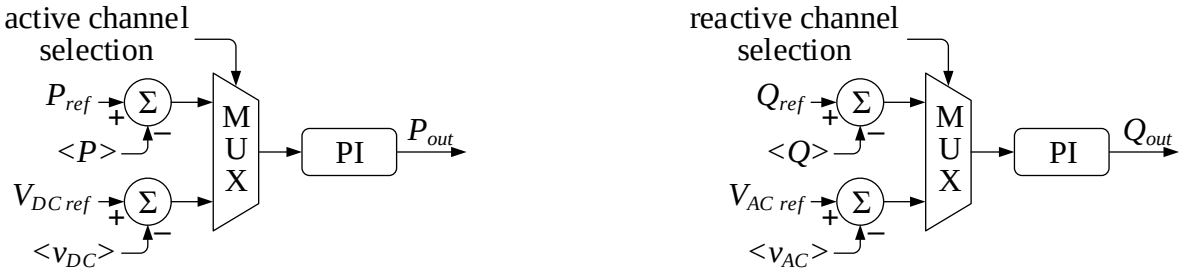


Figure 2.17 Outer control loop

To decouple the inner and outer loop dynamics, the response time of the outer control loop must be several times larger than that of the inner loop. Current regulation can be performed with MMCs in the time-frame of 10 ms, so the outer loop time constant must be in the order of hundreds of milliseconds. For the active (2.101) and reactive (2.102) powers as well as for the AC voltage magnitude (2.104), the inner dynamics of the converter are disregarded, so purely integral regulators can be used, resulting in a first-order closed loop transfer function of the system. As for the DC voltage control, the equivalent capacitor's (2.75) charging process dynamic can be accounted for (2.103). In balanced conditions and when the PLL is perfectly synchronised with the grid voltage (i.e. $v_{q1}^{+}=0$), the control equations are as follows:

$$i_{d1\,ref}^{+}=\frac{k_{I\,P}}{s\,v_{d1}^{+}}\left[P_{ref}-<P>\right] \tag{2.101}$$

$$i_{q1\,ref}^{+} = \frac{k_{I\,Q}}{s\,v_{d1}^{+}}\left[Q_{ref} - < Q >\right] \tag{2.102}$$

$$i_{d1\,ref}^{+} = \frac{k_{I\,VDC} + s\,k_{P\,VDC}}{s\,v_{d1}^{+}}\left[V_{DC\,ref} - < v_{DC} >\right] \tag{2.103}$$

$$i_{q1\,ref}^{+} = \frac{k_{I\,VAC}}{s\,v_{d1}^{+}}\left[V_{AC\,ref} - < v_{AC} >\right] \tag{2.104}$$

where $k_{I\,P}$, $k_{I\,Q}$, $k_{I\,VDC}$ and $k_{I\,VAC}$ are the integral coefficients of the outer loop regulators for the active and reactive powers and DC and AC voltages respectively, and $k_{P\,VDC}$ is the proportional coefficient of the DC voltage regulator. Subscripts 'ref' denote reference values. The period-average values are obtained from the decoupled terms.

During grid unbalance, more advanced techniques are used to link the outputs of the outer loop to the inner loop reference signals, as described in the following subsection.

2.5.4 Current reference distribution

The outer loop generates two signals representing the active and reactive channels, P_{out} and Q_{out}. These signals then need to be converted to a set of reference currents for the internal loop. In balanced grid conditions, only the positive sequence currents are used, so the equations (2.101)–(2.104) are used "as is". During grid unbalance, negative sequence currents can also be utilized to achieve various grid-level objectives [132], so four reference signals must be generated, two for the positive sequence currents and two for the negative sequence. The methods of current reference distribution among the sequences discussed below are based on the following matrix equation linking the active and reactive powers, voltages and currents at the PCC in positive and negative d-q frames [132, 135]:

$$\begin{bmatrix} < P > \\ < Q > \\ P_{\cos} \\ P_{\sin} \\ Q_{\cos} \\ Q_{\sin} \end{bmatrix} = \begin{bmatrix} v_{d1}^{+} & v_{d1}^{+} & v_{d1}^{-} & v_{d1}^{-} \\ v_{q1}^{+} & -v_{d1}^{+} & v_{q1}^{-} & -v_{d1}^{-} \\ v_{d1}^{-} & v_{q1}^{-} & v_{d1}^{+} & v_{q1}^{+} \\ v_{q1}^{-} & -v_{d1}^{-} & -v_{q1}^{+} & v_{d1}^{+} \\ v_{q1}^{-} & -v_{d1}^{-} & v_{q1}^{+} & -v_{d1}^{+} \\ -v_{d1}^{-} & -v_{q1}^{-} & v_{d1}^{+} & v_{q1}^{+} \end{bmatrix} \begin{bmatrix} i_{d1}^{+} \\ i_{q1}^{+} \\ i_{d1}^{-} \\ i_{q1}^{-} \end{bmatrix} \tag{2.105}$$

where $P_{\cos}$, $P_{\sin}$, $Q_{\cos}$, and $Q_{\sin}$ are the amplitudes of the second harmonic oscillatory terms in phase and in quadrature with the positive sequence voltage.

The reference distribution strategies presented below demonstrate interesting grid-level objective functions but are not the only possible and others are available in the literature.

2.5.4.1 Active power ripple suppression

To suppress the active power ripple at the PCC, the corresponding in-phase and in-quadrature terms in (2.105) must be equal to zero:

$$P_{\cos} = P_{\sin} = 0 \tag{2.106}$$

Considering the equations for the average values of P and Q in (2.105), the following matrix equation is obtained [132]:

$$\begin{bmatrix} i_{d1\,ref}^{+} \\ i_{q1\,ref}^{+} \\ i_{d1\,ref}^{-} \\ i_{q1\,ref}^{-} \end{bmatrix} = \begin{bmatrix} v_{d1}^{+} & v_{d1}^{+} & v_{d1}^{-} & v_{d1}^{-} \\ v_{q1}^{+} & -v_{d1}^{+} & v_{q1}^{-} & -v_{d1}^{-} \\ v_{d1}^{-} & v_{q1}^{-} & v_{d1}^{+} & v_{q1}^{+} \\ v_{q1}^{-} & -v_{d1}^{-} & -v_{q1}^{+} & v_{d1}^{+} \end{bmatrix}^{-1} \begin{bmatrix} P_{out} \\ Q_{out} \\ 0 \\ 0 \end{bmatrix} \tag{2.107}$$

2.5.4.2 Balanced positive sequence control

In this approach, only the positive sequence currents are injected by the converter, the negative sequence currents are set to zero. Therefore, all the power must be transmitted through the positive sequence [132]. The multiplication of the positive sequence current by the negative sequence voltage produces the ripple in the active and reactive powers and does not affect their average values. Therefore, only the positive sequence voltage is considered.

The current vector can be treated as a combination of two components: one is in phase with the voltage vector (denoted as $i_{\parallel}$), which generates the active power. The other component is shifted by 90° (in-quadrature component, denoted as $i_{\perp}$) and produces the reactive power:

$$\left|i_{\parallel}\right|\left|v_1^{+}\right| = < P > \tag{2.108}$$

$$\left|i_{\perp}\right|\left|v_1^{+}\right| = < Q > \tag{2.109}$$

where $\left|v_1^+\right| = \sqrt{v_{d1}^+ \, v_{d1}^+ + v_{q1}^+ \, v_{q1}^+}$ is the amplitude of the positive sequence voltage.

During transients, the PLL is not always perfectly synchronised with the grid voltage, so the projections on the d and q axes cannot be considered zero neither for the currents nor for the voltages v_{d1}^+ and v_{q1}^+. Therefore, each current component $i_{\|}$ and $i_{\perp}$ must be treated as a sum of the projections on the d and q axes. The active power component (i.e. aligned with the voltage):

$$i_{\| d1} = \frac{v_{d1}^+ < P >}{\left|v_1^+\right|^2} \tag{2.110}$$

$$i_{\| q1} = \frac{v_{q1}^+ < P >}{\left|v_1^+\right|^2} \tag{2.111}$$

As for the reactive current component, it is aligned with the voltage rotated by 90°, so the d-axis voltage projection is used for the q-axis projection of the current and vice-versa:

$$i_{\perp d1} = \frac{v_{q1}^+ < Q >}{\left|v_1^+\right|^2} \tag{2.112}$$

$$i_{\perp q1} = \frac{-v_{d1}^+ < Q >}{\left|v_1^+\right|^2} \tag{2.113}$$

This is illustrated in Figure 2.18.

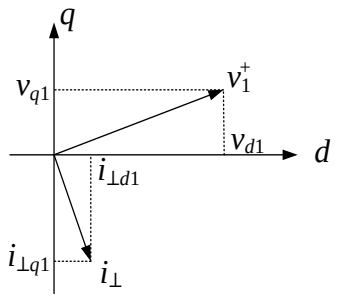


Figure 2.18 Reactive current projections

The d- and q-axis projections are then summed together, which allows to derive the following matrix equation for the current references considering the outputs of the outer loop control described in the subsection 2.5.3:

$$\begin{bmatrix} i_{d1\,ref}^{+} \\ i_{q1\,ref}^{+} \\ i_{d1\,ref}^{-} \\ i_{q1\,ref}^{-} \end{bmatrix} = \frac{1}{\left|v_1^{+}\right|^2} \begin{bmatrix} v_{d1}^{+} & v_{q1}^{+} \\ v_{q1}^{+} & -v_{d1}^{+} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} P_{out} \\ Q_{out} \end{bmatrix} \tag{2.114}$$

2.5.4.3 Flexible positive-negative sequence control

This type of control is defined on the basis that the desired fraction of the active and reactive powers can be transmitted through the positive and negative sequence AC side currents [132]. The coefficients λ_P and λ_Q define the proportions of active and reactive powers transmitted by the positive sequence currents. The negative sequence currents must then transmit $(1-\lambda_P)$ of the active and $(1-\lambda_Q)$ of the reactive power.

Transposing the reasoning presented in the previous subsection 2.5.4.2 for the positive sequence quantities to the negative sequence, (2.114) is amended with two negative sequence current equations, yielding the following system of equations:

$$\begin{bmatrix} i_{d1\,ref}^{+} \\ i_{q1\,ref}^{+} \\ i_{d1\,ref}^{-} \\ i_{q1\,ref}^{-} \end{bmatrix} = \begin{bmatrix} v_{d1}^{+} & v_{q1}^{+} & 0 & 0 \\ v_{q1}^{+} & -v_{d1}^{+} & 0 & 0 \\ 0 & 0 & v_{d1}^{-} & -v_{q1}^{-} \\ 0 & 0 & v_{q1}^{-} & v_{d1}^{-} \end{bmatrix} \begin{bmatrix} \lambda_P\, P_{out} / \left|v_1^{+}\right|^2 \\ \lambda_Q\, Q_{out} / \left|v_1^{+}\right|^2 \\ \left[1-\lambda_P\right] P_{out} / \left|v_1^{-}\right|^2 \\ \left[1-\lambda_Q\right] Q_{out} / \left|v_1^{-}\right|^2 \end{bmatrix} \tag{2.115}$$

where $\left|v_1^{-}\right| = \sqrt{v_{d1}^{-}\, v_{d1}^{-} + v_{q1}^{-}\, v_{q1}^{-}}$ is the amplitude of the negative sequence voltage.

If the grid voltage is balanced, it is not possible to transmit any power through the negative sequence currents, as the negative sequence voltage magnitude $\left|v_1^{-}\right|$ becomes zero in the denominator in the right-hand side of (2.115). The positive sequence voltage is supposed to be always present.

2.5.4.4 Minimal RMS current

It is possible to provide a reference distribution strategy providing the minimal RMS value of the AC side currents for a given average active and reactive powers. The RMS value of the AC side current containing both sequences can be written as

$$I_{RMS} = \sqrt{\left|i_{\parallel}^{+}\right|^2 + \left|i_{\perp}^{+}\right|^2 + \left|i_{\parallel}^{-}\right|^2 + \left|i_{\perp}^{-}\right|^2} \tag{2.116}$$

Minimizing its value is equivalent to minimizing the following equation which is obtained from (2.116) by squaring it and filling in the equations for the positive and negative sequence active and reactive currents:

$$f_{RMS} = I_{RMS}^2 = \left[\frac{\lambda_P < P >}{\left|v_1^{+}\right|}\right]^2 + \left[\frac{\lambda_Q < Q >}{\left|v_1^{+}\right|}\right]^2 + \left[\frac{\left(1-\lambda_P\right) < P >}{\left|v_1^{-}\right|}\right]^2 + \left[\frac{\left(1-\lambda_Q\right) < Q >}{\left|v_1^{-}\right|}\right]^2 \tag{2.117}$$

Partial derivatives of f_{RMS} are

$$\frac{\partial}{\partial \lambda_P} f_{RMS} = 2 < P^2 > \lambda_P \left[\frac{1}{\left|v_1^{+}\right|^2} + \frac{1}{\left|v_1^{-}\right|^2}\right] - 2 < P^2 > \frac{1}{\left|v_1^{-}\right|^2} \tag{2.118}$$

$$\frac{\partial}{\partial \lambda_Q} f_{RMS} = 2 < Q^2 > \lambda_Q \left[\frac{1}{\left|v_1^{+}\right|^2} + \frac{1}{\left|v_1^{-}\right|^2}\right] - 2 < Q^2 > \frac{1}{\left|v_1^{-}\right|^2} \tag{2.119}$$

The extremum points are then found by letting $\frac{\partial}{\partial \lambda_P} f_{RMS}$ and $\frac{\partial}{\partial \lambda_Q} f_{RMS}$ be equal to zero:

$$\lambda_P = \frac{\left|v_1^{+}\right|^2}{\left|v_1^{+}\right|^2 + \left|v_1^{-}\right|^2} \tag{2.120}$$

$$\lambda_Q = \frac{\left|v_1^{+}\right|^2}{\left|v_1^{+}\right|^2 + \left|v_1^{-}\right|^2} \tag{2.121}$$

The extremum points thus found must be the minimums being the only extremums and owing to the physical nature of the equations. By plugging (2.120) and (2.121) into (2.115), the following equation is obtained:

$$\begin{bmatrix} i_{d1\,ref}^{+} \\ i_{q1\,ref}^{+} \\ i_{d1\,ref}^{-} \\ i_{q1\,ref}^{-} \end{bmatrix} = \frac{1}{\left|v_1^{+}\right|^2 + \left|v_1^{-}\right|^2} \begin{bmatrix} v_{d1}^{+} & v_{q1}^{+} \\ v_{q1}^{+} & -v_{d1}^{+} \\ v_{d1}^{-} & -v_{q1}^{-} \\ v_{q1}^{-} & v_{d1}^{-} \end{bmatrix} \begin{bmatrix} P_{out} \\ Q_{out} \end{bmatrix} \tag{2.122}$$

2.5.5 Inner control

The inner control loop is used for the AC side current regulation. It is often based on PI controllers in the d-q frame, but other types are also possible, such as the proportional-resonant control in the stationary α-β frame. The controller regulates the current flowing through an equivalent inductance L_{Σ} between the converter's inner EMF e_{m1} and the PCC:

$$L_{\Sigma} = L_{trfo} + L_{arm}/2 \tag{2.123}$$

where L_{trfo} is the coupling transformer's inductance and $L_{arm}/2$ is the equivalent AC side converter inductance (see Figure 2.11).

The corresponding differential equation for the current control is written as

$$L_{\Sigma} \frac{di_{m1}}{dt} = \Delta v = v_{m1} - e_{m1} \tag{2.124}$$

where i_{m1} is the AC side current that is being regulated; v_{m1} is the PCC voltage (see Figure 2.19).

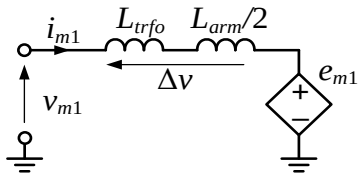


Figure 2.19 Converter station circuit for current control

In case of two- and three-level VSCs as well as the AVM of MMC, the outputs of the current controller are the modulation signals representing the AC voltage references $e_{ref} = e_{m1}$ (see section 2.4), as in (2.126), (2.127), and (2.128). In more detailed MMC models, the outputs of the inner control are slightly different, owing to the dynamics of the SM voltages. In this case, the output signals are used as the first harmonic terms of the arm switching function s_1 and arm voltages are

obtained as the multiplication of the arm switching functions by the total capacitor voltages (supposing that individual SM voltages $\boldsymbol{V_{SM\,j}}$ are identical).

The AC side EMF is obtained as the differential mode voltage in the upper and lower arms:

$$e_{m1} = \frac{v_{low\,m1} - v_{up\,m1}}{2} \tag{2.125}$$

where $v_{low\,m}$ and $v_{up\,m}$ are the lower and upper arm voltages, respectively.

2.5.5.1 Control in d-q frame

To control the positive and negative sequence currents, PI regulators in the positive (2.126) and negative (2.127) d-q frames with PCC voltage feedforward can be used. The system for the positive d-q frame control is shown in Figure 2.20, the negative d-q frame current control circuit uses the same structure.

$$\begin{bmatrix} s_{d1}^{+} \\ s_{q1}^{+} \end{bmatrix} = \begin{bmatrix} v_{d1}^{+} \\ v_{q1}^{+} \end{bmatrix} - \begin{bmatrix} \frac{k_I + s\,k_P}{s}\left[i_{d1\,ref}^{+} - i_{d1}^{+} \right] \\ \frac{k_I + s\,k_P}{s}\left[i_{q1\,ref}^{+} - i_{q1}^{+} \right] \end{bmatrix} - \omega L_{\Sigma} \begin{bmatrix} -i_{q1}^{+} \\ i_{d1}^{+} \end{bmatrix} \tag{2.126}$$

$$\begin{bmatrix} s_{d1}^{-} \\ s_{q1}^{-} \end{bmatrix} = \begin{bmatrix} v_{d1}^{-} \\ v_{q1}^{-} \end{bmatrix} - \begin{bmatrix} \frac{k_I + s\,k_P}{s}\left[i_{d1\,ref}^{-} - i_{d1}^{-} \right] \\ \frac{k_I + s\,k_P}{s}\left[i_{d1\,ref}^{-} - i_{d1}^{-} \right] \end{bmatrix} - \omega L_{\Sigma} \begin{bmatrix} i_{q1}^{-} \\ -i_{d1}^{-} \end{bmatrix} \tag{2.127}$$

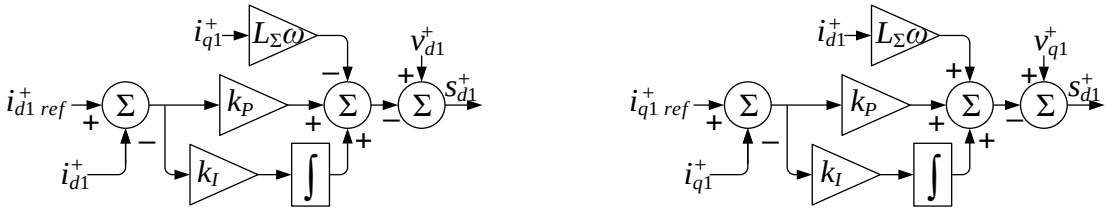


Figure 2.20 Positive sequence current control in d-q frame

2.5.5.2 Control in α-β frame

The AC side currents can also be regulated using Proportional-Resonant (PR) controllers in the stationary α-β frame (2.128) [136]. PR controllers can handle positive and negative sequence currents in the same time. The corresponding implementation is shown in Figure 2.21. According

to [132], PR controllers can have similar transient behavior as the PI controllers discussed in the subsection 2.5.5.1 if the proportional $k_{P\,PR}$ and resonant $k_{I\,PR}$ gains of the controller are two times larger than the values of k_P and k_I in (2.126), respectively.

$$\begin{bmatrix} s_{\alpha 1} \\ s_{\beta 1} \end{bmatrix} = \begin{bmatrix} v_{\alpha 1} \\ v_{\beta 1} \end{bmatrix} - \begin{bmatrix} \dfrac{s\,k_{R\,PR1}}{s^2+\omega^2} + k_{P\,PR1} & 0 \\ 0 & \dfrac{s\,k_{R\,PR1}}{s^2+\omega^2} + k_{P\,PR1} \end{bmatrix} \begin{bmatrix} i_{\alpha 1\,ref} - i_{\alpha 1} \\ i_{\beta 1\,ref} - i_{\beta 1} \end{bmatrix} \tag{2.128}$$

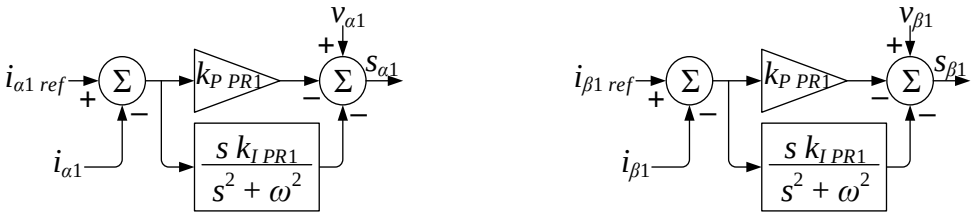


Figure 2.21 Proportional-resonant current controller

2.5.6 Circulating current suppression control

During normal operation of the MMC in balanced conditions, double line frequency negative sequence circulating currents appear inside the MMC if no special control is suppressing them [137]. These additional currents cause supplementary stress on the electrical equipment and may even lead to unstable operation of the converter [138]. During grid unbalance, in addition to the negative sequence currents, positive and zero sequence currents appear [139, 140]. Such currents are caused by the differences between the upper and lower arms' voltages, which result from the inner dynamics of the SM capacitors constantly undergoing charging and discharging process. The positive and negative sequence currents circulate inside the MMC and are not directly observable outside the converter. The zero sequence propagates to the DC side of the converter and can affect the operation of the other equipment connected to the DC side of the MMC.

For the positive and negative sequence currents, the circulating current suppression control (CCSC) based on the current regulators similar to those discussed in the subsection 2.5.5 can be used, as shown in Figure 2.22 and Figure 2.23. Circulating current reference values are set to zero. Since the circulating currents are locked inside the converter, there is no grid voltage feedforward. The angle of the Park's transformation for the d-q frame control (2.129)–(2.130) and the resonant frequency for the α-β frame control (2.131) is twice the value used for the AC side controls.

$$\begin{bmatrix} s_{d2}^{+} \\ s_{q2}^{+} \end{bmatrix} = \begin{bmatrix} \dfrac{k_{I2} + s\,k_{P2}}{s}\left[0 - i_{d2}^{+}\right] \\ \dfrac{k_{I2} + s\,k_{P2}}{s}\left[0 - i_{q2}^{+}\right] \end{bmatrix} + 2\omega L_{arm} \begin{bmatrix} -i_{q2}^{+} \\ i_{d2}^{+} \end{bmatrix} \tag{2.129}$$

$$\begin{bmatrix} s_{d2}^{-} \\ s_{q2}^{-} \end{bmatrix} = \begin{bmatrix} \dfrac{k_{I2} + s\,k_{P2}}{s}\left[0 - i_{d2}^{-}\right] \\ \dfrac{k_{I2} + s\,k_{P2}}{s}\left[0 - i_{d2}^{-}\right] \end{bmatrix} + 2\omega L_{arm} \begin{bmatrix} i_{q2}^{-} \\ -i_{d2}^{-} \end{bmatrix} \tag{2.130}$$

$$\begin{bmatrix} s_{\alpha 2} \\ s_{\beta 2} \end{bmatrix} = \begin{bmatrix} \dfrac{s\,k_{R\,PR2}}{s^2 + 4\omega^2} + k_{P\,PR2} & 0 \\ 0 & \dfrac{s\,k_{R\,PR2}}{s^2 + 4\omega^2} + k_{P\,PR2} \end{bmatrix} \begin{bmatrix} 0 - i_{\alpha 2} \\ 0 - i_{\beta 2} \end{bmatrix} \tag{2.131}$$

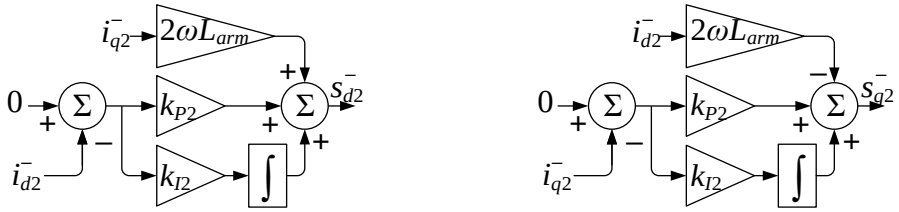


Figure 2.22 Negative sequence d-q CCSC

Figure 2.23 Proportional-resonant CCSC

2.5.7 DC side ripple suppression control

To suppress the zero-sequence double line frequency oscillations, a dedicated controller is needed. In [141], it is proposed to extract the zero-sequence voltage and obtain the DC ripple suppression signal with the help of a band-pass filter:

$$s_{z2} = \frac{k_0\, 2\omega\, s \sum_{m=a,b,c}\left[v_{low\,m} + v_{up\,m}\right]}{s^2 + 2\xi\, 2\omega\, s + 4\omega^2} \tag{2.132}$$

where k_0 is the gain and ξ is the damping coefficient.

The corresponding implementation is shown in Figure 2.24.

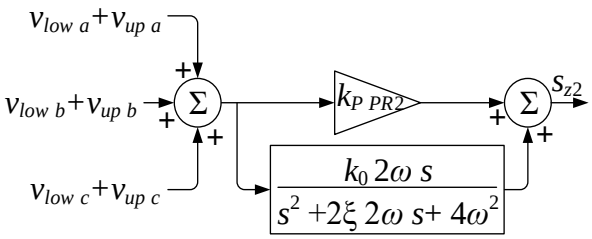


Figure 2.24 DC voltage ripple suppression controller

Another option is to define the suppressing signal directly in the abc frame using PR controllers [139]. In this case, the double line frequency components in the difference current are obtained using a high-pass filter as shown in Figure 2.25.

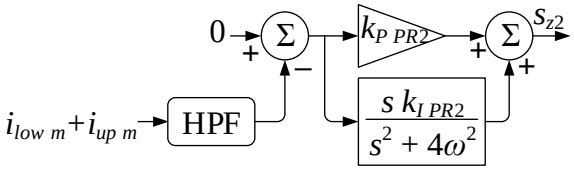


Figure 2.25 DC-loop current controller

It is also possible to use a cascade structure based on PR controllers for the DC voltage and current ripple suppression [134], consisting of the inner controller for the DC current ripple i_{DC2} (2.133) and the outer controller for DC voltage ripple v_{DC2} suppression (2.134), as shown in Figure 2.26.

$$PR_v(s)=\frac{k_{Rv}\, s}{s^2+4\omega^2}+k_{Pv} \tag{2.133}$$

$$PR_i(s)=\frac{k_{Ri}\, s}{s^2+4\omega^2}+k_{Pi} \tag{2.134}$$

where k_{Rv}, k_{Ri}, k_{Pv} and k_{Pi} are the gains of the resonant and proportional parts of the voltage and current controllers, respectively.

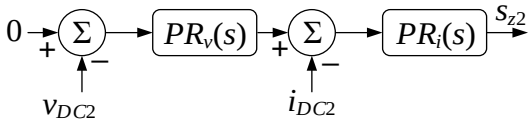


Figure 2.26 DC side ripple suppression controller

2.5.8 Low-level control

In the previous subsections 2.5.5, 2.5.6, and 2.5.7, the values of the fundamental and double line frequency components of arm switching functions have been established. To find individual arm switching function values, the sequence components must be transformed back into the phase domain. For the double line frequency values obtained in d-q frames:

$$\begin{bmatrix} s_{a2} \\ s_{b2} \\ s_{c2} \end{bmatrix} = \left[\mathbf{C}^{-1}\right]\left[\mathbf{P}^{-2}\right]\begin{bmatrix} s_{d2}^{+} \\ s_{q2}^{+} \\ 0 \end{bmatrix} + \left[\mathbf{C}^{-1}\right]\left[\mathbf{P}^{+2}\right]\begin{bmatrix} s_{d2}^{-} \\ s_{q2}^{-} \\ 0 \end{bmatrix} + s_{z2}\begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \tag{2.135}$$

where $\left[\mathbf{C}^{-1}\right]$ represents the inverse Clarke's transformation:

$$\left[\mathbf{C}^{-1}\right] = \frac{1}{2}\begin{bmatrix} 2 & 0 & 2 \\ -1 & \sqrt{3} & 2 \\ -1 & -\sqrt{3} & 2 \end{bmatrix} \tag{2.136}$$

For the α-β frame values:

$$\begin{bmatrix} s_{a2} \\ s_{b2} \\ s_{c2} \end{bmatrix} = \left[\mathbf{C}^{-1}\right]\begin{bmatrix} s_{\alpha 2} \\ s_{\beta 2} \\ s_{z2} \end{bmatrix} \tag{2.137}$$

The fundamental terms in d-q frames:

$$\begin{bmatrix} s_{a1} \\ s_{b1} \\ s_{c1} \end{bmatrix} = \left[\mathbf{C}^{-1}\right]\left[\mathbf{P}^{-1}\right]\begin{bmatrix} s_{d1}^{+} \\ s_{q1}^{+} \\ 0 \end{bmatrix} + \left[\mathbf{C}^{-1}\right]\left[\mathbf{P}^{+1}\right]\begin{bmatrix} s_{d1}^{-} \\ s_{q1}^{-} \\ 0 \end{bmatrix} \tag{2.138}$$

Or in α-β frame

$$\begin{bmatrix} s_{a1} \\ s_{b1} \\ s_{c1} \end{bmatrix} = \left[\mathbf{C}^{-1}\right]\begin{bmatrix} s_{\alpha 1} \\ s_{\beta 1} \\ 0 \end{bmatrix} \tag{2.139}$$

The constant component is identical for all arms and is taken by default as

$$s_0 = 0.5 \tag{2.140}$$

In hybrid or FB-SM-based MMCs, where it is possible to change the DC voltage polarity, s_0 can become negative so that FB-SMs would be inserted negatively.

To obtain the final values of arm switching functions, all harmonic components must be added together. The fundamental terms in the upper and lower arms have the opposite sign whereas the constant and double line frequency components are identical:

$$s_{low\,m} = s_0 + s_{m1} + s_{m2} \tag{2.141}$$

$$s_{up\,m} = s_0 - s_{m1} + s_{m2} \tag{2.142}$$

2.5.8.1 Number of SMs to insert

As defined in (2.34) in the section 2.3, arm switching functions represent the proportion of inserted SMs in each arm. Therefore, once the values of s_{arm} for all arms are identified with (2.141) and (2.142), the number of SMs to be inserted in each arm n_{ref} can be calculated. Two possible options are usually considered: pulse width modulation (PWM) for MMCs with a relatively low number of SMs (below 20-50) and nearest level control (NLC) for MMCs with higher SM count.

Different techniques are available for PWM control in MMCs: phase-shifted PWM, phase-disposition PWM, and others [142, 143]. With them, the number of SMs to insert is defined by comparing the modulating signal (s_{arm}) with multiple triangular carriers, one for each SM: if the modulating signal is above the carrier, the submodule is inserted, $S_j = 1$. Otherwise, the SM is bypassed, $S_j = 0$. If each SM insertion is controlled by a particular carrier, SM voltages drift away from each other and can have significant distortion [137, 143] even if carrier rotation is applied. Therefore, only the total number of inserted SMs is usually considered at this step to avoid unstable operation of the converter [144]:

$$n_{ref} = \sum_{j=1}^{N_{SM}} S_j \tag{2.143}$$

With the NLC, the number of SMs to insert is obtained by finding the closest integer number providing the necessary proportion of the inserted SMs [145]:

$$n_{ref} = round\left(s_{arm}\ N_{SM}\right) \tag{2.144}$$

2.5.8.2 Capacitor voltage balancing

Once the number of SMs to insert has been found either with the PWM-based control or with the NLC, it is then necessary to select the most appropriate SMs to insert. The selection is usually aiming to keep SM voltages balanced among themselves. This is done by applying a capacitor balancing algorithm (CBA), which selects the most appropriate SM depending on the arm current direction and the number of SMs to insert [129, 145]. While many CBA implementations are possible, they generally apply the following logic: when the arm current is positive (i.e. charging the SM capacitors), SMs with the lowest voltage are preferably inserted, which brings their voltage up. With the negative arm current, highest voltage SMs are selected so that their voltage is reduced by the discharging arm current. In this manner, SM voltages do not deviate much from each other.

As previously mentioned, various options exist for the CBA: if SM voltages are sorted, the computational burden is high if N_{SM} is large. Also, this requires a considerable amount of IGBT switching operations, which increases the switching losses [129]. To reduce the amount of losses, several solutions have been proposed in the literature [146, 147], including the introduction of a voltage threshold and sorting when the voltages are outside of it. Another option is to perform voltage sorting only on the SMs that are to be added or removed when n_{ref} changes [137].

In this thesis, two CBAs are used: voltage sorting-based and permutation-based. The voltage sorting CBA inserts n_{ref} SMs with the lowest voltages when the arm current is positive (i.e. charging). If the arm current is negative (i.e. discharging), n_{ref} SMs with the highest voltages are inserted. The sorting is triggered by an external clocking signal.

The permutation-based CBA bypasses the SM having the highest voltage among inserted and inserts the SM having the lowest voltage among bypassed when the arm current is positive (as long as the voltage of the SM that is being inserted is lower than that of the bypassed one). When the arm current is negative, it is the SM having the lowest voltage among inserted that is bypassed and the SM having the highest voltage among bypassed that is inserted (in this case, it is necessary that the voltage of the SM to be inserted be higher than that of the bypassed one). Such swapping occurs at each time-point.

2.5.9 Start-up

The start-up procedure is used to bring the converter to the operational state when the SM capacitors are discharged. It is usually performed in two steps: uncontrolled and controlled charging. Rectifying station can be charged through the AC side and inverting station can be charged through the DC side [148, 149]. The uncontrolled charging is performed first, at this stage all SMs are blocked.

In the MMCs charged through the AC side, SM capacitors are charged with the passing arm currents [150]. Once the SM voltages stabilize at a steady-state value, the controlled charging process starts with the activation of DC voltage control, which brings the SM voltages to the nominal value.

If the MMC is charged through the DC side, the uncontrolled charging results in all SMs having half the nominal voltage. Afterwards, all SMs are unblocked and the number of bypassed SMs rises gradually from 0 to $N_{SM}/2$. The CBA is actively balancing all SM voltages to keep them identical to each other. Once the SMs reach the nominal voltage value, the MMC is synchronised and connected to the AC grid.

2.5.10 DC voltage reversal

The classical control system presented in the previous subsections assumes $s_0 = 0.5$, which restricts the DC voltage polarity reversal. However, such functionality can prove useful when, for example, an MMC is connected to an LCC and needs to change the power flow direction, which is possible with hybrid or FB-SM based MMCs. To be able to invert the DC voltage, another control circuit is used [74, 125].

The value of s_0 is regarded as the contribution of the total capacitor voltage to the DC voltage. To reverse v_{DC}, s_0 must become negative, therefore an additional control block dedicated to s_0 control is used. It is based on a PI control of the DC current, which is used as a replacement of the active power channel control in the classical cascade structure. The active power channel, in its turn, is used to control the average value of the capacitor voltages in all arms of the converter v_{Csum}:

$$v_{Csum} = \frac{1}{6}\sum_m \left(v_{Ctot\,up\,m} + v_{Ctot\,low\,m} \right) \tag{2.145}$$

The outer control loop is therefore modified from Figure 2.17 and contains three regulators as follows:

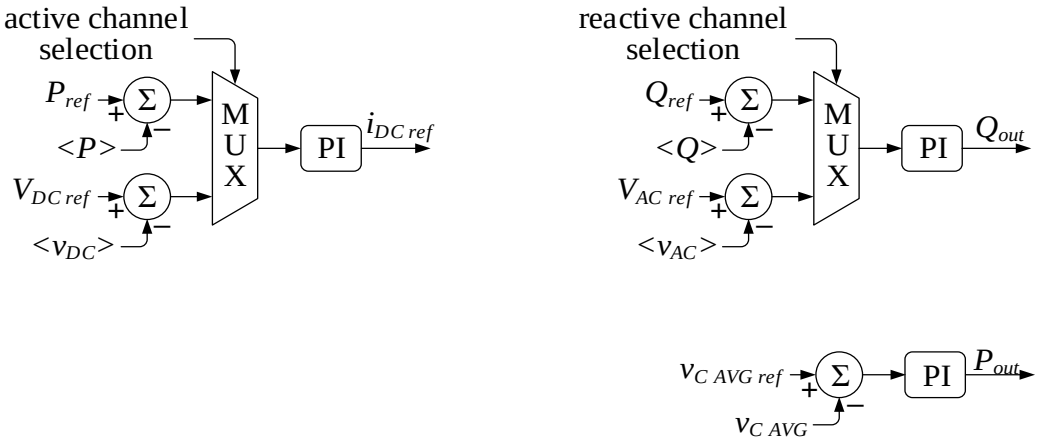


Figure 2.27 Outer control loop for DC voltage reversal

For the active and reactive channel current control (P_{out} and Q_{out}), the regulators discussed in the subsection 2.5.5 can be used, and a dedicated PI controller is added for the DC current:

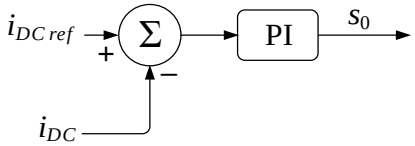


Figure 2.28 DC current controller

2.5.11 Additional functionality

Additional control functions, such as frequency support [151-153], inertial response emulation [154], DC voltage support [155], grid-forming and others can be provided by MMCs. However, such controls are out of the scope of this thesis and are only mentioned here for a more complete picture.

2.6 Simulation cases

The performance of the presented MMC models is demonstrated on a point-to-point MMC-HVDC link shown in Figure 2.29. The two MMCs used in this transmission have identical electrical parameters, the number of SMs in each arm is 100 with 80 FB-SMs and 20 HB-SMs. MMC1 controls the active and reactive powers at the AC terminals and MMC2 controls the DC voltage

and reactive power. The power flow is from MMC1 to MMC2. The DC cable parameters as well as other parameters of the simulated system are listed in Appendix B.

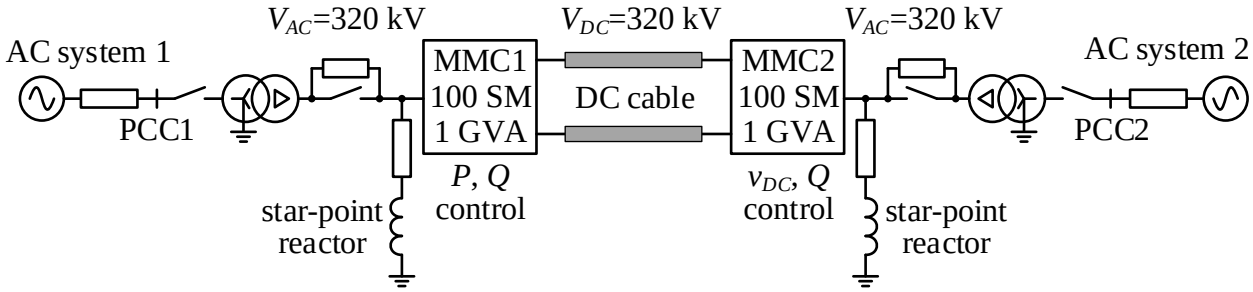


Figure 2.29 Simulated MMC-HVDC link

In the following tests, the time-step of 1 μs is used to represent the smooth commutation of IGBTs. Having the same time-step for all models allows to compare them in identical conditions to make the comparison fair.

2.6.1 Start-up

The DM, DEM, and AEM are compared during the start-up process with the procedure presented in the subsection 2.5.9. The AVM is excluded from the comparisons due to its inability to correctly represent the blocked mode and the charging of capacitors. To more explicitly demonstrate the differences between the models, the CBA block, which is active during the controlled charging part of the start-up procedure, performs the voltage sorting only on the SMs that are to be added or removed when n_{ref} changes [137]. This introduces significant unbalance between SM voltages.

The uncontrolled charging starts with the charging resistors at the MMC2 side inserted to limit the currents during the process. At 1 s, the resistors are bypassed. During the whole uncontrolled charging period (from 0 to 1.2 s), both the AEM and the DEM match the DM reference with a relatively high accuracy, as it can be seen in the total capacitor voltage (Figure 2.30), arm current (Figure 2.31), and DC current (Figure 2.32), because the SM voltages are identical.

When the CBA is activated, the AEM is unable to represent the differences among the SM voltages, which results in the oscillations between 2.2 s and 2.5 s being missing with the AEM. The arm current and total capacitor voltage are also smoother with the AEM at steady-state after 2.8 s. However, the AEM is still able to reproduce the overall behavior of the system. The mismatch between the DEM and DM waveforms during normal operation can be attributed to the differences

in the number of SMs to insert. The average number of iterations per time-step (the averaging window duration is 10 ms) shown in Figure 2.33 is close to one with the DEM and AEM, whereas with the DM it is considerably higher.

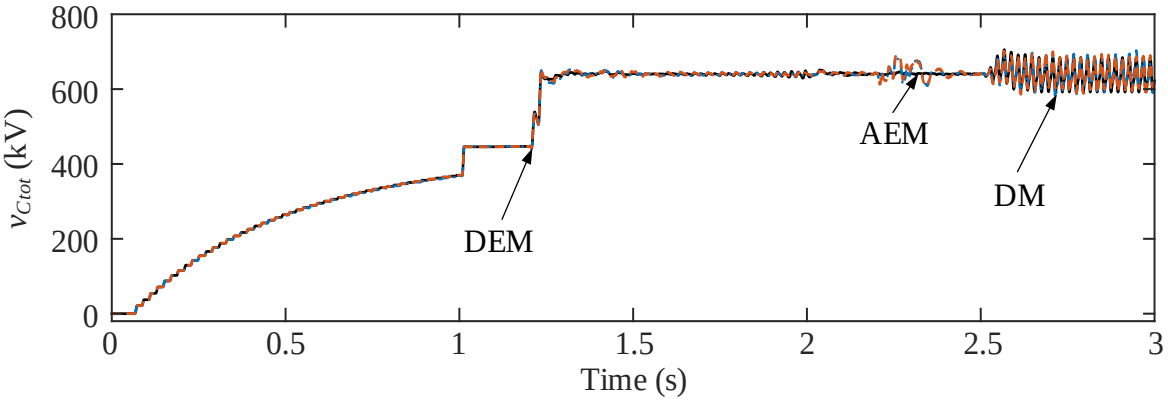


Figure 2.30 Total capacitor voltage in phase A upper arm of MMC2

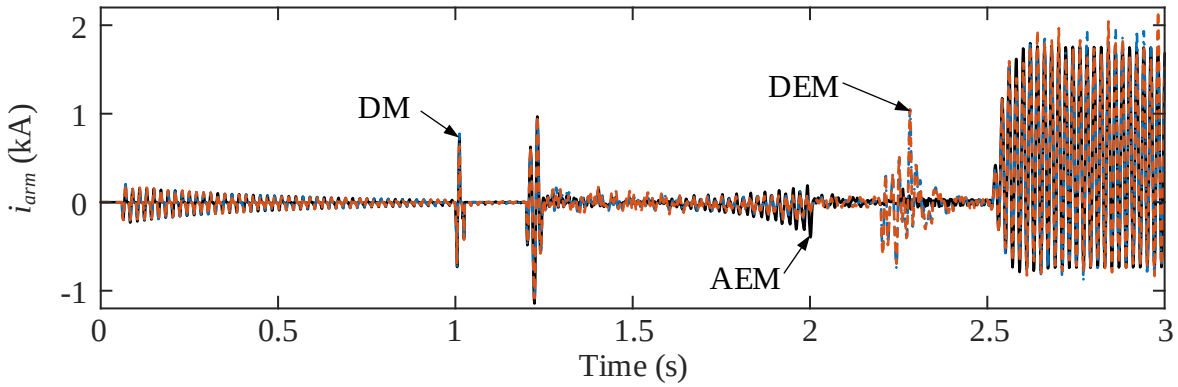


Figure 2.31 Arm current in phase A upper arm of MMC2

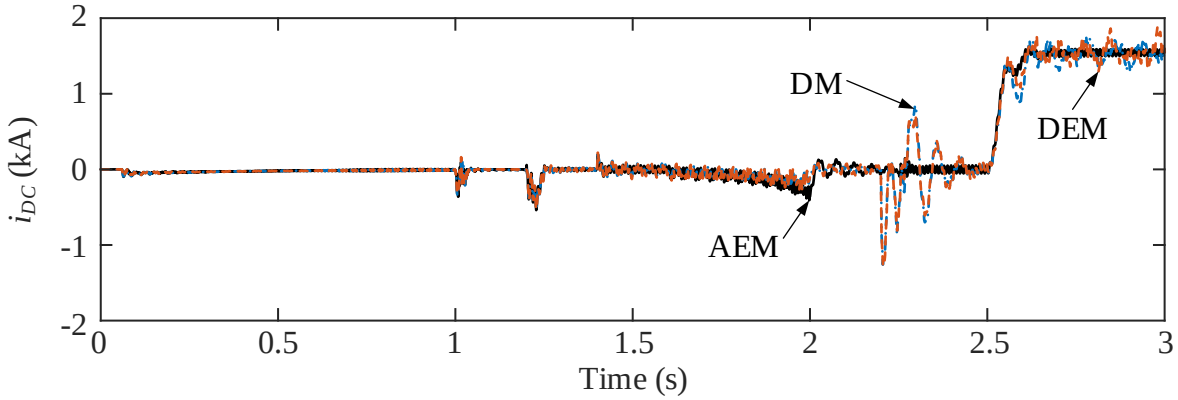


Figure 2.32 DC current

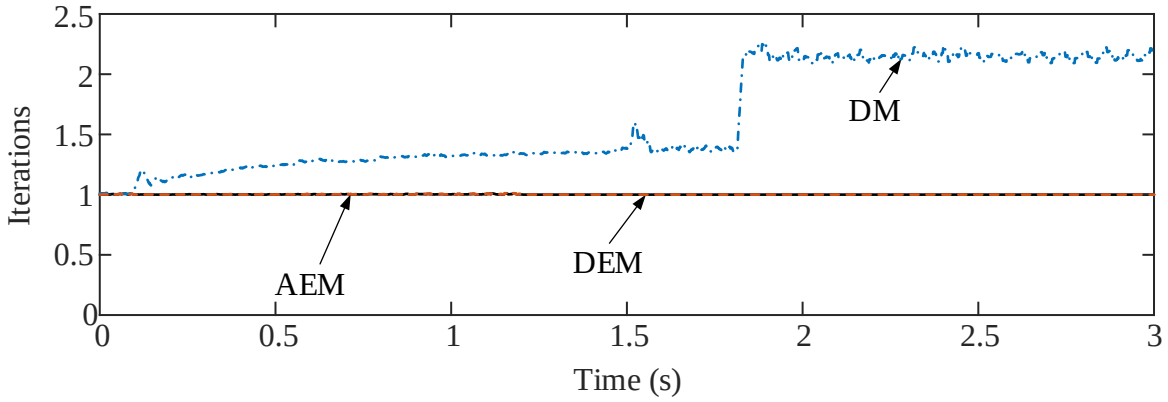


Figure 2.33 Average number of iterations

2.6.1.1 Blocked mode algorithm validation

The proposed blocked mode algorithm is compared with the existing EMTP implementation on the following test-case. The start-up procedure of the same MMC-HVDC link but with 100 HB-SMs is simulated (the uncontrolled charging period only).

With the existing EMTP DEM implementation, the arm voltages exhibit spikes, as shown in Figure 2.34 and Figure 2.35. The DM reference does not have such spikes, which means that they are not realistic. They appear when the SMs in the DEM change their conduction state (charging, bypassed, high-impedance). Since in the DEM only two values are used for the IGBT resistances, the changes are abrupt. In the DM, the v-i characteristics of IGBTs is smooth, and so are the transitions between the states. With the proposed blocked mode algorithm for the DEM, the spikes are eliminated, and therefore a better match is obtained with the DM reference. The average number of iterations with the proposed DEM is considerably lower than with the EMTP DEM and the DM, Figure 2.36.

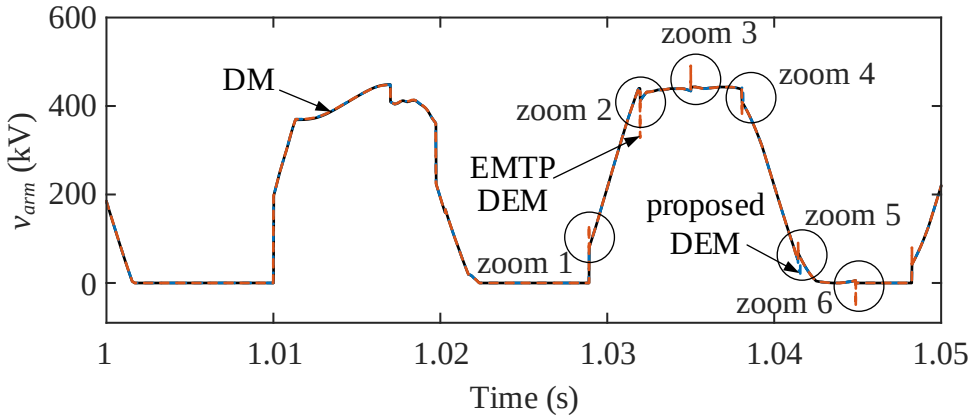
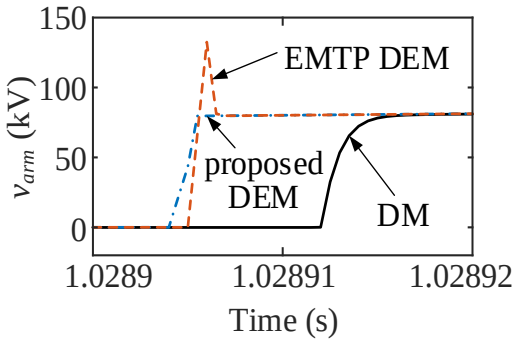
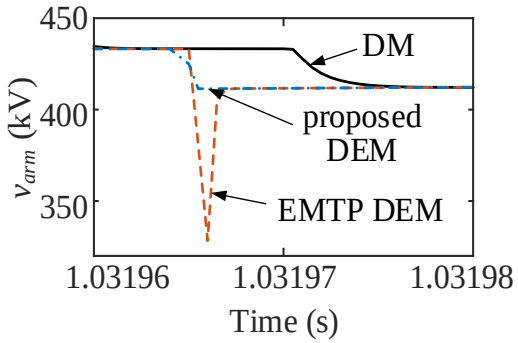


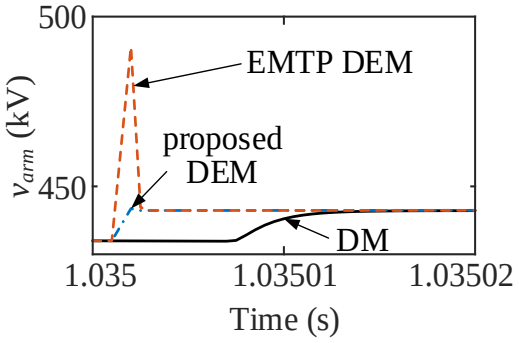
Figure 2.34 Arm voltage in phase C lower arm of MMC2



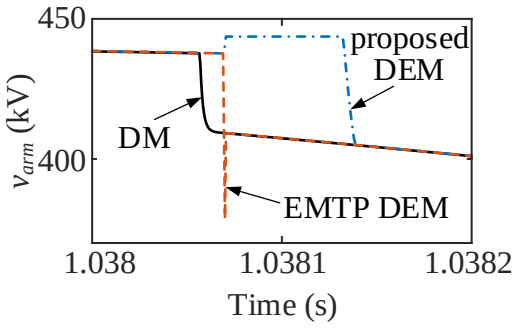
a) zoom 1



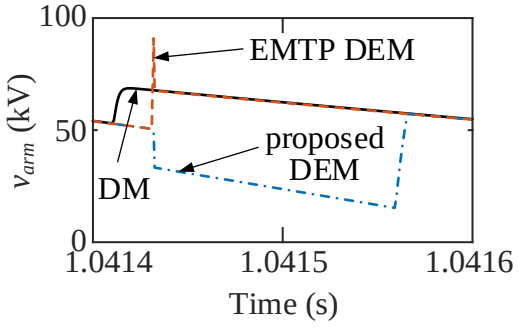
b) zoom 2



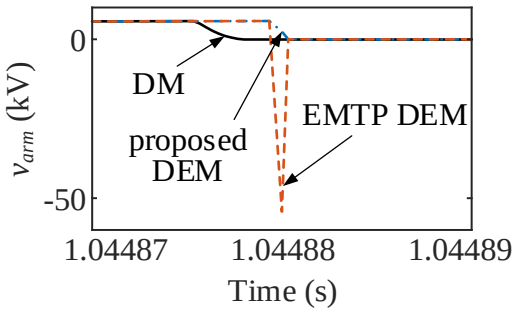
c) zoom 3



d) zoom 4



e) zoom 5



f) zoom 6

Figure 2.35 Arm voltage in phase C lower arm of MMC2 (zoomed)

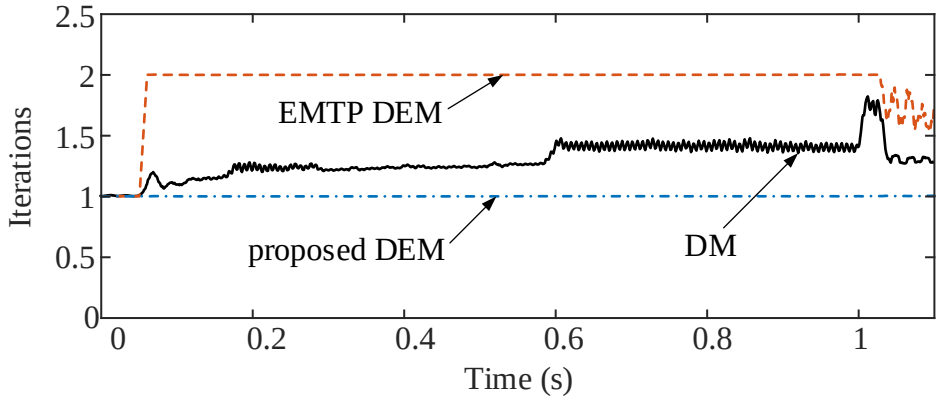


Figure 2.36 Average number of iterations with HB-SMs

2.6.2 AC fault

A single line to ground fault at the point of common coupling (PCC) of MMC1 is applied when the system reaches steady-state at 0.3 s. The fault resistance is 1 Ω and its duration is 200 ms, which allows to see the effects of the DC ripple controller presented in the subsection 2.5.7. The converter blocking is not required so the AVM is also used in this test. It should be noted that the conventional AVM is designed for balanced grid conditions and cannot provide accurate results in this test since the fault is unbalanced. The decoupled AVM (see Figure 2.11) can still provide accurate results in these conditions because the equivalent AVM capacitor C_{AVM} is not directly connected to the DC side so the DC ripple control can be applied. For the SM-level detailed models, the CBA is permutation-based, and the permutation is applied every 50 μs, which allows to see the differences between the SM-level detailed models and the AEM induced by unequal capacitor voltages.

The PCC1 phase voltages are shown in Figure 2.37. The small amplitude oscillations in phase A voltage are caused by the zero sequence currents from the AC system 1. The AC side MMC1 currents are shown in Figure 2.38. The three-phase currents are balanced even though the AC voltages are not. This is due to the balanced positive sequence reference distribution control (see subsection 2.5.4), which actively tracks the negative sequence currents and keeps them equal zero. The outer loop control action such as the AC side power tracking is performed by the positive sequence currents. The waveforms in Figure 2.37 and Figure 2.38 are obtained with the DM but are identical to the waveforms with all other models.

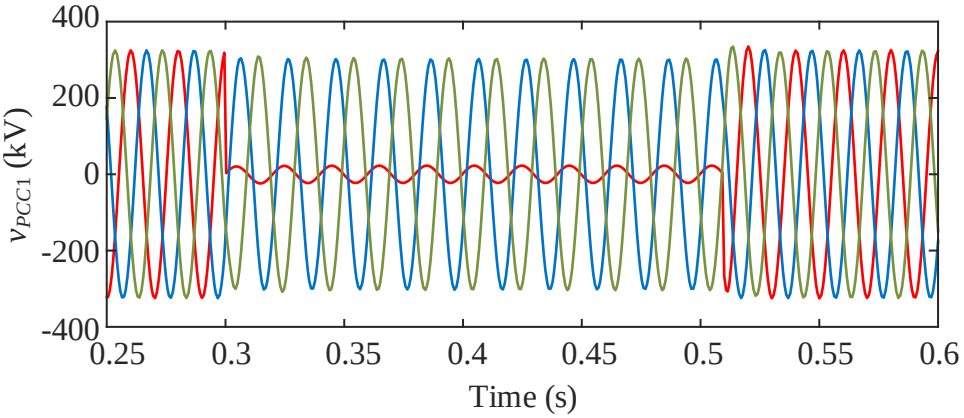


Figure 2.37 PCC1 voltages

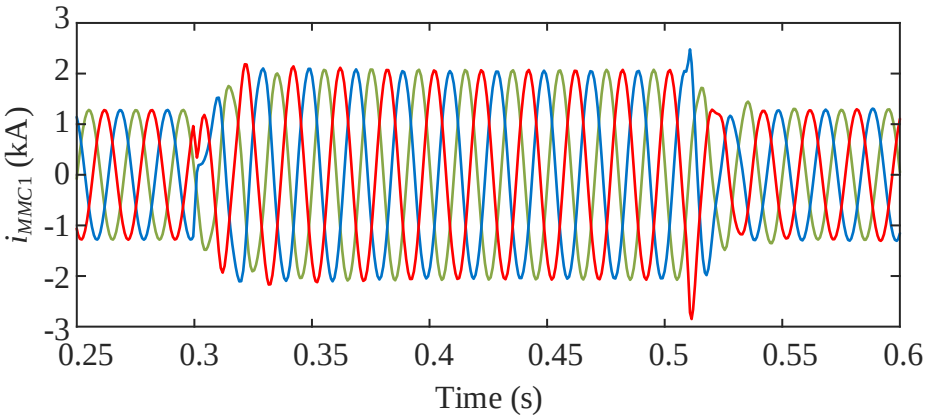


Figure 2.38 MMC1 AC side currents

The DC voltage shown in Figure 2.39 and Figure 2.40 allows to clearly see the difference between the conventional and the Hybrid-AVM: the DC voltage with the conventional AVM oscillates at double line frequency during the fault whereas the Hybrid-AVM keeps the voltage free of oscillations. This is achieved by the additional DC side modulation capability of the model (2.76), which allows to add the DC side ripple control as the more detailed models (see subsection 2.5.7). The DEM closely matches the DM results and only slightly deviates from it, whereas the AEM's DC voltage has larger deviations, as it can be seen in Figure 2.40. The same conclusions can be drawn from the DC current shown in Figure 2.41 and Figure 2.42.

From Figure 2.39 and Figure 2.41 it is clear that the AVM cannot accurately represent fast transients but the overall dynamics are still similar to the behavior of the more detailed models and the steady-state values of currents and voltages match the reference values set in the control system.

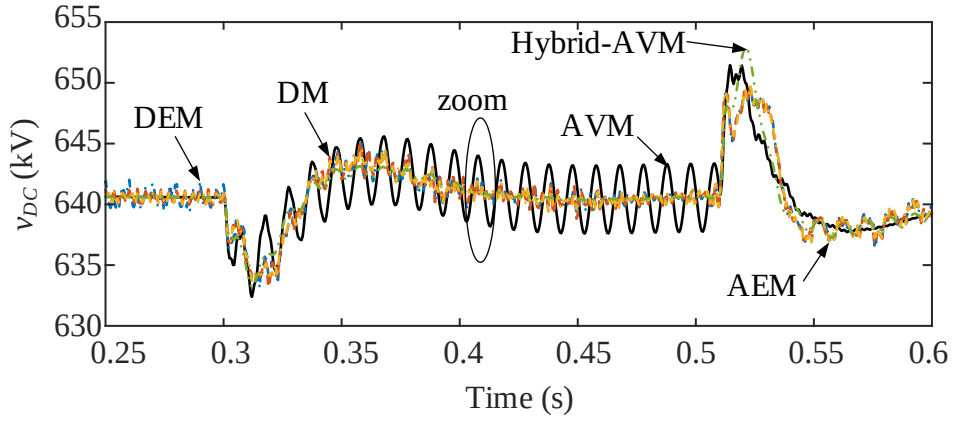


Figure 2.39 DC voltage at MMC1 terminals

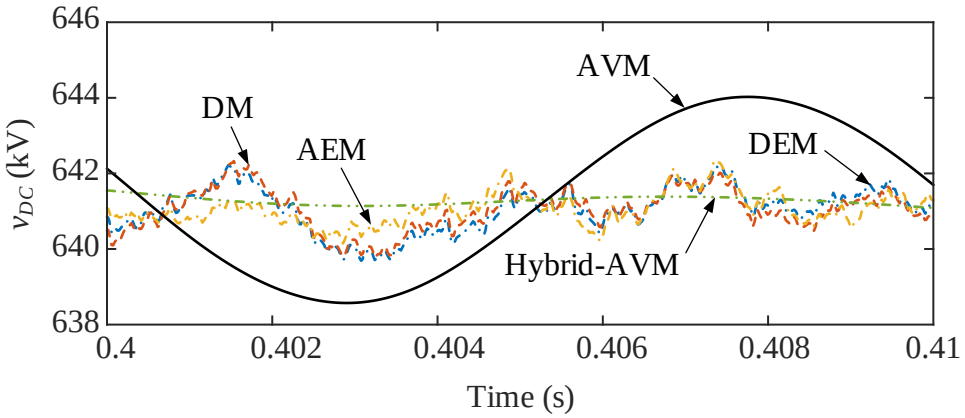


Figure 2.40 DC voltage at MMC1 terminals (zoom)

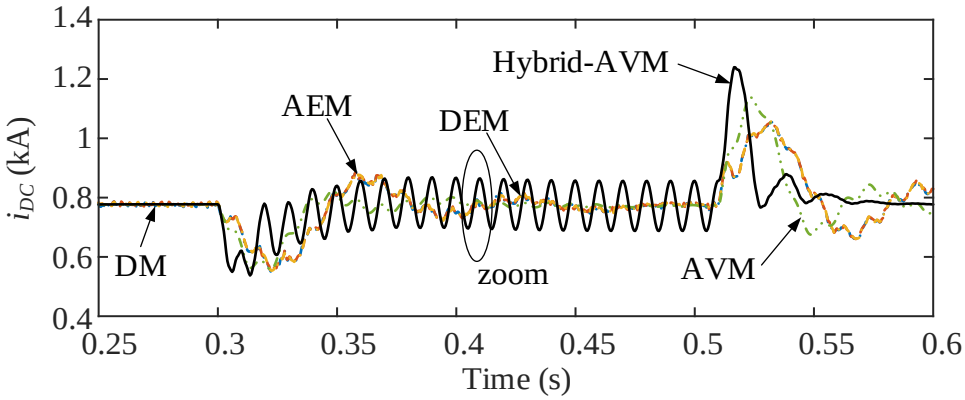


Figure 2.41 DC current at MMC1 terminals

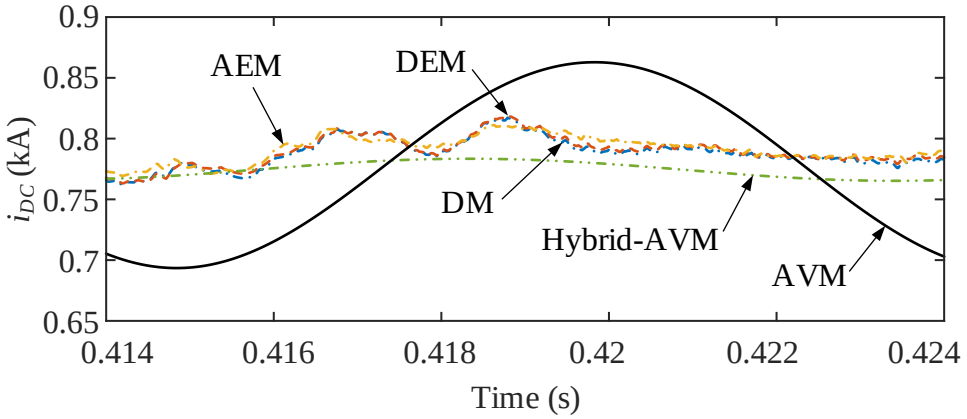


Figure 2.42 DC current at MMC1 terminals (zoom)

The inability to keep the DC voltage constant with the conventional AVM comes from the fact the AC side power is oscillating during grid unbalance, and these power oscillations directly affect the energy stored in the converter capacitor E_{AVM} (2.74). The DC side decoupling in the Hybrid-AVM allows the internal energy to oscillate while keeping the DC voltage constant by varying the value of s_{DC} with the DC ripple suppression controller as in the more detailed models. In the conventional AVM, the capacitor is directly connected to the DC circuit, which makes the oscillations appear at the DC side.

The average capacitor voltage in Figure 2.43 and Figure 2.44 oscillates during the fault at the double line frequency. With the AVMs, the average value of the voltage is higher than the one obtained with more detailed models that represent the internal arm capacitor dynamics.

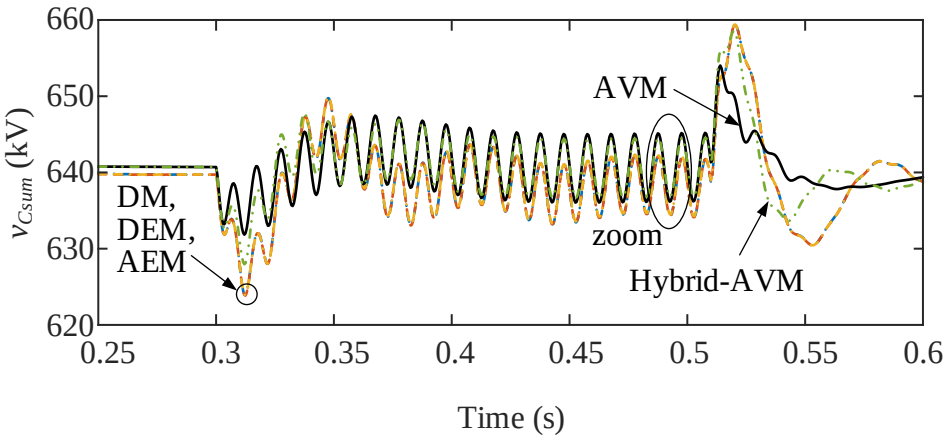


Figure 2.43 Average capacitor voltage of MMC1

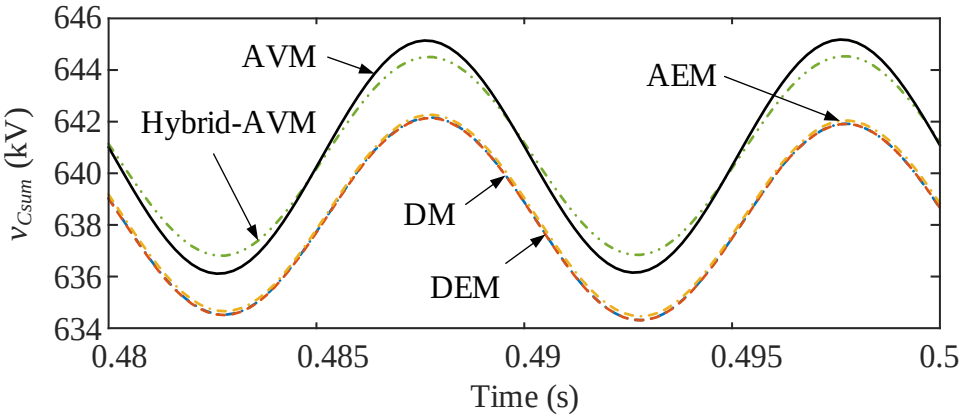


Figure 2.44 Average capacitor voltage of MMC1 (zoom)

2.6.3 DC fault

A pole-to-pole fault in the middle of the DC cable is applied at 0.3 s. Since converter blocking is required, the AVM is not taking part in this comparison, only the DM, DEM, and AEM. The blocking signal is activated by the protection system at 0.301 s when the DC current reaches the value of 5 p.u.

All the tested models exhibit very similar behavior, as demonstrated in the total capacitor voltage (Figure 2.45), arm current (Figure 2.46) and DC voltage (Figure 2.47) waveforms. The only variable where the differences between the models are visible, is the arm voltage (Figure 2.48), where the DM has more variation in the first instants following the fault.

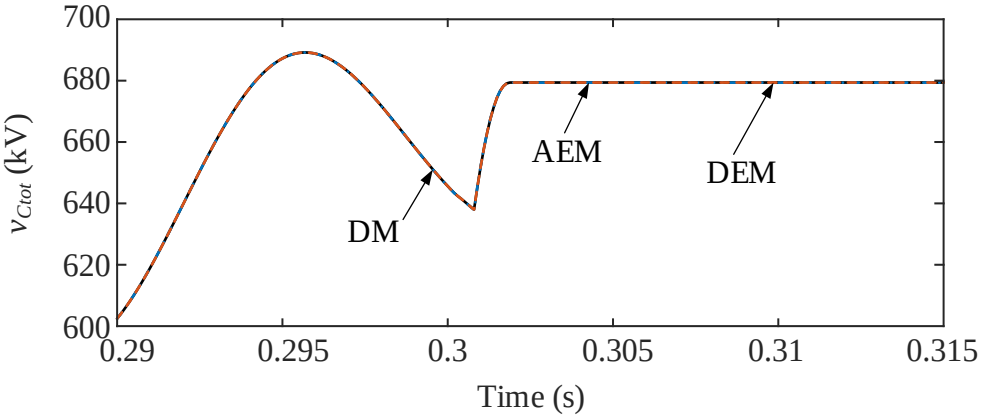


Figure 2.45 Total capacitor voltage in phase A upper arm of MMC2

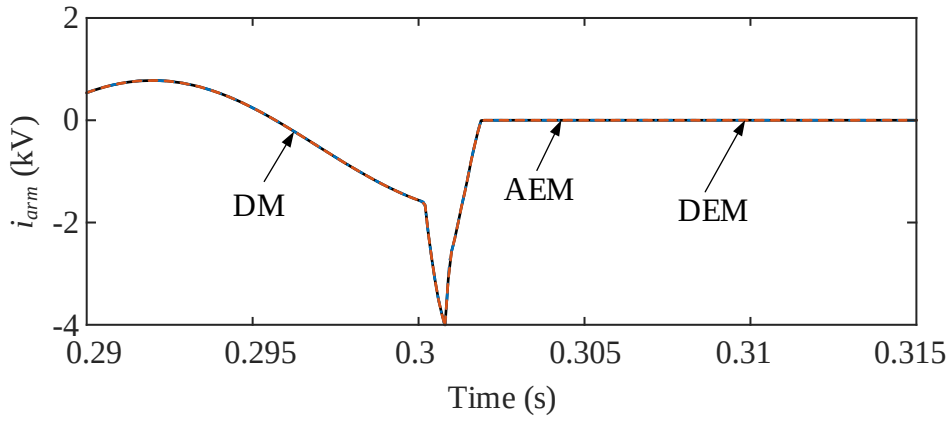


Figure 2.46 Arm current in phase A upper arm of MMC2

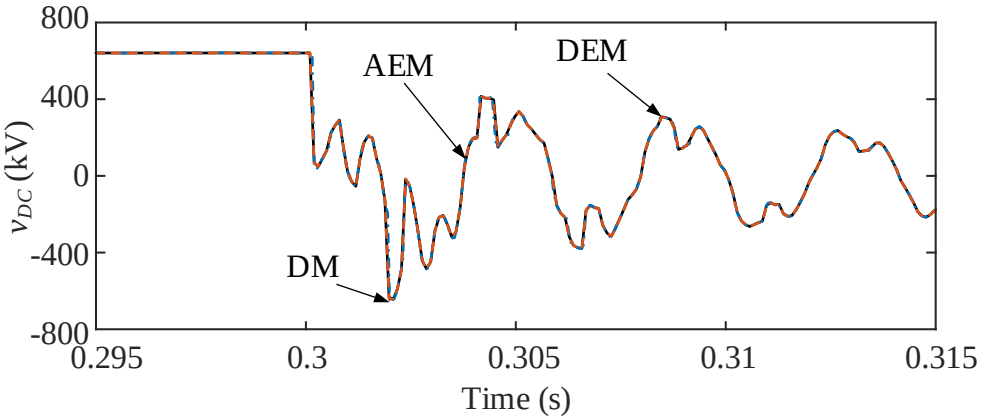


Figure 2.47 DC voltage

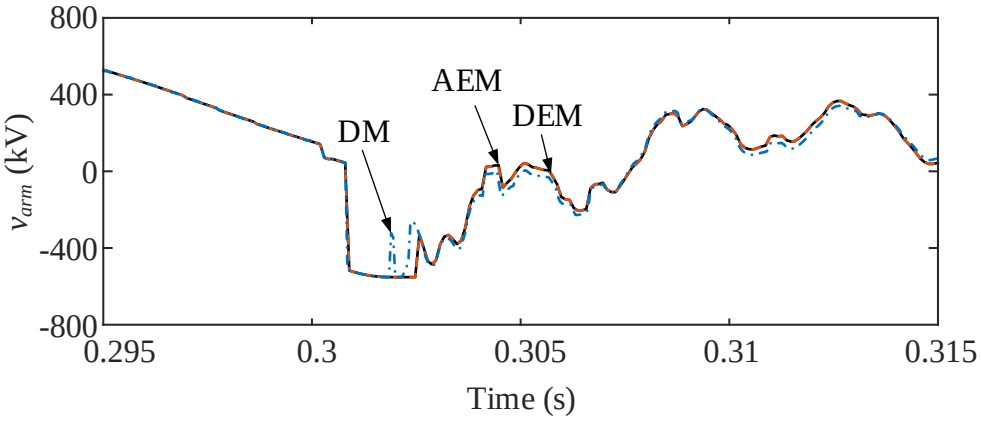


Figure 2.48 Arm voltage

2.6.4 DC voltage reversal

In this test, the DC voltage reference is changed from V_{DC} to $-0.8V_{DC}$. The control system presented in the subsection 2.5.10 is used. The converters have only FB-SMs. Now permutation is applied once every 20 μs. All four models are compared. Since the Hybrid-AVM is also used in the comparison, only the global variables such as the DC current and voltage and the average capacitor voltage are compared, because the AVM does not have the arm-level details.

The average capacitor voltages in Figure 2.49 and Figure 2.50 with all models are smooth and close to each other. However, the voltages of the less detailed models are relatively closer to each other than to the DM reference, as shown in Figure 2.50. The DC currents with different models in Figure 2.51 also match each other well. The zoomed version in Figure 2.52 demonstrates that the AVM does not represent the high-frequency ripple which is visible in the waveforms of more detailed models.

The AEM and DEM have the closest matching waveforms, they are closer to each other than in the previous AC fault test owing to the smaller CBA permutation period, which keeps SM voltages closer to each other. Similar conclusions can be drawn from the DC voltage waveforms in Figure 2.53 and Figure 2.54. With all models, the DC voltage reversal capability is validated. The transients are slow, so even the least detailed models, such as the Hybrid-AEM, are able to provide accurate results.

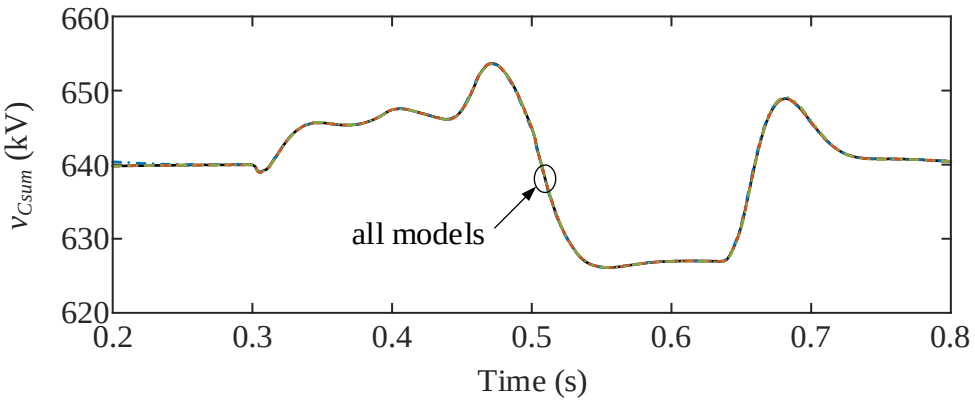


Figure 2.49 Average capacitor voltage of MMC2

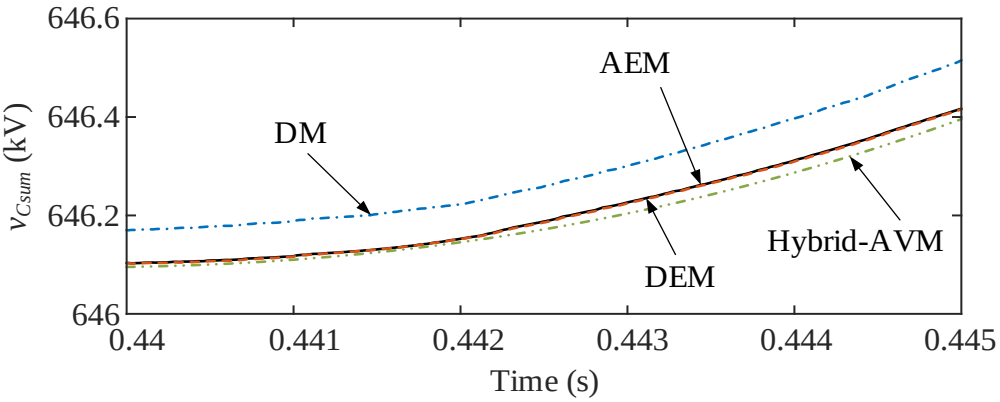


Figure 2.50 Average capacitor voltage of MMC2 (zoom)

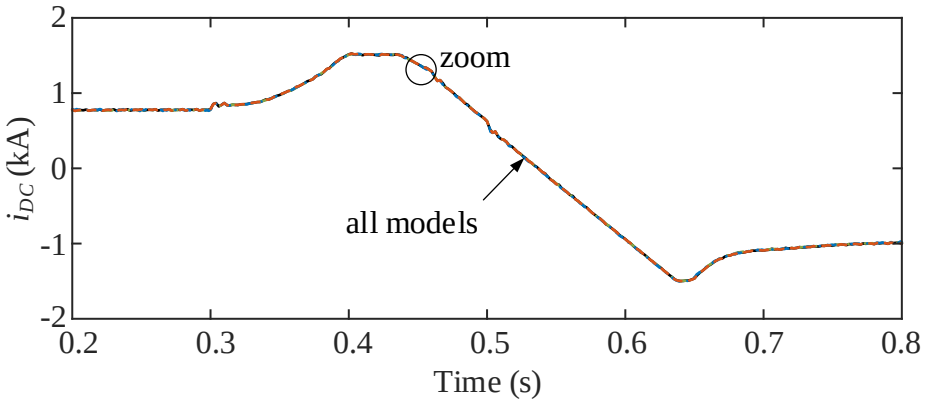


Figure 2.51 DC current

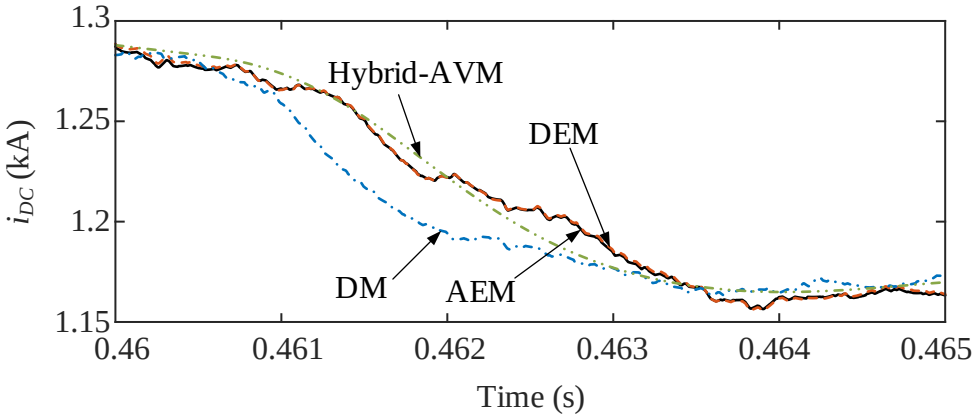


Figure 2.52 DC current (zoom)

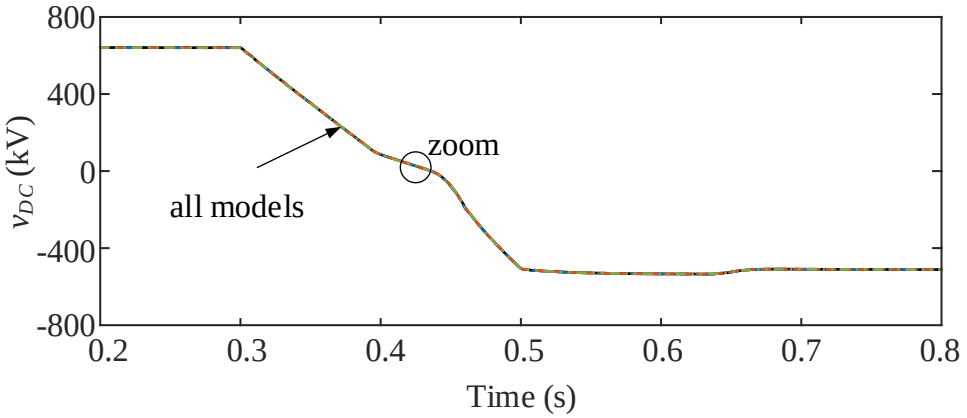


Figure 2.53 DC voltage

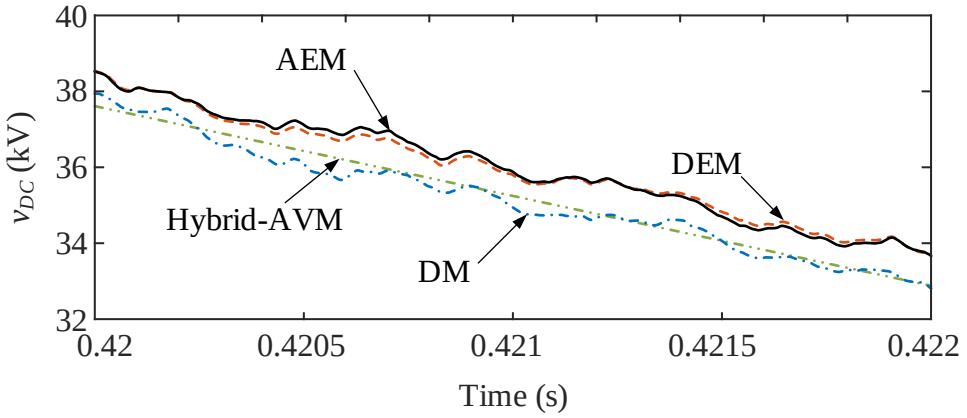


Figure 2.54 DC voltage (zoom)

2.6.5 Computing times

All models are compared during normal operation of the MMC-HVDC link. The simulation time is 0.1 second and the time-step is 1 μs. The results are shown in Table 2.1.

It can be seen that the DM is considerably slower than any other model, it is more than 20 times slower than the DEM. The computing time of the DEM is higher than that of all other models except the DM. The AEM is slower than the AVM, but faster than the Hybrid-AVM with refactoring. This is due to the implementation of the DC side decoupling in the Hybrid-AVM, which is performed by an ideal transformer with a variable transformation ratio. The ideal transformer is implemented using the voltage-source-equations part of the MANA [83], which requires to refactor the MNE matrix every time the value of the transformation ratio changes. The conventional AVM uses only ideal controlled voltage and current sources, which do not cause

matrix refactorization, so its computing time is smaller. If the MNE matrix refactoring is not requested, the computing time of the Hybrid-AVM is only slightly higher than that of the AVM.

Table 2.1 Computing times with different models

Model	**DM**	**DEM**	**AEM**	**AVM**	**Hybrid-AVM**	
					No refactoring	**With refactoring**
Time (s)	1787.07	80.97	35.26	28.96	31.72	55.48

2.7 Conclusions

All hybrid MMC models, (the DEM, the Hybrid-AEM, and the Hybrid-AVM), have been validated against the DM in various transient scenarios, including the start-up procedure, AC and DC faults, and DC voltage reversal tests.

The DEM can replicate the DM behavior with a high degree of accuracy even during high-frequency transients and keep the simulation time considerably lower. The difference between the DEM and the DM reference is that the transitions are much smoother with the DM due to the smooth v-i characteristics of semiconductor switches. The proposed blocked mode algorithm allows to eliminate the spikes in the arm voltage waveforms present in the existing EMTP implementation of the DEM and to reduce the number of iterations.

The proposed Hybrid-AEM matches the results of more detailed models with a high degree of accuracy in various conditions, as long as the individual SM voltages in more detailed models are kept close to each other by the CBA. When the differences between the individual SM voltages is relatively high, the AEM may not be able to capture all transients accurately. The average number of iterations with the proposed Hybrid-AEM is close to one.

The AVM cannot be used during blocking and does not provide accurate results during high-frequency transients; therefore its application is limited to slower transients and higher-level controller design. The decoupling of the internal capacitor and the DC side circuit allows to better represent the converter behavior during unbalanced faults and makes it possible to simulate the DC voltage reversal. However, this additional functionality comes at the expense of increasing computing times.

CHAPTER 3 INITIALIZATION OF MODULAR MULTILEVEL CONVERTER MODELS IN ELECTROMAGNETIC TRANSIENT SIMULATIONS

A typical EMT-type simulation study starts with an initialization transient. Applying a disturbance to simulate a specific phenomenon during initialization may trigger protection functions, cause inaccurate results, and other unwanted effects which will hinder the analysis of the system. Therefore, the disturbance must be applied once the system reaches steady-state, i.e. when the initialization transient falls below an acceptable level. Depending on the system, this transient can take a significant amount of time, in the order of several seconds of simulation time.

The initialization transient occurs because initial values of some variables used in the simulation differ from steady-state values. Accurate steady-state initialization of all variables in EMT simulations can eliminate the transient and associated problems and provide a significant improvement in computation times especially when detailed models are used. However, this is a nontrivial task, especially in cases involving MMC-HVDC transmissions due to the nonlinearity and complexity of MMC models and controls [156].

AC-DC power-flow solution techniques [157-159] are usually considered as the first step of the initialization process but since the power-flow solvers usually do not consider internal control system of AC/DC converters, further analysis is necessary for accurate initialization. Steady-state analysis including MMC controls can be found in [160-165], but in these publications it is assumed that either most of control signals are known in advance or only the fundamental components in the control system are considered, which is not realistic for a typical MMC, where the second harmonic components are present in arm switching functions and cannot be ignored. A more advanced steady-state analysis is presented in [166], but only the cases where the second harmonics of arm switching functions are known in advance are considered.

A method for steady-state initialization of MMCs is proposed in this chapter. It is able to initialize all internal variables of an MMC station, including low-level parameters of the detailed MMC models, such as the voltages and switch states in each individual submodule. The method requires the prior knowledge of AC and DC voltage and current phasors.

3.1 Overview of the initialization process

It should be noted that the proposed method focuses on the MMC models that represent arm capacitor dynamics, namely, the AEM and DEM. The AVM disregards such details and therefore its electrical circuit can be easily initialized by directly using the DC current and voltage values provided by the load-flow solver without the proposed iterative algorithm. It is only the AVM capacitor voltage $v_{C\,AVM}$ that needs to be initialized: $v_{C\,AVM} = v_{DC} - 2\,i_{DC}\,R_{arm}/3$ (see Figure 2.11). Its control system uses the same control blocks as the AEM and DEM and is therefore initialized in the same manner as will be demonstrated further in this chapter.

The proposed initialization method for MMC models consists of two stages. First, steady-state harmonics of capacitor voltages and arm switching functions are calculated using arm voltage and current phasors. Then, internal electrical circuit and control system of the MMC model are initialized. If a large-scale power system is simulated, an AC-DC power-flow solution must be found to obtain accurate steady-state values of arm voltages and currents and to initialize other models, such as transmission lines, cables, electrical machines, etc. In the following, it will be supposed that steady-state arm voltages and currents are known. The initialization process of a generic EMT study involving MMCs can be presented as follows:

1. Prerequisites:
   1.1. perform AC-DC power-flow calculation in the network;
   1.2. initialize time-domain models of other elements.
2. Proposed initialization procedure. For each MMC in the grid:
   2.1. retrieve arm voltages and currents (DC and fundamental phasors $I_0, \bar{I}_1, V_0, \bar{V}_1$) from the power-flow solution for all six arms;
   2.2. for each arm, find the arm switching function and total capacitor voltage harmonics ($S_0, \bar{S}_1, \bar{S}_2$ and $V_{Ctot\,0}, \bar{V}_{Ctot\,1}, \bar{V}_{Ctot\,2}$ respectively) using the iterative algorithm;
   2.3. initialize control system of the MMC based on results from steps 2.1 and 2.2;
   2.4. initialize SM voltages based on results from steps 2.1 and 2.2.

This process is shown schematically in Figure 3.1.

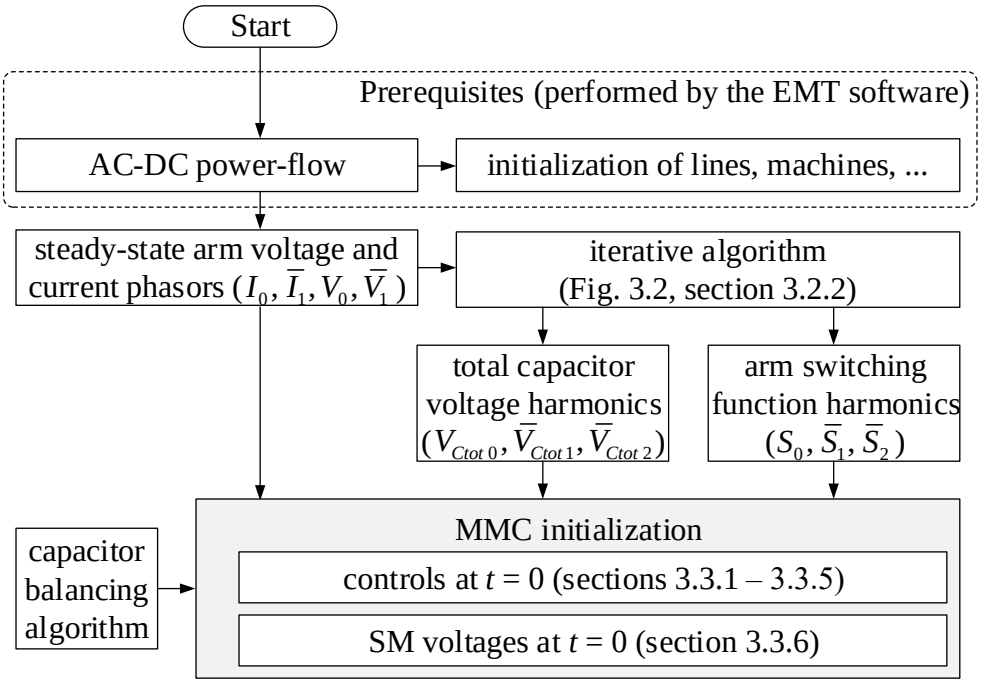


Figure 3.1 Overview of the proposed initialization process

3.2 MMC equations in steady-state

To correctly initialize MMC models, steady-state analysis must be carried out. The following assumptions are made for MMC-HVDC systems considered in this chapter:

- Generic cascade control system is used, achieving perfect reference tracking in steady-state without limit violations.
- CCSC is applied and DC ripple control is present, which is typical in MMC-HVDC transmissions.
- High-order harmonics arising from the discrete modular nature of the converter are neglected as they are small in magnitude due to the large number of MMC levels.

With these assumptions, the control system is considered linear. Also, in such a case, arm currents i_{arm} and voltages v_{arm} contain only DC and fundamental components. In balanced conditions, the DC component of i_{arm} is equal to $-i_{DC}/3$, and that of v_{arm} is equal to $v_{DC}/2$ minus the voltage drop on the arm resistance R_{arm}. Up to the second-order harmonics will be considered for the total capacitor voltage v_{Ctot} (i.e. the sum of all capacitor voltages in the arm), for the arm switching

function s_{arm} and for the capacitor charging current i_{Ctot}. The DC component of i_{Ctot} is equal to zero in steady-state. Therefore, the following equations can be written for each arm:

$$v_{arm} = v_0 + v_1 = V_0 + V_1 \cos\left(\omega t + \varphi_{v1}\right) \tag{3.1}$$

$$i_{arm} = i_0 + i_1 = I_0 + I_1 \cos\left(\omega t + \varphi_{i1}\right) \tag{3.2}$$

$$i_{Ctot} = i_{Ctot1} + i_{Ctot2} = I_{Ctot1} \cos\left(\omega t + \varphi_{ic1}\right) + I_{Ctot2} \cos\left(2\omega t + \varphi_{ic2}\right) \tag{3.3}$$

$$v_{Ctot} = v_{Ctot0} + v_{Ctot1} + v_{Ctot2} = V_{Ctot0} + V_{Ctot1} \cos\left(\omega t + \varphi_{vc1}\right) + V_{Ctot2} \cos\left(2\omega t + \varphi_{vc2}\right) \tag{3.4}$$

$$s_{arm} = s_0 + s_1 + s_2 = S_0 + S_1 \cos\left(\omega t + \varphi_{s1}\right) + S_2 \cos\left(2\omega t + \varphi_{s2}\right) \tag{3.5}$$

where the subscripts 0, 1 and 2 denote the zero-, first- and second-order harmonics respectively, ω is the grid frequency in rad/s, and φ_x is the angle of any variable x in radians.

The following steady-state equations hold for each MMC arm:

$$v_{arm} = v_{Ctot}\ s_{arm} \tag{3.6}$$

$$i_{Ctot} = i_{arm}\ s_{arm} \tag{3.7}$$

$$v_{Ctot\,n} = \frac{1}{C_{eq}} \int i_{Ctot\,n}\left(\tau\right) d\tau \tag{3.8}$$

where the subscript n denotes the n-th harmonic (except zero), $C_{eq} = C_{SM} / N_{SM}$ is the equivalent capacitance, C_{SM} is SM capacitance, and N_{SM} is the number of SMs per arm.

An iterative solution approach is proposed to obtain the steady-state harmonics in (3.4) and (3.5). The details of the algorithm are presented in the following section. Complex notation is used, i.e. for any variable x: $x = X \cos\left(\omega t + \varphi_x\right) \rightarrow X \angle \varphi_x \rightarrow \overline{X}$.

3.2.1 Equations for capacitor voltage and switching function harmonics

For each MMC arm it is necessary to find up to the second harmonic terms of the total capacitor voltage (3.4) and arm switching function (3.5). The DC component of s_{arm} is taken as $S_0 = 0.5$.

The proposed system of complex equations linking known and unknown variables based on the equations (3.1)–(3.8) is formulated as:

$$\bar{V}_{Ctot1} = \frac{1}{j\omega C_{eq}}\left[\bar{I}_1\, S_0 + I_0\, \bar{S}_1 + \frac{1}{2}\bar{I}_1^{*}\, \bar{S}_2\right] \tag{3.9}$$

$$\bar{V}_{Ctot2} = \frac{1}{j2\omega C_{eq}}\left[I_0\, \bar{S}_2 + \frac{1}{2}\bar{I}_1\, \bar{S}_1\right] \tag{3.10}$$

$$\bar{S}_1 = \frac{1}{V_{Ctot0}}\left[\bar{V}_1 - S_0\, \bar{V}_{Ctot1} - \frac{1}{2}\overline{S'^{*}_1}\, \bar{V}_{Ctot2} - \frac{1}{2}\bar{S}_2\, \bar{V}_{Ctot1}\right] \tag{3.11}$$

$$V_{Ctot0} = \frac{1}{S_0}\left[V_0 - \frac{1}{2}\mathrm{Re}\left(\bar{V}_{Ctot1}\, \overline{S_1^{*}} + \bar{V}_{Ctot2}\, \overline{S_2^{*}}\right)\right] \tag{3.12}$$

$$\bar{S}_2 = -\frac{1}{V_{Ctot0}}\left[S_0\, \bar{V}_{Ctot2} + \frac{1}{2}\bar{S}_1\, \bar{V}_{Ctot1}\right] \tag{3.13}$$

The derivation of these equations is presented below. The asterisk represents complex conjugation. This system of equations is nonlinear and unknown quantities are present both on left- and right-hand sides of all the equations.

3.2.1.1 Capacitor voltage fundamental component

The phasor of the total capacitor voltage fundamental ($\bar{V}_{Ctot1}$) can be obtained using the equation of the fundamental term of i_{Ctot}. From (3.2), (3.3), (3.5), and (3.7):

$$\begin{aligned} i_{Ctot1} &= I_{Ctot1}\cos\left(\omega t + \varphi_{ic1}\right) \\ &= I_1 S_0 \cos\left(\omega t + \varphi_{i1}\right) + I_0 S_1 \cos\left(\omega t + \varphi_{s1}\right) + \frac{I_1 S_2}{2}\cos\left(\omega t + \varphi_{s2} - \varphi_{i1}\right) \end{aligned} \tag{3.14}$$

$$\bar{I}_{Ctot1} = \bar{I}_1 S_0 + I_0 \bar{S}_1 + \frac{1}{2}\bar{I}_1^{*}\bar{S}_2 \tag{3.15}$$

From (3.15) and (3.8):

$$\bar{V}_{Ctot1} = \frac{\bar{I}_{Ctot1}}{j\omega C_{eq}} = \frac{1}{j\omega C_{eq}}\left[\bar{I}_1\, S_0 + I_0\, \bar{S}_1 + \frac{\bar{I}_1^{*}\, \bar{S}_2}{2}\right] \tag{3.16}$$

3.2.1.2 Capacitor voltage second harmonic

Using a similar formulation, the second harmonic of the total capacitor voltage ($\overline{V}_{Ctot2}$) can be found:

$$i_{Ctot2} = I_{Ctot2}\cos\left(2\omega t + \varphi_{ic2}\right) = I_0 S_2 \cos\left(2\omega t + \varphi_{s2}\right) + \frac{I_1 S_1 \cos\left(2\omega t + \varphi_{i1} + \varphi_{s1}\right)}{2} \tag{3.17}$$

$$\overline{I}_{Ctot2} = I_0\ \overline{S_2} + \frac{\overline{I_1}\ \overline{S_1}}{2} \tag{3.18}$$

$$\overline{V}_{Ctot2} = \frac{\overline{I}_{Ctot2}}{j2\omega C_{eq}} = \frac{1}{j2\omega C_{eq}}\left[I_0\ \overline{S_2} + \frac{\overline{I_1}\ \overline{S_1}}{2}\right] \tag{3.19}$$

3.2.1.3 Arm switching function fundamental component

The fundamental component of the arm switching function ($\overline{S_1}$) can be calculated from the equation of v_{arm}:

$$\begin{aligned} v_1 &= V_1\cos\left(\omega t + \varphi_{v1}\right) \\ &= V_{Ctot0} S_1 \cos\left(\omega t + \varphi_{s1}\right) + S_0 V_{Ctot1}\cos\left(\omega t + \varphi_{c1}\right) \\ &+ \frac{S_1 V_{Ctot2}}{2}\cos\left(\omega t + \varphi_{vc2} - \varphi_{s1}\right) + \frac{S_2 V_{Ctot1}}{2}\cos\left(\omega t + \varphi_{s2} - \varphi_{vc1}\right) \end{aligned} \tag{3.20}$$

In (3.20), S_1 and φ_{s1} contribute to two summands. The multiplication with the second harmonic of capacitor voltage produces much smaller impact on the final value of $v_1(t)$. Hence, for this summand the values can be taken from the previous iteration (shown as $\overline{S'_1}$). Finally, $\overline{S_1}$ is

$$\overline{S_1} = \frac{1}{V_{Ctot0}}\left[\overline{V_1} - S_0\ \overline{V}_{Ctot1} - \frac{1}{2}\overline{S'^{*}_1}\ \overline{V}_{Ctot2} - \frac{1}{2}\overline{S_2}\ \overline{V}_{Ctot1}\right] \tag{3.21}$$

3.2.1.4 Capacitor voltage DC component

The DC component of capacitor voltage (V_{Ctot0}) can be calculated from the equation of the DC component of v_{arm}:

$$v_0 = V_0 = V_{Ctot0}\ S_0 + \frac{1}{2}V_{Ctot1}\ S_1\cos\left(\varphi_{vc1} - \varphi_{s1}\right) + \frac{1}{2}V_{Ctot2}\ S_2\cos\left(\varphi_{vc2} - \varphi_{s2}\right) \tag{3.22}$$

$$V_{Ctot0} = \frac{1}{S_0}\left[V_0 - \frac{1}{2}\mathrm{Re}\left(\overline{V}_{Ctot1}\,\overline{S_1^*} + \overline{V}_{Ctot2}\,\overline{S_2^*}\right)\right] \tag{3.23}$$

3.2.1.5 Arm switching function second harmonic

The second harmonic of the switching function ($\overline{S_2}$) can be calculated from the second harmonic of v_{arm}, which equals zero at steady-state due to CCSC and DC ripple control.

$$v_2 = 0 = S_0 V_{Ctot2}\cos\left(2\omega t + \varphi_{vc2}\right) + V_{Ctot0} S_2 \cos\left(2\omega t + \varphi_{s2}\right) + \frac{S_1 V_{Ctot1}}{2}\cos\left(2\omega t + \varphi_{vc1} + \varphi_{s1}\right) \tag{3.24}$$

$$\overline{S_2} = -\frac{1}{V_{Ctot0}}\left[S_0\,\overline{V}_{Ctot2} + \frac{\overline{S_1}\,\overline{V}_{Ctot1}}{2}\right] \tag{3.25}$$

3.2.2 Solution and initial approximation

Different methods can be used to solve equations (3.9)–(3.13). A fixed-point iterative method is used in this thesis: at each iteration, unknown variables are successively refined by recalculating equations (3.9)–(3.13) one by one. The initial guess is found as:

$$V_{Ctot0} \approx 2V_0 \tag{3.26}$$

$$\overline{S_1} \approx \frac{V_1}{2V_0}\angle\varphi_{v1} \tag{3.27}$$

$$\overline{S_2} \approx 0\angle 0 \tag{3.28}$$

Initial values from (3.26)–(3.28) are sufficient to start the iterative algorithm. At the end of each iteration, relative errors in amplitude ε_X and phase angle ε_φ are calculated. For any variable x:

$$\varepsilon_X = \frac{\left|X^k - X^{k-1}\right|}{\left[X^k + X^{k-1}\right]/2} \tag{3.29}$$

$$\varepsilon_\varphi = \frac{\left|\varphi_x^k - \varphi_x^{k-1}\right|}{2\pi} \tag{3.30}$$

where k is the iteration count.

The algorithm stops when the amplitude and phase errors of all variables are below a predefined tolerance ε_{MAX}. Since high-order harmonics are not considered in (3.1)–(3.5), the tolerance limit is set to $\varepsilon_{MAX} = 10^{-5}$, higher precision is unnecessary. In all performed tests under various conditions sufficient precision has been obtained in no more than five iterations, so a limit is set on the maximum number of iterations: $k_{MAX} = 5$.

The full algorithm is shown in Figure 3.2.

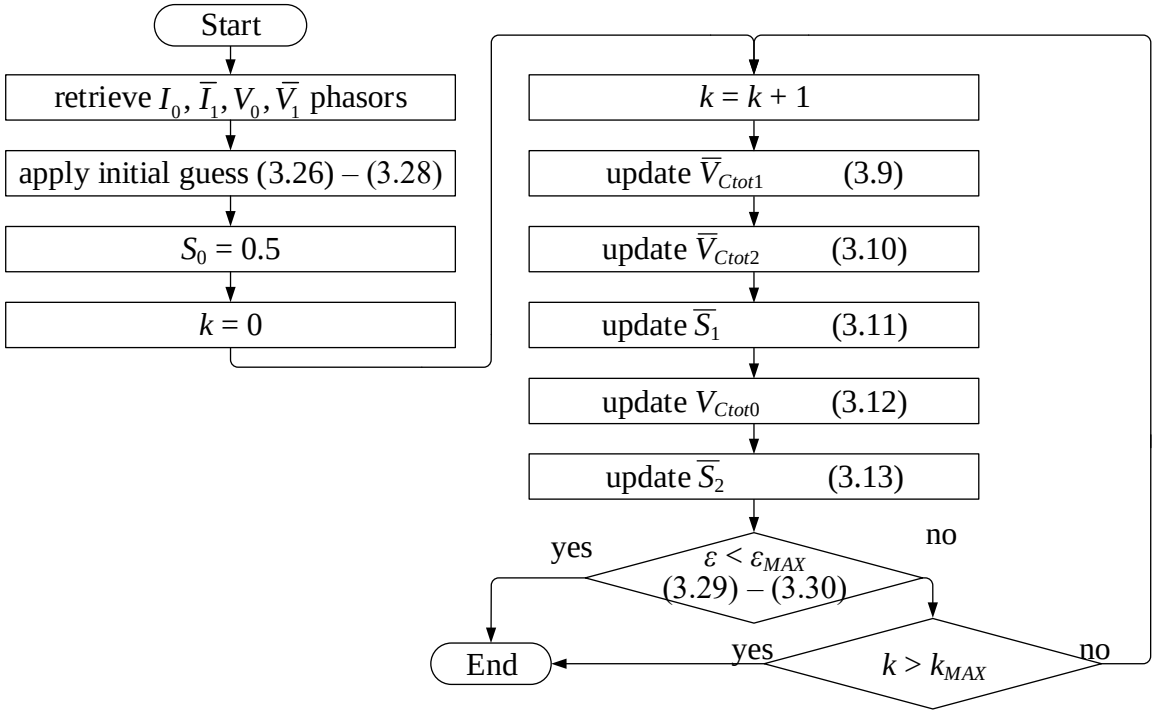


Figure 3.2 Iterative algorithm

3.3 MMC station initialization

Once the steady-state harmonics of v_{Ctot} and s for all six arms of each MMC have been found, the control system of the MMC and its SM voltages can be initialized.

3.3.1 Control system initialization

The considered generic cascade control system consists of linear regulators due to the perfect reference tracking assumption. Hence, only the integral parts of the controllers must be initialized as the contributions of proportional terms are all equal to zero.

Unbalance between upper and lower leg of any given phase is disregarded. The output signals of AC current regulators, CCSC, and DC ripple controls can be found by applying Fortescue, Clarke or Park transformations to the appropriate harmonics of the three-phase control signals (i.e. arm switching functions s). AC current regulators use the fundamentals $\overline{S}_1$ (3.11), and circulating current controls use the second harmonics $\overline{S}_2$ (3.13).

If the above assumptions are not respected, the proposed initialization algorithm might not be able to reduce the initialization transient to negligible values.

3.3.2 Inner control

3.3.2.1 Proportional-integral current control

PI controllers in d-q reference frame can be used to handle the positive and negative sequence AC side currents and CCSC. For the AC current control, AC side currents can be obtained from arm currents with KCL.

Output signals of the current regulator s_{1d}^{+} and s_{1q}^{+} can be obtained by applying Park transformation matrix $\left[\mathbf{P}^{+1}\right]$ to the fundamentals of arm switching functions s_1 (3.11). Lower arm signals are considered but upper arm signals could also be used since unbalance between arms is disregarded:

$$\begin{bmatrix} s_{1d}^{+} \\ s_{1q}^{+} \end{bmatrix} = k_{p.u.} \left[\mathbf{P}^{+1}\right] \begin{bmatrix} s_{1la} \\ s_{1lb} \\ s_{1lc} \end{bmatrix} \tag{3.31}$$

where $k_{p.u.}$ is added to adjust for the p.u. control system.

History terms of the integral blocks of the positive sequence AC current regulator in d-q frame H_{1d}^{+} and H_{1q}^{+} (Figure 3.3) can be then initialized as:

$$H_{1d}^{+} = s_{1d}^{+} + L_{\Sigma}\omega\, i_{q1}^{+} \tag{3.32}$$

$$H_{1q}^{+} = s_{1q}^{+} - L_{\Sigma}\omega\, i_{d1}^{+} \tag{3.33}$$

where $L_{\Sigma} = L_{trfo} + L_{arm}/2$ is the AC side equivalent, L_{arm} is the arm and L_{trfo} is the transformer inductance; i_{d1}^{+}, i_{q1}^{+} are the positive sequence AC side currents in d-q reference frame.

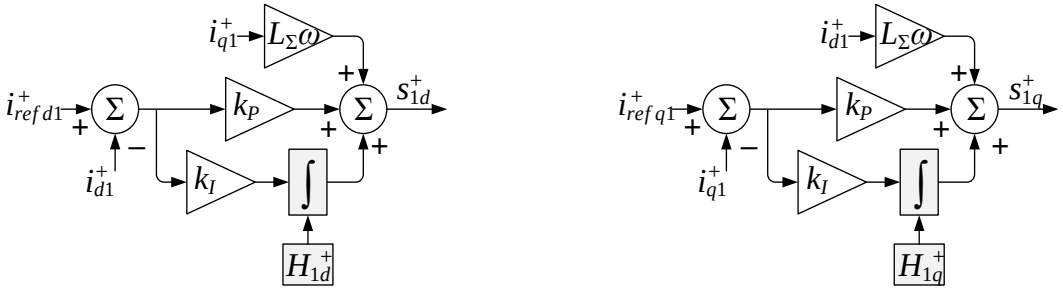


Figure 3.3 AC side current PI controllers with initialization in positive d-q frame

History terms of the negative sequence AC side current control can be found using the same approach

$$H_{1d}^{-} = s_{1d}^{-} - L_{\Sigma}\omega\, i_{q1}^{-} \tag{3.34}$$

$$H_{1q}^{-} = s_{1q}^{-} + L_{\Sigma}\omega\, i_{d1}^{-} \tag{3.35}$$

Considering that there are no second harmonic currents in steady-state conditions, CCSC integral history terms are found as

$$H_{2d}^{+} = s_{2d}^{+} \tag{3.36}$$

$$H_{2q}^{+} = s_{2q}^{+} \tag{3.37}$$

$$H_{2d}^{-} = s_{2d}^{-} \tag{3.38}$$

$$H_{2q}^{-} = s_{2q}^{-} \tag{3.39}$$

3.3.2.2 Proportional-resonant current control

Proportional-Resonant controllers can be used for primary AC side current control, CCSC and DC ripple control. AC side current PR controller equations are formulated in Laplace domain as

$$S_{PR1\alpha}(s) = \left[I_{ref\,1\alpha}(s) - I_{1\alpha}(s) \right] \left[k_P + \frac{k_R\, s}{s^2 + \omega^2} \right] \tag{3.40}$$

$$S_{PR1\beta}(s)=\left[I_{ref\,1\beta}(s)-I_{1\beta}(s)\right]\left[k_P+\frac{k_R\,s}{s^2+\omega^2}\right] \tag{3.41}$$

where $I_{1\alpha}(s)$, $I_{1\beta}(s)$, $I_{ref\,1\alpha}(s)$, and $I_{ref\,1\beta}(s)$ are the Laplace transforms of the measured and reference AC side currents in α-β frame, k_P and k_R are the proportional and resonant coefficients.

Contribution of the proportional branch equals zero in steady-state due to the perfect reference tracking, so only the resonant branch must be initialized. The resonant branch can be implemented as a combination of two integrals (Figure 3.4) based on the following equations. Resonant part of the α-channel PR current controller $S_{R1\alpha}(s)$ in Laplace domain is

$$S_{R1\alpha}(s)=\left[I_{ref\,1\alpha}(s)-I_{1\alpha}(s)\right]\frac{k_R\,s}{s^2+\omega^2} \tag{3.42}$$

Multiplying both sides of (3.42) by $\left[s^2+\omega^2\right]/s^2$ yields

$$S_{R1\alpha}(s)+S_{R1\alpha}(s)\frac{\omega^2}{s^2}=\frac{1}{s}\left[I_{ref\,1\alpha}(s)-I_{1\alpha}(s)\right]k_R \tag{3.43}$$

By rearranging the terms, the following equation is obtained

$$S_{R1\alpha}(s)=\frac{1}{s}\left[\left[I_{ref\,1\alpha}(s)-I_{1\alpha}(s)\right]k_R-\frac{1}{s}S_{R1\alpha}(s)\omega^2\right] \tag{3.44}$$

Knowing that $1/s$ in (3.44) is the Laplace transform of an integral, the implementation shown in Figure 3.4 can be easily obtained. Equation for the β-channel is identical.

In steady-state, the outputs of PR regulators are described by generic cosine functions that can be obtained by applying Clarke transformation to arm switching functions

$$s_{PR1\alpha}(t)=S_{PR1\alpha}\cos\left(\omega t+\varphi_{PR1\alpha}\right) \tag{3.45}$$

$$s_{PR1\beta}(t)=S_{PR1\beta}\cos\left(\omega t+\varphi_{PR1\beta}\right) \tag{3.46}$$

History terms of the integrals for the α-channel $H1_{1\alpha}$ and $H2_{1\alpha}$ are obtained as follows: it can be seen that the output of one integral ($H1_{1\alpha}$) is connected to the output of the regulator, so since the proportional term is disregarded, it is equal to the output signal

$$H1_{1\alpha} = S_{PR1\alpha}\cos\left(\omega t + \varphi_{PR1\alpha}\right) \tag{3.47}$$

The output of the other integral ($H2_{1\alpha}$) can be obtained as the input (i.e. derivative) of the first integral with a minus sign:

$$H2_{1\alpha} = -\frac{d}{dt}H1_{1\alpha} = \omega S_{PR1\alpha}\sin\left(\omega t + \varphi_{PR1\alpha}\right) \tag{3.48}$$

History terms for the β-channel integrals are obtained as

$$H1_{1\beta} = S_{PR1\beta}\cos\left(\omega t + \varphi_{PR1\beta}\right) \tag{3.49}$$

$$H2_{1\beta} = -\frac{d}{dt}H1_{1\beta} = \omega S_{PR1\beta}\sin\left(\omega t + \varphi_{PR1\beta}\right) \tag{3.50}$$

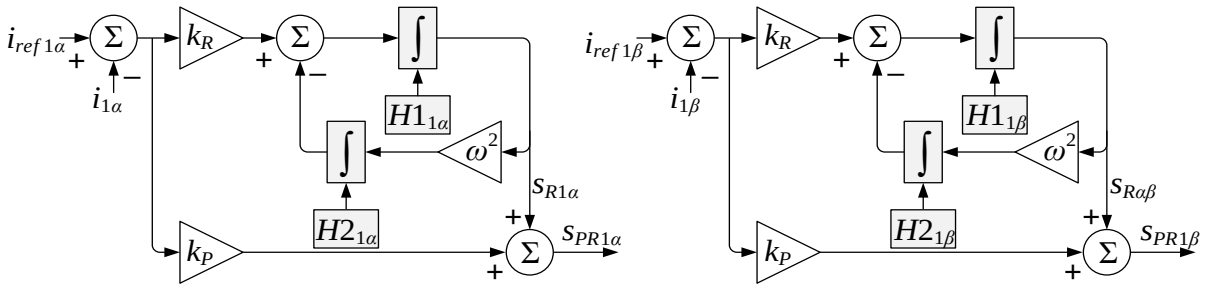


Figure 3.4 AC side current PR controllers with initialization in α-β frame

CCSC integral history terms are found in a similar manner as

$$H1_{2\alpha} = S_{PR2\alpha}\cos\left(2\omega t + \varphi_{PR2\alpha}\right) \tag{3.51}$$

$$H2_{2\alpha} = -\frac{d}{dt}H1_{2\alpha} = 2\omega S_{PR2\alpha}\sin\left(2\omega t + \varphi_{PR2\alpha}\right) \tag{3.52}$$

$$H1_{2\beta} = S_{PR2\beta}\cos\left(2\omega t + \varphi_{PR2\beta}\right) \tag{3.53}$$

$$H2_{2\beta} = -\frac{d}{dt}H1_{2\beta} = 2\omega S_{PR2\beta}\sin\left(2\omega t + \varphi_{PR2\beta}\right) \tag{3.54}$$

3.3.3 Outer control

The outer controls consist of PI regulators and produce the reference values for the inner AC side current controller. The active current channel is used to control either the active power (P) or the

DC voltage (V_{DC}). The reactive current channel is used to control the reactive power (Q) or the AC voltage (V_{AC}). History values of the corresponding integrals (H_P, $H_{V_{DC}}$, H_Q, $H_{V_{AC}}$) are defined by the average active (P_{PCC}) and reactive (Q_{PCC}) powers at the point of common coupling (PCC):

$$H_P = H_{V_{DC}} = P_{PCC} = v_d^+ i_d^+ + v_q^+ i_q^+ + v_d^- i_d^- + v_q^- i_q^- \tag{3.55}$$

$$H_Q = H_{V_{AC}} = Q_{PCC} = v_q^+ i_d^+ - v_d^+ i_q^+ + v_q^- i_d^- - v_d^- i_q^- \tag{3.56}$$

where v_d^+, v_q^+, v_d^-, v_q^- are the voltages and i_d^+, i_q^+, i_d^-, i_q^- are the currents at the PCC in positive and negative d-q frames.

In case of nominal PCC voltage, history terms in (3.55) and (3.56) will simply be equal in p.u. to the positive sequence currents i_d^+ and i_q^+, respectively.

3.3.4 PLL

In steady-state, the frequency is equal to its nominal value and the PLL is perfectly synchronized with the PCC voltage. Hence, the initial phase angle of the PLL (Θ) can be calculated from the positive sequence PCC voltage in α-β frame v_α^+ and v_β^+:

$$\Theta = \text{atan2}\left(v_\beta^+, v_\alpha^+\right) \tag{3.57}$$

3.3.5 SM level control

Since arm switching functions are known with the help of the algorithm in Figure 3.2, the number of SMs to be inserted n_{ref} for each arm is calculated as

$$n_{ref} = \text{round}\left(s_{arm}\ N_{SM}\right) \tag{3.58}$$

As SM level control has an immediate action, there is no history term to initialize. If all SMs have the same initial capacitor voltage, CBA can select SMs in any order for the first time-step (sequentially, uniformly), in any case a transient is inevitable because SM voltages are not exactly equal to each other and are constantly changing their values as long as the arm current is not equal to zero. The initial selection will not have any impact on the simulation results because all SMs are

identical. However, if uniform capacitor voltage distribution is considered (as per section 3.3.6.2), the SMs should be inserted uniformly to minimize transients.

3.3.6 SM capacitor voltage

For accurate initialization, it is necessary to provide initial voltage for each SM if detailed models are used. Several initialization approaches are considered.

3.3.6.1 Equal SM voltages

The easiest approach is initializing all SMs with the same capacitor voltage value which is equal to the average value:

$$v_{SM\,j} = v_{Ctot} / N_{SM} \tag{3.59}$$

where $j = 1, 2, ..., N_{SM}$ is the SM index.

However, this leads to a short initial transient in the simulation because the SM voltages in the arm are not actually equal to each other.

3.3.6.2 SM voltages with NLC CBA

Accurate initialization needs to account for the differences in SM voltages introduced by the capacitor balancing algorithm (CBA). Several CBAs exist, and each can have a different impact on the distribution of SM voltages. The Nearest Level Control (NLC) and permutation-based CBA are considered in the following. A permutation is the insertion of the SM with the lowest voltage and bypassing of the SM with the highest voltage at each time-step (with charging arm current, opposite otherwise).

The following assumptions are made for the CBA:

- Uniform distribution of SM voltages around average value;
- SMs are inserted when their voltage is the lowest and bypassed when their voltage is the highest in the arm (with charging arm current, opposite otherwise);
- Inserted SMs are distributed uniformly by their voltage.

Additional assumptions are made for the simulation:

- The simulation time-step Δt is sufficiently small to assume that the arm current and the number of inserted SMs do not change for several time-steps;
- All SMs are in the same conditions regarding negative insertion in steady-state: if SMs are only inserted positively, presented calculations are valid for hybrid MMCs with any number of HB and FB-SMs. If SMs need to be inserted negatively at some periods, presented calculations will only be valid for MMC arms with only FB-SMs, since HB-SMs would be all bypassed during these periods, i.e. the uniformity would be broken.

In such conditions, it is sufficient to know the maximum excursion of SM voltage around the average value (denoted as Δv_{MAX}) to obtain individual SM voltages. To find Δv_{MAX}, the concept of insertion time τ_{ins} is introduced: if a submodule is inserted at $t = \tau - \tau_{ins}/2$, it will be kept inserted until $t = \tau + \tau_{ins}/2$, after which it will be bypassed. In other words, SMs are kept inserted for τ_{ins} around the instant $t = \tau$. With the small time-step assumption, the insertion time can be obtained as

$$\tau_{ins} = \Delta t \; n_{ref} / n_{perm} \tag{3.60}$$

where n_{perm} is the number of permutations per time-step.

In the simulations with relatively larger time-steps, the precision of τ_{ins} in (3.60) can be improved by deducing the equivalent number of permutations per time-step

$$n_{perm} \approx N_0 + \left| \frac{n_{add}}{2} \right| \approx N_0 + \Delta t \left| \frac{d}{dt} s_{arm} \right| \frac{N_{SM}}{2} \tag{3.61}$$

where N_0 is the constant number of permutations per time-step as defined by the CBA and n_{add} is the number of added SMs (negative if SMs are removed). It is divided by two to get the equivalent number of permutations, because only one SM is affected, whereas the permutation acts on two SMs.

The passing arm current charges inserted SMs, so the voltage change of one SM during τ_{ins} can be calculated as

$$\Delta v_{SM} = \frac{1}{C_{SM}} \int_{t-\tau_{ins}/2}^{t+\tau_{ins}/2} i(\xi)\, d\xi \approx \frac{i\, \tau_{ins}}{C_{SM}} \tag{3.62}$$

and the change in the average value of SM voltage in the arm can be written as:

$$\frac{\Delta v_{Ctot}}{N_{SM}} = \frac{1}{N_{SM} C_{eq}} \int_{t-\tau_{ins}/2}^{t+\tau_{ins}/2} i_{Ctot}(\xi)\, d\xi \approx \frac{i\, s_{arm}\, \tau_{ins}}{C_{SM}} \tag{3.63}$$

Maximum excursion of SM voltage around the average value can be found as the difference between (3.62) and (3.63):

$$\Delta v_{MAX} = \Delta v_{SM} - \frac{\Delta v_{Ctot}}{N_{SM}} \approx \frac{i_{arm}\left[1 - s_{arm}\right]\tau_{ins}}{C_{SM}} \tag{3.64}$$

Finally, the initial SM voltages can be expressed as:

$$v_{SM\,j} = \frac{v_{Ctot}}{N_{SM}} + \Delta v_{MAX}\left[\frac{j-1}{N_{SM}-1} - \frac{1}{2}\right] \tag{3.65}$$

3.3.6.3 SM voltages with PWM-based control

Another type of SM-level control is based on Pulse-Width Modulation, including phase-shift PWM (PS-PWM), phase-disposition PWM and others [143]. Although PWM-based controls are usually applied for the MMCs with a relatively low number of levels, the proposed initialization procedure is still applicable. If PS-PWM control is considered, equations (3.62)–(3.65) are valid if the PWM frequency F_{PWM} is several times higher than the grid frequency. Only the insertion time τ_{ins} should be calculated differently:

$$\tau_{ins} = s_{arm} / F_{PWM} \tag{3.66}$$

It has been reported that without additional measures PWM-based control can cause voltage imbalance [137, 144], therefore, similarly to [144], a simple sorting algorithm can be added that selects the most appropriate SMs to insert or to bypass when the number of SMs changes.

3.3.7 Delays

If the EMT simulation software solves control and power system equations simultaneously, the above initialization procedures are sufficient to avoid initialization transients. However, there can be a one-time-step delay between the solution of control and power system equations. Additional delays can be present when external code is referenced in the form of a dynamic-link library (DLL).

To counteract the presence of these delays and minimize their effects on initialization, it is proposed to extrapolate arm switching function signals by one time-step for each delay present in the control loop:

$$s_{arm}^{ext}(t) \approx s_{arm}(t) + m\,\Delta t \frac{ds_{arm}(t)}{dt} \approx [m+1]s_{arm}(t) - m\,s_{arm}(t-\Delta t) \tag{3.67}$$

where s_{arm}^{ext} is the extrapolated signal; m is the number of time-steps to extrapolate.

3.4 Simulation results

The initialization method developed in this chapter can be implemented in any EMT-type simulation tool using available external programming interfaces. In this paper, it was implemented and tested in EMTP [83] using a DLL interface.

The simulated network is a point-to-point symmetrical monopole hybrid MMC-HVDC link with 101 levels shown in Figure 2.29, its parameters are listed in the Appendix B. The DEM is used for both MMCs. The control system includes PR controllers for AC side currents, CCSC and DC ripple suppression. MMC1 controls P and Q, MMC2 controls V_{DC} and Q.

The convergence of the algorithm proposed in section 3.2 is shown in Figure 3.5 for phase-A upper arm variables of MMC1. All the variables gradually converge to an accurate solution. The values at the fifth iteration are used for the initialization of MMCs (section 3.3) because all the relative errors are below $\varepsilon_{MAX} = 10^{-5}$.

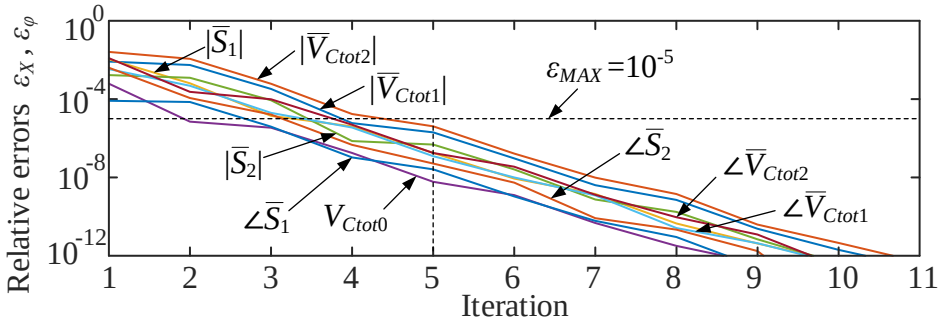


Figure 3.5 Convergence of the iterative algorithm

3.4.1 External behavior

The external behavior of the converter is evaluated from the DC voltage and current of MMC1 in Figure 3.6 and Figure 3.7. The fully initialized converter operates in steady-state conditions from the first time-point. On the other hand, it takes more than 0.5 s of simulation time to reach steady-state when starting without performing steady-state analysis and initializing the simulated circuit.

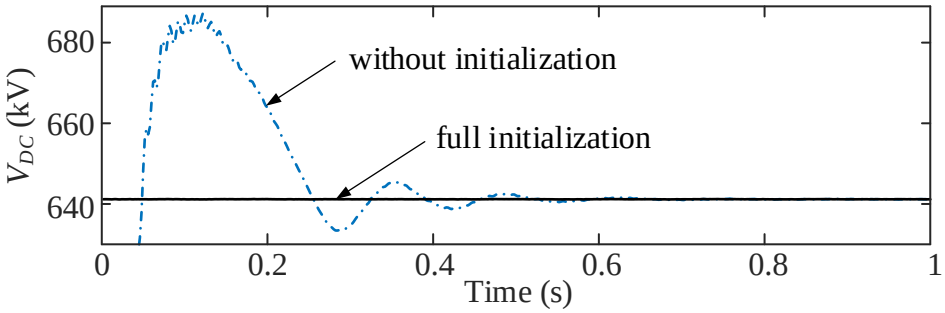


Figure 3.6 DC voltage during initialization transient

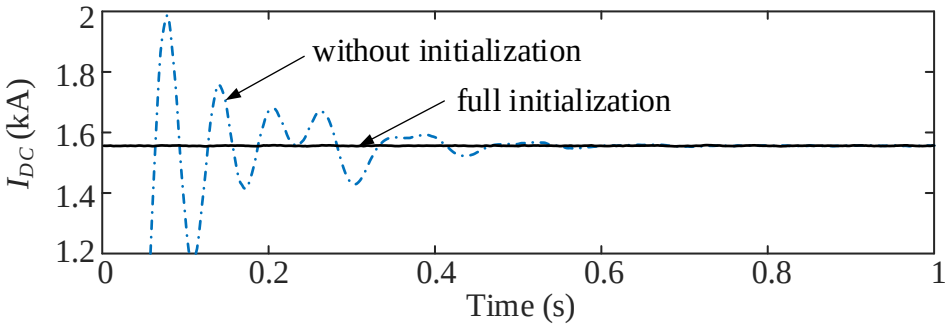


Figure 3.7 DC current during initialization transient

3.4.2 Capacitor voltage

The total capacitor voltage v_{Ctot} of phase A upper arm at MMC1 and its average value during the initial transient are shown in Figure 3.8 and Figure 3.9. In the simulations, the initial values of the capacitor voltages are calculated considering zero-; zero- and first-; zero-, first- and second-order harmonics. Three harmonic components must be considered to eliminate the initialization transient.

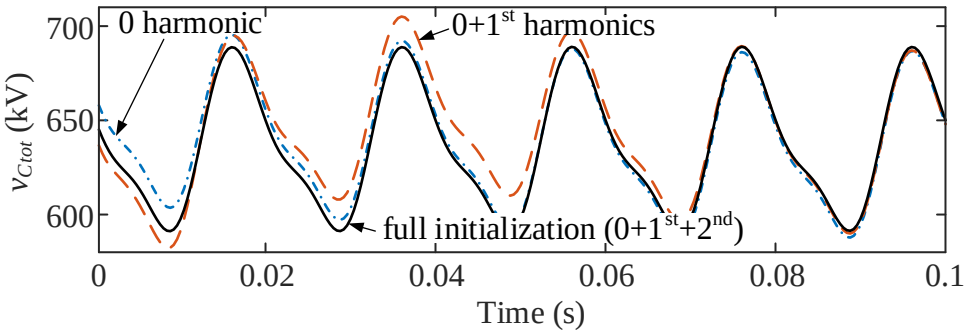


Figure 3.8 Total capacitor voltage waveform depending on the considered harmonics

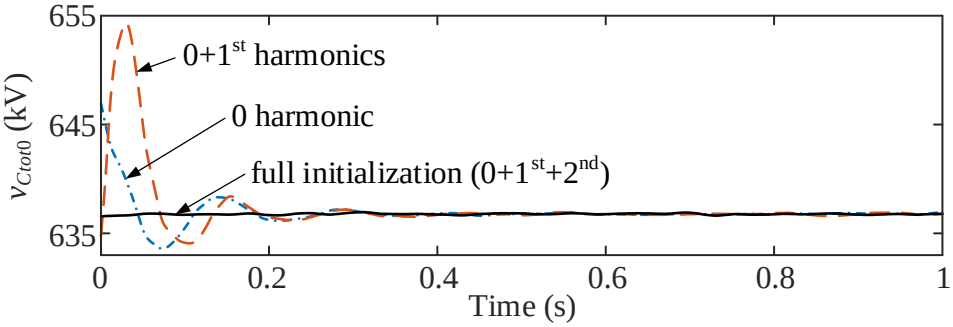


Figure 3.9 Average value of v_{Ctot} depending on the considered harmonics

3.4.3 Control system

The arm switching function s of phase A upper arm at MMC1 and its average value are shown in Figure 3.10 and Figure 3.11. The initial values of the arm switching functions supplied to the time-domain simulation are calculated considering zero-; zero- and first-; zero-, first- and second-order harmonics. For perfect initialization all three harmonic components must be considered.

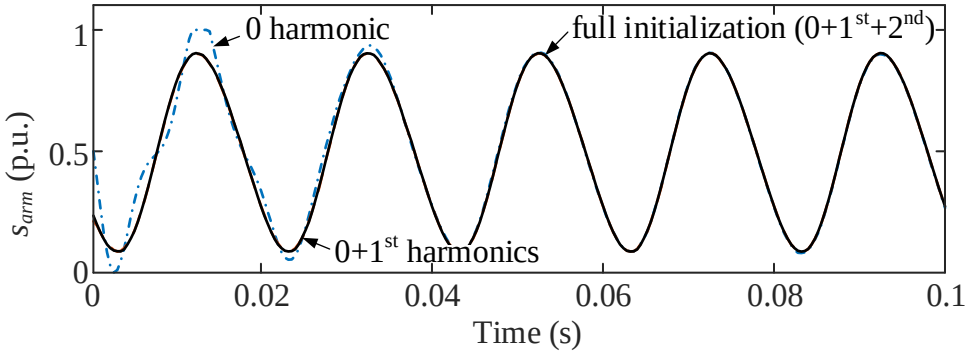


Figure 3.10 Arm switching function waveform depending on the considered harmonics

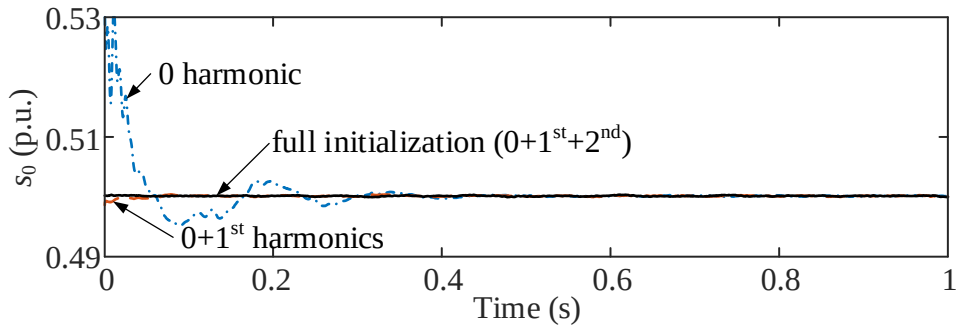


Figure 3.11 Average value of s_{arm} depending on the considered harmonics

3.4.4 SM level initialization

The deviations from the average SM voltage for all capacitors in phase-A upper arm at MMC1 as well as Δv_{MAX} are shown in Figure 3.12 and Figure 3.13. With the identical initial SM voltages, a transient is seen within the first 5 ms. No transient occurs with the uniform distribution of SM voltages. The results also confirm the accuracy of Δv_{MAX} (3.64).

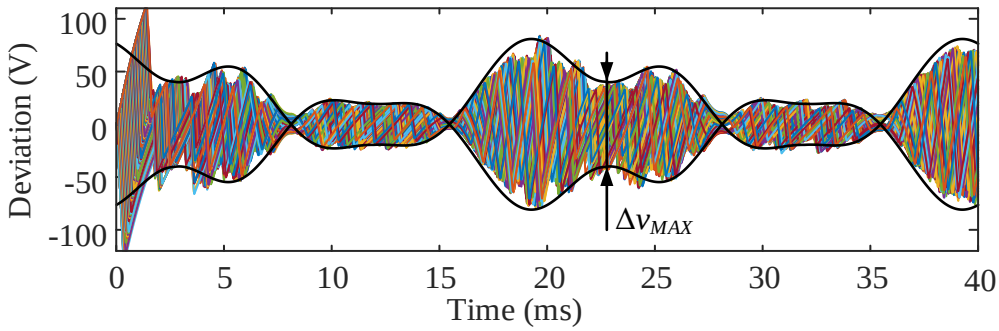


Figure 3.12 Deviations of $v_{SM\ j}$ using identical initial SM voltages

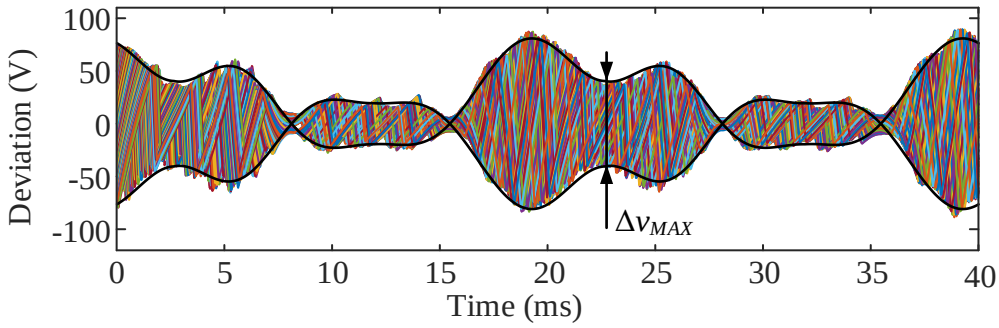
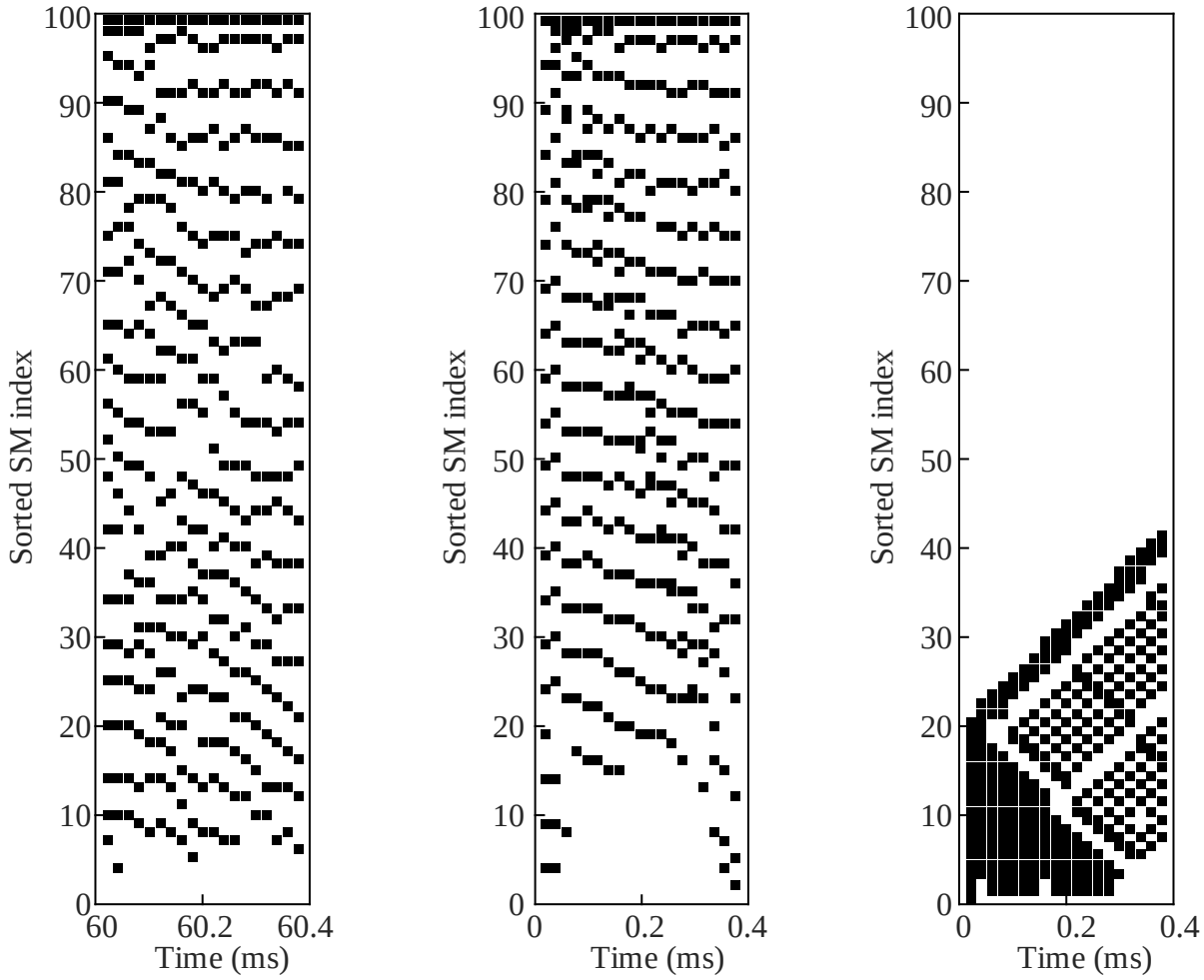


Figure 3.13 Deviations of $v_{SM\ j}$ using uniformly distributed initial SM voltages

Figure 3.14 shows how the inserted SMs are distributed in the arm according to their voltages (black rectangles represent inserted SMs, index 1–lowest voltage, index 100 – highest voltage). Although the distribution is not perfectly uniform in steady-state conditions, as shown in Figure 3.14.a (sometimes adjacent SMs are inserted, up to 10 adjacent SMs are bypassed), it is reasonably close to the uniformity. The initial uniform distribution case in Figure 3.14.b closely resembles the steady-state case. However, when identical initial SM voltages are taken (Figure 3.14.c), distribution is significantly different. As explained in subsection 3.3.1.5, the distribution of inserted SMs in the beginning of the simulation will be as always shown in Figure 3.14.c if all SMs initially have the same voltage, irrespective of the initial selection by the CBA.



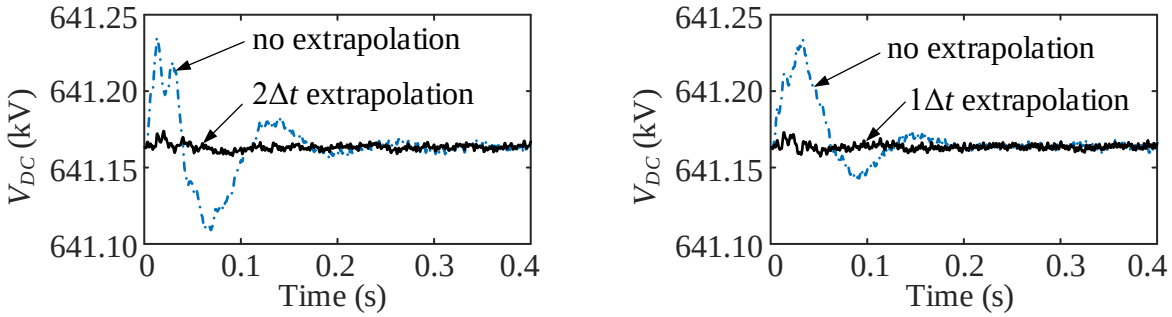
a) at steady-state b) uniformly distributed SM voltages c) identical SM voltages

Figure 3.14 SM indices according to SM voltage sorting

3.4.5 Extrapolation

To demonstrate the effects of extrapolation proposed in section 3.3.7, the number of SMs is set to 400 with 360 FB-SMs and 40 HB-SMs, $\Delta t = 5\,\mu s$. The DC voltage of MMC1 in the beginning of time-domain simulation is shown in Figure 3.15. An initialization transient lasting about 0.2 s can be seen if the extrapolation is omitted. To suppress the transient, a two-time-step extrapolation is applied in the case of DEM (Figure 3.15.a). One time-step covers the delay between the power circuit solution and the control system solution, the other time-step compensates for the delay caused by the implementation of the CBA using a DLL.

In the case of AEM (Figure 3.15.b), only the delay between the power circuit solution and the control system solution is present. Therefore, single-time-step extrapolation can be applied to remove the initialization transient.



a) DEM b) AEM

Figure 3.15 Effect of extrapolation with different MMC models

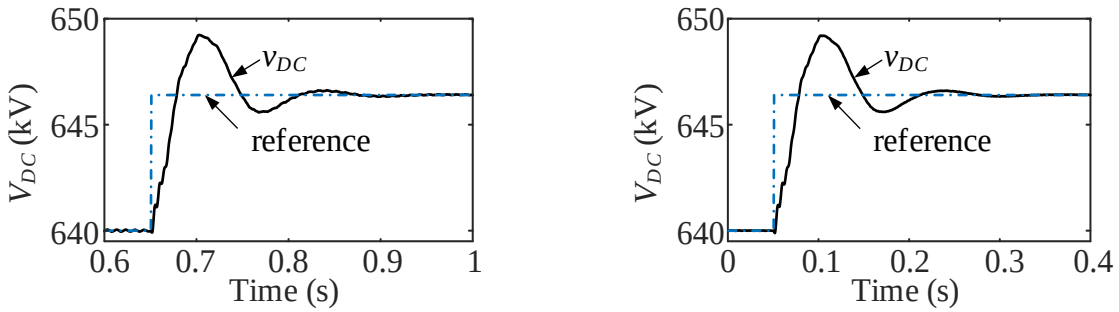
3.4.6 Time gains

3.4.6.1 Test-case 1

To evaluate the computational time reduction resulting from the proposed initialization method, 1% DC voltage reference step is applied at MMC2 when the system reaches steady-state. The same point-to-point MMC-HVDC transmission as in the previous test is used (see Figure 2.29) but with 400 SMs per arm. The DC voltage at MMC2 terminals with and without initialization is shown in Figure 3.16. Without initialization, small oscillations remaining from the initial transient are still visible before the step change (Figure 3.16.a). If these oscillations are neglected, the system is in

steady-state at $t = 0.6\,\text{s}$. With proper initialization, the test can be performed near simulation start-up (Figure 3.16.b).

Transient behavior in both simulations is identical, but the results are obtained faster when initialization is applied because less simulation time is necessary: the CPU time in the test case without initialization is 136.6 s (for 1 s of simulation time). The CPU time in the test case with initialization is 59.2 s (for 0.4 s of simulation time). The time needed to perform initialization of the MMCs with the proposed method is negligible (around 20 milliseconds). Thus, the proposed initialization method allows to save more than 50% of computational time.



a) without initialization b) with initialization

Figure 3.16 DC voltage reference step test

3.4.6.2 Test-case 2

The second test system is shown in Figure 3.17: two 400 kV AC systems are connected through the 101-level MMC HVDC link. The AEM is used for both stations. MMC1 controls active and reactive powers, MMC2 controls DC and AC voltage amplitudes. The system connected to MMC1 is represented with its Thevenin equivalent. The AC system connected to MMC2 is developed using a practical system from [167]. Synchronous machine subnetworks contain detailed machine models with controls and transformers. Loads are modeled by constant impedances. Once the system reaches steady-state, a single-line-to-ground fault is applied at ALIAG bus and is cleared with 0.1 s delay by isolating the ALIAG-SOMA line.

Figure 3.18 shows that initialization transients die out in around 3 s without HVDC link initialization, although all other system components are initialized correctly ($t = 0$ is the time of the fault). The initialization transient is longer compared to the previous test case due to

synchronous machine rotor oscillations. It can be noted that HVDC link variables, such as DC voltage etc., stabilize faster due to the fast control system. Figure 3.19 shows that with the proposed initialization method, the fault can be applied near simulation start-up with no negative effects on the accuracy of the results (both waveforms closely match each other) and therefore save 3 s of simulation time (57.6 s of CPU time).

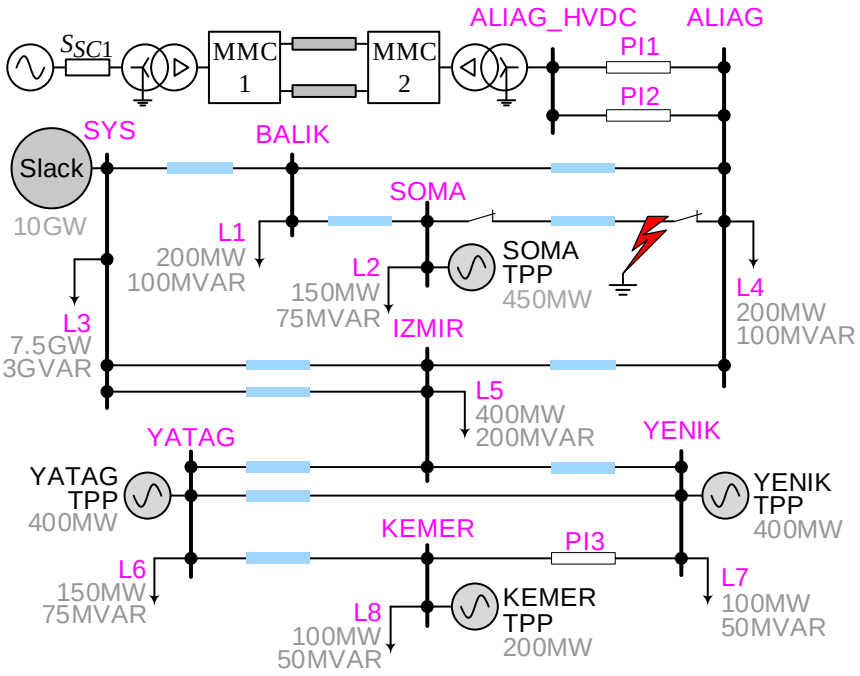


Figure 3.17 Small-scale AC grid

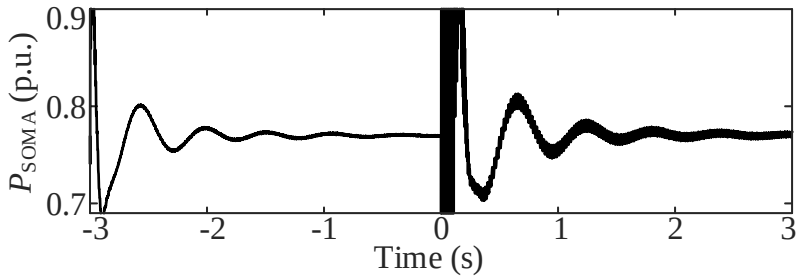


Figure 3.18 Active power at SOMA terminals without MMC initialization

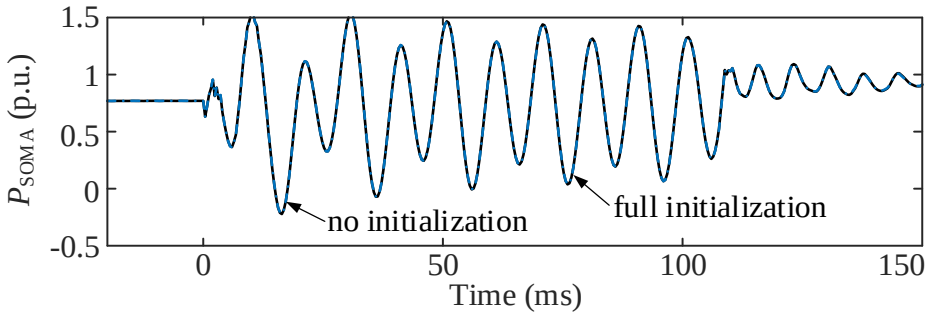


Figure 3.19 Active power at SOMA terminals with and without MMC initialization (zoom)

3.5 Conclusion

This chapter presented an accurate steady-state initialization method for MMC models used in the EMT-type simulations.

The proposed new method uses steady-state arm voltages and currents to obtain steady-state harmonics of total capacitor voltages and arm switching functions for all six arms of each MMC present in the simulated design. It initializes electrical and control system variables, including individual capacitor voltages and gating signals of each SM. The MMC specific controls are considered, as well as the typical upper level VSC controls.

The accuracy of the proposed method is validated through EMTP simulations of 101-level and 401-level MMC-HVDC test systems using DEM and AEM of MMC. Lack of initialization caused large initial transients that took more than 0.5 s of simulation time to decay. Simulation results also demonstrated that elimination of the initial transient can be achieved only with an initialization approach that considers zero-, first-, and second-order harmonics in the MMC. The equal initial SM voltage assumption causes a short initial transient in the simulations. Despite its marginal impact outside the converter, the SM capacitor voltages should be initialized considering capacitor balancing algorithm to perfect initialization. The presence of delays between the solutions of power and control system equations can also cause extraneous transients which can be eliminated using extrapolation. The computing time to perform initialization calculations is negligible compared to the time needed to converge to steady-state solution without initialization.

CHAPTER 4 ADAPTIVE MODULAR MULTILEVEL CONVERTER MODEL

EMT simulation studies of power systems can provide accurate results over a wide frequency range, especially if small time-steps are used. However, during time-domain simulations there can be periods when internal details of all elements in the system are not necessary. This can be the case during the initialization transient or during slow electromechanical transients, when accurate representation of external behavior is sufficient [168, 169]. Such periods can be used to accelerate simulation by dynamically changing detailed models to simpler ones. However, the application of such approach, especially to MMC models, has been limited in EMT simulations: in [170] it is proposed to interface transient stability simulations in phasor domain with time-domain simulation of MMCs. In [171], AVM is used in shifted-frequency analysis with variable time-step. Hybrid simulation with EMT-type and transient stability-type software is discussed in [172]. In [173], it is proposed to switch between half-bridge AEM and DEM. However, the authors did not take into consideration neither full-bridge nor hybrid MMCs. The AVM has also been neglected even though it can further accelerate simulations, as will be shown in this chapter.

This chapter presents an adaptive model of hybrid modular multilevel converters for time-domain EMT simulations. The adaptive model comprises three constituting models with different levels of details: AVM, AEM, and DEM and allows for seamless transitions between them, including corresponding control systems. Such approach provides in the same time a high level of accuracy and lower computing times in time-domain simulations. Two novel arm AVMs are proposed to achieve identical electrical interface for all three constituting models and thus to facilitate transitioning between them. An AVM activation scheme is proposed, which automatically detects the conditions suitable for the AVM activation. A memory pointer exchange scheme for the DEM is proposed, which allows to send hundreds of control signals between the DEM and CBA DLLs without soliciting the generic control solver of the EMT simulation software, which allows to reduce computational burden and accelerate simulations. The proposed adaptive model is applicable to half-bridge, full-bridge, and hybrid MMCs with arbitrary proportions of half-bridge SMs.

4.1 Overview of the adaptive MMC model

4.1.1 Electrical circuit

The schematic diagram of the proposed adaptive model is shown in Figure 4.1. All three constituting model blocks are connected in parallel in each arm but only one is active at any given point in time. The active model recalculates its Norton equivalent at each time-point whereas the two inactive models supply zero equivalent admittance and current between their nodes. Each white block in Figure 4.1 can be implemented in a DLL to facilitate activation/deactivation procedures. Activation of any constituting model requires the activation of the appropriate control system blocks (discussed in the next section).

To facilitate the process of switching between the constituting models, all of them must have identical electrical interface, i.e. be connected to the same nodes. In the DEM and AEM, each arm is interfaced with the network using a two-port equivalent circuit whereas the DM and AVM have significantly different structures: the DM has all its internal nodes available to the solver and the AVM has separate AC and DC circuits [119]. Since DM applications in grid studies are limited [89], it is not included in the proposed adaptive MMC model. The AVM can be used for electromechanical studies, so it is amended to match DEM and AEM interfaces (see section 4.2).

4.1.2 Control system

The control system of the adaptive MMC model shown in Figure 4.2 is based on the generic cascade control system [120] and includes standard control functions, such as the outer power/voltage control, inner current control, circulating current suppression control, capacitor balancing algorithm, and nearest level control for more detailed models. The part of the control system that is common to all models is always kept active. It includes the PLL for grid synchronization and the outer control loop. Other blocks in the control system are activated and deactivated at runtime depending on the selected model.

The outer loop generates AC side current references i_{ref}^{AC} that are used by the inner current control loops. It is supposed that the AVM is used in balanced grid conditions, therefore, PI regulators in the positive d-q frame producing AC side EMF references e_{ref}^{AC} are considered for the AVM. The AEM and DEM can be used during grid unbalance, so inner control must also consider the negative

sequence and therefore is based on the PR regulators in α-β frame. With the AEM and DEM, the outputs of the inner control loop are the fundamentals of the arm switching functions s_1.

Additionally, the AEM and DEM require circulating current suppression that supplies the second harmonics of the arm switching functions s_2 and the NLC block that calculates the number of SMs to insert at each time-point n_{ref}. The DEM requires individual SM-level control and CBA to generate gating signals $\boldsymbol{S}_j$ for IGBTs based on n_{ref} and capacitor voltages $\boldsymbol{V}_{\boldsymbol{SM\,j}}$ (j is SM index).

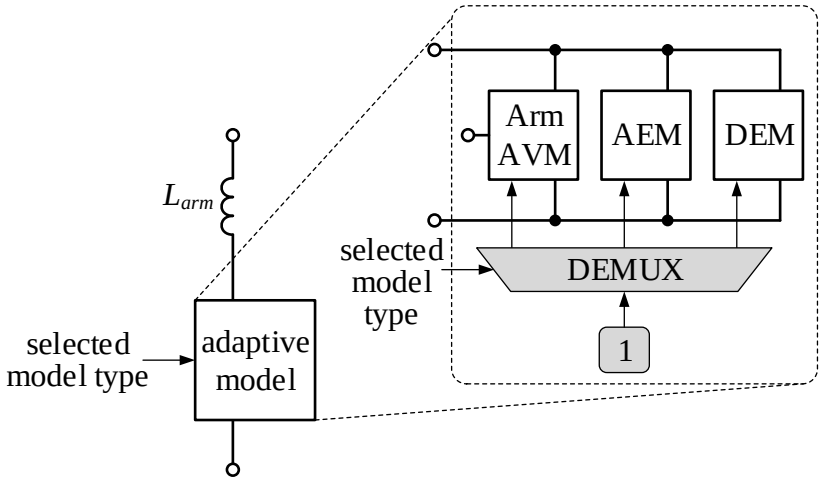


Figure 4.1 Schematic diagram of a single MMC arm with the adaptive model

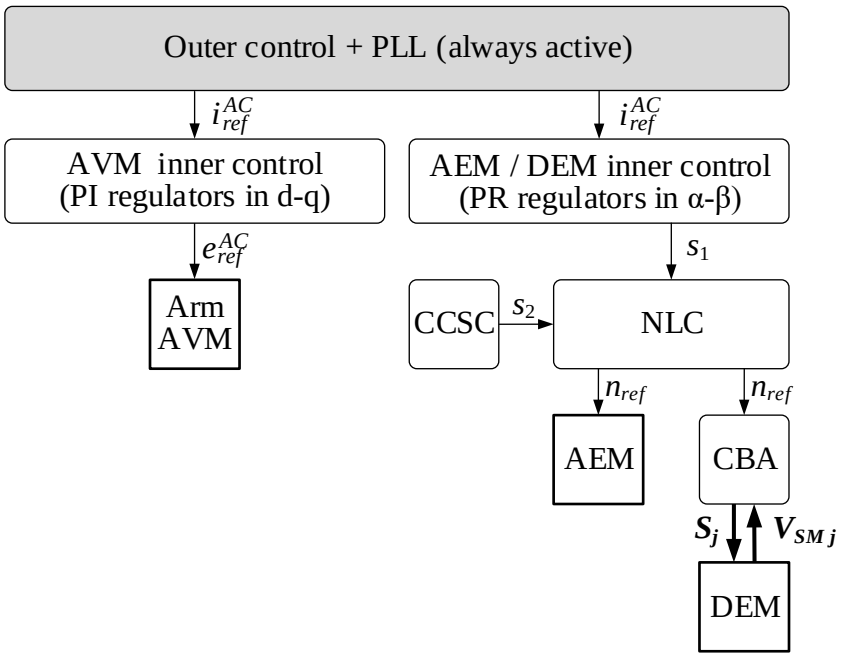


Figure 4.2 Control system of the adaptive MMC model

4.2 AVM

The conventional AVM consists of two electrical circuits disconnected from each other: three-phase AC and single-phase DC equivalent circuit (see Figure 2.11), which constitutes a major topological difference from more detailed models, where AC and DC sides are interleaved. To reduce the differences between the AVM and other models, two novel AVMs are proposed in this section. In these AVMs, arm inductances L_{arm} are preserved in their original places, to facilitate switching to and from more detailed constituting MMC models.

Two AVMs are proposed because two options exist regarding the arm inductor position in the converter: the inductors can be connected either to the DC bus, as in [174, 175], in which case the chains of SMs are connected to the AC bus. Otherwise, arm inductances can be connected to the AC bus, as in [160, 166] and SM chains are connected to the DC bus. The proposed AVMs are suitable for normal operation mode and the blocked mode is not included because the AVM is known to be inaccurate in this operation mode [119]. If blocked mode has to be activated with the AVM, it is proposed instead to switch to the AEM and then activate the blocked mode.

4.2.1 Arm-AVM-1

The Arm-AVM-1 is used when arm inductances are connected to the DC bus. Each arm of the Arm-AVM-1 consists of two branches: main branch for the AC current and auxiliary branch for the DC current. The auxiliary branch represents the DC side of the conventional AVM [119] and includes a current source, a capacitor $C_{arm-AVM}$, and a resistor R_{arm} to represent semiconductor conduction losses. The value of the arm AVM capacitor $C_{arm-AVM}$ can be found using energy conservation principle [120]:

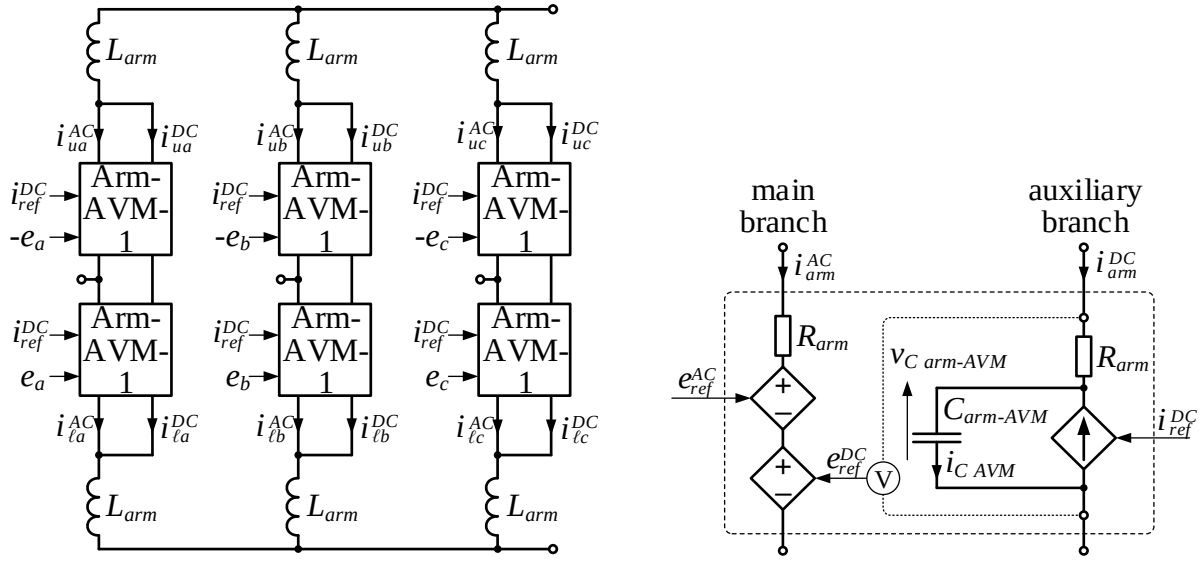
$$C_{arm-AVM} = 4\,C_{SM} / N_{SM} \tag{4.1}$$

The current reference i_{ref}^{DC} in the auxiliary branch is identical for all six arms and is obtained using the power balance principle so that the power generated at the AC side matches the power consumed at the DC side:

$$i_{ref}^{DC} = \frac{e_a\, i_a + e_b\, i_b + e_c\, i_c}{\sum_k v_{C\,arm-AVM\,k}} = \frac{e_a\, i_a + e_b\, i_b + e_c\, i_c}{6\, v_{C\,arm-AVM}} \tag{4.2}$$

where $v_{C\,arm-AVM}$ is the voltage across $C_{arm-AVM}$ (supposed to be identical in all six arms), and $k = 1...6$ is the arm index.

The main branch is composed of the arm resistance R_{arm} and two controlled voltage sources: the DC EMF reference e_{ref}^{DC} is measured in the auxiliary branch and is used to divert the DC component of the arm current to the auxiliary branch. The AC EMF references e_{ref}^{AC} are provided by the control system (see Figure 4.2). They have 180° phase-shift in the upper and lower arms of each phase. Arm-AVM-1 diagram is shown in Figure 4.3.

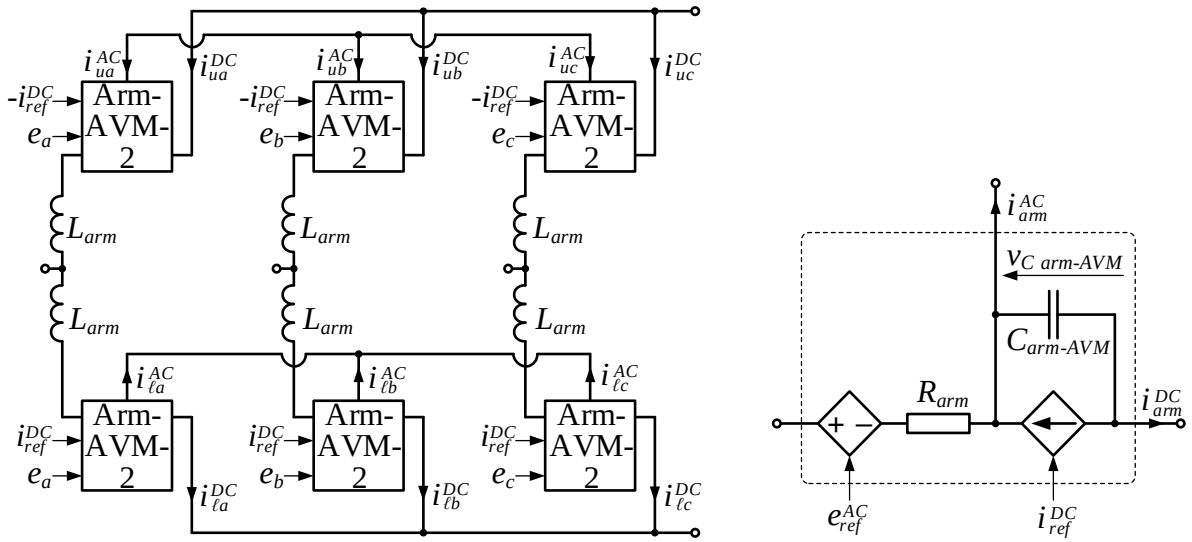


a) connection diagram b) internal structure

Figure 4.3 Arm-AVM-1

4.2.2 Arm-AVM-2

The Arm-AVM-2 is used when the arm inductances are connected to the AC terminals of the MMC. Compared to the Arm-AVM-1, this model consists of fewer elements and the connections are different, as shown in Figure 4.4. Equation (4.1) is still valid but the DC current references i_{ref}^{DC} are different: the reference signal for lower arms is provided by (4.2) and the reference for the upper arms has a negative sign $-i_{ref}^{DC}$. Upper and lower arms of each phase use the same AC EMF reference.



a) connection diagram b) internal structure

Figure 4.4 Arm-AVM-2

4.2.3 Estimation of voltage and current phasors

As it will be shown in section 4.5, it is necessary to know the instantaneous total capacitor voltage v_{Ctot} (i.e. sum of all SM voltages per arm) and arm switching function s signals to activate other MMC models and to initialize appropriate inner control loop. Since these variables are not available in the arm AVMs, it is proposed to use the iterative algorithm presented in Chapter 3 (Figure 3.2) based on the values of arm current and voltage phasors ($I_0, \bar{I}_1, V_0, \bar{V}_1$) to obtain them.

While the DC components for the algorithm are readily available in both arm AVMs ($I_0 = i_{arm}^{DC}$, $V_0 = v_{C\,AVM}$), fundamental frequency AC phasors $\bar{I}_1 = I_1 \angle \varphi_I$ and $\bar{V}_1 = V_1 \angle \varphi_V$ are estimated from two adjacent time-points assuming balanced steady-state conditions. For the AC current phasor:

$$\begin{cases} i_{arm}^{AC}\left(t-\Delta t\right) = I_1 \cos\left(\omega\left[t-\Delta t\right]+\varphi_I\right) \\ i_{arm}^{AC}\left(t\right) = I_1 \cos\left(\omega t+\varphi_I\right) \end{cases} \tag{4.3}$$

By defining $i_x = i_{arm}^{AC}\left(t-\Delta t\right)$, $i_y = i_{arm}^{AC}\left(t\right)$ and applying trigonometric sum and product formulas, fundamental current phasor amplitude and phase angle are obtained as

$$I_1 = \sqrt{\left[i_x / \sin\left(\omega \Delta t\right) - i_y \cot\left(\omega \Delta t\right) \right]^2 + i_y^2} \tag{4.4}$$

$$\varphi_I = \text{atan2}\left(i_x / \sin\left(\omega \Delta t\right) - i_y \cot\left(\omega \Delta t\right), i_y \right) \tag{4.5}$$

In a similar manner, the AC voltage phasor $\bar{V}_1$ is obtained:

$$\begin{cases} e_{ref}^{AC}\left(t - \Delta t\right) = V_1 \cos\left(\omega\left[t - \Delta t\right] + \varphi_V\right) \\ e_{ref}^{AC}\left(t\right) = V_1 \cos\left(\omega t + \varphi_V\right) \end{cases} \tag{4.6}$$

$$V_1 = \sqrt{\left[v_x / \sin\left(\omega \Delta t\right) - v_y \cot\left(\omega \Delta t\right) \right]^2 + v_y^2} \tag{4.7}$$

$$\varphi_V = \text{atan2}\left(v_x / \sin\left(\omega \Delta t\right) - v_y \cot\left(\omega \Delta t\right), v_y \right) \tag{4.8}$$

where $v_x = e_{ref}^{AC}\left(t - \Delta t\right)$ and $v_y = e_{ref}^{AC}\left(t\right)$.

Afterwards, using currents and voltages $I_0, \bar{I}_1, V_0, \bar{V}_1$, the iterative algorithm from Chapter 3 (Figure 3.2) yields the total capacitor voltage and arm switching function harmonics. The instantaneous values are then obtained as

$$v_{Ctot} = v_{Ctot\,0} + v_{Ctot\,1} + v_{Ctot\,2} \tag{4.9}$$

$$s_{arm} = s_0 + s_1 + s_2 \tag{4.10}$$

4.3 AEM

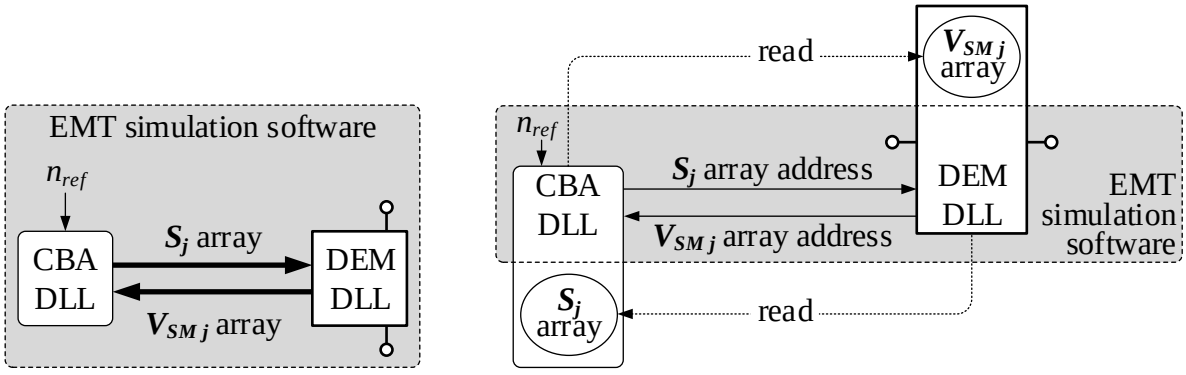
The Hybrid-AEM from Chapter 2 is used. It is composed of two circuits (representing HB and FB parts, respectively) to provide the hybrid functionality.

4.4 DEM

Each SM in the DEM requires at least one input (IGBT gating signal) and provides at least one output (capacitor voltage). The total number of control signals is therefore significant and can be in the order of thousands for each MMC station, which results in long simulation times [174]. Thousands of control signals exchanged between CBA and DEM blocks in the EMT simulation

software (see Figure 4.5.a) significantly increase the size of the control system equations matrix which is solved using a generic control system solver.

To reduce the number of control signals managed by the EMT software, it is proposed to implement CBA and DEM as DLLs, which allows them to read control signals directly from the memory without soliciting the generic solver. This translates into faster simulations. In this case, the DLLs exchange the addresses (pointers) of $\boldsymbol{S_j}$ and $\boldsymbol{V_{SM\,j}}$ arrays through the EMT software as shown in Figure 4.5.b.



a) Standard signal exchange b) Proposed memory pointer exchange

Figure 4.5 Signal exchange scheme between DEM and CBA DLLs

Other than being useful for acceleration, such memory pointer exchange also allows easily changing CBA DLLs at any time during simulation, it is only needed to change the address of the CBA DLL shared memory supplied to the DEM DLL. An example in Figure 4.7 shows two CBA blocks (one can be voltage sorting-based and the other can be permutation-based) that can be interchangeably used in the simulation with the same DEM.

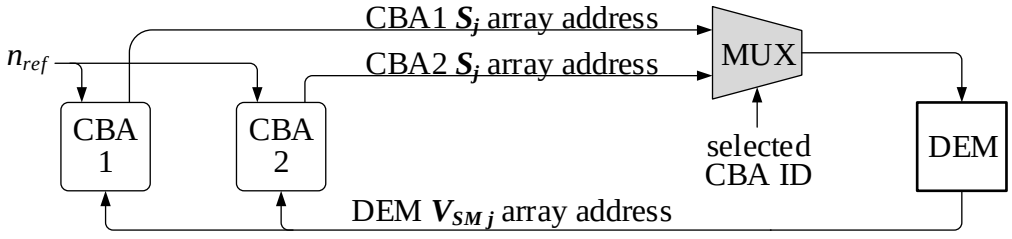


Figure 4.6 Sample setup for switching between different CBA blocks

4.5 Activation of MMC models

Methods of time-domain activation are developed in this section. These methods allow smoothly transitioning from one constituting MMC model to another in any order: AVM to AEM or DEM; AEM to AVM or DEM; DEM to AVM or AEM. It is the user who decides when to activate one or the other depending on the objectives of the simulation study but generally it can be advised that a more detailed model should be activated some moments before a disturbance is applied. It should also be noted that blocked mode in the proposed adaptive model is only available in the AEM and DEM parts, so the AVM cannot be active when the converter must be blocked.

4.5.1 AVM activation

Both arm AVMs proposed in this chapter are based on electrical circuits with similar elements and therefore are activated in a similar manner.

The only internal variable that needs initialization is the capacitor voltage $v_{C_{AVM}}$. To find its value, it is supposed that the MMC is at quasi steady-state operation and arm currents and voltages are balanced. In such conditions, there is no current passing through the capacitor $C_{arm-AVM}$, therefore its voltage can be found using DC current i_{DC} and voltage v_{DC}:

$$i_{arm}^{DC} = i_{DC} / 3 \tag{4.11}$$

$$v_{C_{AVM}} = v_{DC} / 2 - R_{arm}\, i_{arm}^{DC} \tag{4.12}$$

4.5.1.1 Automated AVM activation

Automated AVM activation method is proposed to facilitate model selection process, based on the fact that less detailed models can be used at steady-state conditions whereas more detailed models are required for faster transients. The method is based on the analysis of grid frequency f_{PLL} provided by the PLL and DC voltage v_{DC} signals. When the sum of the instantaneous deviations (denoted as ε_{Σ}) from the respective moving average values for both signals is below a threshold ε_{MAX} (4.16) for a sufficient period of time (denoted as t_{latch}), the simulation is considered to be at quasi steady-state and therefore the AVM can be activated. More detailed models must be activated manually. Error signals are defined as

$$\varepsilon_f = \left| f_{PLL} - f_0 \right| / F_{nom} \tag{4.13}$$

$$\varepsilon_v = \left| v_{DC} - v_{DC\,0} \right| / V_{DC\,nom} \tag{4.14}$$

$$\varepsilon_\Sigma = \varepsilon_f + \varepsilon_v \tag{4.15}$$

$$\varepsilon_\Sigma < \varepsilon_{MAX} \tag{4.16}$$

where ε_f and ε_v are the error signals for the frequency and DC voltage, respectively; f_0 and $v_{DC\,0}$ are moving average grid frequency and DC voltage values, respectively; F_{nom} and $V_{DC\,nom}$ are nominal grid frequency and DC voltage, respectively; ε_{MAX} is maximal tolerable error.

The moving average window duration T_0 for f_0 and $v_{DC\,0}$ used in this automated activation scheme is 0.1 s. The AVM activation circuit is shown in Figure 4.7.

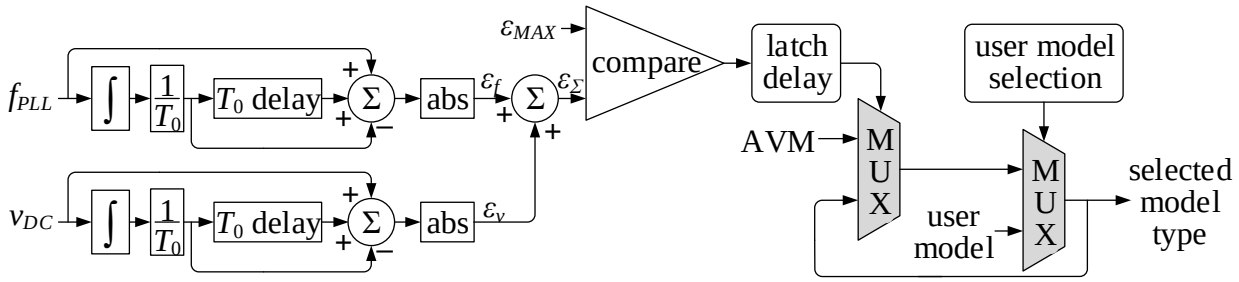


Figure 4.7 Automated AVM activation diagram

4.5.2 AEM activation

To activate the Hybrid-AEM, history voltage values for the HB (2.44) and FB parts (2.45) are required. They can be found using the values of HB- and FB-SM voltages, arm current, and the number of SMs to insert. All these variables are already available in the DEM where HB and FB branch voltages can be obtained by averaging individual SM voltages, the number of SMs to insert is provided by the inner control, and the arm current is measured directly. Therefore, no additional calculations are required when DEM $\rightarrow$ AEM switching occurs.

However, if AVM $\rightarrow$ AEM switching is considered, neither capacitor voltages nor the number of SMs to insert is available in advance. Therefore, it is proposed that arm AVMs provide these values

using the iterative algorithm, as explained in the subsection 4.2.3. HB and FB voltages and the number of SMs to insert are then obtained using (4.9) and (4.10) as

$$v_{HB} = v_{FB} = v_{Ctot} / N_{SM} \tag{4.17}$$

$$n_{ref} = \text{round}(s_{arm}\ N_{SM}) \tag{4.18}$$

4.5.3 DEM activation

Individual history voltages for each SM are necessary to activate the DEM. However, AEM and AVMs can only provide the average value of capacitor voltages. If all SM voltages are set to the same average value similarly to (4.17), activation procedure is identical to that of the AEM in the previous subsection 4.5.2. In this case, a short transient after switching to the DEM will appear.

Another solution is estimating SM voltages. In this case, the initial transient can be minimized. Rigorously estimating individual SM voltages can become difficult because their values depend on the type of CBA and may require the knowledge of additional variables. If permutation CBA is considered, SM voltages are uniformly distributed around the average value. Therefore, it is proposed in this thesis to simplify (3.67) derived in Chapter 3 by neglecting the effects of SM insertion on voltage balancing:

$$v_{SM\ j} = \frac{v_{Ctot}}{N_{SM}} + \left[\frac{j-1}{N_{SM}-1} - \frac{1}{2}\right] i_{arm}\ s_{arm}\ \frac{\Delta t\ N_{SM}}{N_0\ C_{SM}} \left[1 - s_{arm}\right] \tag{4.19}$$

4.6 Activation of controls

4.6.1 AVM inner control

In this chapter, arm AVMs are supposed to operate in balanced conditions, so conventional PI controllers in positive d-q frame is considered. In Chapter 3, initialization of PI inner control has been discussed for AEM and DEM, but contrary to that, in this chapter current control loop for arm AVMs produces AC EMF references and not arm switching functions. So, integral history terms for d (H_d) and q (H_q) axes are obtained differently:

$$H_{1d}^{+} = v_{PCC\,d} - e_d + L_{\Sigma}\ \omega\, i_q \tag{4.20}$$

$$H_{1q}^{+} = v_{PCC\,q} - e_q - L_{\Sigma}\,\omega\, i_d \tag{4.21}$$

where e_d, e_q, i_d, i_q are the AC side EMFs and currents in d-q reference frame, respectively.

Projections on d and q axes are obtained by applying Park transformation to three-phase signals: AC side currents are directly available, and AC side EMFs can be obtained as

$$e_m^{AC} = \left[v_{m\ell} - v_{mu} \right] / 2 - R_{arm}\, i_m / 2 \tag{4.22}$$

where $m = a, b, c$ is phase index

4.6.2 AEM / DEM inner control

Control based on PR regulators is used with the AEM and DEM because it can handle positive and negative sequence currents in the same time [134]. Double integral circuit implementation proposed in Chapter 3 (see Figure 3.4) is taken.

AEM / DEM inner control is activated after AVM has been active. Since AVM is used in balanced grid conditions, only the positive sequence of the first harmonic arm switching functions are considered for initialization. Integral history terms for alpha $H1_{1\alpha}$, $H2_{1\alpha}$ and beta $H1_{1\beta}$, $H2_{1\beta}$ channels (as shown in Figure 3.4) are

$$H1_{1\alpha} = v_{PCC\,\alpha} - s_{1\alpha} \tag{4.23}$$

$$H2_{1\alpha} = \omega \left[v_{PCC\,\beta} - s_{1\beta} \right] \tag{4.24}$$

$$H1_{1\beta} = v_{PCC\,\beta} - s_{1\beta} \tag{4.25}$$

$$H2_{1\beta} = -\omega \left[v_{PCC\,\alpha} - s_{1\alpha} \right] \tag{4.26}$$

where $v_{PCC\,\alpha}$ and $v_{PCC\,\beta}$ are PCC voltages in α-β frame, $s_{1\alpha}$ and $s_{1\beta}$ arm switching function first harmonics in α-β frame.

Variables $v_{PCC\,\alpha}$, $v_{PCC\,\beta}$, $s_{1\alpha}$, and $s_{1\beta}$ can be obtained by applying Clarke transformation to three-phase signals. For CCSC, second harmonic terms of the arm switching function s_2 must be taken, the activation procedure is similar to (4.23)–(4.26).

4.6.3 CBA

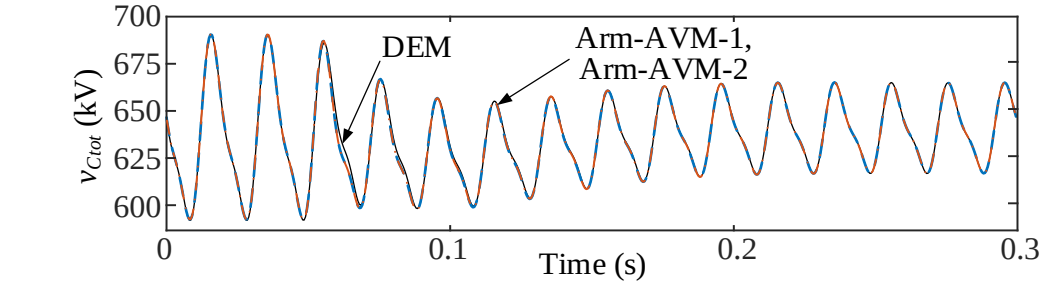
Voltage sorting CBA and permutation-based CBA are considered in this chapter. They do not have history terms, therefore only the initial selection of SMs must be calculated during activation. Uniform SM insertion indices are applied.

4.7 Simulation results

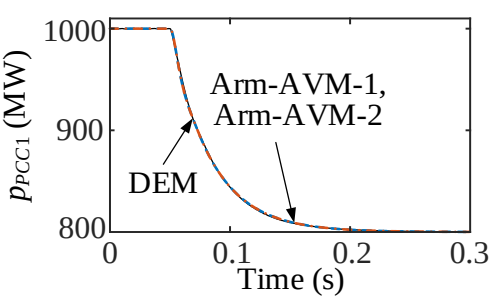
The proposed adaptive MMC model is implemented in EMTP [83]. Simulations used the point-to-point HVDC link presented in the Appendix B.

4.7.1 Validation of arm AVMs

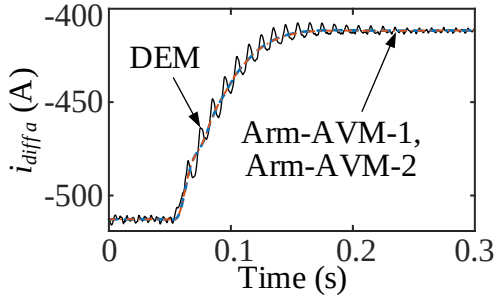
Both arm AVMs are validated against the DEM in Figure 4.8. At first, 50% active power step is applied to MMC1. Results obtained with both arm AVMs closely match the reference except the slight difference observed in the total capacitor voltage v_{Ctot} in the beginning of the disturbance (Figure 4.8.a) and 100 Hz ripple in difference current $i_{diff\,a} = \left(i_{u\,a} + i_{\ell\,a}\right)/2$ (Figure 4.8.c) that can be associated with the circulating current control that is not available in the arm AVMs.



a) total capacitor voltage



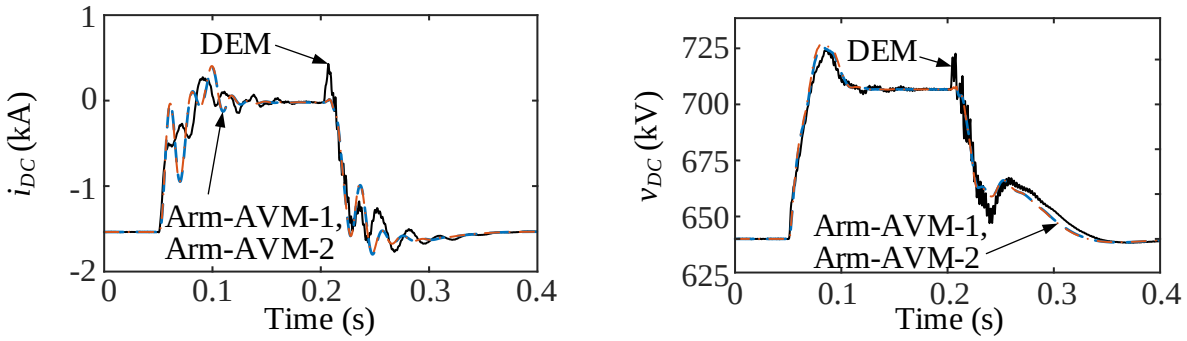
b) PCC1 active power



c) phase A difference current

Figure 4.8 Arm AVM validation: power reference step

To validate the large transient behavior of the arm AVMs, a 150 ms 3-phase AC fault is applied at PCC2. Results are shown in Figure 4.9. Higher frequency transients in DC current and voltage are not well represented with arm AVMs, but a reasonable match is obtained considering lower-frequency transients and steady-state conditions.



a) DC current b) DC voltage

Figure 4.9 Arm AVM validation: AC fault

4.7.2 Validation of DEM memory pointer exchange

To validate the memory pointer exchange approach, switching between two different CBA algorithms is tested: permutation-based (CBA 1) and voltage sorting-based (CBA 2) with 50 µs period (see Chapter 2, section 2.5.8.2). The address of $\boldsymbol{S}_j$ array provided by the CBA blocks is changed during runtime (see configuration in Figure 4.6). Figure 4.10 shows voltages of 10 SMs in phase A upper arm of MMC 1 when switching from the permutation-based CBA to the voltage sorting-based one at $t = 30$ ms. It takes CBA 2 about 5 ms to considerably reduce differences in individual SM voltages. The validity of the memory pointer exchange approach is validated.

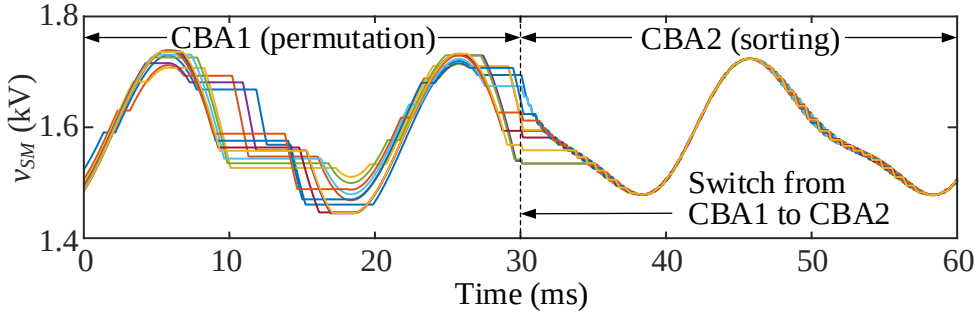


Figure 4.10 Memory pointer exchange validation

4.7.3 Computing times

The HVDC link is simulated in normal operation mode for 1 s and computing times with different constituting models are shown in Table 4.1 and Figure 4.11 depending on the number of SMs.

Models that do not represent SM-level details have constant computing time. Computing time of the DEM depends linearly on the number of SMs in case of permutation-based CBA and quadratically in case of voltage sorting-based CBA. Memory pointer exchange saves 15%–20% of simulation time with permutation CBA. Acceleration factors therefore depend on the number of SMs and can reach 20 if voltage sorting CBA is applied to MMCs with high number of levels.

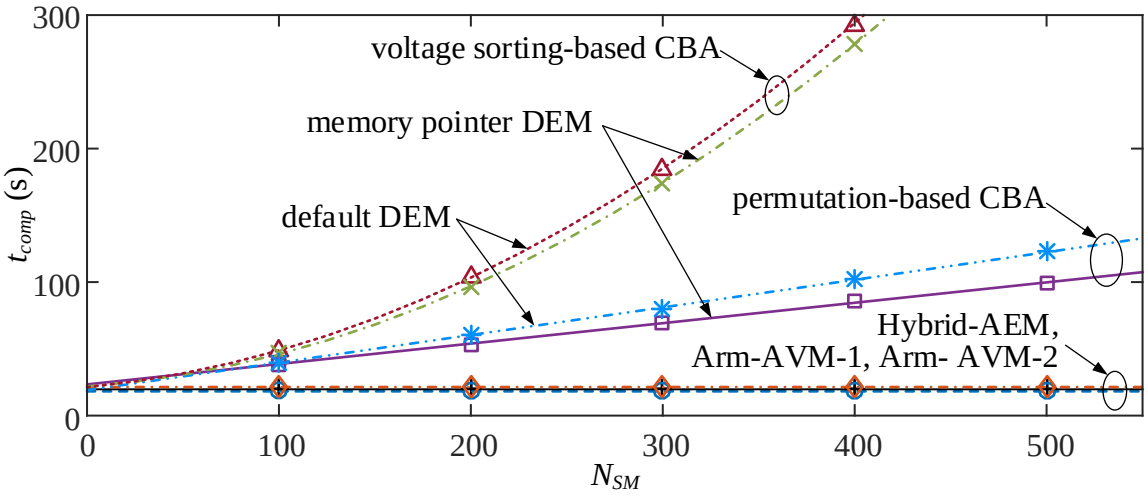


Figure 4.11 Computing times with different constituting models

Table 4.1 Computing times with different constituting models (s)

N_{SM}	Arm-AVM-1	Arm-AVM-2	AEM	Permutation-based CBA		Voltage sorting-based CBA	
				Memory pointer DEM	Default DEM	Memory pointer DEM	Default DEM
100	18.04	19.56	21.31	38.51	40.05	46.31	48.44
200	18.27	19.73	21.49	53.68	60.23	96.44	104.12
300	18.16	19.69	21.31	69.29	80.55	174.12	184.87
400	18.12	19.73	21.44	85.65	101.71	278.59	293.57
500	18.19	19.69	21.51	98.96	122.70	408.26	430.28

4.7.4 DC fault

A DC fault is applied in the middle of the DC cable at $t = 0.5\,\text{s}$. The converters are blocked shortly after, when the DC current reaches the value of 5 p.u. at each station. With the adaptive model, the Arm-AVM-2 is used during initialization transient and the DEM is activated with the voltage sorting-based CBA around the time of the fault from 0.495 s to 0.505 s to study SM voltages. AEM is activated next until 0.6 s (i.e. until the end of the simulation) because arm AVMs cannot be used during blocked mode.

Simulation results show a close match between the adaptive model and the DEM-only reference: DC voltage in Figure 4.12 obtained with the adaptive model is identical to the one obtained using the DEM-only reference. The voltages of 14 uniformly selected SMs in Figure 4.13 demonstrate that even at the SM level the adaptive model replicates well the DEM. It can be observed that HB- and FB-SMs behave differently after the fault: HB-SM voltages stay constant after blocked mode is activated at $t = 0.5007\,\text{s}$ whereas FB-SM voltages start charging. Arm current during this period is negative, which causes HB-SMs to be naturally bypassed whereas FB-SMs are still able to let the arm current flow in any direction. As soon as the arm current reaches zero, the charging process stops, and all SMs are in the high impedance mode, so the voltages keep constant values.

It can be seen that the transitions between the models are smooth and work well in both normal operation and blocked mode. CPU time for 0.6 s of simulation with DEM-only is 167 s whereas with the adaptive model it is only 16.8 s, yielding 9.9 acceleration factor.

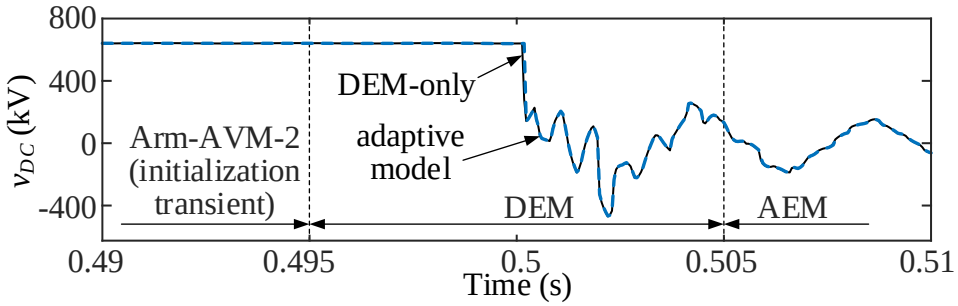
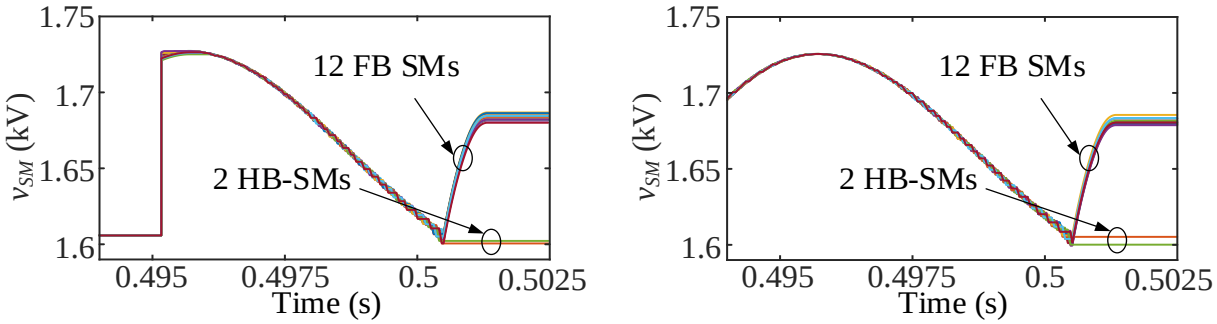


Figure 4.12 DC voltage at MMC 1 terminals during a DC fault



a) adaptive model b) DEM-only

Figure 4.13 SM voltages in phase A upper arm at MMC 1 during a DC fault

4.7.5 Small-scale AC grid

The small-scale AC grid developed from the system presented in [167] shown in Figure 3.17 is used. A 3-phase fault occurs at $t = 2\,\text{s}$ when the system reaches steady-state. The fault is cleared with a 100 ms delay by tripping the line between ALIAG and SOMA buses. The simulation is performed with the proposed adaptive model and using only DEM with a permutation-based CBA, which serves a reference. The switching instants of the proposed adaptive model are as follows (Figure 4.14): the Arm-AEM-2 is used during initialization. The DEM is activated at $t_1 = 1.95\,s$ to study the SM voltages in the first instants of the fault. AEM is activated at $t_2 = 2.05\,s$ until the fast transient is over. At $t_3 = 2.44\,s$ the error signal ε_Σ (4.15) falls below maximal tolerable value $\varepsilon_{MAX} = 0.001$ and 0.15 s later at $t_4 = 4.59\,s$ the Arm-AVM-2 is automatically activated until the end of simulation.

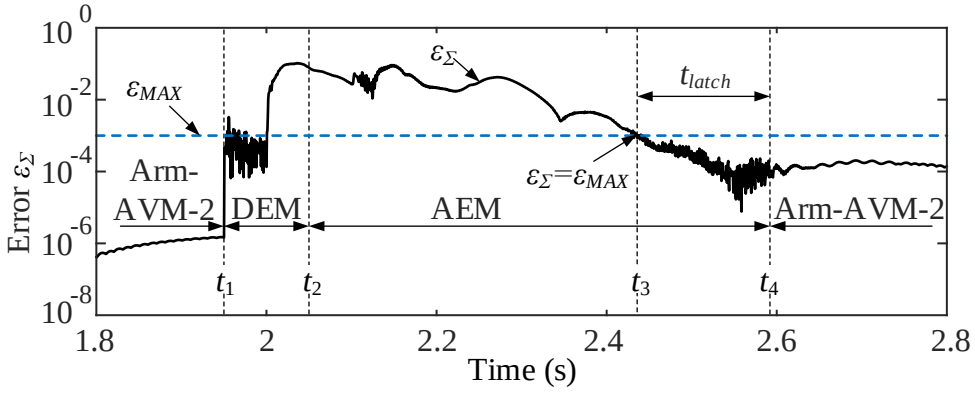
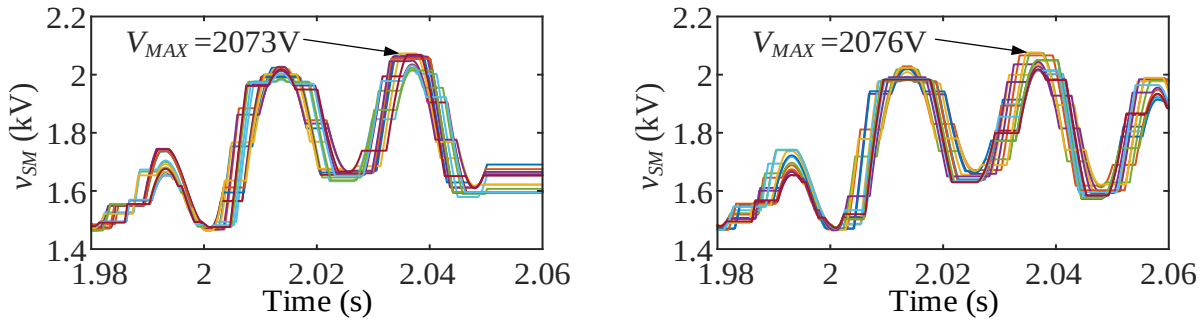


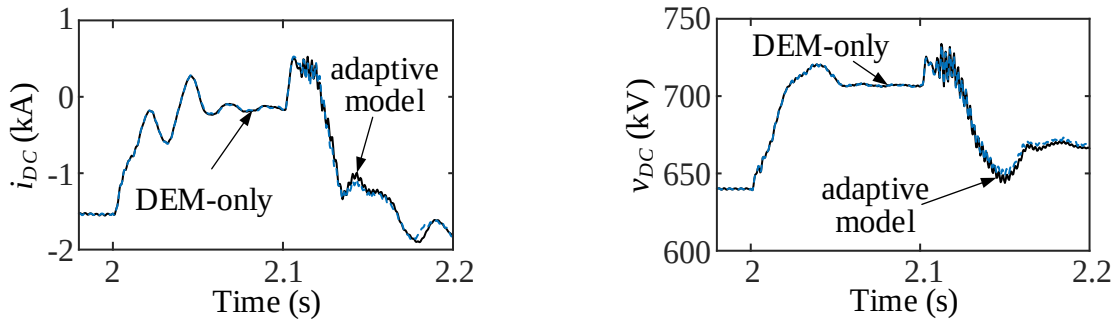
Figure 4.14 Error signal during a transient in a small-scale grid

The voltages of 14 uniformly selected SMs obtained with the adaptive model in Figure 4.15.a match the ones obtained using only DEM in Figure 4.15.b. The maximum SM voltage V_{MAX} in both cases has almost identical value. Fast transients in the DC current and voltage with the adaptive model are in good agreement when compared to the DEM-only usage in Figure 4.16. Considering slower transients in generator power, the waveform of the instantaneous three-phase power of the generator at the KEMER bus p_{KEMER} in Figure 4.17 obtained using the adaptive model also matches the DEM reference.



a) adaptive model b) DEM-only

Figure 4.15 SM voltages in phase B upper arm at MMC 2 during an AC fault



a) DC current b) DC voltage

Figure 4.16 DC current and voltage during an AC fault

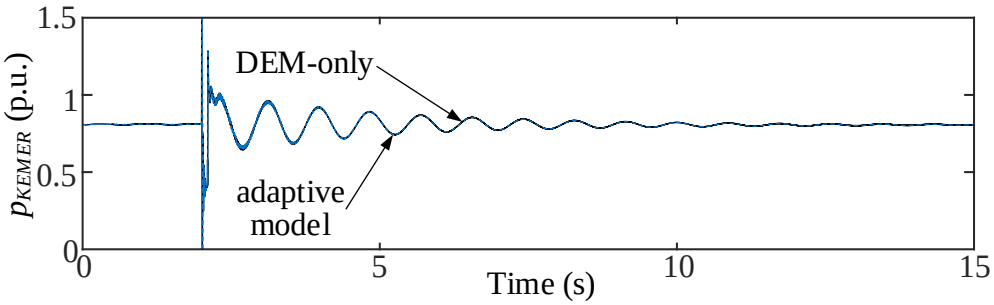


Figure 4.17 Active power at KEMER TPP during a transient in the small-scale grid

The computing time of the performed study using only DEM is 1762 s (for 15 s of simulation time) whereas the proposed model takes 504 s, which results in an acceleration factor of 3.5.

4.8 Conclusion

The arm AVMs developed in this chapter allow to significantly reduce simulation time, compared to the DEM. In steady-state and close-to-steady-state conditions, arm AVMs provide sufficient accuracy and the results are similar to those obtained using DEM-only reference, including capacitor voltages and arm switching functions. Faster transients, however, are not well represented with the arm AVMs. The memory pointer exchange proposed for the DEM is validated and allows seamlessly changing CBA blocks during simulation. Such memory exchange scheme can save up to 15%-20% of the computing time. In the performed transient simulations, the proposed adaptive model demonstrates a high degree of accuracy even at the SM level. Transitions between the constituting models are smooth and do not cause significant additional transients. Both the normal operation and blocked mode transitions are validated. Acceleration factors depend on the simulated grid parameters. In the performed tests, the acceleration factor of 9.9 has been achieved.

CHAPTER 5 PARALLELIZATION OF THE DETAILED EQUIVALENT MODEL

Modern advances in consumer electronics brought to market various types of computer architectures that allow to execute different pieces of code simultaneously instead of running them sequentially. Experience has shown that such parallel execution of code can result in a considerable reduction of computing time necessary to perform a given task. The parallelization can come in different forms and using different types of architectures: multicore CPUs [176], graphic processing units (GPU) [177], flexible parallel gate arrays (FPGA) [178], and others.

Numerous methods to parallelize the computations in the EMT-type simulations have been proposed in the literature. For example, transmission line modes that represent travelling wave phenomena provide a natural decoupling of the network into smaller regions, allowing to compute such subnetworks in parallel [179, 180]. Co-simulation methods has been developed that allow to interface different parts of the network simulated in parallel [181]. LU factorization, which is a common technique to solve matrix equations in the EMT-type software, can be parallelized on CPUs [182]. GPU parallelization has also been applied to the simulation of power grids [183-186], distribution networks [187, 188], and power electronic devices. FPGAs are often used to accelerate the simulations of power electronics-based circuits [189, 190].

This chapter discusses the parallelization of the DEM calculations in offline simulations. Among the conventional MMC models, the DEM is a good candidate for parallelization for the following reasons:

- Its complexity is relatively significant due to the large number of SMs that must be treated individually, which offers potentially significant time-gains.
- The nonlinearities in the DEM are not as complex as in the DM, which allows for a relatively easier implementation.
- The DEM is often implemented independently from the main EMT solver and is interfaced with it using an equivalent Norton or Thevenin circuit, which is also advantageous for an easier implementation.

- There are at least six DEM blocks per MMC, and in HVDC simulations there are usually at least two converters. The total number of DEM units N_{DEM} that can be parallelized is therefore at least 12.
- The CBA computations can also be parallelized.

Unlike GPUs and FPGAs, multicore CPUs are often available in modern day PCs and laptops. This allows to prioritize CPU-level parallelization of the EMT simulations over other types due to the larger availability of the appropriate hardware.

5.1 Procedure overview

The EMT simulation software considered in this chapter is EMTP [83], which is based on the request-participation interface with the constituting modules. The EMT core sends requests to the modules used in the simulation study one by one and they reply with the results of their internal calculations. The main requests of the EMTP during a single time-point computation with nonlinear elements such as the DEM are as follows:

- Request the contributions of the modules participating in the MNE matrix (admittances and history currents in case of the DEM).
- Solve the MNE.
- Check convergence. Repeat two previous steps in case of insufficient precision.
- Request the contributions of the modules participating in the control system equations.
- Solve the control system equations.
- Go to the next time-point.

In the default sequential execution case, the internal model calculations are performed one at a time for each arm when the EMT core requests them. The general idea researched in this chapter is that all internal calculations for all N_{DEM} DEM arm blocks can be performed at once in parallel at the beginning of the current time-point calculations and the next solicited DEMs will only retrieve the results of the calculations when requested by the EMT core, as shown in Figure 5.1.

Since the internal calculations of the DEM modules are performed in parallel, the time necessary to compute the results at the current time-point is reduced. Such approach has been applied to the real-time simulations [189] and its ability to accelerate offline simulations is evaluated here. The CBA parallelization is performed in a similar manner with the difference being that it only participates in the control system equations part and does not participate in the electrical circuit equations.

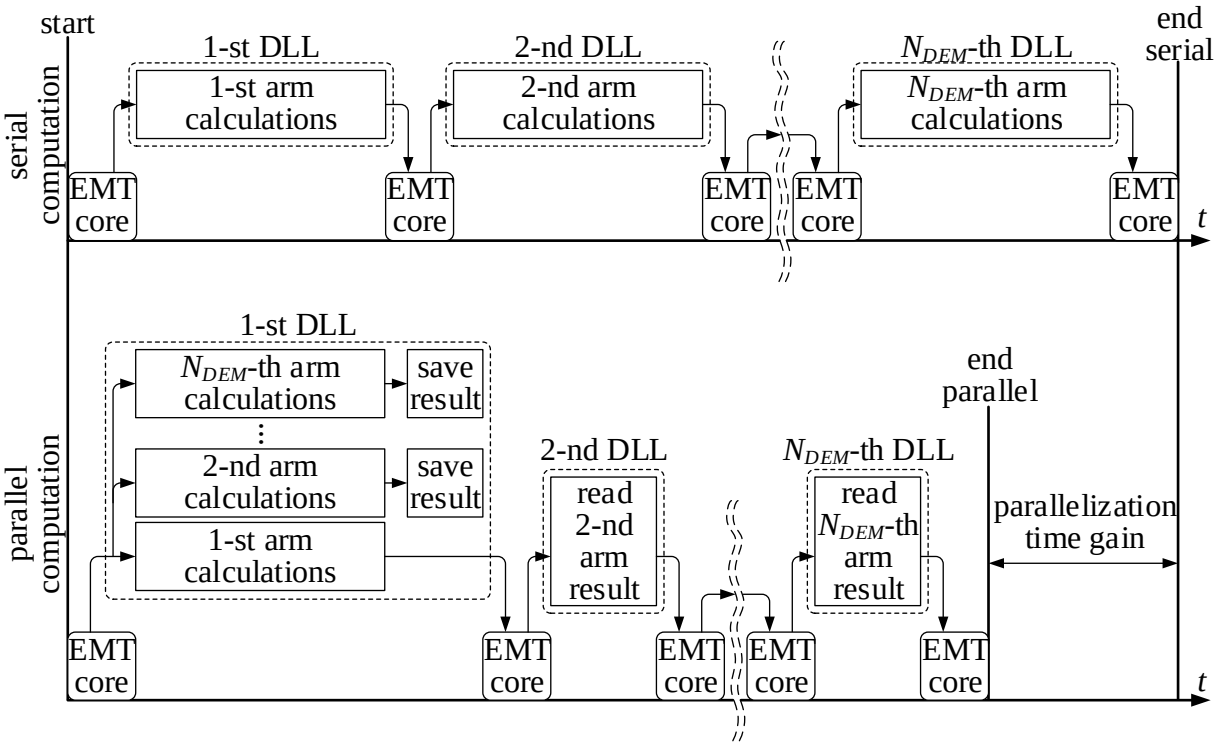


Figure 5.1 Overview of the proposed parallelization scheme

5.2 DEM parallelization

As explained in Chapter 2, section 2.2, each arm of the DEM is interfaced with the EMT core by using its Norton equivalent circuit. To calculate it, in the normal operation mode the DEM requires the IGBT control signals and the input voltage in the blocked mode. The Norton equivalent values supplied by the DEM DLLs to the EMT solver depend on the control and history values from the previous time-point, which means that they do not require iterations in most of the cases.

All internal functions of the DEM can be separated into the following groups:

- Input data acquisition of control and electrical signals (IGBT commands, input arm voltage). It can be performed in parallel because it is reading from memory.
- Internal model equations, which include updating history currents, grouping of SMs, calculating the Norton equivalent, updating capacitor voltage and current values. They only require local variables so can also be parallelized.
- Output data exchange, providing the Norton equivalent and control signals such as SM voltages to the EMT core. This has to be performed in series since calls to internal functions of the EMT core are used that cannot be guaranteed to be thread-safe.

The DEM is implemented as a DLL using Fortran-95 and the parallelization is performed using OpenMP provided by the Intel Fortran complier. Normal mode and blocked mode can be parallelized. Each DEM DLL executes the following algorithm for the MNE contribution and the control system, Figure 5.2.

To be able to study the impact of the number of threads on the acceleration, an additional grouping is added. The DLLs within the same group are launched in parallel. Each DLL group contains $n_{threads}$ DEM blocks and therefore requires $n_{threads}$ threads. Each DLL first checks if it is the first in the group and if so, launches all the DLLs' computations in parallel. To avoid multiple computations of the same data, the first DLL raises a special flag ("first DLL in the group") that indicates that the calculations of this group have been performed.

The DLLs must also check if they are the last one in the group to reset the "first DLL in the group" flag that has been raised by the DLL that performed the calculations in parallel so that at the next time-point the first DLL could be correctly assigned.

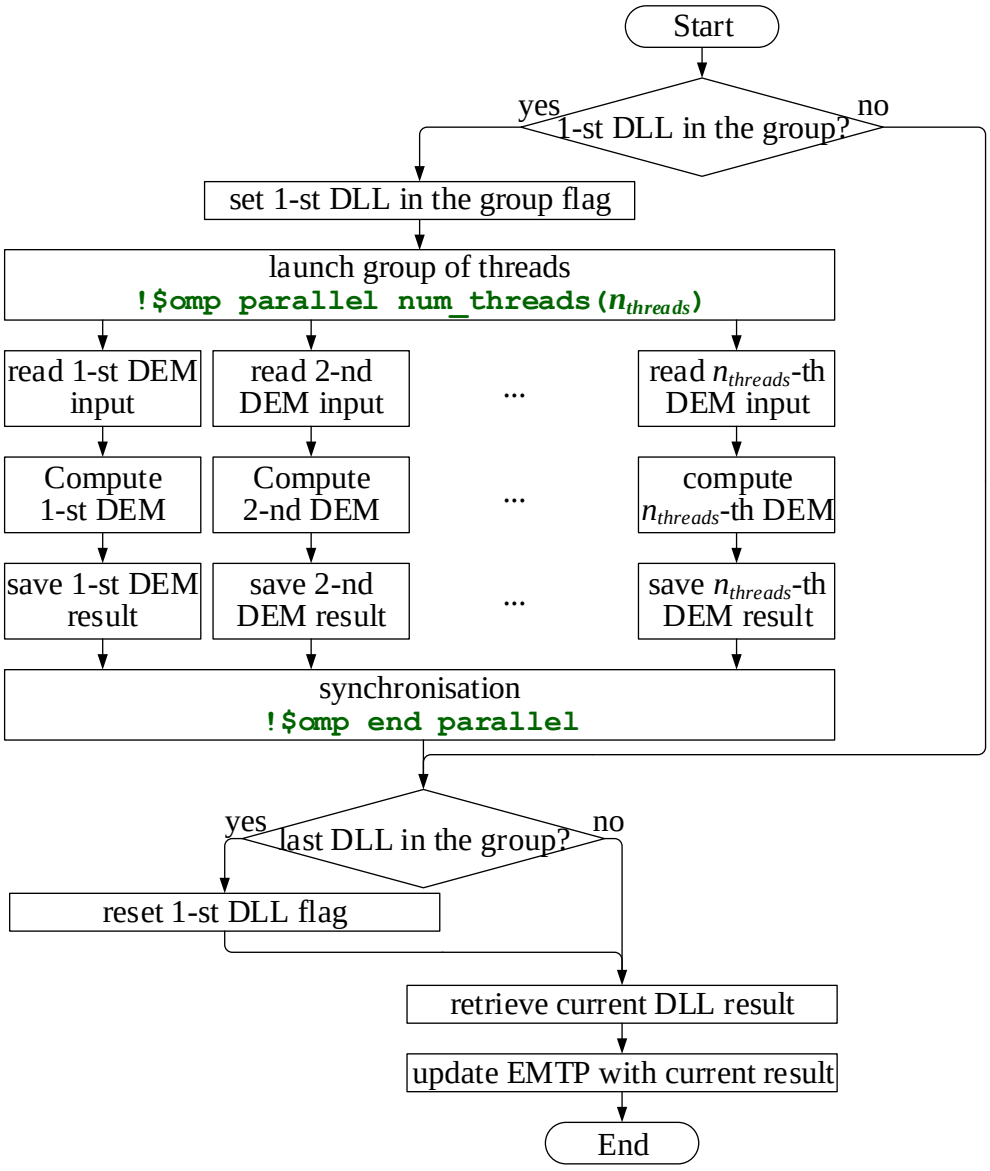


Figure 5.2 Implemented DEM parallelization algorithm

5.3 CBA parallelization

The CBA block deals only with control signals. As with the DEM, all internal functions of the CBA can be separated into the same groups:

- Input data acquisition (SM voltages, arm current). It can be performed in parallel because it is reading from memory.
- Internal model equations (sorting of SM voltages, selecting the SMs to insert and to bypass) require local variables and can also be parallelized.

- Output data exchange (final IGBT gating signals). Performed in series since it uses calls to the internal functions of the EMT core that cannot be guaranteed to be thread-safe.

The CBA is active during the normal operation and only provides blocking signals during the blocked mode. The same implementation as in Figure 5.2 is used with the only difference being that the DEMs are replaced by the CBAs in the parallel computations block.

5.4 Performance evaluation

The goal of the proposed DEM parallelization scheme is to reduce the time needed to perform simulations of MMC-HVDC systems. Therefore, the time gains must be evaluated. They are evaluated using the acceleration factor, which is found as

$$f_{acc} = \frac{t_{sequential}}{t_{parallel}} \tag{5.1}$$

where $t_{parallel}$ is the computational time with parallelization and $t_{sequential}$ is the computational time with the default single-threaded sequential implementation of the DEM.

In the first approximation, the single-threaded and the multithreaded computing times can be represented by the following formulas

$$t_{sequential} = T_0 + T_{DEM}\ N_{DEM} \tag{5.2}$$

$$t_{parallel} = T_0 + T_{DEM}\ \frac{N_{DEM}}{n_{threads}} \tag{5.3}$$

where T_0 is the time necessary to perform all sequential computations such as the resolution of the MNE, line and machine models, etc.; T_{DEM} is the time spent to compute one MMC arm.

Given that the number of DEM blocks in each group $n_{threads}$ is limited between 1 and N_{DEM}, f_{acc} is limited as well:

$$\min\left(f_{acc}\right) = 1 \tag{5.4}$$

$$\max\left(f_{acc}\right) = \frac{T_0 + T_{DEM}\ N_{DEM}}{T_0 + T_{DEM}} \tag{5.5}$$

If the time required to compute the DEM is large compared to the rest of the computations (i.e. $T_{DEM} \gg T_0$), the maximal acceleration factor will be equal to the total number of DEM blocks in the simulated electrical circuit N_{DEM}.

It should be noted that the threads are created at the beginning of each time-step and suppressed at the end of the time-step and thread management and affinity is performed by the operating system. Since (5.4) and (5.5) do not consider the time required to create and manage multiple threads in parallel, the actual acceleration factors will be smaller than the theoretical limit.

5.5 Simulation results

The parallelization tests in this section are performed in EMTP on a point-to-point MMC-HVDC link presented in Appendix B (except subsection 5.5.1.1). In the HVDC link there are two MMC stations, each MMC has six arms, which gives in total 12 blocks to parallelize and the maximum of 12 threads.

5.5.1 Validation

The tests in this subsection are performed to validate the implementation and accuracy of the proposed parallelization method.

5.5.1.1 Parallelization validation

To validate the implementation and to observe the dependencies between computing times and the number of DEM blocks, a simple electrical circuit shown in Figure 5.3 is used. It contains a DC current source and 12 DEM blocks. HB-SMs are used and all of them are inserted. Simulation time is 1 s and the time-step is 5 μs. The tests are performed on a Ciara Tech workstation with 4 physical and 8 logical cores. The number of SMs per arm is varied for a given number of threads.

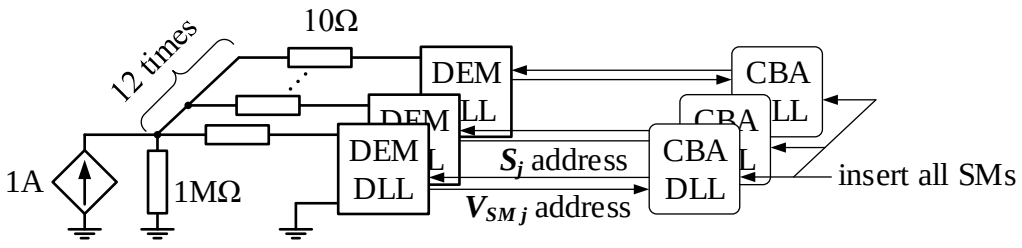


Figure 5.3 Simulated circuit to validate the implemented parallelization

Table 5.1 and Figure 5.4 show the computing times depending on the number of threads and SMs. It can be seen that the dependence on the number of SMs is linear for a given number of threads, which validates (5.2) and (5.3). Extrapolating computing times to $N_{SM} = 0$ yields the value of T_0. With parallelization, T_0 is relatively higher because some additional time is spent on the creation and management of threads. However, no clearly identifiable dependency of T_0 on the number of threads has been observed.

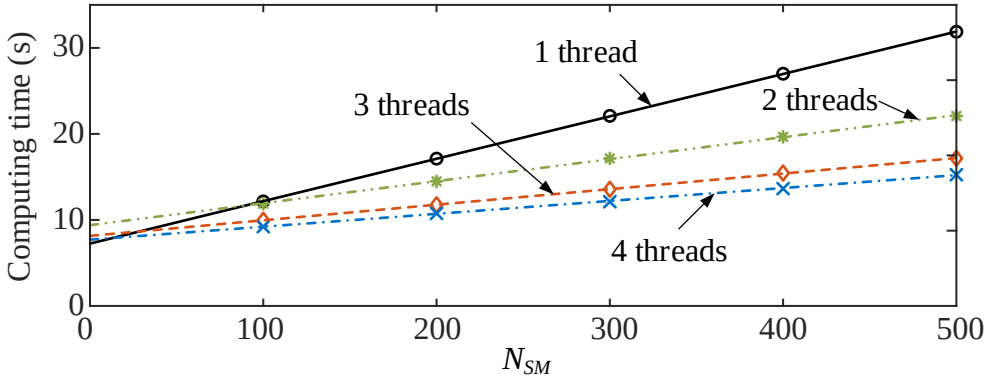


Figure 5.4 Computing times with different number of threads

Table 5.1 Computing times with different number of threads (s)

Number of SMs	**1 thread**	**2 threads**	**3 threads**	**4 threads**
0 (extrapolation for T_0)	7.25	9.39	8.15	7.70
100	12.15	11.89	9.96	9.21
200	17.13	14.49	11.76	10.75
300	22.10	17.15	13.57	12.11
400	27.00	19.66	15.45	13.63
500	31.88	22.08	17.16	15.24

For further analysis, the computing times in Table 5.1 are adjusted for the influence of T_0, i.e. its value is subtracted from the corresponding computing times for a given value of $n_{threads}$. The new values are shown in Table 5.2. The adjusted computing times are plotted in Figure 5.5 as a function of the number of DEM blocks computed in series, which is equal to

$$n_{serial} = \frac{N_{DEM}}{n_{threads}} \tag{5.6}$$

The results show linear dependency, which confirms the implemented parallelization scheme. However, it can be observed that even after the adjustment the extrapolation does not yield zero computing time for $n_{serial} = 0$. This remaining time is due to the computations performed in series for each arm. It is possible to make another observation: the time necessary to compute the DEM is directly proportional to the number of SMs, which also confirms the correctness of the implementation.

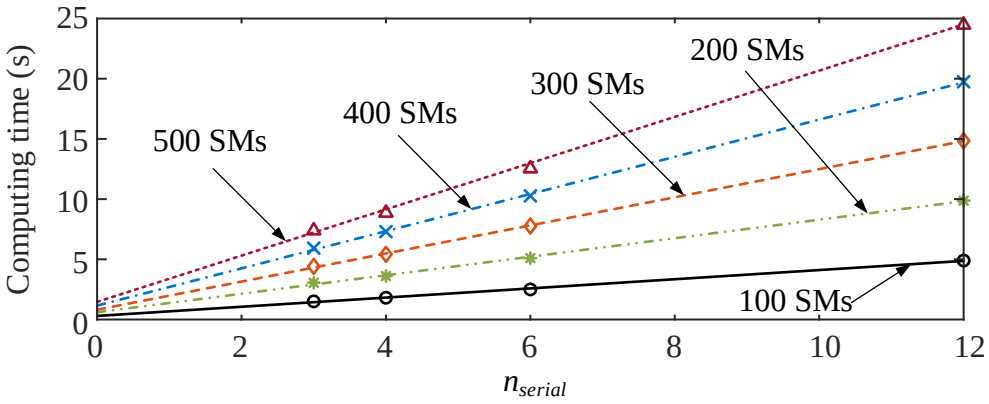


Figure 5.5 Adjusted computing times depending on the number of DEMs computed in series

Table 5.2 Computing times with different number of threads adjusted for T_0 (s)

Number of SMs	**1 thread**	**2 threads**	**3 threads**	**4 threads**
100	4.90	2.50	1.81	1.51
200	9.88	5.096	3.61	3.05
300	14.85	7.763	5.42	4.41
400	19.75	10.27	7.30	5.93
500	24.63	12.69	9.01	7.54

5.5.1.2 Power reference step

In this test, the waveforms obtained with the single-thread simulation are considered as references. The lines used for waveforms in figures of this subsection: 1 thread – solid black, 6 threads – dash-dotted blue, 12 threads – dashed orange. The step in the power reference value is applied once the system reaches steady-state. The step is from 100% to 50% of the nominal power transfer of 1 GW. No visible difference exists between the waveforms of the DC voltage (Figure 5.6), the AC power (Figure 5.7) or the total capacitor voltage (Figure 5.9) irrespective of the number of threads.

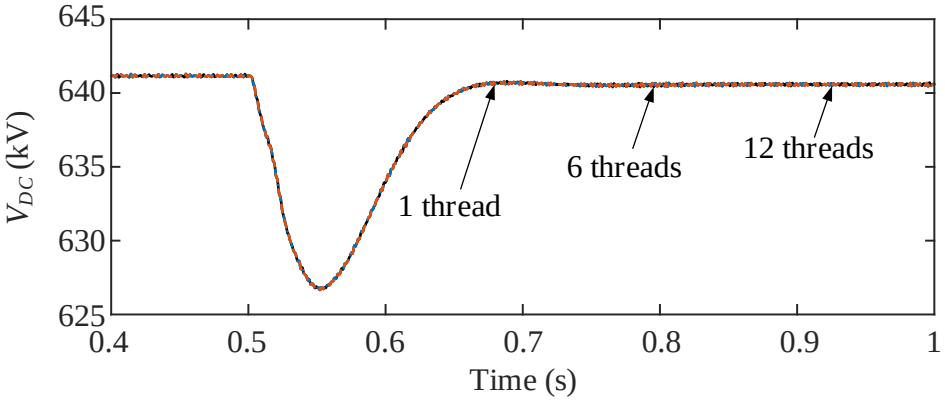


Figure 5.6 DC voltage with different number of threads

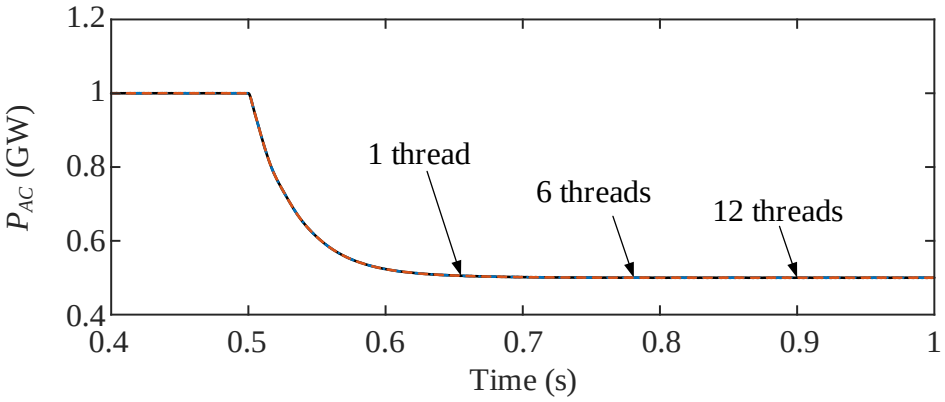


Figure 5.7 AC side active power at MMC1

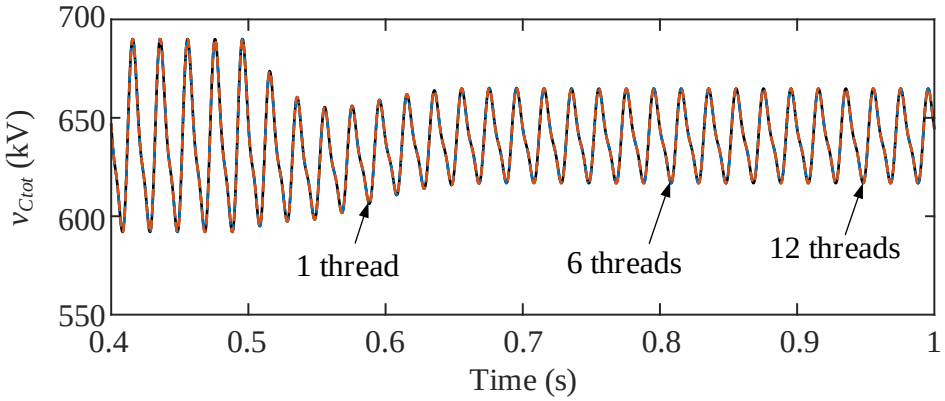


Figure 5.8 Total capacitor voltage in phase A upper arm at MMC1

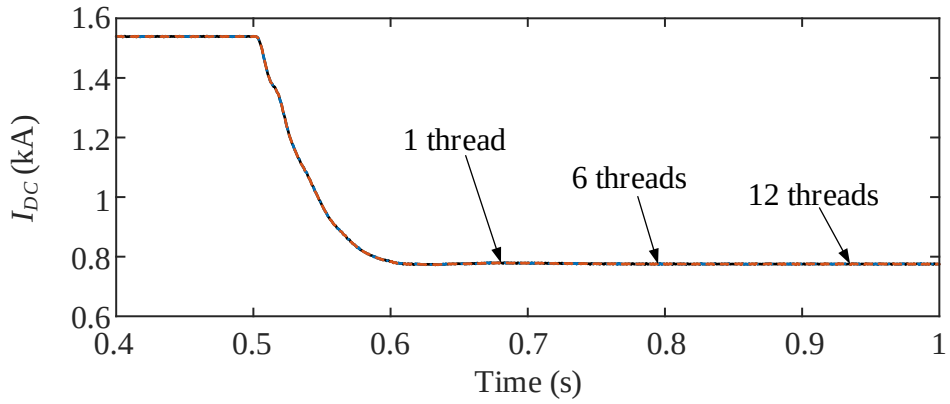


Figure 5.9 DC current

5.5.1.3 DC fault

The DC fault is applied in the middle of the DC link once the system reaches steady-state. The waveforms of different variables are shown in the following figures (Figure 5.10 to Figure 5.12). The blocking signal is activated at MMC1 at 0.50044 s, which causes all HB-SMs (for example, the 5th SM in Figure 5.10) to stop conducting immediately. FB-SMs (for example, the 305th SM in Figure 5.10) are able to pass the current in the negative direction, so continue to conduct for a brief moment after the blocking signal is activated. From the figures, it is clear that the waveforms obtained with parallelization match closely the single-threaded reference, no visible differences exist between the waveforms irrespective of the number of threads even at the SM level of detail.

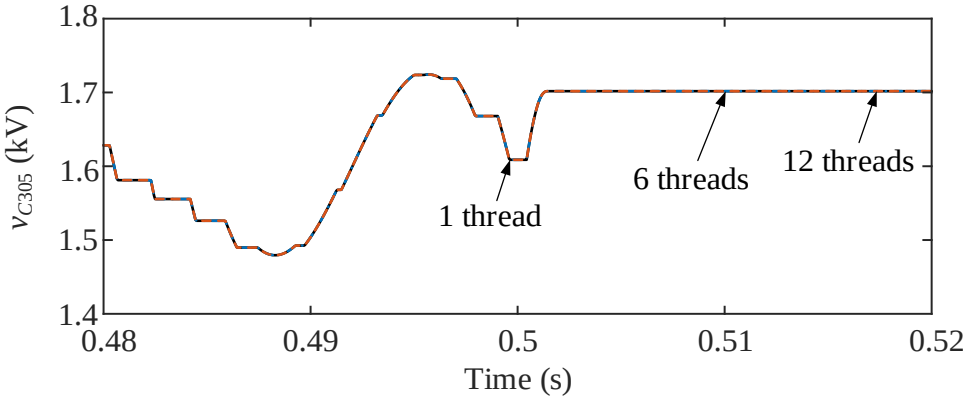


Figure 5.10 Voltage of the 305th SM in phase A upper arm at MMC1

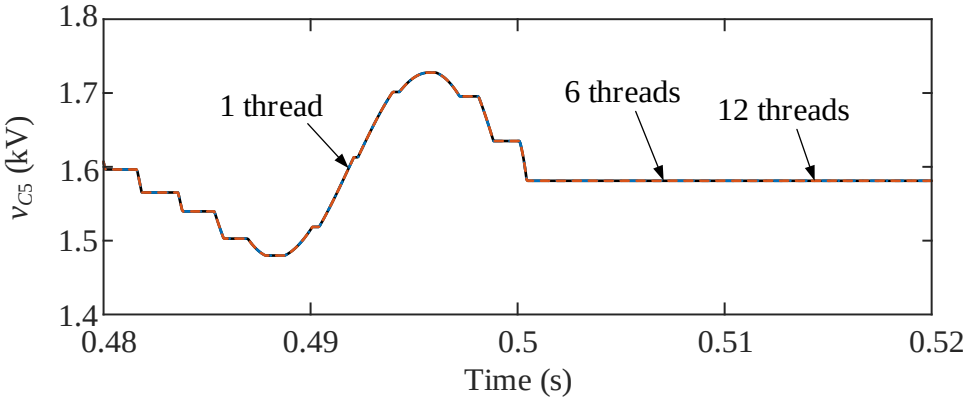


Figure 5.11 Voltage of the 5th SM in phase A upper arm at MMC1

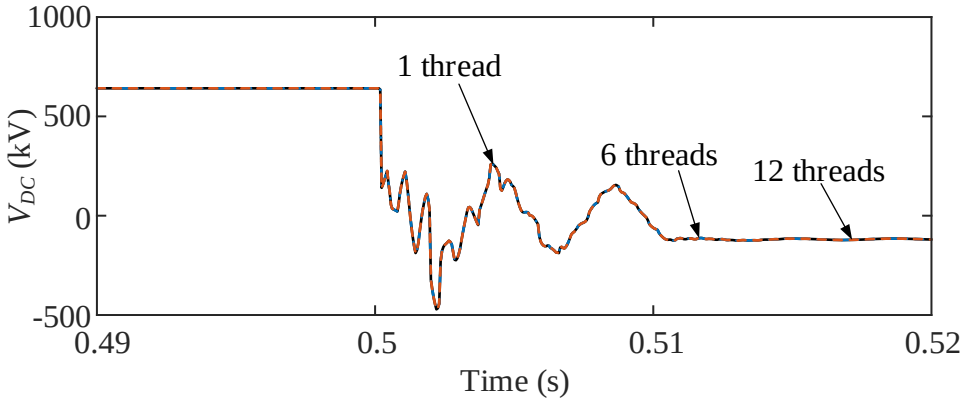


Figure 5.12 DC voltage

5.5.1.4 Error analysis

Theoretically speaking, parallelization should have no effect on the precision of the results, and the same exact values must be obtained irrespective of the number of threads that are used to compute a given task since the equations that are computed are identical. However, in reality, small relative differences in the order of 10^{-12} to 10^{-10} are perceivable in all signals. This can be attributed to the potential differences in the compiled binary code and to the different order of calculations, which can lead to rounding errors in the least significant numbers when representing variables using formats with finite levels of precision, such as the double-precision floating-point format, for example.

It should be noted that such errors also appear when a simulation is performed several times: with the multi-threaded implementation, each time the results are slightly different due to the different task allocation on multiple cores. When the single-threaded simulation is performed multiple times,

the results are identical. Given the small magnitude of the errors, it can be considered that parallelization produces equally accurate results as the default single-threaded implementation, therefore the proposed parallelization method is validated.

5.5.2 Time gains

Two computers are used to evaluate the acceleration resulting form the proposed parallelization: a Lenovo T560 laptop with two physical and four logical cores and a Lenovo P910 Thinkstation with 24 physical cores and 48 logical cores. The first configuration allows to demonstrate the behavior under the restricted number of cores and the second one demonstrates the behavior of the system when the number of cores is higher than the maximum number of threads. In all performed cases, the system is simulated for one second in normal operating mode.

Since different computers are used in the following performance evaluation tests, acceleration factors will be used for comparisons and demonstrations instead of computing times. This allows to eliminate the differences that are present in computing times that appear due to different clock rates, processors architectures, and thread management on different computers.

5.5.2.1 Restricted number of cores (Lenovo T560 laptop)

The computing times of the sequential single-thread simulation are taken as the reference times. The simulations are performed with two different types of CBA: permutation-based and voltage sorting-based. Numerical values of the acceleration factors with different number of threads depending on the number of SMs are shown in Table 5.3 and Table 5.4. Figure 5.13 and Figure 5.14 show the dependence graphically.

Table 5.3 Acceleration factors with permutation CBA

Number of SMs	**2 threads**	**4 threads**	**6 threads**	**12 threads**
100	1.03	0.91	0.52	0.59
200	1.1	1	0.61	0.7
300	1.13	1.06	0.68	0.78
400	1.16	1.07	0.76	0.85
500	1.15	1.11	0.8	0.9

Table 5.4 Acceleration factors with voltage sorting CBA

Number of SMs	**2 threads**	**4 threads**	**6 threads**	**12 threads**
100	1.06	0.98	0.53	0.61
200	1.18	1.17	0.78	0.87
300	1.26	1.3	1.04	1.13
400	1.29	1.37	1.19	1.28
500	1.3	1.4	1.27	1.36

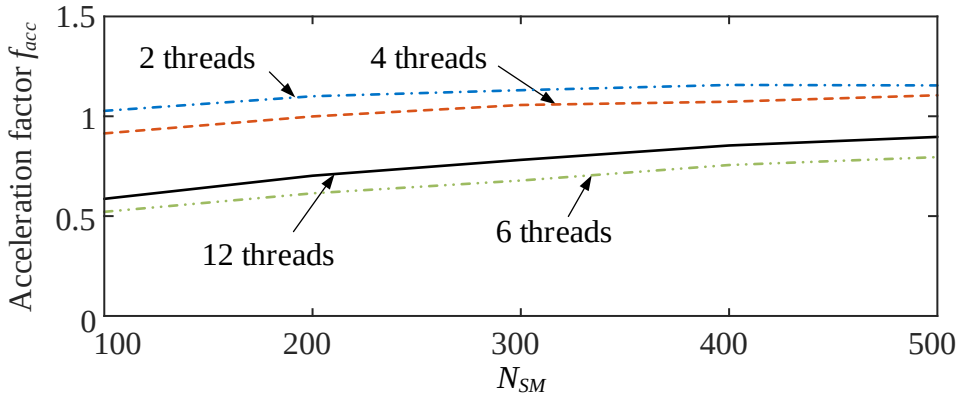


Figure 5.13 Acceleration factors with permutation-based CBA

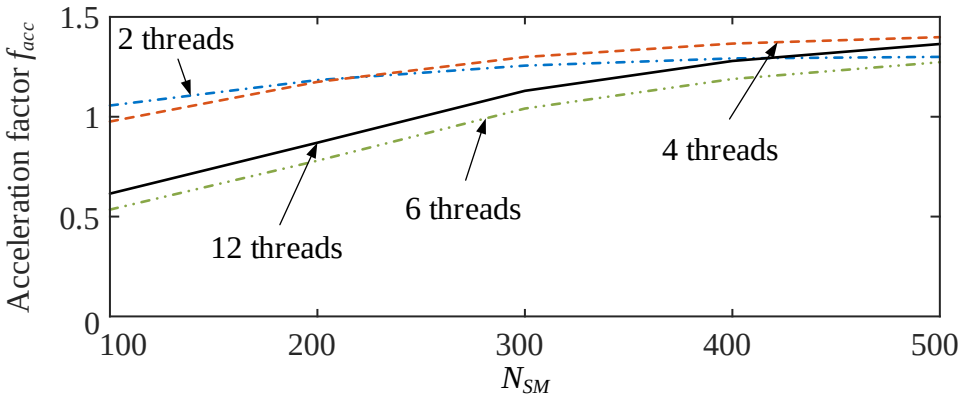


Figure 5.14 Acceleration factors with voltage sorting-based CBA

It can be observed that with a relatively low number of SMs, parallelization on multiple threads does not result in acceleration at all. Quite the contrary, the effort necessary to create multiple threads and manage them in parallel slows down the computations considerably. As the computational load increases with the number of SMs, acceleration factors increase as well. But even in cases with $N_{SM} = 500$, parallelization results in relatively insignificant acceleration factors when only a small number of cores is available. The acceleration tends to a saturation limit as the

number of SMs increases. This limit represents the proportion of the computations performed in parallel to the amount of computations that still have to be performed in series in each arm.

It can also be observed that the acceleration factor is not proportional to the number of threads run in parallel: when the computational burden of the DEM and the CBA is relatively small compared to the rest of the network (which is the case with the permutation-based CBA), the smaller number of threads results in a better acceleration. As the computational burden of the MMC becomes dominant in the simulated design (with the voltage sorting-based CBA), the parallelization on multiple threads performs better in terms of acceleration.

When the number of threads is higher than the number of cores, some threads must wait until others finish their execution, which causes additional time losses. Such effects can be observed when the number of threads is higher than the number of physical cores (see the curves for two and four threads in Figure 5.13 and Figure 5.14, two cores have better acceleration factors more often).

5.5.2.2 Unrestricted number of cores (Lenovo P910 Thinkstation)

The computing times of the single-threaded simulation are taken as the reference times. The simulations are performed with two different types of the CBA: permutation-based and voltage sorting-based (see Chapter 2, subsection 2.5.8.2 for the CBA details). Numerical values of the acceleration factors with different number of threads depending on the number of SMs are shown in Table 5.5, and Figure 5.15 shows the dependence graphically.

Table 5.5 Acceleration factors with high number of cores

Number of SMs	**Permutation-based CBA**		**Voltage sorting-based CBA**	
	6 threads	**12 threads**	**6 threads**	**12 threads**
100	1.21	1.36	1.32	1.5
200	1.43	1.57	1.83	2.28
300	1.56	1.74	2.38	2.97
400	1.62	1.84	2.64	3.53
500	1.68	1.93	2.9	4.03

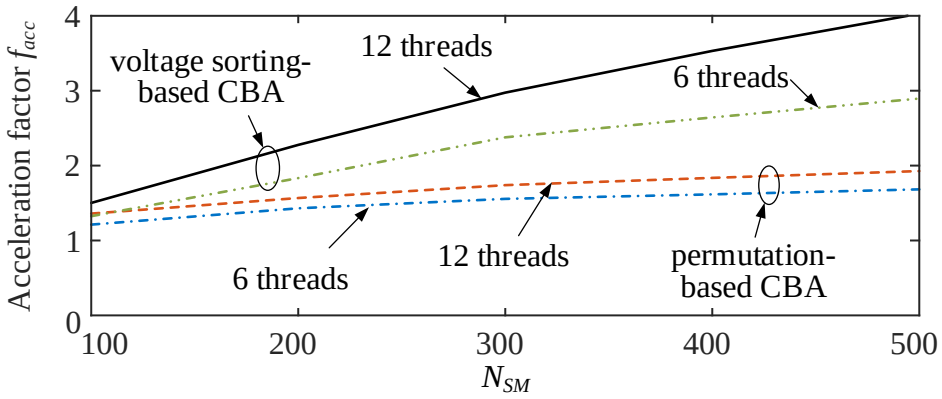


Figure 5.15 Acceleration factors with high number of cores

In the case when the number of cores available for parallelization is high, much better acceleration factors can be observed. In this case, a higher number of parallel threads translates directly to a higher acceleration factor. As in the case with a relatively small number of cores, better acceleration is achieved when the computational burden of the MMC is high relatively to the rest of the simulated design. This is the case with the voltage sorting-based CBA, where the acceleration factor reaches four and can be even higher if more MMCs are present in the simulated design.

5.5.2.3 Two parallel MMC-HVDC links

Another test-case is two MMC-HVDC links running in parallel. In this case, the maximum number of threads is 24. This is used to demonstrate the impact of the number of threads on the acceleration factor. Voltage sorting CBA is used and 400 SMs with 320 of them being FB-SMs. Hyperthreading is disabled. Total simulation time is 1 s and the time-step is 5 μs.

Results are shown in Figure 5.16 and Table 5.6. It can be seen in Figure 5.16 that with the permutation-based CBA the acceleration factor tends to a saturation limit when the number of parallel threads is above six. This saturation indicates that the time spent on the calculations of the parallelizable elements has become negligible compared to the rest of the design which is still performed in series. The elements that are still calculated in series include the two wideband cable models, the grid impedances, the MMC control systems except for the CBA blocks.

With the voltage sorting-based CBAs, the system does not exhibit saturation even at 24 threads, which means that the computational load of such CBAs is relatively high compared to the rest of the simulated design.

In all tests, the memory pointer implementation allows to considerably improve the acceleration factors.

When the number of threads is equal to six, a small dip can be seen in all waveforms in Figure 5.16. This can be attributed to the hardware implementation of multicore processors.

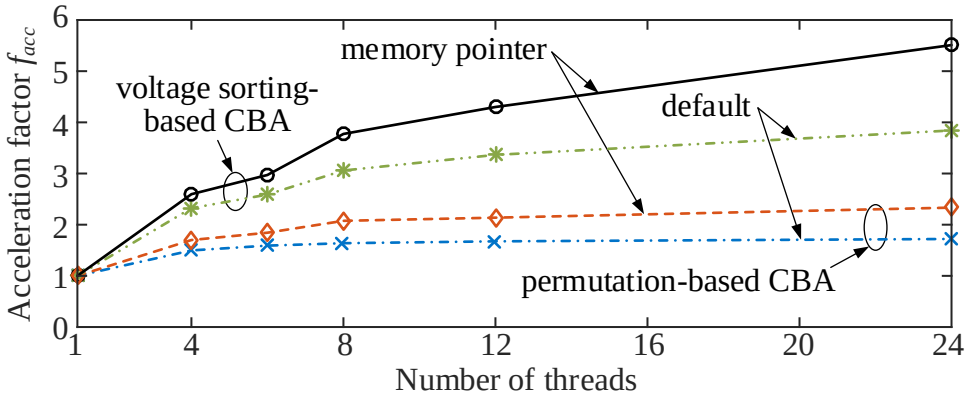


Figure 5.16 Acceleration factors with two HVDC links

Table 5.6 Acceleration factors depending on the number of threads

Thread count	**Permutation-based CBA**		**Voltage sorting-based CBA**	
	Default	**memory pointer**	**default**	**memory pointer**
1 (base time)	1 (289.4 s)	1 (232.2 s)	1 (764.2 s)	1 (730.8 s)
4	1.5	1.7	2.32	2.6
6	1.59	1.84	2.59	2.97
8	1.64	2.08	3.06	3.77
12	1.67	2.14	3.36	4.3
24	1.72	2.33	3.84	5.51

5.5.2.4 DEM-only parallelization

In some cases, individual blocks of the control system, such as the CBA, might not be available for parallelization. This is the case, for example, when the control system is provided by a manufacturer to a transmission system operator in a form of a black box due to the confidentiality of intellectual property. In such cases, only the DEM can be parallelized. The memory pointer implementation of the DEM cannot be used. Consequently, the acceleration factors resulting from the DEM-only parallelization will be less significant.

The same two MMC-HVDC links with 400 SMs as in the subsection 5.5.2.3 are used to demonstrate the effects of DEM-only parallelization. The results are shown in Figure 5.17 and Table 5.7.

It can be seen in Figure 5.17 that when the CBA requires a considerable amount of computations, which is the case of the voltage sorting-based CBA, the DEM parallelization has a negligible effect, the acceleration factors are close to one irrespective of the number of threads. With the permutation-based CBA, DEM parallelization has a more perceivable effect, the acceleration factors are closer to 1.3–1.4. The saturation limit of f_{acc} in this case is reached even with four threads.

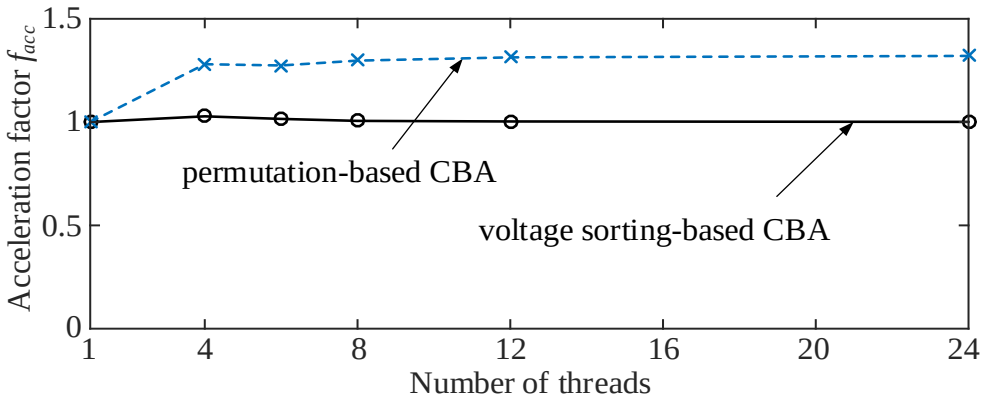


Figure 5.17 Acceleration factors with DEM-only parallelization

Table 5.7 Acceleration factors depending on the number of threads

Thread count	**Permutation-based CBA**	**Voltage sorting-based CBA**
1 (base time)	1 (289.4 s)	1 (756.5 s)
4	1.28	1.03
6	1.27	1.02
8	1.3	1.01
12	1.31	1
24	1.32	1

5.6 Conclusion

This chapter proposed an arm-level parallelization method for the DEM which also includes the parallelization of the CBA. The proposed method allows to significantly accelerate offline EMT simulations.

Two main factors affecting the acceleration gains have been observed. First, it is the number of SMs in the arm. The acceleration factor increases as the number of SMs increases, owing to the increase in the computational burden of the parallelizable computations compared to the rest of the simulated design.

The second important factor is the number of threads used for parallelization. In the situations when a large number of cores is available for the DEM parallelization, the acceleration factor increases with the number of parallel threads until it reaches a saturation limit. This limit indicates that the time spent to perform the internal calculations of the DEM and CBA has become negligible compared to the rest of the simulated circuit. However, when the number of available cores is limited, the parallelization can increase the computing time. Such negative effects can be observed in the situations when the time saved with the parallel computation is smaller than the additional efforts necessary to create and manage multiple threads.

Memory pointer implementation also improves acceleration of computations.

The CBA plays an important role in providing high acceleration factors, owing to its significant computational burden. The highest acceleration factors are achievable when the CBA has a lot of internal calculations and they are parallelized.

DEM-only parallelization can result in some acceleration if its computational effort is comparable to the rest of the simulated circuit. This is not the case when the voltage sorting-based CBA is applied. However, with the permutation-based CBA, the simulations can be accelerated by about 30% to 40%.

CHAPTER 6 SPURIOUS POWER IN THE ARM EQUIVALENT MODEL

Accurate representation of power losses is an important and challenging subject in power grid simulations. In this chapter, it is demonstrated that some amounts of spurious power can be generated in the AEM of MMC. Depending on the operating conditions and simulation parameters, such spurious power can surpass converter station losses, thus deteriorating accuracy of the simulations.

The AEM can be implemented in different ways in an EMT-type software. The model equations can be incorporated into the main network equations (MNE) matrix, in which case the model equations are solved simultaneously with the network. Otherwise, the model equations can be implemented using control diagram blocks of the EMT software [125, 126]. In this case, the drawback is the one-time-step delay between the solution of control blocks and the MNE in the EMT simulation software. If the model equations are not solved simultaneously with the surrounding power circuit equations, the AEM of MMC can generate or consume spurious power. A similar phenomenon of additional power has been reported in [127] for the AVM but no detailed explanation of its origin has been provided.

In this chapter, analytical formulation of spurious power is derived for two implementations of the AEM and several models that eliminate or reduce such power are proposed. The proposed solutions are validated and compared on a practical test case of an MMC-based HVDC transmission.

6.1 Derivation of AEM spurious power

Two operational modes are usually discussed when dealing with MMCs: normal operation and blocked mode. In this chapter, only normal operation is considered because power losses in the converter are important in steady-state operation.

If main AEM equations (2.37)–(2.39) are solved simultaneously at each time-point, the power generated/consumed in the model matches that of the surrounding circuit, as demonstrated below. Instantaneous arm power on the power circuit side is given by:

$$p_{arm} = i_{arm}\, v_{arm} \tag{6.1}$$

Instantaneous power on the equivalent capacitor side is:

$$p_{Ctot} = i_{Ctot}\ v_{Ctot} \tag{6.2}$$

Considering (2.38), (6.2) can be rewritten as

$$p_{Ctot} = i_{arm}\ s_{arm}\ v_{Ctot} \tag{6.3}$$

When considering (2.37), (6.1), and (6.3) it is clear that $p_{arm} = p_{Ctot}$, which means that in the case of simultaneous solution no spurious power is generated irrespective of the waveforms of arm currents and voltages. The presence of delays, however, results in spurious power Δp being generated in the network, which is defined as

$$\Delta p = p_{arm} - p_{Ctot} \tag{6.4}$$

To demonstrate that, two AEM implementations are considered: Classical-AEM-1 and Classical-AEM-2, see Figure 2.9.

6.1.1 Classical-AEM-1

In Classical-AEM-1 (Figure 2.9.a), there is a Δt delay between the input v_{ref} and the output v_{arm} signals of the controlled voltage source block:

$$v_{arm}\left(t+\Delta t\right) = v_{ref}\left(t\right) \tag{6.5}$$

From Figure 2.9.a, $v_{ref} = v_{Ctot}\ s_{arm}$ and $i_{Ctot} = i_{arm}\ s_{arm}$. So, capacitor side power (6.2) is rewritten as

$$p_{Ctot\ AEM\,1}\left(t\right) = i_{arm}\left(t\right) v_{ref}\left(t\right) = i_{arm}\left(t\right) v_{arm}\left(t+\Delta t\right) \tag{6.6}$$

Considering (6.1) and (6.6), the spurious power of the Classical-AEM-1 equals to

$$\Delta p_{AEM\,1}\left(t\right) = -i_{arm}\left(t\right)\left[v_{arm}\left(t+\Delta t\right) - v_{arm}\left(t\right)\right] \tag{6.7}$$

Clearly, $\Delta p_{AEM\,1}$ is not equal to zero if v_{arm} is not a constant value. Assuming that Δt is small, $\Delta p_{AEM\,1}$ can be rewritten using the forward finite difference approximation of a derivative:

$$\frac{d}{dt} v_{arm}\left(t\right) \approx \frac{v_{arm}\left(t+\Delta t\right) - v_{arm}\left(t\right)}{\Delta t} \tag{6.8}$$

With (6.8), (6.7) is rewritten to simplify steady-state analysis:

$$\Delta p_{AEM\,1} \approx -\Delta t\, i_{arm} \frac{d}{dt} v_{arm} \tag{6.9}$$

6.1.2 Classical-AEM-2

Spurious power for the Classical-AEM-2 is found in a similar manner. From Figure 2.9.b, the following equations can be written:

$$v_{ref} = v_{Ctot}\, s_{arm} \tag{6.10}$$

$$i_{Ctot}(t) = i_{arm}(t-\Delta t)\, s_{arm}(t-\Delta t) \tag{6.11}$$

Using (6.2), (6.10), and (6.11), capacitor-side power for the Classical-AEM-2 is formulated as

$$p_{Ctot\,AEM\,2}(t) = i_{arm}(t-\Delta t)\, s_{arm}(t-\Delta t) \frac{v_{ref}(t)}{s_{arm}(t)} \tag{6.12}$$

Since the Δt delay between v_{ref} and v_{arm} signals is also present in the Classical-AEM-2, $p_{Ctot\,AEM\,2}$ is rewritten by using (6.5) as

$$p_{Ctot\,AEM\,2}(t) = i_{arm}(t-\Delta t)\, v_{arm}(t+\Delta t) \frac{s_{arm}(t-\Delta t)}{s_{arm}(t)} \tag{6.13}$$

To simplify this equation, exact values of all signals in (6.13) are replaced by the first-order Taylor series expansion at t:

$$i_{arm}(t-\Delta t) \approx i_{arm}(t) - \Delta t \frac{d}{dt} i_{arm}(t) \tag{6.14}$$

$$v_{arm}(t+\Delta t) \approx v_{arm}(t) + \Delta t \frac{d}{dt} v_{arm}(t) \tag{6.15}$$

$$\frac{s_{arm}(t-\Delta t)}{s_{arm}(t)} \approx 1 - \frac{\Delta t}{s_{arm}(t)} \frac{d}{dt} s_{arm}(t) \tag{6.16}$$

Considering (6.14) and (6.15), the following relation is deduced, where the summand with Δt^2 is neglected due to the small time-step assumption

$$i_{arm}\left(t-\Delta t\right)v_{arm}\left(t+\Delta t\right)\approx i_{arm}\,v_{arm}+\left[i_{arm}\frac{d}{dt}v_{arm}-v_{arm}\frac{d}{dt}i_{arm}\right]\Delta t-\cancel{\Delta t^{2}\frac{d}{dt}i_{arm}\frac{d}{dt}v_{arm}} \quad (6.17)$$

Considering (6.16) and (6.17), capacitor-side power for the Classical-AEM-2 (6.13) is rewritten and the summand including multiplication by Δt^2 is again neglected:

$$p_{Ctot\ AEM\ 2}\approx i_{arm}\,v_{arm}\left[1-\frac{\Delta t}{s_{arm}}\frac{d}{dt}s_{arm}\right]+\left[i_{arm}\frac{d}{dt}v_{arm}-v_{arm}\frac{d}{dt}i_{arm}\right]\left[\Delta t-\cancel{\frac{\Delta t^{2}}{s_{arm}}\frac{d}{dt}s_{arm}}\right] \quad (6.18)$$

With this, spurious power for the Classical-AEM-2 is found as

$$\Delta p_{AEM\ 2}=i_{arm}\,v_{arm}-p_{Ctot\ AEM\ 2}=\Delta t\,v_{arm}\frac{d}{dt}i_{arm}-\Delta t\,i_{arm}\left[\frac{d}{dt}v_{arm}-\frac{v_{arm}}{s_{arm}}\frac{d}{dt}s_{arm}\right] \quad (6.19)$$

To simplify further analysis, the second summand of (6.19) is defined as a convenience variable

$$\delta p_{AEM\ 2}=-\Delta t\,i_{arm}\left[\frac{d}{dt}v_{arm}-\frac{v_{arm}}{s_{arm}}\frac{d}{dt}s_{arm}\right] \quad (6.20)$$

Control signals, such as the arm switching function s_{arm}, are not always available at the stage of steady-state analysis, so s_{arm} is replaced by v_{arm}/v_{Ctot} in (6.20). It should be noted that taking $s_{arm}\approx v_{arm}/V_{DC}$ at this stage will yield insufficiently accurate results since in this case $\delta p_{AEM\ 2}$ would be equal zero. Therefore, $\delta p_{AEM\ 2}$ is rewritten as

$$\delta p_{AEM\ 2}=\Delta t\,i_{arm}\,v_{Ctot}\frac{d}{dt}\left(\frac{v_{arm}}{v_{Ctot}}\right)-\Delta t\,i_{arm}\frac{d}{dt}v_{arm} \quad (6.21)$$

Using the quotient derivative rule and algebraical manipulations, the following equation is obtained

$$\delta p_{AEM\ 2}=-\Delta t\,i_{arm}\frac{v_{arm}}{v_{Ctot}}\frac{d}{dt}v_{Ctot} \quad (6.22)$$

This is further simplified by approximating $v_{Ctot}\approx V_{DC}$ in the denominator and replacing $\frac{d}{dt}v_{Ctot}$ by i_{Ctot}/C_{arm}:

$$\delta p_{AEM\ 2}\approx-\Delta t\frac{i_{arm}\,v_{arm}}{V_{DC}\,C_{arm}}i_{Ctot} \quad (6.23)$$

At this point, i_{Ctot} is replaced by $s_{arm}\, i_{arm}$ with the approximation of $s_{arm} \approx v_{arm} / V_{DC}$:

$$\delta P_{AEM\,2} \approx -\Delta t \frac{i_{arm}\, v_{arm}}{V_{DC}\, C_{arm}} i_{arm}\, \frac{v_{arm}}{V_{DC}} \tag{6.24}$$

So, considering (6.19), (6.20), and (6.24), the spurious power for the Classical-AEM-2 is finally defined as

$$\Delta p_{AEM\,2} \approx \Delta t\, v_{arm}\, \frac{d}{dt} i_{arm} + \delta p_{AEM\,2} = \Delta t\, v_{arm}\, \frac{d}{dt} i_{arm} - \Delta t \frac{i_{arm}^2\, v_{arm}^2}{V_{DC}^2\, C_{arm}} \tag{6.25}$$

It should be noted that $\delta p_{AEM\,2}$ is considerably smaller in amplitude than the first summand in (6.25) due to the V_{DC}^2 contribution in the denominator. Therefore, $\delta P_{AEM\,2}$ will only be considered in the analysis of the constant part of the spurious power in the following section.

6.2 Steady-state analysis of spurious power

The same assumptions for the steady-state MMC operation as in the Chapter 3, Section 3.2 are taken in this chapter, resulting in the consideration of only the DC and fundamental components for arm currents and voltages:

$$i_{arm} = I_0 + I_1 \cos\left(\omega t + \varphi_i\right) \tag{6.26}$$

$$v_{arm} = V_0 + V_1 \cos\left(\omega t + \varphi_v\right) \tag{6.27}$$

Spurious power in the Classical-AEM-1 is then calculated as follows:

$$\Delta p_{AEM\,1} = \Delta t \left[I_0 + I_1 \cos\left(\omega t + \varphi_i\right) \right] \omega V_1 \cos\left(\omega t + \varphi_v - \frac{\pi}{2} \right) \tag{6.28}$$

The above equation can be separated into three harmonic terms: DC component, fundamental component, and double-fundamental-frequency component:

$$\Delta p_{AEM\,1_2} = \Delta t\, \omega \frac{V_1\, I_1}{2} \cos\left(2\omega t + \varphi_v + \varphi_i - \frac{\pi}{2} \right) \tag{6.29}$$

$$\Delta p_{AEM\,1_1} = \Delta t\, \omega V_1\, I_0 \cos\left(\omega t + \varphi_v - \frac{\pi}{2} \right) \tag{6.30}$$

$$\Delta p_{AEM\,1_0} = \Delta t\ \omega \frac{V_1\ I_1}{2} \cos\left(\varphi_v - \varphi_i - \frac{\pi}{2}\right) \tag{6.31}$$

$$\Delta p_{AEM\,1} = \Delta p_{AEM\,1_0} + \Delta p_{AEM\,1_1} + \Delta p_{AEM\,1_2} \tag{6.32}$$

A similar equation is derived for the Classical-AEM-2:

$$\Delta p_{AEM\,2} \approx \Delta t\left[V_0 + V_1 \cos\left(\omega t + \varphi_v\right)\right] \omega I_1 \cos\left(\omega t + \varphi_i + \frac{\pi}{2}\right) + \delta P_{AEM\,2} \tag{6.33}$$

The harmonic components:

$$\Delta p_{AEM\,2_2} = \Delta t\ \omega \frac{V_1\ I_1}{2} \cos\left(2\omega t + \varphi_i + \varphi_v + \frac{\pi}{2}\right) \tag{6.34}$$

$$\Delta p_{AEM\,2_1} = \Delta t\ \omega V_0\ I_1 \cos\left(\omega t + \varphi_i + \frac{\pi}{2}\right) \tag{6.35}$$

$$\begin{aligned} \Delta p_{AEM\,2_0} = {} & \Delta t\ \omega \frac{V_1\ I_1}{2} \cos\left(\varphi_v - \varphi_i - \frac{\pi}{2}\right) \\ & - \frac{\Delta t}{V_{DC}^2\ C_{arm}} \left[V_0^2 + \frac{V_1^2}{2}\right]\left[I_0^2 + \frac{I_1^2}{2}\right] \\ & - \frac{\Delta t}{V_{DC}^2\ C_{arm}} \left[2 I_0\ I_1\ V_0\ V_1 \cos\left(\varphi_v - \varphi_i\right) + \frac{I_1^2\ V_1^2}{2} \cos\left(2\varphi_v - 2\varphi_i\right)\right] \end{aligned} \tag{6.36}$$

$$\Delta p_{AEM\,2} = \Delta p_{AEM\,2_0} + \Delta p_{AEM\,2_1} + \Delta p_{AEM\,2_2} \tag{6.37}$$

The oscillating terms (6.29), (6.30) for the Classical-AEM-1 and (6.34), (6.35) for the Classical-AEM-2 do not deteriorate steady-state power balance of the converter because all the extra-generated power during one half-cycle is consumed during the other half-cycle. The constant terms (6.31) or (6.36), however, are always present and therefore affect the converter power balance.

6.2.1 Double fundamental frequency component

Under balanced conditions, double-fundamental-frequency components (6.29) and (6.34) in the lower arms sum up to zero due to the 120° phase shift in between them. The same can be said about the upper arms, so these components have no effect outside of the MMC.

Depending on the control strategies during grid unbalance [134], fundamental phasors of current and voltage can differ among phases, so it is possible that double-fundamental-frequency spurious power becomes visible outside the MMC under some conditions in the form of a ripple.

6.2.2 Fundamental frequency component

In a given phase, the DC components of current and voltage in the upper and lower arm are identical, while the fundamental components have a 180° phase shift. Therefore, fundamental-frequency terms (6.30) and (6.35) in upper and lower arms cancel each other out in each phase, since they are in phase opposition. Unbalance between upper and lower arms in each phase is usually kept to a minimum even during grid unbalance, so there is no effect of this component on the external behavior of the converter.

6.2.3 Constant component

The constant components of the spurious power (6.31) and (6.36) are the source of power mismatch affecting the whole grid. Depending on the phases of the AC components of arm current and voltage (φ_i and φ_v), power loss or generation can occur. In balanced conditions, the constant terms of the spurious power are the same for all six arms, so their effects sum up and can be observed outside of the MMC. During unbalance, their values can differ among arms.

6.3 Elimination of spurious power

Four solutions to remove or reduce the magnitude of the spurious power are considered: time-step reduction, extrapolating voltage references (extrapolation AEMs), variable resistance implementation, and equivalent voltage source model.

6.3.1 Time-step reduction

According to (6.9) and (6.25), spurious power is proportional to the time-step, so reducing Δt must proportionally reduce the spurious power. However, reducing the time-step slows down the simulations, so a value of Δt must be found that achieves a compromise between accuracy and simulation time. In this chapter, the Δt is taken so that the maximal value of Δp is below or equal to 10% of the average conduction losses in the arm:

$$\max\left|\Delta p_{AEM\,1}\right| \le 0.1 R_{arm}\left[I_0^2 + I_1^2/2\right] \tag{6.38}$$

For the classical-AEM-1:

$$\Delta t_{AEM\,1}\,\omega V_1\left[I_0 + I_1\right] \le 0.1\,R_{arm}\left[I_0^2 + I_1^2/2\right] \tag{6.39}$$

$$\Delta t_{AEM\,1} \le 0.1\frac{R_{arm}\left[I_0^2 + I_1^2/2\right]}{\omega V_1\left[I_0 + I_1\right]} \tag{6.40}$$

Similarly, the time-step for Classical-AEM-2 is:

$$\Delta t_{AEM\,2} \le 0.1\frac{R_{arm}\left[I_0^2 + I_1^2/2\right]}{\omega I_1\left[V_0 + V_1\right]} \tag{6.41}$$

In (6.41), the contribution of $\delta p_{AEM\,2}$ is neglected since its amplitude is relatively small, as explained in subsection 6.1.2. Although $\Delta t_{AEM\,1}$ and $\Delta t_{AEM\,2}$ values in (6.40) and (6.41) depend on the operating conditions and therefore can vary, it can be concluded that for high-power HVDC transmissions where the voltages can reach hundreds of kV and currents are in the order of kA, satisfactory reduction of spurious power can be achieved with Δt at least below 10 μs.

6.3.2 Extrapolation-AEM-1

In steady-state and with relatively small simulation time-steps, arm voltage derivatives do not change significantly between adjacent time-points. This can justify a simple one-time-step extrapolation of the final voltage reference v_{ref}^{ext} supplied to the controlled voltage source:

$$v_{ref}^{ext} = v_{ref} + \Delta t\,\frac{d}{dt}v_{ref} \tag{6.42}$$

$$v_{arm}\left(t\right) = v_{ref}^{ext}\left(t - \Delta t\right) \tag{6.43}$$

The reference voltage derivative in (6.42) can be represented in the vicinity of t using first order Taylor series expansion (O represents higher-order terms):

$$v_{ref}\left(t\right) = v_{ref}\left(t - \Delta t\right) + \Delta t\,\frac{d}{dt}v_{ref}\left(t - \Delta t\right) + O\left(\Delta t^2\right) \tag{6.44}$$

Finally, $\Delta p_{AEM\,1}$ is rewritten as follows:

$$\Delta p_{AEM\,1}(t) = i_{arm}(t)\left[v_{ref}^{ext}(t-\Delta t) - v_{ref}(t)\right] = i_{arm}(t)\,O\left(\Delta t^2\right) \tag{6.45}$$

In steady-state and with small time-steps, the second- and higher-order terms $O\left(\Delta t^2\right)$ are negligible, therefore the spurious power is significantly reduced. The derivative of the voltage reference in (6.42) can be approximated by the backward finite difference

$$\frac{d}{dt}v_{ref}(t) \approx \frac{v_{ref}(t) - v_{arm}(t-\Delta t)}{\Delta t} \tag{6.46}$$

So

$$v_{ref}^{ext}(t) = 2v_{ref}(t) - v_{ref}(t-\Delta t) \tag{6.47}$$

The corresponding implementation is shown in Figure 6.1:

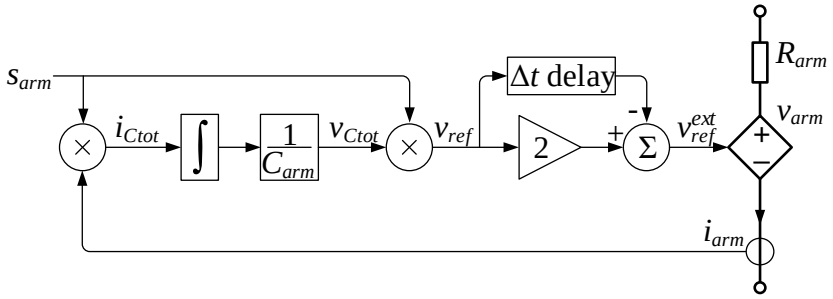


Figure 6.1 Extrapolation-AEM-1 diagram

6.3.3 Extrapolation-AEM-2

Based on the same assumptions, extrapolation can be applied to the Classical-AEM-2. In addition to (6.47), the current source reference is defined as

$$i_{ref}^{ext}(t) = 2i_{ref}(t) - i_{ref}(t-\Delta t) \tag{6.48}$$

The corresponding implementation is shown in Figure 6.2:

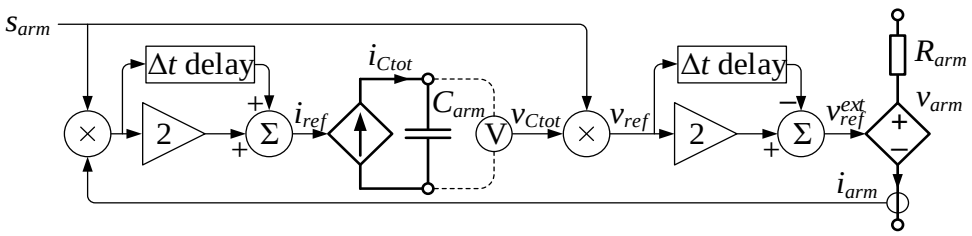


Figure 6.2 Extrapolation-AEM-2 diagram

6.3.4 Variable resistance AEM

It is possible to solve the AEM equations simultaneously with the surrounding network equations even if the AEM is implemented using control blocks. Discretization of (2.39) using trapezoidal integration yields

$$v_{Ctot} = \hat{v}_{Ctot} + R_C \; i_{Ctot} \tag{6.49}$$

with

$$\hat{v}_{Ctot}\left(t\right) = v_{Ctot}\left(t-\Delta t\right) + R_C \; i_{Ctot}\left(t-\Delta t\right) \tag{6.50}$$

$$R_C = \frac{\Delta t}{2\,C_{arm}} \tag{6.51}$$

Multiplying both sides of (6.49) by s_{arm} and considering that $v_{arm} = v_{Ctot}\; s_{arm}$ and $i_{Ctot} = i_{arm}\; s_{arm}$:

$$v_{arm} = s_{arm}\; \hat{v}_{Ctot} + R_C \; s_{arm}^2 \; i_{arm} \tag{6.52}$$

This equation can be implemented in the form of a Thevenin equivalent circuit:

$$v_{th} = \hat{v}_{Ctot} \; s_{arm} \tag{6.53}$$

$$r_{th} = R_C \; s_{arm}^2 \tag{6.54}$$

Since there is still a delay between the control system variables and electrical circuit, a delay is added to the arm switching function signal s_{arm} when calculating i_{Ctot} in (6.49) and (6.50) to adjust to the time point of i_{arm} sampling:

$$i_{Ctot}\left(t\right) = s_{arm}\left(t-\Delta t\right) i_{arm}\left(t\right) \tag{6.55}$$

Equations (6.49)–(6.55) can be implemented using standard control diagram blocks, as shown in Figure 6.3. Owing to the presence of a variable resistance in the diagram, this solution requires MNE matrix refactorization each time the value of r_{th} changes, which can occur at each time point unless very small time-steps are used (in the order of 1 μs).

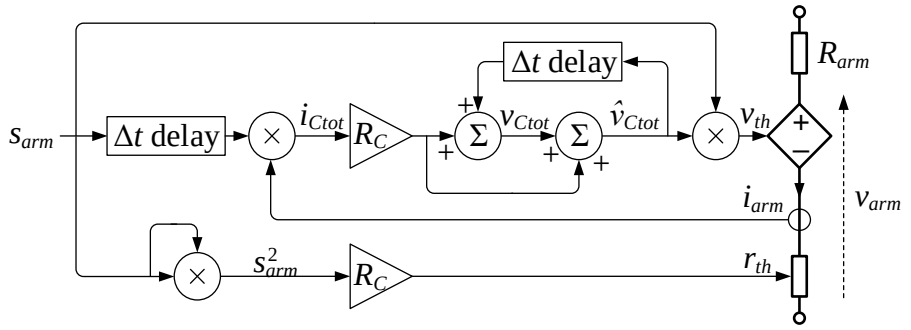


Figure 6.3 Variable resistance AEM diagram

6.3.5 Equivalent voltage source AEM

The effect of the variable resistance r_{th} in the model shown in Figure 6.3 can be emulated by an equivalent voltage source $v_{r\,eq}$, which eliminates the need to refactor the MNE:

$$v_{r\,eq} = r_{th}\, i_{arm}^{ext} \tag{6.56}$$

where i_{arm}^{ext} is the extrapolated arm current.

This current is obtained in a similar way to (6.48) by using backward finite difference derivative approximation:

$$i_{arm}^{ext}(t) = 2i_{arm}(t) - i_{arm}(t-\Delta t) \tag{6.57}$$

The corresponding implementation is shown in Figure 6.4.

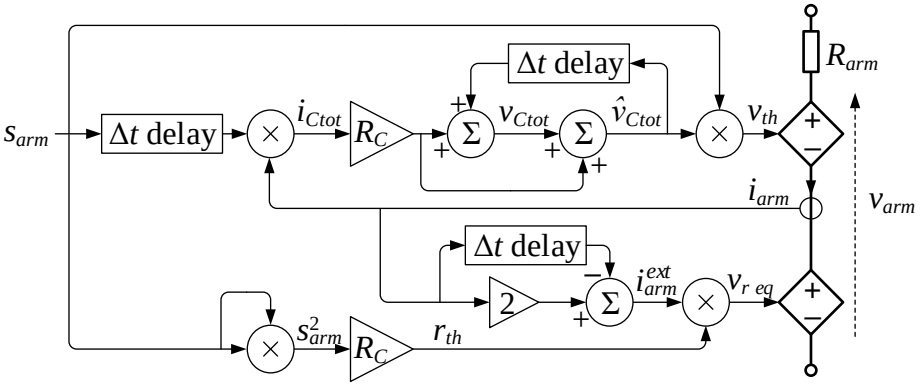


Figure 6.4 Equivalent voltage source AEM diagram

6.4 Simulation results

The HVDC link presented in the Appendix B is used to validate the presented methods for eliminating spurious power. All simulations are performed in EMTP [83].

Total converter station losses with half-bridge MMCs amount to approximately 1% of its nominal power P_{nom} [191]. Considering that power losses in high power transformers can lie within 0.3%–0.5% range of the nominal power [192], the rest is attributed to the converter and auxiliary high voltage equipment losses [89]. The latter is relatively small (around 0.1% [89]) and is neglected in this study. Therefore, the transformer losses are taken as 0.3% and the conduction losses represented by arm resistances R_{arm} are taken as 0.6% of P_{nom}.

The ON-state resistance R_{ON} of a single IGBT switch can be found from (6.58) at the nominal power transfer. The obtained value is 2.304 mΩ, which is realistic for high power MMCs [89].

$$0.6\%\, P_{nom} = 6\, N_{SM}\, R_{ON} \left[I_0^{\,2} + I_1^2 / 2 \right] \tag{6.58}$$

In the simulations, a 50 μs time-step is applied when AEMs are used. Having this relatively large time-step serves two purposes: to emphasize the problem and to demonstrate that accurate results can be obtained even with a large Δt when the proposed spurious power elimination methods are applied. The reference waveforms are obtained with the DEM using $\Delta t = 5\,\mu s$.

6.4.1 Demonstration of spurious power

To demonstrate the effects of the spurious power, active power at different points of the circuit is shown in Figure 6.6: at the point of coupling with the grid (p_{PCC}), at the AC terminals (p_{AC}) and at the DC terminals (p_{DC}) of the converter. These points are shown in Figure 6.5. The HVDC link is subjected to the nominal power transfer of 1 GW. Figure 6.6 also shows the adjusted power p_{adj} for the classical AEMs. This is the DC side power compensated for spurious power:

$$p_{adj} = p_{DC} - \sum \Delta p \tag{6.59}$$

With the DEM and AEMs, the difference between p_{PCC} and p_{AC} is 3 MW, which corresponds to transformer losses (0.3% of the nominal power). However, a visible difference exists between p_{DC}

values with different models. With the DEM, converter losses amount to approximately 6 MW (difference between p_{AC} and p_{DC}), which corresponds to 0.6% of P_{nom} as expected. With the AEMs, the losses are considerably smaller. However, the adjusted power p_{adj} is at the same level as p_{DC} with the DEM, which confirms that the spurious power is the source of the mismatch.

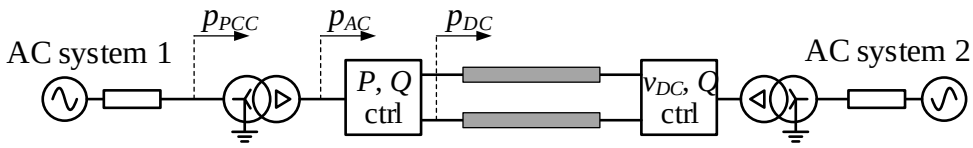
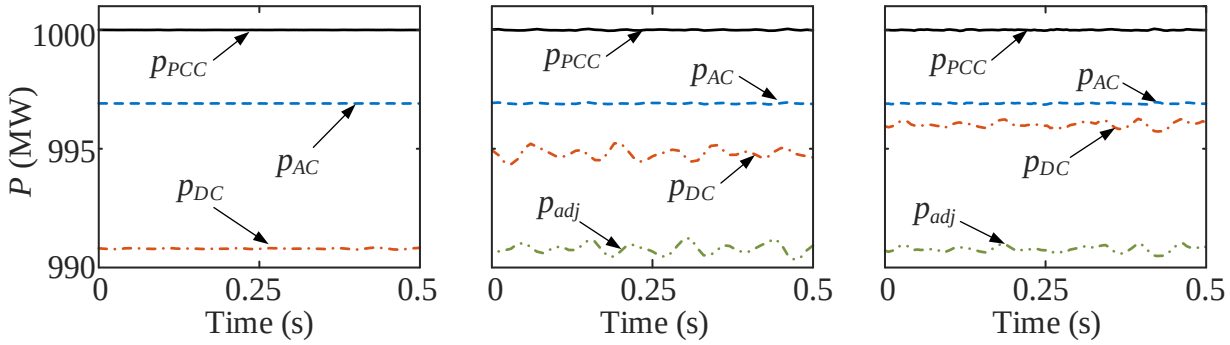


Figure 6.5 Measurement points of the transmitted active power



a) DEM b) Classical-AEM-1 c) Classical-AEM-2

Figure 6.6 Transmitted active power at different measurement points

6.4.2 Validation of analytical formulas

To validate the analytical expression of the spurious power, the measured and calculated time-domain waveforms of Δp in the upper arm of phase A at MMC1 are shown in Figure 6.7. The measured values correspond to (6.4), and the calculated values correspond to (6.32) for the Classical-AEM-1, and to (6.37) for the Classical-AEM-2. Instantaneous conduction power losses $R_{arm}\, i_{arm}^2$ are shown for comparison. The measured and calculated spurious powers match each other well and their values are considerably higher than conduction losses.

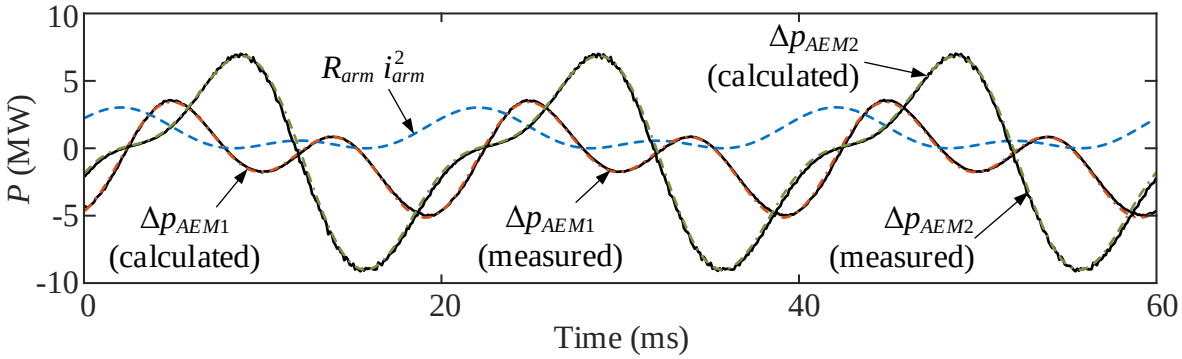


Figure 6.7 Spurious power with classical AEMs

Table 6.1 and Table 6.2 show the amplitudes of Δp harmonics measured and calculated using (6.29)–(6.31) and (6.34)–(6.36) for different power angles $\varphi_{ref} = \varphi_v - \varphi_i$ at the PCC1. Analytical calculations match well simulation results, which validates the analytical expressions. The total spurious power of the Classical-AEM-2 for $\varphi_{ref} = -30°$ ($-2.15\,\text{MW} \times 6 = -12.9\,\text{MW}$) exceeds normal converter station losses, thus making the converter generate power instead of consuming it.

Table 6.1 Spurious power in the Classical-AEM-1 (MW)

Operation mode	**Measures**			**Calculation**		
	$\Delta p_{AEM\,1_0}$	$\lvert\Delta p_{AEM\,1_1}\rvert$	$\lvert\Delta p_{AEM\,1_2}\rvert$	$\Delta p_{AEM\,1_0}$	$\lvert\Delta p_{AEM\,1_1}\rvert$	$\lvert\Delta p_{AEM\,1_2}\rvert$
$\varphi_{ref} = +30°$	0.56	1.50	2.36	0.54	1.50	2.31
$\varphi_{ref} = 0°$	-0.68	2.15	2.70	-0.69	2.15	2.69
$\varphi_{ref} = -30°$	-1.92	2.18	2.94	-1.93	2.18	2.96

Table 6.2 Spurious power in the Classical-AEM-2 (MW)

Operation mode	**Measures**			**Calculation**		
	$\Delta p_{AEM\,1_0}$	$\lvert\Delta p_{AEM\,1_1}\rvert$	$\lvert\Delta p_{AEM\,1_2}\rvert$	$\Delta p_{AEM\,1_0}$	$\lvert\Delta p_{AEM\,1_1}\rvert$	$\lvert\Delta p_{AEM\,1_2}\rvert$
$\varphi_{ref} = +30°$	0.30	6.81	2.38	0.24	6.89	2.31
$\varphi_{ref} = 0°$	-0.87	6.58	2.61	-0.94	6.49	2.69
$\varphi_{ref} = -30°$	-2.15	6.38	2.79	-2.18	6.21	2.96

The same operating conditions are used to demonstrate linear dependency of the spurious power on Δt, Figure 6.8. Measured values (markers) match analytical predictions (lines) for both classical AEMs. Due to several simplifications for $\delta p_{AEM\,2}$ in the Classical-AEM-2 (see section 6.1.2), a slight difference is observed between the measured and analytical values with larger time-steps.

Considering results shown in Table 6.1, Table 6.2, Figure 6.7, and Figure 6.8, it is clear that with both classical AEMs the effects of spurious power are significant and must be removed.

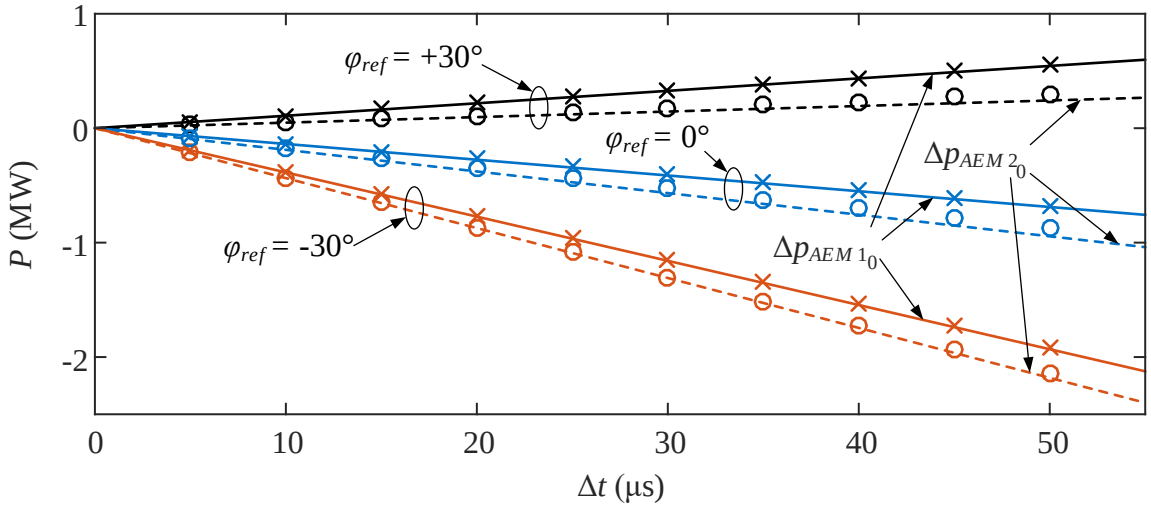


Figure 6.8 Effect of Δt on $\Delta p_{AEM\,1_0}$ and $\Delta p_{AEM\,2_0}$ in different operating conditions

6.4.3 Validation of the proposed solutions

6.4.3.1 Steady-state behavior

To validate steady-state behavior of all proposed solutions and to evaluate their effects on the spurious power, instantaneous values of the spurious power in the upper arm of phase A at MMC1 are shown in Figure 6.9 and Figure 6.10. The solutions are separated into two groups according to the magnitude of the remaining spurious power. In case of time-step reduction, the Δt used for the Classical-AEM-1 is 1.5 μs, as calculated with (6.40). For the Classical-AEM-2, (6.41) provides $\Delta t = 0.43\,\mu s$ but in the simulation the value of 0.5 μs is sufficient.

With all proposed solutions, spurious power is lower than normal conduction losses (which can be as high as 3 MW peak, see Figure 6.7). However, neither significant time-step reduction nor extrapolation eliminates spurious power completely. Variable resistance AEM provides the most

accurate results, the spurious power is equal to zero. Equivalent voltage source AEM reduces the spurious power below 1 kW.

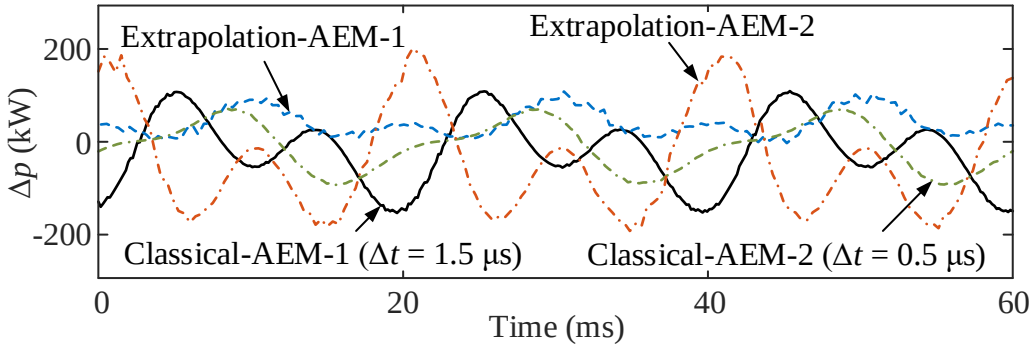


Figure 6.9 Spurious power with different elimination methods (scale 1)

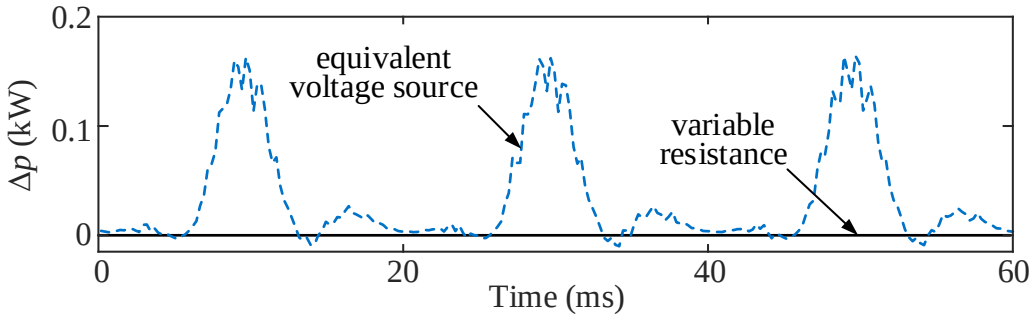


Figure 6.10 Spurious power with different elimination methods (scale 2)

6.4.3.2 Transient behavior

A 200 ms three-phase-to-ground fault at 0.4 s at the PCC1 is used to validate transient behavior of all proposed solutions. Classical AEMs are also considered for comparison. Fault resistance is 0.5 Ω. The transient waveforms obtained with the DEM are taken as a reference.

Arm voltage of phase-A upper arm of MMC1 is shown in Figure 6.11 to Figure 6.13: both extrapolation AEMs exhibit high spikes: 25 kV at 0.4387 s (zoom 1, Figure 6.12) and 180 kV at 0.4526 s (zoom 2, Figure 6.13). These moments correspond to sudden changes in the reference values in the control system. Another adverse effect of extrapolation AEMs in Figure 6.13 is that v_{arm} becomes significantly negative (-18 kV), which is not realistic for MMCs with half-bridge SMs because negative polarization of such SMs would activate antiparallel diodes.

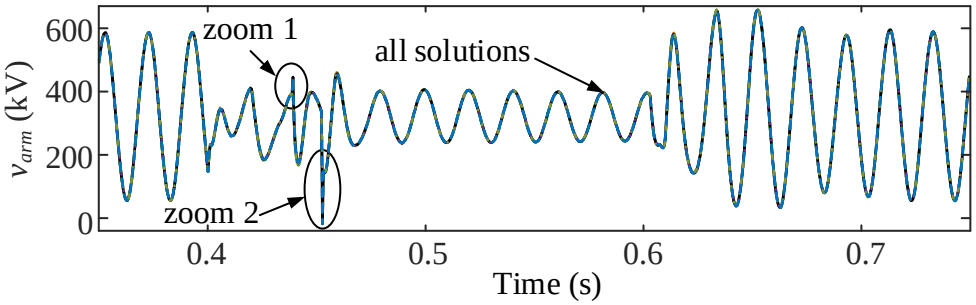


Figure 6.11 Arm voltage during transient with different elimination methods

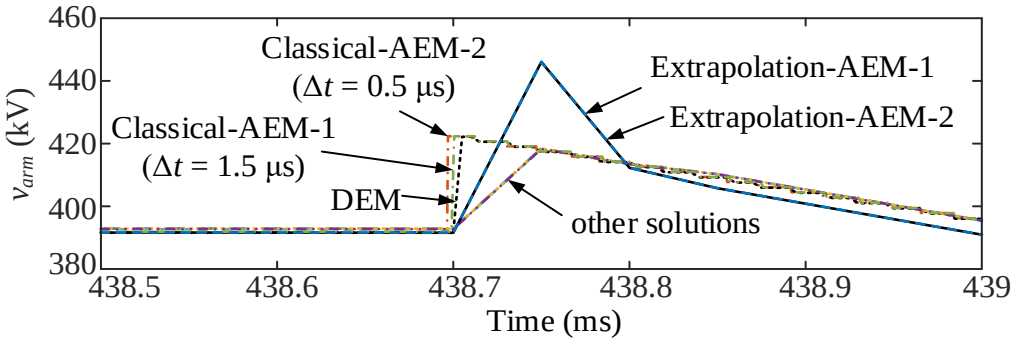


Figure 6.12 Arm voltage during transient with different elimination methods (zoom 1)

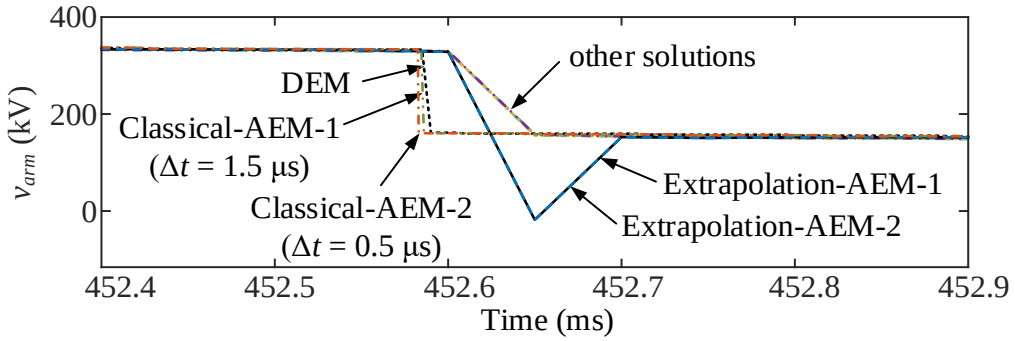


Figure 6.13 Arm voltage during transient with different elimination methods (zoom 2)

Table 6.3 compares the maximal relative deviation of the DC voltage, arm voltage, and capacitor voltage in the upper arm of phase A of MMC 1 during the same simulation with various models. As in [122], relative deviation is computed by dividing the absolute difference between the tested model and the reference by the nominal value of the signal. All models except extrapolation AEMs do not significantly deviate from the reference. Highest deviations are observed in the values of arm voltage. The most accurate match is obtained with time-step reduction because higher-frequency transients can also be represented with such small time-step.

Table 6.3 Maximum relative error with different models

Model	v_{arm} **(%)**	v_{Ctot} **(%)**	v_{DC} **(%)**
Classical-AEM-1 (50 µs)	2.43	1.29	0.66
Classical-AEM-2 (50 µs)	2.43	1.40	0.64
Classical-AEM-1 (1.5 µs)	0.72	0.18	0.19
Classical-AEM-2 (0.5 µs)	0.72	0.18	0.19
Extrapolation-AEM-1	27.79	0.51	0.35
Extrapolation-AEM-2	27.79	0.51	0.35
Variable resistance AEM	2.42	1.18	0.65
Equivalent voltage source AEM	2.42	1.18	0.62

6.4.4 Computing times

To compare computing times of various models, the HVDC link is simulated during 1 s in steady-state conditions. Results are shown in Table 6.4. The reference computing time is taken as the one of the classical AEM 1. Execution time of the DEM is also shown for comparison.

Both classical AEMs have almost identical computing times. Reducing the time-step considerably slows down the simulation, computing times are comparable to that of the DEM. The extrapolation AEMs are only slightly slower, less than 6 % difference compared with the reference. This is due to the presence of additional control blocks. The variable resistance AEM has longer execution time due to the need to refactor the MNE (30% increase in simulation time). The equivalent voltage source AEM is faster than the variable resistance AEM but still about 10% slower than the reference.

Table 6.4 Computing times with different models

Model	**Computing time (s)**	**Computing time (%)**
Classical-AEM-1 (50 µs)	2.02	100.0 (reference)
Classical-AEM-2 (50 µs)	2.05	101.5
Classical-AEM-1 (1.5 µs)	46.99	2324.3
Classical-AEM-2 (0.5 µs)	140.79	6963.4
Extrapolation-AEM-1	2.10	103.9
Extrapolation-AEM-2	2.14	105.8
Variable resistance AEM	2.69	132.9
Equivalent voltage source AEM	2.28	112.8
DEM (5 µs)	63.75	3152.9

6.5 Conclusion

The analysis of the origin of the spurious power generated in the arm equivalent model implemented in control blocks of an EMT simulation software demonstrates that such spurious power is caused by the delays present in the controlled voltage and current source blocks of the software. This causes the electrical network and AEM equations to be solved independently from each other. Derived analytical equations for the two considered implementations of the AEM use the values of AC and DC side steady-state currents and voltages. Harmonic analysis validated by the simulation results shows three components of the spurious power: constant, fundamental frequency, and double fundamental frequency. The oscillating components cancel each other inside the converter during normal operation, whereas the constant part has visible effects outside the converter and disrupts its power balance: depending on the simulation conditions, spurious power can exceed converter station losses, thus making the converter generate power instead of consuming it.

Steady-state performance of the proposed solutions is satisfactory regarding the mitigation of the spurious power impact on the simulation, however time-step reduction requires significant increase in computing times for both classical AEMs. Transient behavior performance analysis demonstrates that extrapolation-based solutions provide unrealistic spikes in the values of arm voltage. Overall, only two solutions do not have significant disadvantages: the variable resistance AEM and equivalent voltage source AEM. The former eliminates the spurious power completely on the expense of MNE matrix refactorization at each time-point, which increases computational burden. The latter allows to keep the MNE matrix constant, but some negligible amounts of spurious power are still present.

CHAPTER 7 CONCLUSION

7.1 Thesis summary

This thesis focuses on the modeling of HVDC equipment in electromagnetic transient simulations. More particularly, on the modeling of hybrid modular multilevel converters for offline simulations. The contributions to the two primary aspects have been considered: results accuracy and simulation time.

The thesis starts with a review of the main DC grid equipment and their modeling aspects, including the AC/DC converters, DC circuit breakers, DC/DC converters, and transmission lines and cables. It is concluded that a significant impact can be achieved by improving the modeling of modular multilevel converters.

The hybrid MMC models with different levels of detail and corresponding controls are then presented and compared. The more detailed models are able to more accurately replicate the behavior of the detailed reference model but require more simulation time. The hypotheses taken to build each model define the conditions in which they can be used.

Initialization of two MMC models is then researched in the thesis as a means to remove the transient in the beginning of the EMT simulations, which results in significant reduction of computing time. An initialization method is proposed, that requires the knowledge of the steady-state voltages and currents at the AC and DC sides of the MMC, which can be obtained from a power-flow solution of the network. A system of five complex nonlinear equations that link the voltage and current signals to the steady-state harmonics of the arm switching function and capacitor voltage is established for each converter arm. It is proposed to solve the system of equations with a fixed-point algorithm. The effectiveness of the method is demonstrated at different levels of detail, from the grid-level to the SM-level variables and the time-gains are calculated. The time-gains depend on the proportion of the initialization transient to the transient under study.

Next, the thesis extends the proposed initialization method to the time-domain model relaxation method, which is useful to accelerate simulations by dynamically changing the computational burden of the MMC model. The methods to seamlessly transition between the AVM, AEM, and DEM are developed. To facilitate the switching to the average value model, two new AVMs are

proposed. In these models, the AC and DC electrical circuits are interleaved, contrary to the conventional AVM. This allows to keep the arm current flowing through the inductances uninterrupted. It is also proposed to use a memory pointer exchange between the DEM and CBA blocks, which allows to read variables directly from the memory. This drastically reduces the number of control signals managed by the EMT simulation software and results in the simulation time reduction. The new models and transition methods are validated in various conditions and the acceleration factors are calculated. It is found that the acceleration factors are case-dependent and can be 10 or above depending on the design.

Parallelization of the internal calculations of the DEM is researched as a means to accelerate offline EMT simulations. A parallelization algorithm is proposed that computes the internal variables of each MMC arm on a dedicated CPU core. The same approach is applied to the CBA blocks. The memory pointer exchange is also applied to further accelerate simulations. The parallelized model is found to produce slightly different results from the default serial computation case, with the relative difference in the order of 10^{-12}. The acceleration factors are impacted by the number of SMs in the simulated MMCs and the number of MMCs in the design. The higher these numbers are, the higher are the acceleration factors. Since the converter control system can be implemented in the form of a black box, it is not always possible to parallelize the CBA, so the acceleration resulting from the DEM-only parallelization is also compared, which is found to be less significant compared to the DEM and CBA parallelization but considerable nonetheless.

The contribution to the accuracy improvement in this thesis lays in the power balance analysis of the arm equivalent model. It is demonstrated that if the AEM is implemented using control system blocks in an EMT simulation software, its equations are not solved simultaneously with the surrounding electrical network equations, which results in some spurious power generation or consumption. Analytical formulas of the spurious power are derived for the two implementations of the AEM, which allow to find the value of such power in various operating conditions. Several methods to eliminate this power are proposed, including new AEM models. The proposed methods are compared in steady-state and transient simulations and it is found that only two solutions have satisfactory performance: the variable resistance AEM and the equivalent voltage source AEM.

7.2 Future work

Future research in the area of electromagnetic transient simulations of HVDC systems can focus on other types of DC grid equipment that have been considered in the literature review part of the thesis. This includes the modeling of DC circuit breakers and DC/DC converters.

Regarding the initialization, the inclusion of energy balancing controls into the initialization method can be an interesting research topic, as well as the initialization of multiterminal DC grids consisting of multiple MMCs and other converters.

An automatic model selection algorithm for the adaptive MMC model can be researched, which could consider various signals available in the MMC. The adaptive model concepts presented in this thesis could be applied to other types of electrical equipment models, which would make it possible to change the level of details of the whole simulated system at once and thus provide even higher acceleration.

Parallelization of the DEM computations on massively parallel architectures, such as the graphics processing units can offer the possibilities for additional acceleration of EMT simulations and requires further research.

The concepts presented in this thesis for the offline simulations can be transposed to the real-time simulation. For example, the initialization of MMC models in the real-time simulations or transitioning between MMC models with different levels of detail. The latter can be especially advantageous on the simulators with a limited number of cores where only a fraction of the whole grid can be modeled with a high level of detail.

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APPENDIX A – LIST OF PUBLICATIONS

The following is the list of publications derived from this Ph.D. project.

Journal publications

A. Stepanov, H. Saad, U. Karaagac, and J. Mahseredjian, "Spurious Power in Modular Multilevel Converter Models," under review.

A. Stepanov, J. Mahseredjian, U. Karaagac, and H. Saad, "Adaptive Modular Multilevel Converter Model for Electromagnetic Transient Simulations," under review.

A. Stepanov, H. Saad, U. Karaagac, and J. Mahseredjian, "Spurious Power Losses in Modular Multilevel Converter Arm Equivalent Model," *IEEE Transactions on Power Delivery*, vol. 35, pp. 205-213, 2020.

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A. Stepanov, H. Saad, U. Karaagac, and J. Mahserdjian, "Spurious Power Generation in Arm Equivalent Model Variants of Modular Multilevel Converter," *International Conference on Power Systems Transients (IPST 2019)*, Perpignan, France, 2019.

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APPENDIX B – MMC-HVDC LINK PARAMETERS

HVDC link parameters

The default MMC-HVDC link parameters shown in Figure B.1 are listed in Table B.1.

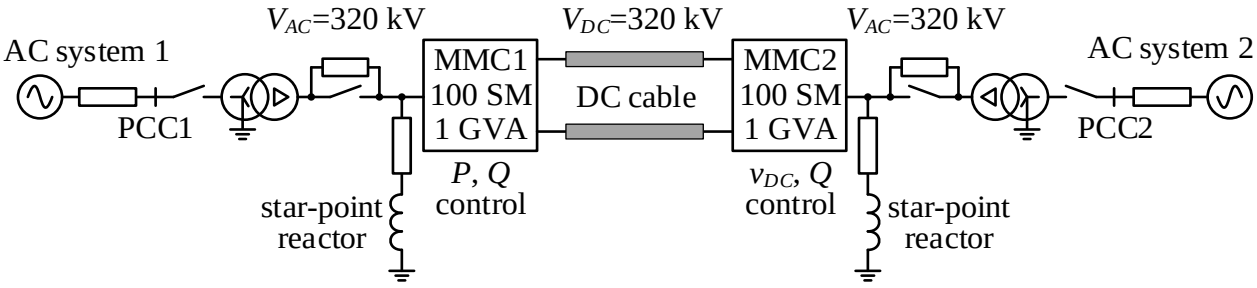

Figure B.1 Point-to-point MMC-HVDC link

Table B.1 System parameters

Parameter	**Nominal value**	**Symbol**
Grid frequency (both grids)	$2\pi \times 50$ rad/s	ω
Grid voltage (both grids)	400 kV	
Grid short-circuit level (both grids)	10 GVA	
MMC AC voltage (both stations)	320 kV	V_{AC}
MMC DC voltage (both stations)	640 kV	V_{DC}
Nominal converter power (both stations)	1000 MW	
Number of SMs per arm (HB / FB)	100 (20 / 80)	N_{SM} (N_{HB} / N_{FB})
ON- and OFF-state resistance of IGBTs	1 mΩ / 1 MΩ	R_{ON} / R_{OFF}
Charging resistance (both stations)	1 kΩ	
Arm inductance	0.15 pu	L_{arm}
Transformer inductance	0.18 pu	L_{trfo}
Capacitor energy	40 kJ/MVA	
Star-point reactor resistance	7700 Ω	
Star-point reactor inductance	6500 H	

DC cable parameters

The underground DC cable is shown in Figure B.2 and its parameters are listed in Table B.2.

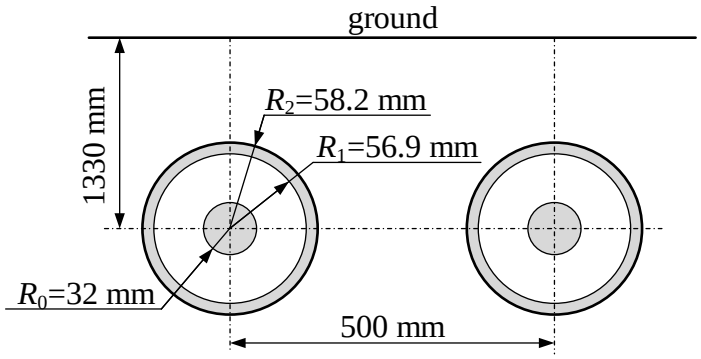

Figure B.2 DC cable configuration

Table B.2 Cable parameters

Parameter	**Nominal value**	**Symbol**
Cable length	70 km	
Relative permeability (conductor and insulation)	1	
Insulation loss factor	0.0004	
Insulation relative permittivity	2.5	
Conductor radius	32 mm	R_0
Conductor resistivity	1.72e-8 Ω m	
Shield inner radius	56.3 mm	R_1
Shield outer radius	58.2 mm	R_2
Shield resistivity	2.83e-8 Ω m	
Earth resistivity	100 Ω m	
Model	Wideband	