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Control of Four-Wire Inverter-Interfaced DGs for Accurate Fault Type Classification

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Control of Four-Wire Inverter-Interfaced DGs for Accurate Fault Type Classification

By

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DECLARATION OF ORIGINALITY

I. Co-Authorship

I hereby declare that this thesis incorporates material that is the result of joint research. Dr. Maher Azzouz contributed with overall supervision with the material listed in Chapters 3 and 4.

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II. Publication

A journal paper has been written using the research findings of this thesis and is going to be under review; details are below.

Thesis Chapters	Publication title/full citation	Publication status
Chapter 3 and 4	Medhat Wael, Azzouz Maher, "Control of Four-Wire Inverter-Interfaced DGs for Accurate Fault Type Classification."	To be submitted to an IEEE journal.

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ABSTRACT

Inverter-interfaced distributed generators (IIDGs) generate fault currents that are different from those generated by conventional synchronous generators (SGs). As a result, commercial relays—that utilize current-angle-based phase selection measurements—misidentify faulty phase(s), which adversely impact the grid resiliency and reliability. In this thesis, a new control scheme is proposed to regulate the sequence components of the IIDG currents during unbalanced faults to ensure accurate fault type classification by commercial relays. The proposed controller controls the positive-sequence and negative-sequence currents in the dq-frame with a decoupled synchronous reference frame (DDSRF) based phase-locked loop (PLL) for components extraction and synchronization. It also uses a second order generalized integrator (SOGI) based PLL to synchronize the zero-sequence components. This scheme forces the angles of the negative-sequence and zero-sequence fault IIDG currents to behave like those of an SG while preserving the inverter's current limits. This leads to proper fault type classification. The proposed control scheme pertains to three-wire IIDGs as well as four-wire IIDGs, which are common in low-voltage distribution networks. A performance evaluation using time-domain simulations is used on a benchmark network to confirm the success of the proposed control scheme under different fault conditions.

DEDICATION

I dedicate my thesis to my parents for giving me the best education and support throughout my life. I hope that this achievement will make them proud. This thesis is also dedicated to my amazing wife for her ongoing encouragement and patience.

ACKNOWLEDGEMENTS

I am very grateful to my supervisor Dr. Maher Azzouz whose support during the past two years was above and beyond what a supervisor would do. Even during a very busy schedule, he was able to provide me with the help that I have benefited from immensely. I am honored to be examined by Dr. Narayan Kar, from who I learned the fundamentals of power systems. I want to express my appreciation to my parents, who did everything they could to provide for me and teach me how to excel in every aspect of life.

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CHAPTER 1

Introduction and Objectives

Inverter-interfaced distributed generators (IIDGs) that interface renewable energy sources (RES) into distribution networks have been increasingly installed to provide and sustain green energy systems. Conventional synchronous generators (SGs) support electricity grids by providing ancillary services, especially during faults and disturbances [1], [2]. In contrast, IIDGs generate fault currents that are different than those from SGs, which could compromise power system protection [3]. Grid codes (GCs) impose requirements on IIDGs, such as fault-ride-through (FRT) requirements, to support the grid voltage and frequency during grid faults [4], [5], which is also observed in international standards such as [6].

The concept of active distribution networks (ADNS) appeared with the ever-increasing installation of distributed generations (DGs). ADNS are distribution networks that allow bidirectional power flow in the presence of DGs. To optimize power distribution and mitigate costs by increasing efficiencies, many papers were concerned with the planning of ADNS [7]–[9]. Microgrids are components of these networks that contain DGs and storage units; they are also capable of switching between grid-connected and islanded modes. Due to the presence of DGs, the current signatures are different than those of SGs, which commercial relays design is based upon. The change of the current signatures makes microgrid protection challenging [10]. A reliable and resilient network should be able only to trip faulty phase(s) during unbalanced faults, which calls out for selective phase tripping by protection relays. Current-angle-based phase selection measurements (PSMs), i.e., utilized by commercial relays [11], [12], are considered most effective in identifying fault types. They utilize the relative angles between the superimposed sequence currents, i.e.,

$$\begin{cases} \delta^{+} = \angle\Delta I^{-} - \angle\Delta I^{+} \\ \delta^{0} = \angle\Delta I^{-} - \angle\Delta I^{0} \end{cases} \tag{1.1}$$

δ^{+} and δ^{0} where the superscripts $+$, $-$, and 0 refer to the positive, negative, and zero-sequence quantities, respectively, and Δ indicates a superimposed quantity [13]. Figure 1.1 displays the detection zones for δ^{+} and δ^{0} at different unbalanced faults, where each zone is confined by the upper and lower limits. For instance, δ^{+}should lie close to zero within $\pm$ 15 degrees, as shown in Figure 1.1(a) to identify an AG fault. Meanwhile, to classify an AG fault using δ^{0}, it should lie close to zero within $\pm$ 30 degrees, as shown in Figure 1.1(b). However, δ^{+} should be used in conjunction with δ^{0} to differentiate between AG and BCG faults and other similar fault patterns

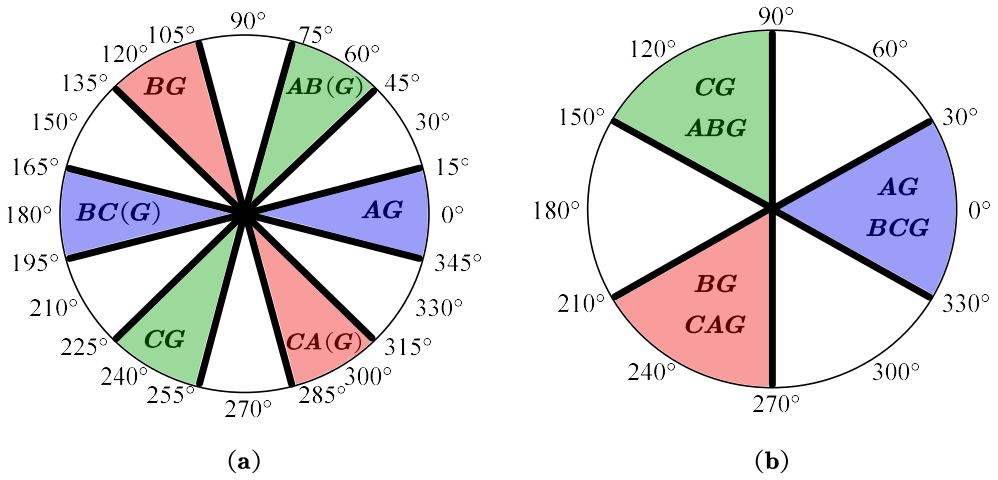

Figure 1.1: Fault type zones for: (a) δ^{+}, (b) δ^{0}.

as δ^{+} is affected by the IIDG power factor and fault resistance, and that is why reliance is mainly on δ^{0} which is not affected by the IIDG power factor and fault resistance. Alternatively, δ^{0} can be supported by estimated fault resistances. If the estimated fault resistance for single-line-to-ground (SLG) faults, R_{lg}, is smaller than that for line-to-line-to-ground (LLG) faults, R_{llg}, then the fault type is AG and vice versa

1.1 Research Objectives

This thesis focuses on developing a control scheme for IIDGs to aid the existing relays to correctly classify the fault type by regulating the inverter's sequence currents during faults. The focus will be given to understand the impact of zero-sequence currents on voltage source converters (VSCs), and hence IIDGs. Existing literature often disregards the effects of zero-sequence currents due to delta-star grounded transformers that open the zero-sequence circuit. However, transformerless or four-wire IIDGs are gaining popularity, especially in low-voltage distribution systems [14]. The popularity of four-wire DGs is due to having either many single-phase loads in residential low-voltage or low voltage loads that do not require transformers. Thus, IIDGs can change the zero-sequence current flow in distribution systems and lead to maloperation of commercially used phase selection methods.

The main objective of the proposed controller is to regulate the positive-sequence, negative-sequence, and zero-sequence currents by injecting sequence currents that mimic those of a conventional SG. The control strategy applies to transmission systems as well as distribution systems. After satisfying the main objective, another secondary objective is achieved by mathematically explaining the relationship between the sequence currents and the phase currents to comply with the IIDG's thermal limits.

1.2 Thesis Approach

1. Literature survey: a literature survey related to controlling the IIDG sequence currents and phase selection is conducted.

2. System modeling: a VSC model is used similar to the one in [15] is modified to account for the negative-sequence and zero-sequence circuits along with the original positive-sequence-circuit.
3. Proposed solution: a complete control solution was conceptualized then implemented by regulating the positive-sequence and negative-sequence circuits in the dq-frame with a decoupled synchronous reference frame (DDSRF)-based phase-locked loop (PLL) to extract the sequence components and synchronize the phase angle with the grid. Proportional integral (PI) controllers were then tuned to control the circuits. Moreover, a SOGI-based PLL was used to control the zero-sequence circuit for its ease of implementation. Proportional resonant (PR) controlled was then tuned to control the circuit.
4. Performance evaluation: The theory of operation was validated using simulation results on the CIGRE low-voltage benchmark microgrid system.
5. Conclusion and future work: A conclusion was drawn based on the steps, and the future work was outlined.

1.3 Thesis Outline

An Introduction is given in Chapter 1 that provides an overall understanding of the problem statement and the relating work in literature. Chapter 2 introduces a background of the conventional VSC control and details the literature survey. Chapter 3 models the system and proposes the control scheme for Transformerless IIDGs. Chapter 4 presents a practical test system to validate the proposed control algorithm. Finally, Chapter 5 discusses the general conclusions and provides potential future work.

CHAPTER 2

Background and Literature Survey

2.1 VSC Topology

This thesis focuses on the two-level three-phase VSC topology, which is depicted in Figure 2.1. The VSC consists of three legs for each phase; every leg consists of a half-bridge converter connected in parallel with a common direct current (DC) voltage source. The alternating current (AC) terminal voltages V_{ta} , V_{tb} , and V_{tc} can be switched to magnitudes of either V_p or V_n which are normally $V_{DC/2}$ and $-V_{DC/2}$ respectively.

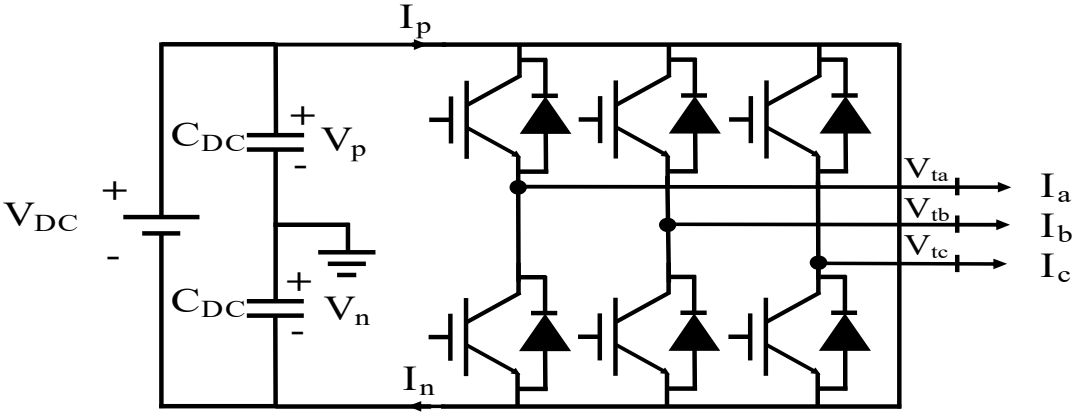

Figure 2.1: Two-Level Three-phase VSC.

To form an understanding of how the two-level VSC works, it is essential to start with the basic block that is the ideal half-bridge converter shown in Figure 2.2. The principle of operation can be understood from the direction of the current I and the switching commands for the transistors. Q_1 and Q_4 are the upper and lower transistor respectively, whereas D_1 and $D_4$are the upper and lower diode respectively that form the power electronic switch. During the positive cycle and

when Q_1 is on Q_4 is off, V_t is equal to $V_{DC/2}$ and D_4 is reversed biased and therefore, I must flow through Q_1. Whereas when Q_1 is off and Q_4 is on, I flows through D_4

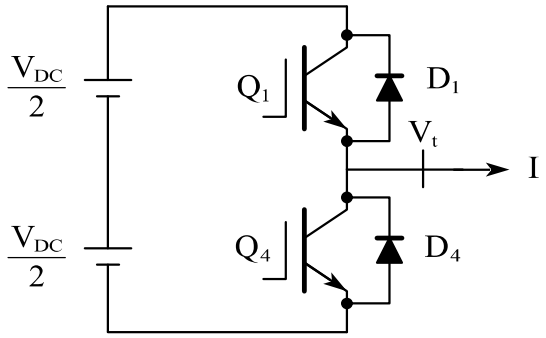

Figure 2.2: Ideal half-bridge Converter.

since the current through D_1 cannot be negative and V_t is equal to $-V_{DC/2}$. Similarly, as presented for the positive cycle case, during the negative cycle and when Q_1 is on Q_4 is off, I flows through D_1 and V_t is equal to $V_{DC/2}$. Whereas when Q_1 is off and Q_4 is on V_t is equal to $-V_{DC/2}$.

2.2 Basic Control of VSCs

A brief about space phasors and two-dimensional frames is required to understand and simplify the control process. For three-phase VSC systems, voltage or current commands are sinusoidal signals, which causes the design of a compensator to be complex as it is implemented for each phase separately. To tackle this issue, two-dimensional frames are introduced. Figure 2.3 shows space-phasor in the complex plane. The vector $f(t)$ represents a three-phase sinusoidal function. It also rotates counterclockwise with an angular speed of ω, and it has an initial phase angle of θ. A closed form of the phasor is shown in (2.1).

$$f(t) = \boldsymbol{F}(t) * e^{j\theta} * e^{j\omega t} \tag{2.1}$$

where $f(t)$ is the amplitude as a function of time, $e^{j\theta}$ is the initial phase shift and e^{jwt} adds the effect of rotating the vector $\boldsymbol{F}(t)$ counter-clockwise which is a sinusoidal signal. Figure 2.3 depicts $\boldsymbol{F}(t)$ being constant such as in the case of a conventional phasor; however, $\boldsymbol{F}(t)$ can also vary with time. Changing the amplitude and phase angle of the $f(t)$ results in a change of the three-phase signal; however, the realization of compensator with such characteristics is difficult due to the presence of the imaginary component $e^{j\theta}$. To help with this issue, mapping to a real-valued function is achieved using the $\alpha\beta$ frame, it resolves $f(t)$ into two components real and imaginary. The aforementioned frame resolves the issue of having to deal with imaginary functions in the compensator; it also reduces the control variables to only two variables. However, the commanding signals are still sinusoidal, which causes the compensator to be of a higher order. The dq frame resolves the issue of having to deal with complex compensator designs as the commanding signals assume a DC form rather than the sinusoidal form. Figure 2.4 shows the synchronous dq frame overlaid on the stationary $\alpha\beta$ frame. $f(t)$ can be represented in the dq frame from the $\alpha\beta$ frame, as shown in (2.2).

$$f_d + jf_q = \left(f_\alpha + jf_\beta\right)e^{-j\varepsilon(t)} \tag{2.2}$$

where the angular component of $\varepsilon(t)$ rotates with the same angular speed of vector $f(t)$ (which represents the three-phase signal) by the action of a PLL, then f(t) appears to be stationary with respect to the rotating dq frame hence appears in DC form. The realization of a compensator is then significantly simplified with a simple PI controller. The overall control system in the dq frame is shown in Figure 2.5, where the feed-forward signal is for start-up transient compensation. In the absence of the feed-forward, the following scenario takes place.

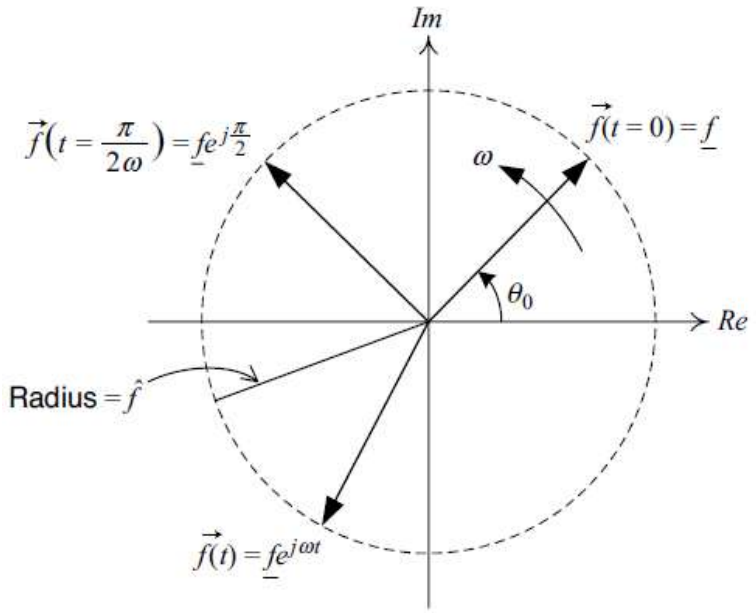

Figure 2.3: Space-phasor, reprinted from [15].

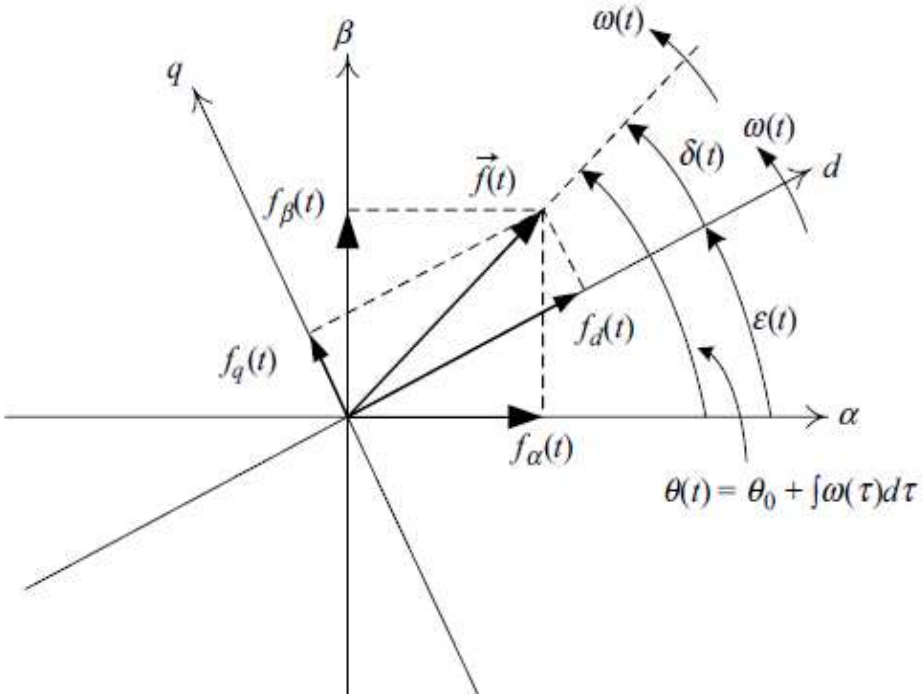

Figure 2.4: Coordinate system, reprinted from [15].

On start-up, the insulated-gate bipolar transistors (IGBTs) are blocked, and the terminal voltage on the inverter is zero. Meanwhile, the AC system voltage is positive, so the current becomes negative immediately and spikes to a large value until the compensator regulates it, which is avoided with the feed-forward compensation. To synchronize the phase angle of the VSC terminal voltage with the phase angle of the AC system, $\varepsilon(t)$ is equated to the angle of the grid voltage using a PLL technique which forces the q-axis component of the grid voltage to be zero. This causes the real and reactive power components to become proportional to the d and q axes, respectively, and thus, independent control of real and reactive powers can be achieved.

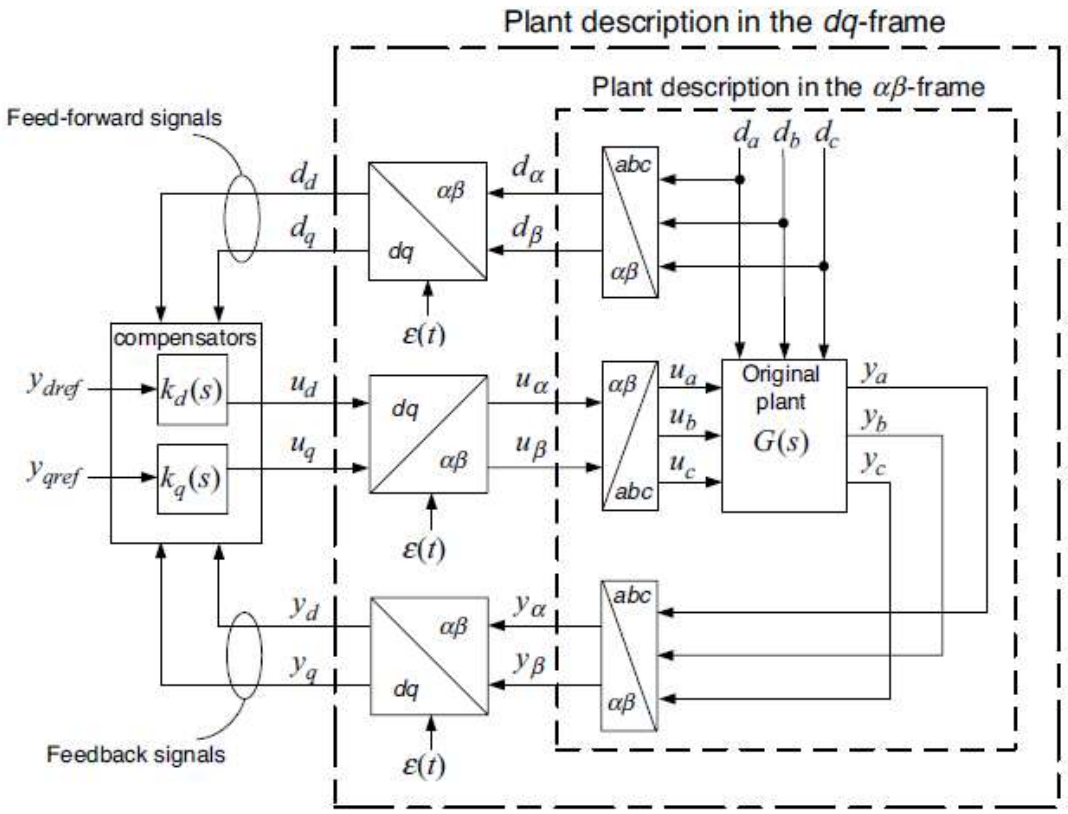

Figure 2.5: Conventional control system in the dq frame, reprinted from [15].

A more detailed control system schematic is shown in Figure 2.6. It consists of outer and inner control loops. The dq frame outer control loops utilize identical PI compensators. The outputs of these compensators feed the inputs of the slower and inner control loops. The VSC then scales those signals up by a factor of $V_{DC/2}$ to generate the VSC dq frame terminal voltages that, in turn, control the VSC dq frame currents and, eventually, the active and reactive power. Another family of VSC known as Controlled DC-Voltage Power Port has recently gained popularity [15]. This family is more suited to interface RES into the grid. In that case, an additional control loop is added to regulate the DC-bus voltage and, eventually, the active power reference, as shown in Figure 2.7. The conventional control system analysis only regulates the positive-sequence components of the inverter's currents and voltage, which will be illustrated to be inefficient during faults to guarantee accurate phase selection.

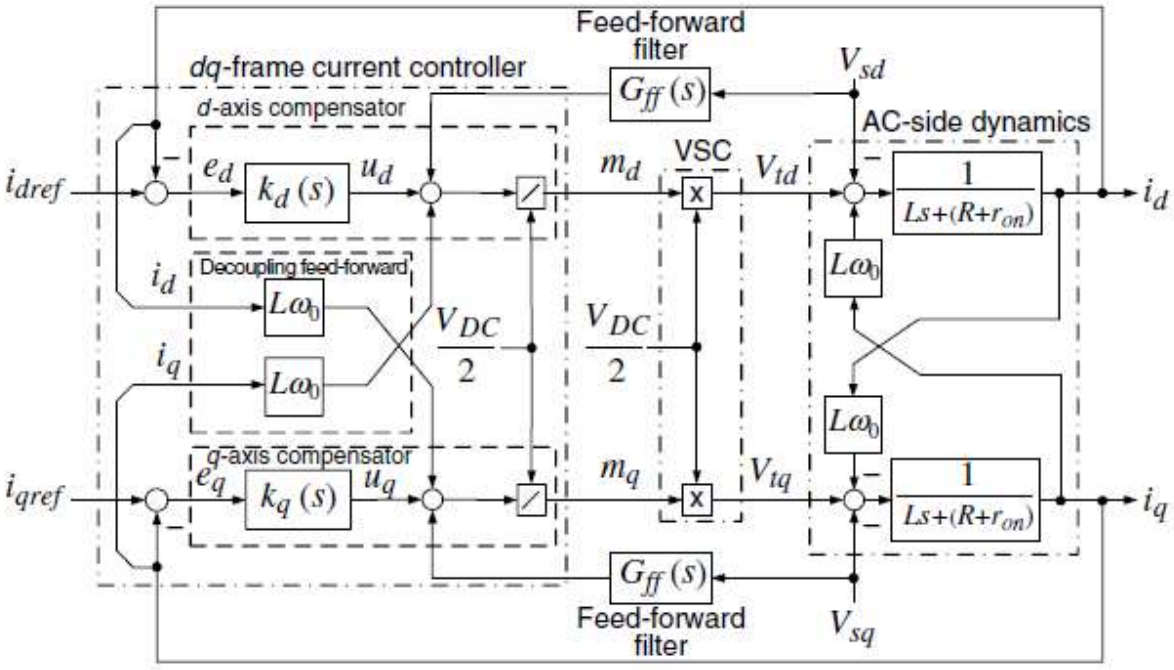

Figure 2.6: Detailed control system schematic, reprinted from [15].

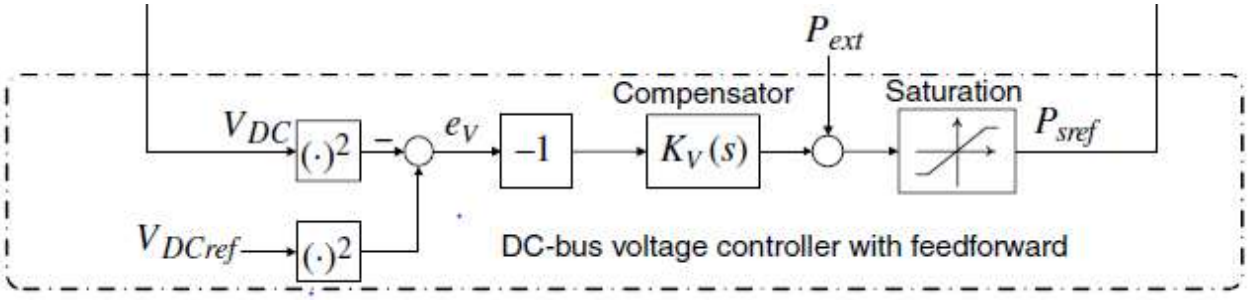

Figure 2.7: DC-bus voltage controller, reprinted from [15].

2.3 Literature survey

The ever-increasing amount of IIDGs connected to power systems leads a lot of researchers to investigate the importance of understanding the different behavior of IIDG under unbalanced faults. The IIDG behavior during faults is mainly governed by its controller objectives. IIDGs are required to provide ancillary services like conventional generation does, which is in the form of FRT capability and grid voltage support. An FRT capability defines voltage limits against time profiles to avoid unnecessary disconnection by supporting the grid voltage to mimic the conventional generation. The voltage support is achieved by injecting reactive power under grid faults according to grid requirements that were shown to lack negative-sequence currents.

A main classification of the IIDG control objective is found in [1], which classifies the control objectives into two groups: power-characteristic-oriented control strategy and voltage-support-oriented control strategy. Under the first group, different objectives can be categorized, such as constant active power, constant reactive power, balanced current control, and flexible oscillating power. Under the second group, two control strategies, namely semi-flexible and flexible, are used to adjust the relationship between positive- and negative-sequence powers, where the

selection of control coefficients was subjected to certain constraints. The classification fails to include another family of objectives that address phase selection problems.

The current angle-based classifiers for a long time were considered the most effective tool for the phase selection. However, these classifiers are effective when the system is powered only by SGs. It is revealed in [16] that these classifiers fail to properly identify the fault type in the presence of IIDGs as their fault currents primarily depend on the control scheme as opposed to the fault properties, which is the case for SGs. Also, two new voltage-based classifiers are proposed in [16]; however, the solution dealt with the problem from the relay side with no provisions on the inverter control. These classifiers necessitate not only upgrading the relay software but also equipping relays with voltage transducers, which may add extra cost. An early control scheme was proposed in [17], which pioneered dual current controllers (DCC) to control the positive-sequence as well as the negative-sequence circuits that fulfilled its control objectives in eliminating power oscillations. However, it did not control the negative-sequence current to mimic that of an SG.

Moreover, other control methods have been proposed in [18]–[20], but none of these control methods discussed the phase selection problem. More recent efforts in [3], [21], [22] propose new DCCs that make the negative-sequence circuit of an IIDG equivalent to a controllable voltage source behind a virtual impedance to imitate the behavior of an SG, which was successful. However, these DCCs are only applicable for three-wire IIDGs because they disregarded the zero-sequence circuit. Zero-sequence components were controlled in [23], [24] to provide more degrees of freedom to achieve higher inverter performance. However, these controllers did not address the phase selection issue and its impact on the protection system.

2.3.1 Dual current control for power-oriented objectives

Grid faults and voltage unbalance conditions in a three-phase system causes performance deterioration of VSCs. That performance deterioration is in the form of undesired 120-Hz ripples in the DC voltage and oscillations in the active power as well as the reactive power. The problem stems from not controlling both positive- and negative-sequence currents simultaneously.

Several control schemes were proposed in the literature to tackle this problem, known as DCCs [17], [20], [25], [26]. These controllers regulate the positive- and negative-sequence currents each in their synchronous reference frame (SRF), i.e., the dq-frame, which rotates at the same frequency but in a different direction. In the positive SRF, the positive sequence current appears as DC quantity in its reference frame, but as a 120-Hz sinusoidal quantity in the negative sequence frame. The opposite was also found to be true for the negative-sequence current. The presence of the AC quantity complicates the control design because it requires a large bandwidth to track the 120 Hz command signals. These proposed dual current controllers applied a 120-Hz notch filter to cancel the 120-Hz components in both the positive and negative SRFs. The elimination of the 120-Hz components and the separation of the positive- and negative-sequence currents lead to simple controller design. Simple PI controllers were able to track the DC command signals that appeared in each of the SRFs. These control schemes met their goals with success; the results were compared to the generic control scheme, which showed better performance for the dual current control schemes. These dual current control schemes met their objectives by reducing and/or eliminating the DC ripples as well as the active and reactive power oscillations. However, the solution was tunnel-visioned and did not consider the phase selection problem. These control schemes were also designed for only three-wire systems.

2.3.2 Voltage classifiers for accurate fault phase selection

Selective phase tripping requires correct fault type identification. The authors in [16] were able to identify that current relaying protection methods such as current angle-based and magnitude-based misidentify the fault type in the presentence of IIDGs due to their different current signatures as opposed to conventional SGs. The current angle-based method uses superimposed sequence currents angles to determine the fault type shown to succeed with SGs but is not reliable in the presence of the IIDG. The deployment of excitation systems in conventional generators maintained voltage during faults, whereas for renewable-based IIDGs are typically modeled as current sources. The current characteristics of IIDGs are governed by the inverter's control objectives, which often make IIDGs inject currents different than the ones injected by SGs. On the other hand, the current magnitude-based method identifies faults by selecting the phases with the largest current magnitudes. The current magnitude-based method tends to be unreliable in the presence of IIDGs because current(s) in the healthy phase(s) could be higher than the faulted ones [27]. The current magnitude-based method is dependent on the level of reactive current during faults, which adds to its unreliability. The proposed two new fault type classifiers in [16] are robust against different values of fault resistance as well as different IIDG power factors. The new classifiers were tested under different modes and different systems with success; however, their implementation is difficult due to the need for upgrading the relay algorithms and logic circuits and equipping them with voltage transducers, which could add extra cost and complexity. The solution offered by these classifiers does not have any provision for the IIDG control and is not studied for four-wire systems.

2.3.3 Dual current control for phase selection objectives

Unlike the solution presented in the previous section, a new proposed dual control scheme solves the phase selection problem from the IIDG side rather than from the relay side. The proposed dual current control schemes, such as [3], [21], focus mainly on the current angle-based phase selection method as the primary source of relay protection for its increased reliability and robustness. The proposed dual current control scheme regulates both the positive- and negative-sequence currents simultaneously under unbalanced faults. In [21] to imitate the behavior of a conventional generation to allow for accurate phase selection, the negative-sequence circuit is modeled as a controllable voltage source behind a virtual impedance so that it injects currents like those of the conventional generations. This dual current control scheme forces the negative-sequence current to mimic the behavior of synchronous generators during asymmetrical faults. It also uses a 120-Hz notch filter to separate the positive and negative sequence components that appear as sine waves with twice the frequency in their opposite synchronous reference frames. The negative-sequence control scheme works by enforcing a zero negative-sequence voltage source behind a virtual impedance, where the design of the virtual impendence is crucial to accurate phase selection. The virtual impedance design is chosen low so that the negative sequence voltage is zero but not too low so that the negative-sequence current can be recognized by commercial relays. Although the results were tested with several systems under different modes of operations as well as a wide range of fault resistances with great success [21]. However, it showed unreliable results for inverters with unity PF operation, which lead to the suggestion of expanding the current-angle based relay zones backward by 90 degrees, as a partial solution. It also disregarded the effect of four-wire systems.

Another dual current control scheme in [3] aimed to overcome the partial solution that required a minor adjustment to the relay software, which might not be feasible. The source of that

adjustment was due to the dependence of the δ^+ zones on the grid code requirements that affect the power factor of the IIDG. The new proposed dual current control scheme allows the correct operation of existing relays; it is also worth mentioning that it is immune to faults conditions as well as grid codes requirements. The proposed control scheme also contains 120-Hz notch filters to separate the positive- and negative-sequence components that appear as sine waves with twice the frequency in their opposite synchronous reference frames. The generic controller scheme is the first control part of the proposed control scheme, and its objective is to regulate the dc-link and provide reactive current compensation for voltage support. The second control part is the negative-sequence current controller, which consists of three stages. Stage one is the voltage-based phase selection, which identifies the fault type using voltage angle-magnitude based classifier to regulate δ^+ and δ^0. The second stage is to calculate the reference angle of the negative sequence current to force δ^+ and δ^0 to reside in their respective fault zones for correct relay operation. The last stage generates the negative sequence current reference to enforce the negative-sequence current reference angle calculated in stage two while persevering the IIDG's current to satisfy its thermal requirements. The proposed controller was tested for several systems given different fault resistances and various fault locations with great success; however, it was shown to only aid the correct placement of δ^+ or δ^0, not simultaneously. The control scheme, likewise, ignored the effects of four-wire systems.

2.3.4 Trial current control for power-oriented objectives.

A new series of control schemes emerged that utilizes zero-sequence components to enhance the power control under unbalance conditions such as gird faults. These control schemes [23], [24], [28] aimed to remove the limitations of typical three-wire inverter systems subjected to grid faults. These limitations were in the form of the inevitable oscillations that are present in either

active power or reactive power. Previous IIDG power-oriented control schemes were shown to be incapable of eliminating both real and reactive power oscillations simultaneously, which have its complications on the system integrity. Inverter systems with a zero-sequence current path such as four-wire inverter systems offered more control freedoms to overcome this issue. It was shown that with the introduction of zero-sequence, the elimination of both active and reactive power oscillations was feasible. However, these control schemes could make commercial relays to malfunction. In [14], a neutral current compensation control scheme is proposed to provide active filtering. That neutral compensation control scheme meets its objective to provide a better economic option than passive filtering. However, it only provides a solution to four-leg IIDGs, and it disregards the phase selection problem.

2.3.5 Literature survey conclusion and shortcomings

From the aforementioned discussion, the research gaps are as follows: the conventional controller is not suitable for accurate phase selection during grid faults because the performance of the IIDG negative-sequence circuit becomes different than that of SGs. The effects of the IIDG negative-sequence circuit were taken into consideration. However, that led to relays maloperation during grid faults because the control objectives were aimed to enhance the VSC performance, not to provide ancillary protection service. An effort was made to tackle the problem from the relay side; however, it disregards the zero-sequence circuit making them only useful for three-wire systems. Eventually, it is shown that even those that took the zero-sequence circuit into account did not present a solution for phase selection rather than focusing on the IIDG performance during normal conditions. Therefore, there is an imperative need for a new IIDG control scheme that simultaneously regulates all sequence-currents to correctly address the phase selection problem and preserve the IIDG thermal limits.

CHAPTER 3

Proposed Control Scheme for Four-Wire IIDGs

3.1 Zero-Sequence Effects on Control Scheme

The effects of the zero-sequence inclusion are essential to understand for three-phase four-wire inverter applications to correctly model the zero-sequence circuit and control the zero-sequence current. Figure 3.1 depicts a simplified three-phase four-wire inverter system where the voltage across the dc bus is denoted by $V_{DC;}$ V_p and V_n are the voltages across the upper and lower capacitors respectively; I_p and I_n represent the upper and lower dc bus currents. On the AC-side, V_{ta}, V_{tb}, and V_{tc} are the inverter terminal phase voltages whereas I_a, I_b, and I_c are the inverter phase currents interfaced with the grid.

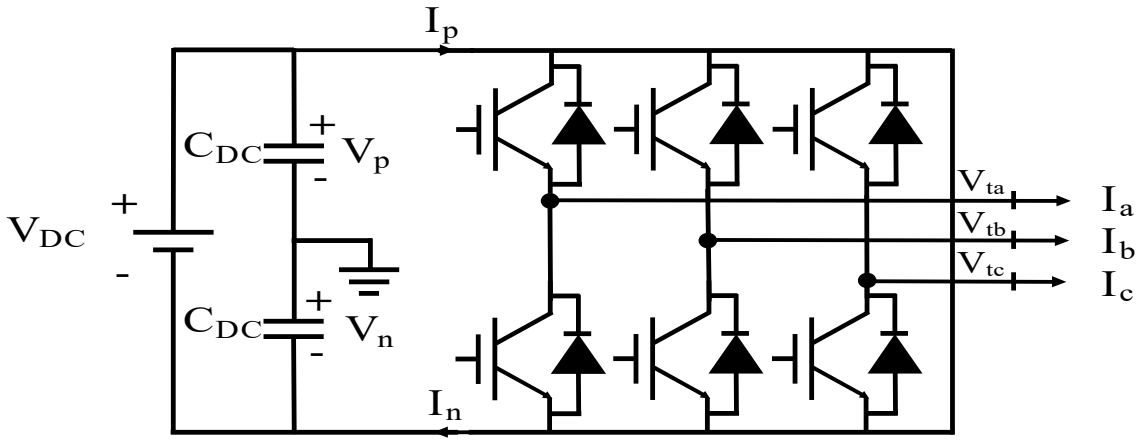

Figure 3.1: Schematic diagram of VSC.

It should be noted that the zero-sequence current flows through the grounded neutral point. The averaged inverter model in [15] is used for the analysis from which the AC-side terminal voltages are

$$V_{tabc} = \frac{V_{DC}}{2} m_{abc} \tag{3.1}$$

where $m_{abc}(t)$ is the phase modulating signals that normally form a balanced three-phase signal. To obtain an expression for I_{DC}, the principle of power balance between the DC-side and the AC-side is utilized as

$$V_{DC} I_{DC} = V_{ta} I_a + V_{tb} I_b + V_{tc} I_c \tag{3.2}$$

by substituting (3.1) into (3.2) and eliminating V_{DC} on both sides, I_{DC} can be formulated as

$$I_{DC} = \frac{1}{2}[m_a I_a + m_b I_b + m_c I_c] \tag{3.3}$$

The upper and lower DC bus currents, I_p and I_n, are the addition of the currents injected by the upper switches and lower switches respectively, i.e.,

$$I_p = \frac{1}{2}[(m_a + 1) I_a + (m_b + 1) I_b + (m_c + 1) I_c] \tag{3.4}$$

$$I_n = \frac{1}{2}[(m_a - 1) I_a + (m_b - 1) I_b + (m_c - 1) I_c] \tag{3.5}$$

I_p and I_n can be expressed in terms of the I_0 by substituting (3.3) into (3.4) and (3.5) and expressing the phase currents in terms of I_0 which is expressed by

$$I_p = I_{DC} + \frac{3}{2} I_0 \tag{3.6}$$

$$I_n = I_{DC} - \frac{3}{2} I_0 \tag{3.7}$$

From (3.6) and (3.7), under balanced conditions, the zero-sequence current is zero, which means the upper and lower dc bus currents are equal to the DC current. However, under unbalanced

conditions I_p and I_n will be different by a factor of the zero-sequence current, which is $\pm\frac{3}{2}I_0$. Moreover, it can be seen from (3.6) and (3.7) that I_p and I_n will contain DC and AC quantities [29]. From (3.6) and (3.7), it can be seen that the capacitors will be charged differently, which suggests that the voltages of the capacitors V_p and V_n will be different; however, their addition is equal to V_{DC} which can be written as

$$V_{DC} = V_p + V_n \tag{3.8}$$

where the terminal phase voltages in (3.1) can be rewritten as

$$V_{tabc} = \frac{1}{2}[(m_{abc} + 1)V_p + (m_{abc} - 1)V_n] \tag{3.9}$$

by substituting (3.8) into (3.9), the terminal phase voltages expressed in terms of the modulating signals are

$$V_{tabc} = \frac{V_{DC}}{2} m_{abc} + \frac{1}{2}[V_p - V_n] \tag{3.9}$$

under balanced conditions, (3.9) transforms to (3.1) as V_p is equal to V_n; however, under unbalanced conditions, a voltage denoted by V_{unbal} is added to all inverter phase voltages that

$$V_{unbal} = \frac{1}{2}[V_p - V_n] \tag{3.10}$$

The inclusion of the zero-sequence current introduces V_{unbal} to the inverter PWM; by expanding (3.9) and adding the three-phase quantities, the inverter zero-sequence terminal voltage can be expressed as

$$V_{t0} = \frac{V_{DC}}{2} m_0 + V_{unbal} \tag{3.11}$$

From (3.11), V_{t0} suggests that the inverter PWM scheme should be treated conventionally like the ones in (3.1). Whereas the V_{unbal} is to be accounted for with the zero-sequence controller. It is crucial to account for V_{unbal} with the zero-sequence controller so that the desired current

command can be tracked properly. The dynamics of the VSC shown in Figure 3.2 are described by

$$L\frac{dI_a}{dt} = -R_a I_a + V_{ta} - V_{ga} \tag{3.12}$$

$$L\frac{dI_b}{dt} = -R_b I_b + V_{tb} - V_{gb} \tag{3.13}$$

$$L\frac{dI_a}{dt} = -R_c I_c + V_{tc} - V_{gc} \tag{3.14}$$

then, by adding (3.12) – (3.14) and dividing by 3 to obtain the zero-sequence circuit dynamics as

$$L\frac{dI_0}{dt} = -RI_0 + V_{t0} - V_{g0} \tag{3.15}$$

It should be noted that resistance R subscript has been dropped as all the phase resistances are equal. Finally, by substituting (3.11) into (3.15) V_{t0} can be expressed in terms of the zero-sequence modulating signal as

$$L\frac{dI_0}{dt} = -RI_0 + \frac{V_{DC}}{2}m_0 + V_{unbal} - V_{g0} \tag{3.16}$$

It should be noted that (3.16) forms the foundation of the zero-sequence control, which is similar to $\alpha\beta$ control schemes that deal with sinusoidal signals that are typically controlled using proportional-integral (PR) controllers.

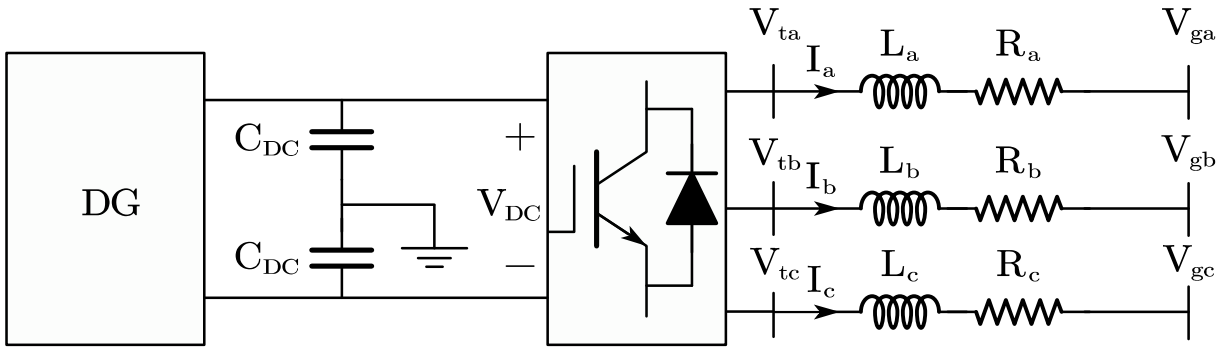

Figure 3.2: Schematic diagram of VSC with grid.

3.2 Problem Statement

To assess the adverse impacts of four-wire IIDG control schemes on phase selection, two case studies are conducted based on the 34.5 kV, 60 Hz system shown in Figure 3.3. The system parameters are shown in the figure, in which, a 9.2 MW inverter is connected to bus 1 through a 4.16/34.5 kV, $X = 0.1$ p.u., dY_gY_g transformer. Rij is the relay between buses *i* and *j*, next to bus *i*. The topology adopted for the four-wire inverter is the mid-point split capacitors; it is to be noted that the behavior of the inverter is dominated by the control scheme rather than the topology or physical properties [30]. The inverter operates at unity power factor and conforms to the North-American GC during a bolted BCG fault at $t = 0.5\,s$. The German GC is later employed to study the effect.

3.2.1 Constant active power control schemes

Constant active power control schemes have been a popular strategy that is used to eliminate the oscillations in both the three-phase real power as well as the DC voltage oscillations during grid faults. A new series of these control schemes have emerged for three-phase four-wire systems [23], [24], [28]. These control schemes offer more control freedoms to achieve higher

performance; however, they provide benefits from the inverter point of view rather than from the grid protection perspective, although these types of control schemes inject negative- and zero-sequence currents, the angles of these sequence currents are different from the angles, an SG would make during faults, which causes fault type classifiers to malfunction. Figure 3.4(a) shows how the constant active power control schemes meet their objectives by eliminating the active power oscillations at twice the nominal frequency as opposed to the conventional positive sequence controller [15] that fails to do so. Nevertheless, the mentioned scheme causes R12 to malfunction because it cannot select the faulted phase correctly, as shown in Figure 3.4(b), because δ^+ and δ^0 are out of the BCG detection regions. δ^+ and δ^0 are not correctly placed in their respective zone as these scheme inject sequence currents with angles different than those of a convetional SG.

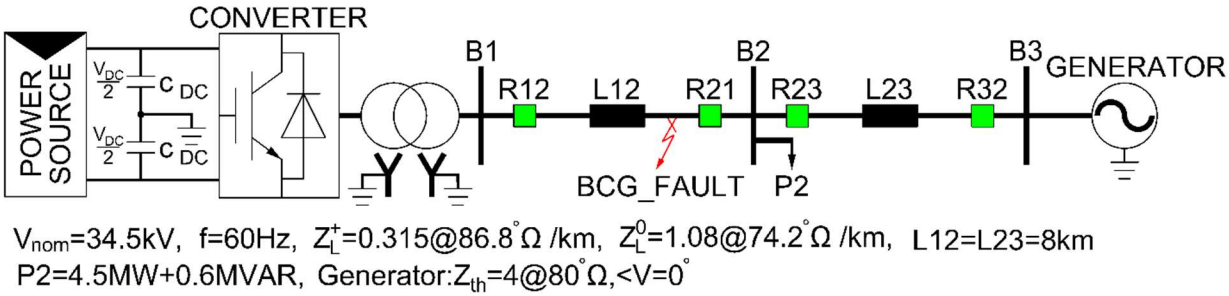

Figure 3.3: One-line diagram of a simplified test system.

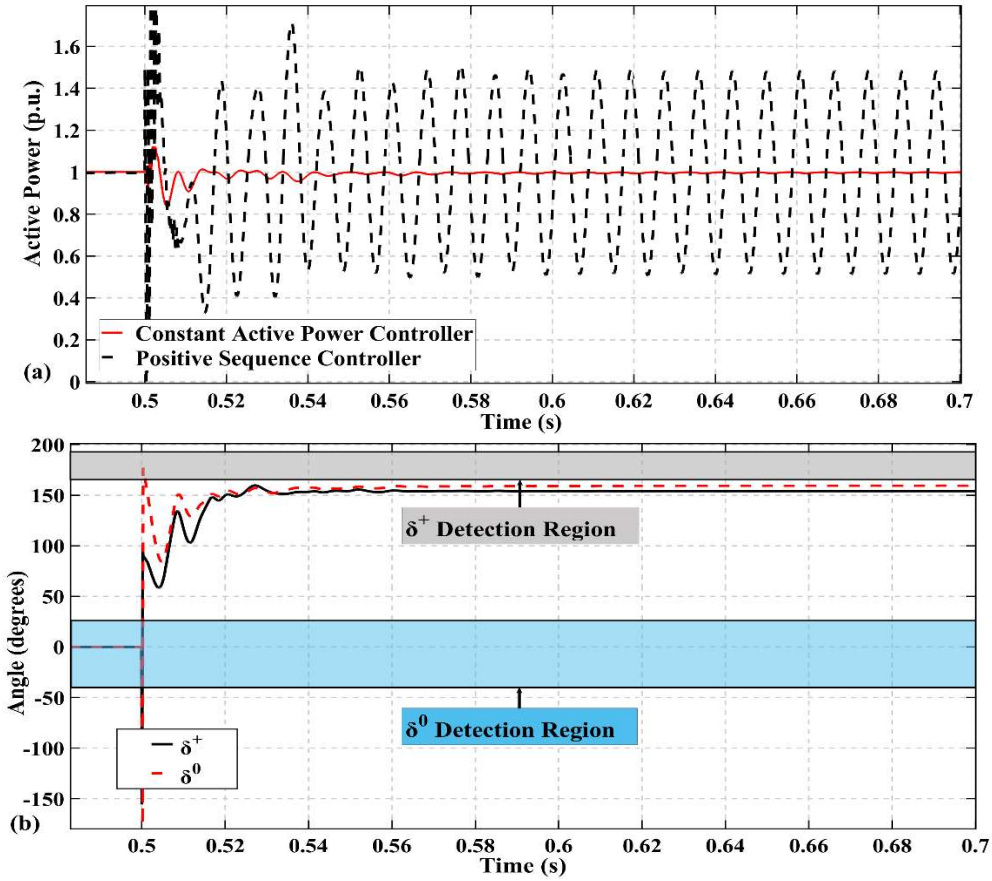

Figure 3.4: (a) output active power, (b) angles measured by R12 for a BCG fault.

3.2.2 Dual current control scheme for fault phase selection

In this study, the IIDG is controlled by a dual current control scheme such as the one discussed in [21], which is referred to as DCC1. This control scheme makes the IIDG behave similar to an SG during asymmetrical grid faults to aid the commercial relays to correctly classify the fault. The control scheme emulates a conventional SG by modeling the negative sequence circuit as a controllable voltage source behind a virtual impedance. Although DCC1 aids relay R12 to correctly classify the fault type based on δ^0 and δ^+ where the zone of δ^+ is shifted backwards by 90 degrees as shown in Figure 3.5(a), the neutral current reaches unacceptable levels as shown in Figure 3.5(b). The problem stems from DCC1 not controlling the zero-sequence current.

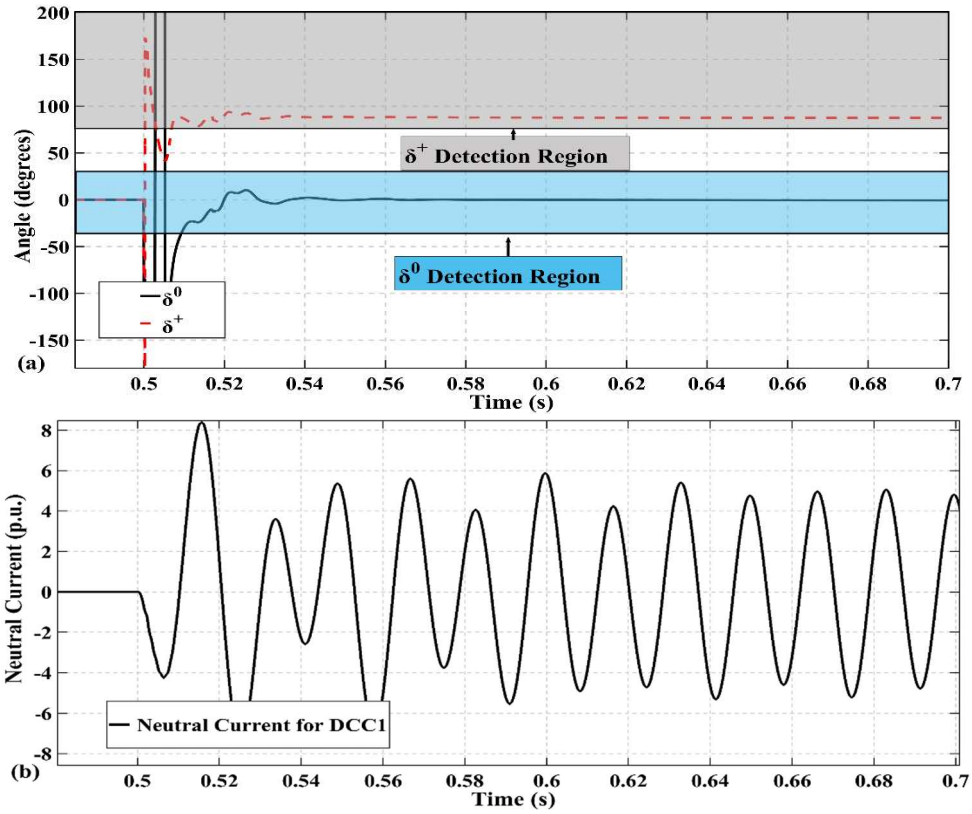

Figure 3.5: DCC1: (a) angles measured by R12 for a BCG fault. (b) neutral Current.

which makes it not suitable for four-wire systems. The reason behind the high current in the neutral conductor can be understood by

$$I_N = 3I_0 = I_a + I_b \tag{3.17}$$

where I_N and I_0 are the neutral current and the zero-sequence current, respectively. It is clear from (2) that by controlling the I_0, I_N can be attenuated to acceptable levels. The results shown in these studies suggest the need for a new inverter control scheme that correctly classifies fault type and preserves inverter limits.

3.3 Proposed Control Scheme

This section explains the controller structure that makes existing commercial relays correctly classify the fault type for proper operation. Figure 3.6(a) depicts the system layout where V_g and I_g are the voltage and current at the point of common coupling (PCC) respectively; V and I are the inverter terminal voltage and current respectively and L_f, R_f, and C_f are the inductance, resistance, and capacitance of the filter, respectively. To control these components for four-wire systems to imitate the behavior of SGs and hence proper relays operation. To achieve that goal, grid synchronization and sequence extraction are required to ensure a robust and reliable controller. Figure 3.6(b) displays the synchronization and extraction blocks that use a DDSRF based PLL [31] for the positive and negative sequences. Sequence extraction filters are avoided as they undermine the controller stability margin [32]. Figure 3.6(B) also displays a SOGI based PLL [33] for the zero-sequence synchronization.

3.3.1 Positive-sequence control scheme

Figure 3.6(c) depicts the positive-sequence control scheme of a conventional inverter controller. The inverter is fed by a RES that is modeled as a current source, which requires DC-link voltage regulation. The model given in [15] is adopted for the dc-link voltage regulation. The positive-sequence reference currents $I^{+}_{d,ref}$ and $I^{+}_{q,ref}$ are generated to regulate the voltage and to comply with reactive current generation (RCG) requirements imposed by grid codes, respectively. The model can be described using

$$I^{+}_{d,ref} = \frac{P_{DG}}{\frac{3}{2}V^{+}_{d}} + \mathbf{PI}\left(V^{2}_{dc} - V^{2}_{dc,ref}\right) \tag{3.18}$$

where P_{DG} is the RES average power, **PI** is the transfer function of the PI controller. $I^{+}_{q,ref}$ is

generated depending on the GCs, which for North America is close to the unity power factor implying almost zero reactive current generation. Whereas, for European grid codes, the reactive current injection is a function of the rate of change of the voltage at the PCC.

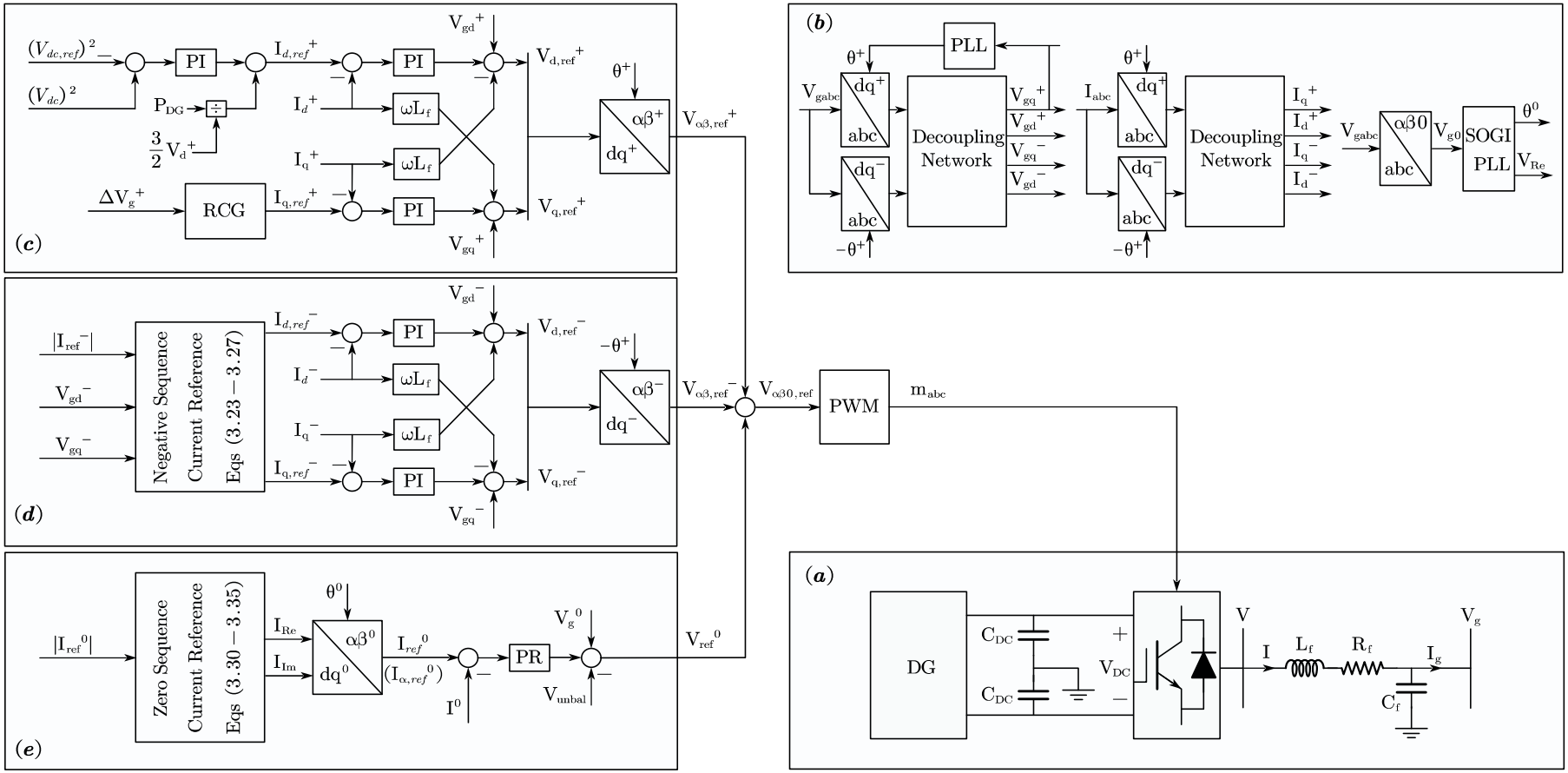

Figure 3.6: Controller Structure: (a) System Layout, (b) Extraction and synchronization blocks , (c) Positive-sequence Controller, (d) Negative-sequence Controller, (e) Zero-sequence controller.

3.3.2 Negative-sequence control scheme

The objective of the negative-sequence control scheme is to ensure that the angle of the negative-sequence current for the inverter behaves like that of an SG. Figure 3.6(d) illustrates how the negative-sequence control scheme meets its objective. $\angle \Delta I^-$ is not only dependent on the fault type but also on the IIDG control parameters [3]. The parallel filter impedance is ignored in short-circuit studies as it is significantly larger than the filter's series impedance [21] that also expresses the negative-sequence current as

$$I^- = -\frac{V_g^-}{Z^-} \tag{3.19}$$

where the negative sign is to be noted for the direction of the current. From (3.19) the angle of the negative-sequence current can be written as

$$\angle I^- = \angle V_g^- - \angle Z^- - 180^\circ \tag{3.20}$$

To achieve the objective of the controller, the IIDG must inject a negative-sequence current where its angle is set apart from the negative-sequence voltage angle by the system negative-sequence impedance angle, which is similar for a grid, line, and transformer. In addition, from (3.20), a 180° offset must be considered due to the direction of the current. Figure 3.6(d) depicts the negative-sequence control scheme where the backbone of the controller is like the positive-sequence controller. However, the current references $I_{d,ref}^-$ and $I_{q,ref}^-$ are generated to meet the criteria in (3.20). Figure 3.7 depicts the coordinate system of the positive and negative dq synchronous reference frames as well as the stationary reference frame. The dq^+ frame rotates counterclockwise while the dq^- rotates clockwise at angular speeds of ω and $-\omega$ respectively.

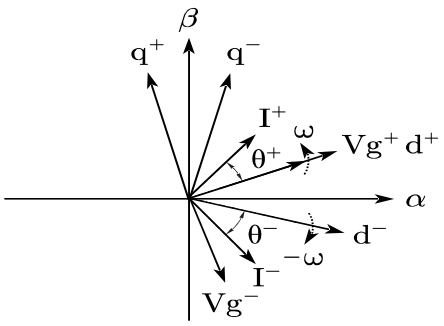

Figure 3.7: Coordinate system.

The angles of the negative-sequence current and the negative-sequence voltage with respect to the dq- frame can be written as

$$\angle I^- = tan^{-1}\frac{I_q{}^-}{I_d{}^-} \tag{3.21}$$

$$\angle V_g{}^- = tan^{-1}\frac{V_{gq}{}^-}{V_{gd}{}^-} \tag{3.22}$$

From (3.21), it is concluded that negative-sequence current angle with respect to the dq^- frame is a function of the ratio of I_q^- to I_d^-. A similar result is drawn to the negative-sequence voltage, as can be seen in (3.22). Moreover, the negative-sequence current control scheme is designed to take the impedance angle seen by the relay into consideration, which is referenced with respect to the positive-sequence direction of rotation. On the contrary, the angle generated from the negative-sequence controller is opposite to the positive-sequence direction of rotation due to the negative-sequence components extraction technique, which leads to modifying (3.20) as

$$\theta_{ref}^- = \angle I^- = (\angle V_g{}^- - \angle -Z^- - 180^\circ) \tag{3.23}$$

where the negative sign associated with Z^- is added to negative sequence impedance to account for the relative angle seen by the relay. From (3.23), the only unknown variable to obtain the reference angle is the angle of the negative-sequence voltage, which is found using (3.22). It should also be noted that $V_g{}^-$ is not necessarily aligned with the d-axis in the dq^- frame. Once

the reference angle is known, the final step is to ensure that the ratio of I_q^- to I_d^- complies with the angle found in (3.23). Whereas the magnitude of the negative-sequence current is chosen to serve a secondary objective to preserve the IIDG phase currents limit. To obtain expressions for the reference currents (3.21) can be rewritten as

$$tan\,\theta_{ref}^- = \frac{I_{q,ref}^-}{I_{d,ref}^-} \tag{3.24}$$

Furthermore, the magnitude of the negative-sequence current can be written as

$$\left|I_{ref}^-\right| = \sqrt{\left(I_{d,ref}^-\right)^2 + \left(I_{q,ref}^-\right)^2} \tag{3.25}$$

$I_{d,ref}^-$ can be solved for by substituting for $I_{q,ref}^-$ in (3.24) using (3.25), which yields

$$I_{d,ref}^- = K_d \sqrt{\frac{\left(\left|I_{ref}^-\right|\right)^2}{1 + \tan\theta_{ref}^{-\,2}}} \tag{3.26}$$

where K_d is either 1 or -1 depending on which quadrant the reference angle lies in. From (3.24), $I_{q,ref}^-$ can be written as

$$I_{q,ref}^- = K_q\,(I_{d,ref}^- * \tan\theta_{ref}^-) \tag{3.27}$$

where K_q is either 1 or -1 depending on which quadrant the reference angle lies in.

3.3.3 Zero-sequence control scheme

Figure 3.8(a) demonstrates the zero-sequence equivalent circuit for the inverter, which shows that the zero-sequence current angle is dependent on the inverter control scheme. The objective of the zero-sequence controller is mainly to control the zero-sequence current angle so that it imitates the zero-sequence current angle of an SG. To achieve that objective, a SOGI-PLL is used to synchronize the zero-sequence quantities to obtain DC-quantities. Using Figure 3.8(a), the zero-sequence current, as well as its angle, can be respectively written as

$$I^0 = -\frac{V_g{}^0}{Z^0} \tag{3.28}$$

$$\angle I^0 = \angle V_g{}^0 - \angle Z^0 - 180^\circ \tag{3.29}$$

where the negative sign in (3.28) is due to the direction of the current that finally translates to a 180° offset added in (3.29). In a similar analogy with the negative-sequence controller, the zero-sequence controller must inject zero-sequence current where its angle is set apart from the zero-sequence voltage angle by the system zero-sequence impedance and the 180° offset. Figure 3.8(b) shows the real-imaginary synchronous reference frame analogous to the dq-frame but in the zero-plane.

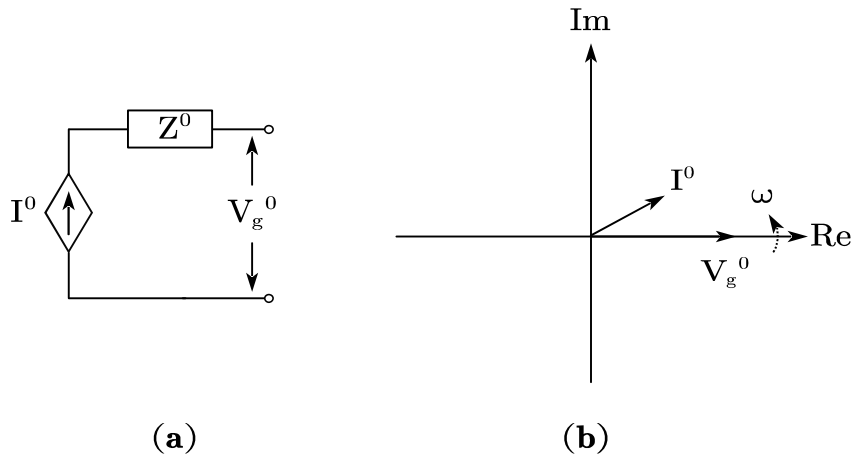

Figure 3.8: (a) Equivalent Zero-sequence circuit, (b) Real-Imaginary reference frame.

In summary, the angle of the zero-sequence voltage with respect to the real-imaginary frame is known and is equal to zero due to the action of the SOGI-PLL, which means there are no unknowns in (26), and it can be rewritten as

$$\angle I^0 = -\angle Z^0 - 180^\circ \tag{3.30}$$

where Z^0 is the typical system zero-sequence impedance, which is also known. From Figure 3.8(b), the angle of the zero-sequence current can be found to be

$$\angle I^0 = tan^{-1}\frac{I_{Im}}{I_{Re}} \tag{3.31}$$

The ratio of I_{Im} to I_{Re} is what affects the zero-sequence current angle, which makes it a primary control objective. The zero-sequence current magnitude serves a secondary objective, which is to preserve the IIDG phase currents limit. To obtain expressions for the zero-sequence reference currents (3.31) can be rewritten as

$$\tan\theta^0_{ref} = \frac{I_{Im,ref}}{I_{Re,ref}} \tag{3.32}$$

In a similar fashion to negative-sequence current controller generator, the expressions for the zero-sequence reference currents can be written by

$$\left|I^0_{ref}\right| = \sqrt{\left(I_{Re,ref}\right)^2 + \left(I_{Im,ref}\right)^2} \tag{3.33}$$

$$I_{Re,ref} = -\sqrt{\frac{\left(\left|{I_{ref}}^0\right|\right)^2}{1 + tan\,{\theta^0_{ref}}^2}} \tag{3.34}$$

$$I_{Im,ref} = \left(I_{Re,ref} * tan\,\theta^0_{ref}\right) \tag{3.35}$$

It should be noted that the negative sign that appears in (3.34) is because the zero-sequence current angle is known, and it lies in the second quadrant.

The proposed control scheme is initially tested on the test system shown in Figure 3.3. A bolted BCG fault takes place at line $L12$. As illustrated in Figures 3.9(a) and 3.9(b), the proposed control scheme makes the relay correctly identify a BCG fault for both North American and German GCs. It can also be noticed that the unity power factor conditions of the North American GC cause δ^+ to deviate from its ideal zone. Hence, the need for the δ^+ zone expansion to accommodate for different IIDG power factors as well as fault resistances for both inductive and resistive grids, as can be seen in Figures 3.10(a) and 3.10(b). On the contrary, RCG aids δ^+ to

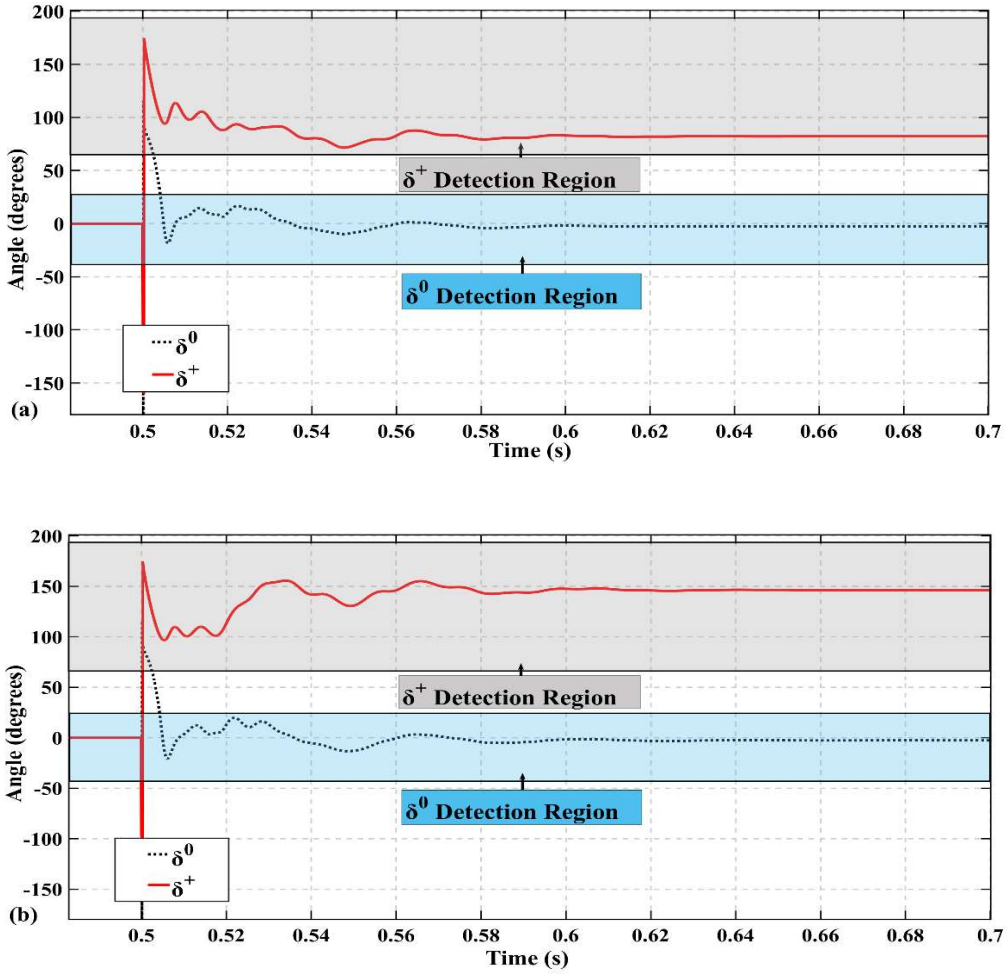

Figure 3.9: Angles measured by R12 for a BCG fault: (a) North American GC, (b) German Grid Code.

remain in its original zone. It can also be concluded that the performance of δ^0 is independent of the grid code imposed. In addition, the neutral current magnitude can be seen in Figure 3.11 for the proposed controller, which is limited to only 0.3 pu.

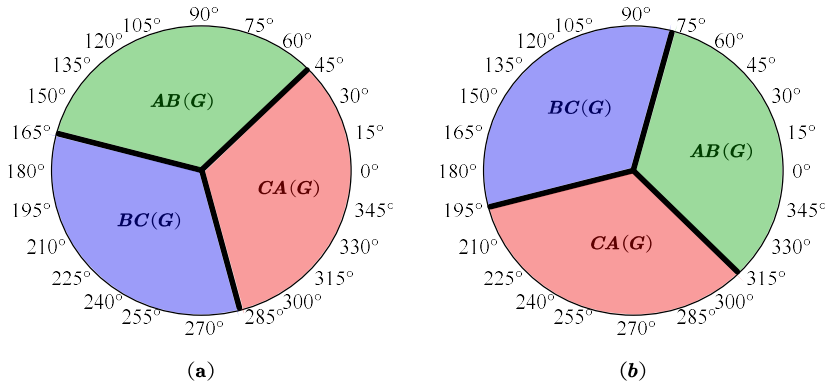

Figure 3.10: expanded zones for: (a) resistive grids, (b) inductive grids.

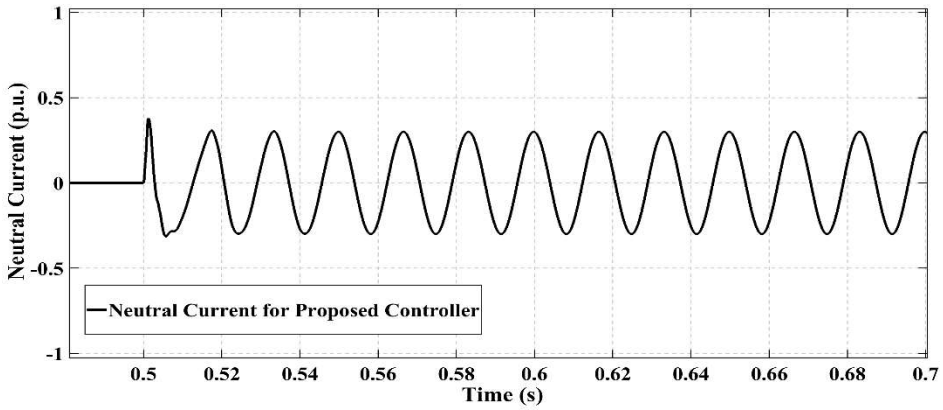

Figure 3.11: Neutral Current for the proposed control scheme.

3.3.4 Inverter current limitation

To limit the inverter's current, a relationship should be drawn between the sequence currents and the phase currents to determine the maximum values of the phase currents injected into the system. It has been shown in [34] that the current vector resulting from positive and negative sequences only describes an ellipse in the $\alpha\beta$ reference frame. However, with the inclusion of the zero-sequence the analysis can be extended where the current vector describes an ellipsoid, as shown in Figure 3.12. The maximum phase currents can be found by obtaining the maximum projection of the ellipsoid on the *abc* axes. The maximum projection onto the a-axis can be

visualized as shown in Figure 3.13 by understanding that the ellipsoid is made up of many ellipses stacked onto on another, from a sliced $\alpha\beta$-plane point of view where the ellipse of significance is the one that coincides with the plane at the zero-sequence value. To facilitate the solution, only a-axis is of significance here as it is aligned with the $\alpha 0$ plane, and then a rotation mechanism will be used to obtain the expressions for the other phases. The phase currents can be presented in the $\alpha\beta 0$ frame using inverse Clarke's transformation as

$$\begin{cases} I_a = I_\alpha + I_0 \\ I_b = -\frac{1}{2} I_\alpha + \frac{\sqrt{3}}{2} I_\beta + I_0 \\ I_c = -\frac{1}{2} I_\alpha - \frac{\sqrt{3}}{2} I_\beta + I_0 \end{cases} \tag{3.36}$$

The objective is to rotate the ellipsoid so that it only contains $\alpha 0$ components. The rotation around the zero-axis can be described as

$$I_{abc} = \begin{bmatrix} 1 & 0 & 1 \\ -1/2 & \sqrt{3}/2 & 1 \\ -1/2 & -\sqrt{3}/2 & 1 \end{bmatrix} \times \begin{bmatrix} I_\alpha \\ I\beta \\ I0 \end{bmatrix} \tag{3.37}$$

where $I^*_{\alpha\beta 0}$ are the rotated $\alpha\beta 0$ components, I is the maximum phase current that contains only $\alpha 0$ components, and γ is rotation angle, which can be found as

$$\begin{cases} I^*_\alpha = I\alpha \cos\gamma - I\beta \sin\gamma \\ I^*_\beta = I\alpha \sin\gamma + I\beta \cos\gamma \\ I^*_0 = I_0 \end{cases} \tag{3.38}$$

$$I = I^*_\alpha + I^*_0 \tag{3.39}$$

$$\gamma = \begin{cases} 0 & for\ phase\ a \\ -120 & for\ phase\ b \\ +120 & for\ phase\ c \end{cases} \tag{3.40}$$

The sequence currents can be decomposed in the αβ0 frame as

$$\begin{cases} I\alpha &= I^{+}\cos\left(\omega t+\theta^{+}\right)+ \ I^{-}\cos(-\omega t-\theta^{-}) \\ I\beta &= I^{+}\sin\left(\omega t+\theta^{+}\right)+ \ I^{-}\sin(-\omega t-\theta^{-}) \\ I_0 &= I^{0}\cos\left(\omega t+\theta^{0}\right) \end{cases} \tag{3.41}$$

where the * notation has been dropped for clarity. By using (3.38), (3.39), and (3.41) and utilizing trigonometric functions, the current can be expressed as

$$\begin{aligned} I = \ \cos\omega t \begin{bmatrix} I^{+}\cos\gamma\cos\theta^{+} \ + I^{-}\cos\gamma\cos\theta^{-} \\ -\ I^{+}\sin\gamma\sin\theta^{+}+I^{-}\sin\gamma\sin\theta^{-} \\ +\ I^{0}\cos\theta^{0} \end{bmatrix}+ \\ \sin\omega t \begin{bmatrix} -I^{+}\cos\gamma\sin\theta^{+}-\ I^{-}\cos\gamma\sin\theta^{-} \\ -\ I^{+}\sin\gamma\cos\theta^{+}+I^{-}\sin\gamma\cos\theta^{-} \\ -I^{0}\sin\theta^{0} \end{bmatrix} \end{aligned} \tag{3.42}$$

where

$$\begin{aligned} A = \begin{bmatrix} I^{+}\cos\gamma\cos\theta^{+} \ + I^{-}\cos\gamma\cos\theta^{-} \\ -\ I^{+}\sin\gamma\sin\theta^{+}+I^{-}\sin\gamma\sin\theta^{-} \\ +\ I^{0}\cos\theta^{0} \end{bmatrix} \\ B = \begin{bmatrix} -I^{+}\cos\gamma\sin\theta^{+}-\ I^{-}\cos\gamma\sin\theta^{-} \\ -\ I^{+}\sin\gamma\cos\theta^{+}+I^{-}\sin\gamma\cos\theta^{-} \\ -I^{0}\sin\theta^{0} \end{bmatrix} \end{aligned} \tag{3.43}$$

The magnitude of the current I in (3.42) can be found as

$$|I| = \sqrt{A^2+B^2} \tag{3.44}$$

which can, after simplification, is rewritten as

$$I = \sqrt{\begin{matrix} I^{+2}+I^{-2}+I^{02}+2I^{+}I^{-}\cos(2\gamma+\ \theta^{+}-\theta^{-}) \\ +\ 2I^{-}I^{0}\cos\left(\gamma-\ \theta^{-}+\theta^{0}\right) \\ +\ 2I^{+}I^{0}\cos\left(\gamma+\theta^{+}-\theta^{0}\right) \end{matrix}} \tag{3.45}$$

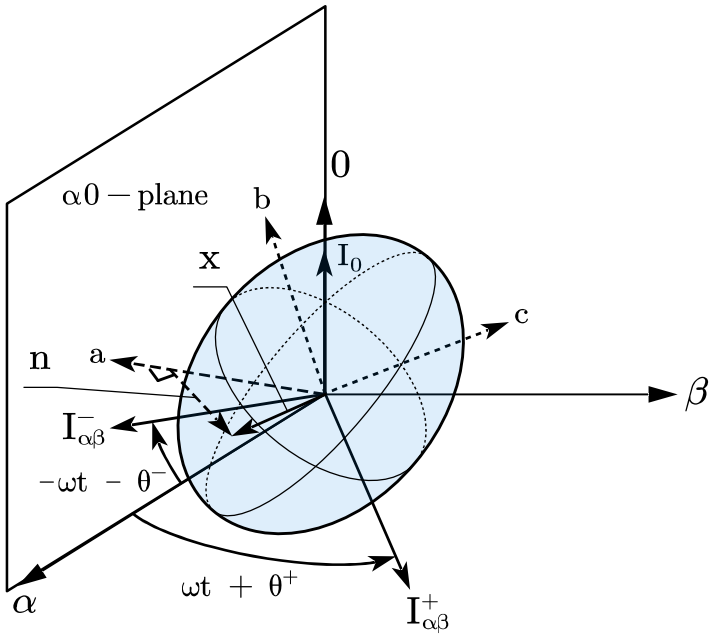

Figure 3.12: Positive, negative, and zero-sequence currents represented in the αβ0 reference frame.

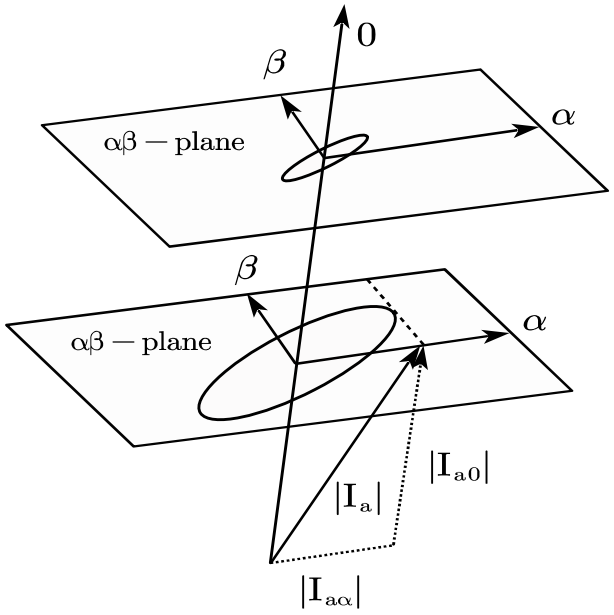

Figure 3.13: The maximum projection of the ellipsoid on a-axis that contains alpha and zero components.

The proposed controller sets the positive, negative, and zero sequence current components magnitudes to 1.2 pu, 0.3 pu, and 0.1 pu, respectively which produces satisfactory phase currents and neutral current magnitudes. The controller strategy is to make δ^0 the primary technique to identify the fault type. Whereas, for LL faults in the absence of the zero-sequence current δ^+ should be used to identify the LL fault type. The magnitudes of the negative-sequence and zero-sequence currents should not be small as commercial relays utilize a minimum threshold [27]. The magnitudes of the sequence currents are then compared against the minimum threshold values to declare a fault. In case the magnitudes of the sequence currents are small, the relays could malfunction by not recognizing a fault condition.

CHAPTER 4

Performance Evaluation

Various case studies are conducted in this section to investigate the behavior of the proposed control scheme for different fault locations, fault resistances, and different GC requirements. The proposed solution was tested on the CIGRE low-voltage (LV) benchmark microgrid system [35], [36] shown in Figure 4.1, which is simulated by Simulink/MATLAB. Two 500-KW IIDGs are connected to the test system at nodes 4 and 9, respectively. The benchmark test system is modified by replacing the main fuse with a circuit breaker (CB), and a second sectionalizing CB is inserted between node 4 and node 5 to allow for selective phase tripping and fault isolation for the microgrid.

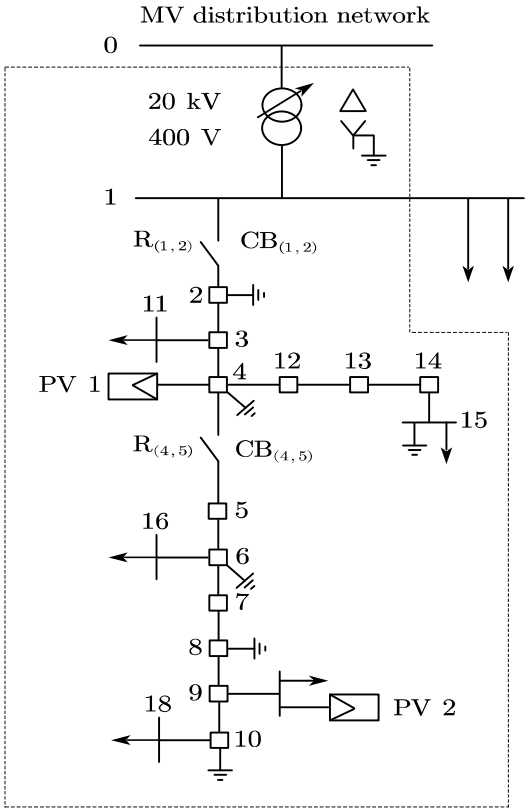

Figure 4.1: The layout of the CIGRE LV benchmark system with two DGs.

4.1 Impact of Grid Codes

Table I reports the angle measurements as well as the estimated fault resistances for relay $R_{(4,5)}$ obtained for the North American GC and the German GC during different bolted SLG and LLG faults at the cable between nodes 12 and 13. The results in Table 4.1 assumes correct PSMs accurately for δ^0 irrespective of the GC as the angles always lie in their proper detection zones. Moreover, R_{lg} is lower than R_{llg} for SLG faults and vice versa for the case of LLG faults implying proper operation. For example, during AG faults δ^0 lies close to zero, which is the mid-point of the detection zone for both GCs. The findings show robust performance for relays that count on δ^0 and the estimated fault resistance. It can be seen from Table 4.1 that the North American GC makes δ^+ to settle in its ideal detection zones while the German GC that requires reactive current compensation causes δ^+ to deviate from its ideal detection zones. For instance, during ABG fault, δ^+ registered a value of 58.91º for the North American GC, which lies close to 60º; however, the German GC registered a value of 112.1º that deviates further from 60º. It can also be seen from Table 4.1 during a BCG fault, δ^0 registered a value of -7.516º for the North American GC, which lies close to 0º; however, the German GC registered a value of -10.06º that also lies close to 0º. Table 4.2 reports the angle measurements as well as the estimated fault resistances for relay $R_{(4,5)}$ obtained for the North American GC and the German GC during different bolted SLG and LLG faults at cable 2-3. The results in Table 4.2 draw a similar conclusion with the results from Table 4.1. For instance, during a BCG fault, δ^+ registered a value of -190.1º and -126.9º for the North American GC and the German GC, respectively. Meanwhile, δ^0 registered a value of -8.688º and -10.50º for the North American GC and the German GC, respectively. The results show that the proposed method is robust for

Table 4.1: Measurements for bolted ground faults at cable 12-13 of the CIGRE LV benchmark system with two DGs.

Fault Type	North American Grid Code			German Grid Code		
	δ^+ (°)	δ^0 (°)	R_{lg}, R_{llg}	δ^+ (°)	δ^0 (°)	R_{lg}, R_{llg}
AG	N/A	-5.117	0.00958, -0.2594	N/A	-7.75	0.01604, -0.545
BG	N/A	-125.1	0.00962, -0.2590	N/A	-127.7	0.01566, -1.605
CG	N/A	115.2	0.00978, -0.2585	N/A	112.3	0.01529, 0.6429
ABG	58.91	112.4	-0.2934, 0.00063	112.1	109.6	-0.2472, 0.00758
BCG	-181.0	-7.516	-0.2964, 0.00062	-128.2	-10.06	-0.2861, 0.00556
CAG	-61.09	-127.7	-0.2960, 0.00063	-7.708	-130.3	-0.2715, 0.00633

Table 4.2: $R_{(4,5)}$ Measurements for bolted ground faults at cable 2-3 of the CIGRE LV benchmark system with two DGs.

Fault Type	North American Grid Code			German Grid Code		
	δ^+ (°)	δ^0 (°)	R_{lg}, R_{llg}	δ^+ (°)	δ^0 (°)	R_{lg}, R_{llg}
AG	N/A	-5.572	-0.0142, -0.2700	N/A	-8.045	-0.0132, -1.279
BG	N/A	-125.6	-0.0140, -0.2618	N/A	-128.0	-0.0139, -4.086
CG	N/A	114.4	-0.0132, -0.2690	N/A	112.0	-0.0150, 0.368
ABG	49.74	111.5	-0.2685, -0.0032	113.3	110.1	-0.1270, 0.00172
BCG	-190.1	-8.688	-0.2709, -0.0032	-126.9	-10.50	-0.1928, 0.00022
CAG	-71.20	-128.3	-0.2706, -0.0031	-6.804	-131.1	-0.1729, 0.00013

Table 4.3: $R_{(4,5)}$ Measurements for bolted LL faults of the CIGRE LV benchmark system with two DGs.

Fault Type	δ^+ (°) measured by $R_{(4,5)}$ for bolted LL faults at Cable 12-13		δ^+ (°) measured by $R_{(4,5)}$ for bolted LL faults at Cable 2-3	
	North American GC	German GC	North American GC	German GC
AB	64.85	126.9	54.79	127.3
BC	-172.6	-108.9	-182.3	-110.1
CA	-54.81	8.727	-64.45	6.899

different fault locations. It can be seen from the previous study that the North American GC places δ^+ in the desired detection zone as opposed to the German GC. The findings obtained here for this low voltage resistive grid is opposite to what was found earlier in a medium voltage inductive grid, which is related to the $\frac{X}{R}$ ratios of the different grids. In a resistive grid with low $\frac{X}{R}$ ratio, the North American GC resembles normal grid operation as it is dominated by real current injection. Whereas, for an inductive grid with high $\frac{X}{R}$ ratio, the German GC resembles normal grid operation as it is dominated by reactive current injection. It can be seen from the previous study that the North American GC places δ^+ in the desired detection zone as opposed to the German GC. Table 4.3 reports the angle measurements for relay $R_{(4,5)}$ during LL faults. All the measurements lie in the proposed detection zone. In addition, it can be concluded that reactive current injection requirements imposed by GC, such as the German GC, disregards the effect of LV distribution networks where the grid is mostly resistive and hence its failure to support voltage for LV systems. Figure 4.2 illustrates the magnitudes of the phase currents for a bolted BCG fault to be less than 1.5 pu.

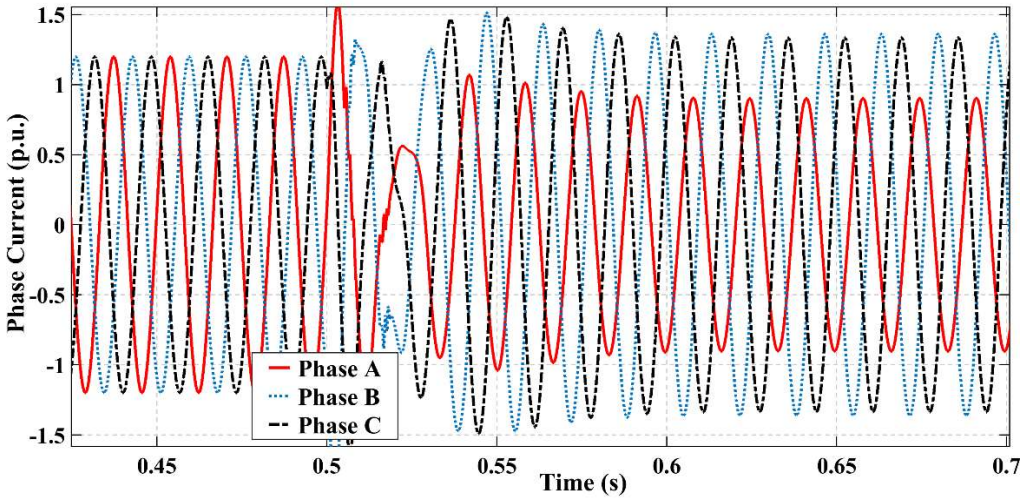

Figure 4.2: Phase currents for bolted BCG fault.

4.2 Behavior under different fault resistances

The performance of the proposed control scheme is tested for a fault resistance $R_{flt} = 1\Omega$ and $R_{flt} = 10\Omega$. δ^+ and δ^0 measured by $R_{(4,5)}$ during ACG faults for the North-American and German GCs are shown in Figures 4.3 and 4.4, for R_{flt} of 10 Ω and 1 Ω, respectively. It can be observed that the fault resistance does not deteriorate δ^0 as it lies in its ideal zone, which is close to 120º regardless of the grid code imposed or fault resistance. It is also observed that δ^+settles close to 100º for the North American GC study while the German GC causes δ^+ to settle close to 110º, which is still confined in the δ^+ proposed detection zone. The results found to prove the effectiveness of the proposed method to classify the fault for δ^0 irrespective of the fault resistance. The proposed method δ^+ helps to place δ^+ in its detection zones for different GC and fault resistances.

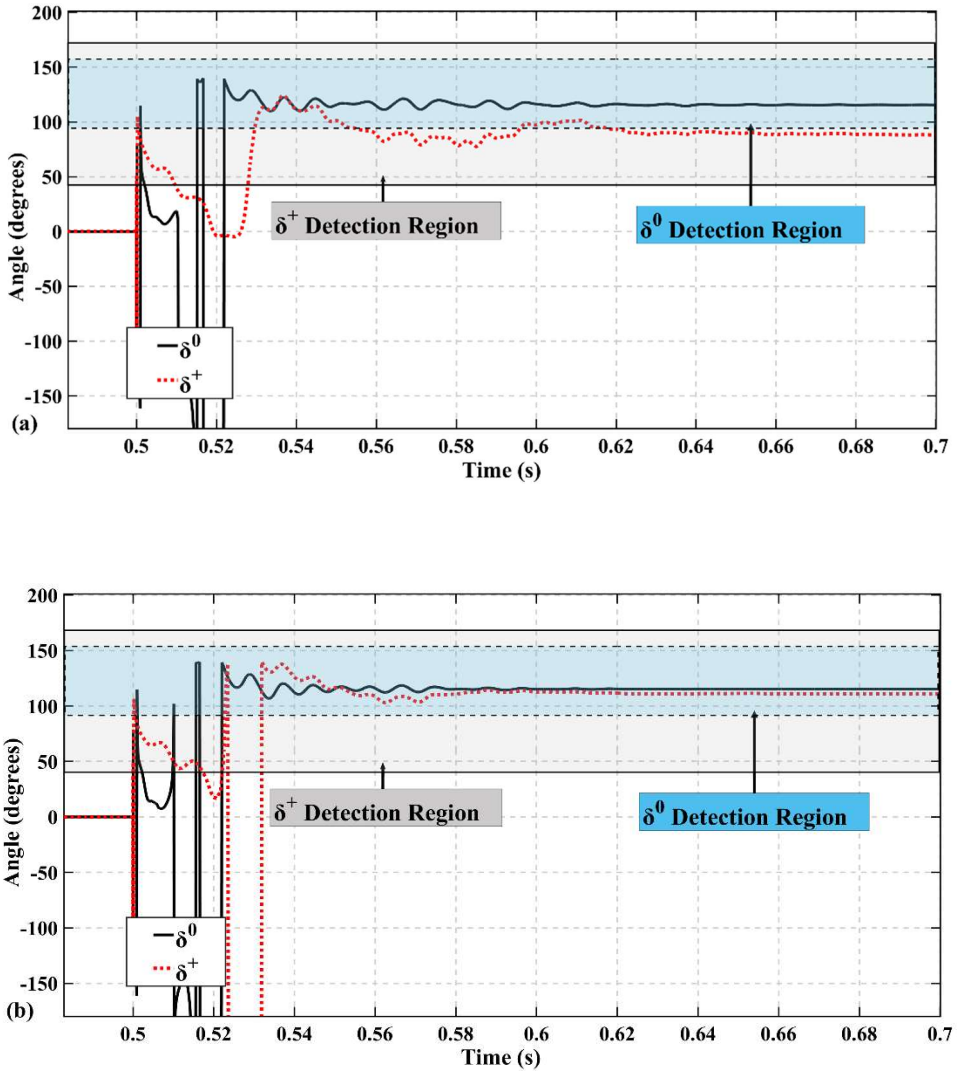

Figure 4.3: Angles of $R_{(4,5)}$ superimposed currents during ABG fault R_{flt} =10Ω: (a) North American GC, (b) German GC.

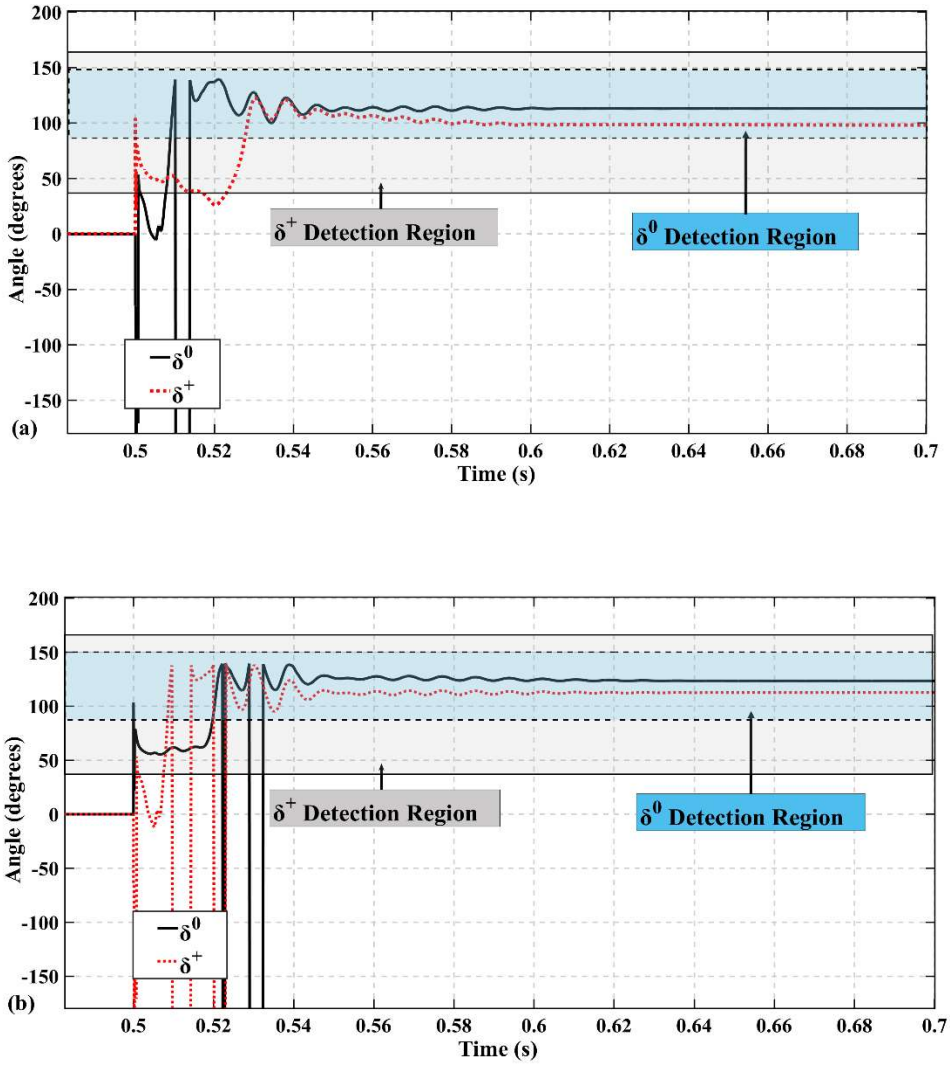

Figure 4.4: Angles of $R_{(4,5)}$ superimposed currents during ABG fault R_{flt} =1Ω: (a) North American GC, (b) German GC.

A measure to detect the level of unbalance is often done through the n-factor, which is defined as the ratio of the negative-sequence voltage to the positive-sequence voltage. As illustrated in Figure 4.5, the North American GC that injects active power has a lower n-factor than the German GC where. Similar results were obtained for other faults, which suggests that for LV system North American GC not only aids the proper operation of protective systems but also supports the voltage of the system.

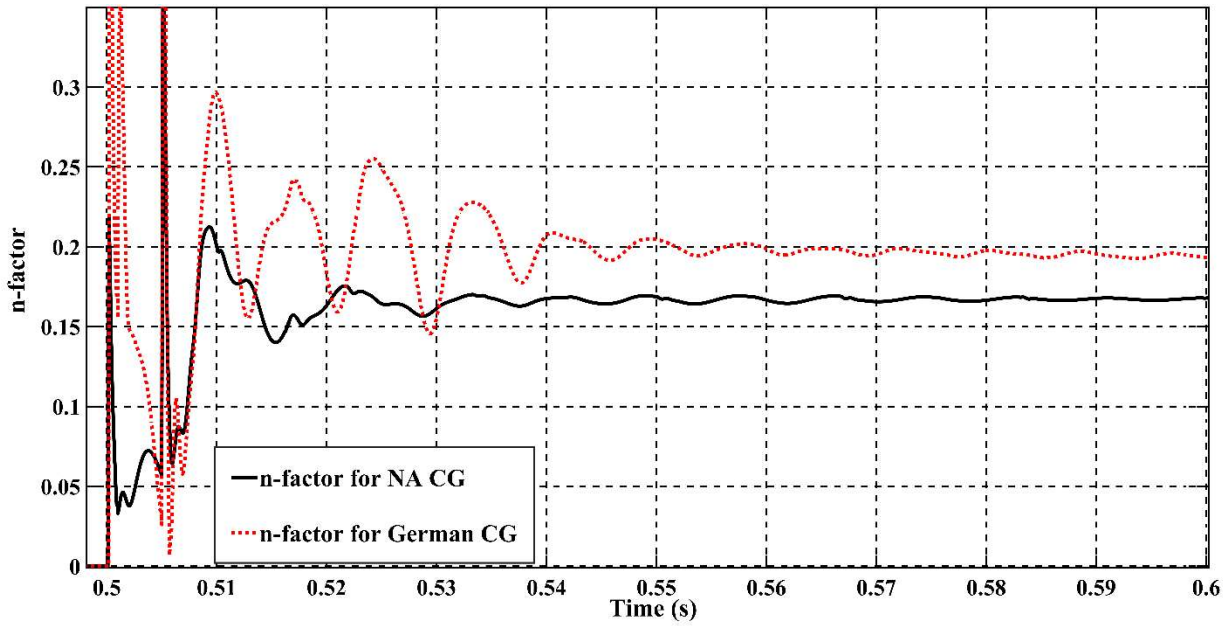

Figure 4.5: n-factor for North American GC & German GC for bolted AG fault.

CHAPTER 5

Conclusion and Future Work

5.1 Conclusion

Fault classifiers that are based on superimposed currents malfunction in the presence of DGs because their currents behave differently than SGs under faults as they are dependent on the control strategy. Different control strategies in the literature that primarily provide ancillary services to the grid other than ensuring reliable power system protection. Others focused on the proper operation of protective devices but only for three-phase three-wire systems. A new control strategy was proposed to enable accurate fault classification in the presence of four-wire (transformerless) IIDGs as well as three-wire IIDGs that interfaced via a transformer. The proposed control scheme consists of three control loops to regulate the sequence currents. it utilizes a DDSRF for the positive- and negative-sequence components extraction, whereas a SOGI is used to synchronize the zero-sequence components. The dynamics of the zero-sequence on the inverter were derived, and an effective control strategy is proposed that forces the angles of the IIDG currents to behave like SGs currents. A relationship to preserve the IIDG's thermal limits is drawn between the sequence components and the magnitude of the IIDG phase currents. The current angle-based classifiers are considered the most effective tool for the phase selection problem for a system subjected to SGs only. The phase selection is performed when the superimposed sequence current angles lie in their two perspective zones, namely δ^+ and δ^0. The proposed solution was tested and shown reliable results for δ^0 zones. A zone relaxation was proposed for δ^+ to counteract different GC as well as fault resistances with success, which was all validated by simulations for a simplified and a practical benchmark system.

5.2 Future Work

Other topics of interest suggested for future work are to:

1. optimize the performance of the VSC using an optimization algorithm to preserve and protect the VSC's power electronics.
2. find a solution for the PSM without the need for a zone expansion for δ^+
3. investigate the proposed control scheme on different VSC topologies, and
4. employ PI controllers to control the zero-sequence current rather than the PR controller to simplify the controller design.

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APPENDICES

A.1 Introduction

It is often very effective to utilize symmetrical components technique with unbalanced AC system conditions. This is achieved based on the following analysis.

A.2 Symmetrical Components

Symmetrical component analysis is considered one of the most effective tools to deal with unbalanced three-phase circuits, which was introduced by C.L. Fortescue [37]. The theorem allows the voltages and currents quantities to be replaced by three separated, balanced, symmetrical components. The unbalanced quantities consist of positive, negative, and zero sequence components that can be expressed as

$$\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} = \begin{bmatrix} X_a^0 + X_a^1 + X_a^2 \\ X_b^0 + X_b^1 + X_b^2 \\ X_c^0 + X_c^1 + X_c^2 \end{bmatrix} \quad \text{(A-1)}$$

where X_a^0 , X_a^1 , X_a^2 are the zero, positive and negative components for phase a that can be either voltage or current denoted by X. the relationship is also extended to phases b and c.

The symmetrical components transformation matrix can be expressed as

$$\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \times \begin{bmatrix} X_a^0 \\ X_a^1 \\ X_a^2 \end{bmatrix} \quad \text{(A-2)}$$

where a is a 120-degrees phasor rotation operator, whereas a^2 is a 240-degrees phasor rotation operator. To obtain an expression for the symmetrical components, the inverse matrix operation is utilized to give

$$\begin{bmatrix} X_a^0 \\ X_a^1 \\ X_a^2 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \times \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{A-3}$$

In a balanced system, only positive-sequence components exist, which in phasor form rotates clockwise, having the three-phase quantities 120 degrees apart. In an unbalanced system without ground availability, a negative-sequence component appears which in phasor form rotation counterclockwise having the three-phase quantities 120 degrees apart as well. Finally, when the ground is available, zero-sequence quantities appear, which have the same phase angles.

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