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Procedures and Procedures and Assessment

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Protection Testing for Multiterminal High-Voltage dc Grid: Procedures and Assessment

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***Abstract*—The application of multiterminal (MT), high-voltage dc (HVdc) (MTdc) grid technology requires test procedures for the operation and implementation of the protection solutions. The test procedures are usually derived from experience and from extensive measurement data, which, at present, are still not widely available. Based on a hardware-in-the-loop (HIL) method, advanced dc protection testing strategies, utilizing existing experience for ac grids and requirements for MTdc grids, may overcome this gap.**

This article proposes procedures and guidelines for testing system-level dc protection based on the functionality of MTdc grids for both primary and backup dc protection. Specific performance criteria have been defined, based on multicase testing and statistical analysis, with the considerations of related critical testing parameters for each functional requirement of the dc protection. Accordingly, procedures for a dc protection testing environment and various fault scenarios are defined. The proposed algorithm test procedures will contribute to the standardization of dc protection system design and testing.

I. Background

Renewable energy sources (RESs) have many advantages for the environment and sustainable energy development. The replacement of traditional fossil fuels by RESs is an energy development trend and energy policy requirement for future power systems [1]. In northern Europe, in particular, the installation of offshore wind power is ever increasing; hence, the development of HVdc systems to support wind power integration is becoming more urgent. The evolution of HVdc systems from point-to-point connections and radial HVdc grids to meshed MTdc grids by making use of voltage source converter (VSC) technology, especially modular multilevel converter (MMC)-based schemes, is also a significant subject for the European power utilities and governments [2]. Worldwide, there are already many relevant projects commissioned or being developed, such as the Québec–New England three-terminal HVdc system [3], Nan'ao four-terminal HVdc system [4], and Zhoushan five-terminal grids [5].

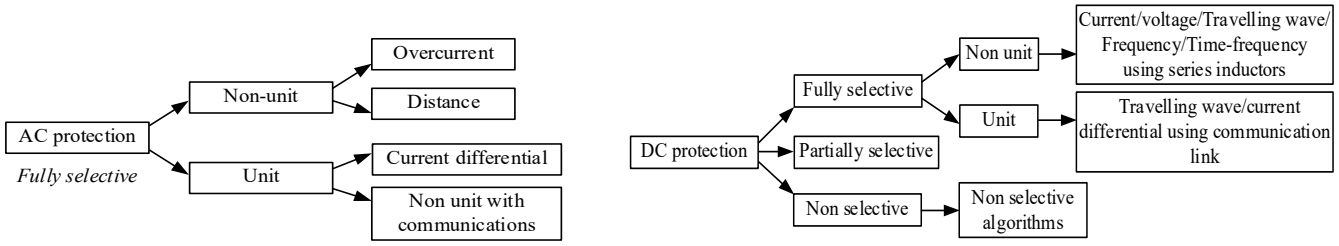
One of the main challenges of the implementation of HVdc power grids is the unavailability of standardized approaches for grid protection, which is a significant barrier for the secure operations of new HVdc grids [5]. dc fault currents in MTdc networks increase rapidly in amplitude, and outages can be easily cascaded from one converter station to another. Thus, protection against these faults is very important to provide safety for the HVdc grid operation and to pave the way for the integration of bulk offshore wind power to the ac grid [6], [7].

Existing HVdc protection concepts are derived from the well-known HVac protection concepts, as illustrated in Figure 1 [8]. Three kinds of protection philosophies are adopted in MTdc protection, i.e., fully selective, nonselective, and partially selective. In the fully selective philosophy, each line is protected using HVdc circuit breakers (dc CBs) at both ends, so power flow remains uninterrupted in the rest of the grid. In the nonselective philosophy, the whole HVdc grid is protected as one zone by converters with fault-blocking capability or by using ac-side CBs (ac CBs). The partially selective philosophy is a compromise between the two former ones, in which the grid is divided into several protection zones based on the placement of dc CBs, the converters with fault-blocking capability, and ac CBs [9].

A simple illustration can be seen in Figure 2. When fault F1 occurs in the middle of lines 2 and 3 in the three-terminal HVdc grid, this faulty line will be only disconnected by the dc CB4 and dc CB5 at both line ends in the fully selective philosophy. In the partially selective philosophy, with an insufficient installation of dc CBs, subgrid2 will be disconnected due to F1 only if dc CB4 and dc CB6 are installed. The red elements [ac CBs, full-bridge (FB) converters, or dc CBs behind converter terminals] will be used to clear F1 in the nonselective philosophy, in which the whole dc grid will be isolated.

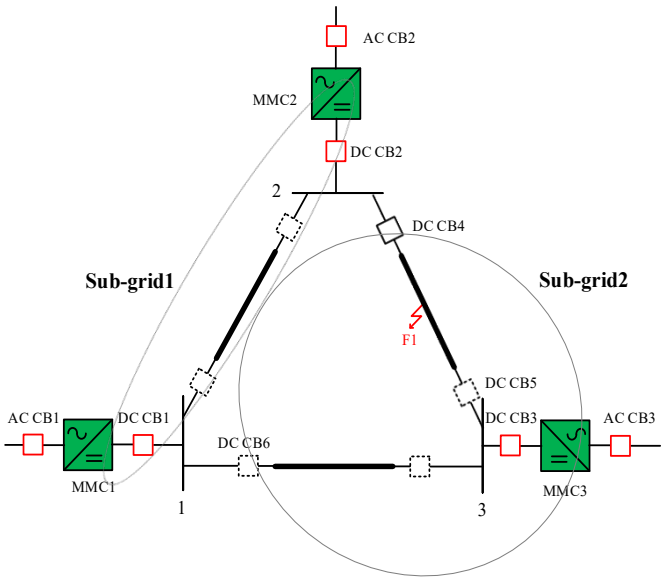
There have been many different HVdc grid protection algorithms proposed by academia and industry so far, which can be categorized as unit protection and nonunit protection. Unit protection algorithms are based on double-ended detection, which makes use of closed protection zones; nonunit protection algorithms are realized with single-ended detection and open zones. The nonunit protection algorithms are mainly used for the primary protection functions, which can be current/current derivative- [10], [11], voltage/voltage derivative- [12], [13], and traveling wave-based approaches [14]–[16]; different combinations of these approaches [17], [18]; and frequency or time domain approaches [19]–[21].

The unit protection algorithms mainly include the current differential [22] and traveling wave differential [23]. Since communication is required for unit protection, it is used for the primary protection functions of the bus bar or for the protection of short lines and as a backup protection function of longer dc lines [24]. Possible protection failures (including breaker failure and relay failure) need to be considered in backup protection functions of an MTdc grid protection system [25].



(a) ac grid protection (b) MTdc grid protection

Figure 1 Categories of protection philosophies and examples of algorithms



HVDC grid protection philosophy		Examples
Fully selective	Protection zones are defined to individually protect each DC line and bus.	Only the fault element has to be disconnected with sufficient DC CBs installed at each end of protected elements, e.g. the faulted line 2-3 is disconnected by DC CB4 and DC CB5 located at two ends of the line.
Partially selective	DC grid is divided into several protection zones or sub-grids.	The grid has been splitted into two sub-grids with an insufficient installation of DC CBs, e.g. the sub-grid2 is disconnected with only DC CB4 and DC CB6 installed in the grid, when F1 occurs.
Non-selective	No protection zones or entire DC grid as one zone	The fault will be cleared by AC CBs or full bridge converters or DC CB behind converter terminals, e.g. only red elements in the grid can be used to clear the DC fault F1.

Figure 2 The different MTdc grid protection philosophies

There are no consensus and standards, so far, about how the dc protection algorithms perform and how they could be used for practical implementation [8]. Considering that today's dc CBs can operate in several milliseconds, fault detection realized by the protection algorithms should also be within the same timescale, which also depends on the speed of fault current development and the withstand capability of system components [26].

In HVdc systems, the current source converter (CSC)-based HVdc, which is known as classic HVdc, can control the dc current during a dc fault. However, the CSC HVdc is, currently, mainly limited to the applications of point-to-point connections, since the reversal of the power flow direction requires a change of voltage polarity on all terminals, and there are other bottlenecks associated with the control systems. The application of dc CBs in CSC HVdc systems is limited, and the maximum ratings are 250 kV, 8 kA or 500 kV, 4 kA, which are not more than 1.6 times the rated nominal current. An interruption time on the order of 35 ms is sufficiently fast for CSC HVdc systems, where large inductors serve to limit the rate of rise of the fault current. These dc CBs are very large and more expensive than the ac CBs for comparable current and voltage ratings. Therefore, for point-to-point CSC HVdc connections, the controlled converter stations or installed ac CBs at the ac side of CSCs are applied to disconnect the HVdc from the ac side [27].

Regarding the fault current characteristics, VSC HVdc systems are mainly distinguished from the CSC HVdc systems by the higher rates of rise and large magnitudes of the fault currents as well as the lower current withstand capability of VSC power electronics [27]. These differences necessitate higher fault current-breaking capabilities within shorter interruption times of the dc CBs in VSC-based HVdc grids.

For VSC HVdc, the MMC, as the most promising option to develop an MTdc grid, can adopt either a half-bridge (HB) or FB structure for each submodule. The HB MMC with freewheeling diodes is unable to stop ac grid contribution to the dc fault currents, and the excessive current stresses may damage the freewheeling diodes. Therefore, the requirement for fast dc CBs becomes inevitable. Moreover, to realize a fully selective protection philosophy and provide power supplying continuity for the healthy part of HVdc grids, more

dc CBs are required to be installed to protect each line and bus in the grid, even though the FB MMC can block current flow in the converter during dc faults.

The objective of the protection testing is to determine whether the performance of an intelligent electronic device (IED) can meet the industry requirements before it can be commissioned in practical applications [28]. Since the converter self-protection scheme is vendor dependent, the scope of the future MTdc grid protection for MTdc grids, here, excludes converter protection. For ac protection testing, well-established designs and methods can be adopted according to IEEE and International Electrotechnical Commission (IEC) standards [29], [30]. In these ac protection standards, the performance test (or type testing) is normally conducted by IED vendors to verify, describe, and certify the performance of protection IEDs used in a specific application, which is normally tested by a simple power system model.

The application tests are normally driven by the users to determine the suitability of an IED for a specific protection system design application. The tests are based on a detailed model of the power system in question and include performance testing against a wide variety of possible fault conditions. The goal of application tests is to ensure that a specific protection IED can perform adequately for a specific application or location before actual installation. These general concepts and classifications of protection testing will be continuously applied in MTdc grids, even though the challenges and requirements are different for dc protection testing [31].

In this article, MTdc grids are the target test power systems, and the application tests are mainly focused from users' viewpoints to provide reasonable test procedures for dc protection testing. Although the fault dynamics and the related protection algorithms of MTdc grids have been investigated and designed by many researchers [10]–[25], no certified HVdc protection IED has been commissioned so far. Moreover, the relatively new testing considerations and methods of MTdc grid protection have rarely been discussed, and many published articles are mainly focused on one specific protection algorithm [32]–[37].

A fault detection and location scheme using the rate of change of voltage measured for an HVdc grid is proposed and tested in [32], where the different fault types and locations have been mainly considered in testing, and a systematic procedure for calibrating the protection threshold values is designed. A transient measured impedance-based protection scheme for HVdc line faults is proposed in [33], where numerous simulations on the power systems CAD/ electromagnetic transients including dc (PSCAD/EMTDC) platform and field fault recording data-based tests have been utilized with the consideration of fault types, fault locations, and sampling frequency. A similar PSCAD/EMTDC-based test has been used in [34] for a generalized protection strategy of HB MMC-based MTdc grids with a fault current limiter branch and hybrid dc CBs, where the different fault resistances, line inductors, and types of dc CBs are considered during the testing.

The types of dc lines and prefault operation points of MTdc grids were used to test a proposed new protection method in [35]. A real-time OPAL-RT-based HIL testing platform was developed in [36] to demonstrate and validate an integrated control and protection scheme for HV ac/dc grids, where the fault types, locations, and combinations are mainly considered. In [37], HIL-based testing was regarded as an ideal choice to simulate the transients of MMC stations and to test the dynamic performance of a complete control and

protection system for the Nan'ao VSC-MTdc grid (i.e., application test).

The aforementioned testing methods are normally introduced together with the new dc protection algorithms, which only consider several important factors or requirements about the specific protection algorithms simulated in the simulation software or hardware environment. They are not appropriate or efficient for industrial testing on multifunctional protection IEDs. In this article, one user-oriented application testing approach for industrial applications of HVdc grid protection is developed based on three steps:

- a systematic investigation and summary of new requirements along with testing considerations for HVdc grid protection in both component and system levels;
- New systematic test procedures for protection IEDs in HVdc grids, based on the statistical analysis of dc fault cases and performance criterion checking;
- a new systematic assessment method for possible protection algorithms implemented in multifunction protection IEDs.

Thus, the main contribution of this article is to develop dc protection testing methods for systematic testing and assessment of the newly proposed MTdc grid protection algorithms. In this way, it can be determined whether the proposed algorithms can meet the operation requirements of the MTdc grids [38].

II. New Challenges and Requirements

A. General considerations

The choice of a specific MTdc grid protection philosophy, i.e., fully selective, partially selective, and nonselective, fundamentally determines the size of the grid part that will be isolated from the rest of the grid during a fault at a particular location. Moreover, since the protection of MTdc grids deals with complex fault scenarios and fast operational performance and takes into account the performance of the dc CBs, the system-level protection of MTdc grids is regarded as one of the most difficult remaining technical challenges in the power system. Some related considerations for future dc applications can be listed as follows [8]:

- multivendor solutions with the proper consideration of interoperability;
- the much quicker response of MTdc grid protection for the dc faults without current zero crossings;
- the development and implementation of dc protection testing methods for the newly available dc protection algorithms.

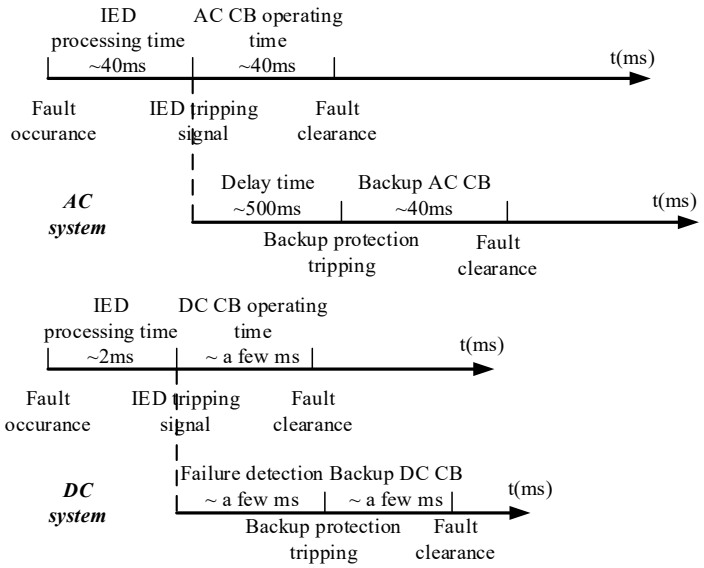


Figure 3 Typical time of primary and backup protection in ac and dc systems

In addition to the general differences from ac protection shown in Figure 1, the fault-clearing times of both the primary and backup protections in MTdc grids are typically one order of magnitude faster compared to those in ac grids. For example, the fault-clearing time of the primary protection is, typically, in the range of several milliseconds, from which 2 ms are allocated for the protection IED processing time and several milliseconds for the dc CB operation time [31]. A related comparison of the time sequences of ac and dc protections can be observed in Figure 3 [8]. As there are only a few practical dc CB prototypes applicable for HVdc grids and there is not much experience in this area, the term a few milliseconds is adopted based on the interruption time of the existing prototypes.

B. Requirements and constraints for dc protection and testing

The system-level protection of MTdc grids needs to consider the coordination between IEDs, dc CBs, and converters to secure the operation of a large meshed MTdc grid. If the whole operation environment of dc protection is considered, the requirements or constraints for the operation of ac/ dc power grids need to be checked [9], [24]. The development and the investment of MTdc grid protection is a tradeoff between the costs and the availability. The constraints for MTdc grid protection are imposed by the following.

(i) *The limits of MTdc system components:* The maximum acceptable time for dc fault clearing is mainly limited by the overcurrent capability of the power electronics of the HVdc converters, and it also depends on the converter topology. Moreover, the dc CBs applied at HV levels must be able to absorb the energy of the fault current by the surge arresters during the fault current interruption.

(ii) *The stability of the control system in the MTdc grid*: The control system responsible for the control of the voltage and the power flow to ensure stability of the MTdc grid imposes a limit on system-level protection. The related criteria and the stability limits have been discussed in CIGRE technical brochure 657 [9].

(iii) *The stability of ac systems:* The loss of power due to a dc fault should not exceed the maximum loss of infeed as designed, according to the ac grid codes of specific power systems. Furthermore, dc faults should be cleared in a timely manner to avoid instability issues in the ac grid.

When local dc protection is considered, the requirements can be listed as follows:

- Functional requirements, as described in Table 1

TABLE 1 Functional requirements for dc protection [24]

Protection Functional requirement	**Definition**
Sensitivity	Detection of every dc fault including high impedance faults
Selectivity	Operating only after fault occurence, and only if the fault is in related protection zone
Speed	To be fast enough to interrupt faults before they may damage grid equipment
Reliability	To perform a required function under given conditions for a given time interval, i.e. security and dependability
Robustness	Having the ability to detect dc faults in normal operation mode as in degraded operation mode, and to discriminate faults from any other operation occurrence (set-point changes, etc)
Seamlessness	After the fault clearance, the remaining part of the system should continue operating in a secure steady state

- Requirements on protection system components

The requirements for the components such as measuring, detecting and acting components can be determined according to how long the system can sustain a particular disturbance. The MTdc grid protection philosophy is fundamentally determined by the selectivity of the protection devices and the way of dc fault current interruption development. In order to effectively implement dc protection algorithms and meet the speed requirement, the non-conventional instrument transformers with a few megahertz bandwidth, e.g., fibre optic current/voltage sensors [39], need to be adopted.

The main technologies and the bandwidth of today's instrument transformers are summarized in Table 2. As an example, the Rogowski coil has attracted much attention in the electric power industry, as it can meet the requirements of dc protection for frequency bandwidth and dynamic accuracy due to its superior performance, inherent linearity, outstanding dynamic response, wide bandwidth, and without magnetic saturation. These features can support accurate and reliable data measurement to trace the faulty dynamics in the dc system for those protection applications when the Rogowski coil is combined with the shunt capacitor [8].

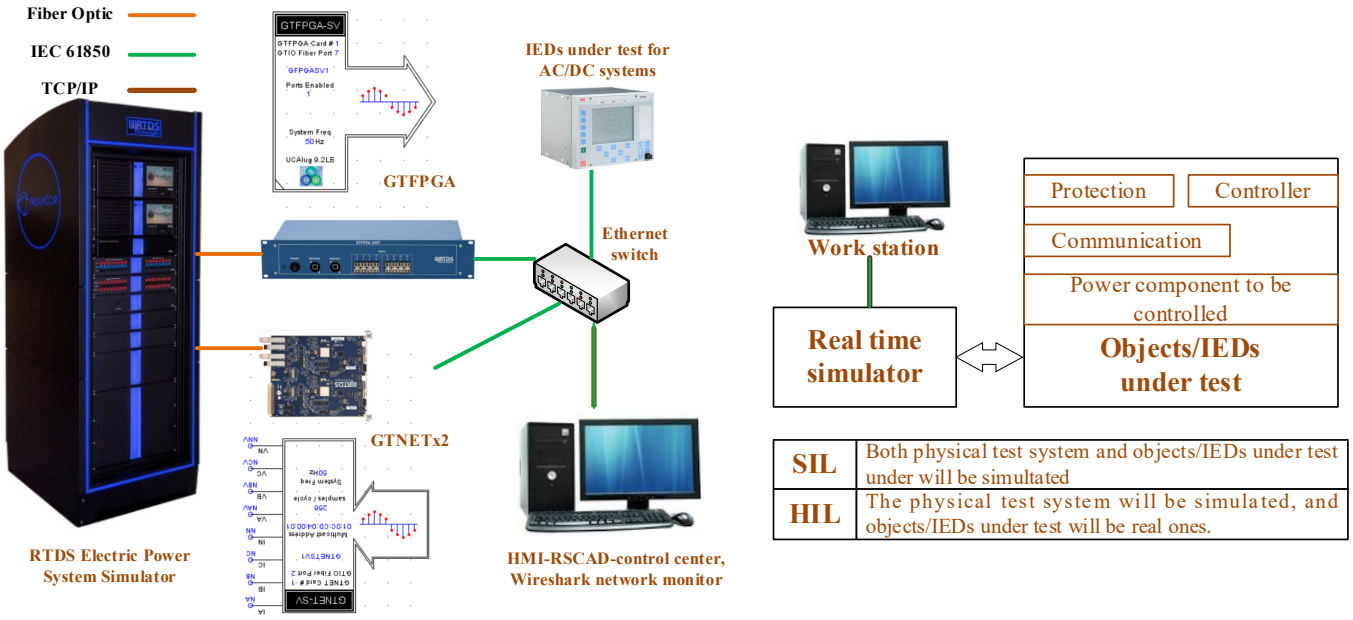
The digital interface of instrument transformers for both ac and dc applications is specified by IEC 61869-9 [40]. To perform general measurement and protective data processing, the typical sampling rates for ac and dc measurements are 4.8 kilo samples (ksa)/s and 96 ksa/s, respectively. The fault current interruption capability of the dc protection system is determined not only by the capability of dc CBs but also by the system design of the converter and the current limiter. The speed requirement and the interaction between the dc CB and dc protection can be briefly observed in Figure 3. If more details and testing of dc protection are considered, the specific hardware, software, and communication protocols should be investigated [9], [29]:

- *hardware platform:* e.g., an HIL testing platform based on the real-time digital simulator (RTDS), protection IEDs, physical interfaces, and connections
- *software platform*: i.e. power system and control function models, reasonable test cases, protective function algorithms, and dc CB models;

- *communication*: a hardware or software-defined data transmission network for the links between any combinations of the hardware platforms and software platforms.

TABLE 2 Technologies and bandwidth of instrument transformers [8]

Type	Technology	Bandwidth	Application
CT	Electromagnetic (iron-core)	few kHz	ac
	Hybrid electro-optical (combined shunt and Rogowski coil)	few MHz	ac/dc
	Fiber optic current sensor (magneto-optic effect)	few MHz	ac/dc
	Zero-flux (dc Current Transformer)	few hundred kHz	dc
	dc Zero-flux (Hall-effect current transformer)	few hundred kHz	dc
VT	Inductive voltage transformer	few kHz	ac
	Capacitor voltage transformer	few kHz	ac
	Compensated RC-divider	few MHz	ac/dc
	Fibre optic voltage sensor (magneto-optic effect)	few MHz	ac/dc



(a) One example based on RTDS and IEC 61850 based ICT infrastructure (b) General groups of real time simulation: SIL and HIL

Figure 4 Real time simulation platforms

An example of a real-time cyberphysical testing platform can be seen in Figure 4(a). The test MTdc grid is first developed in RSCAD software and then simulated in real time using RTDS [41]. To simulate detailed models of HB MMC converters, dc CBs [26], [42] in small time-steps, and new dc protection algorithms, new generations of processors in RTDS are preferred. Furthermore, the IEC 61850-9-2LE sample value communication [43] has been developed based on one GTFPGA unit and one GTNETx2 card, together with the related software interface configuration within the RTDS racks.

The sample values of the critical measurement points in the MTdc grids are provided by GTFPGA-based merging unit functions to the local Ethernet network, while the GTNETx2 card is configured to obtain the sample values from the local network for the protection functions modeled in RTDS. The related message flows can be monitored and analyzed based on the manageable Ethernet switch and Wireshark network analyzer [44]. If the protection IEDs under test for ac/dc systems are available with the required communication interfaces, then the application performances of IED under test can be easily testified based on this simulation platform in Figure 4(a).

There are many different schemes using real time simulation for the testing and commissioning of protection, control, and communication systems, which can be mainly categorized into two groups, i.e., software in the loop (SIL) and HIL. A simple illustration can be seen in Figure 4(b). In an SIL scheme, both the controller and the physical test system are simulated by RTDS, when it is difficult to access IEDs. In an HIL scheme, the IED under test is accessed and connected to the real-time simulator through specific interface converters, e.g., amplifiers and sensors [45]. The test platform shown in Figure 4(a) can be regarded as SIL with additional communication links for IEC 61850-9-2LE, when the object under test is the simulated relay model in RTDS. When the object under test is the protection IEDs, then the related testing schemes based on the test platform in Figure 4(a) belong to HIL schemes.

In an RTDS-based simulation platform, the network solution technique is performed by nodal analysis. This is different from the OPAL-RT-based simulation, which is realized by a state–space nodal method to perform network calculations [46]. For every real-time simulator, the online simulation is discrete time based. With a large number of data points computed within a given power system cycle, the online simulation approximates the continuous time power system appropriately [47].

III. Test Procedures for MTdc Grid Protection

A. The structure of test procedures for dc protection

The script of protection performance testing is depicted in Figure 5. The blocks with black arrows represent the normal progress of fault development and protection performance, whilst the blocks with red arrows represent the evaluation and testing progress.

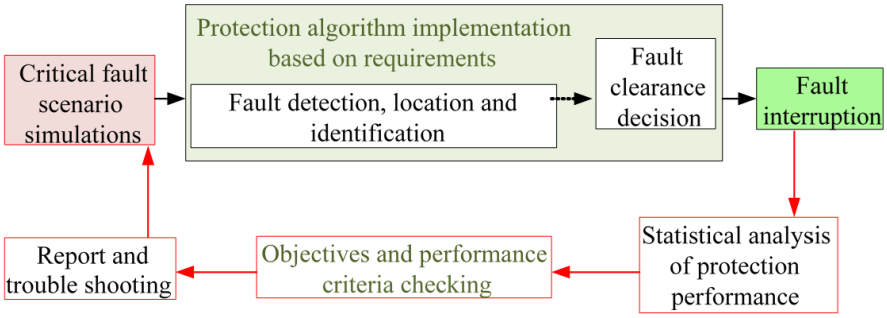


Figure 5 The general script of protection performance testing

The general testing steps for the dc protection can be described as follows:

Step 1: Fault scenarios: simulation based fault studies

Step 2: Statistical analysis of system level performance

Step 3: Threshold setting adjustment

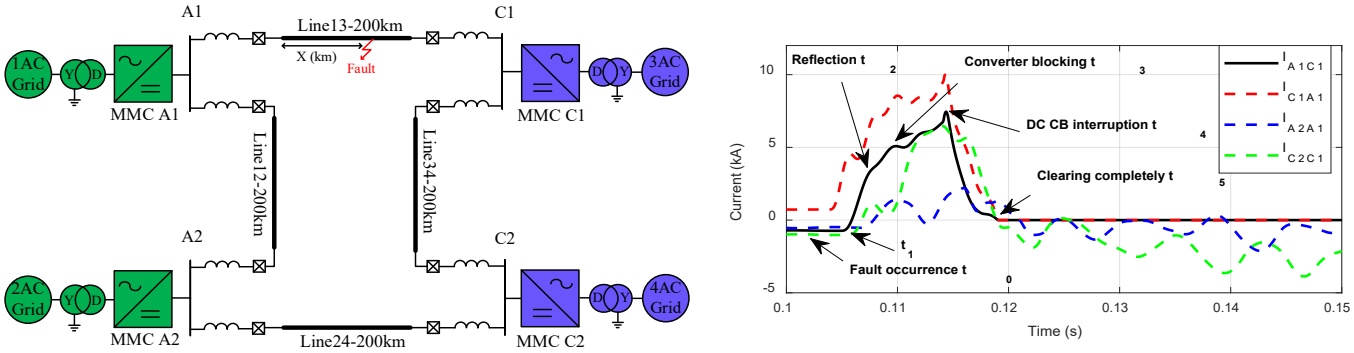
Step 4: Criteria checking

Step 5: Report and trouble shooting.

The details of these five steps are different when the dc protection function is different, e.g., primary protection testing and backup protection testing are conducted with different fault scenarios, which will be introduced later.

B. Test circuit and fault scenarios

Figure 6 shows an example of a simulated dc fault current in the four-terminal meshed HVdc grid based on the testing platform in Figure 4(a). This MTdc grid is built on an HB MMC and cable lines, and each cable is terminated by mechanical dc CBs [6] and series inductors. The related specification of the MTdc grids is included in Table 3, and more data on the system and controllers can be found in CIGRE technical brochure 604 [48]. It should be noted that the MTdc test system, fault scenarios, and the current waveforms are simulated and produced based on the RTDS simulation platform, which aims to testify the system-level performances of studied protection IEDs. The main time-step in RTDS is set as 50 μs, while VSCs and dc CBs make use of a small time-step of 3.124 μs.



(a) Four-terminal HVdc test system in RTDS (b) Fault interruption progress

Figure 6 Fault interruption progress in the 4-terminal HVdc grid

TABLE 3 The ac grids and MMCs parameters

Parameter	Converter	
	MMCs 1, 2, 4	MMC 3
dc voltage	±200kV	±200kV
Converter ac voltage	220kV	220kV
Rated Power	800MW	1200MW
Number of SMs per arm	400	400
Arm resistance R_{arm}	0.54Ω	0.36Ω
Arm reactor L_{arm}	29mH	19mH
Arm capacitance C_{arm}	25μF	37.5μF
Transformer leakage reactance	0.18p.u.	0.18p.u.
ac grids		
1ac grid and 2ac grid	380kV	
3ac grid and 4ac grid	145kV	

When a fault occurs at the end of the line between converter A1 and C1 at time t0=0.1s, the related travelling wave reaches the terminal A1 at t1=0.1056s. Then, the dc fault current quickly increases, and its rate of rise is limited by the series inductors. In the first millisecond, successive reflections (e.g., at t2) occur, caused by waves traveling along the line between the fault location and the protection system location. Furthermore, other terminals start to feed into the fault current. At t3, converter A1 blocks its insulated-gate bipolar transistors (IGBTs), and the dc fault current is fed by the ac side. All converters in the system are blocked around t3. At t4, the mechanical dc CB located at A1 opens to interrupt the fault current increment. Eventually, after t5, the fault is completely cleared by dc CBs installed in the faulty line between A1 and C1. A detailed overview of the phenomena, which occur during the fault, is given in Figure 7.

It should be noted that the dc grid protection considered in this paper excludes the converter protection that is normally designed by different converter vendors. However, in the real or simulated cases, these two protection systems are incorporated with each other. In the simulation example in Figure 6 and 7, the recommended parameters from [48] are directly adopted for the converter protection, e.g. the valve current threshold of 6 kA and dc bus voltage threshold of 0.9 per unit are considered. The fault current withstand capability of the freewheeling diodes is set based on their own design parameters, e.g. the thermal capability limits.

To deal with a possible current imbalance in the combination of diodes for MMC, the thermal capability limit could be calculated based on the minimum current thermal limit of each diode, which could resort to related reliability test. Moreover, when a hybrid dc CB is applied instead of mechanical dc CB, the break time can be improved from 8 to 2 ms approximately [8], which can release the thermal stress on the remaining components in the fault current loop.

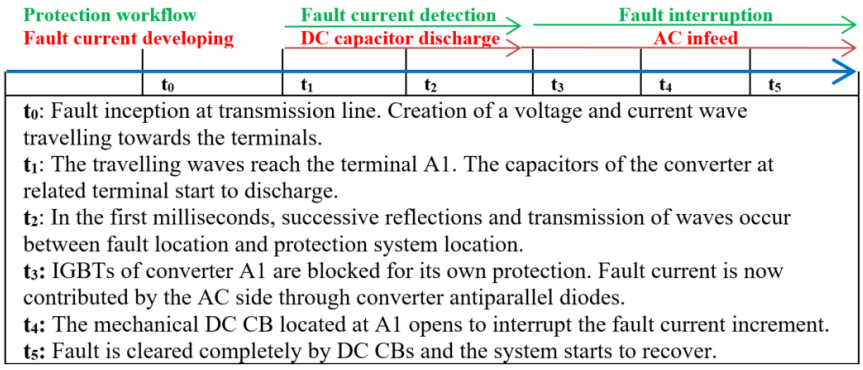


Figure 7 The progress of fault clearance

Based on the progress and mechanism analysis during the dc fault development and interruption, the critical parameters influencing the dc fault current and the related dc protection system can include the type of transmission lines, fault resistance, dc-side inductance, dc-side capacitance, converter blocking instant, ac system strength, earthing system, converter topology [24]. The impact of these parameters is briefly explained in Table 4. In addition, the sampling frequency is critical for the signal processing and the operation speed of dc protection; a sampling frequency of 96 ksa/s is assumed here, considering the IEC 61869 standards [40].

TABLE 4 The critical parameters influencing the dc fault current

Critical parameters	**Influence analysis**
Transmission line type	The characteristic impedance of OHL is larger than for cables, which causes current waves to be smaller in amplitude. The traveling wave speed of OHL is about the speed of light, whereas for cables this is half of to 2/3 the speed of light.
Fault resistance	An increasing fault resistance leads to a smaller prospective steady-state fault current.
dc side inductance	Increasing the dc side inductance decreases the rate of rise of the current but does not make impact to the prospective steady-state fault current.
dc side capacitance	A dc side capacitance (as e.g. used in two-level topologies) initially provides a large discharge current.
Converter blocking instant	The converter blocking instant determines the amount of discharge of submodule capacitors. Delaying the converter blocking instant increases the capacitor discharge.
ac system strength	The ac system strength mainly determines the value of the prospective steady-state current. An increased ac system strength leads to an increased value of the prospective steady-state current only limited by the short circuit impedance of the connecting equipment such as transformers.
System earthing	Low impedance earthing results in higher fault current and high impedance earthing leads to a lower fault current. Earthing impedance and topology also has effect on fault transient behaviour.
Converter topology	With new VSC converter topology concerned, HB MMC cannot block the fault current, since there is always an uncontrolled current path via the freewheeling diodes in this topology; and FB MMC can block the fault current and reach current zero, since there are no fault current paths avaiable when IGBTs has been switched off during the fault period.

C. Test procedures

For the testing of a specific protection IED, the specifications of the protection functions should be provided by the IED vendor first. The critical ratings and the performance limitations of the basic protection functions, e.g., input, output, detection, directional determination, measurement accuracy, sampling rate, and so on, should be declared by the IED vendor as well. According to IEC 60255-1 [30], the general type (unit) testing is used to verify the new hardware/software designs against the product specifications and the standards. However, the verification procedure for the overall system is important to ensure that equipment is in accordance with its specifications, all functions perform correctly during the initial measurement at the beginning of the test sequence, and it maintains its design characteristics throughout all of the specified tests.

With the consideration of the fully selective fault-clearing strategy, the primary protection algorithms should be implemented together with the suitable dc CB models. The operation time and the sequences of the protection system can be obtained directly based on the RTDS models, as shown in Figure 5. Then, the failure rate of the primary protection can be easily obtained based on the simulated performances. Different test scenarios will be required for different dc system configurations. It is assumed that the testing system is developed for a symmetric, monopole, HB MTdc grid, a fully selective fault-clearing strategy, and related dc CBs. The general testing progress of the primary protection's system-level performance is depicted in Figure 8. The detailed procedures of the related testing steps are listed as follows:

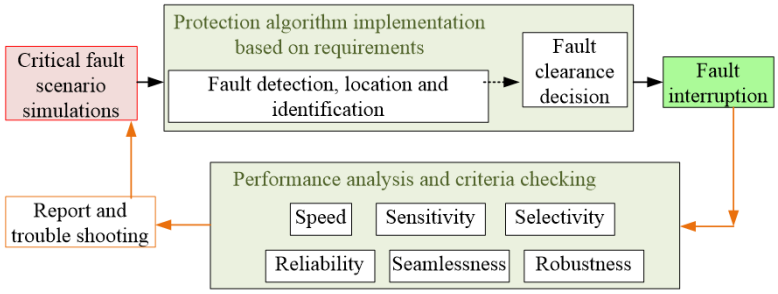


Figure 8 The general process of primary protection performance testing

TABLE 5 The critical testing parameter for performance testing

Testing parameter	**Typical values**	**Testing parameter**	**Typical values**
Fault resistance	0-400 Ohm Variation: 0, 25, 50, 100, 150, 200, 250, 300, 350, 400 Ohm	Fault location	0%-100% of the line with reasonable interval, $0\%_{L-}$, $0\%_{L+}$, 20%, 40%, 60%, 80%, $100\%_{L+}$, $100\%_{L-}$, 110% 'L+': the fault is applied at the end of the line before the series inductor. 'L-': the fault is applied after the series inductor close to the bus.
Fault type	PTP1: pole-to-pole permanent fault PTP2: pole-to-pole self clearing fault PTG1: pole-to-ground permanent fault PTG2: pole-to-ground self clearing fault PTG11: positive pole-to-ground permanent fault PTG12: negative pole-to-ground permanent fault PTG21: positive pole-to-ground self clearing fault PTG22: negative pole-to-ground self clearing fault	Series line inductor	0-200 mH with reasonable interval, 0, 10, 50, 80, 100, 120, 160, 200 mH

Step 1: Fault scenarios simulation-based fault studies

Table 5 shows the critical testing parameters and the related typical values, which could be different according to different testing systems and testing objectives. In order to perform multi-case testing and to record the responses of the objective protection systems or protection IEDs, these critical testing parameters can be changed in the proposed scopes. However, the choice of these parameters are

system dependent and are generally decided by the user/vendor through the knowledge of system studies and operations.

Step 2: Statistical analysis of system level performance

The basic accuracy checking of protection characteristics and the operation time based on the performance analysis will be mainly conducted in this step. The statistical analysis of IED system level performance is important in order to find a fault type based probability distribution, which is the precondition to obtain and check the related criteria. The classical method-transient overreach analysis used in IEC 60255-121 [49] is adopted here for the accuracy testing.

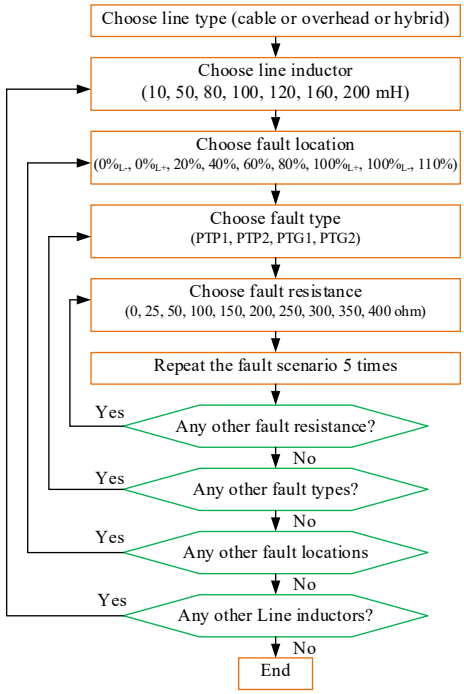
An example of the testing procedures can be seen in Figure 9 (a). With the chosen testing parameters in Figure 9 (a), the multi-case testing can be easily conducted. The repeating sequence of 5 times is a common practice in the IED testing in terms of reliability checking.

Based on the recorded test performances, the operation times can be determined in a statistical form. For example, the test data at the three fault positions (0 $\%_{L+}$, 50 % and 80 %) and with L = 100 mH for the line inductor will be considered. This will result in a total of 1800 (600 operation times for the cable line tests, 600 operation times for overhead line (OHL) tests, and 600 operation times for hybrid line tests) obtained operation times. This is equal to 450 operation times for each fault type. To create a fault type distribution in the operation time statistics, the following weights are given to the available data according to the fault categories defined in [50].

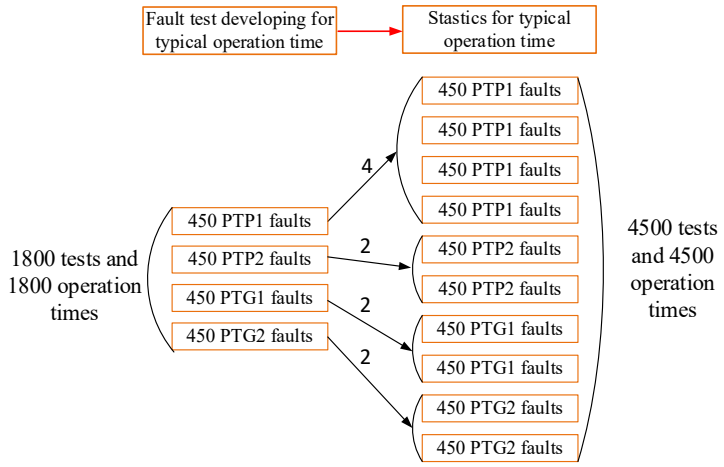
1) Test results for PTP1, will be weighted by a factor of four.

2) Test results for the fault type PTP2, PTG1, PTG2, will be weighted by a factor of two.

3) Test results for other faults will be weighted by a factor of one. These factors are defined according to the fault occurrence probability and its impact on the system.



(a) System level accuracy testing



(b) The statistics for typical operation time

Figure 9 The general procedures for system level performance analysis

The weighting is done by simply repeating the available results. Figure 9 (b) shows the fault statistics of the typical operation time. Totally, 4500 operation times are available for the statistics.

These tests are aimed at determining the accuracy of the operation times of primary functions. They are based on monitoring the time difference between the arriving instant of the first fault travelling wave to the line end and the operation output signals of the IED. The time range and the associated classes based on the operation time could be defined based on the collected data set. For example, the minimum and maximum operation times in the data set are: min_T=1512 us, max_T=4167 us. Thus, a range of operation time could be defined as [1500, 4200] us, similar to that reported in [30]. The classes of the performances of the IED under testing can be defined by making average groups with an interval of 300 us, as can be seen in Table 6. Here, it is necessary to point out that under IED class, a particular operation time range is chosen.

TABLE 6 The operation time classes of target IED

Class	**From t ≥ [us]**	**To t ≤ [us]**	**N**	**% N**
Class 1 (min=1500 us)	min	min + 300	The number of operation times belonging to each class (n)	The probability of N for each class (n)
Class 2	min + 300	min + 600		
Class 3	min + 600	min + 900		
Class 4	min + 900	min + 1200		
…				
Class n	min + (n-1)×300	min + n×300		
…				
Class M (max=4200 us)	min + (M-1)×300	max		

The number of operation times belonging to each class (N), with 300-us resolution, is counted to show the probability distribution of the operation times. The probability of N for each class is calculated and the values can be filled in Table 6. These procedures are related generally for all IEDs, and the table refers to the IED that will be tested.

Step 3: Threshold setting adjustment

The setting rules, variation range and the accuracy of the thresholds will be introduced and analyzed in the type testing of protection IED specifications. However, for the system level testing, more influencing factors will be involved and the corresponding thresholds can be optimally adjusted to achieve better system-level performance. Thus, the test settings of the thresholds can be expressed as percentages of the available range, with 0 % representing the minimum available setting and 100 % representing the maximum available setting. Similarly, 50 % would represent the mid-point of the available setting range. The actual setting to be used can be calculated using the following formula:

$$S_{AV} = (S_{MAX} - S_{MIN})X + S_{MIN} \qquad (1)$$

where S_{AV} is the actual setting value to be used in the test; S_{MAX} is the maximum available setting value; S_{MIN} is the minimum available setting value; and X is the test point percentage value expressed in the test methodology. For example, assuming the available setting range is 0.1-5 A and 40% test point percentage, the actual operating current settings will be 2.06 A.

To tune the threshold setting, the testing procedures can be performed with the consideration of variable threshold setting values that will result in the determination of the most accurate threshold setting. For example, if the pre-calculated threshold setting is 63.5%, threshold setting values change from 62 to 65 % by 0.5 %, then the related testing procedures can be seen in Figure 10. The statistics

data analysis can be conducted using weighting factors of step 2 to obtain the best threshold settings corresponding to the highest probability of correct operation.

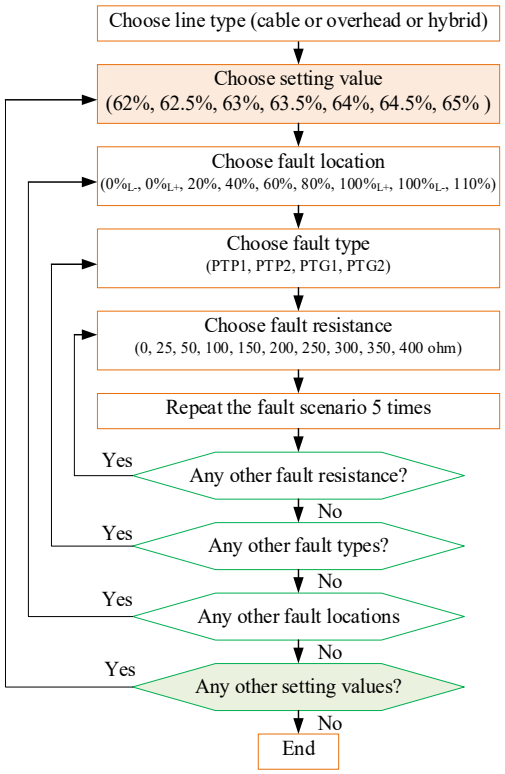


Figure 10 The testing procedures for threshold setting adjustment

Step 4: Criteria checking

After the verification of the accuracy and the threshold settings for the specific system operation conditions, the primary protection functions need to be tested when the objectives of protection system performance are met. The critical criteria are speed, sensitivity, selectivity, reliability, seamlessness and robustness, which have been mentioned in Section II. To develop these criteria, the performance of the dc protection is divided in three different operations:

- *Correct operations:* The protection system operates for faults in its protection zone within the required time
- *Failed operations:* The protection system does not operate for faults in its protection zone within the required time
- *Incorrect operations:* The protection system operates for faults out of its protection zone

Then, the related qualification criteria can be expressed as follows:

$$\text{Pclasses.speed} = \frac{Number\ of\ correct\ operations}{Total\ number\ of\ tests} \quad (2)$$

$$\text{Pclasses.sensitivity} = \frac{Number\ of\ correct\ operations}{Total\ number\ of\ tests} \quad (3)$$

$$\text{Pclasses.selectvitiy} = \frac{Number\ of\ correct\ operations}{Total\ number\ of\ tests} \quad (4)$$

$$\text{Pclasses.security} = \frac{Number\ of\ correct\ operations}{Total\ number\ of\ correct\ and\ incorrect\ operations} \quad (5)$$

$$\text{Pclasses.dependability} = \frac{Number\ of\ correct\ operations}{Total\ number\ of\ correct\ and\ failed\ operations} \quad (6)$$

$$\text{Pclasses.reliability} = \frac{Number\ of\ correct\ operations}{Total\ number\ of\ tests} \quad (7)$$

$$\text{Pclasses.seamless} = \frac{Number\ of\ effective\ operations}{Total\ number\ of\ tests} \quad (8)$$

$$\text{Pclasses.robustness} = \frac{Number\ of\ neccessary\ operations}{Total\ number\ of\ tests} \quad (9)$$

where Pclasses.speed, Pclasses.sensitivity, Pclasses.selectvitiy, Pclasses.security, Pclasses.dependability, Pclasses.reliability, Pclasses.seamless, Pclasses.robustness represent the probabilities of related operations for the checking of speed, sensitivity, selectivity, security, dependability, reliability, seamless and robustness on the protection IED under the test, respectively.

For the checking of each criterion, the critical testing parameters are revised according to specific requirements, which can be compared and observed from Figure 11. The testing procedures on speed, sensitivity, selectivity, and security can be seen from Figure 11(a), (b), (c), and (d), respectively. Thus, the meanings of (2), (3), (4) and (7) are different with different testing parameters, even though they are in the same form.

Since the speed of the primary protection is related to the time when the current reaches the dc CB interruption capability, a fast breaker could allow more complex and time-consuming algorithms to be applied. Thus, the different dc CB types are considered in the test procedures of speed checking as shown in Figure 11 (a). For the sensitivity checking in Figure 11 (b), those testing parameters, which have big impacts on operation quantities to give the possible minimum faulty condition, will be considered more, e.g., high fault impedances, different line inductors, converter blocking instants and fault locations.

PTG faults will be mainly considered in the sensitivity checking. For the selectivity checking, the fault resistance, the fault location, the fault type and the line inductor will be chosen as critical testing parameters with the focus to consider more on the borders of protection zones. The related changes on the related parameters can be found in Figure 11 (c).

For the security checking, the unnecessary protection operations could result from the loss of selectivity and sensitivity due to wrong thresholds or operation condition changing, e.g., dc line outage (dcL), energization/de-energization of a converter, and so on. Thus, in an addition to the testing parameters considered for selectivity and sensitivity, the operation condition changes due to dc line outage and energization/de-energization of a converter that needs to be considered in the security related testing. Neighboring dcL1 and de-energization of a local converter [converter event 1 (COE1)] are added in the fault type block in Figure 11 (d).

After these multi-case tests conducted by the corresponding testing procedures, the fault data statistics analysis will be derived based on the user-defined ranges of testing parameters, which have been described in the former steps. Then, the related probabilities can be calculated based on (2)-(5). For the latter, the four criteria checking are related to (6)-(9), and the testing procedures or work flowcharts are similar to the first four criteria checking, but with different focus. The Dependability is highly related to the Sensitivity and the Speed. Thus, in the related testing, the similar testing parameters and critical time ranges based on dc CB types can be chosen as critical testing parameters. For the reliability, the total number of tests is the sum of the tests performed for the criteria of Dependability and Security.

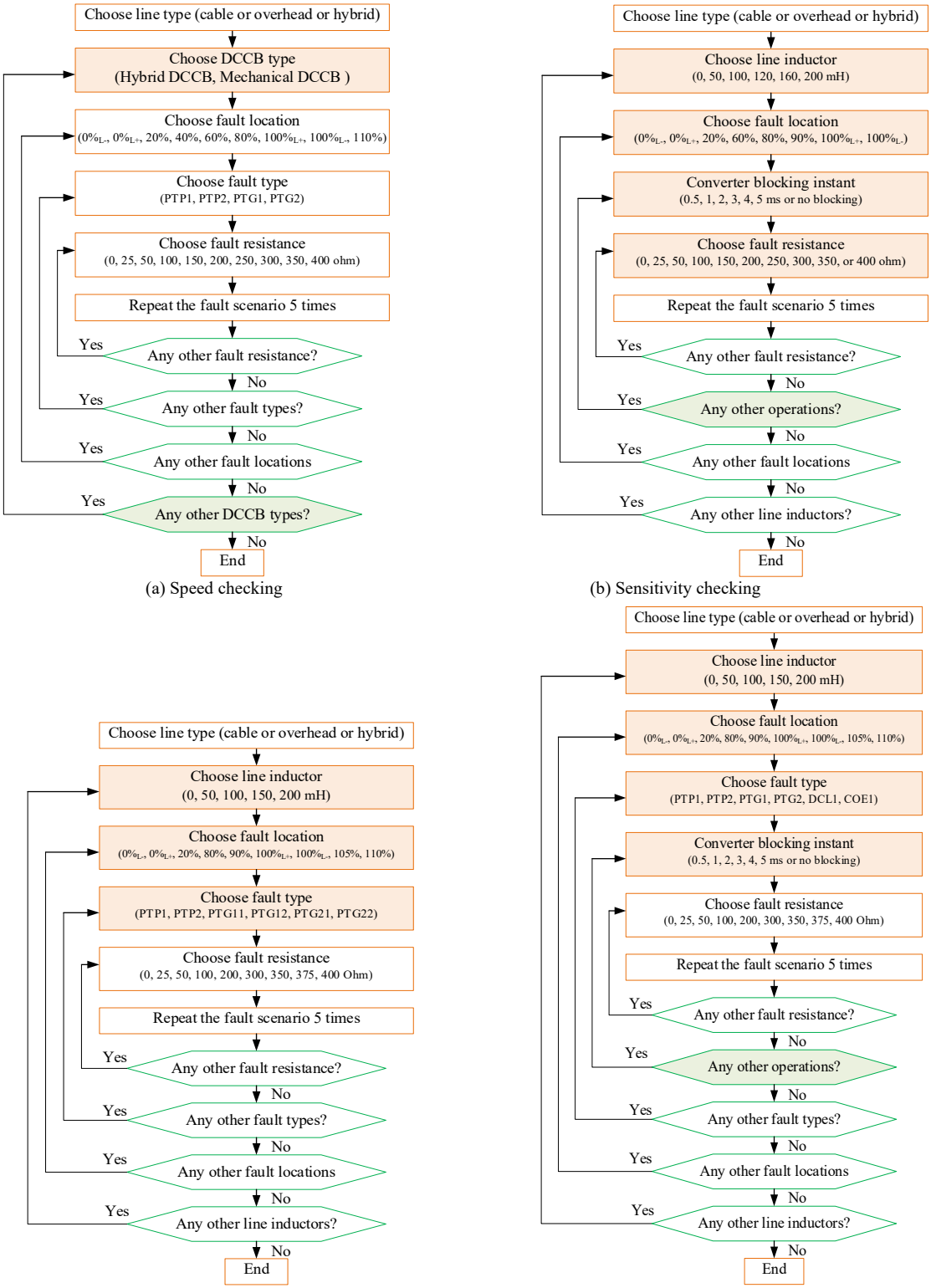


Figure 11 The testing procedures for the checking of different criteria

The Seamlessness of the MTdc grid protection refers to the ability of holding the remaining part of the grid to continue operating in a secure state after the fault clearance [51]. This is related to the continuous adaptability of the MTdc grid protection when the system transfers from a normal operation condition to N-1 or N-k conditions due to a fault clearance. In this case, the effective operations in (8) mean the correct operations of the protection with predefined settings (for specific operation conditions) in a post-fault stage, such as N-1 or N-k stages.

The Robustness of the MTdc grid protection refers to the detection of faults in normal or degraded mode and the discrimination from other operational events in the grid [50]. The difference with respect to Seamlessness is that the adaptability to both normal and degraded operational modes is required but continuous operation transition is not. Moreover, the discrimination from any other operational events causes the Robustness to become a kind of reliability as well. Accordingly, in this case, the necessary operations in (9) mean the correct operation of the protection with different predefined settings for different stages; those being adaptive and available for several operation conditions.

Step 5: Report and trouble shooting

In this step, the summary of the data analysis should be given based on the work steps above, the limitations and related trouble shooting should be registered as illustrated in Figure 8, so that this can be improved for all work steps in the future work. For the backup protection testing from the viewpoint of the IED under test, the different actions of the backup protection should be mapped to the backup fault clearing options given for fault interruption and based on categories in Figure 2 [52].

Due to rigorous requirements on the time of fault clearance and communication delays, only local backup will be considered here for the dc protection system. The general testing progress of the backup protection performance is depicted in Figure 12. The testing considerations and steps are similar to those in the primary protection testing, but the failure detection is a critical function of backup protection. Here, two kinds of failures have been considered, i.e. the failure of primary protection and the failure of dc CB operations.

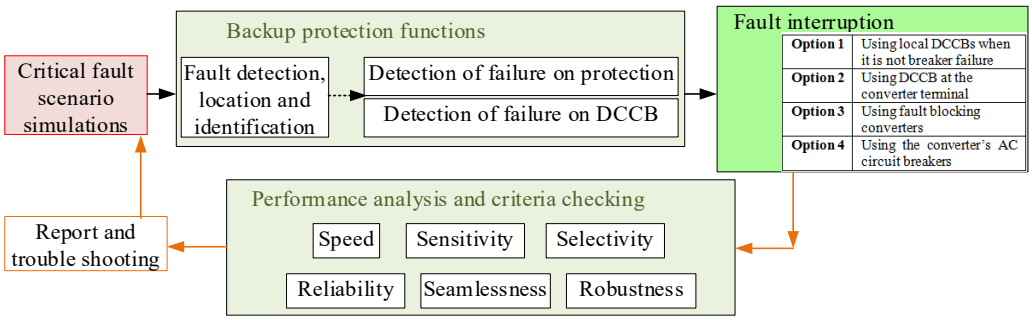


Figure 12 The testing progress of backup protection performance testing

Moreover, the test cases for the backup protection testing need to be processed based on previous cases in the primary protection testing. The cases used in the testing of Dependability checking can be adopted directly here, since some non-dependable operations (e.g. non-tripping signals) in the required time interval are regarded as the failure of primary protection. Inversely, the failures of dc CB operations will be tested with those dependable cases, which are mainly induced by dc CB' own capabilities and features. Thus, when the failure of primary protection and the failure of dc CB operation are identified, the backup protection functions will be initiated to choose one of the backup options of fault interruption to execute suitably. These two types of failures and their derived rules can be seen in Figure 13. Based on the obtained cases, similar performance analysis of related backup protection functions can be undertaken accordingly.

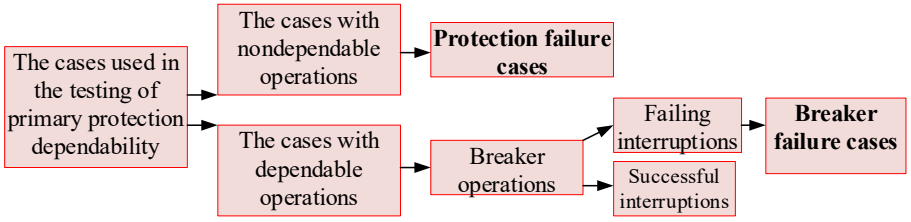


Figure 13 The evolution from primary protection to backup protection testing

IV. Suggestions on Technical Guidelines for DC Protection Testing

A. Definitions of Test Environment and Scenarios

The critical requirements and testing parameters of the test environment and fault scenarios are varied, as the target MTdc grid under study and applied protection algorithms are changed. In case a reduction of the number of test scenarios is needed from several tens of thousands scenarios [Figure 9 (b)] to a reasonable number, it is proposed to define test scenarios considering the limitations of the protection algorithms. For example, when an algorithm is intrinsically limited with respect to the fault resistance, the fault scenarios are determined with more focus on this parameter.

If more practical parameters are considered in the test environment, some standard or proposed models can be improved and adapted to the actual grid under study with the consideration of:

- The types of transmission lines including cable, overhead and hybrid lines
- The length, parameters (resistance, inductance and capacitance) and structure of transmission lines
- More fault types and resistances (e.g., self-clearing fault in case of overhead lines, and faults involving metallic return wire in bipolar HVdc grids with metallic return)
- More MMC converter station structure including monopolar and bipolar
- The converter station earthing including earthed (earth return or metallic return) and unearthed systems, and earthing method
- More converter topology including two level and MMC (FB, HB and so on)
- The dc side capacitance
- The control methods and control modes of the converters (PV, PQ etc.)
- More type of dc CBs and other switchgears
- HVdc grid ratings such as voltage, current and transferred power
- Different ac side equivalent system

With respect to fault scenarios, besides those parameters mentioned in Section III, (i.e. fault resistance, fault location, dc-side inductance, and converter blocking instant) the measurement accuracy, sampling rate and noise level on voltage and current can be considered as well.

B. System Level Assessment of dc Protection

After a test of different protection algorithms is carried out, the performance of the algorithms can be analyzed. The algorithms will

show different performance in terms of different requirements. Therefore, it is necessary to classify the performance of the protection algorithms considering each requirement or criterion. Here, the performance obtained by performed tests in Section III, can be classified into low, medium and high performance classes for all protection algorithms based on the value of corresponding qualification criteria. In order to determine the range of qualification criterion values of these classes for each requirement, the computed qualification criteria of each requirement for all protection algorithms are sorted in a decreasing order. Then, these qualification criteria (of a particular requirement) and their corresponding algorithms are divided into three groups with equal (in the case of an odd number of algorithms) or almost equal (in the case of an even number of algorithms) members; group 1, 2 and 3. An example with the consideration of nine algorithms and speed criterion has been given in Table 7.

The range of each performance class is defined by taking into account an average value of these three groups in the following way:

- High Performance ≥ average of group 1
- average of group 2 ≤ Medium Performance < average of group 1
- Low Performance < average of the group 2

It is also possible to use minimum and maximum values of the groups instead of average values:

- High Performance ≥ minimum of group 1
- minimum of group 2 ≤ Medium Performance < minimum of group 1
- Low Performance < minimum of the group 2

This classification method can be applied to all the requirements in Table 1. Then, the performances of the algorithms can be compared considering each requirement. It should be noted that the range of classes of each requirement may be different from other requirements, and may also differ for different IEDs. Because the test procedures and assessment methods are designed in a systematic way, the efficiency for the full performance assessment of IEDs will be higher and more difficult to quantify than the simple testing methods used in [32]-[37] for only single protection algorithms. By comparing to single protection algorithm testing with less performance requirement, the computation efforts of the proposed testing method will be made to systematically consider all the requirement criteria, i.e. speed, sensitivity, selectivity, security, dependability, seamless and robustness, which are necessary for the industrial application and the certification of protection IEDs. Compared to IEEE and IEC standards for ac protection testing, the proposed methods are more advanced and applicable for dc protection IEDs. The extra system level assessment method proposed in the paper can help evaluate the different kinds of dc protection algorithms implemented in the protection IEDs. It should be noted that the efficiency of the proposed method can be quantified by comparing the test results and practical results recorded in practical multi-terminal HVdc grids. However, performing such a study needs a reasonable amount of practical information about the performance of IEDs and the protection algorithms, which implies longer time exploitation and operation of multi-terminal HVdc grids. At this moment, such information is not available because there are a few newly commissioned practical multi-terminal HVdc grids and even fewer protection IEDs equipped with different protection algorithms.

TABLE 7 An example for the determination of performance classes on speed

Groups	Algorithms	Pclasses.speed (%)	Classes	Range (%) (Average method)	Range (%) (Min & Max method)
Group 1	Alg. 5	99	High	≥ 97.66	≥ 96
	Alg. 3	98			
	Alg. 4	96			
Group 2	Alg. 1	94	Medium	91.66 - 97.66	89 - 96
	Alg. 6	92			
	Alg. 8	89			
Group 3	Alg. 2	85	Low	91.66 <	89 <
	Alg. 9	83			
	Alg. 7	80			

V. CONCLUSION

This paper first identifies challenges for system-level testing of MTdc grid protection, and it exploits the already available standard procedures for ac protection system testing in order to develop MTdc grid protection testing procedures. It also applies the knowledge of dc protection testing, and makes recommendations based on the developed procedures and guidelines for both primary and backup dc protection functions. The specific performance criteria are designed, based on multi-case testing and statistical analysis, with the considerations of related critical testing parameters for the functional requirements of dc protection. Suggestions for dc protection testing environment and fault scenarios and the assessment methods of the algorithms' performance are provided, which will be important for the future standardization of MTdc grid development and related protection testing.

VI. ACKNOWLEDGMENT

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VII. BIOGRAPHIES

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