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High Frequency Multicell Cascaded Quasi-Square-Wave Boost Converter

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Abstract—This paper presents a multicell cascaded quasi-square-wave (MCQSW) boost converter for non-isolated DC-DC applications with high voltage conversion ratios. The MCQSW boost converter is designed to operate at high frequencies and can achieve zero voltage switching (ZVS), soft charging, current sharing, and automatic voltage balancing. In the MCQSW converter, many boost cells are connected in parallel in series to distribute the high input current; multiple output capacitors are stacked in series to achieve high output voltage. The multicell parallel-input series-output configuration can significantly extend the voltage conversion ratios of the traditional QSW boost converters while maintaining low power conversion stress and enable low input current ripple due to interleaving. The high-frequency ZVS operation is enabled by an analogy control circuitry which can operate up to a few MHz. A 700 kHz to 5 MHz, 15 V-180 V (1:12 conversion ratio), 250 W MCQSW converter was built to validate the effectiveness of the MCQSW converter achieving a peak efficiency of 91%.

Index Terms—DC-DC power conversion, switched-capacitor circuit, high frequency, boost converter, quasi-square-wave converter, interleaved structure, soft-switching, soft-charging

I. INTRODUCTION

Boost converters with high voltage conversion ratios are needed in a wide range of applications including renewable energy, electric vehicles, and grid-scale energy storage systems [1]–[5]. The voltage gain of a traditional boost converter is usually limited due to the need for an extreme duty ratio and poor device utilization [6], [7], especially at high switching frequencies. They do not fully leverage the strength of wide bandgap devices at high switching frequencies. Many efforts have been made to develop non-isolated boost converters with high voltage-gains [8]–[11]. One possible way to extend the voltage conversion ratio of a dc-dc converter is to connect many power conversion cells in series or in parallel [12]. Modular multicell converters with parallel-input series-output configurations are promising candidates to achieve high voltage-gains, low current ripple, and high power density [13]–[15].

It is known that the high power losses from a hard-switching converter degrade the performance of the boost converter to some extent. To address this, many soft-switching techniques have been explored to reduce power losses [6], [7], [16], [17]. For instance, soft-switching converters can achieve zero-voltage-switching (ZVS) or zero-current-switching (ZCS) by utilizing the stray capacitance and inductance in a resonant loop. The quasi-square-wave (QSW) converter, as a representative of the resonant/quasi-resonant converters, features lossless
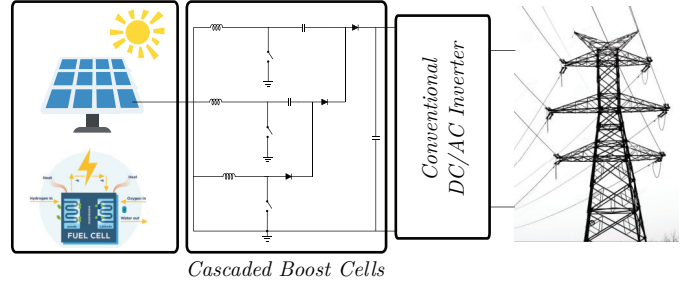

Fig. 1. Block diagram of the power conversion stages with MCQSW implemented in the system. The MCQSW converter fits particularly well to boost power conversion systems with multiple input sources.

transitions and can greatly improve the performance of high-frequency dc-dc converters benefiting from the zero-voltage-switching (ZVS) and zero-current-switching (ZCS) mechanisms [6], [7]. The QSW-ZVS operation is a unique feature of Pulse Width Modulation (PWM) converters operated in the discontinuous conduction mode (DCM). In addition to achieving soft switching, maintaining soft charging in dc-dc converters is critical to achieve high performance at high switching frequencies. In non-isolated high conversion ratio dc-dc converter applications, switched-capacitor circuits are very attractive due to their high efficiency and high power density. Soft-charging techniques can eliminate the charge sharing losses in switched capacitors, allowing switched capacitor circuits to operate at lower frequencies with reduced switching loss and improved efficiency, with a limited capacitor size [11], [18], [20].

Inspired by the above, this paper explores a multicell cascaded quasi-square-wave (MCQSW) boost converter suitable for high voltage-gain and high-frequency applications with zero-voltage-switching and soft charging. As shown in Fig. 1, the MCQSW boost converter can be used as the DC-DC boost stage to boost the low input sources, e.g., photovoltaic or fuel cells. The MCQSW converter merges the operation of the parallel boost stage and the cascaded switched capacitor stage to achieve higher efficiency and high power density, as shown in Fig. 2. It can ensure automatic voltage balancing and current sharing among the multicells, which are important for high voltage conversion ratio applications with high input current and output voltage.

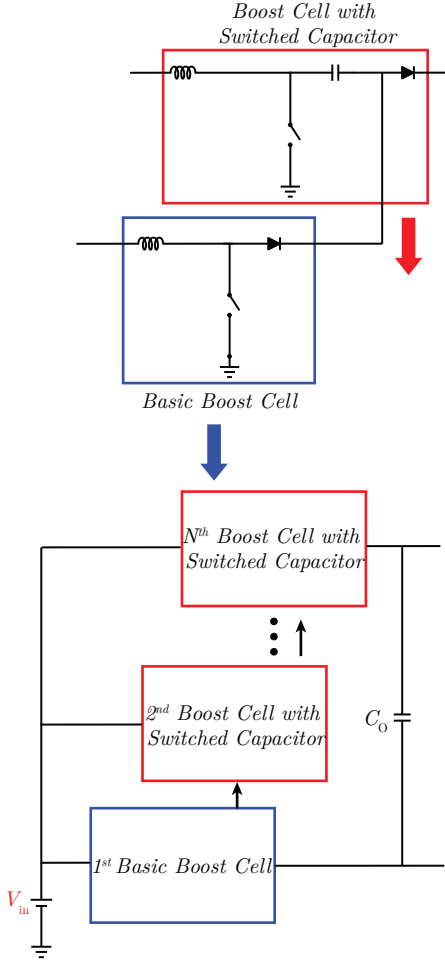The rest of this paper is organized as follows. Section II

Fig. 2. Schematic of N-cell MCQSW converter.

Fig. 3. Schematic of the three-cell MCQSW converter.

introduces the basic operation principle of the MCQSW boost converter. Section III presents the operation mechanisms of the MCQSW boost converter, including the interleaving currents, soft charging, current sharing, and voltage balancing mechanisms. The design guidelines for selecting components in an MCQSW converter and the variable on-time valley-detection analogy control circuitry are provided in Section IV. Section V presents the experimental results to verify the performance of the MCQSW topology with a 250 W, 15 V-180 V MCQSW prototype which can achieve a peak efficiency of 91%. Finally, Section VI concludes this paper.

II. PRINCIPLES OF THE MCQSW CONVERTER

Fig. 3 shows a schematic of the MCQSW boost converter with three boost cells. The MCQSW converter has a hybrid switched-capacitor voltage multiplying mechanism. Compared to a conventional QSW boost converter, a series capacitor is inserted into each cell to achieve automatic current sharing and voltage balancing between cells. The diodes of multiple cells are cascaded to achieve voltage multiplying. The three ground-referenced boost switches are operating in boundary continuous conduction mode (BCM) with ZVS-turn-on by resonating the drain-source capacitance of the switches. One switching cycle
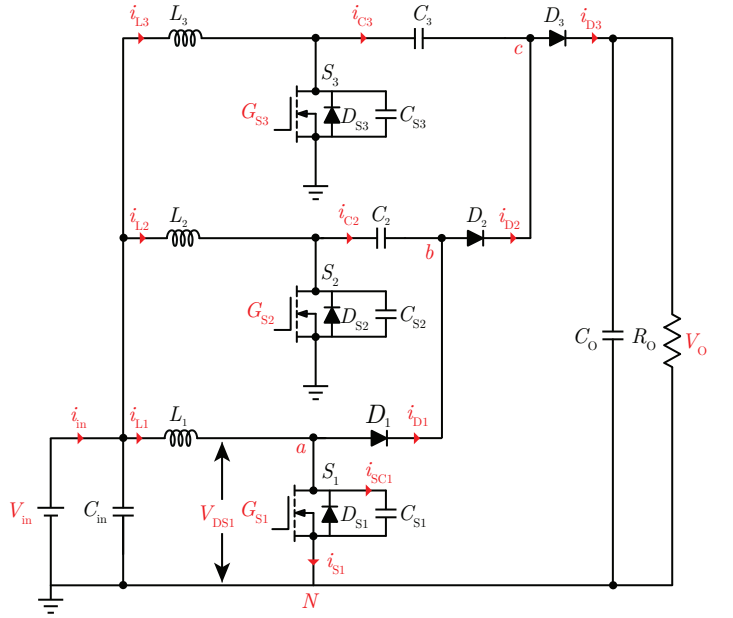
of the MCQSW boost converter includes five stages (Stage I to Stage V) and its key operation waveforms and equivalent circuits under five stages are illustrated in Fig. 4. Due to the similar operation principles between the boost QSW cells, only one cell is utilized to demonstrate the analysis.

Stage I (t_1-t_2)[Fig. 4a and Fig. 4f]: S_1 is turned-OFF and D_1 is ON. S_1 blocks the high voltage, and the inductor current of L_1 linearly decreases. The energy from inductor L_1 is released to the next boost cell by charging the series capacitor C_2.

Stage II (t_2-t_3)[Fig. 4b and Fig. 4f]: S_1 is still in OFF-state and D_1 is reverse-biased. The inductor current i_{L1} has reached zero and begins to increase in the opposite direction. Meanwhile, the parasitic capacitance of S_1 is discharging. When V_{DS1} reaches near zero voltage (V_{ZVS}), S_1 is turned ON with almost ZVS.

Stage III (t_3-t_4)[Fig. 4c and Fig. 4f]: S_1 is in the ON-state and D_1 is OFF. The inductor current linearly reduces to zero from negative.

Stage IV (t_4-t_5)[Fig. 4d and Fig. 4f]: S_1 is ON and D_1 is OFF. The inductor current linearly increases from zero to positive until it reaches a targeted peak value.

Stage V (t_5-t_6)[Fig. 4e and Fig. 4f]: S_1 is OFF and D_1 is OFF. The inductor current charges the parasitic capacitance of S_1 until the diode is turned ON.

The topology shown in Fig. 3 has three cascaded modular QSW boost cells. The three cells have identical duty ratio and operate in interleaving. The inputs of these boost cells are connected in parallel, and the outputs of these boost cells are cascaded as a series capacitor voltage multiplier [10], [11]. The voltage gain of a MCQSW converter with N cascaded cells is:

$$G = \frac{V_{out}}{V_{in}} = \frac{N}{1-D}. \tag{1}$$
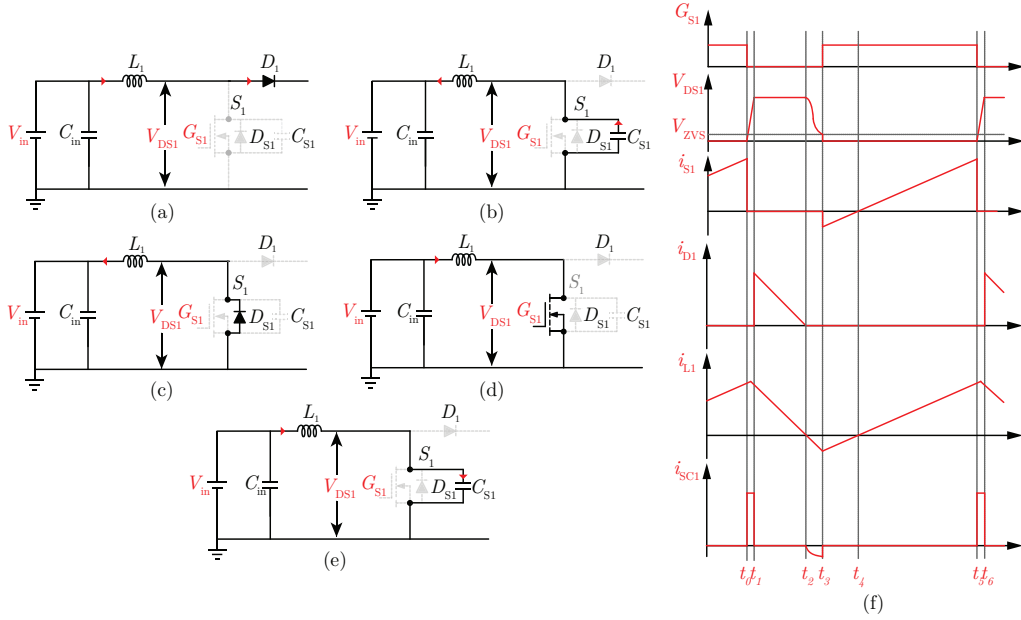
where D is the duty cycle.

Fig. 4. Equivalent circuit operation mechanisms under five different operation stages: (a) Stage I (t_1-t_2), (b) Stage II (t_2-t_3), (c) Stage III (t_3-t_4), (d) Stage IV (t_4-t_5), (e) Stage V (t_5-t_6), and (f) Key waveforms of the converter for the first QSW boost cell.

III. OPERATION MECHANISMS

A. Interleaving and Voltage Multiplying

The multiple cascaded QSW boost cells are operated in interleaving to minimize the input current ripple. Fig. 5 shows the principles of the interleaving operation for an MCQSW boost converter with 3 (N=3) cascaded cells. Since $D > \frac{N-1}{N}$, there is at most one switch OFF at any arbitrary time instance and other switches are ON. If the switch of the ith-cascaded cell is OFF, the output current of the ith-cascaded cell discharges the series-capacitor of the ith cascaded cell, and charges the series-capacitor of the $(i+1)^{th}$ cascaded cell. When the switch of the $(i+1)^{th}$-cascaded cell is OFF, the output current of the $(i+1)^{th}$-cascaded cell discharges the series-capacitor of the $(i+1)^{th}$-cascaded cell, and charges the series-capacitor of the $(i+2)^{th}$-cascaded cell. The MCQSW boost converter pumps the charge through N modular cascaded cells, one after the other in an interleaved sequence. The voltage is multiplied by N times in each switching cycle, allowing the voltage conversion ratio to be increased by a factor of N without increasing the power conversion stress of the switches and diodes.

B. Automatic Current Sharing and Voltage Balancing

The current balancing of the MCQSW converter is automatically guaranteed by the charge balancing mechanisms of the series capacitors, similar to the series-capacitor buck topology in [11], [20]. The current discharging the series capacitor needs to be equal to the current charging the series capacitor within one switching cycle. This forces the current balance between two neighboring cells, and yields the current balance of all cascaded cells, together with voltage balancing in the series capacitors. The current sharing and voltage balancing
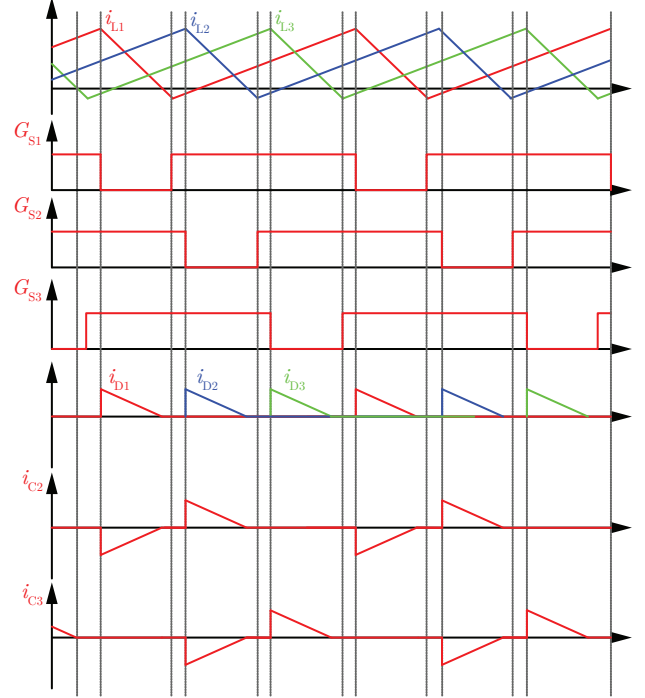

Fig. 5. Interleaved operation of the MCQSW boost converter with three input-parallel output-series cells. The interleaving operation reduces the input current ripple and input capacitor size.

mechanism enables the MCQSW converter to evenly manage the loss and heat when processing a large amount of power.

A large signal state space averaging analysis was performed to analyze the current sharing and voltage balancing mechanisms (Fig. 3). R represents the parasitic resistance of each cell

considering the conduction loss and switching loss. Assume all switches have the same duty cycle (e.g., D), the differential equations which determine the state variables (i_{L1}, i_{L2}, i_{L3}, v_{C2}, v_{C3}) in a MCQSW converter with three cells are:

$$L_1 \frac{di_{L1}}{dt} = \langle v_{L1} \rangle = DV_{C2} - i_{L1}R - V_{in}, \qquad (2)$$

$$L_2 \frac{di_{L2}}{dt} = \langle v_{L2} \rangle = -DV_{C2} + DV_{C3} - i_{L2}R - V_{in}, \qquad (3)$$

$$L_3 \frac{di_{L3}}{dt} = \langle v_{L3} \rangle = DV_o - DV_{C3} - i_{L3}R - V_{in}, \qquad (4)$$

$$C_2 \frac{dv_{C2}}{dt} = \langle i_{C2} \rangle = D\left(i_{L2} - i_{L1}\right), \qquad (5)$$

$$C_3 \frac{dv_{C3}}{dt} = \langle i_{C3} \rangle = D\left(i_{L3} - i_{L2}\right). \qquad (6)$$

Furthermore, for simplicity, assume all inductances (e.g., L_1, L_2, and L_3) and series capacitances (e.g., C_1 and C_2) are L and C. By subtracting (2) from (3) leads to

$$L \frac{d\left(i_{L2} - i_{L1}\right)}{dt} = -2DV_{C2} + DV_{C3} - R\left(i_{L2} - i_{L1}\right). \qquad (7)$$

Combining (7) with (5) and (6),

$$L \frac{d^2\left(i_{L2} - i_{L1}\right)}{dt^2} + \frac{R}{L}\frac{d\left(i_{L2} - i_{L1}\right)}{dt} + \frac{D^2}{LC}\left(i_{L2} - i_{L1}\right) = 0. \qquad (8)$$

Similarly, i_{L2} and i_{L3} are related by

$$L \frac{d^2\left(i_{L3} - i_{L2}\right)}{dt^2} + \frac{R}{L}\frac{d\left(i_{L3} - i_{L2}\right)}{dt} + \frac{D^2}{LC}\left(i_{L3} - i_{L2}\right) = 0. \qquad (9)$$

As a result, (8) and (9) are expressed in the form of a second-order damper harmonic oscillator, which describes the large-signal dynamics of the current sharing mechanism.

Referring to the standard form of second-order differential equations, the decay rate α is $\frac{R}{2L}$, the angular resonant frequency is $D\sqrt{\frac{1}{LC}}$, the damping ratio ξ is $\frac{R}{2D}\sqrt{\frac{C}{L}}$, and the quality factor Q is $\frac{D}{R}\sqrt{\frac{L}{C}}$. Therefore, similar to conventional second-order systems, the current differences between the inductors of the MCQSW converter can respond to perturbations, and finally reduces to zero in steady state.

The current sharing mechanism further ensure voltage balancing. Assuming the inductor currents are identical ($i_{L1} = i_{L2} = i_{L3} = i_L$) under the steady state and their derivatives are zero, and as a result, the capacitor voltages are

$$V_{C2} = \frac{1}{3}V_o \qquad (10)$$

$$V_{C3} = \frac{2}{3}V_o \qquad (11)$$

Furthermore, (5) and (6) can be used to demonstrate the transient dynamics of the capacitor voltages. Similar to the inductor current differences, the capacitor voltages gradually damp to the steady-state values, as presented in (10) and (11).

C. Soft Charging

Typical switched-capacitor-based voltage multipliers are usually hard-charged: capacitors are forced to be connected in parallel with frequency-dependent charge sharing losses. The MCQSW boost architecture allows complete soft-charging operation of the voltage multiplier capacitors [18]–[20]. Capacitors are never connected in parallel and the charge sharing losses are eliminated. The linear and extendable conversion ratio of the MCQSW boost converter comes without a significant increase in the switching loss, conduction loss, or charge sharing loss.

As illustrated in Fig. 5 and Fig. 6, the series capacitors are only charged and discharged by the boost inductors. More concretely, it can be seen in Fig. 6a that only when G_{S1} is OFF, the capacitor C_2 is discharged by the inductor L_1. After this, G_{S2} is turned OFF, and the capacitor C_2 is charged by the inductor L_2 and the capacitor C_3 is discharged by the inductor L_2. Finally, the capacitor C_3 is charged by L_3 when only G_{S3} is turned OFF. In this way, complete soft charging is achieved by all the series capacitors in the MCQSW converter.

IV. DESIGN CONSIDERATIONS

A. Design of Variable ON-time Control

The bandwidth of a typical microcontroller is not capable of performing ZVS for the QSW boost converter in the sub-MHz range, especially when the power level is low. Fig. 7 shows an analogy circuit which can enable robust ZVS for the QSW boost cell [8], [9]. This circuit comprises two comparators, one integrator, three voltage dividers, and three logic gates. The ZVS valley detection circuit utilizes the drain-source voltage V_{DS1}, ZVS threshold voltage V_{ZVS}, and two reference voltages V_1, V_2 to determine the switching action. The comparator IC_1 is used to determine the ON-time duration and switch turn OFF. From the beginning of t_4 in Fig. 4f, low V_{DS1} leads to a low IC_2 output. Thus, the transistor IC_3 is OFF and V_1 starts to charge C_{C1}. After a certain period, the output of IC_1 becomes high and the switch S_1 turns OFF. According to the capacitor charging principle, the capacitor voltage mimics the inductor current which linearly ramps up during the ON period:

$$V_2 \cdot \frac{R_4}{R_3 + R_4} = V_1 \left(1 - e^{-\frac{t}{R_{C1}C_{C1}}}\cdot\right) \qquad (12)$$

Thus, the charging time t can be modulated by adjusting the variable resistance R_{C1}.

The turn on of the switch G_{S1} (at t_3) is controlled by the comparator IC_2. When the switch turns OFF at t_0, V_{DS1} being larger than V_{ZVS} leads to IC_3 turn-ON. Meanwhile, the discharged voltage on C_{C1} makes the output of IC_1 low. Once the current becomes negative (at t_2), the diode is OFF, and the inductor current discharges the parasitic capacitance of the switch, reducing the voltage at the switch node. When the resistor-divided V_{DS1} becomes smaller than V_{ZVS}, the low output of IC_2 triggers the ZVS turn-ON action.
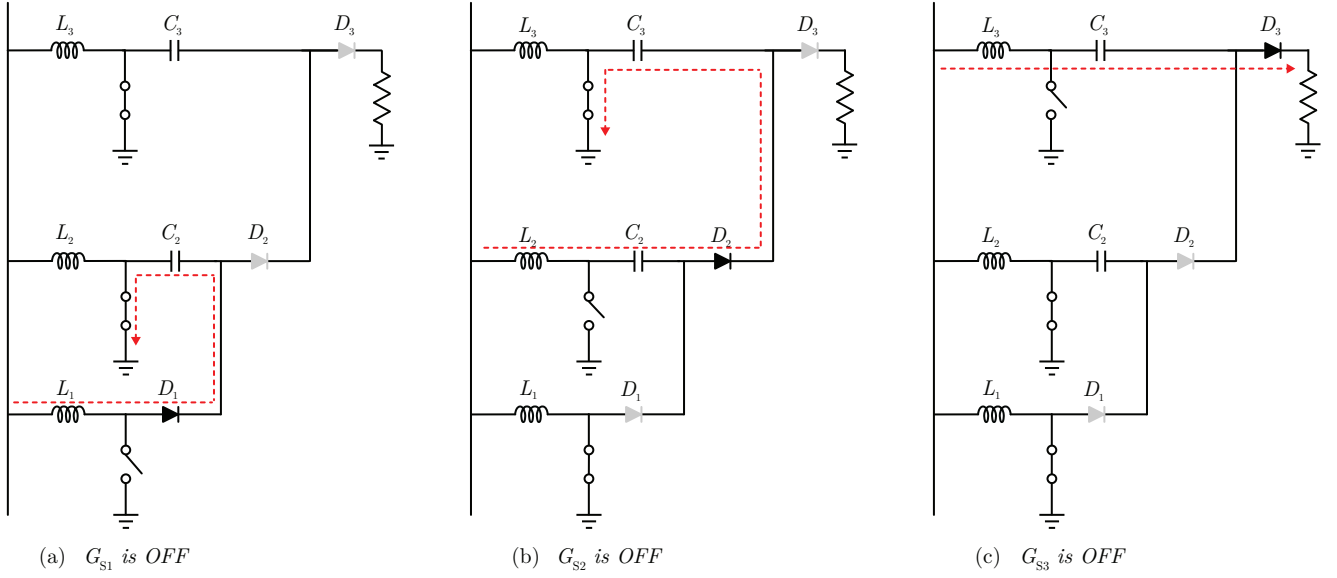
Fig. 6. Soft charging mechanism of the MCQSW converter.
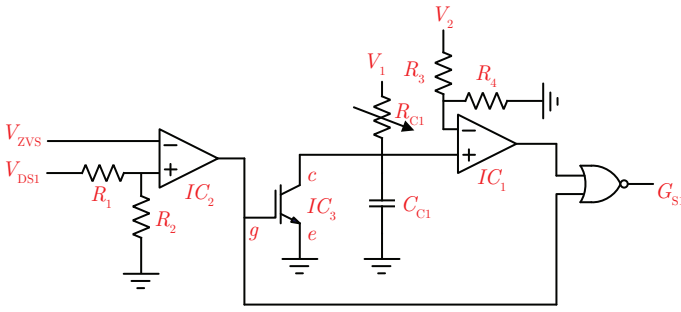

Fig. 7. Schematic of the high-frequency ZVS valley detection and ON-time control circuit.

B. Boost Inductor and Series Capacitor Design

As discussed in variable on-time control, the charging time t of the capacitor C_{C1} is also the conduction time of the switches. Therefore, the boost inductor can be expressed as

$$L = \frac{V_{\text{in}}}{\frac{I_{in}}{3} + \Delta i_L} \cdot t \quad (13)$$

where I_{in} is the input current and Δi_L is the predefined ripple current. Moreover, the series capacitor can be selected according to the voltage ripple requirement. The capacitor current I_c is

$$I_c = C\frac{dv_C}{dt} = C\frac{\Delta v_c f}{D} \quad (14)$$

in which f is the switching frequency. Then, the series capacitor can be expressed as

$$C = \frac{DI_c}{\Delta v_c f} = \frac{DI_{in}/3}{k_c V_c f} \quad (15)$$

where k_c is the ripple percentage. The capacitor voltage V_c can be obtained based on (10) and (11).

C. Example MCQSW Converter Design

A 15 V-180 V, 250 W three-level MCQSW converter was designed and tested in this paper. The voltage conversion ratio of this converter is 1:12 with 75% duty ratio, as illustrated in Fig. 3. The switching frequency is selected as 70 kHz under the rated power (i.e., 250 W), and will increase to 5 MHz at light load. To ensure boundary DCM operation, the inductors are chosen as 1 μH according to (13). Note that according to the previous analysis, the drain-source voltages across the switches are the same and equal to $\frac{V_{\text{in}}}{1-D}$. Therefore, three 100 V GS61004B Gallium Nitride (GaN) devices from GaN Systems were used as the boost switches. Fig. 8 illustrates the relationship between the switching frequency and the output power. The ON time of the switches is controlled to set the peak inductor current, and the offtime of the switches is free-wheeling. At light load, the converter operates at high frequencies up to 5 MHz.

As shown in Fig. 7, the drain-source voltage V_{DS1} is sensed by the comparator IC_2 through a voltage divider. It is worth noting that the parasitic capacitance C_P can impose a negative effect on the output voltage through the voltage divider, especially when the converter operates at high-frequencies. To mitigate the parasitic effect, a capacitor C_{R2} is added in parallel with R_2, as shown in Fig. 9 to create a capacitive voltage divider which carries the high frequency voltage information. As can be seen in Fig. 10, by choosing an appropriate capacitance for C_{R2}, the output voltage through the voltage divider can maintain a constant value without phase delay across a wide switching frequency range. Table I listed the key parameters of the prototype and the equivalent capacitance considering capacitance degradation.

Fig. 11 shows a loss analysis for the MCQSW converter. The power losses are mainly classified into switch conduction losses, switching losses, diode conduction losses and inductor
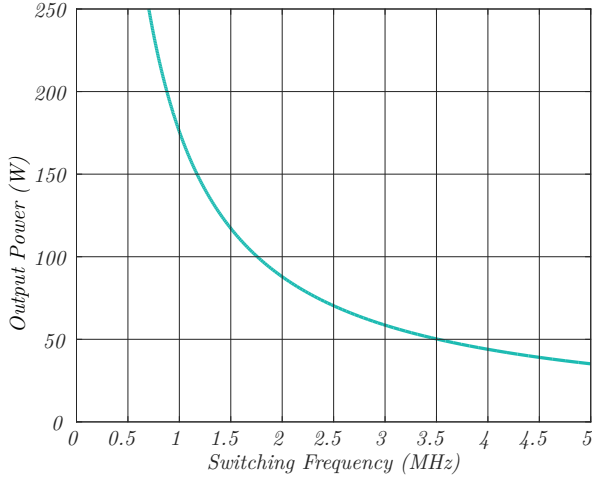
Fig. 8. Output power as a function of the switching frequency with constant ON-time control.
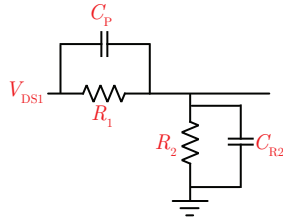

Fig. 9. Schematic of the high frequency voltage divider for valley-detection.
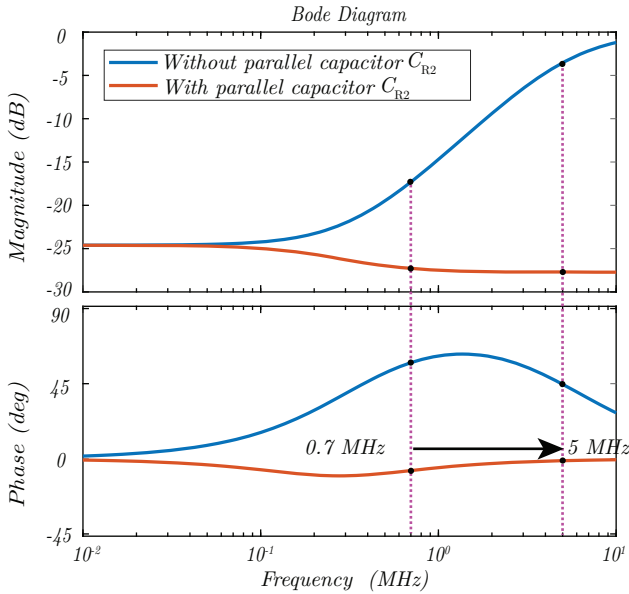

Fig. 10. Frequency response of the high frequency voltage divider combining a resistive divider and a capacitive divider.

TABLE I
BILL-OF-MATERIAL OF THE 15 V-180 V, 250 W MCQSW PROTOTYPE.

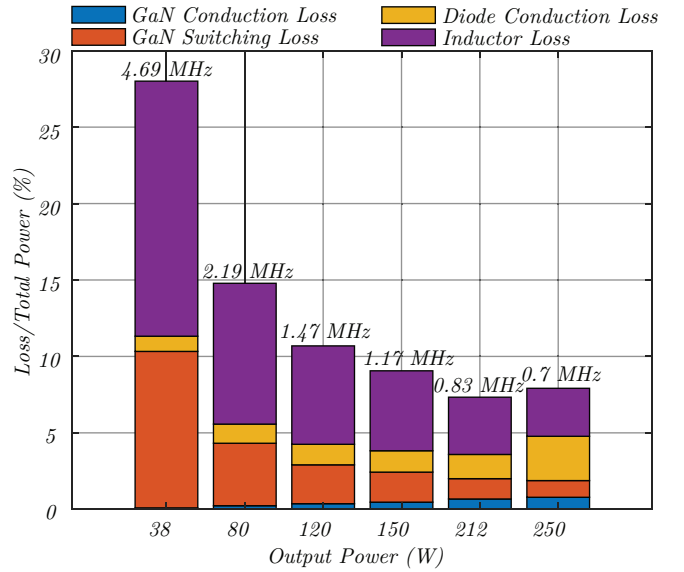| Input voltage V_{in}	15 V
Output voltage V_o	180 V
Rated power P_o	250 W
Switching Frequency	700 kHz to 5 MHz
S_1, S_2, S_3	GS61004B, 100 V/38 A/16 mΩ
Diodes D_1, D_2, D_3	VS-16CDH02-M3, 200 V/16 A
Inductors L_1, L_2, L_3	HC11R0R, 1.12 μH
C_2	2.2 $\mu F \times 6$, C_{eq}=10.2 μF, 250 V X7T, TDK
C_3	2.2 $\mu F \times 10$, C_{eq}=11.7 μF, 250 V X7T, TDK
C_o	2.2 $\mu F \times 12$, C_{eq}=10.38 μF, 250 V X7T, TDK
C_{in}	10 $\mu F \times 10$, 50 V, X5R, Murata

Fig. 11. Power loss analysis of the prototype MCQSW converter.

switches also have higher switching losses due to the higher switching frequency. As the output power increases from light load to full load, the switch and diode conduction loss, and the inductor loss begin to dominate the total power loss. The core loss contributes to most of the inductor loss. However, the switching loss significantly decreases due to the lower switching frequency.

V. EXPERIMENTAL RESULTS

Fig. 12 shows the MCQSW converter prototype with three cascaded QSW boost cells. The PCB layout of the prototype is shown in Fig. 13. The duty ratio is selected as 75% and therefore, the voltage conversion ratio is 1:12 according to (1). The input voltage is 15 V, the output voltage is 180 V, and the power rating is 250 W. 100 V GaN MOSFETs (GS61004B) are used as the boost switch considering the maximum drain-source voltage of each switch is only 60 V.
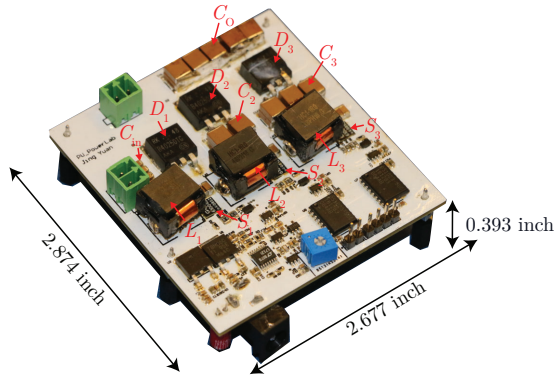
losses. A majority of the power loss at light load is mainly attributed to the inductor losses and switching losses. The higher switching frequency at light load pushes the inductor to generate more ac winding losses. At the same time, the boost

Fig. 12. Prototype of the MCQSW converter.
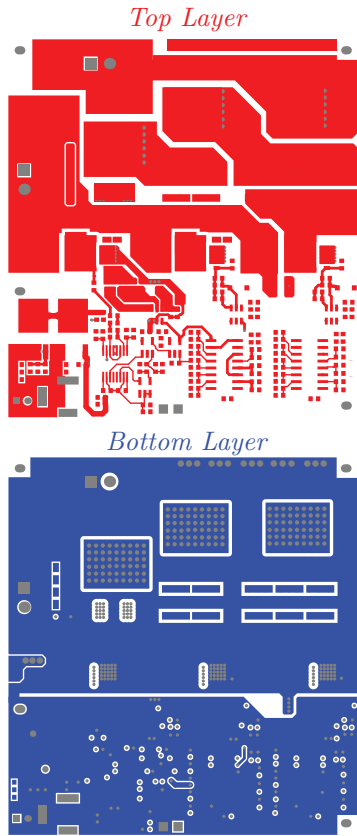
Fig. 13. PCB layout of the 15 V-180 V/250 W MCQSW converter.

Fig. 14. Measured waveforms of the MCQSW converter operating at 150 W: inductor currents i_{L1}, i_{L2}, and i_{L3} [5 A/div], switching signal G_{S1} [5 V/div], switch voltage V_{DS1} [50 V/div], time [400 ns/div].

Fig. 15. ZVS operation for the switch S_1.

Fig. 16. Measured waveforms of the MCQSW converter operating at 150 W: voltages V_{aN}, V_{bN} and V_{cN} [50 V/div], time [1000 ns/div].

The high-frequency gating signal G_{S1} is synthesized by a ZVS valley detection circuit designed for the first phase. The other two gate signals (G_{S2} and G_{S3}) are created by adopting a digital delay integrated circuit (DS1023-500+) with programmable propagation delay. The three cascaded cells are interleaved with 120°phase-shift among each other, as proven in Fig. 14. Interleaving reduces the input capacitor size. As designed, the boost converters operated in BCM and achieved ZVS. It can be observed in Fig. 15 that the drain-source voltage begins to decrease when the inductor current flows in the opposite direction; when the drain-source voltage drops to
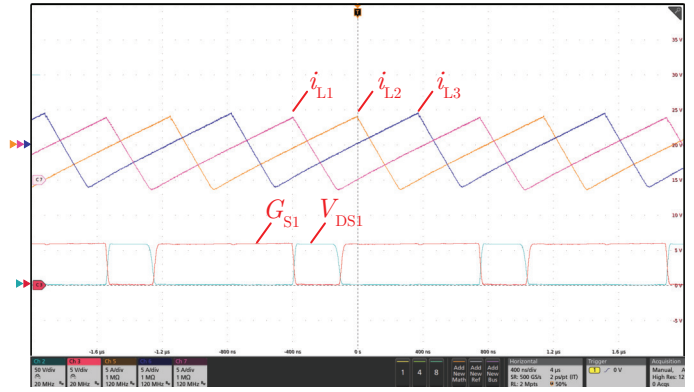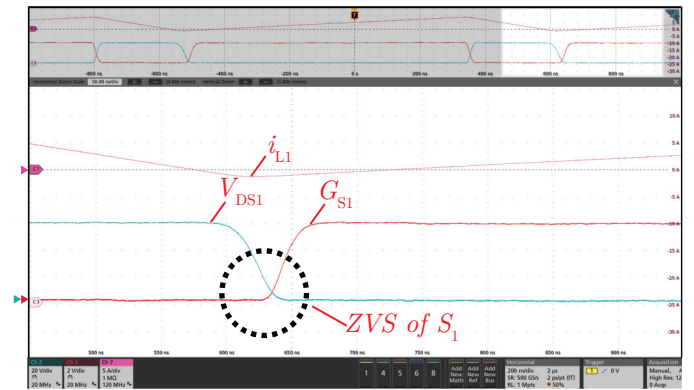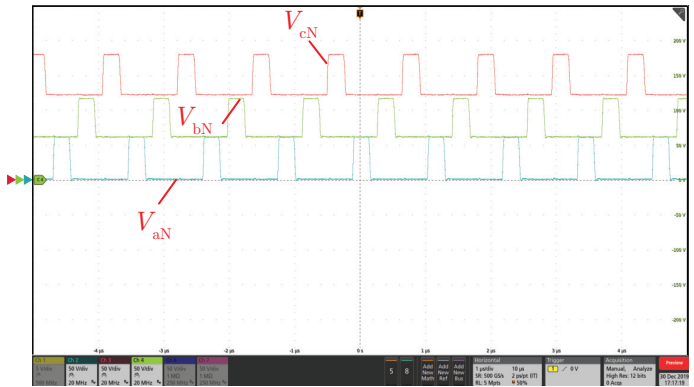
nearly zero, the switch S_1 turns ON and ZVS is achieved for the switches.

Fig. 16 shows the output voltage of the three switch nodes V_{aN}, V_{bN} and V_{cN}. The peaks of V_{aN}, V_{bN} and V_{cN} are about 60 V, 120 V and 180 V, respectively, indicating voltage balancing among the boost cells. Each QSW boost cell offers a voltage gain of 1:4, and the overall voltage conversion ratio of the three-cell-cascaded system is 1:12, as expected.
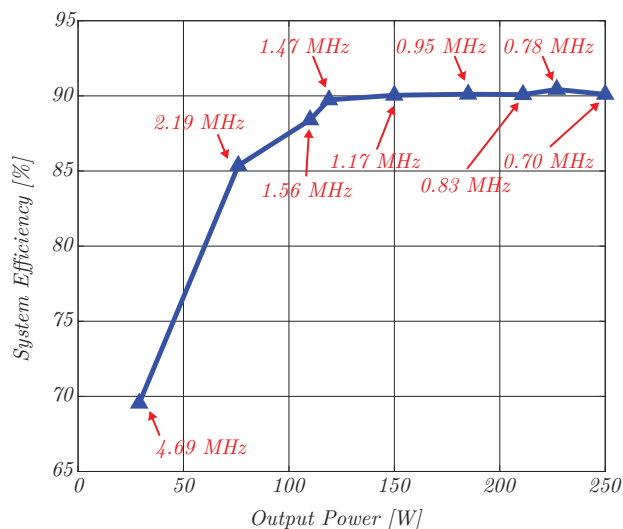
Fig. 17. System measured efficiency of the prototype.

The MCQSW converter regulates the output power by modulating the ON-time of the switches - the converter delivers more power with a longer ON-time period. The OFF time of the switch is jointly determined by the input and output voltages. As a result, the MCQSW converter requires variable ON-time variable frequency control. The switching frequency of the prototype was designed to change between 700 kHz to 4.69 MHz, leading to a power range of 38 W to 250 W. The converter delivers 38 W at 4.69 MHz, and delivers 250 W at 700 kHz. As shown in Fig. 17, the system efficiency of the 15 V-to-180 V 250 W DC-DC converter is measured across a range of different switching frequencies. The maximum power is 250 W. The maximum efficiency of the system is over 90% across a wide range. The light load efficiency of the converter is around 70%. Notably, the burst-mode control can be adopted to improve the converter efficiency at light load.

VI. CONCLUSION

This paper presents a multicell cascaded quasi-square-wave (MCQSW) boost converter for non-isolated high conversion ratio applications. The MCQSW features low input current ripple benefiting from the interleaved structure, low switching losses because of the soft-switched operation, and high boosting capability by the cascaded boost cells. The MCQSW converter offers natural current sharing and automatic voltage balancing among many cells, which is critical for multicell architectures. To ensure the ground-referenced switches operating in boundary continuous conduction mode with ZVS turn-ON, A ZVS analogy control circuitry was adopted. A 250 W MCQSW prototype, which can operate with a frequency of 0.7 to 5 MHz and a conversion ratio of 12 (15 V-to-180 V), was built and tested to validate the key advantages.

ACKNOWLEDGMENT

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