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Mechanistic Power Module Degradation Modelling Concept with Feedback

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Abstract

A platform will be presented based on physics-of-failure-based models. The platform gives an overview of the couplings between simulation, health monitoring and online lifetime prediction of a power module. The platform is modular and is not tied to any specific software product to make it as generally applicable as possible.

Introduction

Reliability and lifetime engineering have been relevant fields of study since their conception. After the invention of power electronics, the analyses and findings from the reliability analysis of other fields were applied to power electronics as well. As conventional energy sources are replaced with renewable sources of energy the demand for reliable power electronics increases[1].

One of the most widely used power electronics devices is the IGBT(Insulated Gate Bipolar Transistor), combining the power capability of the bipolar transistor and the fast switching of MOS(Metal-Oxide-Semiconductor) devices.

IGBTs are mature devices, and as a result of many years of improvements and study, the fatigue relevant failure mechanisms have been reduced to consisting mainly of package related failures[2]. The main degrading sections of the IGBT geometry are the solder layer attaching the semiconductor chip and the bond-wires functioning as interconnects from the top surface of the semiconductor chip.

This paper will describe the characteristic behaviour of IGBT and packaging degradation and reliability modelling. This will be presented in a large flow chart connecting cause and effect. The proposed mechanistic model is meant to serve as an overview and inspiration for power module reliability analysis.

The content of the mechanistic model will be described in this manuscript. Special focus will be placed on the empirical damage models.

The general procedure used to characterise empirical models will be described along with introductions to the relevant life testing methods for power electronics.

Finally, the mechanistic relationships will be validated by comparing the predicted wear out Vce evolution with experimental results.

Degradation Models

In manuscript [3] a range of damage models for IGBT fatigue are reviewed. One of the conclusions drawn in this paper is that cycle based damage models are limited, and time-dependent damage modelling is needed. The authors however fail to provide a complete damage modelling approach, even in subsequent papers[4].

Traditionally, empirically fitted damage equations have been used for damage modelling of a broad range of devices and constructions, physics-based simple damage models quite simply do not exist yet. Alternatively, an effort-costly approach to damage modelling can be found in the microstructural mechanical approach used for the solder layer of an IGBT in [5]. This approach was found to be able to accurately model both the crack initiation and crack propagation of the solder joint.

The traditional damage approach is used in [6], however, this approach adds a thermal model degradation feedback loop to emulate the effects of damage accumulation on the thermal characteristics of the device. The cumulative degradation of the device will in some cases greatly influence the device behaviour during device life and may have a large effect on life predictability using parameter monitoring.

The practical implementation of the traditional empirical approach to reliability modelling can be seen executed thoroughly in [7]. The authors analyse an entire DC micro-grid system with PV generation, battery storage, fuel cell and a load profile based on both a clinic and an apartment case. The final result of the paper is a reliability assessment of the entire system.

In [2] the degradation of an IGBT module is modelled through a successive series of models and physics simulations. One simulation is based on the results of the previous, and previous simulations are updated if the model requires it.

[8] offers a review of the state of the art for lifetime prediction of power electronics devices. The review reports a large number of empirical damage models and discusses degradation monitoring and power cycling methodology.

Paris Law

The Paris Law is similar in form and origin to the Coffin-Manson and Basquin equations. Instead of number of cycles to failure it predicts the crack increase per cycle. It is an empirical equation and as such requires fitting to experimental lifetime tests. The stressor input to this equation is the stress intensity factor which is a geometry weighting method for the mechanical stress.

$$\frac{da}{dN} = C(\Delta K)^p \tag{1}$$

Where a is the crack length, N is the cycle, ΔK is the stress intensity factor range and C and p are fitting parameters. It is important to note that the Paris Law only models crack propagation and not crack formulation/initiation/nucleation.

Life and degradation link

A non-linear degradation functional can be used to link the damage from one of the damage models with the degradation effects [9].

$$1 - D = \left(1 - \frac{N}{N_f}\right)^k \tag{2}$$

Table I: Table of Damage Models

Name	Equation	Stress Term(s)	Ref(s)
Coffin-Manson	$N_f = A(\Delta\varepsilon_{pl})^B$	$\Delta\varepsilon_{pl}$	[10]
Basquin	$N_f = a(\Delta\sigma_e)^{-b}$	$\Delta\sigma_e$	[11]
Modified Coffin-Manson	$N_f = A\Delta T_j^{-\alpha} exp\left(\frac{E_a}{k_B T_{jm}}\right)$	$\Delta T_j, E_a, T_{jm}$	[12]
Bayerer	$N_f = K(\Delta T_j)^{\beta_1} e^{\left(\frac{\beta_2}{T_j+273}\right)} t_{on}^{\beta_3} I^{\beta_4} V^{\beta_5} D^{\beta_6}$	$\Delta T_j, T_j, t_{on}, I, V, D$	[13]

Where D is a representation of degradation (from 0-1), N is the current number of cycles, N$_f$ is the number of cycles to failure and k is the exponential fitting parameter.

Proposed Mechanistic Model

In the time between module assembly and first bond-wire liftoff, the bond wires on a single chip can be modelled as having identical behaviour.

This manuscript details a new power module wear-out and degradation mechanism platform. The methodology is conceptualised for a single semiconductor chip with both wire bond and die attach layers for which the degradation is modelled. The module considered in this manuscript is a Si IGBT module so it is assumed that no degradation of the semiconductor chip itself takes place.

The mechanistic model presented in this section is based on the model in fig. 1. The thermal networks is based on the thermal model from [14].

Superimposed on the material and structural representation are two networks, a blue, and a black. The blue network is the basic electric network of the micro-device, including the forward voltage of the semiconductor and bond-wire and bond-wire interface resistances.

The black network is the basic thermal network of the micro-device. Including the main thermal resistances and a simplified heat modelling approach using two heat sources, one for the chip representing the chip power loss and one for the bond-wire.

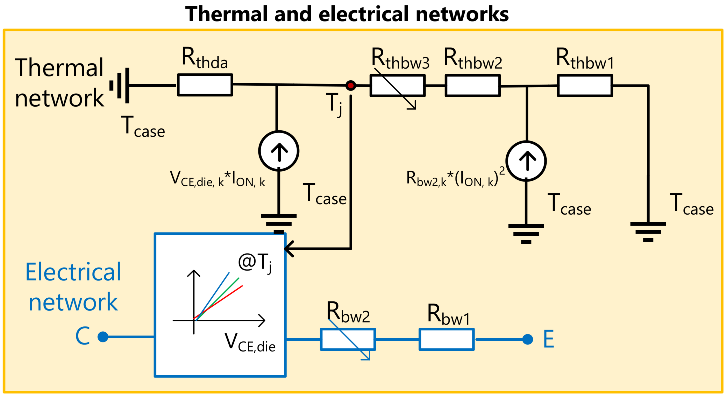


Fig. 1: Basic semiconductor thermal and electrical modelling.

Damage Functions

The damage function blocks contain the damage models needed for wire bond and die attach metallization damage calculations. The modelling platform can be updated with new damage models as long as they are capable of estimating a damage quantity which can be related to the crack propagation in the two metallization layers. A damage model can be chosen from Table I or elsewhere.

The platform itself can be implemented in both the continuous time and discrete time-domains. These functions are the green boxes in fig. 3.

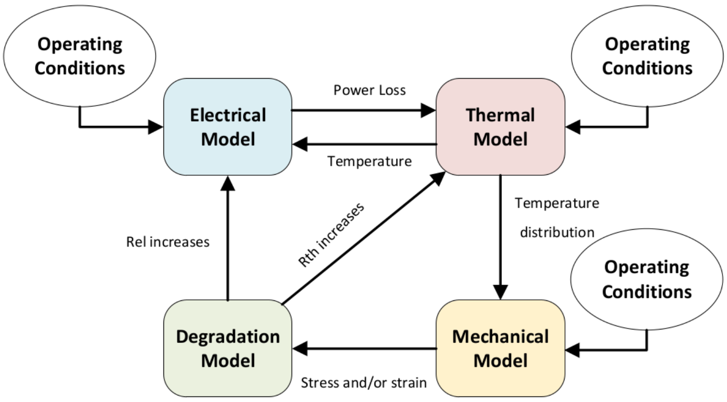


Fig. 2: Modelling Concept Flow.

Effect Functions

The effects of the degradation on the thermo-electrical model of the system are clear with the definitions of the characteristic values. These functions are the red boxes in fig. 3.

The electrical resistances change based on temperature and degradation:

$$R_{el}(T,a) = R_{0el} f(a) f(T) \tag{3}$$

Where T is temperature, a is crack length, R_{0el} is initial resistance, R_{el} is electrical resistance and f() are general formulations expressing the existence of functions describing crack and temperature dependence of the resistance.

The thermal resistance change based on degradation.

$$R_{th}(a) = R_{0th} f(a) \tag{4}$$

Where T is temperature, a is crack length, R_{0th} is initial resistance, R_{th} is thermal resistance and f() are general formulations expressing the existence of functions describing crack and temperature dependence of the resistance.

Thermal Model

The platform contains basic thermal and electrical models of the power module. The implemented thermal model contains the loop from DBC through wire bond, semiconductor die and die attach back to DBC and ambient temperature. This network is black and yellow box in fig. 3.

The split wire bond and die thermal resistances are constant, with the wire bond metallization and die attach thermal resistances being affected by the damage as described in equation 4.

Electrical Model

The electrical model included has a similar scope of the thermal model. It includes the wire bond resistance, the wire bond metallization resistance, the electrical behaviour of the semiconductor die and the die attach metallization resistance. All of the electrical resistances are affected by the local temperatures, and the *Rme* resistances are affected by the damage as described in equation 3.

Model Predicted Wear-Out Comparison

The wear-out predicted by this model is compared with the degradation reported by [15] to validate the mechanistic relationship of fig. 3.

The Vce measurement is comprised of a number of components, the main categories of which are the voltage drop across the semiconductor die and the resistive voltage drop across the interconnect path

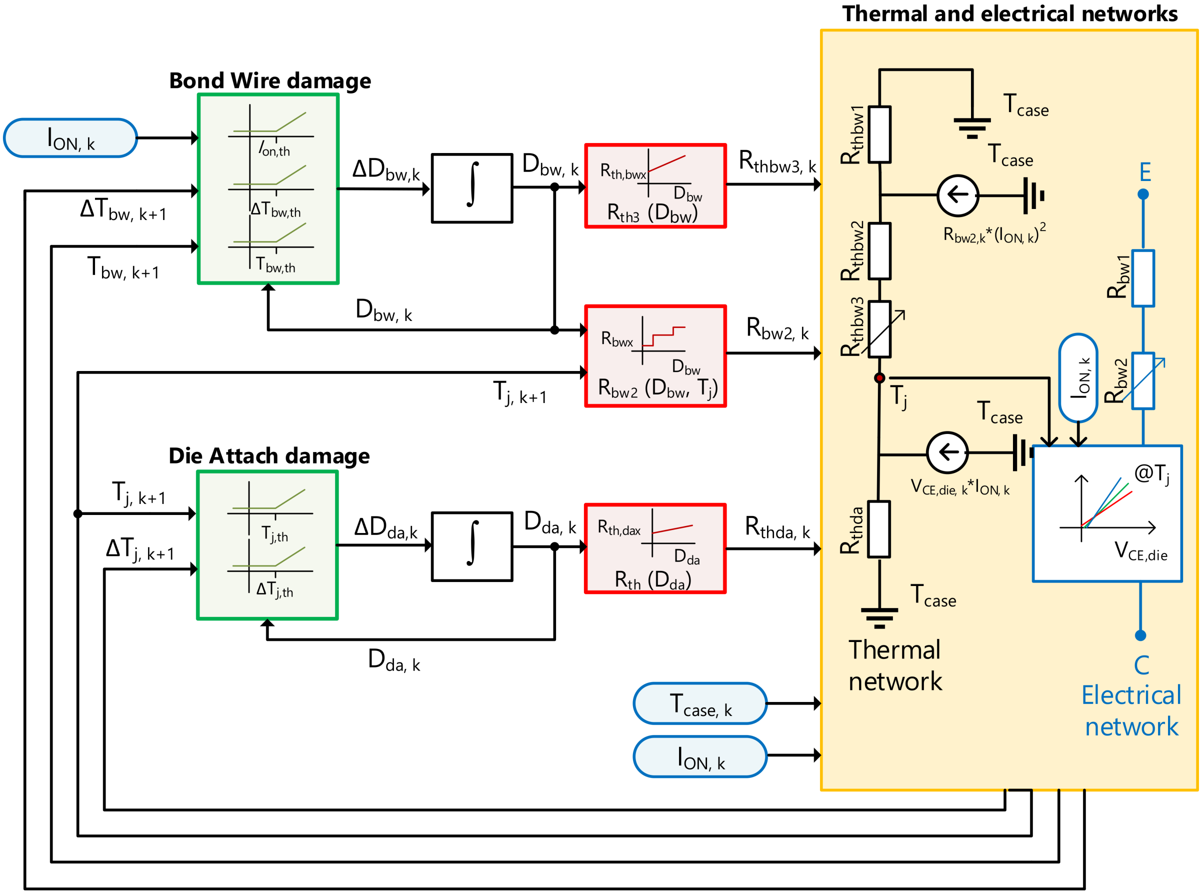
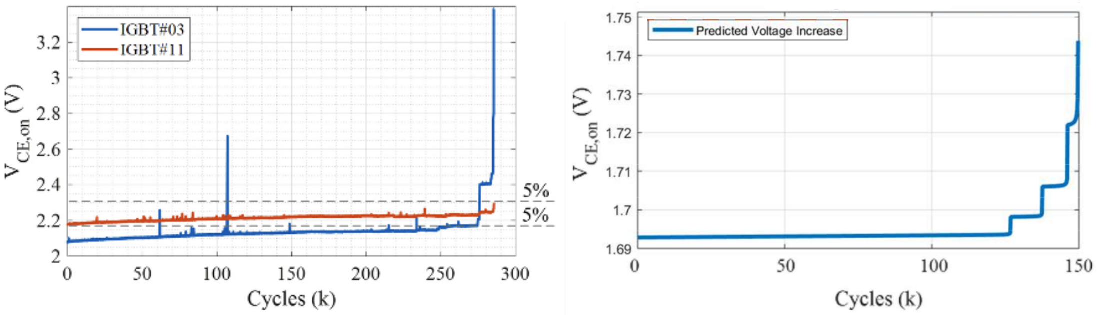


Fig. 3: Original model detailing the damage model.



(a) Case I

(b) Case II

Fig. 4: a) Experimental wear out curve from [15]. b) Predicted wear out curve.

contained in the voltage measurement. Generally, interconnect degradation is seen in bond-wires, chip top metallization, and solder layer. Of these, the solder layer degradation has the smallest electrical effect. The resistance of the degrading bond-wires is estimated using crack propagation modelling using FEM.

A comparison of figs. 4a and 4b shows that the model is able to predict the main degradation effects experienced by the device from [15]. As the Paris Law coefficients were not fitted to the degraded device from [15] the crack propagation rate should not be considered for the comparison instead the internal timing and behaviour should be. This example implementation was done in MATLAB.

Conclusion

This manuscript presented a mechanistic damage and effect model for power electronics module reliability analysis. The model details the cause and effect of each phenomenon. General discussion is made concerning the trends of the subcomponents.

The mechanistic model is multi-physical, as it contains electrical, thermal and structural damage modelling of a power semiconductor chip. The model is formulated and presented as the basis on which reliability analysis and modelling can be conducted. The model can and should be adapted and improved according to the focus of the use case.

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