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Cost-Effective DC Current Suppression for Single-Phase Grid-Connected PV Inverter

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***Abstract*—Due to the disparity of power modules, asymmetry of driving pulses and measurement errors of sensors, dc currents may be injected to grid-connected photovoltaic (PV) inverters. The dc current injection may cause magnetic saturation of the power transformers. To solve this issue, this paper thus proposes an effective current control strategy and compensation method, which does not require any extra sensor and hardware circuit. Firstly, the root-cause of dc current injection is comprehensively analyzed. Subsequently, a proportional-integral-resonant (PIR) controller is proposed to eliminate the dc component caused by disparity of power modules, asymmetry of driving pulses and measurement errors of grid voltage. The injected dc current caused by grid current measurement error is estimated from the line-frequency ripple of the dc-link voltage and then it is suppressed by a feedback compensation controller. In addition, the dc current rejection capability is evaluated and the proposed method is benchmarked with the virtual capacitor-based method. Finally, experimental tests are performed on a 1.2-kW single-phase PV inverter to verify the effectiveness of the proposal.**

***Index Terms*—Photovoltaic (PV) systems, grid-connected inverter, dc current injection, transformer saturation, PIR current controller.**

I. Introduction

Due to the merits of high efficiency, low cost and small size, transformerless grid-connected inverters have become more and more attractive in photovoltaic (PV) systems [1], [2]. Despite the gained advantages from the transformerless structure, it may lead to several technical and safety issues, e.g., galvanic non-isolation, ground fault current, leakage current, dc current injection and voltage-level mismatch between the solar panel and grid [3], [4]. As one of the major issues, the dc current injection may result in saturation of the distribution transformers, increase system losses, cause fast corrosion of the grounding wires and degrade power quality [5]. Consequently, several standards have been established to limit the dc current injection from PV inverter into the grid [6]-[8].

To suppress or mitigate dc current injection, many attempts have been made. They are broadly grouped into two categories: a) passive methods and b) active hardware or software techniques. The main idea of passive methods is to introduce a capacitor in the injected current path, which makes the system inherently free of dc current injection. For instance, in [9], a dc capacitor instead of an ac capacitor was serially connected between the inverter and the grid to block the dc component, where a method to prevent the capacitor from reverse polarity connection was used. However, it requires an expensive and bulky capacitor that has a low reactance at the line-frequency to effectively block the dc currents. An alternative is to use a two or three-level half-bridge inverter which utilizes the dc-link capacitor to block the dc currents [10], [11]. However, the low utilization rate of the dc-link voltage and large volume of capacitor hinder its wide application.

Regarding active methods, the auto-calibrating dc-link current sensing technique is effective to compensate for the dc component caused by the dc offset of the current measurement [12]. However, this method is not suitable for the case if the dc current is induced by other sources like the grid voltage measurement error and asymmetry of driving pulses [13]. Furthermore, to enhance the mitigation of dc current injection, many dc component measurement schemes combined with control methods have been proposed in the literature. In [14] and [15], a small 1:1 voltage transformer and an RC circuit were used to detect the dc voltage at the inverter output of an H-bridge inverter, and then the dc offset was fed back to a compensation loop. However, it is difficult to extract the dc voltage component when the inverter system operates with non-unity power factor. In addition, the impact caused by grid side bias cannot be eliminated either. Ref [16] introduced a two-stage RC filter to detect the dc component by measuring the dc voltage on the filter inductor. However, the detected result may be disturbed by noise, as the dc offset of the grid current and the series equivalent resistance of the filter inductor is small. Ref [17] and [18] develop nonlinear reactors to detect the dc voltage component at the converter output. Despite its precise dc bias measurement, the reactors should be specifically designed, which increases the system complexity. Similarly, to detect the dc component at the inverter output, the authors in [6] and [19] utilized a voltage sensor combined with a differential amplifier and a low pass filter for single-phase and three-phase systems. However, the step-down offset voltage from the differential amplifier introduces accurate measurement challenges [20]. To directly measure the grid current dc component, a coupled -inductor-based technique was presented

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in [21], where the dc current was obtained by using a coupled-inductor and a small-range high accuracy Hall current sensor. Although this technique is effective, the use of an extra high accuracy Hall current sensor increases the overall cost.

Different from the aforementioned active hardware dc suppression schemes, the active software techniques that utilize the existing measurement signals to obtain the dc component and then feed it back to a controller are more cost-effective. Ref [22] introduced an enhanced current control scheme to eliminate the dc offset current caused by voltage measurement error. However, this current control method is not suitable for the dc component caused by other sources. In [13], [23] and [24], a virtual capacitor scheme was proposed for single and three-phase PV inverters. It replaces the physical capacitor by integrating the grid current to block the dc component in ac side. To increase the accuracy of dc component extraction, a sliding window double iteration method was proposed in [25]. After the dc component is obtained, a neural network based proportional-integral-differential (PID) controller is used in the compensation loop to eliminate the dc component. Moreover, in [20], a method to suppress dc injection was proposed, where the dc component was extracted from the dc-link current and then mitigated via a control loop. To reduce the requirement of the current sensor, the dc-link current was reconstructed by the grid current. Although the solutions in [13], [20], [23]-[25] directly extract or suppress the dc component from the grid current and do not need extra sensors, the dc component caused by the nonlinearity and offset drifts in current transducers and sampling circuits cannot be eliminated. The reasons are as follows: 1) Hall-effect sensors are usually adopted to measure the grid current. However, due to the remanence, a dc bias will be introduced into the control system [26]; 2) According to the control theory, the dc bias caused by current sensors and sampling circuits is in the controller feedback channel, and thus, it is difficult to eliminate it only using the current feedback control. To solve this issue, a compensation scheme for current and voltage measurement errors in three and single-phase grid-connected inverters was proposed in [27] and [28], where the dc-link voltage ripple combined with a low-pass filter or mean average filter was used to suppress the dc component. More specifically, in [27], the dc offset and scaling error in grid current measurement were estimated by extracting the line-frequency and double-line-frequency voltage ripples in three-phase systems. Thus, the dc offset and scaling error in current measurement can be corrected in real time, but the estimation is quite challenging, as the two variables are very small in practice. Moreover, this method cannot be applied to single-phase system due to its inherent double-line-frequency ripple in the dc-link voltage. In [28], a dc current injection compensation scheme was proposed for a current transformer (CT) sensed static synchronous compensator (STATCOM), where the impact of CT on system and the effectiveness of the proposed dc current injection elimination method have been analyzed. Despite its capability of dc current injection suppressing, the presented method still has two limitations. First, the impact of disparity of power modules and asymmetry of driving pulses on grid current offset has not been considered. Second, the root and impact of dc current injection on the inverter system have not been fully investigated and analyzed.

In light of the above, for single-phase transformerless grid-connected PV inverters, this paper proposes a simple and effective scheme to mitigate the dc current caused by all sources without any extra sensor and hardware circuit. First, the root-causes of dc current injection and its impact on the inverter performance are thoroughly analyzed. The analysis reveals that the dc current caused by the disparity of power modules, asymmetry of driving pulses and grid voltage measurement errors can be mitigated by increasing the low-frequency gain of the current loop, while it does not work for the dc component induced by the current measurement errors. In addition, it has been further revealed that the dc current injected into the grid will result in line-frequency ripples on the dc-link voltage. Accordingly, a simple but effective proportional integral resonant (PIR) method and dc current compensation scheme are proposed. The PIR control can increase the low frequency gain, while the injected dc current due to the grid current measurement errors is estimated using the line-frequency ripple of the dc-link voltage. It is then eliminated by an extra compensation loop. Notably, the proposed compensation scheme can also be regarded as a hardware method. Compared with tradition hardware methods, e.g., by measuring inverter output voltage [6], [14], [15], [19], grid current [21] and dc-link current [20], the difference is that, as the dc-link voltage is usually measured in the PV system control, no extra sensors and hardware circuits are needed in the proposed method. Therefore, the impact of the proposed compensation method on the system stability and its control complexity are almost the same as the traditional hardware methods. The main contributions of this paper are summarized as:

1) The root-causes of the dc current injection and its impact on the system are analyzed in detail.
2) A cost-effective current control and compensation method is proposed to suppress the dc current injection without any extra sensors and hardware circuits, thus, maintaining the overall cost of the PV system.
3) Design guidelines for the proposed strategy are presented in detail and its dc injection rejection capability is evaluated, enabling its wide application.

The rest of this paper is organized as follows. In Section II, the root causes of the dc current injection and its impact on systems are analyzed. The proposed current control scheme is then detailed in Section III, followed by the proposed compensation method. Experimental tests are performed on a 1.2-kW single-stage single-phase PV inverter. The results are provided in Section V, where the proposed method is also benchmarked with prior-art solutions. Finally, concluding remarks are provided in Section VI.

II. DC Injection Analysis

A. System Configuration and Modeling

The circuit configuration and a typical cascaded control structure of the studied single-phase transformerless PV grid-connected system are shown in Fig. 1. The PV grid-connected system is built with a single-stage highly efficient and reliable inverter concept (HERIC) to realize the dc/ac inversion, maximum power point tracking (MPPT) and transfer the power derived from the solar array to the grid. The

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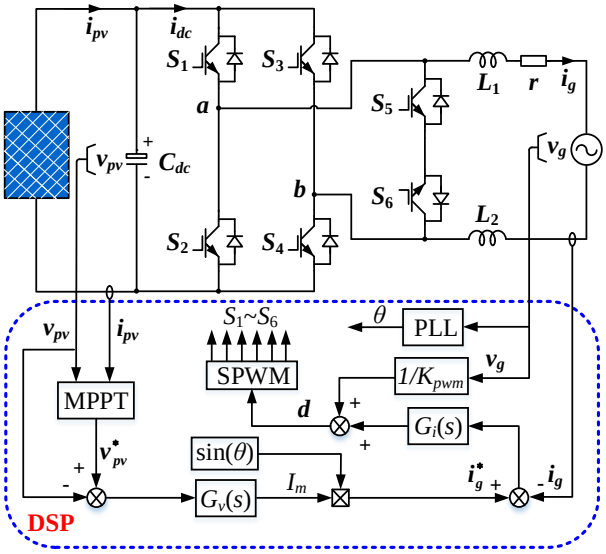

Fig.1. System schematics and control diagrams of a single-phase transformerless grid-connected PV system (L_1=L_2, MPPT is maximum power point tracking, PLL is phase locked loop, SPWM is sinusoidal pulse width modulation, DSP is digital signal processor).

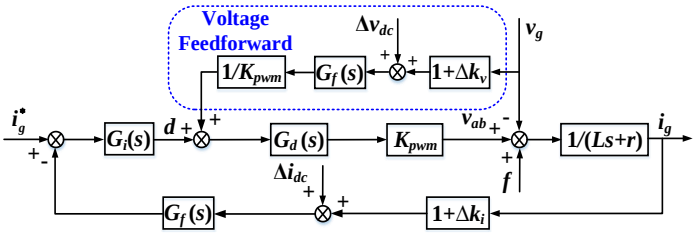

Fig. 2. Detailed control block diagram of the current loop.

main role of the two auxiliary switches S_5 and S_6 of the HERIC is to suppress leakage currents [29]. Considering the electromagnetic interference (EMI) filter and the grid line impedance in the practical inverter system, the ac filter is a *LCL* configuration. However, as the inverter is connected with an ideal programmable ac source and no EMI filters are considered in this study, for simplicity, the *L*-type (L_1 = L_2) filter is adopted instead of an *LCL* filter to demonstrate the proposed dc current injection suppression strategy.

According to Fig. 1, the single-phase grid-connected PV inverter can be modeled as

$$C_{dc}\frac{dv_{pv}}{dt}=i_{pv}-i_{dc} \tag{1}$$

$$L\frac{di_g}{dt}=v_{ab}-ri_g-v_g \tag{2}$$

where L=L_1+L_2 with r being the total series equivalent resistance of the filter inductors, i_{dc} is the dc-link current, v_{pv} and i_{pv} are the PV output voltage (dc-link voltage) and current, respectively, v_g and i_g are the grid voltage and current, respectively.

In order to control this PV grid-connected system, a typical cascaded control, as shown in Fig. 1, is presented, where v_{pv}^* is the voltage reference generated by the MPPT algorithm; $G_v(s)$ is voltage loop regulator; $G_i(s)$ is the current loop regulator; K_{pwm} is the gain of PWM modulator. The grid voltage feedforward is usually added into the current loop to suppress the background harmonics and disturbances of grid voltage.

B. Root-Causes of the DC Current Injection

In order to explore the mechanism of the dc current injection and its impact on the system performance, the actual current loop control block diagram is shown in Fig. 2, where $G_f(s)\approx 1/(T_f s+1)$ is the sampling delay caused by filter in conditioning circuit and T_f being its time constant; $G_d(s)\approx e^{-1.5T_s s}\approx 1/(1.5T_s s+1)$ is the total control delay in the digital control system, including the analog to digital conversion (ADC) delay, computation delay and pulse width modulation (PWM) delay with T_s being the sampling period; Δi_{dc} and Δk_i are the dc offset and scaling error in the grid current measurement, respectively; Δv_{dc} and Δk_v are the dc offset and scaling error in the grid voltage measurement; f represents the disturbance caused by disparity of power modules and asymmetry of driving pulse, and others. Ideally, if the current, voltage sensors and the conditioning circuit are accurate enough, driving pulses are symmetrical and there is no disparity in power modules, the dc offset Δi_{dc}, Δv_{dc}, the scaling error Δk_i and Δk_v and disturbance f will be zero.

According to Fig. 2, the closed-loop transfer function of the grid current in the *s*-domain is derived as

$$\begin{aligned} i_g(s)=&G_{c-ig}(s)i_g^*+G_{c-\Delta idc}(s)\Delta i_{dc}+G_{c-vg}(s)v_g\\ &+G_{c-\Delta vdc}(s)\Delta v_{dc}+G_{c-f}(s)f \end{aligned} \tag{3}$$

where $G_{c\text{-}ig}(s)$, $G_{c\text{-}\Delta idc}(s)$, $G_{c\text{-}vg}(s)$, $G_{c\text{-}\Delta vdc}(s)$ and $G_{c\text{-}f}(s)$ are the closed-loop transfer function from the current reference i_g^*, dc offset of the grid current Δi_{dc}, grid voltage v_g, dc offset of the grid voltage and disturbance to the grid current i_g, respectively. They are defined as

$$G_{c-ig}(s)=\frac{i_g(s)}{i_g^*(s)}=\frac{G_i(s)G_d(s)K_{pwm}}{Ls+r+G_i(s)G_d(s)G_f(s)K_{pwm}(1+\Delta k_i)} \tag{4}$$

$$G_{c-\Delta idc}(s)=\frac{i_g(s)}{-\Delta i_{dc}(s)}=\frac{G_i(s)G_d(s)G_f(s)K_{pwm}}{Ls+r+G_i(s)G_d(s)G_f(s)K_{pwm}(1+\Delta k_i)} \tag{5}$$

$$G_{c-vg}(s)=\frac{i_g(s)}{v_g(s)}=\frac{(1+\Delta k_v)G_d(s)G_f(s)-1}{Ls+r+G_i(s)G_d(s)G_f(s)K_{pwm}(1+\Delta k_i)} \tag{6}$$

$$G_{c-\Delta vdc}(s)=\frac{i_g(s)}{\Delta v_{dc}(s)}=\frac{G_d(s)G_f(s)}{Ls+r+G_i(s)G_d(s)G_f(s)K_{pwm}(1+\Delta k_i)} \tag{7}$$

$$G_{c-f}(s)=\frac{i_g(s)}{f(s)}=\frac{1}{Ls+r+G_i(s)G_d(s)G_f(s)K_{pwm}(1+\Delta k_i)} \tag{8}$$

From (4)-(8), it can be seen that due to the digital and sampling delays in the control system, the dc offset in the grid voltage measurement results in dc component in the grid current. What's more, the background harmonics and disturbances of the grid voltage cannot be fully suppressed by the voltage feedforward method. To realize the zero steady-state error tracking of the grid current, a PR controller is usually adopted in the current loop [30]. Its transfer function in the *s*-domain is given as

$$G_{PR}(s)=k_p+\frac{2k_r\omega_c s}{s^2+2\omega_c s+\omega_0^2} \tag{9}$$

where k_p and k_r are the proportional and resonant gain, respectively. ω_c is the cutoff frequency of the resonant

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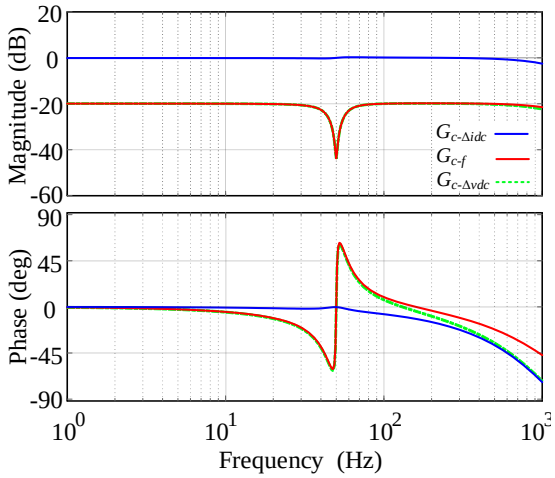

Fig.3. Bode diagram of *Gc-Δidc*(*s*), *Gc-Δvdc* (*s*) and *Gc-f* (*s*) with the scaling factor of the grid current and voltage measurement being 1.

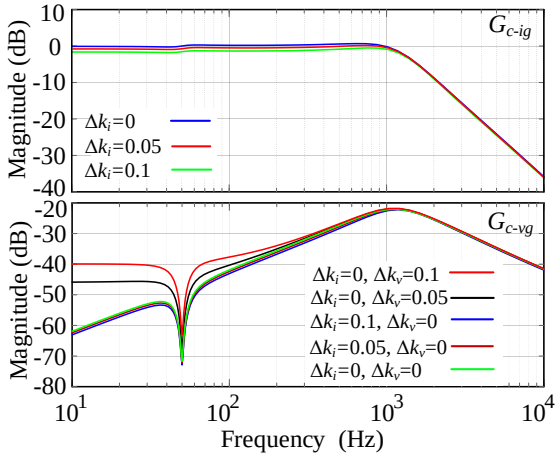

Fig.4. Bode diagram of *Gc-ig*(*s*), *Gc-v*g (*s*) with different grid voltage and current measurement scaling factors.

controller, and ω_0 is the fundamental angular frequency of the grid voltage.

The magnitudes of $G_{c\text{-}\Delta idc}(s)$, $G_{c\text{-}\Delta vdc}$ (*s*), and $G_{c\text{-}f}$ (*s*) at the frequency of 0 Hz correspondingly decide the dc injection rejection capability. Thus, the dc injection caused by disturbances, grid voltage and current dc offset measurement are given as

$$I_{dc-\Delta idc} = \Delta i_{dc} G_{c-\Delta idc}(s)|_{s=j2\pi 0} \approx \frac{\Delta i_{dc}}{1+\Delta k_i} \tag{10}$$

$$I_{dc-\Delta vdc} = \Delta v_{dc} G_{c-\Delta vdc}(s)|_{s=j2\pi 0} \approx \frac{\Delta v_{dc}}{k_p(1+\Delta k_i)K_{pwm}} \tag{11}$$

$$I_{dc-f} = f G_{c-f}(s)|_{s=j2\pi 0} \approx \frac{f}{k_p(1+\Delta k_i)K_{pwm}} \tag{12}$$

According to (10)-(12), it can be seen that the scaling error of the grid current measurements will amplify the dc component if its value is negative. Although increasing the proportional gain of the PR controller contributes to the reduction of the dc component caused by disturbances and dc offset in grid voltage measurement, a large gain may affect the system stability. Fig. 3 shows the Bode diagram of $G_{c\text{-}\Delta idc}(s)$, $G_{c\text{-}f}$ (*s*), $G_{c\text{-}\Delta vdc}$ (*s*) in the case of the scaling errors in the grid current and voltage measurement being zero. The parameters of PR controller designed in [31] are adopted here and the parameters of the entire system are listed in Table I. From Fig. 3, it is indicated that $G_{c\text{-}\Delta idc}(s)$ produces a unity gain (0 dB) at 0 Hz, which means that the dc component caused by the dc offset in the grid current measurement cannot be suppressed by the current controller. In addition, the gain of $G_{c\text{-}f}$ (*s*) and $G_{c\text{-}\Delta vdc}$ (*s*) at 0 Hz is -20 dB, which is not sufficient to effectively suppress the dc component caused by disturbances and dc offset in the grid voltage measurement. In addition, Fig. 4 shows the Bode diagram of $G_{c\text{-}ig}(s)$ and $G_{c\text{-}vg}$ (*s*) with different grid current and voltage measurement scaling errors. Observations from Fig. 4 indicate that the scaling error of the grid current measurement will lead to current tracking errors, but it has negligible effect on the grid voltage disturbance suppression. While, the scaling error in the grid voltage measurement will reduce the capability to attenuate the low frequency harmonics of the grid voltage.

C. DC-Link Voltage Line-Frequency Ripple Analysis

Rewriting (1) as

$$\frac{1}{2}C_{dc}\frac{dv_{pv}^2}{dt} = v_{pv}i_{pv} - v_{pv}i_{dc} \tag{13}$$

When neglecting the power losses of the system and the small instantaneous power of the filter inductor, (13) is rewritten as

$$\frac{1}{2}C_{dc}\frac{dv_{pv}^2}{dt} = v_{pv}i_{pv} - v_g i_g \tag{14}$$

Assuming that the grid voltage is ideally sinusoidal and the grid current has a dc component I_{DC}, that is, the grid voltage and current are expressed as

$$v_g = V_m \sin(\omega_0 t) \tag{15}$$

$$i_g = I_m \sin(\omega_0 t + \varphi_i) + I_{DC} \tag{16}$$

where V_m and ω_0 are the amplitude and angular frequency of the grid voltage, respectively; I_m is the amplitude of the grid current, and φ_i is the phase angle of the grid current referring to the grid voltage phase. Substituting (15) and (16) into (14), and considering unity power factor operation, we have

$$C_{dc}\frac{dv_{pv}^2}{dt} = 2P_{pv} - V_m I_m + V_m I_m \cos(2\omega_0 t) - \underbrace{2I_{DC}V_m \sin(\omega_0 t)}_{P_{f0}} \tag{17}$$

where $P_{pv} = v_{pv}i_{pv}$ is the PV output power and P_{f0} is the line-frequency power caused by dc current injection.

From (17), it can be seen that the dc-link voltage will naturally include the line-frequency ripple if the grid current has a dc component. In addition, it should be noticed that, in PV system, as the PV output power is always oscillating with the dc-link voltage ripple, it will inevitably contain line-frequency power oscillations. This will in turn affect the line-frequency ripple on the dc-link voltage. However, through analysis (shown in the Appendix I and according to (17)), it can be found that the grid current dc component is the dominant or even the only cause for the dc-link voltage line-frequency ripple. What's more, compared with the line-frequency power caused by dc current injection i.e., P_{f0}, the line-frequency power in P_{pv} is much smaller. Thus, in this paper, the oscillation of PV output power is neglected thereafter for simplicity.

Based on the above analysis, the impact of the disturbances, dc offset and scaling error in the grid voltage and current measurements on the entire inverter system can be summarized

as follows. 1) The dc component caused by the dc offset of current measurements cannot be mitigated by the current controller. By contrast, increasing the low frequency gain of the current controller benefits to reduce the dc component produced by the dc offset of the voltage measurement and disturbances. 2) The dc current injected into the grid will produce a line-frequency ripple on the dc-link voltage, which in turn will lead to 2nd-order harmonics in the grid current. Moreover, negative scaling errors in the grid current measurement will worsen the dc injection issue, and thus increasing the dc-link voltage line-frequency ripple.

III. Proposed Current Control Scheme

A. Current Controller Design

As analyzed in Section II, the scaling error in the grid voltage measurement will lower the capability to suppress low frequency harmonics of the grid voltage. What's more, the dc component caused by disturbance and dc offsets in the grid voltage measurement can be suppressed by properly designing the current controller. Therefore, to eliminate the influence of the grid voltage measurement scaling errors on the system and to suppress dc component caused by the dc offset of the grid voltage measurement and disturbances, a PIR current controller is employed, which can be expressed as

$$G_i(s) = \underbrace{k_p + \frac{k_i}{s}}_{\text{PI}} + \underbrace{\frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega_0^2}}_{\text{R}} \tag{18}$$

where k_i is the integral gain. In (18), the PI controller is used to increase the low frequency gain and ensure a good dynamic response of the system, while the resonant (R) controller is used to achieve zero steady-state error tracking of the grid current.

Referring to Fig. 2, the open-loop transfer function of the current loop with the proposed PIR controller is obtained as

$$G_{o-PIR}(s) = G_i(s)G_d(s)G_f(s)K_{pwm}\frac{1}{Ls+r}(1+\Delta k_i) \tag{19}$$

To ensure fast dynamics, maintain good steady-state performance of the system, and eliminate the dc current injection caused by disturbances and the grid voltage measurement errors, the design requirements of the PIR controller are listed as follows:

1) A large phase margin (PM), PM ≥ 45 °, is set to ensure a good dynamic response and robustness.

2) The gain at the low frequency band (≤ 1 Hz) is larger than 50 dB to ensure good dc current injection suppression.

3) $|G_{o\text{-}PIR}(j\omega_0)| \geqslant 50$ dB is set for small steady-state errors.

As the R controller only provides a large gain at the frequency close to the selected resonance frequency (ω_0), and the crossover frequency f_c of the system is usually set far away from ω_0, the PIR controller can be approximated to be a PI controller at the low frequency band and the frequencies higher than f_c [32]. Thus, when the requirements 1) and 2) are considered, the PIR controller is simplified as

$$G_i(s) = k_p + \frac{k_i}{s} \tag{20}$$

According to (19), the PM of the system is expressed as

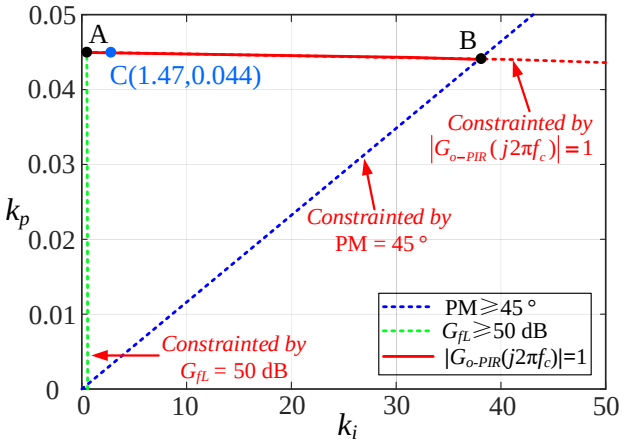

Fig.5. Regions of the control gain k_p and k_i constrained by the design requirements of 1) and 2).

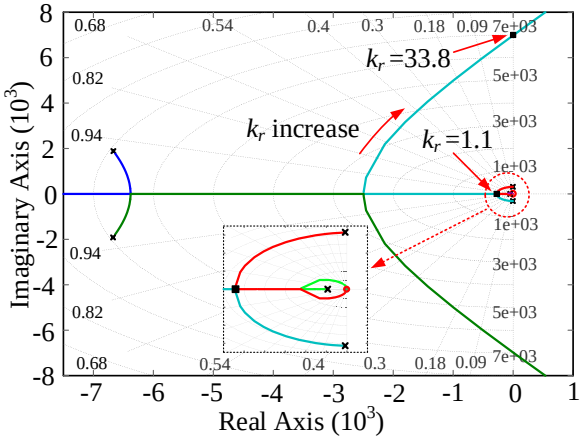

Fig.6. Root locus of the current loop with the gain k_r varying from 0 to infinity.

$$\text{PM} = 180^\circ + \angle\frac{G_i(s)G_d(s)G_f(s)K_{pwm}(1+\Delta k_i)}{Ls+r}\bigg|_{s=j2\pi f_c} \tag{21}$$

To facilitate the analysis, the scaling error Δk_i in the grid current measurement is assumed as zero in the controller design. Then, substituting (20) into (21) gives

$$\begin{aligned}\text{PM} = 90^\circ &+ \arctan\frac{2\pi f_c k_p}{k_i} - \arctan 3\pi T_s f_c \\ &- \arctan 2\pi T_f f_c - \arctan\frac{2\pi f_c L}{r}\end{aligned} \tag{22}$$

For $|G_{o\text{-}PIR}(j2\pi f_c)|$=1, the relationship of k_p and k_i is obtained as

$$4\pi^2 f_c^2 k_p^2 + k_i^2 = \frac{4\pi^2 f_c^2(4\pi^2 f_c^2 L^2 + r^2)(9\pi^2 f_c^2 T_s^2 + 1)(4\pi^2 f_c^2 T_f^2 + 1)}{K_{pwm}^2} \tag{23}$$

The gain at low frequency f_L is then expressed as

$$\begin{aligned}G_{f_L} &= 20\log_{10}|G_{o-PIR}(j2\pi f_L)| \\ &= 20\log_{10}\left(\frac{K_{pwm}\sqrt{4\pi^2 f_L^2 k_p^2 + k_i^2}}{2\pi f_L\sqrt{(4\pi^2 f_L^2 L^2 + r^2)(9\pi^2 f_L^2 T_s^2 + 1)(4\pi^2 f_L^2 T_f^2 + 1)}}\right)\end{aligned} \tag{24}$$

Based on the design requirements of 1) and 2), the satisfactory region of k_p and k_i can be obtained once f_c and f_L are determined. Generally, f_c can be set as one tenth of the sampling frequency to ensure fast dynamics. However, owing to the

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$$k_r = \sqrt{10^{\frac{G_{f0}}{10}} \frac{(4\pi^2 f_0^2 L^2 + r^2)(9\pi^2 f_0^2 T_s^2 + 1)(4\pi^2 f_0^2 T_f^2 + 1)}{K_{pwm}^2} - \frac{k_i^2}{4\pi^2 f_0^2}} - k_p \tag{26}$$

$$G_{o-k_r}(s) = \frac{2k_r K_{pwm}\omega_c s^2}{(s^2 + 2\omega_c s + \omega_0^2)\left\{1.5LT_sT_f s^3 + (1.5rT_sT_f + 1.5LT_s + LT_f)s^2 + (1.5rT_s + rT_f + k_p K_{pwm} + L)s + r + k_i K_{pwm}\right\}} \tag{27}$$

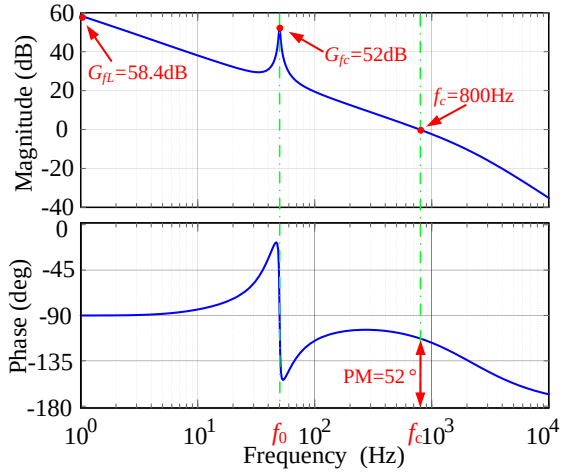

Fig.7. Bode diagram of $G_{o\text{-}PIR}(s)$ with the designed controller.

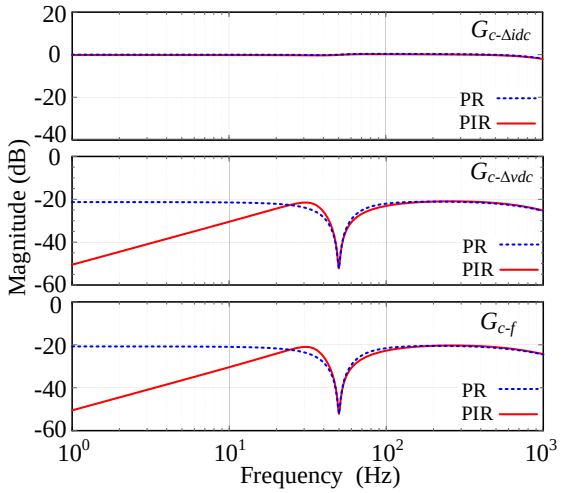

Fig.8. Bode diagram of $G_{c\text{-}\Delta idc}(s)$, $G_{c\text{-}\Delta vdc}(s)$ and $G_{c\text{-}f}(s)$ with a PR or a PIR controller.

control delay and sampling delay in practice, the large current loop bandwidth will cause stability issue. With this, in this study, f_c is set as approximately 4% of the sampling frequency f_s (i.e, 0.8 kHz) to achieve a sufficient PM and small overshoot [33]. Considering the dc offset of the grid voltage measurement and disturbances vary at a low frequency, it is reasonable to set f_L as 1 Hz to ensure an enough gain. According to the system parameters in Table I, the satisfactory region of k_p and k_i is depicted, as shown in Fig. 5. The red solid line from point A to B includes all the possible k_p and k_i that meet the aforementioned design requirements. To reduce the order of the system, the pole-zero compensation technique is used. Thus, the controller gains k_p and k_i are selected as $k_p/k_i=L/r$. Consequently, the point C shown in Fig.5 is a proper design. However, it should be noted that as the R controller can introduce negative phase shift at the frequencies higher than the resonant frequency, the PM will not hold. Therefore, it is necessary to check the system PM. If it does not meet the design requirements, the crossover frequency f_c should be adjusted following a few iterations of k_p and k_i.

Regarding the design of the R controller, ω_c is the cut-off frequency. In view of a typical ±1% variation of the grid fundamental frequency [34], the ω_c is set as 1% $2\pi f_0 = \pi$ rad/s. To satisfy the requirement 3), the gain at resonant frequency f_0 should be calculated first, it is shown as

$$\begin{aligned} G_{f_0} &= 20\log_{10}\left|G_{o-PIR}(s)\right|_{s=j2\pi f_0} \\ &= 20\log_{10}\left|\frac{G_i(s)G_d(s)G_f(s)K_{pwm}}{Ls+r}\right|_{s=j2\pi f_0} \end{aligned} \tag{25}$$

where $G_i(s)$ is the PIR controller.

Rewriting (25), the resonant gain k_r is expressed as (26), shown at the top of this page. From (26), it can be seen that increasing k_r contribute to increase the gain at the frequency f_0. Thus, to meet the requirement 3), it is better to select k_r as large as possible. However, it will degrade the system stability, which limits the range of the gain k_r. According to (19), the equivalent open-loop transfer function related to the gain k_r is given in (27). Thus, the root locus of the current loop with k_r varying from 0 to infinity is depicted in Fig.6, where the system parameters are listed in Table I. From Fig.6, it can be seen that the closed-loop system is stable when $k_r < 33.8$. To achieve a sufficient stability margin as well as meet the requirement $G_{f0} \geq 50$ dB, k_r is set as 1.18 in this paper, where two dominant poles are located at the same place in the real axis. Fig.7 then shows the Bode diagram of the open-loop transfer function $G_{o\text{-}PIR}(s)$ with the designed controller parameters. As it can be observed in Fig.7, the crossover frequency f_c of the system is 800 Hz with the PM being 52 °and the gain at fundamental frequency f_0 being 52 dB. This indicates that the system is stable with a good steady-state and dynamic performance.

B. Evaluation of the DC Current Suppression Capability

Substituting the proposed PIR controller into (5), (7) and (8), the magnitude of $G_{c\text{-}\Delta idc}(s)$, $G_{c\text{-}\Delta vdc}(s)$ and $G_{c\text{-}f}(s)$ at the low frequency f_L determines the magnitude of the injected dc current. From (5), (7) and (8), we have

$$G_{c-\Delta idc} = 20\log_{10}\left|\frac{i_g(s)}{\Delta i_{dc}(s)}\right|_{s=j2\pi f_L} \tag{28}$$

$$G_{c-\Delta vdc} = 20\log_{10}\left|\frac{i_g(s)}{\Delta v_{dc}(s)}\right|_{s=j2\pi f_L} \tag{29}$$

$$G_{c-f} = 20\log_{10}\left|\frac{i_g(s)}{f(s)}\right|_{s=j2\pi f_L} \tag{30}$$

Thus, the dc current caused by grid current and voltage measurement errors and disturbances is determined as

$$I_{dc-\Delta idc} = \Delta i_{dc} 10^{\frac{G_{c-\Delta idc}}{20}} \tag{31}$$

$$I_{dc-\Delta vdc} = \Delta v_{dc} 10^{\frac{G_{c-\Delta vdc}}{20}} \tag{32}$$

$$I_{dc-f} = f 10^{\frac{G_{c-f}}{20}} \tag{33}$$

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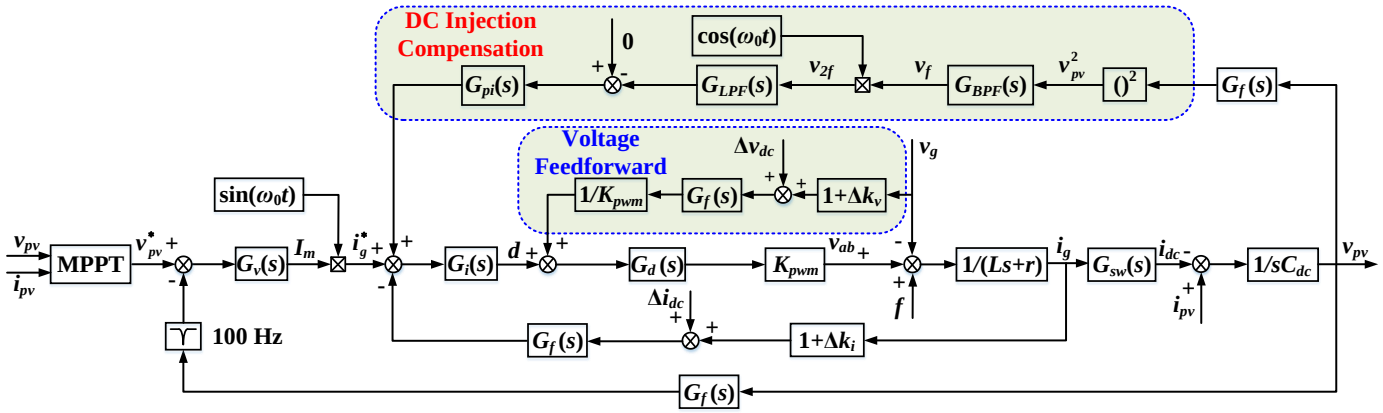

Fig.9. Block diagram of the entire control scheme of the single-phase inverter with the proposed control and compensation scheme.

Fig. 8 shows the frequency response of $G_{c\text{-}\Delta idc}(s)$, $G_{c\text{-}\Delta vdc}(s)$ and $G_{c\text{-}f}(s)$, where PR controller and PIR controller are adopted in the current loop. In Fig. 8, the magnitude of $G_{c\text{-}\Delta vdc}(s)$ at the low frequency f_L(1Hz) with the PR and PIR controller are 20.6 and 50.4 dB, respectively. By contrast, the magnitude of $G_{c\text{-}f}(s)$ at the low frequency f_L with the PR and PIR controller are 20.3 and 50.2 dB, respectively. Thus, according to (32) and (33), the injected dc current caused by the grid voltage measurement error can be approximately determined as $I_{dc\text{-}\Delta vdc}$=0.093Δvdc with the PR controller and $I_{dc\text{-}\Delta vdc}$ =0.003Δvdc with the proposed PIR controller. Similar results can be obtained from $G_{c\text{-}f}(s)$ with the PR and PIR controller. Obviously, due to the large low frequency gain of the proposed controller, the injected dc current caused by the grid voltage measurement error and disturbances can be mitigated to a large extent. Nevertheless, as shown in Fig.8, the magnitude of $G_{c\text{-}\Delta idc}(s)$ at the low frequency f_L with the PR and PIR controller is nearly 0 dB, which indicates that the injected dc current induced by the grid current measurement errors cannot be mitigated by the current controller.

IV. Proposed DC Injection Compensation Scheme

From the above, it is known that the current controller cannot suppress the dc component resulted from the grid current measurement errors. This is because the grid current is the feedback signal of the current controller, utilizing the current controller to suppress the dc injection caused by measurement errors in the feedback path will be ineffective. Thanks to the physical relationship between the dc current injection and the line-frequency ripple of the dc-link voltage, as shown in Section II-*C*, the dc component produced by grid current measurement error can be estimated indirectly. As a result, an effective dc injection compensation scheme is developed.

A. Proposed DC Injection Compensation Scheme

From (17), the dc-link line-frequency voltage ripple caused by the dc injection of the grid current is derived as

$$\frac{dv_f}{dt} = -\frac{2I_{DC}V_m}{C_{dc}}\sin(\omega_0 t) \Leftrightarrow v_f = \frac{2I_{DC}V_m}{C_{dc}\omega_0}\cos(\omega_0 t) \tag{34}$$

where v_f is the line-frequency ripple of the dc-link voltage v_{pv}^2.

In order to extract the line-frequency ripple v_f from v_{pv}^2, a band- pass filter with the central frequency at ω_0 is introduced as

$$G_{BPF}(s) = \frac{\omega_b s}{s^2 + \omega_b s + \omega_0^2} \tag{35}$$

where $\omega_b = 2\pi$ (rad/s) is the bandwidth of the band-pass filter.

The obtained line-frequency voltage ripple v_f is then multiplied by cos($\omega_0 t$), and thus, a dc component proportional to I_{DC} is generated, which is expressed as

$$v_{2f} = \frac{I_{DC}V_m}{C_{dc}\omega_0} + \frac{I_{DC}V_m}{C_{dc}\omega_0}\cos(2\omega_0 t) \tag{36}$$

Following, a second-order low-pass filter (LPF) shown in (37) is then used to extract the dc component.

$$G_{LPF}(s) = \frac{\omega_n^2}{s^2 + \xi\omega_n s + \omega_n^2} \tag{37}$$

where ξ is the damping coefficient and ω_n is the natural angular frequency. They are set as 1 and 20π (rad/s), respectively.

Subsequently, the estimated dc component is expressed as

$$v_{dc} = \mathrm{LPF}\{v_{2f}\} = \frac{I_{DC}V_m}{C_{dc}\omega_0} \tag{38}$$

After the dc component is estimated by (38), it can be eliminated through an indirect compensation loop. Fig. 9 shows the entire control and compensation block diagram of the single-phase inverter system, where $G_{sw}(s)$ represents the switching function of the inverter, and $G_{pi}(s)$ is a PI controller that is utilized to suppress the dc injection by controlling the estimated dc component to zero. Notably, as it can be seen in Fig. 9, since the dc-link voltage reference generated by MPPT algorithm changes very slowly, it can be viewed as a constant. Therefore, if the bandwidth of voltage loop is high, the dc-link voltage can track it reference well, which will lead to the dc-link voltage ripple to be significantly attenuated and the grid current to be greatly distorted. So, in this study, the voltage loop bandwidth is set 20 Hz. This low bandwidth is helpful for blocking the line-frequency ripple from penetrating into the current loop. And thus, it is beneficial for the proposed compensation strategy.

B. Evaluation of the DC Injection Rejection Capability

To evaluate the proposed compensation scheme, the equivalent control block diagram of the dc injection

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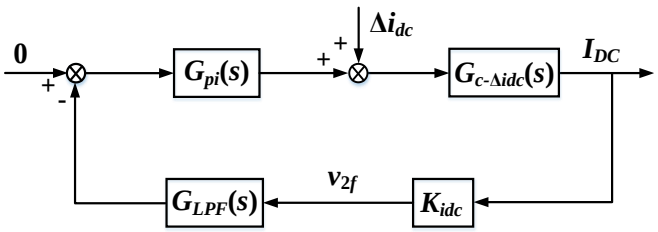


Fig.10. Equivalent control block diagram of the proposed compensation scheme.

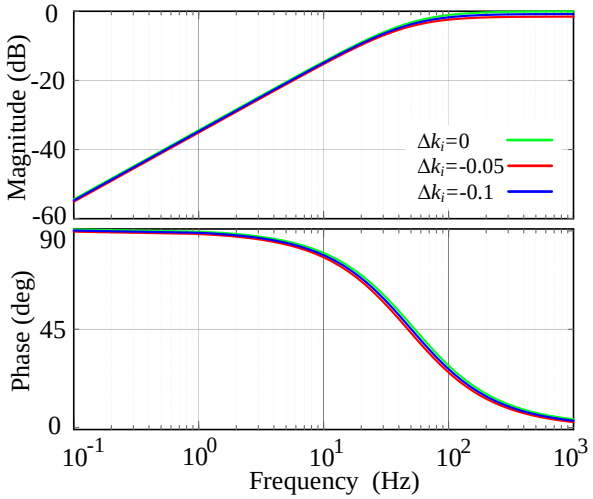


Fig. 11. Bode diagram of transfer function $G_{c\text{-}Idc}(s)$ with the proposed dc injection compensation scheme.

suppression is shown in Fig. 10, where K_{idc} is the steady-state gain from the dc injection I_{DC} to v_{2f}, it is shown as

$$K_{idc} = \frac{V_m}{2C_{dc}\omega_0} \tag{39}$$

The detailed derivation of K_{idc} can be found in the Appendix II. Since we only focus on the very low frequency range, $G_{c\text{-}\Delta idc}(s)$ and $G_{LPF}(s)$ can be approximated as gains, shown as

$$G_{c-\Delta idc}(s) = \frac{G_i(s)G_d(s)G_f(s)K_{pwm}}{Ls + r + G_i(s)G_d(s)G_f(s)K_{pwm}(1+\Delta k_i)}\bigg|_{s=j2\pi\cdot 0} \approx \frac{1}{1+\Delta k_i} \tag{40}$$

$$G_{LPF}(s) = \frac{\omega_n^2}{s^2 + \xi\omega_n s + \omega_n^2}\bigg|_{s=j2\pi\cdot 0} \approx 1 \tag{41}$$

Thus, the closed-loop transfer function of the system from Δi_{dc} to I_{DC} is obtained as

$$G_{c-Idc}(s) = \frac{I_{DC}}{\Delta i_{dc}} = \frac{1/(1+\Delta k_i)}{1 + \frac{1}{1+\Delta k_i}\frac{V_m}{2C_{dc}\omega_0}(k_{pdc} + \frac{k_{idc}}{s})} \tag{42}$$

Regarding the parameters selection of the PI controller, the rule is to ensure the closed-loop transfer function $G_{c\text{-}Idc}(s)$ has a large attenuation gain at the low frequency range. In this paper, the proportional gain k_{pdc} and integral gain k_{idc} are set as 0.0003 and 1, respectively. Fig. 11 shows the Bode diagram of the closed-loop transfer function $G_{c\text{-}Idc}(s)$ with the scaling error Δk_i of the grid current measurement varying from -0.1 to 0. As it can be observed in Fig. 11, the gain at the low frequency f_L (1Hz) is -33 dB. Thus, the injected dc current can be suppressed to a large extent. What's more, even if the scaling error in the grid current measurement is around -0.1, the impact on the low frequency attenuation is negligible. In all, the proposed compensation strategy has strong ability to reject the dc current injection.

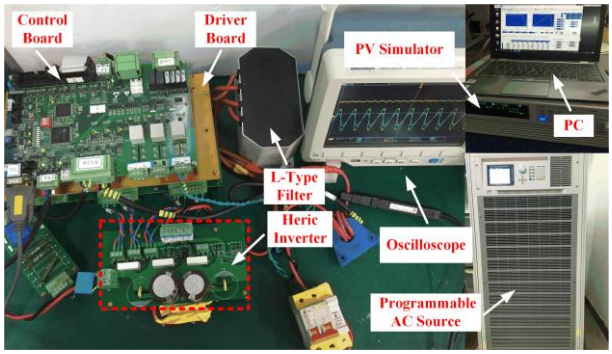


Fig.12. Experimental setup of the 1.2-kW single-phase HERIC inverter system.

TABLE I
EXPERIMENTAL PARAMETERS

Parameters	Values	Parameters	Values
Output Power: P_o	1.2 kW	Filter delay time :T_f	39.6 μs
MPP voltage: v_{pv}	220 V	Proportional gain :k_p	0.042
Grid voltage: v_g (rms)	110 V	Integral gain : k_i	1.4
Grid frequency: f_g	50 Hz	Resonant gain: k_r	1.18
Switching frequency: f_{sw}	20 kHz	Cutoff frequency: ω_c	π
Sampling frequency: f_s	20 kHz	Proportional gain: k_{pdc}	0.0003
Filter inductor: L	3 mH	Integral gain: k_{idc}	1
Equivalent resistance: r	0.1 Ω	DC-link capacitor: C_{dc}	1400 μF

TABLE II
THE VALUES OF DC INJECTION SOURCE

Parameters	Values	Parameters	Values
Disturbance: f	2 V	Scaling error in current measurement: Δk_i	-0.03
DC offset in voltage measurement: Δv_{dc}	4 V	DC offset in current measurement: Δi_{dc}	0.2 A
Scaling error in voltage measurement: Δk_v	-0.03		

TABLE III
CONDITIONS OF THE EXPERIMENTAL TESTS

Cases	f	Δv_{dc}	Δk_i	Δi_{dc}	Δk_v	DC injection suppression strategy	Solar irradiance step change
Case I	✓	✓	✗	✓	✗	PR	✗
Case II	✓	✓	✓	✓	✗	PR	✗
Case III	✓	✓	✗	✓	✗	PIR	✗
Case IV	✓	✓	✓	✓	✗	PIR + Compensation	✗
Case V	✓	✓	✓	✓	✗	PR + Virtual capacitor	✗
Case VI	✓	✓	✓	✓	✗	PIR + Compensation	✓
Case VII	✓	✗	✓	✗	✗	PIR	✗

V. Experimental Results

A 1.2-kW single-phase transformerless grid-connected PV inverter prototype, as shown in Fig. 12, has been built and tested to verify the effectiveness of the proposed method. The controller is implemented by a floating-point digital signal processor (DSP) TSM320F28335 and the gate-driving signals of the IGBT devices are generated by a field programmable gate array (FPGA) EP2C8T144C8N. A HIOKI 3390 power analyzer is used to measure the power quality of the grid voltage and current. A Chroma PV simulator and a programmable ac source are adopted to imitate the PV array and the power grid, respectively. The key experimental parameters are listed in Table I.

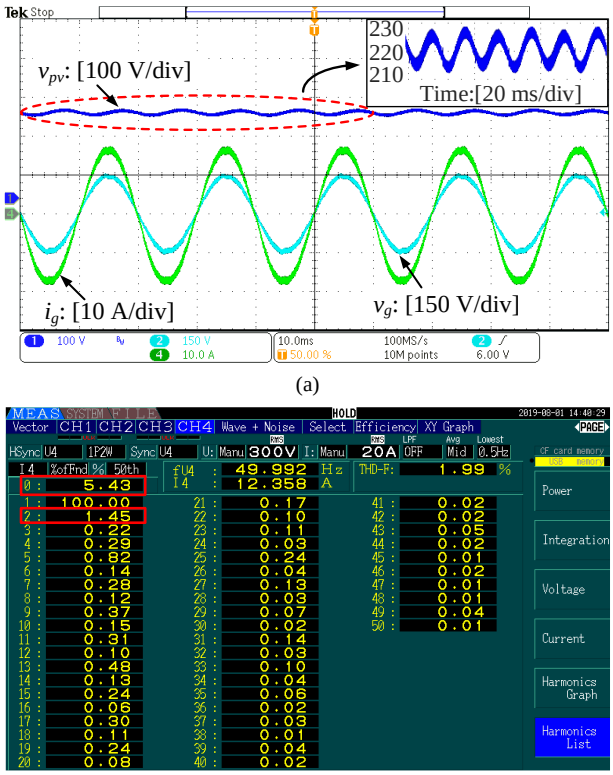
Notably, as the dc-link line-frequency voltage ripple is utilized in the proposed dc injection compensation scheme and its value is small, the sampling precision of the conditioning circuit for the dc-link voltage should be considered. Therefore, two improvements were made in the dc-link voltage conditioning circuit: 1) The precision of the sampling resistor and operational amplifier in the conditioning circuit is improved; 2) In the conditioning circuits, a fixed constant voltage value, e.g., 180V (3V in the conditioning circuit), which is slightly higher than the amplitude of the grid voltage, is subtracted from the measured dc-link voltage. Then, the actual voltage is restored in the DSP by adding the subtracted voltage, i.e., 180V. Based on the above two improvements, the sampling precision of the dc-link voltage meets the requirements in practice. It is worth noting that the dc-link voltage sampling is realized by a resistance voltage divider. Thus, although the accuracy of sampling resistance is improved, it is still economical when compared with active hardware strategies. To verify the effectiveness of the proposed method, the following seven cases are considered, where the values of the disturbance, scaling error and dc offset in the voltage and current measurement are taken from practical applications, as shown in Table II. All the testing conditions are summarized in Table III and described in the following:

1) *Case I*: The grid voltage and current have dc offsets as given in Table II, while the scaling error is zero. There are disturbances in the system. A typical PR controller is adopted in the current loop according to the discussions in previous sections.

2) *Case II*: The grid voltage and current have dc offsets, the scaling error of the current measurement is -0.03. There are disturbances in the system. The PR controller is adopted in the current loop like *Case I*. This study case is used to verify the impact of the current scaling error measurement on the dc current injection in the system.

3) *Case III*: The grid voltage and current have dc offsets, while the scaling error is zero. Disturbances also appear in the system. The proposed PIR controller is then adopted in the current loop. This case is designed to evaluate the capability of the PIR controller to suppress the dc component caused by the grid voltage dc offset measurement and disturbances.

4) *Case IV*: The grid voltage and current have dc offsets, the scaling error of the current measurement is -0.03. Disturbances are also considered in this case. The proposed PIR control and dc injection compensation scheme is activated in order to verify the effectiveness of the proposed dc injection suppression method for single-phase inverters.



(a)

(b)

Fig. 13. Experimental results of the inverter with the PR controller under disturbances and dc offset. (a) Experimental waveform, (b) the fast Fourier transform (FFT) analysis of the grid current.

5) *Case V*: The grid voltage and current have dc offsets, the scaling error of current measurement is -0.03. The disturbances are also present in the system. The virtual capacitor method in [13] is adopted in order to compare the performance of the proposed method.

6) *Case VI*: The grid voltage and current have dc offsets, while in this case, the scaling error of the current measurement is -0.03. There are disturbances in the system. The proposed PIR control and dc injection compensation scheme is activated. The solar irradiance step changes from 1000 W/m^2 to 500 W/m^2 to demonstrate the dynamics and robustness of the system.

7) *Case VII*: The grid voltage and current measurement do not contain dc offsets. The disturbances caused by the disparity of power modules and asymmetry of driving pulses always appear in the system. In this case, only the current loop is adopted in the system (the input of inverter is connected with a dc voltage source) and the scaling error of the current measurement is set as 0.1 to clearly show its impact on the grid current reference tracking and grid voltage disturbance suppression. The proposed PIR control is activated in the current loop.

A. *Case I*

To clearly show the dc injection issue in the transformerless PV inverter system, all possible sources, i.e., the disturbances, the dc offset in the grid voltage and current measurement, are considered in this case. Fig. 13 shows the experimental results

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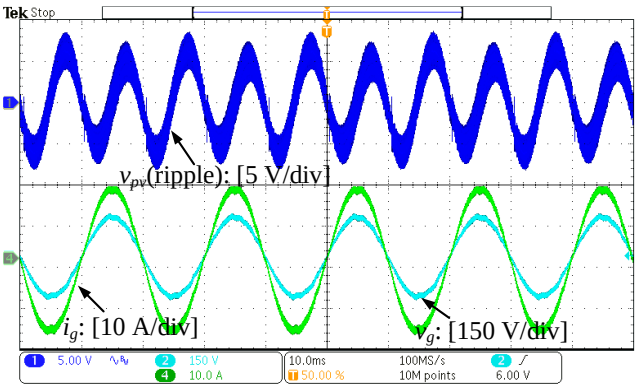
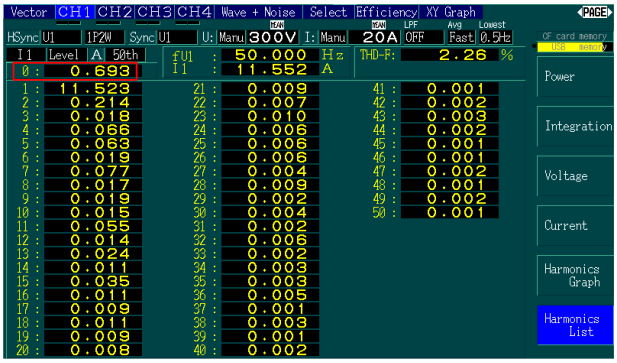


(a)



(b)

Fig. 14. Experimental results of the inverter with the PR controller in the case that the system contains disturbance, grid voltage measurement dc offsets, current measurement dc offset and scaling errors. (a) Experimental waveform; (b) Harmonic level.

of the inverter system with a traditional PR controller in the current loop. From Fig. 13, it can be seen that the dc component in the grid current is 5.43%, which is far higher than 0.5% required in the IEEE Standard 1547-2018 [7]. Furthermore, as analyzed in Section II, the dc component injected into grid will lead to the line-frequency ripple in the dc-link voltage, which increases the 2nd-order harmonics of the grid current. As shown in Fig. 13(a) and (b), the ripple of the dc-link voltage contains line-frequency component and the 2nd-order harmonics of the grid current exceed the threshold in the standards [7]. In all, the results verified the theoretical analysis presented in Section II.

B. Case II

To verify the impact of the grid current measurement scaling error on the dc injection of system, the scaling error in the grid current measurement is set as -0.03. In this test, the disturbances, dc offset in the grid voltage and current measurement are given in Table II. The same experiment test as Case I is considered and the results are shown in Fig. 14. As shown in Fig. 14, since the negative scaling error in the grid current measurement can increase the dc component caused by the dc offset in the current measurement, the dc component of the grid current is higher than that shown in Fig. 13, which goes up to 5.61%, as compared in Table IV. As a result, the higher dc component increases the line-frequency ripple in the dc-link voltage and then further deteriorates the power quality of the grid current. This results in a total harmonic distortion (THD) of the grid current being 2.26%, which was 1.98% in

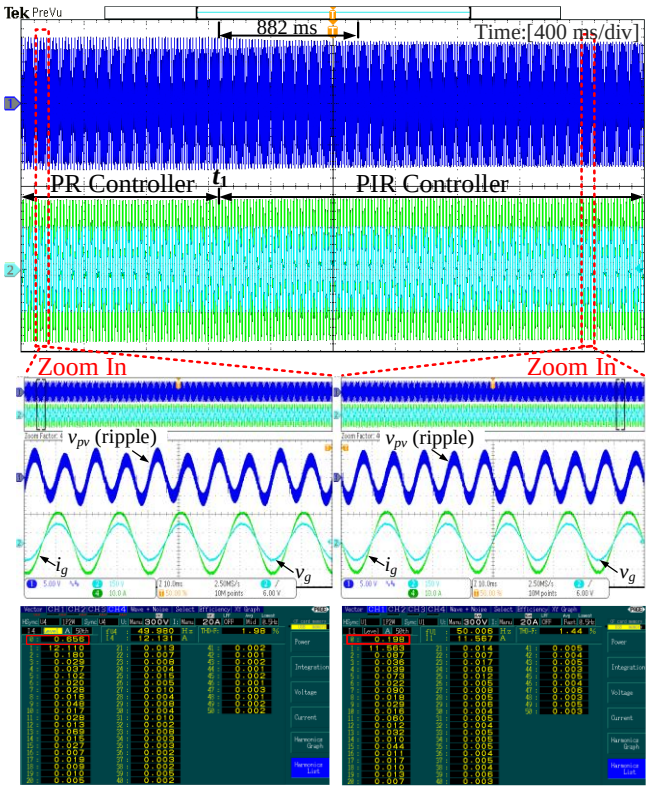


Fig. 15. Experimental results of the inverter with the PIR controller in the case that the system contains disturbances, dc offsets in the grid voltage and current measurement.

TABLE IV
THD AND DC CURRENT COMPONENT OF THE GRID CURRENT

Test Case	DC Component	2nd-order Harmonic (%)	THD (%)
I	5.43% (0.656A)	1.45	1.98
II	5.61% (0.693A)	1.66	2.26
III	1.68% (0.198A)	0.53	1.44
IV	0.24% (0.022A)	0.29	1.25
V	1.72% (0.204A)	0.55	1.45
VI	0.27% (0.025A)	0.32	1.36

Case I. In all, the experimental results are consistent with the theoretical analysis.

C. Case III

To demonstrate the effect of the PIR controller on the dc component suppression, the experiment of the inverter with the grid current controller being the proposed PIR controller under the same conditions of Case I is performed. The results are shown in Fig. 15. As it can be observed in Fig. 15, when the integral term is added into the controller at t_1, the grid current is effectively regulated to be sinusoidal and the dc component is reduced from 5.43% to 1.68%, as compared in Table IV. Thus, it can be concluded that the integral controller added into the current loop contributes the suppression of the dc component of the grid current to a large extent. Nevertheless, the dc component in the grid current is 1.68% (about 0.2 A), which still exceeds the IEEE Standard 1547-2018. This is because, as analyzed in section II-B, the dc

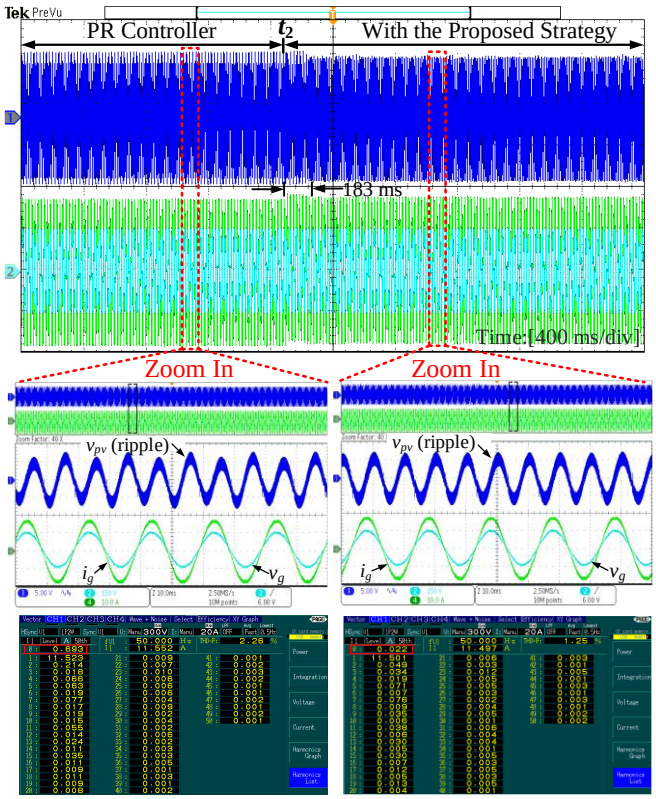


Fig. 16. Experimental results of the inverter with the proposed dc injection compensation strategy in the case that the system contains disturbances, dc offsets in the voltage measurement and dc offset and scaling errors in the current measurement.

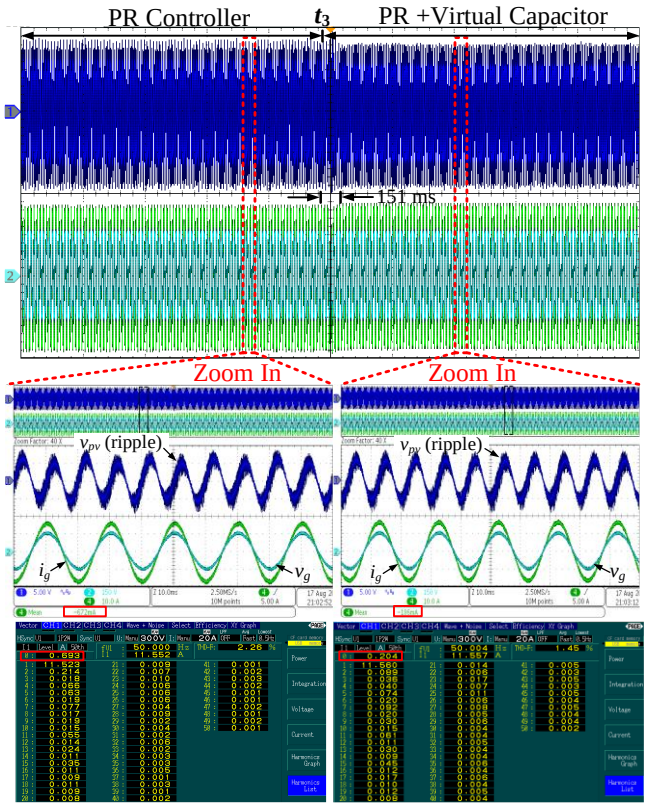


Fig.17. Experimental results of the inverter with the virtual capacitor strategy in the case that the system contains disturbance, grid voltage measurement dc offsets, current measurement dc offsets and scaling errors.

component caused by the dc offset in the grid current measurement cannot be eliminated only by the closed-loop current controller. Therefore, in order to further suppress the dc component, a more effective solution should be developed.

D. Case IV

To verify the efficacy of the proposed compensation method, further experimental tests are carried out. The results are shown in Fig. 16. This case is similar to Case II, where the current controller is the PR controller before t_2, and the system has disturbances, dc offset and scaling error in the voltage and current measurement. Observations from Fig.16 imply that, when the integral term and the compensation strategy are activated at t_2, the dc component in the grid current is mitigated from 5.61% to 0.24% (see Table IV) with less than 0.2s. However, it is worth noting that, as shown in Section IV-B, the theoretical gain of the proposed compensation loop at the low frequency f_L (1Hz) is -33 dB, which means that the dc component caused by the dc offset in the grid current measurement can be mitigated to be nearly zero. The reason for this discrepancy is that the precision of the dc-link voltage sampling is limited in practice. When the dc component of the grid current is reduced to a small value, the dc-link voltage line-frequency ripple will be also very small, which increases the difficulty of the ripple measurement. Nevertheless, the results completely comply with the IEEE 1547-2018 dc current injection limit standards, i.e., <0.5%. In addition, after the proposed method is activated, the ripple in the dc-link voltage purely varies at the double-line frequency. Thus, it benefits to the reduction of the 2nd-order harmonic component of the grid current. In this case, the 2nd-order harmonic and the THD of the grid current is 0.29% and 1.25%, respectively, as shown in Table IV, achieving a good power quality. From the above tests, it has been verified that the proposed method is of cost-effectiveness for the dc injection suppression.

E. Case V

To further demonstrate the superior performance of the proposed method, an active software dc suppression solution called the virtual capacitor method [13] is tested to make a comparison. To avoid large voltage drops, the capacitance of the virtual capacitor is set as 2000 μF. Fig. 17 shows the experimental results of the grid current and the dc-link voltage with the virtual capacitor method under the same conditions of Case IV. As presented in Fig. 17, when the virtual capacitor strategy is activated at time t_3, the dc component of the grid current is reduced from 5.61% to 1.72% (see Table IV) with the dynamic time being 0.15 s. Although the dc component is reduced rapidly and significantly, it is still beyond the limitation, i.e., 0.5% in the IEEE Standard 1547-2018. Moreover, the dc component is 0.204 A (see Table IV) after the virtual capacitor strategy is activated, which is equal to the dc bias caused by the current measurement. In all, the experimental results have verified the analysis in Section I, since the dc bias induced by current sensors and sampling circuits is in the controller feedback channel, it is difficult to eliminate it by a current feedback control. As it has been quantitatively summarized in Table IV, with the proposed method, not only the injected dc current is significantly reduced but also the power quality of the grid current is increased. Hence, the proposed method can be a cost-effective solution to the dc current injection for single-phase inverters.

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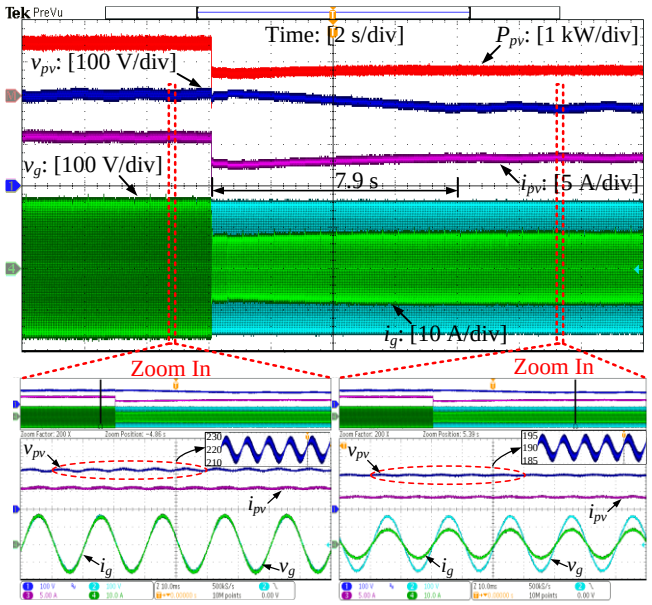

Fig. 18. Experimental results of the system with the proposed dc current injection suppression strategy in the case that the irradiance is suddenly changed from 1000 W/m^2 to 500 W/m^2.

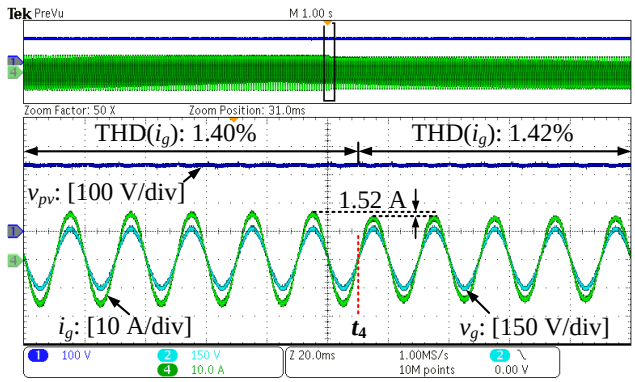

Fig. 19. Experimental results of the inverter in the case that the scaling error of the grid current measurement Δk_i is suddenly changed from 0 to 0.1.

F. Case VI

To show the dynamics and robustness of the system with the proposed dc current injection suppression strategy, the experiment in the case of solar irradiance step change from 1000 W/m^2 to 500 W/m^2 was tested. In this case, a perturb and observe (P&O) MPPT algorithm is employed with the updating time is 0.5 s and the step size is 4 V. Fig. 18 shows the experimental results. As it is observed in Fig. 18, despite the step change of irradiance, the system is still stable with the MPPT time is 7.9 s. In addition, when the irradiance changed from 1000 W/m^2 to 500 W/m^2, the dc component of grid current is slightly increased from 0.24% to 0.27% (see Table IV Case IV and VI), nevertheless, it is still below the standard limit (i.e., 0.5%). From this result, it can be concluded that the proposed dc current injection suppression strategy is effective and suitable for PV generation system.

G. Case VII

To show the impact of scaling error in grid current measurement on the grid current reference tracking and grid voltage disturbance suppression, the scaling error is set as 0.1 and only the current loop is adopted (the input of inverter is connected with a dc voltage source) in this case. Fig. 19 shows the experimental results of the inverter system, where the scaling error in grid current measurement Δk_i is suddenly changed from 0 to 0.1 at t_4. It can be observed that, although the scaling error of grid current is 0.1, the inverter system achieves a sinusoidal grid current and the THD of current is almost the same. However, after the step change in Δk_i, there exists a considerable steady-state error in grid current (approximately 1.52A). This is because, as analyzed in Section II-B, the scaling error in grid current measurement will lead to current tracking errors. Consequently, this result verified the correctness of theoretical analysis.

TABLE V
COMPARISONS OF THE PROPOSED METHOD WITH THE PRIOR-ART SCHEMES

Method (year)	Steady-state DC Component (mA)	Transient time (s)	Cost
[21] (2018)	2 mA	–	High
[19] (2018)	5 mA	60 s	Medium
[27] (2018)	30 mA	3 s	Low
[25] (2019)	109 mA, 31 mA and 78 mA (phase a, b, c)	0.03 s	Low
Proposed	22 mA	0.18 s	Low

H. Comparisons with Existing Solutions

To further show the performance of the proposed dc current suppression strategy, a detailed comparison is carried out among the proposed method and the prior-art dc component suppression schemes in terms of steady-state, dynamic performance and cost. The results are shown in Table V. As it can be observed in Table V, although the coupled inductor-based technique [21] achieved the lowest dc component, it is costly, since a coupled inductor combined with a high accuracy Hall effect current sensor were adopted to directly measure the dc component. To reduce the cost, alternative active hardware method was proposed in [19], where the dc component was detected by measuring the inverter output voltage and then mitigated through a compensation loop. Furthermore, according to Table V, although the method in [19] achieves a good steady-state performance, the dynamic performance is the worst. To further reduce the cost, the active software solutions were proposed in [25] and [27]. With the help of the neural network PID controller in the dc component compensation loop, the PID parameters can be adjusted adaptively and the shortest transient time is achieved in [25]. However, as aforementioned, since the dc component information is directly obtained from the grid current by using a sliding window double integration method, the dc bias caused in the current measurement cannot be eliminated by the current feedback control. The steady-state results shown in [25] confirmed this conclusion, where the dc component is 109 mA, 31 mA and 78 mA in phase a, b and c, respectively. The method in [27] achieves moderate steady-state and dynamic performance. Yet, it is also shown in Table V that the proposed strategy outperforms it both in steady-state and dynamic performance. As good dc current suppression performance and low cost are of importance in PV generation systems, the proposed method is very suitable for PV applications.

VI. Conclusion

The dc current injection in grid-connected inverters lead to transformer saturation and current distortions. To address the issues, this paper explored the root-causes of the dc current injection and its impact on grid-connected PV inverters. The exploration shows that the dc component caused by the grid voltage measurement errors and disturbances can be eliminated by increasing the current controller gain at the low frequency. A PIR controller was then employed to achieve a high gain in the low frequency band. A step-by-step controller parameters design, including the loop-gain, phase margin and bandwidth, was presented to realize the dc injection suppression with high control performance. To eliminate the dc current induced by grid current measurement errors, which cannot be suppressed by the current controller, a simple compensation method was proposed. The injected dc current was estimated by extracting the line-frequency voltage ripple on the dc-link voltage, and then, it was reduced by adding a dc component control loop. The detailed design guidelines of the proposed compensation method were described, and its dc injection rejection capability was evaluated and demonstrated experimentally. The various experimental cases and comparisons have verified the analysis and the efficacy of the proposed method.

Appendix I

According to [35], the simplified mode of PV modules is shown as

$$i_{pv} = I_{sc}[1 - C_1(e^{\frac{v_{pv}}{C_2 V_{oc}}} - 1)] \tag{A.1}$$

where

$$C_1 = (1 - \frac{I_{mpp}}{I_{sc}})e^{\frac{-V_{mpp}}{C_2 V_{oc}}}, \quad C_2 = (\frac{V_{mpp}}{V_{oc}} - 1)\ln[1 - \frac{I_{mpp}}{I_{sc}}]^{-1} \tag{A.2}$$

where i_{pv} and v_{pv} are the PV current and voltage, respectively. I_{sc} is short circuit current, V_{oc} is open circuit voltage, I_{mpp} and V_{mpp} are the current and voltage at the maximum power point (MPP), respectively. According to (A.1) and (A.2), the PV output power P_{pv} can be estimated as (A.3) under the standard test condition (i.e. 25 ℃, 1000 W/m^2).

$$P_{pv} = f(v_{pv}) = v_{pv} I_{sc}[1 - C_1(e^{\frac{v_{pv}}{C_2 V_{oc}}} - 1)] \tag{A.3}$$

TABLE VI
Parameters of PV Cells at the Standard Test Conditions

Parameters	Values	Parameters	Values
Short circuit current: I_{sc}	6.14 A	MPP current: I_{mpp}	5.45 A
Open circuit voltage: V_{oc}	282 V	MPP voltage: V_{mpp}	220 V

Based on the PV parameters shown in Table V and by taking the Taylor series of (A.3) at the MPP, we have

$$\begin{aligned} P_{pv} &= 1193 - 0.1674(v_{pv} - 220) - 0.1244(v_{pv} - 220)^2 \\ &\quad -0.0016(v_{pv} - 220)^3 + \cdots\cdots R_n(v_{pv}) \end{aligned} \tag{A.4}$$

where $R_n(v_{pv})$ is the remainder.

According to (A.4) and (17), it can be seen that, if there is no dc component in grid current, the dc-link voltage will not contain the line-frequency ripple, and then there will no line-frequency power oscillation in PV output power.

Appendix II

To obtain the steady-state gain from the dc injection I_{DC} to v_{2f}, a generalized state-space averaging (GSSA) method [36] which considers the average of state variables and harmonics is adopted. If the time-domain periodic variable meets the condition $\int_0^T |x(t)|^2 < \infty$, $x(t)$ can then be transformed in the period (t-T, t) by

$$x(t) = \sum_{k=-\infty}^{\infty} \langle x \rangle_k (t) e^{jk\omega t} \tag{A.5}$$

where $\omega = 2\pi/T$ is the fundamental angular frequency, and $\langle x \rangle_k(t)$ are the k-th Fourier coefficients that are defined by

$$\langle x \rangle_k (t) = \frac{1}{T}\int_{t-T}^{t} x(\tau) e^{-jk\omega t} d\tau \tag{A.6}$$

Eq. (A.5) and (A.6) lead to two fundamental properties of the GSSA, which is expressed as

$$\left\langle \frac{d}{dt} x \right\rangle_k (t) = \frac{d}{dt}\langle x \rangle_k (t) + jk\omega \langle x \rangle_k (t) \tag{A.7}$$

$$\langle xy \rangle_k = \sum_{i=-\infty}^{\infty} \langle x \rangle_{k-i} \langle y \rangle_i \tag{A.8}$$

According to (14), since only the fundamental frequency of ac variables is of interest, the generalized state-space averaging model is expressed as

$$\left\langle \frac{1}{2} C_{dc} \frac{dv_{pv}^2}{dt} \right\rangle_1 = \frac{1}{2} C_{dc} \left(\frac{d\langle v_{pv}^2 \rangle_1}{dt} + j\omega_0 \langle v_{pv}^2 \rangle_1 \right) = \langle v_{pv} i_{pv} \rangle_1 - \langle v_g i_g \rangle_1 \tag{A.9}$$

where

$$\begin{aligned} &\frac{d\langle v_{pv}^2 \rangle_1}{dt} = 0; \qquad \langle v_{pv} i_{pv} \rangle_1 = 0; \\ &\langle v_g i_g \rangle_1 = \langle v_g \rangle_0 \langle i_g \rangle_1 + \langle v_g \rangle_1 \langle i_g \rangle_0 = -j\frac{V_m}{2}\langle i_g \rangle_0 \end{aligned} \tag{A.10}$$

Thus, the steady-state gain from I_{DC} to v_{pv}^2 is derived as

$$\frac{\langle v_{pv}^2 \rangle_1}{\langle i_g \rangle_0} = \frac{V_m}{C_{dc}\omega_0} \tag{A.11}$$

Similarly, the steady-state gain from v_{pv}^2 to v_f, shown in Fig. 9, can be derived as

$$\langle v_f \rangle_1 = G_{BPF}(j\omega_0)\langle v_{pv}^2 \rangle_1 = \langle v_{pv}^2 \rangle_1 \tag{A.12}$$

From v_f to v_{2f}, we only focus on the steady-state gain from the fundamental frequency to dc component, thus, we have:

$$\begin{aligned} \langle v_{2f} \rangle_0 &= \langle v_f \cos(\omega_0 t) \rangle_0 \\ &= \langle v_f \rangle_0 \langle \cos(\omega_0 t) \rangle_0 + \langle v_f \rangle_1 \langle \cos(\omega_0 t) \rangle_{-1} = \frac{1}{2}\langle v_f \rangle_1 \end{aligned} \tag{A.13}$$

Consequently, according to (A.11)-(A.13), the steady-state gain from $\langle i_g \rangle_0$ i.e. I_{DC}, to $\langle v_{2f} \rangle_0$ is derived as

$$\frac{\langle v_{2f} \rangle_0}{\langle i_g \rangle_0} = \frac{V_m}{2C_{dc}\omega_0} \tag{A.14}$$

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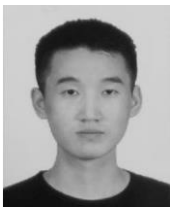

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