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Common-Ground-Type Single-Source High Step-Up Cascaded Multilevel Inverter for Transformerless PV Applications

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Abstract: Cascaded multilevel inverter (CMI) is one type of common inverters in industrial applications. This type of inverter can be synthesized either as a symmetric configuration with several identical H-bridge (HB) cells or as an asymmetric configuration with non-identical HB cells. In PV applications with the CMI, the PV modules can be used to replace the isolated dc sources; however, this brings inter-module leakage currents. To tackle the issue, the single-source CMI is preferred. Furthermore, in a grid-tied PV system, the main constraint is the capacitive leakage current. This problem can be addressed by providing a common ground, which is shared by PV modules and the ac grid. This paper thus proposes a topology that fulfills the mentioned requirements and thus it is a promising inverter in wide industrial area such as PV applications. The proposed CMI topology also features high boosting capability, fault current limiting, and transformerless configuration. To demonstrate the capabilities of this CMI, simulations and experimental results are provided.

Keywords: Cascaded multilevel inverter; Photovoltaic; Leakage current;

1. Introduction

Multilevel inverters (MIs) are attractive devices in many industrial applications. These devices can reduce the Total Harmonic Distortion (THD), Electromagnetic interference (EMI), dv/dt, switching frequency and voltage stress. One of the most regarded applications of MIs is PV application. The neutral point clamped converter (NPC) and CMI are two types of multilevel inverters, which are popular in PV applications [1-2]. Between the two topologies, the CMI stands out for its modularity and high magnitude of the output voltage. However, this topology requires several isolated dc sources. This drawback not only calls for a complex control system, but also it gives rise to inter module leakage currents in grid-tied PV applications. The inter-module leakage currents are resulted from differential-mode voltage (DMV) and common mode voltage CMV variations. In order to tackle the issue, several topologies are suggested in the literature [3-5]. One solution is using only one dc-source along with some passive components. Single-source CMIs are categorized into three types. *i)* Topologies which use low frequency transformers instead of several isolated dc sources. These topologies are referred to as cascaded transformers multilevel inverters (CTMIs) [6-9]. *ii)* Topologies which provide the isolated dc sources by adopting a high-frequency link and a single dc-source (HFLMI) [10, 11]. *iii)* Switched-capacitor (SC) based cascaded multilevel inverter (SC-CMI) [12-13]. The main advantage of CTMIs is their ability to provide galvanic isolation between the dc source and the load/grid. This is also the case when applying HFLMIs in PV

applications, where the leakage current issue is addressed. On the contrary, CTMIs need several bulky and inefficient transformers. Although the transformer size in HFLMIs is reduced due to the use of a high frequency link, many rectifiers are required to convert the isolated high frequency voltages to the desired dc voltages. Thus, the reliability decreases and the cost increase in this topology. Alternatively, SC-CMIs employ several capacitors instead of the isolated dc sources. Therefore, the SC-CMI topologies have a compact size and lower cost. However, these kinds of multilevel inverters lack galvanic isolation.

Moreover, many attempts have been made to use isolated PV arrays as the isolated dc sources in grid-tied CMIs [14]. However, as illustrated in [15], the main constraint of these configurations is the capacitive leakage currents between the HB cells and grid. Even using an interfacing transformer cannot address the mentioned problem, because inter-module leakage currents appear and circulate between the cascaded HB cells. In [15], the mentioned problem was addressed by equipping each HB cell with additional ac and dc side filters. Apart from limiting various leakage currents, these filters are deemed to eliminate the EMI; however, equipping each cell with several filters increases the volume and cost of the inverter. In [16], several level-double networks (LDN) are used as the auxiliary blocks to enhance the quality of the output voltage. This topology can also offer a common ground between the PV module and the grid, which results in the elimination of the leakage current. Although the suggested topology can eliminate the leakage current in PV applications, balancing of the capacitor voltage in the auxiliary cell is challenging. In another attempt, a two-stage inverter was suggested in [17], which can be regarded as a combination of the H5 and HERIC topologies. When the output voltage is higher than the grid voltage, the inverter operates in the H5 mode; when the dc link voltage decreases, the inverter is switched to the two-stage HERIC mode. This inverter can properly deal with voltage variation. However, it uses a complicated structure and control approach. Moreover a charge pump circuit was employed to eliminate the leakage in [18]. The topology is simple and compact, but it imposes a non-continuous current to the input side. Notably, in [19] a comprehensives study was conducted to investigate the state-of-the-art inverters for grid-tied PV applications.

In light of the above, a single-source asymmetric CMI is proposed in this paper, which provides a common ground for ac and dc sides. This topology uses capacitors instead of the isolated dc sources in the HB cells. Each capacitor is independently charged through a charging switch. Since there is a common ground for ac and dc sides, the common mode voltage is zero; hence, this topology can totally eliminate the leakage current in grid-tied PV applications. Another merit of the proposed topology is the capability to boost the input dc voltage; this is also an advantage in many applications such as grid-tied transformerless PV and fuel cell systems. In addition to the mentioned features, the three-phase configuration of the proposed topology draws a continuous input current, which makes it feasible in battery, un-interruptible power supply, and PV applications. The proposed topology can exchange reactive power with the load and the grid as well. Furthermore, it can smoothly charge the capacitors, facilitate the protection, and avoid bulky and expensive transformers in the grid-tied mode. As mentioned, the main issue of the conventional CMI in PV applications is the inter-module leakage currents. However, the proposed topology can address this problem properly and effectively. Compared to the transformer-based single-source multilevel inverters, the proposed topology is smaller in size, lower in cost, and higher in efficiency. Additionally, considering that the SC-based single-source MIs mostly suffer from inrush currents, the proposed topology is however, an inrush-current free CMI, being a promising converter in many industrial applications.

The rest of the paper is organized as follows: In section 2, the structure and operation principle of the proposed topology are illustrated. In Section 3, the proposed MI is compared with state-of-the-art MI topology. In section 4 the performance of the proposed topology in off-grid and grid-tied modes is investigated through simulations. Experimental tests are provided in Section 5, where a fifteen-level 0.55 kVA prototype is adopted to demonstrate the off-grid performance of the proposed topology. Moreover, a seven-level 1.5 kVA prototype is used to extract the grid-tied results. Finally, the overall work is concluded in Section 6.

2. Proposed Topology and Operation Principle

2.1. Conventional CMI in PV Systems

Many solutions are presented in the literature to improve the performance of the CMIs in PV systems. The main problem arises due to the parasitic capacitor in each HB cell that brings inter-module leakage currents [20-21]. These circulating currents cause power loss, EMI, and safety problems [15]. Figures 1(a) and (b) show a grid-tied PV system with a three-cell CMI, and equivalent circuit of the CMV, DMV and leakage currents, respectively.

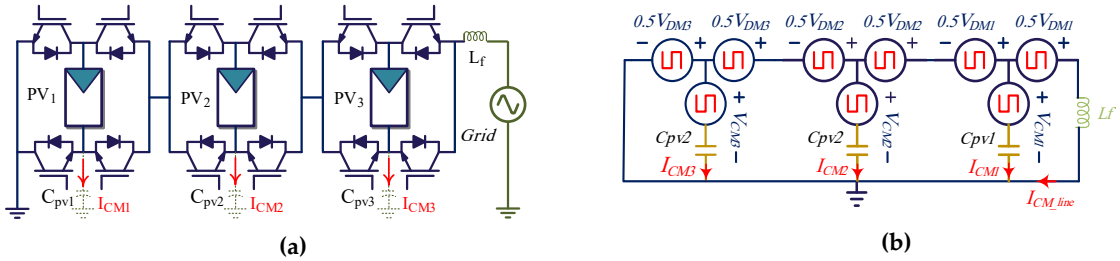


Figure. 1. Conventional CMI-based PV system: **(a)** a three-cell grid-tied CMI; **(b)** equivalent circuit to illustrate the CMV, DMV and inter-module currents.

2.2. General Structure of the Proposed Topology

The proposed topology is synthesized with two parts, namely the main and charging parts. The main part is the conventional asymmetric CMI, in which the isolated dc sources are replaced with capacitors (C_1, C_2, …, C_n). The charging part is composed of a single dc source (e.g. a PV string, fuel-cell, and batteries), a charging inductor, a freewheeling diode and charging switches (S_{c1}, S_{c2}, …, S_{cn}). The general grid-tied configuration of the proposed topology (a configuration with n HB cells) is depicted in figure 2. Where the main part is colored in black, the charging part is in blue.

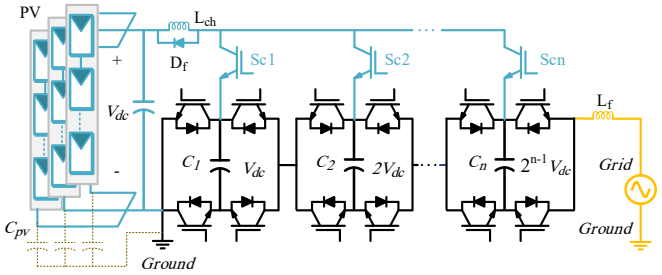


Figure. 2. General configuration of the proposed topology in grid-tied PV applications.

As mentioned, the most undesirable phenomenon in an SC-based converter is the inrush currents that emerge in the charging stage of the capacitors. This phenomenon can adversely affect the charging switches and capacitors. In order to limit these currents, a charging inductor (L_{ch}) is connected in series with the dc source, as shown in figure 2. This inductor can effectively limit the inrush currents. On the contrary, the mentioned inductor can cause voltage spikes and commutation problems in the charging switches. To avoid this and alleviate the EMI, the size of the charging inductor (L_{ch}) can be obtained as

$$L_{ch} = \frac{1}{(4\pi f)^2 C_n} \quad (1)$$

where f and C_n are the output voltage frequency and equivalent capacitance of the capacitors.

It should be noted that a larger inductor can be used to further reduce the inrush currents. However, it can increase the cost and volume of the inverter. A large inductor can also cause overvoltage across the capacitors. To avoid this, as shown in figure 2, a freewheeling diode (D_f) is connected in parallel with the inductor.

In order to illustrate the operation principle of the proposed topology, a fifteen-level configuration, which is depicted in figure 3, is exemplified. Table 1 shows the switching pattern for

each level and different states of the capacitors. It should be mentioned that in table 1, "on" and "off" states of the switches are indicated by "1" and "0". The capacitors in the proposed topology experience three states namely the charging, discharging, and floating states. In table 1, "C", "D", and "F" denote the charging, discharging, and floating states of the capacitors. In addition, since the upper switches of the main part (S_{11}, S_{31}, S_{12}, S_{32}, S_{13}, and S_{33}) have complementary states with the lower switches (S_{21}, S_{41}, S_{22}, S_{42}, S_{23}, *and* S_{43}), only the states of the upper switches are indicated in table 1 for simplicity.

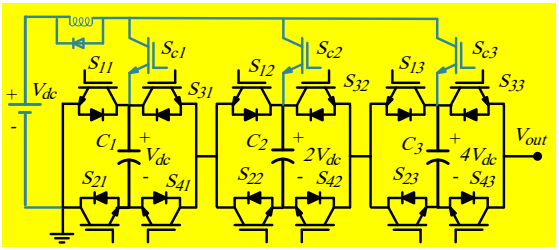


Figure. 3. A fifteen-level configuration of the proposed topology.

To clarify, the equivalent circuits of the voltage levels are provided. Due to the page limit, only the positive voltage levels are demonstrated in figure 4. The negative levels can be found referring to table 1. In figure 4, the charging paths, the capacitors under charge and the load current paths are in red, blue, and dark blue, respectively.

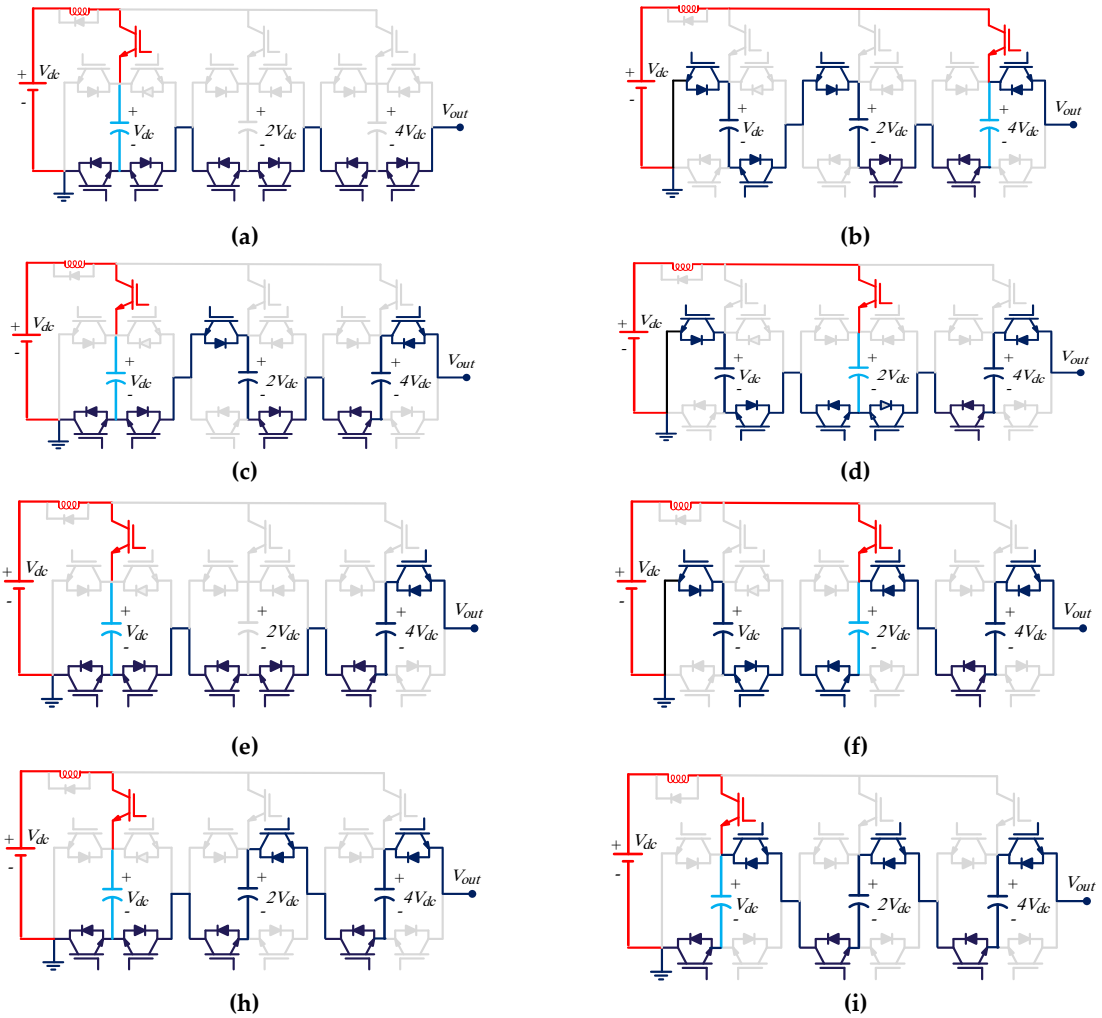


Figure. 4. Charging and load current paths: **(a)** to **(h)** zero to seventh voltage-levels of the topology in figure 3, respectively, where the PV module is replaced with a dc source for clarity.

Table. 1. Operation states of components shown in figure 6.

Levels	Main switches	Charging switches	Capacitors	V_{out}
	S_{11},S_{31},S_{12} S_{32} S_{13},S_{33}	S_{c1}, S_{c2}, S_{c2}	C_1,C_2,C_3	
7	010101	100	C,D,D	$7V_{dc}$
6	000101	100	C,D,D	$6V_{dc}$
5	100101	010	D,C,D	$5V_{dc}$
4	000001	100	C,D,D	$4V_{dc}$
3	100001	010	D,C,D	$3V_{dc}$
2	001001	100	C,D,D	$2V_{dc}$
1	101001	001	D,DC	$1V_{dc}$
0	000000	100	C,F,F	0
-1	100000	010	D,C,D	$-1V_{dc}$
-2	001000	100	C,D,D	$-2V_{dc}$
-3	101000	001	D,D,C	$-3V_{dc}$
-4	000010	100	C,F,D	$-4V_{dc}$
-5	100010	010	D,C,D	$-5V_{dc}$
-6	001010	100	C,D,D	$-6V_{dc}$
-7	101010	000	D,D,D	$-7V_{dc}$

2.3. *Three-Phase Configuration*

Continuity of the input current in many applications is of high importance. A continuous input current can facilitate the maximum power point tracking (MPPT) process in PV applications and prolong battery life span in storage systems. Referring to table 1, it can be seen that a single-phase configuration of the proposed topology cannot guarantee a continuous input current because there is no possibility to connect the dc source to any of the capacitors when realizing the highest negative voltage level (this is the case for a configuration with any number of voltage-levels). Since the input current is only interrupted in the highest negative voltage level, which is a short interval, this problem will not exist in a three-phase configuration. In such a configuration, when the input current is interrupted in one phase, there are always two paths in the other two phases for the current to flow. Figure 5 depicts the general three-phase configuration of the proposed topology. It is worth mentioning that in the three-phase configuration, the CMV is reduced but not totally eliminated. Thus in a grid-tied PV application with the three-phase configuration, a limited leakage current is achieved. However, the inter-module leakage currents are totally cancelled out in this configuration.

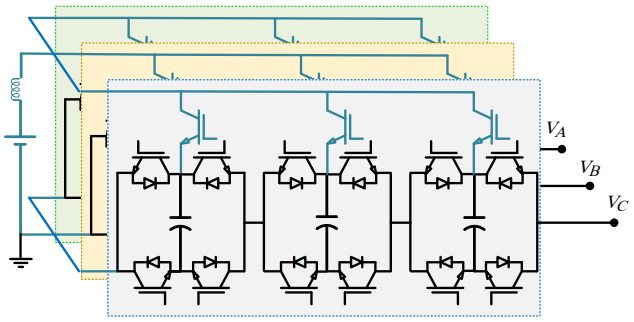


Figure 5. General three-phase configuration of the proposed topology.

2.4. *Component design*

Referring to figure 4 and table 1, it is seen that during one cycle, the lower the dc voltage an HB cell contains, the longer time it resides in the charging mode. For example, as shown in table 1, the

first HB cell, which contains 1 pu voltage, resides in the charging mode for eight times. The number of being in the charging mode for the second and third HB cells is four and two, respectively. Thus, in an *l*-level structure, the number of being in the charging state for the n^{th} HB cell is calculated as

$$Nch_n = 2^{\frac{\ln(l+1)}{ln2}-n} \quad (2)$$

In respect to this, an HB cell with a higher dc voltage will provides the load current for a longer time than others. Therefore, it experiences the highest voltage ripple. The highest voltage ripple of the n^{th} HB cell (Δv_n) is given as

$$\begin{cases} \Delta v_n = \frac{I_m \Delta t_n}{C_n} \\ \Delta t_n = T(l - Nch_n) \end{cases} \quad (3)$$

where I_m, T, and C_n are the maximum value of the load current, time duration of a cycle, and capacitance of the n^{th} capacitor, respectively. This equation can be used to select a proper capacitor for the n^{th} HB cell.

Considering Fig. 2, the equivalent circuit of the capacitor experiencing the highest voltage ripple (C_n) is shown in Fig. 6. Taking the parameters indicated in Fig. 6 into account, the instantaneous voltage in the n^{th} capacitor and the voltage of the mentioned capacitor at the end of a half cycle are, respectively given as

$$v_{c_n}(t) = (2^{n-1})v_{dc}{}^{\frac{-t}{RC_n}} \quad (4)$$

$$v_{c_n}(T_d) = (2^{n-1})v_{dc}{}^{\frac{-T_d}{RC_n}} \quad (5)$$

The maximum voltage ripple in the n^{th} capacitor can be given as

$$\Delta v_{c_n} = fT_d\left((2^{n-1})v_{dc} - v_{c_n}(T_d)\right) = fT_d(2^{n-1})v_{dc}(1 - e^{\frac{-T_d}{RC_n}}) \quad (6)$$

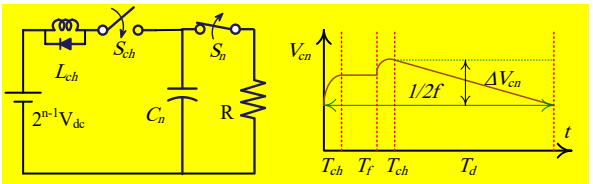


Fig. 6. Equivalent circuit and discharging diagram of a capacitor in an HB cell.

As it is an asymmetric topology, the HB cells in the proposed topology include different dc voltage values. Considering v_{dc} as the input voltage, the voltage across the n^{th} cell is given as

$$V_{c_n} = 2^{n-1}v_{dc} \quad (7)$$

The voltage stress on the main and charging switches in the n^{th} HB cell is equal to the voltage of capacitor in that HB cell.

The peak output voltage of an n-cell configuration is given as

$$v_m = v_{dc}\sum_{k=1}^{n} 2^{k-1} \quad (8)$$

The number of switches of an *l*-level configuration of the proposed and conventional asymmetric CMI topologies is, respectively, indicated as

$$N_{sw}^{P}\ \frac{5\ln(\frac{l+1}{2})}{ln2} \quad (9)$$

$$N_{sw}^{C}\ \frac{4\ln(\frac{l+1}{2})}{ln2} \quad (10)$$

This implies that the proposed topology requires one extra switch in each cell (one charging switch for each cell).

The total voltage stresses of the switches in the proposed and the conventional asymmetric CMI topologies are, respectively, indicated as

$$TVS_p = \frac{5v_{dc}}{N_{sw}^{P}}\sum_{k=1}^{N_{sw}^{p}/5} 2^{k-1} \quad (11)$$

$$TVS_c = \frac{4v_{dc}}{N_{sw}^{C}}\sum_{k=1}^{N_{sw}^{c}/4} 2^{k-1} \quad (12)$$

Implying that the voltage stresses of the switches in both topologies are the same.

3. Benchmarking With Prior-Art Inverters

Several efforts have been done to make the CMI compatible with grid-tied PV applications. The main difficulties with the CMI in PV applications are the leakage current and complicated MPPT [14]. Single-source CMIs facilitate the MPPT, but the leakage current problem remains. A transformer can solve the problem, however, transformers are not recommended in grid-tied PV applications due to extra power losses and additional costs. Therefore, as stated previously the SC-based CMI can fulfill many requirements. The state-of-the-art PV MI topologies are compared with the proposed MI topology in this section to assess its pros and cons. Table 2 lists the main features of the considered MI topologies.

In table, N_{sw}, N_d, N_c, G, *and* TSV are the number of switches, diodes, capacitors, voltage gain, and the total voltage standing of the switches. The TSV is calculated as

$$TSV = \frac{\sum_{n=0}^{n=k} V_{sw_n} + \sum_{n=0}^{n=k} V_{sd_n}}{V_{out}} \quad (12)$$

Table 2. Comparison

Topology	Nsw	Nd	Nc	G	TSV	Coupled inductor	Leakage current limiting
[22]	14	0	2	3	4.67	no	no
[23]	12	-	2	2	5.5	no	no
[24]	10	-	2	0.5	8	yes	yes
[25]	8	3	3	4	5.75	no	no
[26]	12	-	3	4	5.25	no	no
[27]	9	-	2	2	5.5	no	no
[28]	11	-	3	2	5	no	no
[29]	8	4	4	2	6	no	no
[Proposed]	10	0	2	3	5	no	yes

The proposed topology and the topology in [29] can be scaled up to obtain higher voltage gains and levels. However, this is not the case for the other topologies. Since the proposed MI topology is common-ground-type inverter and the topology in [24] is a mid-point-grounded topology, these two topologies can limit the leakage current in grid-tied PV applications. In this regard, the other topologies listed in table 2 encounter serious problems. The main disadvantage of the MI topologies in [24] and [25] is that they require a complicated control approach to balance the voltages across the capacitors. The voltage balancing system of these topologies should sense the direction of the ac current and the capacitor voltage magnitude, and then the sensed values are processed though the processor to execute the right switching pattern to balance the voltage of the capacitors. However, this does not happen in the other topologies and the proposed one. Notably, the topology in [23], [25], [27] and [28] suffer from high inrush currents in the charging stage of the capacitor. Owing to the controlled voltage balancing of the capacitors, the inrush current does not appear in [31] and [33] topology. In the proposed topology and the topology in [29], the inrush current is limited through the charging inductor. As it is seen in table 2, the proposed inverter has fairly low TSV, high voltage gain and fewer components.

4. Simulation Results

In order to verify the performance of the proposed topology, both the single-phase and three-phase configurations are simulated under Mathlab/Simulink. The main parts in the considered configurations are assumed to be a fifteen-level CMI. The simulated models are tested under off-grid

and grid-tied modes. In the off-grid mode, a general dc source supplies the load through the proposed topology.

4.1. Off-grid mode

As illustrated earlier, the three-phase and single-phase configurations only differ in the input current shapes. For this reason, mostly the single-phase configuration is investigated. Table 3 shows the characteristics of the utilized components in the off-grid mode. Figure 7(a) shows the output and capacitor voltages under no-load condition. A Fast Fourier Transform (FFT) analysis of the output voltage is depicted in figure 7(b).

Table 3. Components of the Off-grid Model.

Component	Value	Component	Value
V_{dc}	46 V	$L_{ch}(3\phi)$	0.5 mH
Power rating	550 W	C_1, C_2, C_3	3300 μF
$L_{ch}(\phi)$	1.8 mH	f_{sw}	5 kHz
Reference voltage		220 V (RMS), 50 Hz	

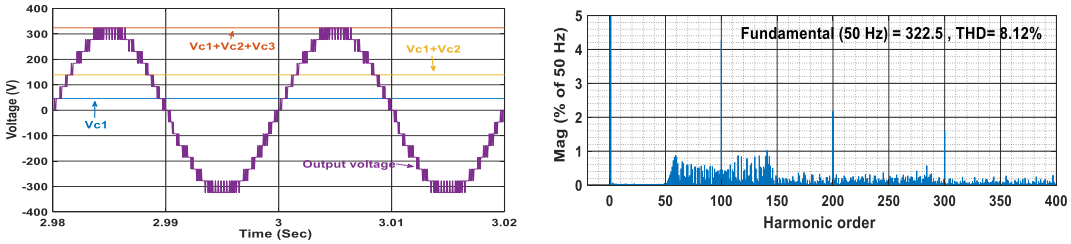


Figure 7. Simulation results of the single-phase configuration in the off-grid mode (no-load condition): **(a)** capacitor and output voltages; **(b)** FFT analysis of the output voltage

Furthermore, the output voltage, load current, and capacitor voltages, when supplying a purely resistive load of 0.55 kW, are shown in figure 8(a). As seen in figure 8(a), under this condition, the voltage across the capacitors is properly balanced through the charging circuit. Additionally, the capacitor currents along with the input current under the studied loading condition are shown in figure 8(b). It can be seen that the charging unit can properly limit the inrush current of the capacitors. However, the main demerit of the charging process is the discontinuity of the input current due to the absence of a path for the input current when developing the highest negative voltage level.

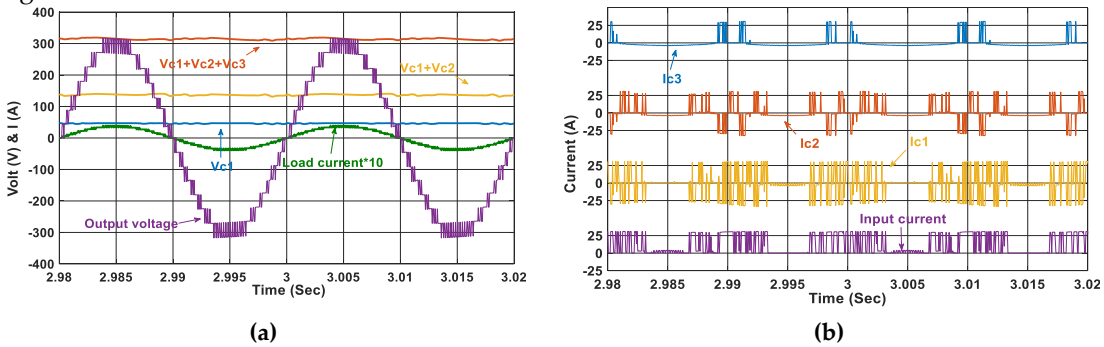
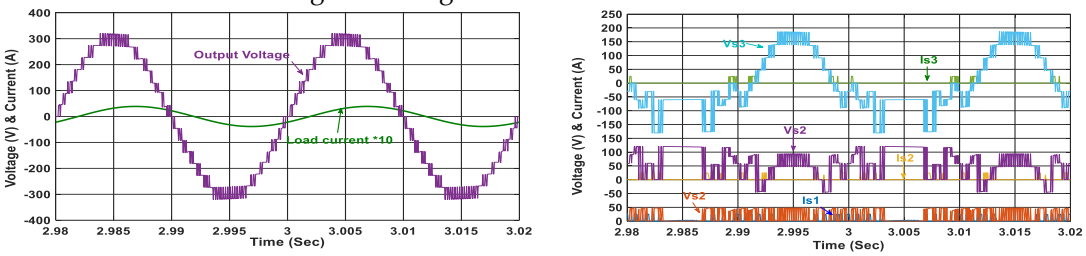


Figure 8. Simulation results of the single-phase configuration in the off-grid mode (under a purely resistive loading condition): **(a)** load current along with the capacitor and output voltages; **(b)** capacitor and input currents.

In order to demonstrate the ability of the proposed topology to provide reactive power, a resistive-inductive load of 0.5 kW+0.35 kVar is connected. Figure 9(a) shows the output voltage and load current under the mentioned condition. As shown in figure 9(a), the proposed topology can satisfactorily supply the reactive power. Additionally, the voltage stress and current of the charging

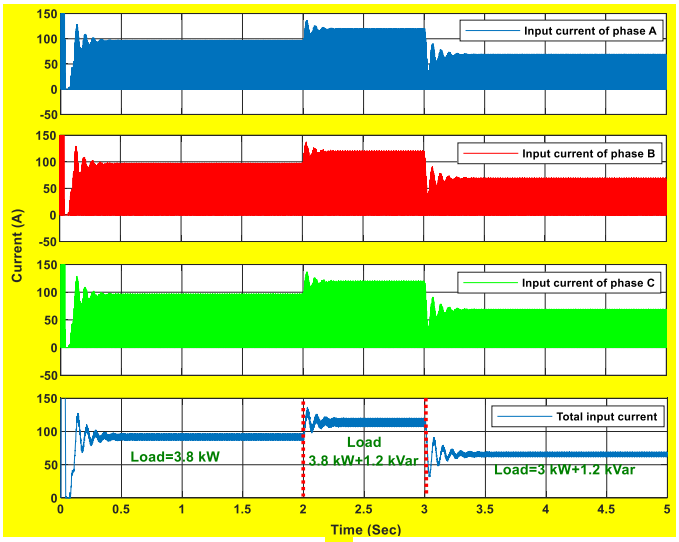
switches are shown in figure 9(b). According to figure 9(b), it is known that the charging switch in the last cells can tolerate the highest voltage stress.



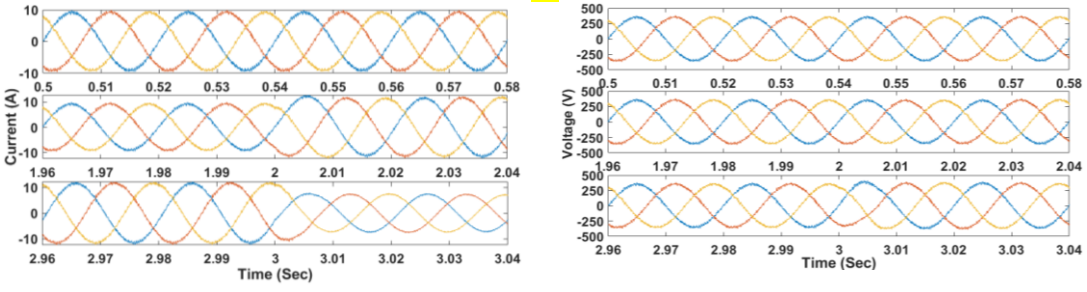
(a) **(b)**

Figure 9. Simulation results of the single-phase configuration in the off-grid mode (under a resistive-inductive loading condition): **(a)** load current and output voltage; **(b)** voltage stress and current of the charging switches.

As mentioned previously, a three-phase configuration of the proposed topology draws a continuous current from the input side. This is proven by considering a three-phase fifteen-level configuration, which supplies a balanced three-phase load under three loading cases (3.8 kW, 4.8 kW+1.2 kVar, 3 kW+1.2 kVar). The input current of the phases and the total input current under the mentioned loading condition are shown in figure 10(a). As it is seen in figure 10(a), the input current is a continuous current. Moreover, the output voltages together with the load current under the mentioned condition are shown in figure 10(b) and (c), respectively. When the freewheeling diode is removed, the capacitors are exposed to overvoltage at the initial instance. Soft starting strategies can be employed to avoid the overvoltage of the capacitors.



(a)



(b) **(c)**

Figure 10. Simulation results of the three-phase configuration in the off-grid mode: **(a)** input current of the phase and total input current; **(b)** load current; **(c)** output voltage.

5. *Grid-tied mode*

Similar to the off-grid mode, a fifteen-level configuration of the proposed topology is used to deliver the desired powers to the grid. To this end, the ac components are transferred to the dq0 frame and two proportional-integral (PI) controllers are employed to control the active and reactive powers. Table 4 shows the characteristics of the considered system.

Table 4. component of the grid-connected model

Ki	42.3	Grid-side filter	2.8 mH + 30 mΩ
Kp	700	f_{sw}	5 kHz
$V_{g_{max}}$	320 V	L_{ch}	1.8 mH
f	50 Hz	C_1, C_2, C_3	3300 µF

The simulation results of the single-phase grid-connected model are shown in figure 11. The desired (reference) and delivered active power to the grid is shown in figure 11(a). The reference of the active power can be obtained by the MPPT system in PV applications. The reference and developed reactive powers are exhibited in figure 11(b). As shown in figure 11(b), the proposed topology has succeeded to provide a bidirectional reactive power flow. The input current is depicted in figure 11(c). The output voltage of the inverter along with the injected current is exhibited in figure 11(d).

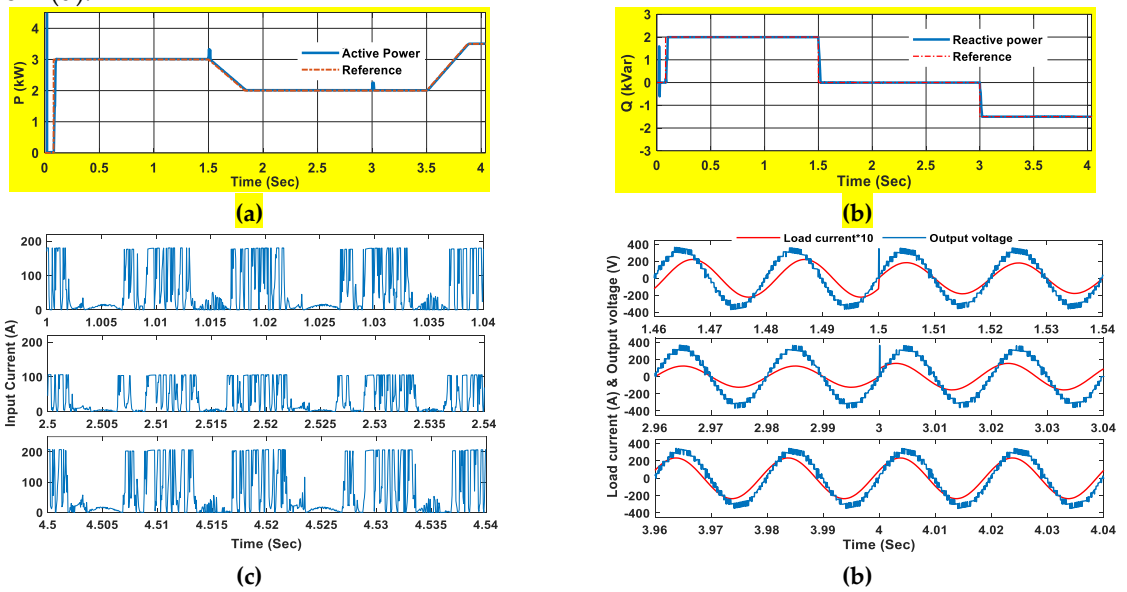


Figure 11. Simulation results of the single-phase grid-connected model: **(a)** the developed and reference of the active power; **(b)** the developed and reference of the active power; **(c)** input current; **(d)** output voltage and load current.

It should be pointed out that one of the significant features of the proposed MI topology is its ability to eliminate the leakage current in grid-tied PV systems without using any additional components.

Furthermore, the simulation results of a grid-connected three-phase model are demonstrated in figure 12. The injected active and reactive powers to the grid are depicted in figures 12(a) and (b). As it is seen in figure 12, the proposed MI has deservedly developed the desired powers.

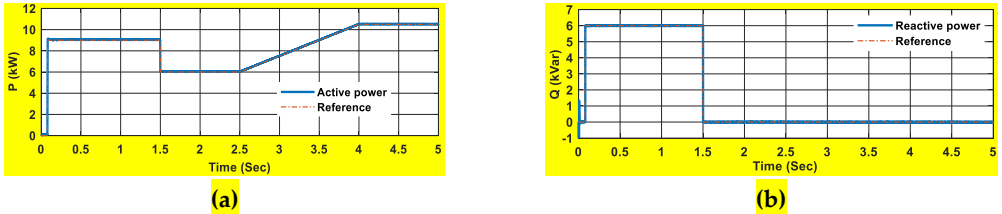


Figure 12. Simulation results of the active and reactive power of the three-phase grid-connected model: **(a)** the injected active power to the grid; **(b)** the injected reactive power to the grid.

As discussed previously the three-phase configuration of the proposed topology draws a continuous current from the dc-link. Figure 13(a) shows the input current and proves this. In order to investigate the leakage current, a parasitic capacitor of 200 *nF* is considered between the negative pole of the dc-side and ac-ground, figure 13(b) shows the leakage current. As shown in figure 13(b), the RMS value of the leakage current is in the acceptable range. However, it is possible to reduce it through a proper control and/or switching approaches. It is worth mentioning that since the proposed topology does not use PV modules inside the H-bridge cells, there are no inter-module leakage currents.

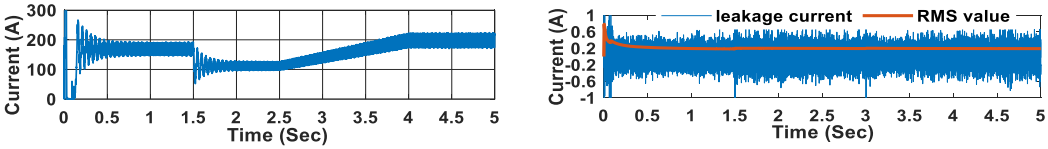


Figure 13. Simulation results of input and leakage current of the three-phase grid-connected model: **(a)** input current; **(b)** leakage current.

Furthermore the output voltage and the injected current are shown in figure 14. It is to be noted that this paper is not aimed at designing a proper control system. It is possible to obtain a more accurate result through a precise control approach.

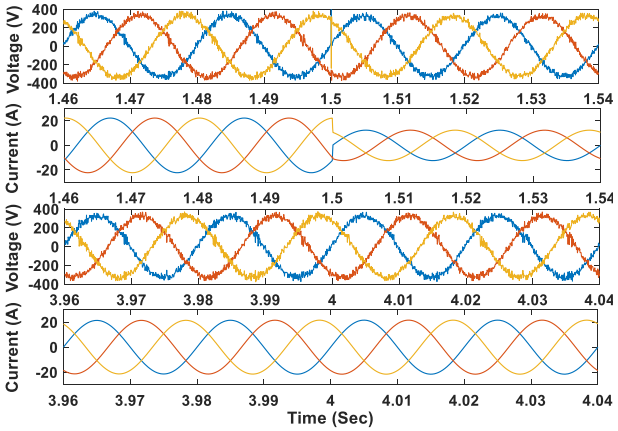


Figure 14. Simulation results of the output voltage and injected current of the three-phase grid-connected model.

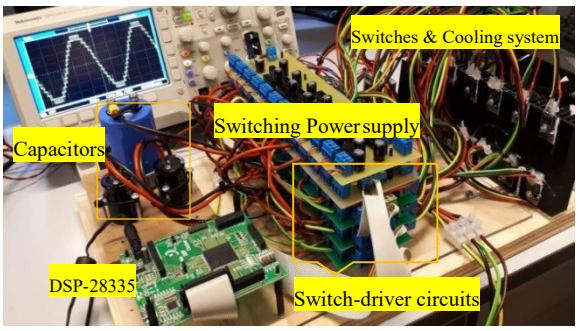
5. Experimental Results

5.1. Off-gird Results

In order to validate the feasibility of the proposed topology, a laboratory-scale prototype is tested. Figure 15 depicts the employed prototype and table 5 lists the utilized components. It should be noted that the level-shifted SPWM strategy is adopted to compute the switching signals.

Table 5. Electrical Parameters and Component Specifications

Component	Specification	Electrical parameter	Value
Main Switches	IRFP350	Resistive load	550 W
Charging switches	IRFP460	RL load	650 VA
Opto-coupler	TLP250	V_{out}(RMS)	220 v, 50 Hz
Capacitors	3300 µF	V_{dc}	47 V
L_{ch}	2.8 mH	f_{sw}	5 kHz
Diodes	FFPF20UP40S	# of HB cells	3 (15-level)



296

297 **Figure 15.** Experimental setup of the proposed topology (15-level).

298 Figure 16 exhibits the output voltage under the no-load condition and the FFT analysis of the
299 voltage. As it is seen, the harmonics around the fundamental frequency have negligible magnitude,
300 while the harmonics around the multiples of the switching frequency are of high amplitude. Since
301 these harmonics are far away from the fundamental frequency, they can easily be eliminated using
302 small filters.

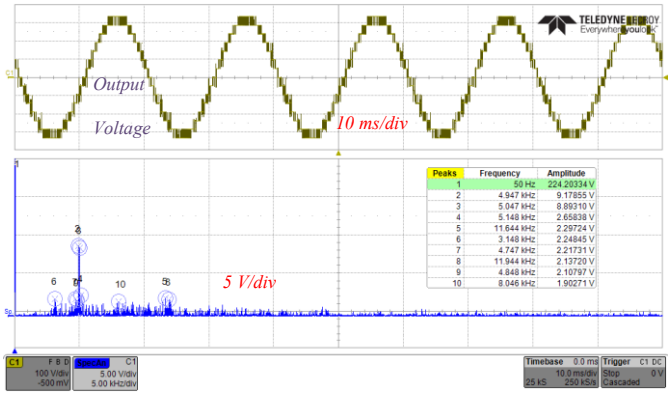
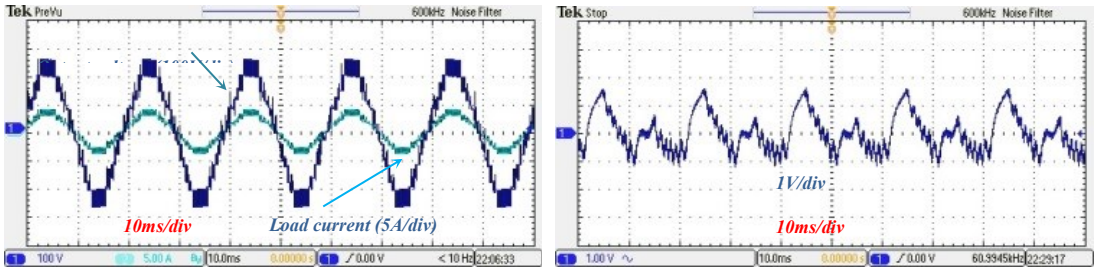


Figure 16. Measured output voltage of the proposed single-phase configuration (15-level) under no-load condition and its FFT analysis.

303 The output voltage along with the load current, when the prototype supplies a purely resistive
304 load of 550 W is shown in figure 17(a). In order to assess the voltage ripple of the capacitors, the ac
305 components of the capacitor voltages are shown in figures 17(b), (c) and (d). Additionally, the
306 charging current of the capacitor under 550 W load is shown in figure 17(e). As it is seen, there is no
307 sharp spike on the charging current of the capacitors, which implies that the charging inductor
308 smoothen the charging currents.



(a) **(b)**

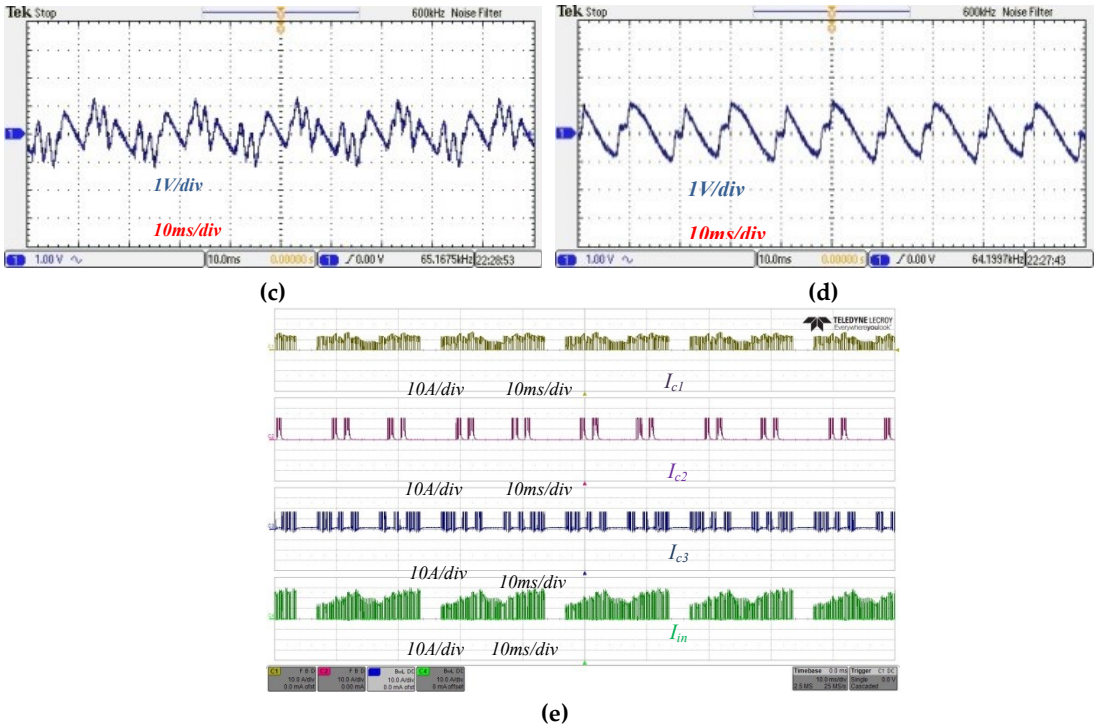


Figure 17. Experimental results under a purely resistive loading condition: **(a)** output voltage and load current under the purely resistive loading condition; **(b)**, **(c)**, and **(d)** ac components of the capacitor voltages; **(e)** input current and charging current of the capacitors.

In order to prove the capability of the proposed topology to provide reactive power, a resistive-inductive load of 500 W+350 Var is then considered. Figure 18 exhibits the output voltage and load current under this condition. As it can be seen, the proposed topology can supply the reactive power without any constraints.

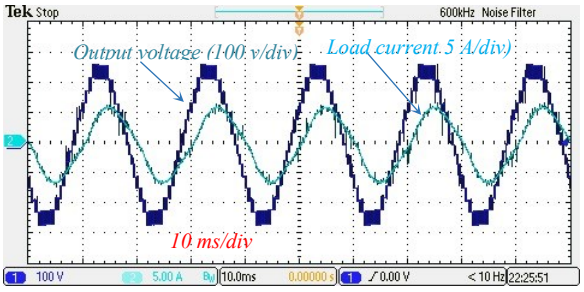


Figure 18. Output voltage and load current under the inductive-resistive loading condition.

5.2. Grid-tied results

In order to extract the grid-tied results a seven-level prototype with two cells is employed. The characteristic of the prototype and grid is listed in table 7. In this test the sample based current control is used to inject the desired active and reactive powers to the grid.

Table 7. Component Of The Grid-Connected Model.

Main Switches	FQA14N30	Grid-side filter	1.73 mH
Charging switches	STP30NM30N	Switching frequency (f_{sw})	22 kHz
RMS grid voltage	220 V	L_{ch}	1.6 mH
Grid frequency (f)	50 Hz	C_1, C_2,	3300 µF

Three scenarios are considered in grid-tied test. In the first scenario a pure active power of 1.5 kW is injected to the grid. The injected current and grid voltage under this condition are shown in

figure 19(a). The FFT analysis of the injected current under the mentioned condition is shown in figure 19(b). Furthermore, the output voltage of the inverter along with the provided current is shown in figure 19(c).

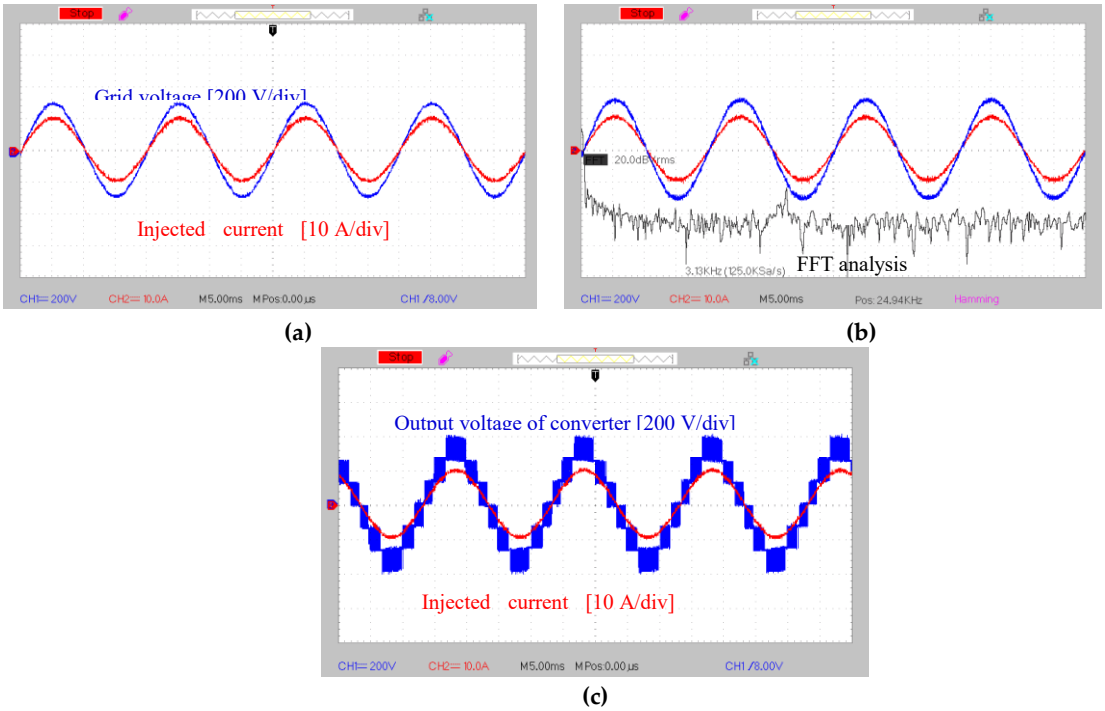


Figure 19. Grid-tied results of the active power: **(a)** grid voltage and injected current; **(b)** FFT analysis of the injected current; **(c)** output voltage and current of the prototype.

In the second scenario the active power of 1.2 kW and reactive power of 0.9 kVar is injected to the grid and in the third scenario the active power of 1.2 kW is injected to the grid and reactive power of 0.9 kVar absorbed from the grid. The grid voltage together with the injected current to the grid is shown in figure 20(a) and (b).

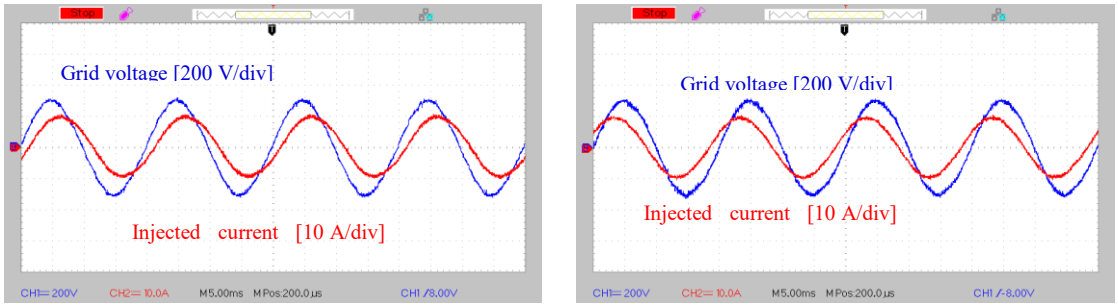


Figure 20. Grid-tied results of the injected current: **(a)** the output voltage and load current when injecting the active and reactive current to the grid; **(b)** grid-voltage and injected current when injecting the active power and absorbing the reactive power.

The seven-level prototype for grid-tied application is exhibited in figure 21.

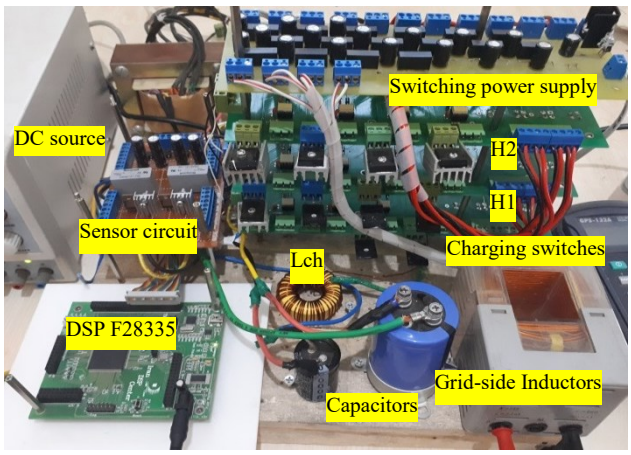


Figure 21. Seven-level setup for grid-tied application.

6. Conclusion

In this paper, a single-source high step-up asymmetric power converter topology was proposed. The proposed topology offers several advantages in many industrial applications such as PV, fuel cell and etc. It is synthesized with two parts, namely the main and charging parts. The main part is the same as the conventional asymmetric CMI with certain capacitors instead of the isolated dc sources. The charging part, however, consists of charging switches, a charging inductor, a freewheeling diode, and one dc source. The main feature of the proposed topology is to provide a common-ground for ac and dc sides, which eliminates the leakage current in grid-tied PV applications. It also has the ability to boost the input voltage. Thus, in the grid-tied PV applications, bulky and expensive transformers can be avoided. Moreover, it uses only one dc source, at the expense of using many switches, employing many switches can be count as the main demerit of the proposed inverter. Simulations and experiments were performed to verify the effectiveness of the proposed topology. Through simulations, the performances of the suggested topology with single- and three-phase configuration in both off-grid and grid-tied conditions were assessed. In the experimental tests, the performance of the proposed topology was studied in the presence of a 550-VA load. Moreover, using a 1.5 kVA seven-level prototype the grid-tied results were provided. Both results have demonstrated the feasibility of the proposed multilevel inverter in terms of the ability to develop a boosted voltage of high quality using only one dc source.

References

[1] F. Wu; X. Li; F. Feng; and H. B. Gooi. Modified cascaded multilevel grid-connected inverter to enhance European efficiency and several extended topologies, *IEEE Trans. Ind. Inform.,* Dec. 2015, vol. 11, no. 6, pp. 1358 – 1365.

[2] H. Sepahvand; J. Liao; M. Ferdowsi; and K. A. Corzine. Capacitor voltage regulation in single-DC-source cascaded H-bridge multilevel converters using phase-shift modulation, *IEEE Trans. Ind. Electron.*, Sept. 2013, vol. 60, no. 9, pp. 3619 – 3626.

[3] M. R. Banaei; H. Khoun Jahan; and E. Salary. Single-source cascaded transformers multilevel inverter with reduced number of switches, *IET Power Electron.,* Nov. 2012, vol. 5, no. 9, pp. 1748 – 1753.

[4] S. Vazquez; J. I. Leon; L. G. Franquelo; J. J. Padilla; and J. M. Carrasco. DC-voltage-ratio control strategy for multilevel cascaded converters fed with a single DC source, *IEEE Trans. Ind. Electron.,* Jul. 2009, vol. 56, no. 7, pp. 2513 – 2521.

[5] A. Taghvaie; J. Adabi; and M. Rezanejad. A multilevel inverter structure based on a combination of switched-capacitors and DC sources, *IEEE Trans. Ind. Inform.,* Oct. 2017, vol. 13, no. 5, pp. 2162 – 2171.

[6] H. Khoun Jahan; K. Zare; and M. Abapour; Verification of a low components nine-level cascaded-transformer multilevel inverter in grid- tied mode, *IEEE J. Emerg. Sele.Topi. Power Electron.*, 2018, vol. 6, no. 1, pp. 429-440,

[7] S. G. Song; F. Soon Kang; and S. J. Park. Cascaded multilevel inverter employing three-phase transformers and single DC input, *IEEE Trans. Ind. Electron.,* Jun. 2009, vol. 56, no. 6, pp. 2005 – 2014.

[8] H. Khoun Jahan; M. Naseri, M. M. Haji-Esmaeili; M. Abapour, and K. Zare. Low component merged cells cascaded-transformer multilevel inverter featuring an enhanced reliability, *IET Power Electron.*, Jun. 2017, vol. 10, no. 8, pp. 855 – 862.

[9] A. K. Panda; and Y. Suresh. Performance of cascaded multilevel inverter by employing single and three-phase transformers, *IET Power Electron.*, Nov. 2012, vol. 5, no. 9, pp. 1694 – 1705,

[10] J. Pereda; and J. Dixon. High-frequency link: A solution for using only one dc source in asymmetric cascaded multilevel inverters, *IEEE Trans. Ind. Electron.*, Sep. 2011, vol. 58, no. 9, pp. 3884 – 3892.

[11] L. Wang; D. Zhang; Y. Wang; B. Wu; and H. S. Athab. Power and voltage balance control of a novel three-phase solid-state transformer using multilevel cascaded H-bridge inverters for microgrid applications, *IEEE Trans. Power Electron.*, Apr. 2016, vol. 31, no. 4, pp. 3289 – 3301.

[12] R. Barzegarkhoo; H. M. Kojabadi; E. Zamiry; N. Vosough; and L. Chang. Generalized structure for a single phase switched-capacitor multilevel inverter using a new multiple DC link producer with reduced number of switches, *IEEE Trans. Power Electron.*, Aug. 2016, vol. 31, no. 8, pp. 5604 – 5617.

[13] Z. Du, B. Ozpineci; L. M. Tolbert; and J. N. Chiasson. DC–AC Cascaded H-bridge multilevel boost inverter with no inductors for electric/hybrid electric vehicle applications, *IEEE Trans. Ind. Appl.*, May 2009, vol. 45, no. 3, pp. 963 – 970.

[14] E. Villanueva; P. Correa, J. Rodriguez; and M. Pacas. Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems, *IEEE Trans. Ind. Electron.*, Nov. 2009, vol. 56, no. 11, pp. 4399 – 4406.

[15] Y. Zhou; and H. Li. Analysis and suppression of leakage current in cascaded-multilevel-inverter-based PV systems, *IEEE Trans. Power Electron.*, Oct. 2014, vol. 29, no. 10, pp. 5265 – 5277.

[16] A. Kadam; and A. Shukla. A multilevel transformerless inverter employing ground connection between PV negative terminal and grid neutral point, *IEEE Trans. Ind. Electron.*, Nov. 2017, vol. 64, no. 11, pp. 8897 – 8907.

[17] Y. P. Siwakoti; F. Blaabjerg. A single-phase transformerless inverter with charge pump circuit concept for grid-tied PV applications, *IEEE Trans. Ind. Electron.*, Mar. 2018, vol. 65, no. 3, pp. 2100 – 2111.

[18] A. Anurag; N. Deshmukh; A. Maguluri; and S. Anand. Integrated DC–DC Converter Based Grid-Connected Transformerless Photovoltaic Inverter With Extended Input Voltage Range, *IEEE Trans. Power Electron.*, Oct. 2018, vol. 33, no. 10, pp. 8322 – 8330.

[19] M. N. H Khan; Mo. Forouzesh; Y. P Siwakoti; L. Li; T. Kerekes; and F. Blaabjerg. Transformerless Inverter Topologies for Single-Phase Photovoltaic Systems: A Comparative Review, *IEEE J. Emerg. Sele.Topi. Power Electron.*, Apr. 2019, vol. 65, no. 2, pp.805 - 835,

[20] V. V. S. Pradeep Kumar; and B. G. Fernandes. Minimization of inter-module leakage current in cascaded H-bridge multilevel inverters for grid connected solar PV applications, *in Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2016, pp. 2673-2678,

[21] F. Wang; Z. Li; H. T. Do; and D. Zhang. A modified phase disposition pulse width modulation to suppress the leakage current for the transformerless cascaded H-bridge inverters, *IEEE Trans. Ind. Electron.*, Feb. 2018, vol. 65, no. 2, pp. 1281–1289,

[22] X. Sun; B. Wang; Y. Zhou; W. Wang; H. Du; Z. Lu. A Single DC Source Cascaded Seven-Level Inverter Integrating Switched-Capacitor Techniques, *IEEE Trans. Ind. Electron.*, Nov. 2016, vol. 63, no. 11, pp. 7184 - 7194,

[23] S. S. Lee, "Single-Stage Switched-Capacitor Module (S3CM) Topology for Cascaded Multilevel Inverter," in IEEE Transactions on Power Electronics, vol. 33, no. 10, pp. 8204-8207, Oct. 2018, doi: 10.1109/TPEL.2018.2805685.

[24] C. Phanikumar, J. Roy and V. Agarwal, "A Hybrid Nine-Level, 1-φ Grid Connected Multilevel Inverter With Low Switch Count and Innovative Voltage Regulation Techniques Across Auxiliary Capacitor," in IEEE Transactions on Power Electronics, vol. 34, no. 3, pp. 2159-2170, March 2019, doi: 10.1109/TPEL.2018.2846628.

[25] J. Liu, W. Lin, J. Wu and J. Zeng, "A Novel Nine-Level Quadruple Boost Inverter With Inductive-Load Ability," in IEEE Transactions on Power Electronics, vol. 34, no. 5, pp. 4014-4018, May 2019, doi: 10.1109/TPEL.2018.2873188.

[26] N. Sandeep and U. R. Yaragatti, "Operation and Control of an Improved Hybrid Nine-Level Inverter," in IEEE Transactions on Industry Applications, vol. 53, no. 6, pp. 5676-5686, Nov.-Dec. 2017, doi: 10.1109/TIA.2017.2737406.

[27] M. D. Siddique et al., "A Single DC Source Nine-Level Switched-Capacitor Boost Inverter Topology With Reduced Switch Count," in IEEE Access, vol. 8, pp. 5840-5851, 2020, doi: 10.1109/ACCESS.2019.2962706.

[28] M. D. Siddique et al., "A New Single Phase Single Switched-Capacitor Based Nine-Level Boost Inverter Topology With Reduced Switch Count and Voltage Stress," in IEEE Access, vol. 7, pp. 174178-174188, 2019, doi: 10.1109/ACCESS.2019.2957180.

[29] H. K. jahan, M. Abapour, K. Zare, S. H. Hosseini, F. Blaabjerg and Y. Yang, "A Multilevel Inverter with Minimized Components Featuring Self-balancing and Boosting Capabilities for PV Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, doi: 10.1109/JESTPE.2019.2922415.