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A New Topology of Switched-Capacitor Multilevel Inverter With Eliminating Leakage Current

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ABSTRACT This paper proposes a new topology of the switched-capacitor multilevel inverter (SCMLI) for photovoltaics system, which can eliminate the leakage current. In the proposed topology, the capacitors are employed as a virtual DC power supply to boost the input voltage. Here, all capacitors are charging equal to DC source, thus, just one DC source is needed to achieve the staircase waveform. In this structure in order to make the negative levels, the capacitors are connected to the output in reverse polarity. Thus, the H-bridge circuit which is used in traditional SCMLI to build zero and negative voltage levels and leads a variable common mode voltage is removed. Due to the direct connection of the neutral terminal of the grid to the negative polarity of the PV; then this topology can eliminate the leakage current. In addition, the topology has an excellent ability to path the reverse current as well as an acceptable output waveform spectrum. The operating states of all components and loss calculations are analyzed and formulated accurately as well as simulated by using MATLAB-SIMULINK software. To confirm the performance of the proposed topology; a 500 W prototype is built and experimental results are presented.

INDEX TERMS Switched capacitor, multilevel inverter, leakage current, H-bridge, common mode voltage.

I. INTRODUCTION

Nowadays, many solar energy users tend to inject their surplus energy into the grid. The grid-connected photovoltaic systems can be divided into two different categories, with transformer and transformerless systems. For the systems with transformer, there is galvanic isolation between PV panel and grid. However, it leads to increase of cost, size and loss of power. Thus, transformerless system is a significant advantage to improve the overall system efficiency. One of the fundamental issues in the transformerless grid-connected systems is the negative effect of the leakage current due to the parasitic capacitor between the PV panels and the ground [1], [2].

Multilevel voltage source inverters (MLVSIs) have emerged as a popular solution to inject renewable energy sources, such as wind turbines, photovoltaic cells as well as into electric vehicles (EVs), advanced adjustable speed drives and different new power electrical applications [3], [4]. This category of converters can reduce the voltage stresses on the switches and decrease the electromagnetic interference (EMI) by generating a staircase voltage waveform, increase the voltage level numbers. In addition, the produced staircase waveforms at the output could decrease the total harmonic distortion (THD). Thus, to achieve acceptable THD, they need a smaller size output filter, which in turn, will decrease the size of inverters [5], [6]. The switched-capacitor multilevel inverters (SCMLIs) has the ability to boost the input voltage. In addition, they can create multilevel staircase waveform at the output, which eliminates the need for a large filter [5], [7]–[15]. Some conventional SCMLI's are illustrated in Fig. 1. The basic structure of a single-phase grid-connected inverter and the CM current path are shown in Fig. 2(a), where P and N indicate positive and negative polarity of the PV panel respectively. In this case, Z_G and C_{PV} refer to the ground impedance and the parasitic capacitance between the PV array and the ground. This CM voltage and the caused leakage current may lead to safety threats and

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reduce the efficiency as well as increase the grid current distortion [16]–[18]. Fig. 2(b) illustrates the facilitated equivalent scheme of the CM resonant current. The CM voltage is given by:

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} + (v_{AN} - v_{BN})\frac{L_2 - L_1}{2(L_1 + L_2)} \quad (1)$$

where v_{AN} and v_{BN} refer to the voltage difference between terminal A and B, the output of the inverter, in comparison with the neutral point of the PV cell. It is evident that by keeping the common mode voltage constant, the leakage current can be reduced. To achieve this, in the structure of full-bridge inverters such as H5 inverter [19], H6 inverter [17], HERIC inverter [20], etc., two inductors having identical values ($L_1 = L_2$) are used as the output filter. Thus, the equation of common mode voltage will be simplified as follows:

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} = Constant \quad (2)$$

In this solution, the output filter structure consists of two inductors with two separate cores, which increase the size and cost. Using half-bridge family inverters, such as neutral point clamped (NPC) inverters [21], is another way to keep the common mode voltage constant. It will eliminate one of the inductors (or is equal zero), so only one inductor is utilized as an output filter. In this case, the relationship of the common mode voltage is defined as:

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} + \frac{v_{AN} - v_{BN}}{2} \quad if: L_1 = 0 \quad (3)$$

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} - \frac{v_{AN} - v_{BN}}{2} \quad if: L_2 = 0 \quad (4)$$

The requirement of the double DC bus voltage is one of the drawbacks of this design when compared to the full-bridge structures. Fig. 3 shows topologies of the grid-connected inverter based on full-bridge and half-bridge power converter structures. On the other hand, all conventional switched-capacitor inverters suffer from the H-Bridge circuit to build negative polarity voltage levels at the output, which leads to a variable common mode voltage and thereby generating leakage current. Thus, it requires extra circuitry elements to obtain the constant CMV [22], [23].

Using a common ground (CG) is one of the effective methods to eliminate the leakage current. For this purpose, the negative terminal of the PV panel is directly connected to the neutral line of the grid, which ensures that the common mode voltage is stabilized and thus eliminates the leakage current [16] and [24]–[26]. In recent years some modified switched-capacitor inverters, as shown in Fig. 4, have used this solution to cancel the leakage current. Generally, for three-level inverters, if the capacitor does not connect in parallel with the voltage source at two consecutive levels, the voltage variations of the capacitor will increase considerably.

Fig. 4(a) illustrates an inverter structure, which uses this technique and include of five power switches [16]. In this

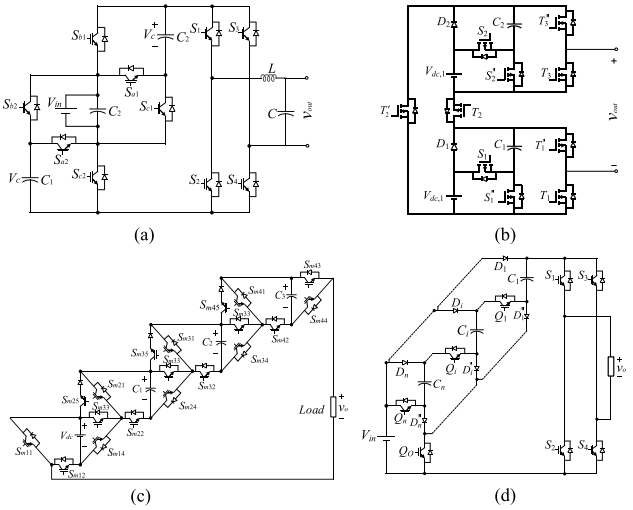

FIGURE 1. Switched-capacitor multilevel inverter topologies: (a) series-parallel SCMLI proposed in [10], (b) cascade SCMLI [13], (c) step-up SCMLI in [14], (d) SCMLI for pure resistance load [7].

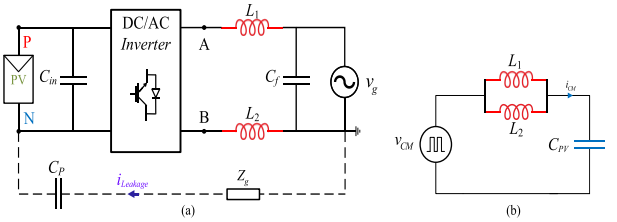

FIGURE 2. Basic structure of the single-phase grid-tied inverter: (a) CM current path, (b) equivalent scheme [16].

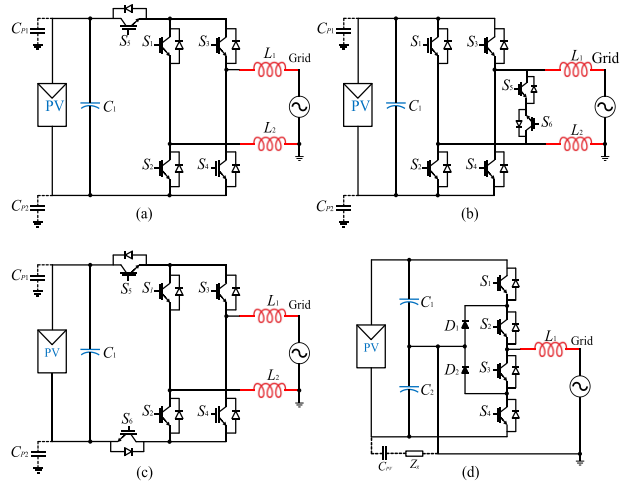

FIGURE 3. Full-bridge and Half-bridge topologies for grid-connected transformerless inverters: (a) H5 inverter [19], (b) HERIC inverter [20], (c) H6 inverter with DC bypass [17], (d) NPC half-bridge inverter [21].

topology, the capacitor at zero and $+V_{DC}$ levels goes in parallel with the source. Meanwhile, due to the circuit structure and the use of conventional switches, which also can flow the reverse current, it has the capability to be utilized as a reactive load. The flying capacitor transformerless inverter as shown

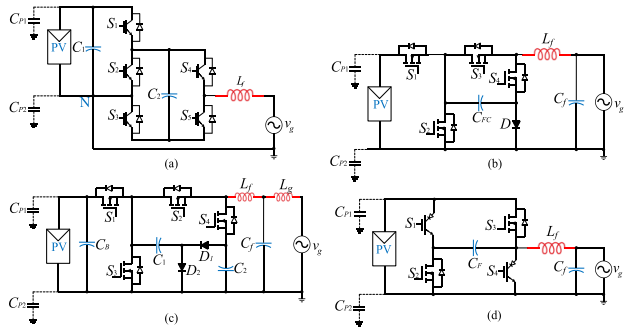

FIGURE 4. (CG) topologies for grid-connected inverters: (a) CG inverter proposed in [16], (b) Flying Capacitor CG Inverter proposed in [24], (c) Charge Pump CG Inverter proposed in [25] (d) Siwakoti-H inverter [26].

in Fig. 4(b) has reduced the number of controllable elements of the topology [24]. In this structure, there are two paths to charge the capacitor, while it makes +VDC and negative zero levels in output. However, for the inductive load, the current of the inductor cannot change quickly. Thus, the capacitor is in the path across the load and the current passes within the capacitor whilst the output is switching to positive zero level and then increases its voltage. Therefore, in re-switching to $+V_{DC}$ level, the capacitor cannot be tuned by DC source. In addition, at the negative level, as long as there is the reverse current, it will path through the capacitor (depending on the power factor), thus, the voltage variation of the capacitor raises. Fig. 4(c) shows the charge-pump topology which is proposed to resolve the abovementioned problem [25]. In this design, the capacitor that produces the negative output voltage level sets to the input source at the zero level, and the issue of increased voltage variation, is eliminated. Meanwhile, another path is considered for the reverse current. Thus, the reverse current does not pass through the capacitor. Siwakoti-H inverter topology [26], which is shown in Fig. 4(d), only consists of four switches and uses the lowest power semiconductor devices in comparison with other presented topologies. However, in the reactive power, there are the same problems as the flying capacitor inverter introduced in Fig. 4(b). At the positive cycle, the capacitor cannot regulate by the DC source. Moreover, at the negative cycle, it has reverse current. Thus, the circuit suffers from the increasing of capacitor voltage variation. Moreover, all the inverter structures mentioned above are only able to produce three-level output waveform. Therefore, boost circuit has to be added.

By considering the above-mentioned problems, this paper presents a novel switched-capacitor multilevel inverter topology, which has the potential to boost voltage as well as to eliminate the leakage current. The basic unit of the proposed topology contains four power switches and one capacitor. In summary, the advantages of the proposed topology and circuit characteristics can be described as follows.

(1) The proposed circuit only needs one input voltage source. Thus, the need for the boost circuit, which increases the size and costs, has been eliminated.

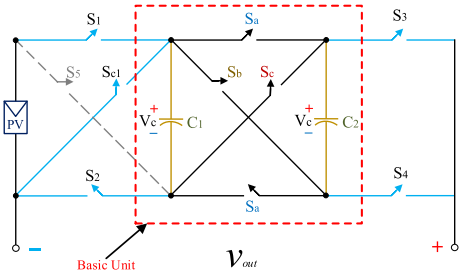

FIGURE 5. Basic topology for the proposed SCMLI.

(2) According to the symmetric structure in the proposed topology, each additional capacitor can be charged equal to the input voltage. Thus, two voltage levels can be achieved at the output and increases the maximum output voltage.
(3) In conventional SCMLIs, the H-bridge circuit is used to generate negative output levels. It will make a variable common mode voltage and thus lead to the leakage current. In the proposed SCMLI, direct connection of the neutral point of the grid to the negative polarity of PV panels leads to the formation of common ground in the circuit. Therefore, the leakage current is zero. On the other hand, the proposed inverter is the first MLI topology which can eliminate the leakage current.
(4) Some new equations by high accuracy are presented in this paper to calculate the switching losses, conduction losses and losses caused by the voltage drop of the capacitors (ESR).

The following sections organize this paper. The basic unit concept of the proposed inverter is described in Section 2. Based on that, a novel general topology is acquired, and the reason to choose unidirectional switches are explained. In section 3, the topology of a 5-level and a 9-level inverter are analyzed, which are derived from advanced general topology. In addition, the modulation strategy and operation states of switches and capacitors are described in detail. The voltage drop analysis of capacitors and calculation of the power loss have been given in Section 4. A comparison with other topologies have been done in Section 5 to prove the performance of the proposed circuit. The simulation and experimental results are shown in section 6 to confirm the validity of the proposed inverter.

II. PROPOSED CONCEPT

A. BASIC CIRCUIT

Fig. 5 illustrates the basic circuit of the proposed SCML inverter. It should be noted that S_a includes two groups of unidirectional switches. According to Fig. 5, the capacitors C_1 and C_2 are charging equally the DC source when the group of the switches S_a, S_1 and S_2 become ON and the other switches are OFF. In this state, the positive and negative polarity of C_1 and C_2 are connected to each other respectively, and two capacitors are in parallel. Another

Condition happens when S_b becomes ON, and other switches are OFF. Here, the positive polarity of C_1 is connected to the negative polarity of C_2. In this situation, if S_3 and S_2 become ON, the capacitors C_1 and C_2 will be in series to the load and generate a higher positive level in the output. In the last state, if S_c along with S_2 becomes ON (other switches of the unit were OFF), the negative polarity of C_1 is connected to the positive polarity of C_2 and if S_4 was ON, thus, the stored voltage in the capacitor C_2 is pumped to the output in reverse polarity. In fact, during the generation of positive and negative output voltage levels, S_3 and S_4 become ON respectively. In this structure, the DC power supply does not have a direct role to generate negative output levels. However, if the switch S_5 becomes ON, the DC source will be series with the capacitor; thus, it can make an extra positive output level rather to the negative levels. This state disturbs the symmetrical output waveforms. Thus, the switch S_5 is eliminated in order to prevent this state.

B. PROPOSED GENERAL SCMLI TOPOLOGY

Based on the primary unit presented in Fig. 5 a general topology of the multi-level inverter is shown in Fig. 6. According to this structure, to reach the higher voltage levels and increase the output voltage, it is enough to connect k basic unit in series. Each basic unit consists of four power switches and one capacitor. If the number of output voltage levels assumed to be n, then the number of capacitors, which is applied to build a multilevel inverter as well as the number of required power switches and the maximum output voltage are as follows:

$$N_{Level} = n \tag{5}$$

$$N_{Switches} = 2n - 1 \tag{6}$$

$$N_{Capacitor} = (n-1)/2 \tag{7}$$

$$V_{Out(\max)} = (n-1)\,V_{dc}/2 \tag{8}$$

III. PROPOSED TOPOLOGY AND MODULATION METHOD

A. PROPOSED 5-LEVEL AND 9-LEVEL SCMLI

According to the proposed generalized structure, the topology of the 5-level inverter, which comprises of one input voltage source, two capacitors, nine switches (seven ordinary switches and two unidirectional switches), is shown in Fig. 7 (a). In this case, unidirectional switches are utilized to charge the capacitors, which are located in higher stages, and when these kinds of switches are ON, the switches of S_b and S_c group will be OFF. On the other hand, it is noteworthy that the switches of S_a group make the capacitors charging path. The switches of S_b group make a series the capacitors with positive polarity. Moreover, while the S_c category switches are turning ON, the capacitors will be series with negative polarity to generate the negative levels. To confirm the functionality of proposed circuit in generating more output voltage levels and comparing with the similar structures in terms of the number of output levels, the 9-level structure of the inverter based on the proposed topology is introduced and

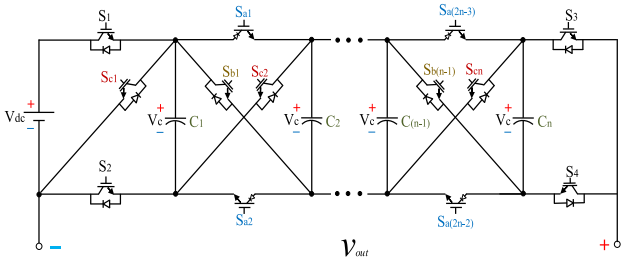

FIGURE 6. General structure of proposed SCMLI.

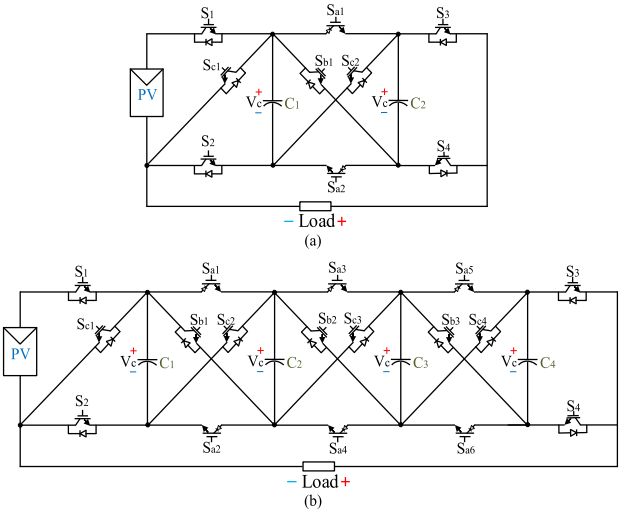

FIGURE 7. Proposed dc-ac inverter. (a) 5-level inverter, (b) 9-level inverter.

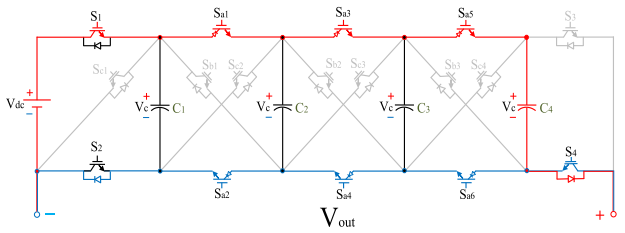

FIGURE 8. The state of switches and current flow in zero level (start-up).

analyzed, as shown in Fig. 7 (b). On the other hand, the states of the switches and capacitors in the 5-level is similar to the state of the switches in the 9-level circuit to make the same output levels, so the analysis of the 9-level inverter also includes the function of the switches in the 5-level inverter.

B. START-UP MODE

In the proposed switched-capacitor inverter in order to form the zero level, all S_a group switches (unidirectional switches) are ON, and all capacitors are charging as much as the input voltage source. In this case, the switches S_3 and S_4 are OFF and ON respectively as shown in Fig.8.

Fig. 9 and Fig.10 show the different switching states and the current flow path of the proposed 9-level inverter. Regarding the use of unidirectional switches in the circuit, there

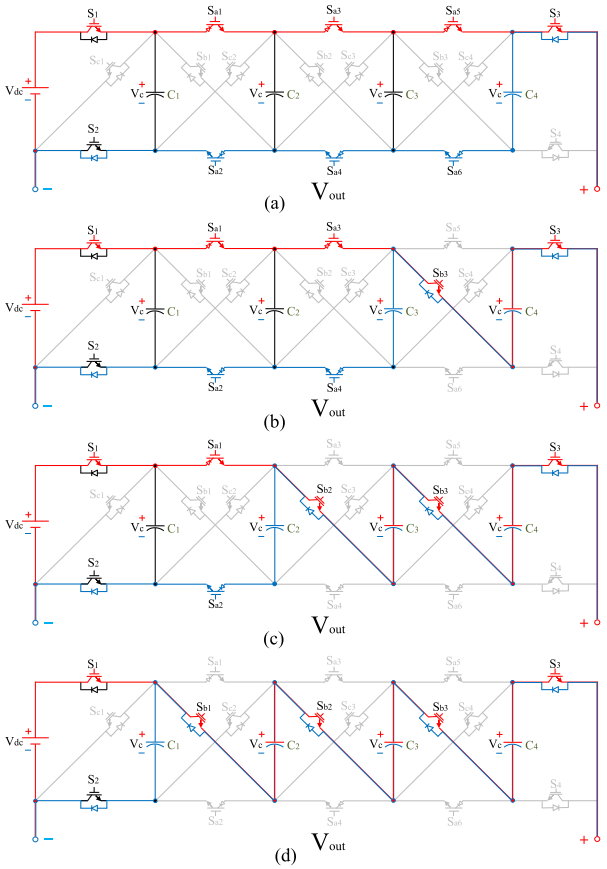

FIGURE 9. The states of switches and current flow in positive levels. (a) $V_{Out} = +V_{DC}$, (b) $V_{Out} = +2V_{DC}$, (c) $V_{Out} = +3V_{DC}$, (d) $V_{Out} = +4V_{DC}$.

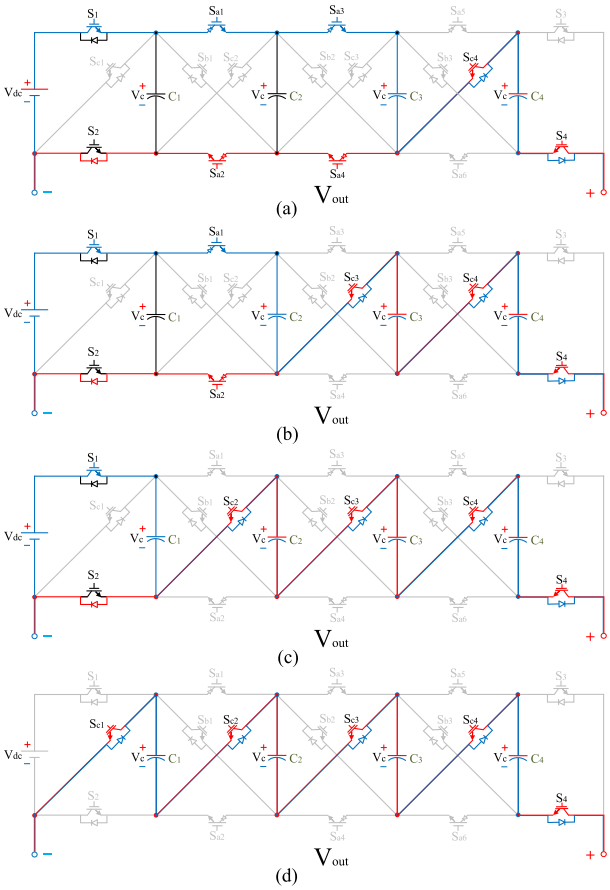

FIGURE 10. States of switches and current flow in negative levels. (a) $V_{Out} = -V_{DC}$, (b) $V_{Out} = -2V_{DC}$, (c) $V_{Out} = -3V_{DC}$, (d) $V_{Out} = -4V_{DC}$.

are two paths for forward and reverse current in the loop. The direction of the reverse flow caused by the inductive load marked in blue and the path of the working states of the inverter to determine the output voltage levels, as well as the charging path of the capacitors, are specified in red line. In addition, from this figure the different status of the capacitors in terms of charging/discharging are apparent. As it can be seen, the switches of the S_c group connect the capacitor to the output in reverse polarity to generate the negative output levels, and thus the need of H-bridge is eliminated.

When the $+V_{DC}$ level is forming, all S_a switches are still ON and only the switches S_3 and S_4 varies mode, and the voltage source directly generates the $+V_{DC}$ level as shown in Fig. 9(a). In this situation, all capacitors are in charging mode same as the zero voltage level. To make the $+2V_{DC}$ level, S_{a5} and S_{a6} are switched OFF and switch S_{b3} turned ON to pump the capacitor C4 in series with the voltage supply to the output load. Here, the capacitor C_4 is in the discharge mode, and other capacitors (C_1, C_2 and C_3) are charged by the DC power supply simultaneously (Fig.9 (b)). In the same way, other voltage levels will be created. To form each positive level, the capacitor of the related unit by the switch Sb is connected in series with the voltage source to the output load and the other switches of the unit turn OFF. It should be noted that the capacitor C_1 in all states of the production of positive levels is in parallel to the voltage source and is charging, thus it has no role in the creation of positive levels as shown in fig. 9. In the production of negative output levels, the switch S_c of each unit has illuminated to connect the capacitor of the unit with reverse polarity to the output. To build the first negative voltage level, the stored voltage of the capacitor C_4 is pumped through the switch S_{c1}. In this case, the other capacitors are in charging mode simultaneously as shown in Fig.10 (a). As it can be seen in Fig. 10(b) the capacitors C_3 and C_4 via the switches S_{c3}, S_{c4} and S_4 are series connected to the output to generate $-2V_{DC}$ level. In this term, the switches S_{a2} and S_2 are ON. Continuing this process makes $-3V_{DC}$ level (Fig. 10(c)). To create $-4V_{DC}$ level, all switches in the S_c group (S_{c1}, S_{c2}, S_{c3} and S_{c4}) with S_4 become ON and other switches are OFF as shown in (Fig. 10(d)). In this state, all capacitors are in discharging mode.

IV. SPWM MODULATION

Fig. 11 shows the modulation strategy and the corresponding control pulses of each switch in the proposed 9-level inverter. In this term, by utilizing a carrier-based level-shifted SPWM (LSSPWM) technique, the gate driver pulses are created. Based on this figure, four triangular carrier waveforms where

TABLE 1. On switches and capacitors states in proposed 9-level SCMLI.

	Reference	ON State Switches	Capacitor state				V_{out}
			C_1	C_2	C_3	C_4	
Positive ref	$ref > e_4$	$S_{b1}, S_{b2}, S_{b3}, S_1, S_2, S_3$	C	D	D	D	$4V_{DC}$
	$e_4 \geq ref > e_3$	$S_{a1}, S_{a2}, S_{b2}, S_{b3}, S_1, S_2, S_3$	C	C	D	D	$3V_{DC}$
	$e_3 \geq ref > e_2$	$S_{a1}, S_{a2}, S_{a3}, S_{a4}, S_{b3}, S_1, S_2, S_3$	C	C	C	D	$2V_{DC}$
	$e_2 \geq ref > e_1$	$S_{a1}, S_{a2}, S_{a3}, S_{a4}, S_{a5}, S_{a6}, S_1, S_2, S_3$	C	C	C	C	V_{DC}
	$\|ref\| \leq e_1$	$S_{a1}, S_{a2}, S_{a3}, S_{a4}, S_{a5}, S_{a6}, S_1, S_2, S_4$	C	C	C	C	0
Negative ref	$e_2 \geq \|ref\| > e_1$	$S_{a1}, S_{a2}, S_{a3}, S_{a4}, S_{c4}, S_1, S_2, S_4$	C	C	C	D	$-V_{DC}$
	$e_3 \geq \|ref\| > e_2$	$S_{a1}, S_{a2}, S_{c3}, S_{c4}, S_1, S_2, S_4$	C	C	D	D	$-2V_{DC}$
	$e_4 \geq \|ref\| > e_3$	$S_{c2}, S_{c3}, S_{c4}, S_1, S_2, S_4$	C	D	D	D	$-3V_{DC}$
	$\|ref\| > e_4$	$S_{c1}, S_{c2}, S_{c3}, S_{c4}, S_4$	D	D	D	D	$-4V_{DC}$

* *C*: Charging Mode * *D*: Discharging Mode

the amplitude of all carries are the same and equal to A_c, with similar frequency ($fs = 10$ kHz) are compared with a completed sinusoidal reference signal by the magnitude corresponding to A_r and frequency of 50 Hz. In this case, to produce switching control pulses in the negative cycle of the absolute amount of the reference signal is compared with the carrier. Therefore, the modulation index M is obtained from the following equation:

$$M = \frac{A_r}{4A_c} \tag{9}$$

Table 1 demonstrates the ON switches at various levels in proposed the 9-level inverter. Additionally, the operation of each capacitor at various levels are further shown in Table 1.

V. CALCULATION OF VOLTAGE DROP OF THE CAPACITORS, LOSSES, AND EFFICIENCY

One of the critical parameters in the design and analysis of power electronics circuits is the calculation of power dissipation. The accuracy of the estimate of this characteristic of the circuit in the technical evaluation and the application of the circuit and thus the final cost has a significant impact. The power losses in the proposed circuit consists of three categories. Power losses due to capacitor voltage drop, switching losses and conduction losses.

A. VOLTAGE DROP AND LOSSES OF CAPACITORS

In the proposed SCMLI, the capacitor will be parallel with the source during a time interval and charged equal to the input voltage while the group switches are ON. Then, to build up higher output levels, the stored energy in the capacitor is pumped to the output in series, which leads to decrease the voltage of the capacitor. On the other hand, due to the series connection of the capacitor with the output load at the discharging time, a voltage drop on the capacitor is created which leads to generating the power losses. Here, the charging and discharging of the capacitor by the switching

TABLE 2. Effectual charge/discharge modes of capacitors.

Level								
-4	-3	-2	-1	0	1	2	3	4
CD	C	C	C	C_1	C	C	C	C
D	CD	C	C	C_2	C	C	C	CD
D	D	CD	C	C_3	C	C	CD	D
D	D	D	CD	C_4	C	CD	D	D
	t_3	t_2	t_1		t_1	t_2	t_3	

*C: Charging *D: Discharging *CD: Charge-Discharge

frequency leads to making small, but large quantities of voltage drop.

In the intervals, where the capacitor is continuously connected to the output in series, this causes large voltage drop and effective power losses in comparison with the small voltage drop. According to Table 1, during two consecutive level $\pm n$ and $\pm(n+1)$, when the capacitor is in discharging mode; thus, it has an effective voltage drop. This voltage drop leads to generating power dissipation. On the other hand, when the capacitor is discharging continuously (at least in two levels that are sequential), the large voltage drop will have happened. While the capacitor is in charge/discharge mode by switching frequency, the caused voltage drop by this condition is low. Table 2 shows the effectual charge / discharge modes of the capacitors for the 9-level proposed inverter [27]. The determination of the time interval for various output levels in one-half cycle is shown in Fig. 12.

Based on this pattern, in each time interval, the reference wave is compared to the respective carrier to generate various output levels. Following equations represent t_i and t_i' [27].

$$\theta_i = \arcsin \frac{i}{M\,n} \tag{10}$$

$$t_i = \frac{\theta_i}{2\pi} T \tag{11}$$

$$t_i' = \frac{T}{2} - t_i \tag{12}$$

$$t_n = \frac{T}{4}, \quad \theta_n = \frac{\pi}{2} \tag{13}$$

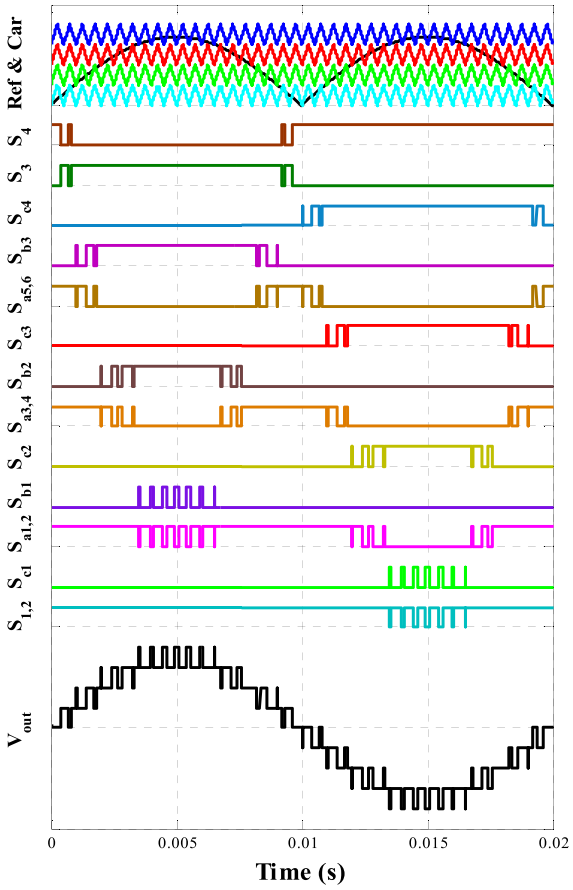

FIGURE 11. SPWM modulation and corresponding gate pulses.

$$\Delta t_i = t_i - t_{i-1} \tag{14}$$

where i is equal to $1, 2, \ldots, n$ and θ_i represents the corresponding angle to i. The voltage drop of the capacitor is obtained by:

$$\Delta V = \frac{1}{C} \int idt \tag{15}$$

The current waveform among to the pure resistive load is the same as the staircase voltage waveform, which leads to complicated calculations of the voltage drop. Thus, by an accurate assumption, the current is obtained as follows:

$$i = I_m \sin \omega t \tag{16}$$

$$I_m = \frac{nMV_{DC}}{R} \tag{17}$$

Due to Table 1 and Table 2 , it is obtained that the operation states of capacitors in positive and negative cycles are different. Therefore, the voltage drop of the capacitors for each cycle is derived from the following equations:

$$\Delta V_{Ci}^{+} = \frac{I_m}{C} \int_{t_{n+2-i}}^{t'_{n+2-i}} \sin \omega t dt = \frac{2I_m \cos \theta_{n+2-i}}{C\omega} \tag{18}$$

$$\Delta V_{Ci}^{-} = \frac{I_m}{C} \int_{t_{n+1-i}}^{t'_{n+1-i}} \sin \omega t dt = \frac{2I_m \cos \theta_{n+1-i}}{C\omega} \tag{19}$$

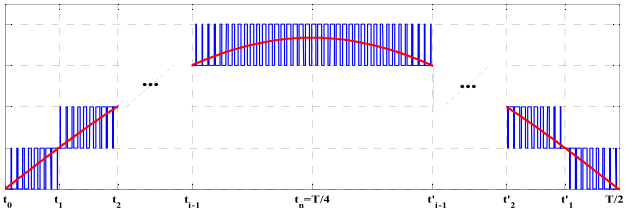

FIGURE 12. The half-cycle of output waveform of SCMLI.

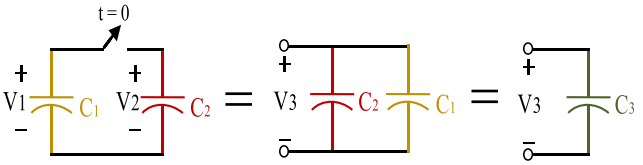

FIGURE 13. The states of switches and current flow in zero level.

Fig. 13 shows the connecting of two capacitors in the parallel term. The following equation gives the balanced voltage of two capacitors when are connected parallel:

$$V_3 = \frac{C_1 V_1 + C_2 V_2}{C_1 + C_2} \tag{20}$$

The total energy differences before and after the parallelization of the capacitors determine their energy dissipation. This energy is lost in the circuit as a form of the spike, which can be calculated from the following equations.

$$\begin{aligned} E_{Loss} &= E - E' = \frac{1}{2}C_1\left(V_1^2 - V_3^2\right) + \frac{1}{2}C_2\left(V_2^2 - V_3^2\right) \\ &= \frac{1}{2}C_1 \underbrace{(V_1 - V_3)^2}_{\Delta V_1^2} + \frac{1}{2}C_2 \underbrace{(V_2 - V_3)^2}_{\Delta V_2^2} \end{aligned} \tag{21}$$

Due to the equation $\Delta E_{Loss(C_i)} = C_i \Delta V_i^2/2$ and with considering (21), the equation of energy loss is summarized as follows:

$$\begin{aligned} \frac{E_{Loss_{C_2}}}{E_{Loss_{C_1}}} &= \frac{\frac{1}{2}C_2\Delta V_2^2}{\frac{1}{2}C_1\Delta V_1^2} = \frac{C_2}{C_1}\left(\frac{V_3 - V_2}{V_3 - V_1}\right)^2 = \frac{C_1}{C_2} \\ &\Rightarrow E_{Loss_{C_1}} = \frac{C_2}{C_1} E_{Loss_{C_2}} \end{aligned} \tag{22}$$

By simplifying the above equations, the energy losses due to the voltage drop of the capacitor are expressed as follows:

$$E_{Loss}|_{C_1 \to \infty} = \lim_{C_1 \to \infty} \frac{1}{2}\frac{C_2}{C_1}(C_1 + C_2)\Delta V_2^2 = \frac{1}{2}C_2\Delta V_2^2 \tag{23}$$

Thus, by concerning the previous equations, and modelling the DC power supply with the capacitor, which has infinity capacitance, and zero voltage drop, the losses due to the parallelization of the capacitors with the voltage source are obtained from the following equation.

$$E_{Loss}|_C = \frac{1}{2}C\Delta V^2 \tag{24}$$

$$P_{Loss}|_C = E_{Loss} f_L \tag{25}$$

where f_L is the output frequency. Notwithstanding a large number of small spikes (which happened due to parallelization of the capacitor with the voltage source at the switching frequency), their voltage variations are negligible. Therefore, it is possible to ignore the losses of these spikes compared to large spikes.

B. SWITCHING LOSS

The output current path for different voltage levels (positive, zero and negative), and the ON switches in this flow path as well as ON switches on the charge path of the capacitors are shown in Fig. 8. In the zero levels, the current flow to the output via the switches S_1, S_{a1}, S_{a3}, S_{a5} and S_4. Likewise, the ON switches can be found on the output current path for other levels. While the output voltage is changing from zero to the positive level ($+V_{DC}$), only two switches change (S_3 turns ON, and S_4 turns OFF). In generating different positive levels always, one unidirectional switch from S_a group turns OFF and one traditional switch from S_b group turns ON. The switch S_4 during the time interval of generating zero level and the whole time interval of negative levels turns ON. In the formation of negative levels, at each stage, one unidirectional switch is turned OFF, and one traditional switch from S_c group goes ON. Thus, the switching losses due to considering the state of switches in each level are calculated as follows [28].

$$P_{SW} = f_s \left(E_{SW(on)} + E_{SW(off)}\right) \times D_S \tag{26}$$

where $E_{SW(on)}$ and $E_{SW(off)}$ represent the turn-on and turn-off energy loss respectively that can be achieved from the datasheet. Because in multilevel inverters, most switches are not switching during the whole of the period; therefore, in calculating the switching losses, only the active switching times of each switch are used. The correction factor for switching losses is the ratio of the effective switching time of each switch to the whole period, which can be derived as follows:

$$D_{S(i,i+1)} = \frac{2\,\Delta t_{(i,\,i+1)}}{T} \tag{27}$$

Here $D_{S(i,i+1)}$ is the ratio of time while the output waveform is switching between two levels i and $(i+1)$ to the whole period.

C. CONDUCTION LOSS

In other studies, in the calculation the conduction losses it is assumed that the switch is used to conduct during the whole period. However, the switch conducts only in the part of the period. Therefore, accurate calculation of conductive losses, especially in the SPWM modulation method, requires correction coefficient. This coefficient represented the ratio of the activation of the levels over the whole of the period and indicated by DC. Therefore, the conduction losses can be derived by follow:

$$P_{CON} = V_{CE(ON)} \times I_{C(ON)} \times D_C \tag{28}$$

$$D_{Ci} = \frac{t_{Li}}{T} \tag{29}$$

$$t_{Li} = 2\left[S_i(t_i - t_{i-1}) + (1 - S_{i+1})(t_{i+1} - t_i)\right] \tag{30}$$

$$S_i = \frac{1}{t_i - t_{i-1}} \int_{t_{i-1}}^{t_i} (Mn \sin \omega t - i + 1)\, dt \tag{31}$$

where D_{Ci} and t_{Li} represent the correction coefficient and activation time in level i respectively. While the output waveform is switching between two levels i and $(i-1)$, S_i indicates the ratio of the time, which the output is on level i to the whole time interval.

VI. COMPARISON DISCUSSION

A comparison of the proposed inverter concerning the number of semiconductor devices, output levels, ability to be extended, the capability to eliminate the leakage current as well as boosting the input voltage and the efficiency are listed in Table 3 . It should be noted that there is no the same condition in comparison Table. Because this comparison contains some traditional SCMLIs which can boost the voltage and make more than three levels at the output but, cannot eliminate the leakage current and, some other three-level inverters, which can eliminate the leakage current but suffer from needing to boost circuit and cannot be extendible. Therefore, the proposed circuit is the first SCMLI, which can eliminate the leakage current and can be easily extendible. Only by adding four switches and one capacitor can be achieved two more voltage levels at the output.

As can be seen in Table 3 , in the proposed inverter, for each basic unit, four power switches further are required, which compared to the proposed inverter in [14] it has an optimal number of switches and only is more than the number of the switches used in the technology proposed in [10] (one switch further per unit). On the other hand, in comparison with other SCMLIs that have the potential to boost the voltage, only the proposed topology can eliminate the leakage current, and other SCMLIs suffer from this issue. In addition, the topologies introduced in Table 3 which can eliminate the leakage current [23]–[26] are not capable to increase the voltage and required boost circuitry. The proposed inverter, unlike traditional SCMLIs, does not need to H-bridge circuit. In this case, similar to the inverters mentioned in [23]–[26], to create the negative levels, the capacitor with reverse polarity is connected to the output. Due to the multilevel waveform at the output of the proposed inverter, the output waveform compared to the suggested topologies in [23]–[26] is qualitative. Thus, the THD of the proposed inverter is less than them.

VII. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

This section presents several simulation results for the proposed 9-level, and 5-level derived inverters by utilizing MATLAB/SIMULINK software. In this case, all semiconductor devices are assumed with internal resistance $R_{on} = 0.1\ \Omega$. The switches are driven based on the proposed modulation strategy with a switching frequency $f_{SW} = 10$ kHz and the modulation index $M = 0.85$. Table 4 gives the parameters

TABLE 3. Comparison of the proposed topology with suggested topologies of [10], [11], [14], [23], [24], [25] and [26].

Parameter	[10]	[11]	[14]	[23]	[24]	[25]	[26]	Proposed
Output level	n	n	n	3	3	3	3	n
Number of Switches	(3n-1)/2	(3n-1)/2	(5n-7)/2	5	4	4	4	(2n-1)
Number of Capacitors	(n-3)/2	(n-3)/2	(n-3)/2	1	1	2	1	(n-1)/2
H-bridge circuit	Need	Need	--	--	--	--	--	--
Number of diode	--	--	(n-3)/2	--	1	2	--	--
Ability to boost the voltage	Yes	Yes	Yes	No	No	No	No	Yes
Ability to be extended	Yes	Yes	Yes	No	No	No	No	Yes
Eliminating the leakage current	No	No	No	Yes	Yes	Yes	Yes	Yes
Efficiency (%)	85.9	92.9	88.9	97.5	99.2	97.4	98	96.7

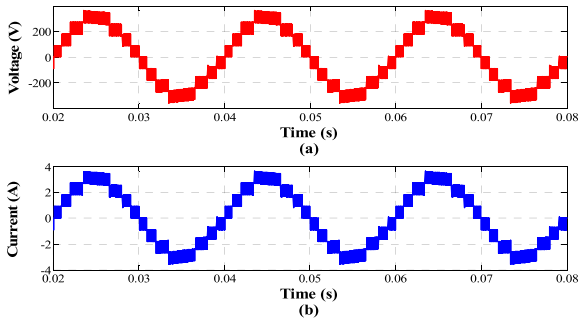

FIGURE 14. Waveform of 9-level inverter cos(φ) = 1.

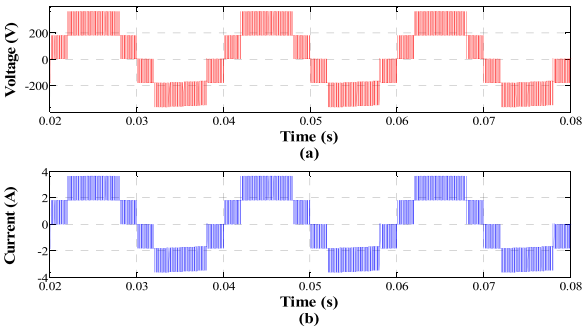

FIGURE 15. Waveform of 5-level inverter cos(φ) = 1.

that are applied for the simulation of the proposed topologies. The output voltage and current waveforms of the 9-level and 5-level inverter for pure resistive R_{Load} = 100 Ω with a line frequency equal to 50 Hz are shown in Fig. 14 and Fig. 15 respectively.

According to the proposed method, the maximum values of output voltage and current waveform (peak value) are equal to 366 V and 3.66 A, respectively. Fig.16 and Fig. 17 show the output waveform of these two structures by considering Inductive-Resistive load (R-L), which R_{Load} = 90 Ω and L_{Load} = 140 mH ($cos\varphi$ = 0.9). The THD of the output waveform without having a filter for inductive-resistive load ($cos\varphi$ = 0.9) are 18% and 36.4% for 9-level and 5-level inverter respectively as shown in Fig. 18.

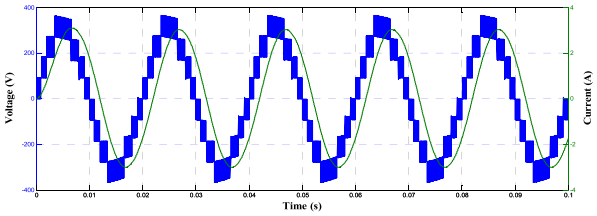

FIGURE 16. Voltage and current waveform of 9-level inverter with cos(φ) = 0.9.

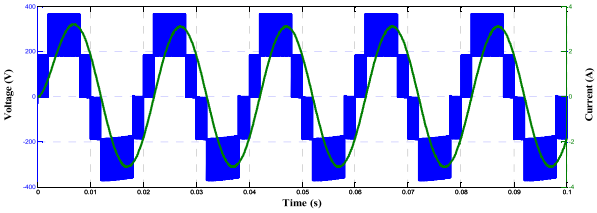

FIGURE 17. Output voltage and current waveform of 5-level inverter with cos(φ) = 0.9.

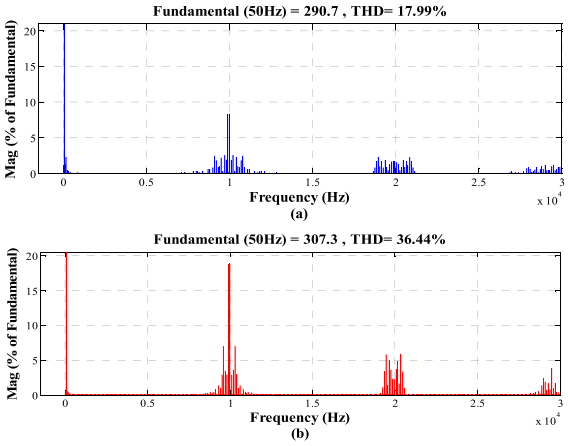

FIGURE 18. Frequency spectrum of voltage. (a) 9- level inverter (b) 5-level inverter (cos(φ) = 0.9).

The dynamic performance of step load for the output voltage/current waveforms and the voltage of the capacitors for changing the load from (90 Ω + 140 mH) to (45 Ω + 70 mH)

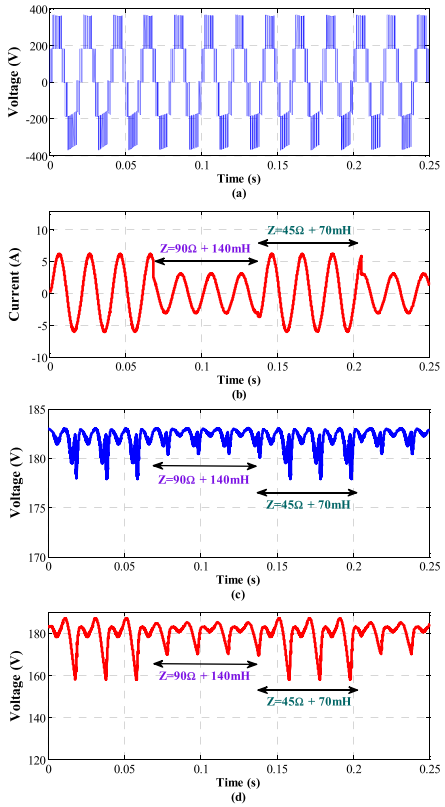

FIGURE 19. Simulation result of the proposed 5-level inverter in dynamic state. (a) V_{out}, (b) i_{out}, (c) V_{c1} and (d) V_{c2}.

and vice versa is shown in Fig. 19. It has been represented that the proposed inverter can track step change when the output power is decreased from 1000 W to 500 W (or increased from 500 W to 1000 W). As it can be seen, this test demonstrates the effectiveness of the power control strategy used in this paper in terms of fast response.

Fig. 20 and 21 show the voltage variation across the capacitors in the proposed 9-level and 5-level inverter respectively. In this case, the voltages of capacitors are simulated two times. Fig. 20 (a) and Fig. 21 (a) represent the voltage variation of the capacitors for the R-L load with $cos\varphi = 0.9$. Fig. 20 (b) . and Fig. 21 (b) show the voltage variation of the capacitors for pure resistive load $cos\varphi = 1$ ($R_{Load} = 100\Omega$).

In this structure, due to, the capacitor of upper unit (C_i) compared with the capacitor in down unit (C_{i-1}), will be series connected with the DC source in large time. Thus, it has a higher voltage drop when the output is at the peak value. It is necessary to mention that, the capacitor C_1 in generating all states except $-4V_{DC}$ in the 9-level inverter and $-2V_{DC}$ at 5-level is in parallel with the DC source. In addition, in generating these levels, this capacitor is charged and discharged with the switching frequency. Therefore, there is no significant voltage drop. In respect to (18) and (19), in the 5-level proposed inverter, the voltage drop of capacitor C_1 does have a small, while the capacitor C_2 has a large voltage drop for the negative half-cycle, which results in a

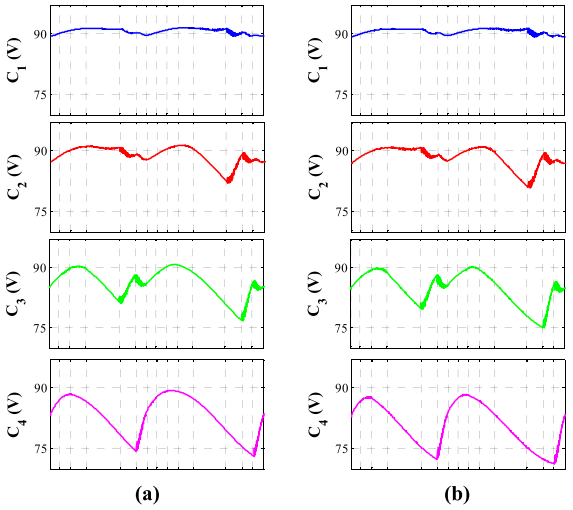

FIGURE 20. Voltage variation of capacitors in 9-level SCMLI. (a) cos(φ) = 0.9, (b) cos(φ) = 1.

TABLE 4. Effectual charge/discharge modes of capacitors.

Parameter	9-Level	5-Level
Input voltage V_{dc}	91.5 V	183 V
Output voltage v_{ac}	220 V	220 V
Carrier frequency (f_S)	10 kHz	10 kHz
Line frequency	50 Hz	50 Hz
Capacitors (μF)	4* C_{FC}=1000	2* C_{FC}=1000
Resistive load	100 Ω	100 Ω
Load (R-L)	90 Ω + 140 mH	90 Ω + 140 mH

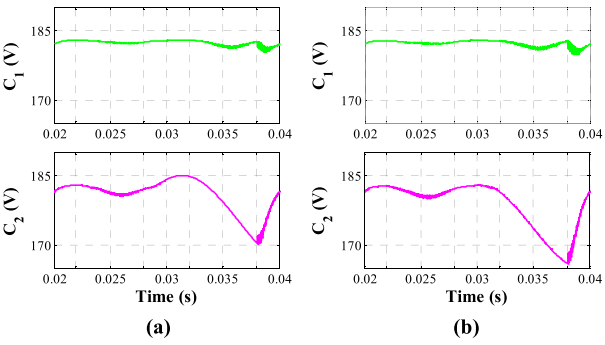

FIGURE 21. Voltage variation of capacitors in 5-level SCMLI. (a) cos(φ) = 0.9, (b) cos(φ) = 1.

voltage drop of 16 V. Here, according to the simulation results and based on the loss equations in section 4, the losses due to the voltage drop of the capacitors as well as switching and loses and conductive losses for 5-level inverter are obtained by follows.

According to the (24) and (25), the losses due to the voltage drop across the capacitors in the 5-level inverter obtained 6.5 W. Based on (26) and (27), switching losses for 5-level

propose inverter calculated by following equations:

$$P_{SW(S_1)} = f_{SW}\left(E_{on}+E_{off}\right)_{\substack{V=183^V\\I=0^A}} D_{S(-2,-1)} = 0 \quad (32)$$

$$P_{SW(Diode)} = f_{SW}\left(E_{RR}\right)_{\substack{V=183^V\\I=1.83^A}} D_{S(-2,-1)} \quad (33)$$

$$P_{SW(S_{c_1})} = f_{SW}\left(E_{on}+E_{off}\right)_{\substack{V=183^V\\I=3.66^A}} D_{S(-2,-1)} \quad (34)$$

$$P_{SW(S_{a_1})} = f_{SW}\left(E_{on}+E_{off}\right)_{\substack{V=183^V\\I=0^A}} D_{S(-1,0)} + f_{SW}\left(E_{on}+E_{off}\right)_{\substack{V=183^V\\I=1.83^A}} D_{S(1,2)} \quad (35)$$

$$P_{SW(S_{a_2})} = f_{SW}\left(E_{on}+E_{off}\right)_{\substack{V=183^V\\I=0^A}} D_{S(-1,0)} + f_{SW}\left(E_{on}+E_{off}\right)_{\substack{V=183^V\\I=0^A}} D_{S(1,2)} = 0 \quad (36)$$

$$P_{SW(S_{b_1})} = f_{SW}\left(E_{on}+E_{off}\right)_{\substack{V=183^V\\I=3.66^A}} D_{S(1,2)} \quad (37)$$

$$P_{SW(S_{c_2})} = f_{SW}\left(E_{on}+E_{off}\right)_{\substack{V=183^V\\I=1.83^A}} D_{S(-1,0)} \quad (38)$$

$$P_{SW(S_3)} = f_{SW}\left(E_{on}+E_{off}\right)_{\substack{V=183^V\\I=1.83^A}} D_{S(0,1)} \quad (39)$$

$$P_{SW(S_4)} = f_{SW}\left(E_{on}+E_{off}\right)_{\substack{V=183^V\\I=0^A}} D_{S(0,1)} = 0 \quad (40)$$

where E_{RR} refers to the reverse recovery energy of the diode. Therefore, switching losses of all switches in the proposed inverter can be derived as follow:

$$P_{SW} = \sum P_{SW(S_i)} \simeq 1\,W \quad (41)$$

Due to (27-30) the conduction losses of each switch is obtained from the following equations:

$$P_{C(S_1)} = V_{CE(on)}I_{C_{|_{I=0^A}}} D_{C(-1)} + V_{CE(on)}I_{C_{|_{I=0^A}}} D_{C(0)} + V_{CE(on)}I_{C_{|_{I=1.83^A}}} D_{C(1)} + V_{CE(on)}I_{C_{|_{I=3.66^A}}} D_{C(2)} \quad (42)$$

$$P_{C(S_{2_{(Diode)}})} = V_{CE(on)}I_{C_{|_{I=1.83^A}}} D_{C(-1)} \quad (43)$$

$$P_{C(S_2)} = V_{CE(on)}I_{C_{|_{I=0^A}}} D_{C(0)} + V_{CE(on)}I_{C_{|_{I=0^A}}} D_{C(1)} + V_{CE(on)}I_{C_{|_{I=0^A}}} D_{C(2)} = 0 \quad (44)$$

$$P_{C(S_{c_1})} = V_{CE(on)}I_{C_{|_{I=3.66^A}}} D_{C(-2)} \quad (45)$$

$$P_{C(S_{a_1})} = V_{CE(on)}I_{C_{|_{I=0^A}}} D_{C(0)} + V_{CE(on)}I_{C_{|_{I=1.83^A}}} D_{C(1)} \quad (46)$$

$$P_{C(S_{a_2})} = V_{CE(on)}I_{C_{|_{I=0^A}}} D_{C(0)} + V_{CE(on)}I_{C_{|_{I=0^A}}} D_{C(1)} = 0 \quad (47)$$

$$P_{C(S_{b_1})} = V_{CE(on)}I_{C_{|_{I=3.66^A}}} D_{C(2)} \quad (48)$$

$$P_{C(S_{c_2})} = V_{CE(on)}I_{C_{|_{I=1.83^A}}} D_{C(-1)} + V_{CE(on)}I_{C_{|_{I=3.66^A}}} D_{C(-2)} \quad (49)$$

$$P_{C(S_3)} = V_{CE(on)}I_{C_{|_{I=1.83^A}}} D_{C(1)} + V_{CE(on)}I_{C_{|_{I=3.66^A}}} D_{C(2)} \quad (50)$$

$$P_{C(S_4)} = V_{CE(on)}I_{C_{|_{I=3.66^A}}} D_{C(-2)} + V_{CE(on)}I_{C_{|_{I=1.83^A}}} D_{C(-1)} + V_{CE(on)}I_{C_{|_{I=0^A}}} D_{C(0)} \quad (51)$$

Therefore, the conduction losses of all switches in the proposed inverter can be derived as follow:

$$P_{Cond} = \sum P_{C(S_i)} \simeq 9\,W \quad (52)$$

Finally, the following equation can represent the efficiency of the proposed SCMLI:

$$\eta = \frac{P_{Out}}{P_{Out} + P_{Loss,\,Cap} + P_{SW} + P_{Cond}} \quad (53)$$

From (53) for 5-level proposed inverter the efficiency is given 96.7%.

TABLE 5. Parameters and components of five-level inverter.

Parameter	Value
Power rating (P)	500 W
Input voltage V_{dc}	183 V
Output voltage v_{ac}	220 V
Carrier frequency (f_S)	10 kHz
Line frequency	50 Hz
Capacitors	2* C=1000 µF, 200 V
Power switches, IGBT	HGTG12N60A4D Fuji Electric FGW85N60RB
Resistive load	100 Ω
R-L load	90 Ω + 140 mH

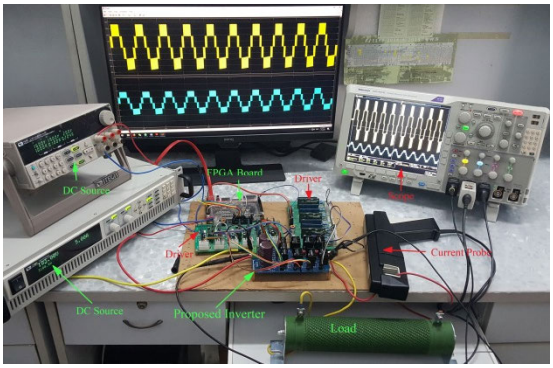

FIGURE 22. Laboratory prototype of the grid-tied proposed inverter used in the experiment.

B. EXPERIMENTAL RESULTS

To confirm the feasibility of the proposed topology, a 5-level, 500 W, single-phase inverter has been made and tested to get experimental results. A picture showing the implemented inverter is depicted in Fig. 22. The components and parameters which are listed in Table 5 has been used in the prototype.

The control pulses for IGBTs are generated by the processor (FPGA AX301) based on LSSPWM technique. With an input DC voltage of 183 V, a 5-level waveform, which is boosted to 363 V, is given at output of the inverter.

All switches are working at the same switching frequency of 10 kHz. According to result, the maximum value (peak) of

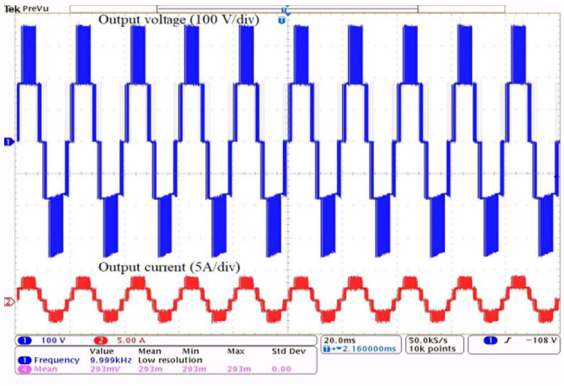

FIGURE 23. Observed voltage and current waveform of 5-level inverter with cos(φ) = 1 (R = 100 Ohm).

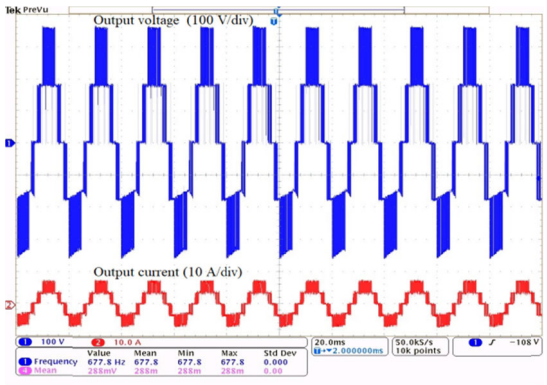

FIGURE 24. Observed voltage and current waveform of 5-level inverter with cos(φ) = 1 (R = 50 Ohm).

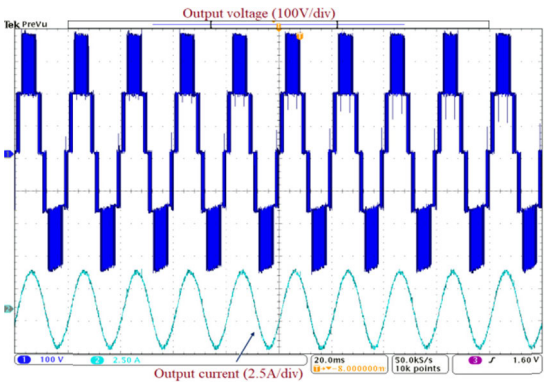

FIGURE 25. Observed voltage and current waveform of 5-level inverter with cos(φ) = 0.9.

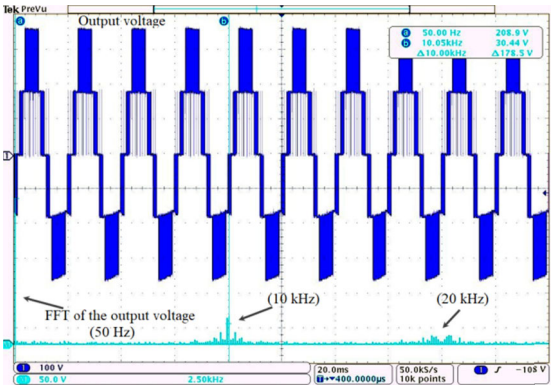

FIGURE 26. Output waveform and fast Fourier transform analysis of V_{out}. [50 V/div and 2.5 kHz/div] (R = 100 Ohm).

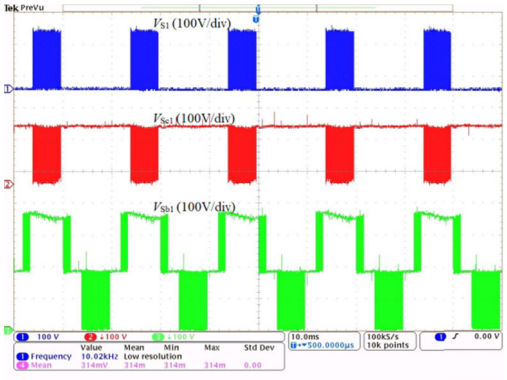

FIGURE 27. Voltage Stress (V_{CE}) across the switches S_1, S_{C1} and S_{b1} [100 V/div].

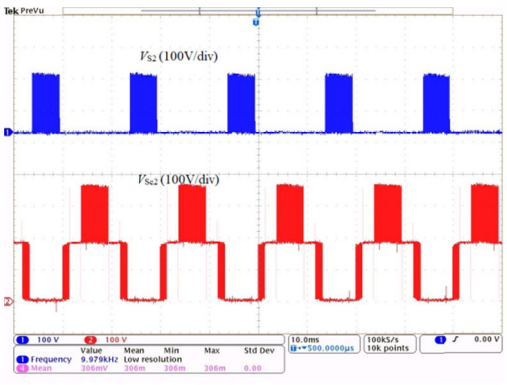

FIGURE 28. Voltage Stress (V_{CE}) across the switches S_2 and S_{C2} [100 V/div].

the output voltage and current waveform (which are in the same phase) are equal to 363 volts (RMS value is 220 V) and 3.6 A, respectively for pure resistive load R = 100 Ohm ($cos\varphi = 1$) as shown in Fig. 23. Fig. 24 shows the output voltage and current waveform for pure resistive load R = 50 Ohm, which leads to generate a maximum value current equal to 7.2 A. The output voltage and current waveforms in R-L load ($cos\varphi = 0.9$) is shown in Fig. 25. The measured efficiency of the proposed inverter for the purely resistive load is around 96 %.

Fig. 26 shows the harmonic spectrum of the output voltage for pure resistors of 100. As it can be seen, the first disturbing harmonic appears at a switching frequency of 10 kHz, and its value is close to the simulated value equal to 14.5%.

The voltage stress across the all switches are shown in Fig. 27-30. According to these diagrams, the voltage stress of two categories of switches, which connect the capacitors in

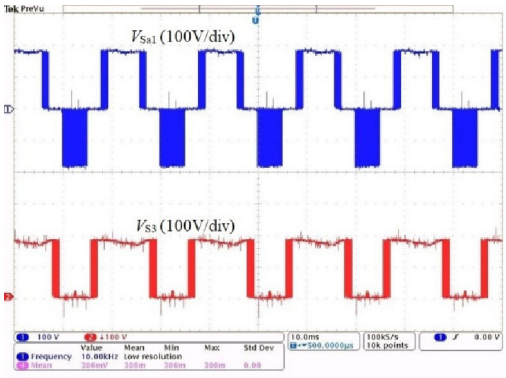

FIGURE 29. Voltage Stress (V_{CE}) across the switches S_{a1} and S_3 [100 V/div].

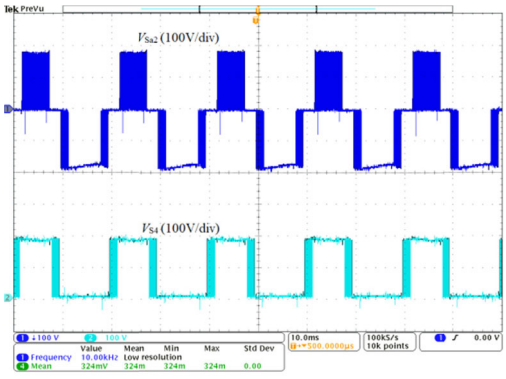

FIGURE 30. Voltage Stress (V_{CE}) across the switches S_{a2} and S_4 [100 V/div].

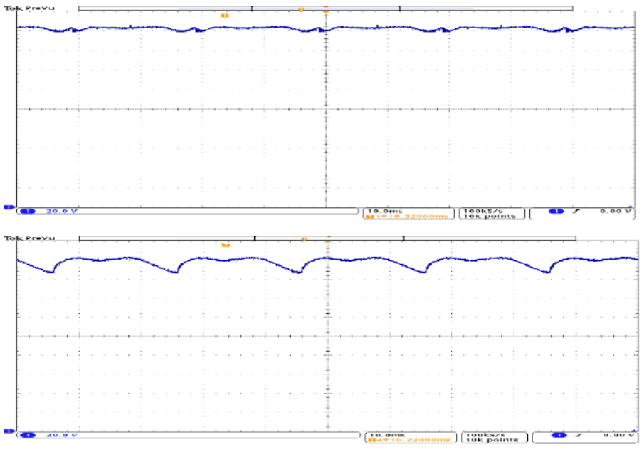

FIGURE 31. Laboratory Measured voltage waveform of the capacitors. (a) V_{C1}, (b) $V_{C2}(\cos(\varphi) = 1)$ [20 V/div].

series is twice as input DC source, and voltage stress on other switches is equal to the input DC voltage. It should be noted that the voltage stress of the switches S_b and S_c in each unit by extending the proposed structure to generate more output voltage level, always are equal to $2V_{DC}$.

As expected, and as it is shown in Fig. 31, the voltage drop of capacitor C_1 is negligible. However, the capacitor C_2 in the negative half cycle is in discharge mode at two consecutive levels ($-V_{DC}$ and $-2V_{DC}$), then, the voltage drop is significant, and its value is approximately 16.5 V, which is equal to the calculated value based on the theoretical.

VIII. CONCLUSION

This paper has proposed a new topology of the switched-capacitor multilevel inverter, which can eliminate the leakage current. The proposed inverter can be extended as n-level SCMLI, and thus, the output waveform has an acceptable quality as well as decrease in the output filter size compared to 3-level inverters which eliminate the leakage current. Traditional SCMLI is based on H-bridge circuit to make zero and negative levels, which suffer from a variable common mode voltage. However, here, the H-bridge circuit is eliminated. In this case, to generate the negative levels, the capacitor pumped the stored energy to the output in reverse polarity. In this circuit, the neutral polarity of the grid is directly connected to the negative point of the PV panels, which leads to make a common ground and eliminate the leakage current. In the proposed topology, a sinusoidal pulse-width modulation method is employed to self-balance the voltage of all capacitors equal to the DC source. A nine-level and five-level SCMLI have been analyzed and studied, and the losses, which contain capacitor loss, switching loss, and conduction loss, are all calculated and formulated. The comparison between the proposed topology and other existing circuits shows excellent performance of it in both boosting the voltage and eliminating the leakage current. The 9-level and 5-level structures of the proposed inverter are simulated by MATLAB/SIMULINK software. A 500 W 5-level prototype is built, and several experimental results have been presented to confirm the validity the performance of the proposed topology.

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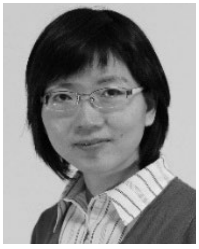

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