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Abstract—This paper presents a novel switched-capacitor (SC) based (2n+1)-level single-phase inverter with a reduced number of components and input DC voltage supply. This inverter is designed in a way that just one DC source is required to generate different voltage levels. The circuit consists of three major parts, i.e., front-end boost stage, active switched capacitor cell(s) in the middle and H-bridge inverter at the end. The total number of output voltage level is up to (2n+1) levels, where $n \geq 2$ is the number of switching cells, which consists of three active switches and two capacitors. Compared to conventional SC-based multilevel inverter topologies, the proposed topology features many advantages such as: (1) low number of semiconductor devices, (2) quasi-resonant charging of capacitors that reduce the inrush current and current stress on the devices, (3) self-balancing of capacitor and (4) reduced voltage stress on the switches. Moreover, a simple sinusoidal pulse-width modulation technique is employed here to generate the modulation signals for the proposed inverter. The operating principle is presented in detail followed by comparative analysis, thermal modelling and design guidelines. Finally, computer simulation and laboratory test results are carried out for a 5-level inverter with one SC cells as well as a 7-level inverter with two SC cells as two examples to verify the performance of the proposed (2n+1)-level inverter. Measurement results show that the proposed inverter has the 96.5±1% efficiency over a wide range of load with a peak efficiency of 98.56%.

Index Terms—Multilevel inverter, Transformerless inverter, switched capacitor, voltage boost, quasi resonant switching.

I. INTRODUCTION

DURING the last decade, the percentage of electric energy generated from renewable energy sources has been increasing dramatically. This trend is due to new energy policies in order to tackle global issues like climate change, high energy cost, insecurity and unavailability of electric energy to everyone. Among various renewable energy sources (e.g. photovoltaic (PV), wind, biogas, biomass, hydro, and geothermal), PV systems have been broadly implemented around the world in different scales. It is predicted that the installation of PV panels will increase dramatically because of the rapid reduction in production costs, and it is expected that the PV generation will reach 25% of the total generated energy by 2050 [1]. As a result, the demand of grid-tied inverters for small- and large-scale PV installations has gradually been increasing throughout the world [2]. High power quality with minimum distortion factor is one of the essential requirements that any utility company is looking for, which is difficult to meet by a simple three-level inverter. Different multilevel converters have been introduced for PV applications to improve power quality, efficiency and power density [3], [4]. Similar trends can be found in other renewable sources such as small-scale wind turbine and fuel cell, where application of high boost type multilevel inverters considerably increase the energy throughput and deployment of such scalable energy sources.

The most common types of multilevel converters are diode clamped, cascaded H-bridge (CHB), capacitor clamped, and active neutral point Clamped (ANPC) [5]-[7]. These topologies often require a high number of semiconductor devices with complex control schemes to realize a 5- or 7-level inverter. In addition, the flying capacitor (FCC) voltage as well as the DC-link voltage is difficult to balance in some topologies [8], [9]. Moreover, most multilevel inverters require a high DC-link voltage that is up to two times of the peak AC voltage. A single-stage DC-AC converter with boost capability offers an interesting alternative compared to two-stage approaches [10]-[12]. Recently, various single-stage inverters have been proposed to eliminate the need of a front-end high step-up DC-DC converter [13]-[15]. A 5-level inverter topology presented in [16] that uses the FCC principle [16], enhances the voltage gain from half to unity, thus reducing the DC-link voltage by half. However, this topology is not capable of extending the voltage level. In [17], a new topology with boosting feature is presented using switched capacitor (SC), but one main drawback related to this circuit is that it is not capable of extending the voltage level due to the variation in the input voltage. In addition, a large number of semiconductor devices are required.

The first generation of the SC-based multilevel inverters are proposed in the early 90's and up to now they are well developed, and many new topologies have been presented [9]-[10], [13], [18]-[20]. Fig. 1 shows six boost inverter topologies with reactive power capability based on SC structure leading to (2n+1)-level inverters. Fig. 1(a) is a topology that was proposed in 1998 [10], where each cell requires a large number of semiconductor devices (i.e. two MOSFETs, and two diodes) with one capacitor. The single-direction-balance mode or bi-direction-balance mode based multilevel inverter is presented in Fig 1(b) [18], where each cell requires four power switches with one capacitor followed by H-bridge configuration. Another interesting topology with three active switching devices in each switching cell is proposed in [9] as shown in Fig. 1(c). Two of the active devices are replaced by diode in a new configuration in [19] as shown in Fig. 1(d). The reduction in active switching devices in [19] is penalized by the higher voltage stress on the semiconductor in the successive cells. Similarly, a large number of semiconductors and higher voltage stress on the devices in [4] and [13] as shown in Fig. 1(e) and Fig. 1(f) respectively make it less suitable for industrial applications. All the mentioned topologies share the same drawback of hard-charging of the switched-capacitors, which produces high inrush-current leading to high current stress on components that degrades their performance and reliability. Fig. 1(g) shows the equivalent circuit of the switched-capacitor inverter hard-charging current loop. Moreover, the capacitor charging current loops are highlighted with red color lines in all the topologies in Fig. 1. To overcome the issue of inrush current, a switched-capacitor multilevel inverter with quasi-resonant charging is presented in [20] [21]. A resonant inductor (L_r) is utilized in this circuit to realize a soft-charging current path for the capacitors.

Fig. 2(c) shows the equivalent circuit of this inverter with soft-charging current loop for the capacitors. However, the major disadvantage of the circuit [20] is that it is not capable to boost the input voltage, i.e. the peak of the DC-link voltage is equal to the input voltage. Also, the capacitors in the succeeding cell are charging from the capacitors in the antecedent cells, which increases the inter-module charging (inrush) current [21]. Table I summarizes the basic switching cell of various conventional topologies.

The initiative of this paper is to propose an alternative multilevel inverter with voltage-boosting capability and generation of $(2n+1)$ voltage levels, where $n \geq 2$ is the number of switching cells. The proposed inverter consists of three parts, a DC-DC converter at the front end to boost the input source voltage followed by an SC cell to synthesize different voltage levels, and a 2-level H-bridge voltage source inverter (VSI) at the end to invert the DC to AC waveform. The operating principle is based on a variable DC-link voltage generation, which is shared by H-bridge at the output inverter stage. The variable DC-link is generated by a multi-cell arrangement of DC-switched capacitor cells, where several DC-cells at the DC-link can increase the number of voltage levels generated at the AC side, without proportionally increasing the number of active and passive devices. Moreover, the charging of capacitors is realized through a quasi-resonant current path that allows low current stress soft charging. In particular, the paper explores the details of a 5-level configuration using one switching cell and a 2-level VSI output stage. A small LC filter is required at the output to obtain the pure sinusoidal waveform. Compared to previous similar topologies, the proposed inverter requires lower voltage rated devices and can provide the boosting feature with high conversion efficiency and power density.

The rest of this paper is organized as follows. Section II introduces the general structure of the $(2n+1)$-level inverter followed by an implementation example of 5-level inverter with its modulation and capacitor charge balance strategy. Section III demonstrates the implementation of 5-level and 7-level topologies with comparison. Both the simulation and experimental results of an example 5-level and 7-level inverter are provided in Section IV to verify the performance and efficacy of the circuits, and the paper is finally concluded in Section VI.
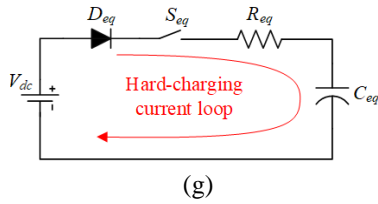

(c)

(d)

(e)

(f)

(a)

(b)

(g)
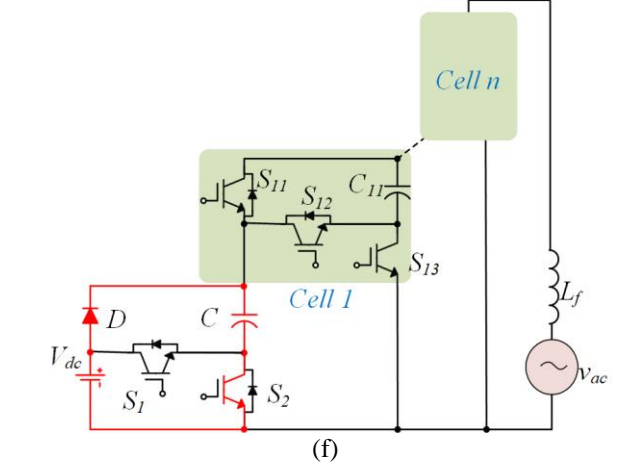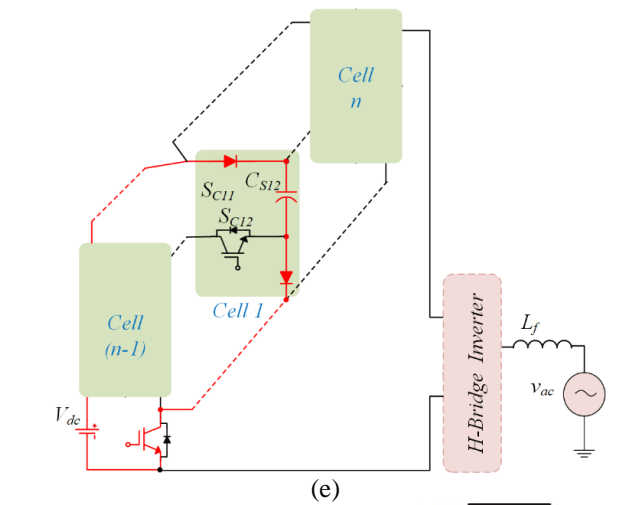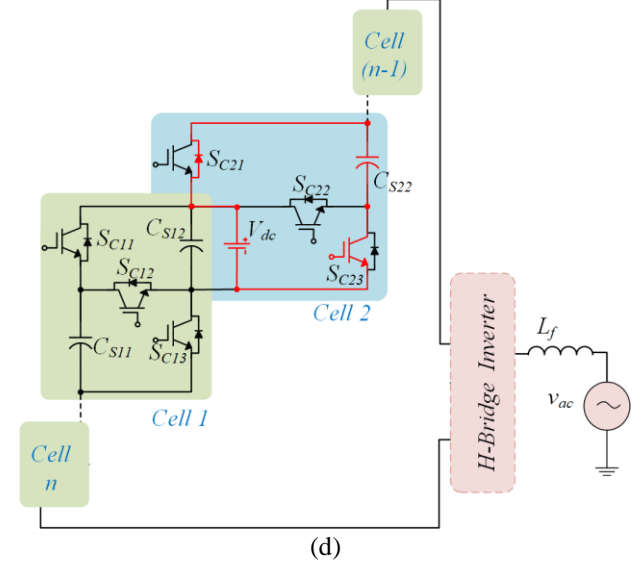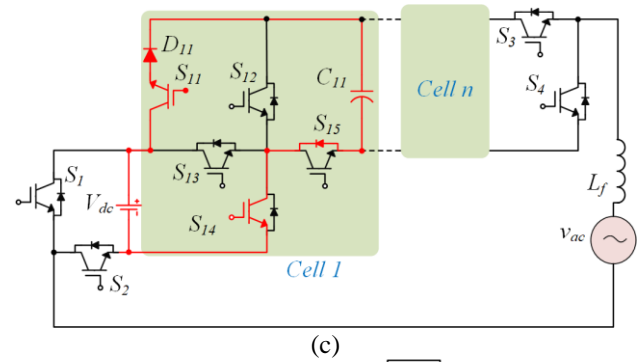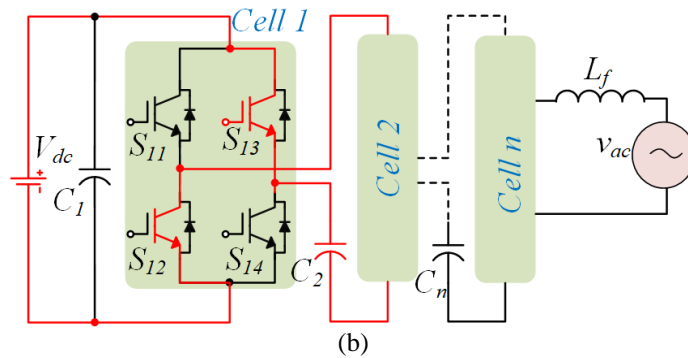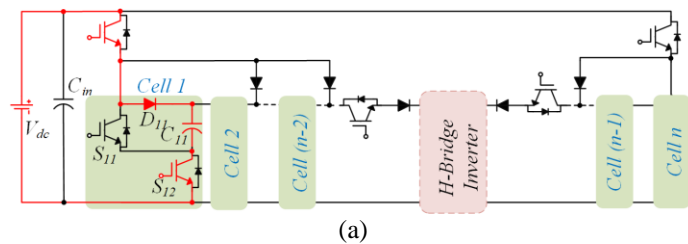
Fig. 1. The topology of switched-capacitor multilevel inverters: (a)-(f) high-inrush and hard-charging current-loop, and (g) the equivalent circuit with hard-charging current loop.
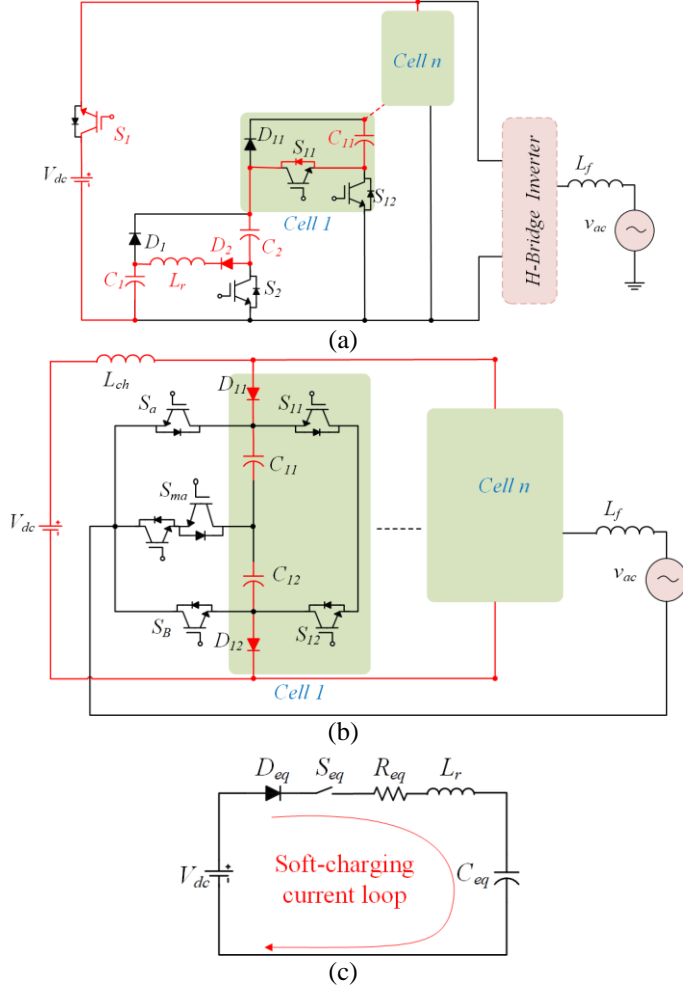

(a)

(b)

(c)

Fig. 2. The topology of switched-capacitor multilevel inverter (a) quasi-resonant charging current and soft-charging current-loop of the topology in [20], (b) soft-charging loop of the topology in [21], and (c) the equivalent circuit with soft-charging current loop.

II. PROPOSED (2N+1)-LEVEL INVERTER

A. Circuit description

The proposed variable DC-link multilevel inverter is a modular multicell structure similar to the FCC or CHB, where it is possible to increase/decrease the number of levels by connecting/disconnecting the basic switching cell units following the multicell arrangement. Fig. 3 shows the generic circuit of the proposed converter to generate (2n+1) levels in the output voltage. Each cell consists of three active switches and two capacitors and represents two extra voltage levels ($V_{C1} = V_C$ or $V_{C2} = V_C$ and $V_{C1} + V_{C2} = 2\,V_C$). However, the number of capacitors in the succeeding cell is one less than that of the antecedent cells, as one of the capacitors is shared between the cells. Hence, the total number of switches and capacitors for (2n+1)-level inverter is 3(n-1) and n respectively. Their allowed

switching states provide a path to connect the capacitor of each cell in such a way that it adds or bypasses the capacitor voltage, which is pre-charged through a boost DC-DC converter at the front side. This creates a variable DC-link voltage across P and N, which is fed to the 2-level VSI at the output side. Combinations of several SC-cells at the DC-link can increase/decrease the number of voltage levels generated at the AC side, without increasing the number of active devices proportionally to the three phases. In addition, the output voltage can be regulated to a suitable AC voltage regardless of the drop in the input voltage from the source such as renewable energy (PV panel, small wind turbine or fuel cells). As seen from Table I, only the proposed cell provides duty cycle (D_b) combined SC voltage for inverter voltage levels, with quasi-resonant capacitor charging.

The equivalent circuit of the proposed multilevel inverter is shown in Fig. 4. The inductor L_B in the front boost converter also serves as a quasi-resonant inductor to charge the capacitors C_{S11}~C_{Sn2} in different modes of operation. Here, R_{eq} is the equivalent resistance of the circuit consisting of ON resistance of the switches ($R_{DS,on}$), series resistance of diodes and equivalent series resistance (ESR) of capacitors, and S_{eq} is the equivalent of switch(es) in series with the capacitor(s). All capacitors are considered to be identical with equal capacitance value and ESR. Similarly, all the switches are identical with the same voltage and current rating and same $R_{DS,on}$. Hence, unlike conventional topologies where the rating of devices in the successive cells is higher than that of the antecedent cells, the rating of all devices is same in the proposed topology.

To simplify the circuit analysis, the following conditions are assumed:
1) Capacitors C_{S11}, C_{S12}, …, $C_{S(n-1)n}$ are large enough to keep V_{Cs11}, V_{Cs12}, …, $V_{Cs(n-1)n}$ constant in one switching period.
2) The power MOSFET and diodes are treated as ideal. The ON-state resistance R_{DS-on} and parasitic capacitances of the switches are neglected. In addition, the forward voltage drops of the diode is ignored.
3) ESRs of all the capacitors are neglected.

B. Circuit Operation

The operating principle of the proposed (2n+1)-level inverter is illustrated in Fig. 5. The operating principle is based on the generation of a variable DC-link voltage using the switched capacitor cells. Here, each capacitor in each switching cells is charged up to V_C, where

$$V_{CS11} = V_{CS12} = ... = V_{SC(n-1)1} = V_{SC(n-1)2} = V_C = \frac{V_{dc}}{1-D_b} \quad (1)$$

Since there are two capacitors in each cell and every cell has two allowed switching states, the peak voltage across each cell in each switching state is

$$\hat{V}_{cell} = \begin{cases} V_C = \frac{V_{dc}}{1-D_b}, & S_{C(n-1)1} = S_{C(n-1)3} = 1 \ and \ S_{C(n-1)2} = 0 \\ 2V_C = \frac{2V_{dc}}{1-D_b}, & S_{C(n-1)1} = S_{C(n-1)3} = 0 \ and \ S_{C(n-1)2} = 1 \end{cases} \quad (2)$$

where, $S_{Cni} = 1$ means that the ith switch on cell n is ON and $S_{Cni} = 0$ means that it is OFF.

Fig. 5 shows a selection of the n different DC-link level generation possibilities. In Fig. 5(a) and Fig. 5(b), all the capacitors are charging and discharging in parallel, respectively.

TABLE I
SUMMARY OF BASIC SWITCHING CELLS IN VARIOUS SWITCHED-CAPACITOR TYPE MULTILEVEL INVERTERS.

| Switching cell	No. of components in each switching cell				Max. cell voltage	Charging type
	Capacitor	Diode	Switch	Inductor		
Fig. 1(a) [10]	1	1	2	0	V_{dc}	Hard-charging
Fig. 1(b) [18]	1	0	4	0	V_{dc}	Hard-charging
Fig. 1(c) [9]	1	1	5	0	$2V_{dc}$	Hard-charging
Fig. 1(d) [19]	2	0	3	0	$2V_{dc}$	Hard-charging
Fig. 1(e) [4]	1	2	1	0	V_{dc}	Hard-charging
Fig. 1(f) [13]	1	1	2	0	$2^n V_{dc}$	Hard-charging
Fig. 2(a) [20]	1	1	2	1	V_{dc}/n	Soft-charging
Fig. 2 (b) [21]	2	2	2	1	$2^n V_{dc}$	Soft-charging
Proposed in Fig. 3	2	0	3	1	$2V_{dc}/(1-D_b)$	Soft-charging
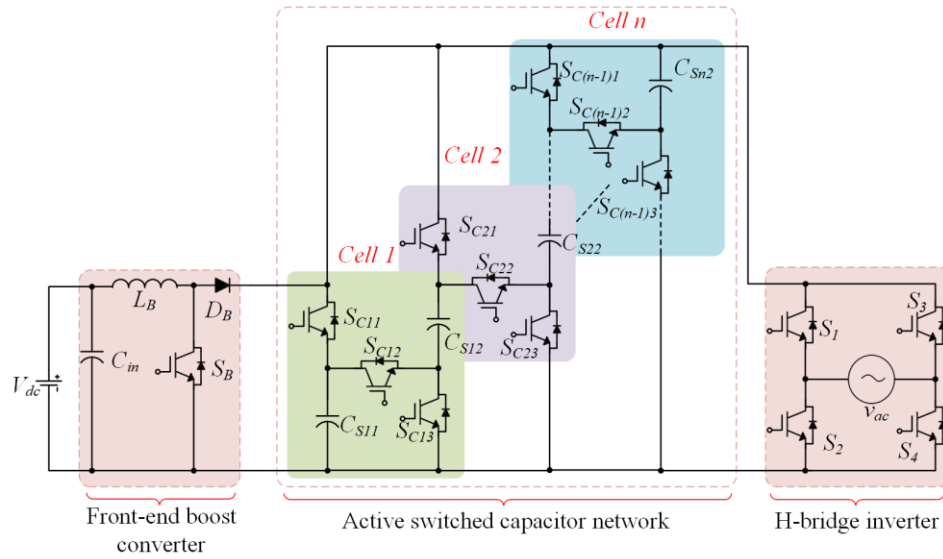
Fig. 3. Circuit diagram of the proposed ($2n$+1)-level inverter.

In this mode, the switches S_{Cn1} and S_{Cn3} are ON, whereas S_{Cn2} are turned OFF to connect all the capacitors in parallel, and the equivalent capacitance in this mode is $C_{eq} = \sum_{i=1}^{n} C_{si1}$. The peak voltage across PN and the AC output is $\hat{V}_{PN} = V_C$ and $\hat{v}_{ac} = \mp V_C$ respectively. The next level of voltage is generated by turning ON the switch S_{Cn2} sequentially to combine the capacitor voltages, where $\hat{V}_{PN} = V_{CS11} + V_{CS12} = 2V_C$ and $\hat{v}_{ac} = \mp 2V_C$. Similarly, the maximum peak voltage across the DC-link is created by turning ON S_{Cn2} and turning off rest of the switches. In general, the peak of DC-link voltage is given as:

$$\hat{V}_{PN} = \frac{n V_{dc}}{1 - D_b}. \tag{3}$$

TABLE II
SWITCHING STATES AND CORRESPONDING OUTPUT VOLTAGE LEVEL SHOWING CAPACITOR STATE.

Reference/ Switching State	Voltage level	Max. output voltage ($\hat{v}_{ac}$) (For M = 1.0)	Cell 1			Cell 2			...	Cell n			H-Bridge				Impact on capacitor voltage
			S_{C11}	S_{C12}	S_{C13}	S_{C21}	S_{C22}	S_{C23}	...	S_{Cn1}	S_{Cn2}	S_{Cn3}	S_1	S_2	S_3	S_4	
Fig. 5(a)	∓ 1	$-V_C$	1	0	1	1	0	1	...	1	0	1	1	0	0	1	↑
A		$+V_C$											0	1	1	0	↑
Fig. 5(b)		$-V_C$	1	0	1	1	0	1	...	1	0	1	1	0	0	1	↑
B		$+V_C$											0	1	1	0	↑
Fig. 5(c)	∓ 2	$-2V_C$	0	1	0	1	0	1	...	0	1	0	1	0	0	1	↓
C		$+2V_C$											0	1	1	0	
Fig.5(d)	∓ 3	$-3V_C$	0	1	0	0	1	0	...	1	0	0	1	0	0	1	↓
D		$+3V_C$											0	1	1	0	
Fig. 5(e)	$\mp n$	$-nV_C$	0	1	0	0	1	0	...	0	1	0	1	0	0	1	↓
N		$+nV_C$											0	1	1	0	
Fig. 5(f)		0 V	1	0	1	1	0	1	...	1	0	1	1	0	1	0	↑
Z	∓ 0	0 V	1	0	1	1	0	1	...	1	0	1	0	1	0	1	↑

Note: "↓" means discharging of capacitor; "↑" means charging of capacitors.
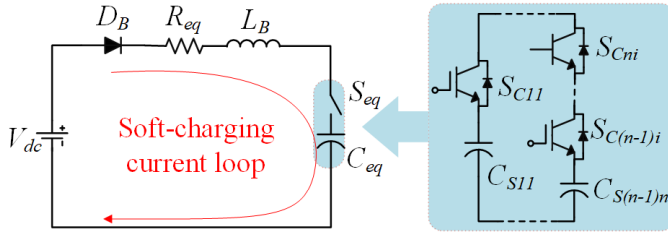
Fig. 4. Equivalent circuit of the proposed multilevel inverter with soft-charging current loop.

where M is the modulation index and is defined as the ratio of the peak of sinusoidal reference to the total peak-to-peak voltage of the two triangular carriers. Therefore, the maximum voltage gain of the proposed topology is the product of the gain of pre-boost converter and the gain of the switched capacitor network.

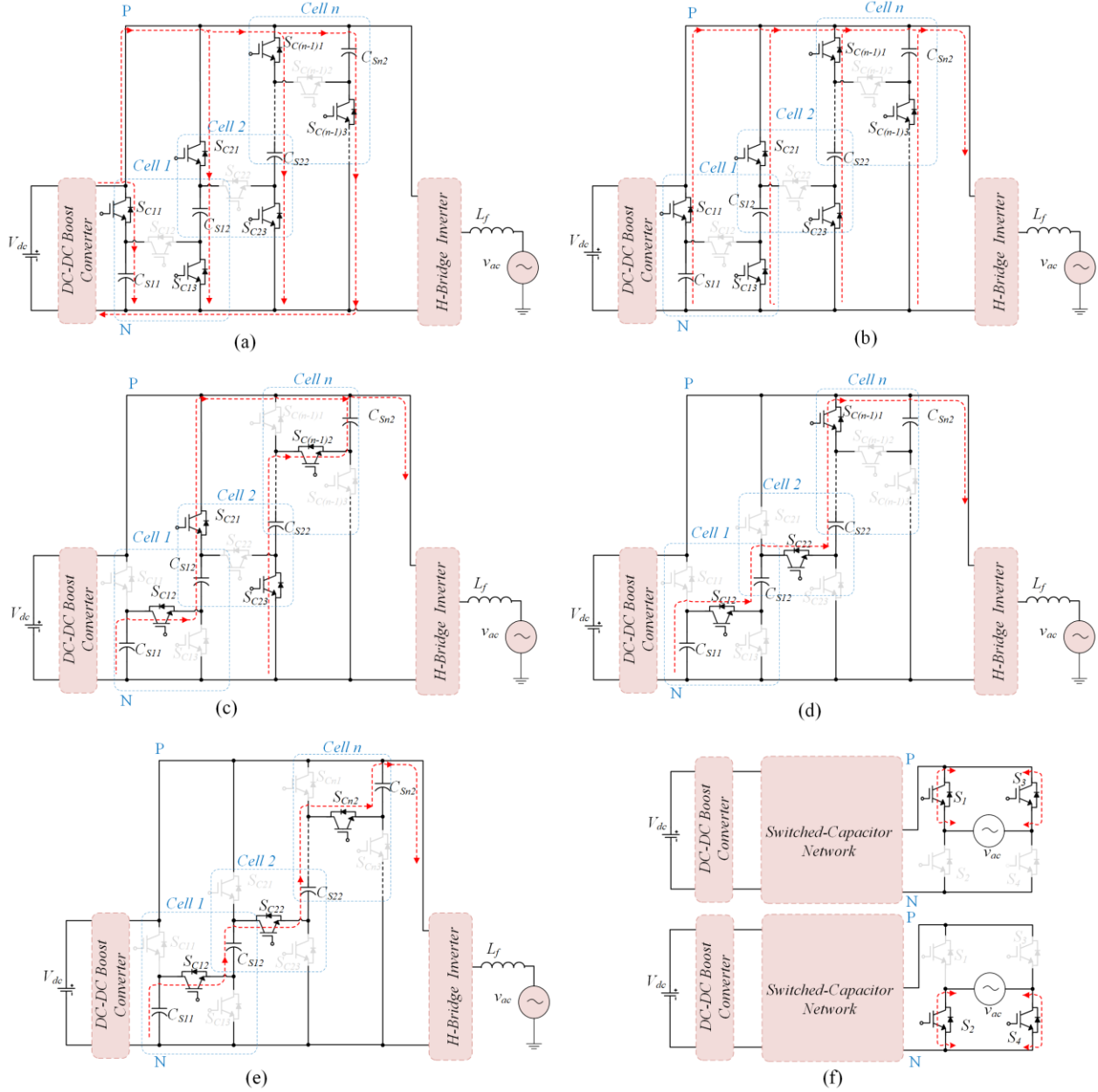$$\frac{\hat{v}_{ac}}{V_{dc}} = G = \frac{nM}{1-D_b} \qquad (5)$$

Fig. 5. Illustration of principle of operation: (a) capacitor charging in parallel $\hat{V}_{PN} = V_C$ and $\hat{v}_{ac} = \mp V_C$, (b) level 1 to create $\hat{V}_{PN} = V_C$ and $\hat{v}_{ac} = \mp V_C$, (c) level 2 to create $\hat{V}_{PN} = 2V_C$ and $\hat{v}_{ac} = \mp 2V_C$, (d) level 3 to create $\hat{V}_{PN} = 3V_C$ and $\hat{v}_{ac} = \mp 3V_C$, (e) level n to create $\hat{V}_{PN} = nV_C$ and $\hat{v}_{ac} = \mp nV_C$, and (f) H-bridge to create $\hat{v}_{ac} = 0\,V$.

The zero state in the circuit is created by turning ON the upper switches (S_1 and S_3) or lower switches (S_2 and S_4) of the H-bridge. The details of the switching states of the converter are also presented in Table II.

Using (3), the peak of the AC output voltage of the $(2n+1)$-level inverter is

$$\hat{v}_{ac} = MV_{PN} = \frac{nM\,V_{dc}}{1-D_b} \qquad (4)$$

III. IMPLEMENTATION AND COMPARISONS

This section explores the 5-level and 7-level as an example configuration and compares them with the conventional topologies. The details of the analysis and implementation are presented as follows:

A. 5-level inverter implementation (n = 2)

Fig. 6 shows the implemented 5-level inverter with possible switching states. It consists of a front side boost DC-DC converter, one switching cell ($n = 2$) and a 2-level VSI at the output stage. The SC has two switching states as shown in Fig. 6 (b) and (c) to create level ∓1 ($\hat{V}_{PN} = V_C$ across PN and $\hat{v}_{ac} = \mp V_C$ at the output of the H-bridge) and level ∓2 ($\hat{V}_{PN} = 2V_C$ across PN and $\hat{v}_{ac} = \mp2V_C$ at the output of the H-bridge).
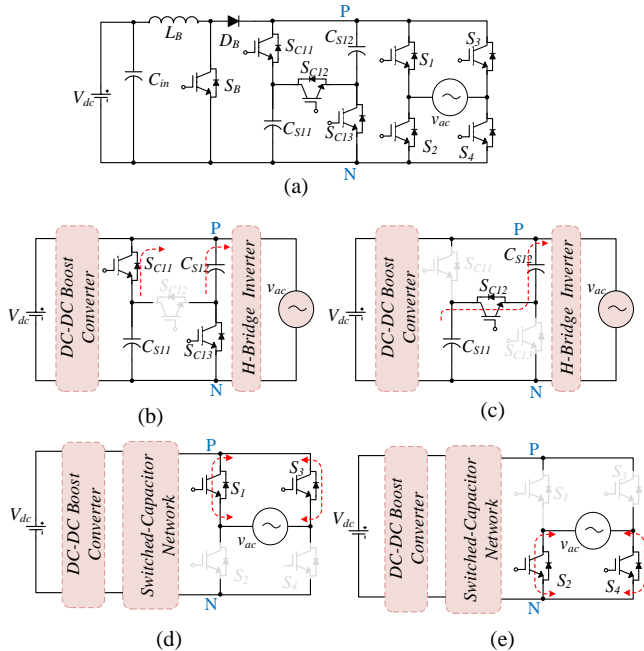

Fig. 6. (a) An example of the 5-level ($n = 2$) inverter implementation with its operating modes (b) state A or B [∓1] to create $\hat{V}_{PN} = V_C$ and $\hat{v}_{ac} = \mp V_C$, (c) state C [∓2] to create $\hat{V}_{PN} = 2V_C$ and $\hat{v}_{ac} = \mp2V_C$, (d)&(e) state Z [∓0] to create $\hat{v}_{ac} = 0\,V$.
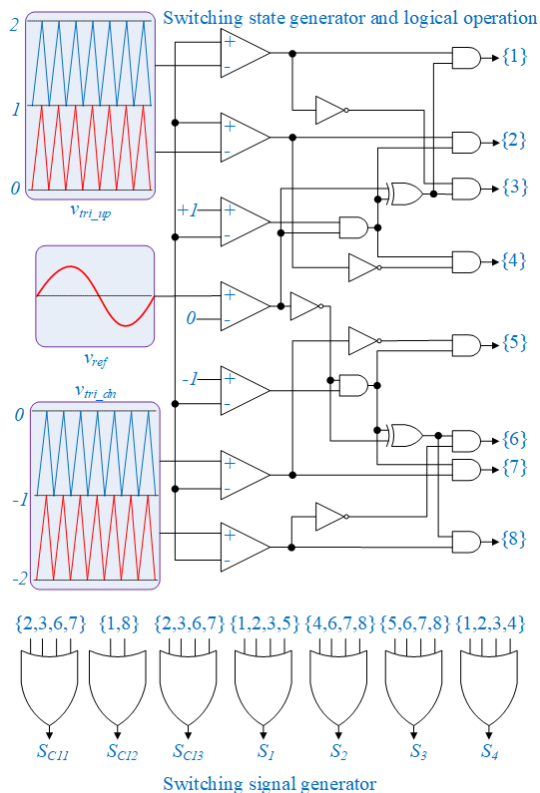

Fig. 7. An example of sinusoidal pulse width modulator implementation for 5-level inverter.

The additional zero states are created by the H-bridge VSI as shown in Fig. 6 (d) and (e). The capacitors C_{S11} and C_{S12} charges through the input voltage in parallel (Fig. 6 (b), (d) and (e)) to ensure their voltage balancing and discharges to the load in Fig. 6 (b) and (c) to create ∓1 and ∓2 voltage levels.

The inverter is controlled by a level-shifted sinusoidal pulse-width modulation (LS-SPWM) as depicted in Fig. 7.

A sinusoidal reference (v_{ref}) is compared with two level-shifted triangular carriers ($\hat{v}_{tri}$) for switching states computation, followed by a combinational logic circuit, which is used to compute switching signals for each power switch. For a 5-level circuit, the peak of fundamental AC output voltage is

$$\hat{v}_{ac} = M V_{PN} = \frac{2M\,V_{dc}}{1 - D_b} \tag{6}$$

From this, the maximum peak of fundamental output voltage of 5-level inverter is equal to the DC-link voltage $V_{PN} = 2\,V_{dc}/(1 - D_b)$ at $M = 1.0$.

B. 7-level inverter implementation (n = 3)

Combinations of two SC-cells at the DC-link increase the number of voltage levels from 5 levels ($n = 2$) to 7 levels ($n = 3$) generated at the AC side without increasing the number of active devices proportionally. The implemented 7-level inverter is shown in Fig. 8 with all possible switching states. The SC has four switching states as shown in Fig. 8(b)-(e) to create level ∓1, ∓2 and ∓3 at the output voltage levels. Fig. 8(b) shows ∓1 level, where all the capacitors are connected in parallel to generate $\hat{V}_{PN} = V_C$ across PN and $\hat{v}_{ac} = \mp V_C$ at the output of the H-bridge.
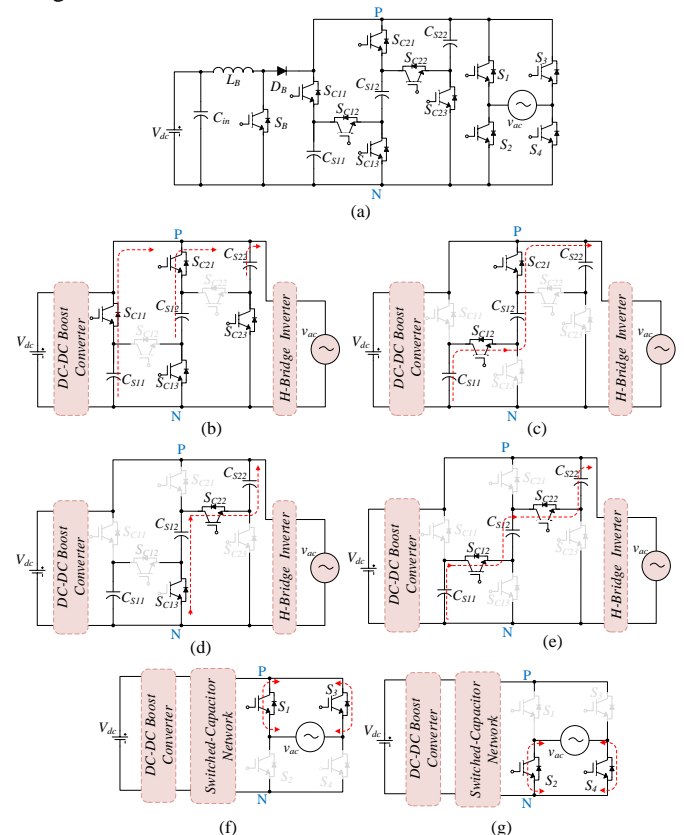
Fig. 8. (a) An example of the 7-level ($n = 3$) inverter implementation with its operating modes (b) level 1 to create $\hat{V}_{PN} = V_C$ and $\hat{v}_{ac} = \mp V_C$, (c), & (d) level 2 to create $\hat{V}_{PN} = 2V_C$ and $\hat{v}_{ac} = \mp2V_C$, (e) level 3 to create $\hat{V}_{PN} = 3V_C$ and $\hat{v}_{ac} = \mp3V_C$, (f)&(g) state Z [∓0] to create $\hat{v}_{ac} = 0\,V$.

There are two redundant switching states to create ∓2 as shown in Fig. 8(c) and Fig. 8(d), where two capacitors are connected in series to generate $\hat{V}_{PN} = 2V_C$ across PN and $\hat{v}_{ac} =$

$\mp 2V_C$ at the output of the H-bridge. Level 3 is created by adding the voltage of all the capacitors in series to generate $\hat{V}_{PN} = 3V_C$ across PN and $\hat{v}_{ac} = \mp 3V_C$ at the output of the H-bridge. The additional zero states are created by the H-bridge VSI as discussed before. Similar LS-SPWM as shown in Fig. 7 can be implemented for 7-level as well to control the capacitor and output voltages during the different switching states.

C. Comparative Summary

The foremost challenging issue for multilevel inverter topologies is related to the number of passive and active components and their voltage/current ratings. To compare the proposed topology with the conventional SC based multilevel inverter topologies, a comparative summary is provided in Table III. The comparison is done considering the required semiconductor devices and SCs for each multilevel inverter. Furthermore, the number of output voltage levels as well as the peak AC output voltage are compared. The voltage stress of components in conventional topologies has a proportional or an exponential relationship with the DC input voltage, however, compared to other topologies, the voltage stress is equal or lower in the proposed topology for the same level of voltages. Moreover, due to voltage gain increasing feature of the proposed topology, the voltage stress and peak AC output voltage are dependent on the boost duty cycle. Moreover, the required passive components and semiconductor devices are less or equal to the components in conventional topologies. For example, considering the same voltage gain ($D_b = 0$) for a 5-level configuration, the maximum switch voltage stress and the switched capacitor voltage stress of the proposed topology is V_{dc} which is equal or lower than other topologies. Finally, the proposed topology features the capability of quasi-resonant charging of the capacitors (soft-charging), which results in reducing the current spike on the devices and thus enhances the performance by increasing the reliability and lifetime of the inverter.

the voltage and current rating of the selected semiconductor devices are 650 V and above 50 A accordingly.

To select the components of the proposed inverter, a few more things need to be calculated such as boost inductor (L_B), Switched-capacitors (C_{Sn2}) and the output filter (L_f, and C_f).

The following parameters are considered for practical design: the switching frequency (f_s) of the inverter is 20 kHz, input voltage (V_{in}) is 100-150 V, forward voltage (V_D) of the diode (C5D50065D) is 1.8 V, modulation index (M) is 0.90, the DC-link voltage (V_{PN}) is 400 V. As the operation of the boost converter in the discontinuous conduction mode (DCM) is load dependant and the power loss in the boot inductor is high due to large current ripples, only the continuous conduction mode (CCM) operation is considered here and the maximum input current ripple is selected 40% of the average input value. Moreover, a large inductance value in CCM operation helps to alleviate the inrush current problem in the capacitor charging loop to a higher extent.

The boost inductor can be calculated using (7), which depends on the desired input current ripple (ΔI_{in}), minimum input voltage (V_{in_min}) and output voltage of the boost converter (V_{PN}). Using (7), the boost inductor value can be found.

$$L_B \geq \frac{V_{in\_min} \times (V_{PN} + V_D - V_{in\_min})}{\Delta I_{in} \times f_{sw} \times (V_{PN} + V_D)} \quad (7)$$

The switched-capacitor C_{Sn2} can be calculated by (8) which is dependent on the total capacitor discharging value (Q_N) and the permissible voltage ripple across the applied input voltage (ΔV_{in}) of the system.

$$C_{Sn2} \geq \frac{Q_N}{\Delta V_{in} V_{in}} \quad (8)$$

The selection criteria mentioned here are for voltage source type inverters that only need filter inductor at the output to provide filtering for the output waveform. However, to reduce the inductor size, usually a capacitor is used in parallel with the load, and hence, the solution here would be similar to the use of a low

TABLE III
COMPARISON OF BASIC PARAMETERS IN VARIOUS SWITCHED-CAPACITOR TYPE MULTILEVEL INVERTER.

Referred Topology	No. of components				Output voltage levels	Peak of AC output voltage ($\hat{v}_{ac}$)	Voltage stress on				Inrush/ spike current
							Switched capacitor n/w			H-bridge switch	
	C	D	S	L			C	S	D		
[10]	$4(n-1)$	$2(3n-1)$	$8n$	0	$2n+1$	$\mp(n-1)V_{dc}$	$(n-1)V_{dc}/n$	$(n-1)V_{dc}/n$	$(n-1)V_{dc}/n$	$(n-1)V_{dc}$	Yes
[18]	$n-1$	0	$4n$	0	2^n+1	$\mp 2^{n-1}V_{dc}$	$2^{n-1}V_{dc}/n$	$2^{n-1}V_{dc}/n$	NA	$2^{n-1}V_{dc}$	Yes
[9]	$n-1$	$n-1$	$5n-1$	0	$2n+1$	$\mp(n+1)V_{dc}$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}/n$	NA	Yes
[19]	$n-1$	0	$3n+1$	0	$4n-1$	$\mp(n+1)V_{dc}$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}/n$	NA	$(n+1)V_{dc}$	Yes
[4]	$n-1$	$2n-2$	$6(n-1)$	0	$2n+1$	$\mp(n+1)V_{dc}$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}$	Yes
[13]	$n-1$	$n-1$	$3n-1$	0	2^n	$\mp 2^n V_{dc}$	$2^n V_{dc}/n$	$2^n V_{dc}/n$	$2^n V_{dc}/n$	$2^n V_{dc}$	Yes
[20]	n	n	$2(n+1)$	1	$2n+1$	$\mp V_{dc}$	V_{dc}/n	V_{dc}/n	V_{dc}/n	V_{dc}	No
[21]	$2n$	$2n$	$3n+1$	1	$2^{n+1}+1$	$\mp 2^n V_{dc}$	$2^n V_{dc}/n$	$2^n V_{dc}/n$	$2^n V_{dc}/n$	NA	No
[22]	$n-1$	$n-1$	$2n+3$	0	$2n+1$	$\mp(n+1)V_{dc}$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}$	Yes
[23]	$n-1$	1	$3n+1$	0	2^n	$\mp 2^n V_{dc}$	$2^n V_{dc}/n$	$2^n V_{dc}/n$	NA	$2^n V_{dc}$	Yes
Proposed	n	1	$3n+2$	1	$2n+1$	$\mp n V_{dc}/(1-D_b)$	$V_{dc}/(1-D_b)$	$(n-1)V_{dc}/(1-D_b)$	NA	$V_{dc}/(1-D_b)$	No

IV. COMPONENT SELECTION GUIDELINES

A component selection guideline at the end is helpful in estimation and selection of the parameters for the practical design. First of all, the voltage and current rating of the active switches and diodes must be selected just above the safety margin. Even though the input DC-link capacitor helps to maintain a constant voltage at the DC-link, there are some small spikes in practice across the semiconductor devices. As a result,

pass LC filter. Fig. 9 shows the waveform of output current ripple factor (ΔI_{factor}) for a selected modulation index (M) to obtain the maximum ripple factor which helps to calculate the filter inductor value by (10). The maximum ripple factor is approximately 0.25 which, applied in (10) together with a ripple across the inductor of 40%, calculates the required inductance.

$$\Delta I_{Factor} = M \sin(2\pi f_m t) - M^2 \sin^2(2\pi f_m t) \quad (9)$$

where f_m is the fundamental frequency.

$$L_f = \frac{v_{ac} \times \Delta I_{Factor}}{f_s \times \Delta I_{Lf}} \qquad (10)$$

On the other hand, the filter capacitor (C_f) can be calculated by (11) where the cut-off frequency (f_c) is set to be 10% of f_s.

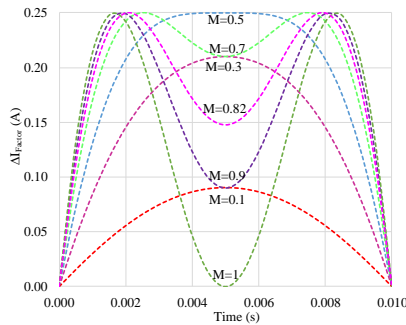$$C_f = \frac{1}{4 \times \pi^2 \times f_c^2 \times L_1} \qquad (11)$$

Fig. 9. ΔI_{factor} waveform to highlight the maximum ripple factor.

V. SIMULATION AND EXPERIMENTAL RESULTS

The performance of the proposed topology is first simulated in MATLAB-Simulink using the PLECS toolbox and then verified experimentally with a 500 VA laboratory prototype.

TABLE IV
PARAMETERS AND COMPONENTS USED FOR SIMULATION AND MEASUREMENT.

Description	Value/Parameter Used
Input voltage (V_{in})	100-150 V
Output voltage (v_{ac})	230 V
Power rating (P_O)	500 VA
Carrier frequency (f_s)	20 kHz
Line frequency (f)	50 Hz
DC-link capacitor (C_1 & C_2)	680 μF, 250 V
Boost inductor (L_B)	0.9 mH
Filter inductor (L_f) & capacitor (C_f)	0.68 mH & 4.7 μF
Switches S_B, ($S_{C11} - S_{C13}$) and ($S_1 - S_4$)	SCT3022AL
Boost diode (D_B)	C5D50065D
Load (resistor and inductor)	500 VA (90-110 Ω, 150 mH)
Controller	sb-RIO GPIC
Dead time	300 ns

(a)

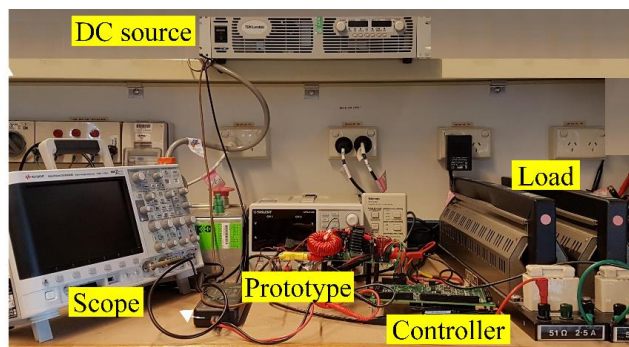(b)   (c)

Fig. 10. Prototype and measurement platform of 5-level inverter: (a) test setup, (b) top view of the inverter and (c) bottom view of the inverter.

In order to precisely verify the performance of the proposed inverter and to have a fair comparison, the same parameters are used as listed in Table V for both the simulation and experiment. A picture showing the implemented 5-level inverter with measurement setup is shown in Fig. 10. SB-RIO GPIC with LabVIEW software was used to control and modulate the converter. The input voltage V_{in} was variable from 100 V to 150 V, which is pre-boosted to ≈ 200 V (voltage across the switch capacitor) to produce 230 V ac at the output of the inverter, which technically can be achieved by varying the duty ratio of the boost switch S_B.
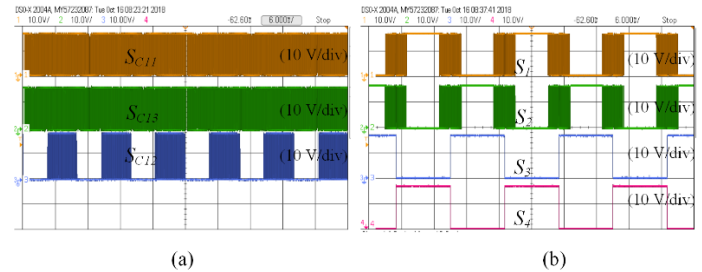

(a)   (b)

Fig. 11. Measured gate signals: (a) active switch capacitor network switches (S_{C11}, S_{C12} and S_{C13}), and (b) H-bridge switches ($S_1 - S_4$).
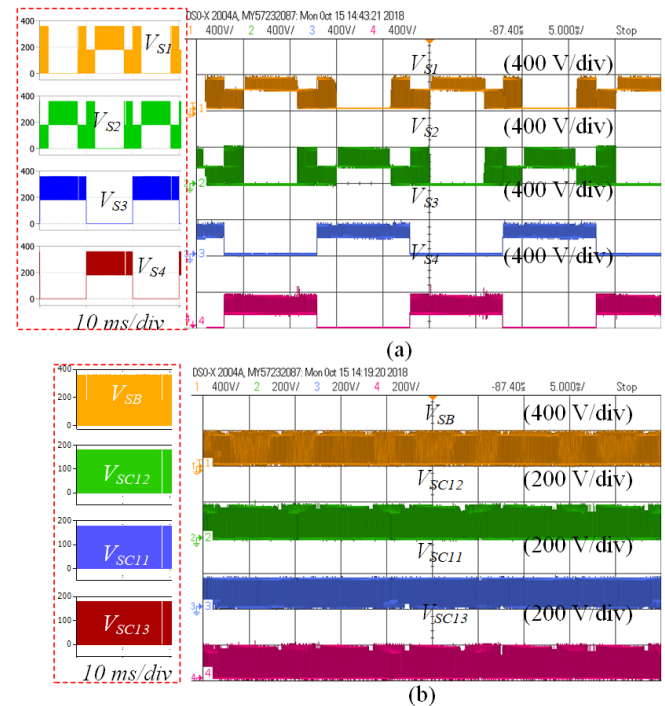

(a)

(b)

Fig. 12. Voltage stress on switches: (a) simulated and measured voltage stress on switches S_B, S_{C12}, S_{C11}, and S_{C13}, and (b) simulated and measured voltage stress on H-bridge switches ($S_1 - S_4$).

The switch capacitor circuit boost the DC-link voltage to make it ≈ $2 \times 200\ V = 400$ V, which is required to produce 230 V ($230 \times \sqrt{2} /M)V$. Details of simulation and experimental results are systematically presented as follows.

Fig. 11 shows the pulse-width modulation signals generated for all switches in active switch capacitor network (S_{C11}, S_{C12} and S_{C13}) and the H-bridge ($S_1 - S_4$). Fig. 12 to Fig. 15 shows the waveforms of the inverter when the input voltage is 140V. The corresponding voltage stress on switches are illustrated in Fig. 12.

The voltage stress on the switch in the switch capacitor network is half of the H-bridge circuit switches. Hence, the maximum voltage stress on the switch is 400 V for all switches

in the H-bridge and 200 V for the switches in the switched capacitor network.

Fig. 13 shows the waveform of the input voltage and the DC-link capacitor voltages. The variable DC-link voltage (V_{PN}) level is created by the step-up converter, where the magnitude of the SC voltage is dependent on the duty cycle (D_b) of the pre-boost converter. The input voltage of 140 V is pre-boost to 192 V (using $D_b = 0.3$) across the DC-link capacitors as shown in Ch3 and Ch4 of the measured waveform. The measured peak-to-peak voltage ripple of the SC is 8 V (8 V/192 V = 5%) and they are self-balanced due to the parallel operation of the switching network. Using this capacitor voltage, the SC generates the variable voltage of 192 V and 384 V across P and N in steps (Ch2).
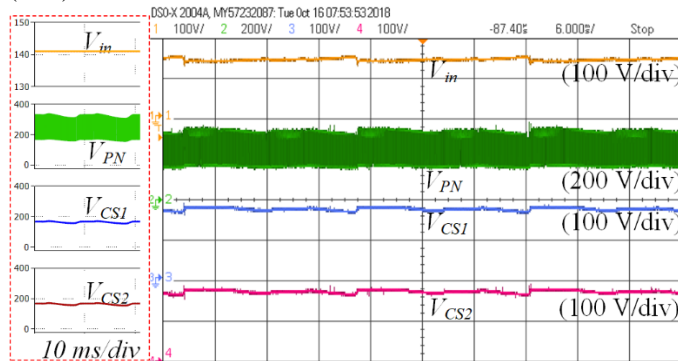

Fig. 13. The input voltage, DC-link voltage, voltage across the switched-capacitors: (a) simulation waveform, and (b) corresponding experimental waveform.
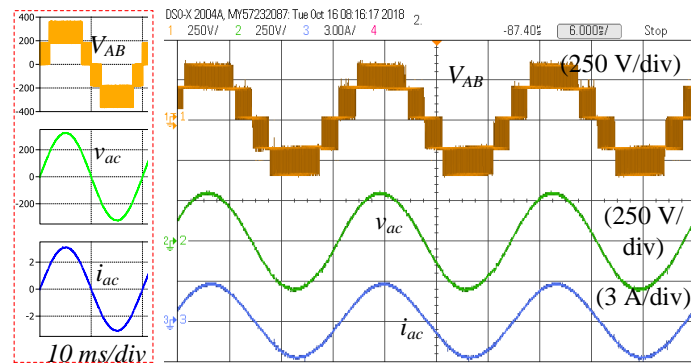

Fig. 14. The inverter voltage without filter, output voltage and current after the LC filter for resistive (R) load: (a) simulation waveform, and (b) corresponding experimental waveform.
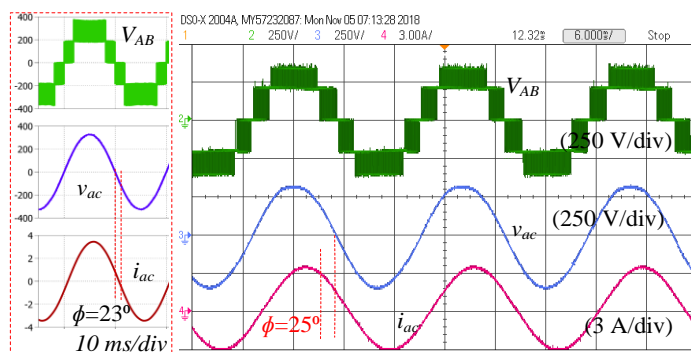

Fig. 15. 5-level voltage and voltage and current after the LC filter output voltage in reactive power condition (cos φ = 0.9): (a) simulation waveform, and (b) corresponding experimental waveform.

Fig. 14 shows the inverter input/output voltage and current waveforms with clear five levels in the output voltage with a clear sinusoidal output voltage and current. The RMS value of the output voltage and current is 230 V and 2.3 A. The reactive

power operation mode is also tested as shown in Fig. 15 with a power factor of 0.9 (inductive). The inverter still produces good-quality voltage and current waveforms without high distortion (THD < 2.1 %).
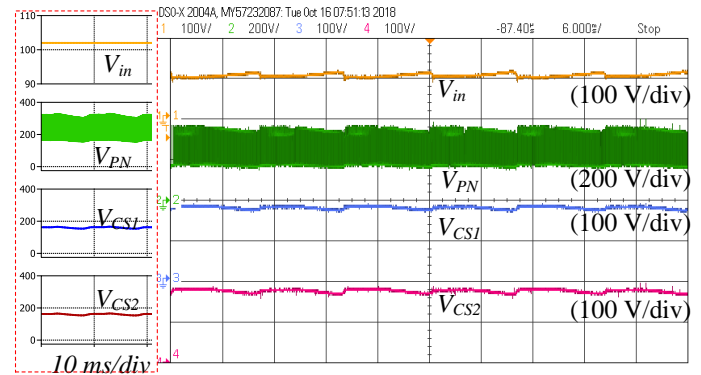

Fig. 16. The input voltage, DC-link voltage, voltage across the switched-capacitors: (a) simulation waveform, and (b) corresponding experimental waveform.
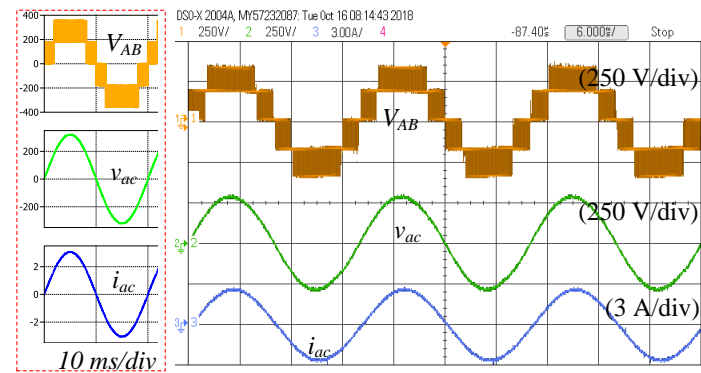

Fig. 17. The inverter voltage without filter, output voltage and current after the LC filter for resistive (R) load: (a) simulation waveform, and (b) corresponding experimental waveform.
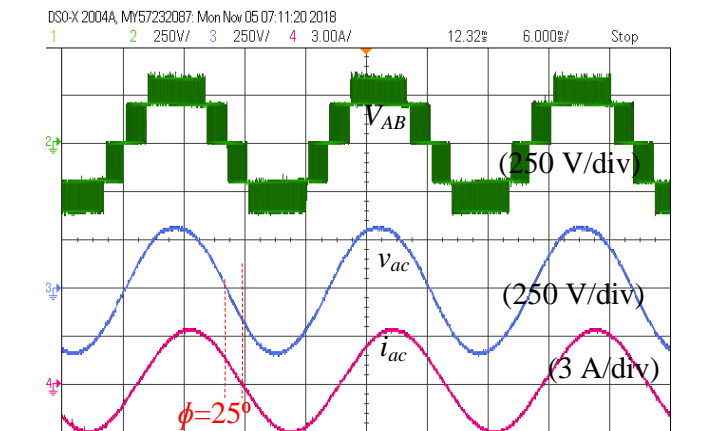

Fig. 18. Measured waveforms at φ = 25º showing inverter input/output voltage and current waveforms.

Further, to illustrate the benefits of the proposed topology in a wide input voltage range, a lower input voltage of 102 V is applied, whilst operating the converter at the same power and output voltage (Fig. 16 to Fig. 18). As shown in Fig. 16, the SC voltage is maintained constant at approximately 200 V using $D_b = 0.5$ to produce the variable DC-link voltage of 192 V and 384 V across P and N in steps (Ch2).

As shown in Fig. 17, the output voltage is clearly 5-level with clean sinusoidal output voltage and current of 225 V and 2.18 A respectively. The operation of the converter delivering reactive

power to the AC side is also tested at φ = -25º as shown in Fig. 18.
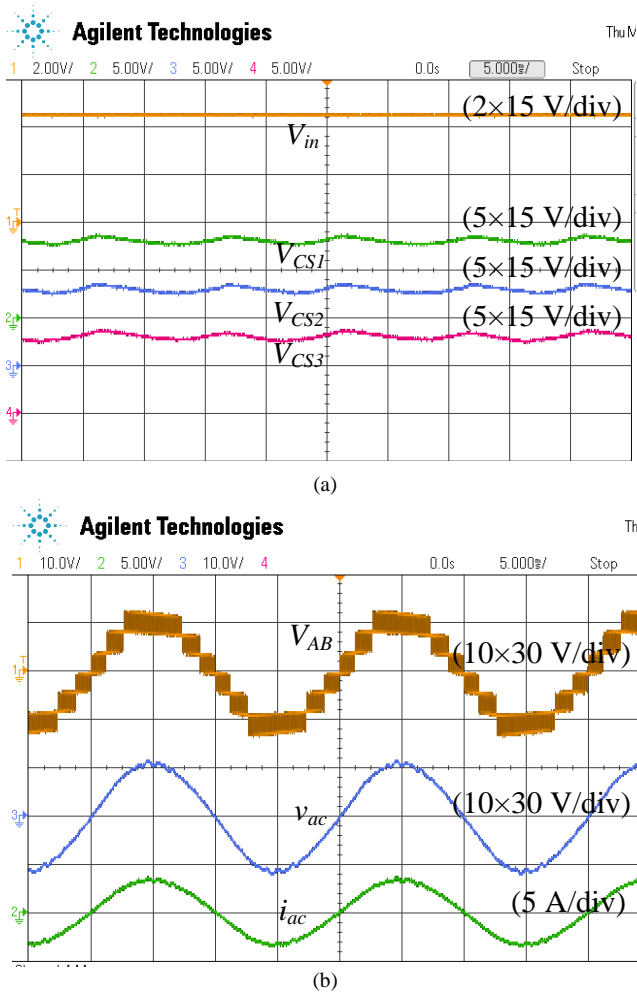

(a)

(b)

Fig. 19. Measured waveform of the 7-level inverter: (a) the input voltage, voltage across the switched-capacitors and (b) inverter voltage, output voltage and current after using the LC filter for resistive (R) load.

Some measurement results from the 7-level ($n = 3$) inverter are also presented at the end to support the analysis made in Section II. In this case, the Simulink model is implemented in OPAL-RT to get some useful results from the real-time model, such as 7-level output voltage, capacitor voltages and input and output voltages as shown in Fig. 19. The presented results show the efficacy of the proposed concept for any level inverter.

The losses on power devices have been calculated for 5-level, and 7-level configurations (see Fig. 20). A detailed thermal analysis and loss calculation using PLECS software can be found in the previous literature [24]. It can be seen that in 7-level configuration, the power loss in SC network is increased by 4% due to additional SCs used for level extension.

The calculated full load efficiency for 7-level configuration is 95.45%, which is 1.05% lower than that of the same condition for 5-level configuration. In both cases, a large part of the losses occurs in boost converter that can be reduced by using a switch with lower R_{ds_ON} and by replacing the boost diode with a MOSFET. Moreover, the second considerable part of the losses is related to the H-bridge switches for both cases and the losses in the passive components are considerably low.

The overall efficiency of the proposed converter (when $n = 2$) is investigated and compared between the calculated and experimental results for different load levels as depicted in Fig. 21. Fig. 21 (a) shows the losses on each power device where the

maximum loss occurs through the boost components. The efficiency of the prototype is measured by a FLUKE 345 power quality clamp meter. The maximum measured efficiency is 98.40% with the input voltage of 141 V and the load level of 25% of the full load. Moreover, the lowest efficiency measurement is 93.90% which is at the full load condition with the lowest input voltage level of 102 V.
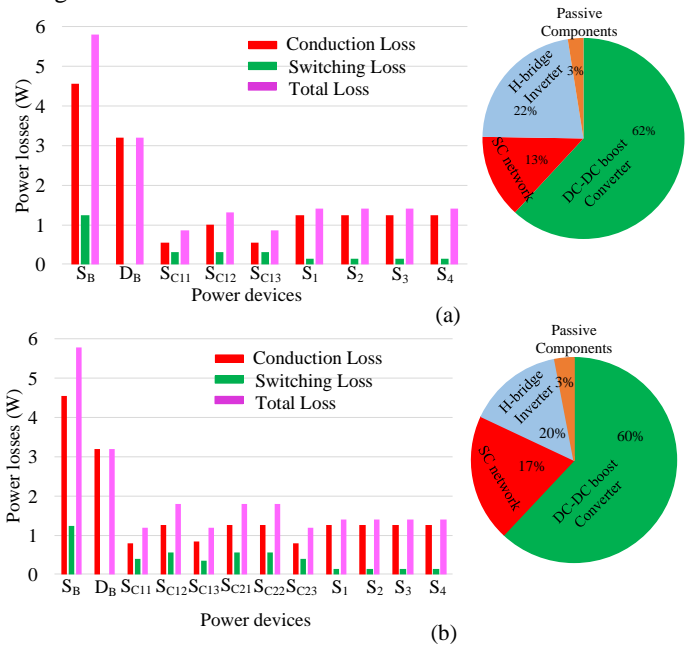

(a)

(b)

Fig.20. Loss distribution analysis for full load condition (500VA), (a) 5-level configuration, and (b) 7-level configuration.
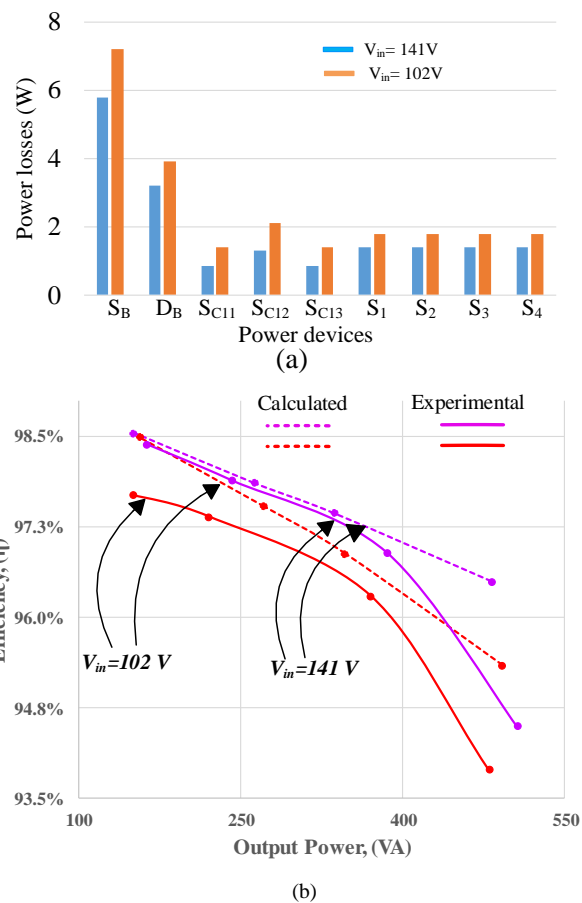

(a)

(b)

Fig. 21. 5-levels inverter prototype for two input voltages (V_{in}= 141V, and V_{in}= 102 V), (a) loss distribution for each power device, and (b) power conversion efficiency.

In Fig. 21 (b), the efficiency curves are illustrated for two different input voltages where the calculated results quite match with the experimental results. Due to miscellaneous losses, there are some differences between the measured and calculated efficiency at different load conditions. The calculated efficiency varies from 96.50% to 98.56% when the input voltage is 141 V and the experimental measurement varies from 94.50% to 98.40%. On the other hand, when the input voltage is changed to 102 V for 50% boost duty cycle, the calculated efficiency varies from 95.35% to 98.50% and the measured efficiency varies from 93.90% to 97.70%.

VI. CONCLUSION

A new (2n+1)-level inverter has been presented in this paper with boost capability. The proposed inverter can increase the voltage level with a single low input voltage source and benefit from low voltage stress on the semiconductors. The theoretical analysis of the proposed topology is derived and presented in detail. The proposed topology features many advantages when compared with various suggested single input SC-based (2n+1)-level inverter topologies, namely scalability, utilization of a low number of semiconductors, low voltage stress, high efficiency and power density, low cost and size, and simple modulation control. In addition, the comparison with existing single-phase multi-level inverters verifies that the proposed inverter is a viable and efficient solution when it is required to supply from a low voltage DC source. Furthermore, the simulation and experimental waveforms of an example 500 VA prototype are presented to show the validity of the proposed inverter.

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