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Frequency Adaptive Virtual Variable Sampling-based Selective Harmonic Repetitive Control of Power Inverters

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***Abstract*—Due to the n-pulse commutation, the power harmonic distortions caused by power inverters usually concentrate on particular $(nk \pm m)$-order harmonic frequencies. The conventional repetitive control (RC) uses an identical gain to equally compensate for the distortions at all harmonic frequencies. This leads to slow dynamics as it fails to optimize the convergence rate of the RC at dominant harmonic frequencies. The selective harmonic RC (SHRC) can efficiently suppress dominant power harmonic distortions. However, the ratio of the sampling rate of the SHRC to the fundamental frequency must be an integer. This severely limits the use and lowers the performance of the SHRC with a fixed sampling rate in the presence of frequency variations of interested harmonics. To address this problem, this paper proposes a frequency adaptive virtual variable sampling-based SHRC (FA-VVS-SHRC) scheme that is immune to the issue of the fractional ratio of the sampling rate to the interested harmonics. The proposed FA-VVS-SHRC scheme can provide flexible fractional phase lead compensation to achieve accurate power harmonic control in the presence of frequency variations. Moreover, it is a low-cost and easy-to-implement solution that does not require hardware modifications. Experiments on a three-phase power inverter and comparison studies are presented to verify its effectiveness.**

***Index Terms*—DC/AC inverter, frequency fluctuation, repetitive control, selective harmonics, virtual variable sampling**

I. Introduction

In electrical power systems, harmonics caused by power converter commutations usually concentrate on particular $(nk \pm m)$-order harmonic frequencies with n being the pulse number of the power converter, $m < n$, and $k = 1, 2, \cdots$. For instance, the harmonic frequencies of single-phase H-bridge inverters are mainly $4k \pm 1$ times of the fundamental frequency, while distortions of three-phase two-level inverters are typical $(6k \pm 1)$-order harmonics [1]–[8]. To deal with these particular harmonics, selective harmonic repetitive control (SHRC) schemes were developed [9]. The SHRC can effectively and accurately compensate for harmonics and, at the same time, maintain fast dynamics and strong robustness.

The SHRC scheme is typically implemented in digital signal processors with a period delay unit, $z^{-N/n}$, where N is the number of sample points in one reference fundamental signal period ($N = f_s/f_r$, f_s is the sampling frequency and f_r is the reference signal frequency) [10]. For digital control systems, the delay length N/n must be an integer, i.e., the sampling frequency f_s has to be an integral multiple of $f_r \times n$. This requirement, however, often does not hold in practical applications due to the following reasons: (1) The sampling frequency is not an integral multiple of $f_r \times n$. For example, a 60-Hz reference signal with a 10-kHz sampling frequency requires the period delay unit of $z^{-N/n} = z^{-27.78}$ to implement the SHRC in order to compensate for the dominant harmonics of 6-pulse converters, which is unachievable in DSPs or very difficult to do. (2) For grid-connected applications, the grid frequency always varies due to the power imbalance between the generation and load demands [11]–[13]. With a fixed sampling frequency of 10 kHz for 6-pulse converters, if the grid frequency fluctuates from 59.5 Hz to 60.5 Hz, the delay length N/n will correspondingly vary from 27.55 to 28.01. The fractional delay length N/n will degrade the harmonic suppression and deteriorate the output performance of SHRC, as N/n is usually approximated as an integer. Moreover, the employment of a fixed sampling frequency also leads to poor portability of the controllers. That is, the SHRC schemes designed for a 50-Hz system cannot universally be used in 60-Hz systems, as the control accuracy cannot be maintained.

To address this issue, variable sampling frequency schemes provide a general and intuitive solution that can achieve a constant integer ratio of N/n in the presence of frequency variations [14]–[17]. However, variable sampling methods not only require DSP's special variable sampling programming capacity but also need to recalculate or re-tune other digital control parameters to maintain the system stability and robustness [18], [19]. For example, in LCL-filtered systems, the active damping is closely related to the sampling frequency. It, in turn, increases the system cost and complexity.

Recently, the virtual delay unit concept was developed [16], [17], [20], which enables the virtual variable sampling (VVS) control. As an emerging technique, the VVS has some limitations that should be addressed. One major limitation is its performance degradation under frequency fluctuations. To tackle this problem, the virtual delay unit in [20] approximates the fractional delay due to frequency variations based a linear interpolation method, which requires heavy computation for a large number of delays and it is only suitable for a limited range of frequency mismatches. Accordingly, this paper

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extends the VVS control and proposes a frequency adaptive VVS-based SHRC (FA-VVS-SHRC) scheme to enable a low-cost and flexible solution. Different from the prior-art VVS methods, the FA-VVS-SHRC scheme accommodates frequency fluctuations by replacing fixed sampling period delays with virtual variable sampling period delays. By doing so, the FA-VVS-SHRC can accurately compensate for power harmonics distortions in the presence of a fractional ratio of N/n due to the fundamental frequency variations and/or the hardware limitations. It thus provides a generic and robust solution to the fractional delay unit issue of digital RC schemes [16], [20]. Experiments on a three-phase pulse width modulation (PWM) inverter (i.e., a 6-pulse inverter) are presented to demonstrate the effectiveness of the proposed method in dealing with frequency fluctuations.

The remainder of this paper is organized as follows: Section II introduces the conventional RC, the SHRC, and more importantly, proposes the FA-VVS-SHRC scheme. Experimental verification is performed on a three-phase PWM inverter, and the results are compared with conventional control methods in Section III. Concluding remarks are provided in Section IV.

II. Frequency Adaptive VVS-SHRC

A. Conventional RC

Fig. 1 illustrates the conventional RC (CRC) [21] with a plug-in structure, in which $R(z)$ is the periodic reference input, $G_c(z)$ is the feedback controller, $Y(z)$ is the system output, $G_p(z)$ is the plant model, and $D(z)$ is the disturbance. As shown in Fig. 1, the CRC scheme is a feed-forward controller that consists of an RC gain K_r, a low pass filter $Q(z)$, a phase lead filter $G_f(z)$, and a period delay z^{-N}. Let f_r and $T_r = 1/f_r$ denote the reference fundamental frequency and period of $R(z)$, and f_s and $T_s = 1/f_s$ be the system sampling frequency and period, respectively. Then, the number of sampling points in one reference signal period of $R(z)$ is calculated as $N = f_s/f_r = T_r/T_s$. In most existing RC designs, N must strictly be an integer. According to Fig. 1, the transfer function of the plug-in CRC $G_{RC}(z)$ is expressed as

$$G_{RC}(z) = \frac{U_r(z)}{E(z)} = K_r \frac{z^{-N}Q(z)}{1 - z^{-N}Q(z)} G_f(z) \qquad (1)$$

where $E(z) = R(z) - Y(z)$ is the system tracking error.

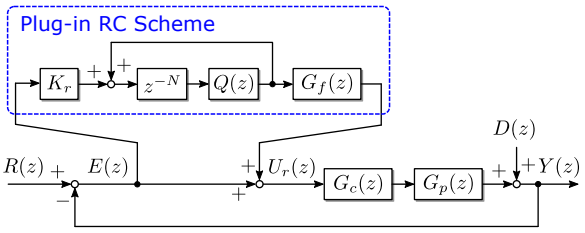


Fig. 1: Control system with the plug-in RC scheme.

A frequency domain analysis can be applied to Eq. (1), which shows that, when the low-pass filter $Q(z)$ is not considered, the CRC presents infinite magnitude gains at the fundamental and all harmonic frequencies of the reference signal. This means that, theoretically, the CRC can achieve zero tracking error on the desired frequency and higher order harmonic components to achieve zero total harmonic distortion (THD).

B. Digital Selective Harmonic RC

As mentioned previously, the harmonics of power inverters usually concentrate on $nk\pm1$ ($k = 0, 1, 2...$) order frequencies. Based on the internal model principle, a universal selective harmonic compensation module that includes only the internal models of $(nk \pm m)$-order harmonics can be designed. Fig. 2 shows the selective harmonic compensation module, which is tailored for the $(nk\pm m)$-order harmonics, will achieve perfect compensation of the harmonics at the selective frequencies.

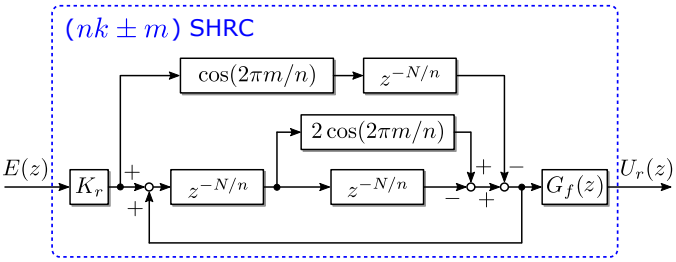


Fig. 2: Digital selective harmonic RC scheme.

The transfer function of the SHRC is given as

$$G_{SHRC}(z) = K_r \frac{\cos(2\pi m/n)z^{-N/n} - z^{-2N/n}}{1 - 2\cos(2\pi m/n)z^{-N/n} + z^{-2N/n}} \qquad (2)$$

where $n, m \in \mathbb{N}$, $n > m \geq 0$. Since $G_{SHRC}(z)$ has infinite magnitudes at $(nk \pm m)$-order frequencies, it can achieve zero tracking error at these harmonic frequencies, as aforementioned. More importantly, the design shown in Fig. 2 provides a flexible realization of the SHRC for different inverter topologies. For example, let $n = 1$ and $m = 0$, it is the CRC scheme, and let $n = 4$ and $m = 1$, it becomes an odd-order harmonic RC scheme for single-phase inverters [9]. More can be easily constructed by paralleling the SHRC modules.

C. Frequency Adaptation of SHRC

Similarly, the SHRC scheme requires the ratio of $N/n = T_r/T_s/n$ be an integer such that the internal models in the SHRC controller can well match the power harmonics. However, when the sampling period T_s does not meet the requirement and/or the reference signal's period T_r has fluctuations, the sampling points between two cycles of the reference signal will not be in the same phase. This means that the internal models in the RC mismatch the signals of interest. To further explain this issue, Fig. 3 illustrates the scenario when the reference signal's period T_r fluctuates under a constant sampling period of nT_s. As observed in Fig. 3, when the reference signal's period deviates from T_r to $\tilde{T}_r$, the sampling points in the period of $\tilde{T}_r$ are not in the same phase with those in the period of T_r. This phase mismatch will severely degrade the RC's performance, including the SHRC, and even lead to system instability. Hence, it is necessary to develop frequency adaptive schemes to ensure the harmonic compensation performance.

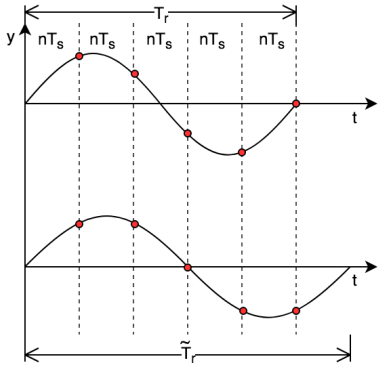


Fig. 3: Illustration of the performance degradation of the RC schemes with a constant sampling period nT_s when the reference signal frequency T_r varies.

D. Virtual Variable Sampling

To avoid the phase mismatch of sampling points under frequency fluctuation, the frequency adaptive RC requires a fixed sampling point number in one reference period under a varying reference frequency. When the reference period changes, the sampling period is adjusted accordingly to maintain the fixed sampling number, as illustrated in Fig. 4. That is, the variable sampling period $\tilde{T}_r$ should meet the following requirement:

$$\tilde{T}_s = \tilde{T}_r/(n \cdot N) \tag{3}$$

where $\tilde{T}_r$ is the variable reference signal period, n is the ratio from selective $(nk \pm m)$-order harmonics, and N is the number of sampling points in the RC.

The variable sampling period can be achieved by hardware modification. However, there are some limitations: 1), it requires particular DSP processing capacity that will increase the hardware cost; and 2), the hardware variable sampling period affects not only the RC scheme itself but also the conventional feedback controller $G_c(z)$, as aforementioned. The variable sampling period also needs to consider the influence on the stability of the conventional control loop.

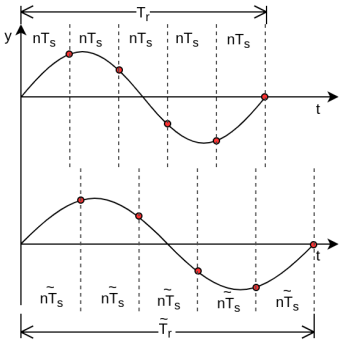


Fig. 4: Adaptive sampling period under T_r fluctuation.

These limitations can be overcome by the VVS technique, which employs fixed sampling period delays to approximate a variable sampling period delay in the control system. Fig. 5 exemplifies a 3-sampling-point VVS, which is based on the three sampling points at the time instants of $-T_s$, $-2T_s$, and $-3T_s$, and the approximation range is between $-T_s$ and $-3T_s$. By constructing a polynomial through the three sampling points, the approximation can be calculated through this polynomial. One way to make such an approximation is the Lagrange interpolation method, with which the n-sampling-point approximation equation can be generalized as

$$\tilde{z}^{-1} = \sum_{i=1}^{h} a_i z^{-i}, \text{with } a_i = \prod_{j=1, j\neq i}^{h} \frac{\tilde{T}_s - jT_s}{iT - jT_s} \tag{4}$$

where $\tilde{z}^{-1}$ denotes a virtual sampling delay, $\tilde{T}_s$ is the corresponding virtual variable sampling period, a_i is the Lagrange polynomial coefficients, and h is the approximation order, i.e., how many points are used in the approximation.

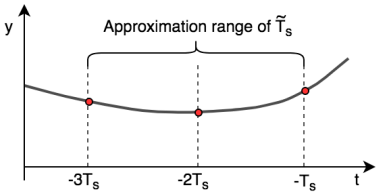


Fig. 5: Example of a variable sampling period approximation with 3 sampling points.

Clearly, a higher order approximation provides better accuracy and a wider range, while it also brings more computational burden. In this paper, the approximation order h is selected as 3, which ensures that the virtual variable sampling period $\tilde{T}_s$ is able to be well approximated by the fixed sampling periods from T_s to $3T_s$. In the z-domain, this can be expressed as

$$\tilde{z}^{-1} = a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-3}, \tag{5}$$

in which $a_1 = \frac{(\tilde{T}_s - 2T_s)(\tilde{T}_s - 3T_s)}{2T_s^2}$, $a_2 = \frac{(\tilde{T}_s - T_s)(\tilde{T}_s - 3T_s)}{-T_s^2}$, and $a_3 = \frac{(\tilde{T}_s - T_s)(\tilde{T}_s - 2T_s)}{2T_s^2}$.

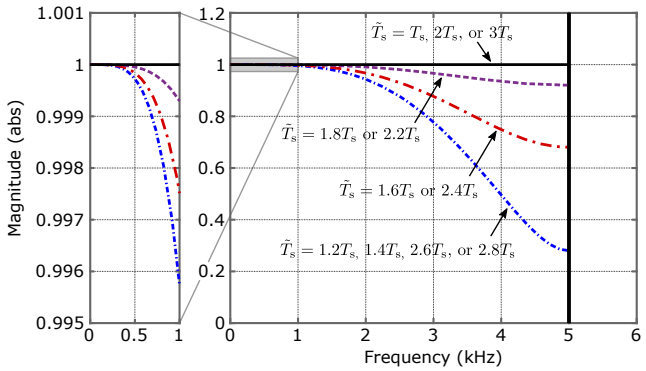


Fig. 6: Magnitude of the variable sampling period delay when the variable sampling period changes from T_s to $3T_s$.

To demonstrate the feasibility of this approximation, Fig. 6 shows the magnitude of a virtual variable delay unit $\tilde{z}^{-1}$ using the 3-order Lagrange approximation when the VVS adaptive sampling period $\tilde{T}_s$ changes from T_s to $3T_s$ under the sampling frequency of 10 kHz. From Eq. (4), the VVS adaptive delay unit $\tilde{z}^{-1} = z^{-1}$, z^{-2}, or z^{-3}, when the virtual sampling period $\tilde{T}_s = T_s$, $2T_s$, or $3T_s$, as shown in Fig. 6. There is no

approximation error obviously when $\tilde{T}_s = T_s, 2T_s$, or $3T_s$. The virtual variable delay unit performs as a low pass filter below the Nyquist frequency. For the low-frequency signal from 0 to 500 Hz, the virtual variable delay unit can approximate a real variable delay with an accuracy of above 99.97%, as observed in Fig. 6.

E. Frequency Adaptive VVS-SHRC

The virtual variable sampling approximation makes the SHRC frequency-adaptive. First, a proper constant sampling number N in one period is selected. Assuming that the reference period $\tilde{T}_r$ fluctuates within the range $[T_{r\_min}, T_{r\_max}]$, and the virtual variable sampling period $\tilde{T}$ has the range between T and $3T$, the constant sampling number N can be chosen as

$$\frac{T_{r\_max}}{3nT} < N < \frac{T_{r\_min}}{nT} \tag{6}$$

Normally, the constant sampling number N is chosen to be an integer near the middle of the range in Eq. (6) to allow the largest frequency adjustable range. With N being selected, the virtual variable sampling period $\tilde{T}_s$ is set based on Eq. (3). When the period $\tilde{T}_r$ of the reference signal varies, the virtual variable sampling period $\tilde{T}_s$ adjusts accordingly to determine the virtual variable delay unit $\tilde{z}$. It is worth mentioning that the virtual variable delay unit is also flexible to realize fractional order phase lead compensation [8].

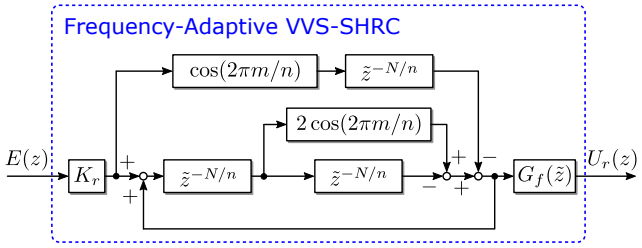


Fig. 7: Block diagram of the proposed FA-VVS-SHRC.

Replacing the fixed delay z^{-1} with the virtual variable delay $\tilde{z}^{-1}$, the transfer function of the FA-VVS-SHRC shown in Fig. 7 can be obtained as

$$G_{FA-VVS-SHRC}(\tilde{z}) = K_r \frac{[\cos(\frac{2\pi m}{n})\tilde{z}^{-\frac{N}{n}} - \tilde{z}^{-2\frac{N}{n}}]G_f(\tilde{z})}{1 - 2\cos(\frac{2\pi m}{n})\tilde{z}^{-\frac{N}{n}} + \tilde{z}^{-\frac{N}{n}}} \tag{7}$$

which does not require any hardware modifications, as aforementioned

III. Experiments on Three-phase PWM Inverters

A. System modeling and state feedback controller

Fig. 8 shows a $(6k \pm 1)$-order FA-VVS-SHRC controlled three-phase programmable PWM inverter, where E_n is the DC bus voltage, and L and C form a three-phase LC filter. The performance of the AC source is tested under a linear resistor load of R and a nonlinear rectifier load with diodes, capacitor C_r, and resistor R_r. The output voltage V_{ab}, V_{bc}, and V_{ca}, and inductor current I_{La}, I_{Lb}, and I_{Lc} are two states for a state feedback controller (SFC).

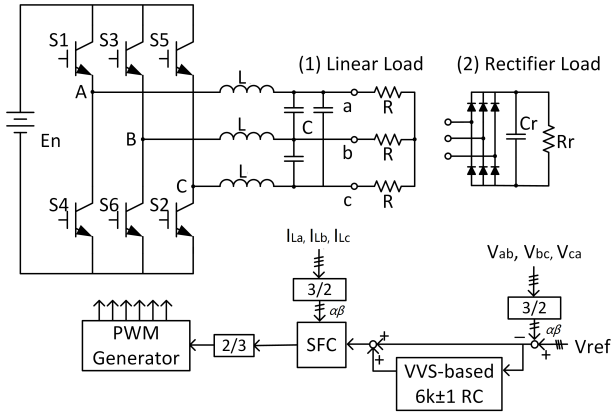


Fig. 8: Plug-in $(6k\pm1)$-order FA-VVS-SHRC controlled PWM inverter system.

The state space representation of the three-phase PWM inverter with the linear load in Fig. 8 is given as

$$\begin{bmatrix} 1 & 0 & -1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} \dot{v}_{ab} \\ \dot{v}_{bc} \\ \dot{v}_{ca} \\ \dot{i}_{La} \\ \dot{i}_{Lb} \\ \dot{i}_{Lc} \end{bmatrix}$$

$$= \begin{bmatrix} \frac{-1}{2RC} & 0 & \frac{1}{2RC} & \frac{1}{C} & 0 & 0 \\ \frac{1}{2RC} & \frac{-1}{2RC} & 0 & 0 & \frac{1}{C} & 0 \\ 0 & \frac{1}{2RC} & \frac{-1}{2RC} & 0 & 0 & \frac{1}{C} \\ \frac{-1}{L} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{L} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{L} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \\ i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{8}$$

$$+ \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix}$$

where V_{AB}, V_{BC} and V_{CA} are the PWM voltages with values of either E_n or $-E_n$, and R, C, L are the load resistor, filter capacitor, and filter inductor of each phase [21].

When three-phase loads are balanced, Eq. (8) can be transformed into the $\alpha\beta$-stationary reference frame [21] as

$$\begin{bmatrix} \dot{v}_\alpha \\ \dot{i}_\alpha \\ \dot{v}_\beta \\ \dot{i}_\beta \end{bmatrix} = \begin{bmatrix} \frac{-1}{3RC} & \frac{1}{3C} & 0 & 0 \\ \frac{-1}{L} & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{3RC} & \frac{1}{3C} \\ 0 & 0 & \frac{-1}{L} & 0 \end{bmatrix} \begin{bmatrix} v_\alpha \\ i_\alpha \\ v_\beta \\ i_\beta \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ \frac{E_n}{L} & 0 \\ 0 & 0 \\ 0 & \frac{E_n}{L} \end{bmatrix} \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} \tag{9}$$

where state variables v_α, v_β, i_α, and i_β are the output voltages and the inductor currents in the $\alpha\beta$-reference frame. The vector $[u_\alpha \;\; u_\beta]^T$ is the corresponding control vector. Eq. (9) can be treated as two independent systems with the same state space as [22]

$$\begin{bmatrix} v(k+1) \\ i(k+1) \end{bmatrix} = \begin{bmatrix} \varphi_{11} & \varphi_{12} \\ \varphi_{21} & \varphi_{22} \end{bmatrix} \begin{bmatrix} v(k) \\ i(k) \end{bmatrix} + \begin{bmatrix} g_1 \\ g_2 \end{bmatrix} u(k) \tag{10}$$

in which $v = v_\alpha$ or v_β, $i = i_\alpha$ or i_β, $u = u_\alpha$ or u_β, and the coefficients $\varphi_{11} = 1 - T_s/(3RC) + T_s^2/(18R^2C^2) - T_s^2/(6LC)$, $\varphi_{12} = T_s/(3C) - T_s^2/(18RC^2)$, $\varphi_{21} = -T_s/L + T_s^2/(6RLC)$, $\varphi_{22} = 1 - T_s^2/(6LC)$, $g_1 = E_n T_s^2/(6LC)$, $g_2 = E_n T_s/L$.

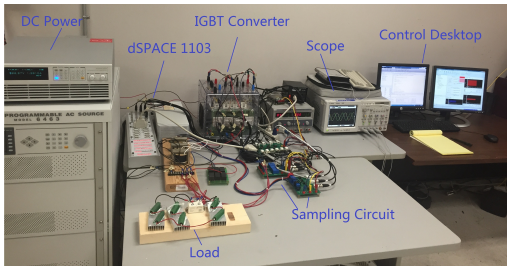


Fig. 9: Experimental platform of the three-phase inverter.

The SFC has the form of

$$u = -k_1 v(k) - k_2 i(k) + g v_{ref}(k) \tag{11}$$

where k_1, k_2 and g are the SFC parameters, v_{ref} is the reference sinusoidal voltage. With the SFC in Eq. (11), the transfer function can be rewritten as

$$G(z) = \frac{m_1 z + m_2}{z^2 + p_1 z + p_2} \tag{12}$$

with $p_1 = -(\varphi_{22} - g_2 k_2) - (\varphi_{11} - g_1 k_1)$, $p_2 = (\varphi_{11} - g_1 k_1)(\varphi_{22} - g_2 k_2) - (\varphi_{12} - g_1 k_2)(\varphi_{21} - g_2 k_1)$, $m_1 = g_1 k$, $m_2 = g_2 k - g_1 k(\varphi_{22} - g_2 k_2)$ [22]. The above SFC is then implemented in an experimental setup.

TABLE I: System Parameters.

Parameter	Value	Parameter	Value
DC voltage, E_n	400 V	Inductor, L	3 mH
Capacitor, C	10 μF	PWM frequency	10 kHz
Sampling frequency, f_s	10 kHz	Linear load, R	200 Ω
Rectifier capacitor C_r	60 μF	Rectifier inductor L_r	3 mH
Rectifier resistance R_r	200 Ω		

Fig. 9 shows the experimental platform. The SFC and RC schemes are designed in MATLAB Simulink, which are then loaded and implemented on a dSPACE DS1103 control board to control the PWM IGBT three-phase inverter. Table I lists the system parameters. Referring to Eq. (12) and Table I, the system transfer function is obtained as

$$G(z) = \frac{0.5971z + 0.0058}{z^2 - 0.8116z} \tag{13}$$

which indicates that the SFC system has poles at 0 and 0.81, implying that the system is stable. With only the feedback controller, there is a severe phase lag and the output waveform shows high distortions under both linear and rectifier load conditions, as shown in Fig. 10. Due to the structure of the 6-pulse commutation, the major distortion components appear at frequencies of $6k \pm 1$ times of the fundamental frequency, as observed in the harmonic analysis in Fig. 10 (the bottom ones).

Fig. 11 shows the Bode plots of the SFC and SFC with an RC. As the RC with a low pass filter provides identical compensation on all harmonics, there will be certain impact around crossover frequencies. This impact will limit the RC gain design range.

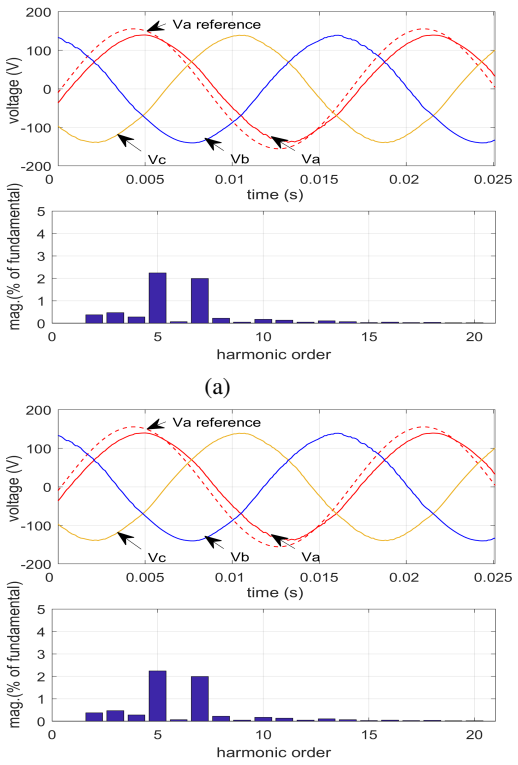


Fig. 10: Steady-state of the three-phase inverter with the SFC under (a) the linear load and (b) the nonlinear load.

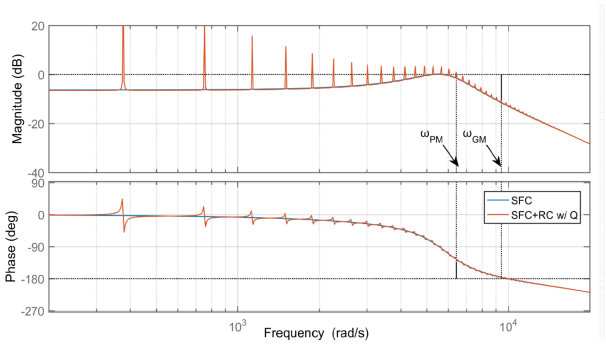


Fig. 11: Bode plot of the state feedback control with a repetitive control.

B. $(6k \pm 1)$-order FA-VVS-SHRC

With the reference signal frequency $f_r = 60$ Hz ($T_r = 1/60$ s) and the sampling frequency $f_s = 10$ kHz ($T_s = 0.1$ ms), the delay length N is selected as 84, which is an integer multiple of $n = 6$. The adaptive delay unit is obtained from Eq. (4) as

$$\tilde{z}^{-1} = 0.0081 z^{-1} + 0.9997 z^{-2} - 0.0078 z^{-3} \tag{14}$$

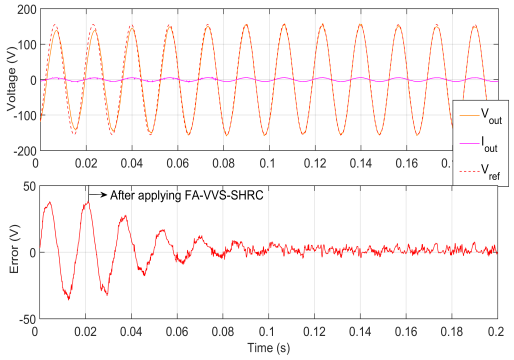
The next step is to choose the RC gain K_r and to build the linear phase-lead filter $G_f(\tilde{z})$. In this case, K_r is selected as 0.5 to achieve fast dynamics after applying the $(6k \pm 1)$-order FA-VVS-SHRC. Note that $G_f(\tilde{z})$ will be used to compensate for not only the phase lag of the system model but also the unmodeled delays in the system. The phase lead of $G_f(\tilde{z})$

is designed following the analysis in [23], by measuring the actual system phase lag. The final phase lead is selected as

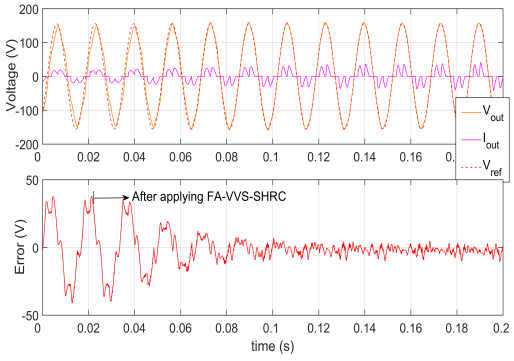
$$G_f(\tilde{z}) = \tilde{z}^{2.2} \approx -0.048\tilde{z}^1 + 0.864\tilde{z}^2 + 0.216\tilde{z}^3 - 0.032\tilde{z}^4 \tag{15}$$

C. Experimental validation

1) Transient responses: Fig. 12 shows the transient response and tracking error when the proposed $(6k \pm 1)$-order FA-VVS-SHRC is applied to (a) the linear load and (b) the rectifier load, referring to Fig. 8. When the system operates with only the SFC, the peak tracking error is about 40 V due to the severe phase lag and magnitude error. After the $(6k \pm 1)$-order FA-VVS-SHRC is put into use, the tracking error converges effectively and becomes stable within about 5-6 cycles or 0.1-0.12 seconds, as shown in Fig. 12.



(a)



(b)

Fig. 12: Transient response of the three-phase inverter with the FA-VVS-SHRC (a) the linear load, (b) the nonlinear load.

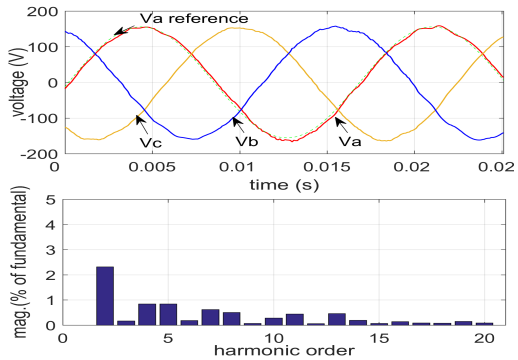
2) Steady-state responses: Figs. 13 and 14 compare the steady-state performance of the three-phase $(6k \pm 1)$-order SHRC without and with the frequency adaptive scheme under (a) the linear load and (b) the rectifier load. Comparing with the SFC performance in Fig. 10, the major distortion that locates at $(6k \pm 1)$-order harmonics have been eliminated with the SHRC. However, Fig. 13 shows that the SHRC cannot achieve an accurate steady tracking because of the inaccuracy of the delay length of N/n. This is addressed by the precise phase compensation offered by the proposed virtual variable sampling approximation, as presented in Fig. 14. It is observed in Fig. 14 shows that the $(6k \pm 1)$-order FA-VVS-SHRC provides the most accurate voltage tracking and the least distortion.

TABLE II: Steady State Performance Comparison at 60Hz.

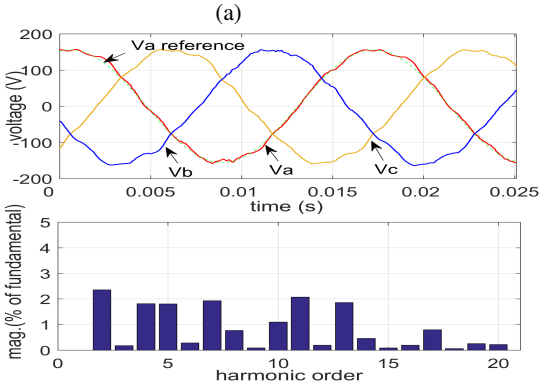
		SFC	SHRC	FA-VVS-SHRC
Linear Load	RMSE	23.77 V	5.43 V	2.59 V
	THD	2.34%	3.22%	1 %
Rectifier Load	RMSE	26.62 V	5.94 V	3.27 V
	THD	6.17%	4.11%	2.02 %

The PWM inverter steady-state performance is further assessed quantitatively by the root mean square tracking error (RMSE) and THD. Table II summarizes and compares the steady-state performance of the SFC, the conventional SHRC, and the FA-VVS-SHRC. The conventional SHRC under the linear and the rectifier loads yields the tracking errors of 5.43 V and 5.94 V, and the THD of 3.22% and 4.11%, respectively.

With the FA-VVS-SHRC, the tracking errors have 52.3% and 44.9% improvement over that of the conventional SHRC under the linear and the rectifier loads, and the THD improvement is 68.9% and 50.9%, respectively.



(a)



(b)

Fig. 13: Steady-state of the three-phase inverter with the conventional SHRC (a) the linear load, (b) the rectifier load.

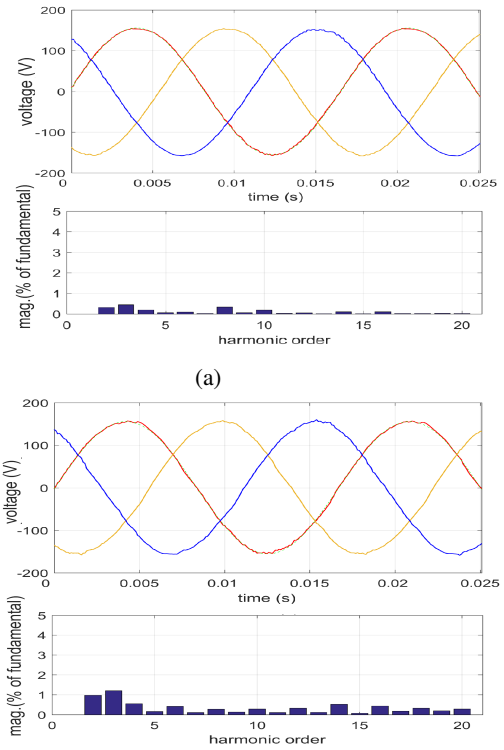


Fig. 14: Steady-state of three-phase inverter with the FA-VVS-SHRC (a) the linear load, (b) the rectifier load.

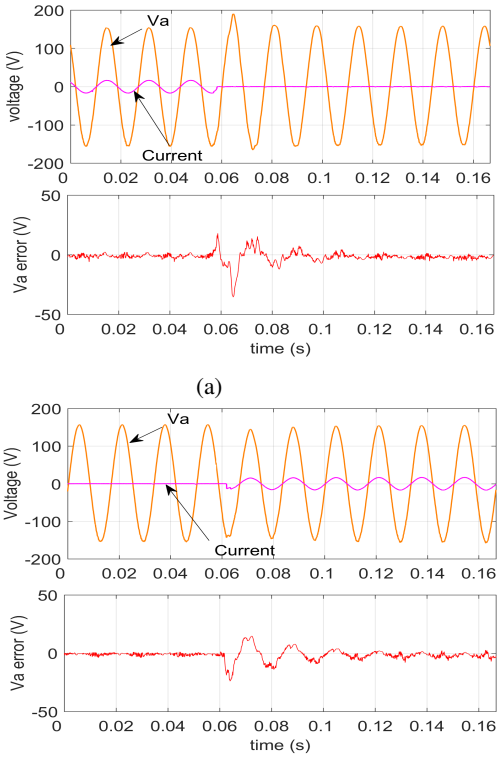


Fig. 15: Sudden load change (linear load and no load) with the proposed FA-VVS-SHRC.

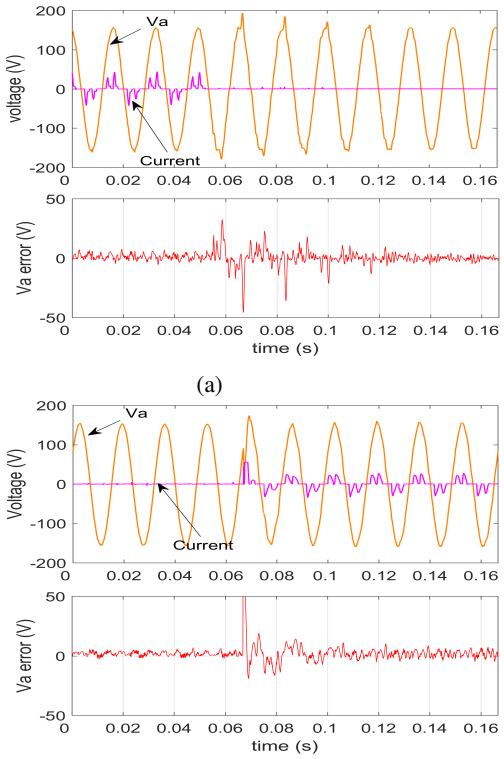


Fig. 16: Sudden load change (rectifier load and no load) with the proposed FA-VVS-SHRC.

3) Sudden load change responses: To further demonstrate the effectiveness of the FA-VVS-SHRC, Figs. 15 and 16 show the performance of the three-phase inverter under a load sudden change. The output voltage recovers to the steady state with limited tracking errors after several cycles fluctuation. The robustness of the proposed FA-VVS-SHRC is then verified based on the experimental tests.

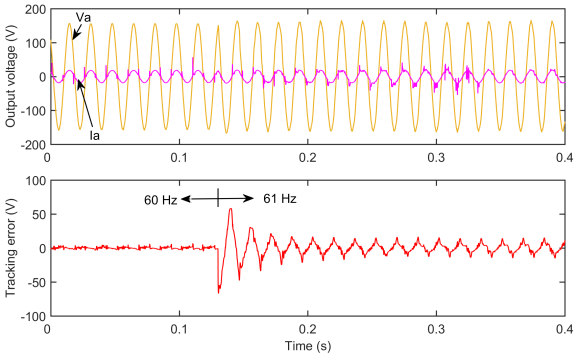


Fig. 17: Conventional SHRC under a linear load with frequency fluctuation (60 Hz to 61 Hz).

4) Frequency change responses: Figs. 17 and 18 show the transient response comparison of the conventional SHRC and the FA-VVS-SHRC when the reference frequency fluctuates. When the reference frequency changes from 60 Hz to 61 Hz, the FA-VVS-SHRC achieves 1.02 % THD and 2.63 V RMS tracking error after a certain transient process. On the contrary, the RMS tracking error and the THD of the conventional

SHRC are 6.80 V and 3.11 % when it reaches the steady state. Table III summarizes the results, which show that the proposed FA-VVS-SHRC can accommodate the disturbance from frequency fluctuations.

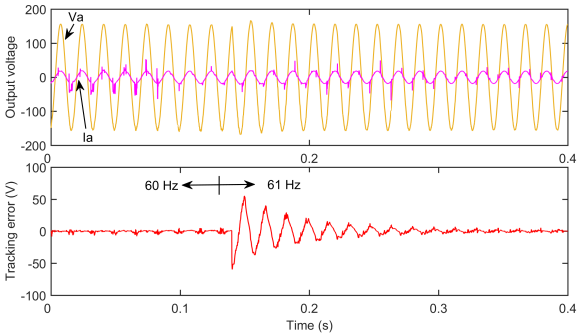


Fig. 18: FA-VVS-SHRC under a linear load with frequency fluctuation (60 Hz to 61 Hz).

TABLE III: Steady State Performance Comparison at 61 Hz.

	SHRC	**FA-VVS-SHRC**
RMSE	6.80 V	2.63V
THD	3.11%	1.02 %

IV. Conclusion

A frequency adaptive virtual variable sampling-based selective harmonic repetitive control (FA-VVS-SHRC) scheme is proposed in this paper to provide a tailor-made solution to compensate for harmonics produced by power inverters. The proposed FA-VVS-SHRC scheme offers a generic solution to the selective harmonic RC with high control accuracy guaranteeing strong robustness, enabling flexible fractional phase lead compensation, and being feasible for implementation in the presence of the fractional ratio of the sampling frequency to the fundamental reference frequency or time-varying reference frequency. Experiments on a three-phase power inverter under different load conditions, frequency fluctuations, sudden load changes have demonstrated the effectiveness of the proposed solution. The proposed FA-VVS-SHRC method can also be applied to other RCs and fractional phase delay compensation.

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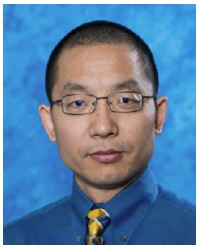

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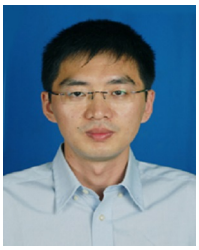

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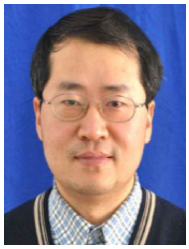

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