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Modeling of Converter Synchronization Stability under Grid Faults: The General Case

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***Abstract*—The synchronization dynamics of grid-connected power converters are known to have a tremendous impact on transient stability and fault ride-through performance under grid faults. Up till now, the modeling of converter synchronization stability, which has paved the way for numerous enhanced control methods, is developed around the assumption that the grid fault is symmetrical. However, this is rarely the case. Moreover, grid codes require dual-sequence current injection during asymmetrical faults, which implies that the previously developed models are no longer valid during unbalanced conditions. To address these issues, this article identifies the necessary stability conditions during asymmetrical conditions and presents a quasi-static large-signal reduced-order model of a grid-following converter for analyzing its synchronizing interaction with the external network during symmetrical and asymmetrical grid faults. The modeling approach is developed and tested for three different short-circuit faults: A single line-to-ground fault, a double line-to-ground fault, and a line-to-line fault. The accuracy of the proposed model is verified through detailed simulation studies and experimental tests. Thus, this model can be used to assess the transient synchronization stability of grid-following converters during any type of grid fault, and due to its low-order representation, it may be well applicable for large-scale power system studies.**

***Index Terms*—Fault Ride-Through, Grid-Connection, Synchronization Stability, Transient Stability, Unbalanced Grid Fault, Voltage-Source Converter.**

NOMENCLATURE

i_d^*, i_q^*	Reference values for d- and $q-$axis current components
L_L, L_{tr}, L_g	Line, transformer leakage, and grid inductances, respectively
R_L, R_g	Line and grid resistances
V_g, ϕ_g	Magnitude and phase angle of grid voltage
$V_{PCC}^{\pm}$	Positive/negative sequence PCC voltage magnitude
$\theta_{PCC}^{\pm}$	Positive/negative sequence PCC voltage phase angle
$\theta^{\pm}$	Positive/negative sequence control angle of synchronization unit
$V_F^{\pm}$, $\theta_F^{\pm}$	Positive/negative sequence fault voltage magnitude and phase angle
Z_L	Magnitude of line impedance.
Z_{LT}, ϕ_{LT}	Magnitude and phase of combined line and transformer impedance
$I^{\pm}$, $\theta_C^{\pm}$	Positive/negative-sequence magnitude and phase angle of injected converter current
$\theta_I^{\pm}$	Positive/negative-sequence phase angle of converter current relative to $\theta^{\pm}$
Z_F	Fault impedance
$V_{th}^{\pm 0}$	Positive/negative/zero-sequence component of Thevenin equivalent voltage
$Z_{th}^{\pm 0}$	Positive/negative/zero-sequence component of Thevenin equivalent impedance
$I_F^{\pm 0}$	Positive/negative/zero-sequence fault currents
ω_N	Natural angular frequency of synchronization unit

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I. INTRODUCTION

WITH a rapidly increasing penetration of renewable energy sources interfaced with power electronic voltage-source converters (VSCs), the dynamical behavior of modern and future power grids are strongly influenced by the operation and control of these converters [1]. A high penetration of converter-based generation strongly affects how the surrounding network is being supported during fault conditions. To that end, their dynamic response is, unlike synchronous generators, determined by the internal control. As addressed by the British network operator, National Grid, an increasing risk of synchronization instability of phase-locked loop (PLL)-synchronized converters is identified during grid faults and weak-grid conditions [2]. Therefore, an increasing interest in understanding the transient stability of converter-based generation has emerged [3]. To enhance the network stability during fault conditions, converters must comply with low-voltage ride-through requirements defined in the grid codes by the network operator. The study of grid-synchronization during fault conditions using different synchronization methods has been thoroughly investigated [4], yet without the influence of the converter current injection on the synchronization point. It has been repeatedly shown that under grid faults and weak-grid conditions, converter instability may occur as the synchronization unit is unable to remain synchronized with the voltage at the point of connection [5]–[9]. This phenomenon is referred to as grid-synchronization instability or loss of synchronization (LOS). Accordingly, being able to model the LOS is essential for accurate transient stability assessment

and for identification of potential controller solutions which enhance the synchronization stability.

Initially, a static model identifying necessary conditions for synchronization stability during severe grid faults was presented in [5]. Here, it was recognized that the instability occurs as a power transfer problem in an RL-circuit, where depending on the phase-angle between the voltage and the injected current, only a limited magnitude of the currents can be provided. Since this model is static, it contains no system dynamics, which means it is only able to assess instability, accurately, when the static limit is violated. To address this problem, a quasi-static large-signal PLL model was proposed in [6]. In this model, a destabilizing positive-feedback loop was identified, which is caused by the interaction between the injected currents and the grid impedance on the voltage at the point of synchronization. This model has paved the way for understanding and describing LOS [10]–[13]. Besides the revelation this model brought in understanding LOS, it has certainly initiated ideas for enhanced controller designs aiming to avert instability [14]–[17]. To that end, the dynamics of the PLL is shown in [18] to be equivalent to the equations governing the motion of a synchronous machine. Therefore, equivalent inertia and damping of the PLL can be identified, which has further enhanced the understanding between the PLL controller gains and the anticipated dynamical response. As the model presented in [6] is second order and nonlinear, it has no known analytical solution. To address this, recent research has adopted phase portraits and numerical approximations to estimate the critical PLL damping and area of attraction [19]–[21]. Moreover, it is shown in [22] that the synchronization stability of PLL-synchronized grid-following converters can be improved by adopting a first-order synchronization unit during the fault. It should be noted that in the model development, laying the foundations for all the mentioned methods, the grid fault is assumed to be symmetrical, although more than 95% of all occurring grid faults are actually asymmetrical [23]. To that end, in California, 2016, PLL instability occurred during asymmetrical line-to-line and single line-to-ground faults, causing a disconnect of 700 MW in a large photovoltaic power plant [24]. This raises the question of how LOS should be characterized and assessed under such circumstances. Only [22] describing synchronization stability is found to address asymmetrical conditions somewhat. In this work, it is described that under asymmetrical conditions, a pre-filtering stage is used before the PLL input to extract the fundamental positive-sequence voltage. Since it is assumed that the pre-filtering stage has a bandwidth much higher than the PLL, it is neglected, and the model developed for positive sequence conditions is valid. This assumption depends on the type of pre-filter used and the tuning of it. Besides this, it is only valid if the converter is considered to inject only positive sequence current during the fault. Nevertheless, as described in recent German grid codes [25], [26], dual-sequence current injection is required by the power converter during asymmetrical faults. Considering this, the above assumption can no longer be justified, and the system must be modeled in the sequence domain, taking into account that both positive and negative sequence currents are injected during a fault. The LOS problem during asymmetrical conditions is, in essence, not significantly different from the symmetrical fault case since it still relies on a power transfer issue between the converter and the faulted bus. However, how to model and analyze it is mathematically different since LOS is now specified in two sequence-frames that are coupled to each other at the fault location.

Several recent research employs the complex vector modeling approach to model asymmetrical fault conditions of grid-connected converters [27], [28]. Also, high-order state-space models have been developed for asymmetrical fault analysis [29], [30]. These models are, however, not focused on the LOS phenomenon, they analyze the fault condition from a pre-fault and post-fault small-signal point of view, and due to high model complexity, they are not suitable for large-scale analysis.

Consequently, this article aims to extend the modeling and assessment of the large-signal synchronization stability of grid-following converters into a general framework, which is valid for both symmetrical and asymmetrical fault conditions. Additionally, this article proposes a simplified sequence model of grid-connected converters during asymmetrical fault conditions, which may be useful for system operators in their fault analysis of large-scale multi-converter systems. The main research contributions provided in this article can be summarized as

1) Identifying and describing the necessary condition for stability during asymmetrical faults which are used to attain a physical understanding of LOS. (Section III).
2) Providing a general modeling framework for representing the converter control and grid-interactions as sequence equivalents in the positive, negative, and zero-sequence frames taking into account dual-sequence operation. (Section IV).
3) Proposing a reduced-order large-signal model for stability assessment using a generalized sequence-domain modeling framework with the opportunity for user-specific synchronization units, which is general to any short-circuit fault type, both symmetrical and asymmetrical grid faults. (Section V).

The remainder of the article is as follows: A description of the system is given in Section II. Following this, the necessary stability conditions during asymmetrical faults are derived in Section III. Based on these, the general equivalent sequence-domain model of the system is developed in Section IV for three types of asymmetrical short-circuit faults. A proposed simplified model is presented in Section V, which is validated against a detailed simulation model. The proposed model is experimentally verified in Section VI and the article is finally concluded in Section VII.

II. System of Study

In this article, a grid-following VSC is studied. The high-frequency switching waveform at the converter terminals is filtered through an LCL-filter from where it is connected to the grid via a Delta-wye (Dy) grounded step-up transformer as depicted in Fig. 1. Between the line impedance, Z_L, and the

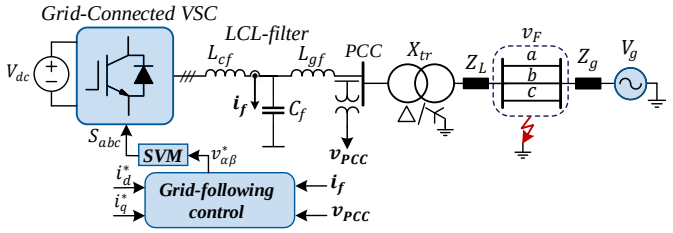

Fig. 1. Structure of grid-tied converter with grid-following control connected to the grid where an asymmetrical grid fault is considered to occur at v_F. SVM: Space Vector Modulation. A detailed view of the grid-following control can be seen in Fig. 2(a).

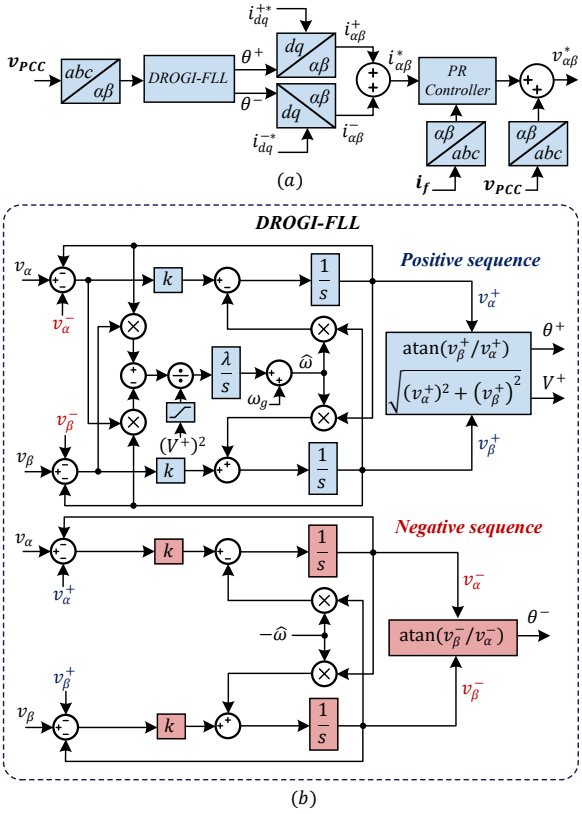

Fig. 2. Details on implemented converter control. (a): Complete outlook of the grid-following control shown in Fig. 1. (b): Detailed view of the DROGI-FLL used for sequence extraction and synchronization.

external grid, an asymmetrical fault is considered to occur as a short-circuit between one or more phases and the ground. The dc-side of the converter is usually connected to a generator-side converter in the case of a type IV wind turbine system or a DC/DC boost converter in case of a photovoltaic system. In either cases, the back-to-back converters are carefully controlled, meaning that the two converters can be considered decoupled and analyzed independently. Furthermore, in the case of grid faults, any accumulation of energy at the dc-side may be regulated using a dc-side chopper, also under unbalanced faults [31]. Accordingly, the dc-side can be approximated as a constant voltage source as it is in this work.

To perform phase-tracking of both the positive-sequence and the negative-sequence voltages during the fault, a single SRF-PLL or single PLLs with a pre-filtering stage cannot be used since the negative-sequence voltage component cannot be tracked. To achieve this, the grid-following structure in Fig. 1 uses a dual reduced-order generalized integrator frequency-locked loop (DROGI-FLL) (visualized in Fig. 2(b)) [32], to extract the sequence voltage components at the point of common coupling (PCC). It is important to notice that the DROGI-FLL is just one realization of a synchronization unit that can perform phase-tracking in both sequence frames. Also, the generalized modeling framework to be presented in this work is independent of the synchronization unit considered, and is therefore not limited to the DROGI-FLL.

The DROGI-FLL is considered in this work due to its reduced-order dynamical structure. However, due to the independence of the proposed modeling framework to the applied synchronization unit, alternative solutions for synchronization could have been selected instead, e.g. a dual second-order generalized integrator PLL (DSOGI-PLL) [33], a decoupled double synchronous-reference frame PLL (DDSRF-PLL) [34], or an SRF-PLL with a complex coefficient notch and band-pass filters [35]. For dual-sequence current control, a proportional-resonant (PR) controller is used to control the converter-side currents, and the PCC voltage feed-forward control is used to enhance the dynamic response of the converter. i^*_d is set to 1 per-unit (pu) under normal operating conditions whereas i^*_q is calculated based on the required dynamic voltage support from the considered grid code. Following the German grid code for installation in the medium-voltage network [25], the system should tolerate severe low-voltage conditions and in case of asymmetrical faults, currents should be injected in both the positive and the negative sequence proportionally to the change in the sequence voltage components at the PCC. To that end, the negative sequence current injection is necessary to avoid phase overvoltages [31] and excess heating of machines alongside providing a balanced voltage for loads and customers [36].

III. Necessary Conditions for Transient Stability

The single-line diagram used for a balanced three-phase system can no longer be applied to analyze LOS during asymmetrical conditions. Instead, considering the converter to operate in a three-wire system, an unbalanced condition can be represented by a positive-sequence and negative-sequence network [37]. Using the diagram from Fig. 1, the state equations of the inductances in the positive and negative sequence frames can be written as

$$(L_L + L_{tr})\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i^+_\alpha \\ i^+_\beta \end{bmatrix} = \begin{bmatrix} v^+_{PCC\alpha} \\ v^+_{PCC\beta} \end{bmatrix} - R_L \begin{bmatrix} i^+_\alpha \\ i^+_\beta \end{bmatrix} - \begin{bmatrix} v^+_{F\alpha} \\ v^+_{F\beta} \end{bmatrix} \quad (1)$$

$$(L_L + L_{tr})\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i^-_\alpha \\ i^-_\beta \end{bmatrix} = \begin{bmatrix} v^-_{PCC\alpha} \\ v^-_{PCC\beta} \end{bmatrix} - R_L \begin{bmatrix} i^-_\alpha \\ i^-_\beta \end{bmatrix} - \begin{bmatrix} v^-_{F\alpha} \\ v^-_{F\beta} \end{bmatrix} \quad (2)$$

and

$$L_g\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i^+_{g\alpha} \\ i^+_{g\beta} \end{bmatrix} = \begin{bmatrix} v^+_{F\alpha} \\ v^+_{F\beta} \end{bmatrix} - R_g \begin{bmatrix} i^+_{g\alpha} \\ i^+_{g\beta} \end{bmatrix} - \begin{bmatrix} v^+_{g\alpha} \\ v^+_{g\beta} \end{bmatrix} \quad (3)$$

$$L_g\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i^-_{g\alpha} \\ i^-_{g\beta} \end{bmatrix} = \begin{bmatrix} v^-_{F\alpha} \\ v^-_{F\beta} \end{bmatrix} - R_g \begin{bmatrix} i^-_{g\alpha} \\ i^-_{g\beta} \end{bmatrix} - \begin{bmatrix} v^-_{g\alpha} \\ v^-_{g\beta} \end{bmatrix} \quad (4)$$

where i is the current flowing into the grid from the PCC and L_{tr} is the transformer leakage inductance. Expressing (1)-(2) in phasor form, the PCC voltage may be expressed in its sequence components as

$$V_{PCC}^{+}\mathrm{e}^{\mathrm{j}\theta^{+}} = V_F^{+}\mathrm{e}^{\mathrm{j}\theta_F^{+}} + Z_{LT}\mathrm{e}^{\mathrm{j}\phi_{LT}^{+}} I^{+}\mathrm{e}^{\mathrm{j}\theta_C^{+}} \tag{5}$$

$$V_{PCC}^{-}\mathrm{e}^{\mathrm{j}\theta^{-}} = V_F^{-}\mathrm{e}^{\mathrm{j}\theta_F^{-}} + Z_{LT}\mathrm{e}^{\mathrm{j}\phi_{LT}^{-}} I^{+}\mathrm{e}^{\mathrm{j}\theta_C^{-}} \tag{6}$$

where $\theta_C^{\pm} = \theta^{\pm} + \theta_I^{\pm}$, Z_{LT} and ϕ_{LT} are the combined line and transformer impedance magnitude and phase, respectively, and $\theta_{PCC}^{\pm} = \theta^{\pm}$ during steady-state, i.e. $\theta^{\pm}$ is the control angle of the used synchronization unit. Multiplying both sides of (5)-(6) with $\mathrm{e}^{-\mathrm{j}\theta^{\pm}}$ and taking the imaginary part gives

$$v_q^{+} = V_F^{+}\sin\left(\theta_F^{+} - \theta^{+}\right) + Z_{LT} I^{+}\sin\left(\phi_{LT}^{+} + \theta_I^{+}\right) \tag{7}$$

$$v_q^{-} = V_F^{-}\sin\left(\theta_F^{-} - \theta^{-}\right) + Z_{LT} I^{-}\sin\left(\phi_{LT}^{-} + \theta_I^{-}\right). \tag{8}$$

During normal operating conditions where $\theta^{\pm} = \theta_{PCC}^{\pm}$ then $v_q^{+} = v_q^{-} = 0$. To achieve stable synchronization after a disturbance, one must be able to control $v_q^{\pm} = 0$. This means that the following necessary conditions must be satisfied

$$I^{+} \leq \frac{-V_F^{+}\sin\left(\theta_F^{+} - \theta^{+}\right)}{Z_{LT}\sin\left(\phi_{LT}^{+} + \theta_I^{+}\right)}$$

$$\implies I^{+} \leq \frac{V_F^{+}}{\left|Z_{LT}\sin\left(\phi_{LT}^{+} + \theta_I^{+}\right)\right|} \tag{9}$$

and

$$I^{-} \leq \frac{-V_F^{-} sin(\theta_F^{-} - \theta^{-})}{Z_{LT}\sin\left(\phi_{LT}^{-} + \theta_I^{-}\right)}$$

$$\implies I^{-} \leq \frac{V_F^{-}}{\left|Z_{LT}\sin\left(\phi_{LT}^{-} + \theta_I^{-}\right)\right|}. \tag{10}$$

It is observed that the same limitation is present in the positive and the negative sequence network, which makes sense as there are no physical differences between them besides the orientation. Since the negative-sequence current will only be considered during fault conditions where only reactive current is injected, $\theta_I^{-} = \pi/2$ always. Inserting this gives

$$I^{-} \leq \frac{V_F^{-}}{R_L}. \tag{11}$$

Similarly, if nominal capacitive reactive current injection is considered in the positive sequence, i.e., $\theta_I^{+} = -\pi/2$, then

$$I^{+} \leq \frac{V_F^{+}}{R_L}. \tag{12}$$

It can be noticed that under pure reactive current injection, the necessary stability condition is defined by the voltage magnitude at the fault location and the line resistance.

The operating area for which the necessary conditions are satisfied is visualized in Fig. 3. The area is shown for the positive-sequence limitation expressed in (9) during a non-severe fault (Fig. 3(a)) and a severe fault (Fig. 3(b)). Based on these, the following observations can be made:

- If $I^{+} \leq V_F^{+}/Z_{LT}$, any orientation of the current vector will provide a stable operating point during the fault.
- During a severe fault, the stable operating area may diminish such that 1 pu of pure reactive current injection cannot be accomplished (see Fig. 3(b)).
- If the current vector is aligned with the negative impedance angle, i.e., $\theta_I^{+} = -\phi_{LT}$, any current magnitude can be injected while still providing a stable operating point during the fault. This may, however, not comply with the LVRT requirements.

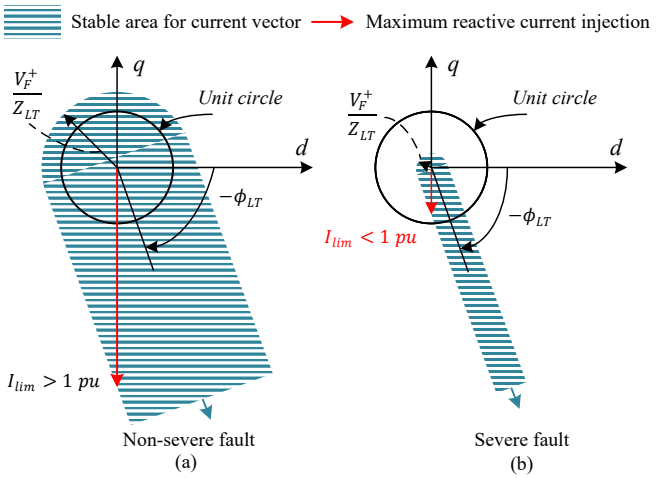

Fig. 3. Positive-sequence stable operating area for injected current vector during (a): a non-severe fault with the possibility for 1 pu pure reactive current injection and (b): a severe fault without the possibility for 1 pu pure reactive current injection.

The observations made from Fig. 3 were exemplified for the positive-sequence model but are equally valid for the negative-sequence one.

With this, the current transfer limits for both sequences during asymmetrical faults are described in (9) and (10). With these at hand, the next step is to identify the expected value of V_F^{+} and V_F^{-} during different fault conditions. By using symmetrical components theory, the sequence components can be calculated as [23]

$$\begin{bmatrix} v_F^{+} \\ v_F^{-} \\ v_F^{0} \end{bmatrix} = \underbrace{\frac{1}{3}\begin{bmatrix} 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \\ 1 & 1 & 1 \end{bmatrix}}_{\mathrm{T}} \begin{bmatrix} v_{Fa} \\ v_{Fb} \\ v_{Fc} \end{bmatrix} \tag{13}$$

where all quantities are phasor quantities, i.e., complex numbers and $\alpha = \mathrm{e}^{\mathrm{j}2\pi/3}$. As the zero-sequence component is not controlled or present in the three-wire system, this is not considered for the necessary conditions. However, the zero-sequence component is present at the secondary side of the step-up transformer due to its grounding configuration.

Considering a single line-to-ground fault (SLG) where phase-a is solidly connected to ground, i.e. $v_{Fa} = 0$, and the remaining phases are unaffected, the symmetrical components of the voltage at the fault location are $V_F^{+} = 2/3$ pu, $V_F^{-} = 1/3$ pu, and $V_F^{0} = 1/3$ pu using (13). This result is valid under the condition that the converter and external grid have no influence on the voltage sequence components at the fault location. Realistically, this is not the case, but it serves as a good way of testing the applicability and accuracy of the static stability limits since the sequence components at the fault location are known and constant.

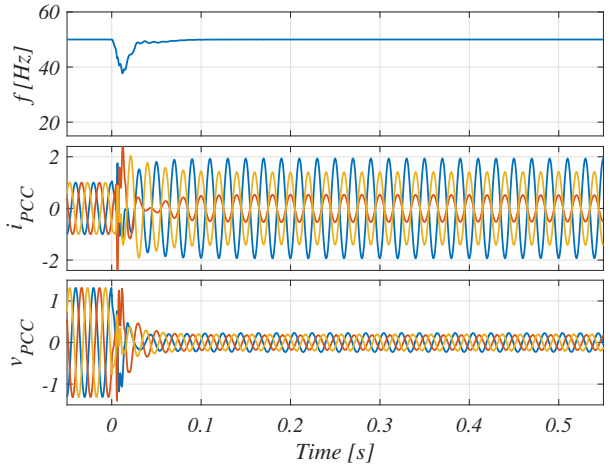

Fig. 4. Detailed system simulation of DLG fault with $R_L = 0.32$ pu which results in a stable response as expected from (11)-(12). 1 pu of current in both sequences are injected where $\theta_I^+ = -\pi/2$ and $\theta_I^- = \pi/2$.

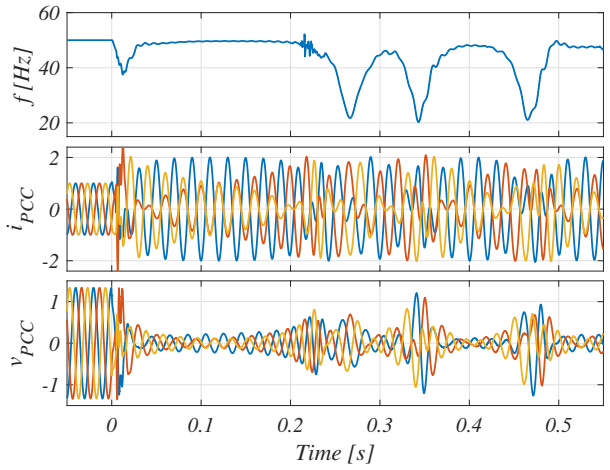

Fig. 5. Detailed system simulation of DLG fault with $R_L = 0.34$ pu, which results in an unstable response as expected from (11)-(12). 1 pu of current in both sequences are injected where $\theta_I^+ = -\pi/2$ and $\theta_I^- = \pi/2$.

Similarly for a solid double line-to-ground (DLG) fault where ($v_{Fb} = v_{Fc} = 0$), and phase-a remains unchanged, the symmetrical components of the voltage at the fault location are $V_F^+ = 1/3$ pu, $V_F^- = 1/3$ pu, and $V_F^0 = 1/3$ pu.

At last, for a line-to-line (LL) bolted fault on phases b and c, the zero sequence remains zero as there is no physical connection to ground, and the positive and negative sequence components are $V_F^+ = 1/2$ pu and $V_F^- = 1/2$ pu, respectively. Considering these three fault types, the DLG fault represents the worst-case sequence components seen from the static stability limits given in (9) and (10). To analyze the derived static limits for current injection, a simulation of a DLG fault is conducted for two cases. One per unit of current is injected in both sequences with $\theta_I^+ = -\pi/2$ and $\theta_I^- = \pi/2$. With this, the stability reduces to the ratio between the sequence component of the fault voltage magnitude and the line resistance. Hence, for a DLG fault with $V_F^+ = V_F^- = 1/3$, stability should result for $R_L = 0.32$ pu and instability would occur for $R_L = 0.34$ pu. These two cases are tested and shown in Fig. 4 and Fig. 5, where the three subfigures show the

TABLE I
MAIN PARAMETERS OF THE SYSTEM SHOWN IN FIG. 1.

Symbol	Description	Physical Value
S_N	Nominal power	2.5 kVA
V_N	Nominal grid voltage	$200 \cdot \sqrt{3}$ V
I_N	Nominal converter current	$6/\sqrt{2}$ A
V_g	RMS grid phase voltage	200 V
f_n	Nominal frequency	50 Hz
V_{dc}	dc-link voltage	730 V
L_{cf}	Converter-side inductor	5 mH
L_{gf}	Grid-side inductor	3 mH
C_f	Filter capacitor	20 μF
f_{sw}	Switching frequency	10 kHz
f_s	Sampling frequency	10 kHz
Z_L	Line impedance	0.23 + 0.073j pu
Z_g	Grid impedance	0.1 pu
X_{tr}	Transformer leakage reactance	0
$K_{p,ic}$	Proportional gain PR controller	10 Ω
$K_{r,ic}$	Resonant gain of PR controller	1000 Ω/s

estimated frequency, the per-unit grid current, and the per-unit PCC voltage. As anticipated, the system remains stable when $R_L < V_F^{\pm}$ whereas it is clearly unstable when $R_L > V_F^{\pm}$. The control and network parameters used for the simulation results are listed in Table I. It should be mentioned that the modeling framework presented in this work is independent of the converter nominal power and that a nominal power of 2.5 kVA is selected to match the experimental test setup presented in Section VI.

For further analysis of the transient stability, (7) and (8) can be viewed as the voltage-angle curves shown in Fig. 6, where the positive-sequence frame is exemplified. When a fault occurs, the voltage-angle curve drops since V_F^+ is reduced to a lower value, initiating a dynamic response in δ^+. For the negative-sequence case, the voltage before the fault would be zero and then shift to a higher value during the fault. For the case shown in Fig. 6(b), there exist no stable operating points during the fault, and the system is clearly unstable. However, in the case in Fig. 6(a), two operating points exist during the fault (point *c* and *d*). From the small-signal analysis around the point *d*, this is an unstable operating point, as it is also highlighted in Fig. 6(c) which shows the q-axis voltage for the cases in Fig. 6(a)-(b). As an example, the system in Fig. 6(a) operates at the operating point *a*. When a fault occurs, the voltage curve drops, and the operating point shift to point *b*. Since v_q^+ is now positive, the frequency in the synchronization unit will increase and the phase-angle of the system will advance till it reaches the new stable operating point *c*. At this point, the frequency of the synchronization unit is still higher than the grid frequency, which causes δ^+ to surpass point *c* towards point *d*. If the frequency deviation of the system returns to zero before point *d*, the phase-angle will again decline and the system will return to the stable operating point *c* and remain stable. However, if δ^+ surpasses point *d*, v_q^+ will be once again positive, which increases the operating frequency, resulting in an unstable response.

From the analysis of the conventional power system, a

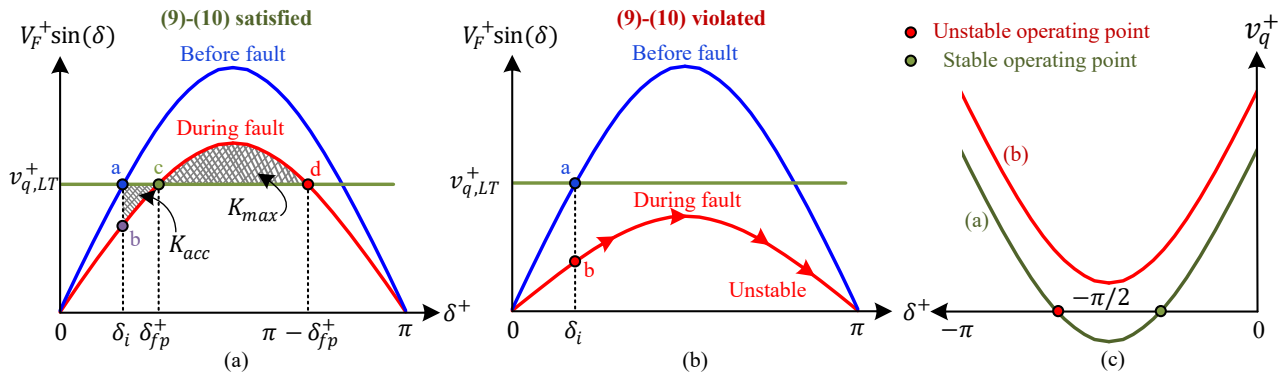

Fig. 6. Transient analysis of faulted system using voltage-angle curves. $\delta^+ = \theta_F^+ - \theta^+$. (a): With a stable operating point during the fault (δ_{fp}^+) and $v_{q,LT}^+ = Z_{LT} I^+ \sin\left(\phi_{LT}^+ + \theta_I^+\right)$. K_{acc} and K_{max} is the accelerating and maximum decelerating area, respectively. (b): Without an operating point during the fault. (c): Visualization of the q-axis components from cases (a) and (b). Only case (a) has a solution to $v_q^+ = 0$

similar power-angle curve is used to describe this and the equal-area criterion may be used for stability assessment [16]. Using the equal-area criterion, it can be shown that if the maximum allowed decelerating area, K_{max}, is larger than the accelerating area, K_{acc}, shown in Fig. 6(a), then the system will remain stable. However, an analytical expression for this is only achieved by neglecting the damping of the system, which makes the equal-area criterion a conservative assessment tool. As can be disclosed by Fig. 6(a), a large damping ratio in the synchronization dynamics will lower the risk of the system trajectory to surpass the unstable point d since a lower overshoot will occur. However, the needed sufficient damping is unknown.

Accordingly, the static limits and the analysis from Fig. 6 serve as a strong tool for analyzing the transient stability of converters during asymmetrical faults if the necessary conditions in (9) and (10) are violated. However, to be able to accurately assess the stability when the necessary conditions are satisfied, the dynamics of the converter synchronization process must be considered. In addition to this, the analysis presented here was based on fixed sequence voltages at the fault location ($V_F^{\pm}$). In a real system, the fault happens due to a short-circuit connection between phases and the ground through a fault impedance. Hence, the sequence voltage at the fault location will not only be dependent on the fault type and fault impedance, but also the currents injected by the converter as well as the external grid. Therefore, the following section aims to derive the sequence voltages at the fault location including the influence of the current injected by the converter and the grid. Additionally, the dynamics of the converter synchronization process (DROGI-FLL) are included to be able to accurately assess the transient stability of the system and the associated critical damping.

IV. Equivalent Sequence-Domain Modeling of VSC

A. Assumptions and Considerations for Model Development

For the proposed model, the converter is being represented as an ideal controllable current source whose orientation is determined by the dynamics of the synchronization unit. Such a representation can be justified for two reasons. First, the dominating dynamics of LOS lies in the low-frequency range [21], [38]. Secondly, the bandwidth of the inner current regulator is usually placed much higher than that of the synchronization process, which facilitates that they can be analyzed individually [6], [15], [16].

To be able to analyze the sequence voltage at the fault location more accurately, the system is being presented in the sequence domain rather than the phase domain [23, p. 458-478]. This is visualized in Fig. 7 where the positive-, negative-, and zero-sequence networks are shown alongside the notation for their Thevenin equivalents seen from the fault location at bus 3. As can be seen, the converter is modeled to inject current in both the positive and negative sequences, whereas the external grid is assumed only to provide positive sequence voltages. Considering the line impedances and the transformer, the positive-sequence, negative-sequence, and zero-sequence impedances are all equal. However, how the path for zero-sequence current develops depends on the winding configuration of the step-up transformer. Since the transformer considered for this study is a *Dyn* type, the path for zero-sequence current is blocked seen from the low-voltage side, whereas a path is formed on the high-voltage side through the ground connection of the star neutral point. The zero-sequence network is then formed via the neutral grounding of the secondary side of the transformer and that of the external grid. Using the sequence-domain representation, the coupled unbalanced set of phasors can be represented as three symmetrical independent networks assuming the network impedances to be internally balanced. Asymmetrical faults do however cause coupling between the sequence networks at the fault location. This coupling is depending on the fault type and will influence how the Thevenin equivalents of the sequence networks should be interconnected.

B. Thevenin Equivalents of Sequence Networks

The Thevenin equivalent for dependent and independent sources, like for this case, is found by first calculating the open-circuit voltage at the fault location (V_{oc}), then the short-circuit current at the fault location (i_{sc}). Finally, the equivalent impedance is computed as $Z_{th} = V_{th}/i_{sc}$.

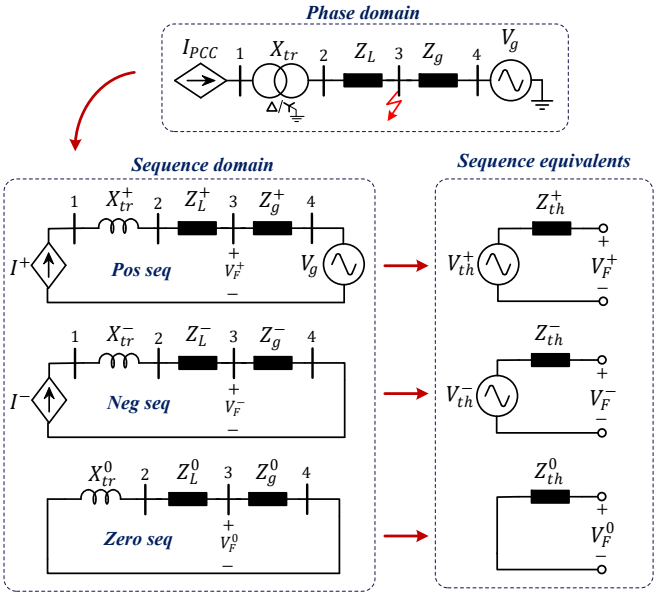

Fig. 7. The considered system shown in phase domain is used to define the sequence domain networks from where the Thevenin sequence equivalents can be derived. The fault location is on bus 3 and the PCC is on bus 1.

For the *positive-sequence network*, the Thevenin voltage can be found to be

$$V_{th}^{+} = V_{oc}^{+} = V_g + I^{+}\mathrm{e}^{\mathrm{j}\theta_{I,oc}^{+}} Z_g^{+} \mathrm{e}^{\mathrm{j}\phi_g} \tag{14}$$

where

$$\theta_{I,oc}^{+} = \tan^{-1}\left(\frac{-I^{+}R_L}{\sqrt{V_g^2 - (I^{+}R_L)^2}}\right) - \frac{\pi}{2}, \tag{15}$$

$$\phi_g = \tan^{-1}\left(\frac{X_g}{R_g}\right), \tag{16}$$

since the phase of the current source is dependent on the phase-angle of the voltage across it, i.e. $\theta_I^{+} = \theta_{PCC}^{+} - \pi/2$ for full reactive current injection during the fault. It should be noted that the value of the square root function will be real for the test cases of interest since the static network limitation is not considered violated. Also, the $\tan^{-1}$ functions presented in this article should be implemented as a four-quadrant inverse tangent function and can, therefore, not be further simplified from what is presented here. Calculating the short-circuit current at the fault location, the positive sequence Thevenin impedance is

$$Z_{th}^{+} = \frac{V_{th}^{+}}{\frac{V_g}{Z_g \mathrm{e}^{\mathrm{j}\phi_g}} + I^{+}\mathrm{e}^{\mathrm{j}\theta_{I,sc}^{+}}} \tag{19}$$

where

$$\theta_{I,sc}^{+} = -\tan^{-1}\left(\frac{X_{tr} + X_L}{R_L}\right). \tag{20}$$

Here, it should be noted that the desired response of $\theta_I^{+} = \theta_{PCC}^{+} - \pi/2$ cannot be achieved during this short-circuit network as the phase difference between the converter voltage and injected current is simply determined by the network impedance.

The *negative-sequence network* only consists of a depending source since the grid voltage has no negative-sequence component. Accordingly, the equivalent voltage is found as for the previous case where the equivalent impedance is found by inserting a known voltage source at the fault location and calculate the resulting current injected by it. Using this, the Thevenin equivalents are found to be

$$V_{th}^{-} = \Gamma V_{oc}^{-} = \Gamma Z_g \mathrm{e}^{\mathrm{j}\phi_g} I^{-} \mathrm{e}^{-\mathrm{j}\theta_{I,oc}^{-}} \mathrm{e}^{\mathrm{j}\theta_{V_{th}}^{+}} \tag{21}$$

$$Z_{th}^{-} = \left(\frac{1}{Z_g \mathrm{e}^{\mathrm{j}\phi_g}} - I^{-}\mathrm{e}^{\mathrm{j}\theta_{I,sc}^{-}}\right)^{-1} \tag{22}$$

where

$$\theta_{I,oc}^{-} = \tan^{-1}\left(\frac{X_g + X_{tr} + X_L}{R_L + R_g}\right), \tag{23}$$

$$\theta_{I,sc}^{-} = \tan^{-1}\left(\frac{I^{-}R_L}{\sqrt{1-(I^{-}R_L)^2}}\right) + \frac{\pi}{2}, \tag{24}$$

$$\theta_{V_{th}}^{+} = \tan^{-1}\left(\frac{I^{+}\left[R_g \sin\left(\theta_{I,oc}^{+}\right) + X_g \cos\left(\theta_{I,oc}^{+}\right)\right]}{V_g + I^{+}\left[R_g \cos\left(\theta_{I,oc}^{+}\right) - X_g \sin\left(\theta_{I,oc}^{+}\right)\right]}\right). \tag{25}$$

Γ represents a sign operator whose value is depending on the phase-angle between the positive and negative sequence networks. For a DLG and an LL fault, the positive and negative sequence voltages at the fault location are in phase ($\Gamma = e^{j0} = 1$), whereas for an SLG fault, the positive and negative sequence voltages are in anti-phase, i.e., ($\Gamma = e^{j\pi} = -1$). The term $\theta_{V_{th}}^{+}$ aligns the negative-sequence frame with the positive sequence one, all referenced to the positive-sequence grid voltage. For $\theta_{I,oc}^{+}$ and $\theta_{I,sc}^{-}$ presented in (15) and (24), it is considered that the positive-sequence current injection is fully capacitive whereas for the negative-sequence current it is fully inductive, i.e., $\theta_I^{+} = -\pi/2$ and $\theta_I^{-} = \pi/2$. Considering that this analysis may also be done for cases where active current is provided in addition to the reactive support, and for completeness, the general expressions for $\theta_{I,oc}^{+}$ and $\theta_{I,sc}^{-}$ are included in (17) and (18) visible on the top of this page.

Finally, for the *zero-sequence network*, the Thevenin equivalents are $V_{th}^{0} = 0$ and

$$Z_{th}^{0} = \frac{Z_g^{0}(X_{tr}^{0} + Z_L^{0})}{Z_g^{0} + X_{tr}^{0} + Z_L^{0}}. \tag{26}$$

C. Sequence Voltages at Fault Location

With the equivalent circuits being derived for each sequence network, the sequence voltage at the fault location including the influence of converter current injection and the external grid is to be derived. As mentioned previously, the interconnection of the sequence networks is determined by the fault condition.

a) SLG Fault: Considering the SLG fault in Fig. 8(a), the following boundary conditions exist: $i_{Fb} = i_{Fc} = 0$ and $v_{Fa} = Z_F i_{Fa}$. With this, the sequence components of the fault currents become

$$\begin{bmatrix} I_F^{+} \\ I_F^{-} \\ I_F^{0} \end{bmatrix} = \mathrm{T} \begin{bmatrix} i_{Fa} \\ 0 \\ 0 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} i_{Fa} \\ i_{Fa} \\ i_{Fa} \end{bmatrix}. \tag{27}$$

$$\theta^+_{I,oc} = \tan^{-1}\left(\frac{I^+\left[(R_L+R_g)\sin(\theta^+_I)+(X_{TL}+X_g)\cos(\theta^+_I)\right]}{\sqrt{V_g^2+(I^+)^2\left[((R_L+R_g)^2-(X_{TL}+X_g)^2)\cos^2(\theta^+_I)-(R_L+R_g)(X_{TL}+X_g)\sin(2\theta^+_I)-(R_L+R_g)^2\right]}}\right)+\theta^+_I \tag{17}$$

$$\theta^-_{I,sc} = \tan^{-1}\left(\frac{I^-\left[R_L\sin(\theta^-_I)+X_{LT}\cos(\theta^-_I)\right]}{\sqrt{1+(I^-)^2\left[(R_L^2-X_{LT}^2)\cos^2(\theta^-_I)-R_LX_{LT}\sin(2\theta^-_I)-R_L^2\right]}}\right)+\theta^-_I \tag{18}$$

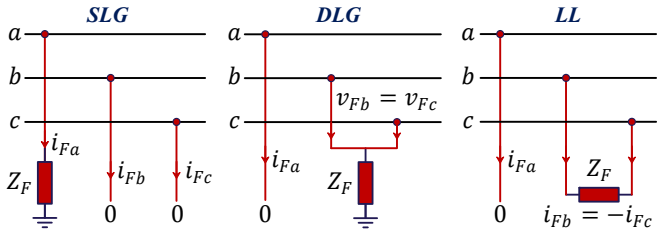

Fig. 8. Phase configurations at fault location for a single line-to-ground (SLG), a double line-to-ground (DLG), and a line-to-line (LL) fault.

From this, the equation for the second boundary conditions can be written in the sequence domain as

$$V_F^+ + V_F^- + V_F^0 = Z_F(I_F^+ + I_F^- + I_F^0) = 3Z_FI^+. \tag{28}$$

To satisfy (27)-(28), the derived sequence networks should all be connected in series at the fault terminals through the impedance $3Z_F$. This is shown in Fig. 9 labeled SLG. Using the sequence representation of the SLG fault, the sequence voltages at the fault location can be readily calculated, and the result is shown in Table II.

b) DLG Fault: For the DLG fault depicted in Fig. 8, the boundary conditions at the fault location are $i_{Fa} = 0$, $v_{Fb} = v_{Fc}$, and $v_{Fb} = Z_F(i_{Fb} + i_{Fc})$. Similarly as for the SLG fault, this is expressed in the sequence domain as

$$I_F^+ + I_F^- + I_F^0 = 0 \tag{29}$$
$$V_F^0 - V_F^+ = 3Z_FI_F^0 \tag{30}$$
$$V_F^+ = V_F^-, \tag{31}$$

which are satisfied if all the equivalent sequence networks are connected in parallel at the fault location, and $3Z_F$ is connected in series with the zero-sequence network. This is shown in Fig. 9 labeled DLG, and the sequence components of the voltage at the fault location are shown in Table II.

c) LL Fault: Finally, the boundary conditions for the LL fault shown in Fig. 8(c), are $i_{Fa} = 0$, $i_{Fb} = -i_{Fc}$, and $v_{Fb} - v_{Fc} = Z_Fi_{Fb}$. Transforming this to the sequence domain gives the conditions

$$I_F^0 = 0 \tag{32}$$
$$I_F^+ = -I_F^- \tag{33}$$
$$V_F^+ - V_F^- = Z_FI_F^+, \tag{34}$$

which are satisfied if the positive and negative sequence networks are paralleled through Z_F as shown in Fig. 9 labeled LL. For the LL fault, the sequence voltages at the fault terminals are as well contained in Table II.

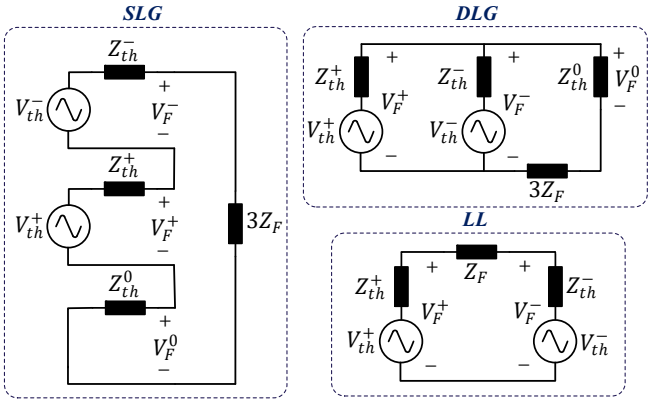

Fig. 9. Interconnection of equivalent sequence domain models for an SLG, a DLG, and an LL fault.

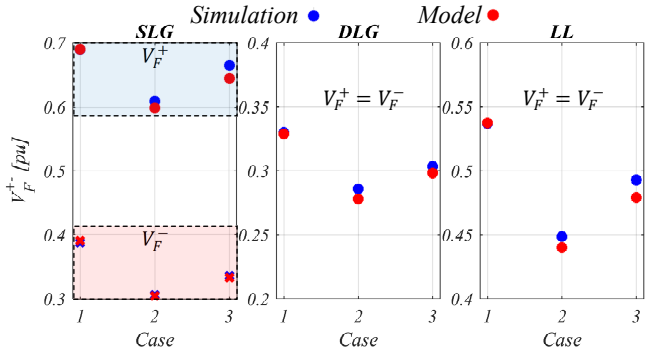

Fig. 10. Comparison of steady-state sequence voltages at fault location for different fault types and current injections (cases) between detailed simulation model and model from Table II. Case 1 is $I^+ = 1$, $I^- = 0$, Case 2 is $I^+ = 0$, $I^- = 1$, and Case 3 is $I^\pm = 1$, all in per unit. For all cases, $\theta^+_I = -\pi/2$ and $\theta^-_I = \pi/2$. Dots denote positive-sequence voltages and crosses denote negative-sequence voltages.

d) 3LG Fault: For completeness, the symmetrical three-phase fault is included. In this case, all phases are influenced identically by the fault. Hence, the balanced system remains symmetrical after the fault, and only the positive sequence voltage component will exist. This condition is modeled by shorting the positive-sequence equivalent network through the fault impedance Z_F. The voltage at the fault location considering a three-phase symmetrical fault is as well shown in Table II.

e) Effect of Transformer Phase Shift: For the *Dyn* transformer, a phase shift between the primary-side and secondary-side voltage will be present, which is not considered in the above model. In addition to this, the factor of $\sqrt{3}$ and the

TABLE II
EXPRESSIONS FOR CALCULATING SYMMETRICAL COMPONENTS AT FAULT LOCATION FOR DIFFERENT FAULT TYPES.

	SLG	DLG	LL	3LG
V_F^+	$V_{th}^+ - \frac{Z_{th}^+(V_{th}^+ + V_{th}^-)}{Z_{th}^+ + Z_{th}^- + Z_{th}^0 + 3Z_F}$	$\frac{(V_{th}^+ Z_{th}^- + V_{th}^- Z_{th}^+)(Z_{th}^0 + 3Z_F)}{Z_{th}^+ Z_{th}^- + Z_{th}^+ Z_{th}^0 + Z_{th}^- Z_{th}^0 + 3Z_F(Z_{th}^+ + Z_{th}^-)}$	$V_{th}^+ - \frac{Z_{th}^+(V_{th}^+ - V_{th}^-)}{Z_{th}^+ + Z_{th}^- + Z_F}$	$\frac{V_{th}^+ Z_F}{Z_{th}^+ + Z_F}$
V_F^-	$V_{th}^- - \frac{Z_{th}^-(V_{th}^+ + V_{th}^-)}{Z_{th}^+ + Z_{th}^- + Z_{th}^0 + 3Z_F}$	$\frac{(V_{th}^+ Z_{th}^- + V_{th}^- Z_{th}^+)(Z_{th}^0 + 3Z_F)}{Z_{th}^+ Z_{th}^- + Z_{th}^+ Z_{th}^0 + Z_{th}^- Z_{th}^0 + 3Z_F(Z_{th}^+ + Z_{th}^-)}$	$V_{th}^- - \frac{Z_{th}^-(V_{th}^+ - V_{th}^-)}{Z_{th}^+ + Z_{th}^- + Z_F}$	0
V_F^0	$\frac{Z_{th}^0(V_{th}^+ + V_{th}^-)}{Z_{th}^+ + Z_{th}^- + Z_{th}^0 + 3Z_F}$	$V_F^+ \frac{Z_{th}^0}{Z_{th}^0 + 3Z_F}$	0	0

turns-ratio of the transformer are neglected since they can be included in the per-unit representation of the impedances.

For accurate modeling, this phase-shifting effect should be considered. This paragraph is devoted to describing why neglecting the phase shift can be justified. At first, since this model only cares about the magnitude of the sequence voltages at the fault location, the transformer phase shift has no impact on the negative sequence model. This is the case since the circuit only contains a single acting source. Hence, a 30° phase shift in the voltages produces a 30° phase shift in the currents, which does not affect the magnitude. However, for the positive-sequence model when evaluating the open-circuit voltage as in (14), a 30° shift in the secondary-side voltage will not necessarily cause a 30° shift in the secondary-side current due to the presence of the external grid voltage. However, modeling the accurate phase-shifting effect on the secondary-side currents starts to complicate the model significantly [39], which reduces the applicability of the reduced-order simplified model. To investigate the error associated with neglecting the phase shift, the predicted positive and negative-sequence voltages at the fault location for different current injections are compared to a detailed simulation model, including the transformer dynamics. As seen from the simulated results and the model in Fig. 10, the error associated with this assumption is low, while the model complexity is kept reasonable. Only the positive-sequence voltages are shown for the DLG and LL faults since the negative sequence ones are the same in this case. It is evident that the modeled results closely match the simulated results, including feedback control, sequence extraction, and a detailed transformer model. To that end, the presented model seems to underestimate the voltages a bit which gives some beneficial conservatism as instability is more likely to occur when $V_F^{\pm}$ is low.

It should be noted that the equivalent sequence-domain modeling applied in this section is a well-known approach used in traditional power system fault studies [23]. However, the model presented here distinguish itself in several ways compared to the traditional and prior art approaches:

1) Contrary to a synchronous machine, the grid-connected converter is represented in both the positive-sequence and the negative-sequence frame.
2) The expressions for the Thevenin equivalents are not just based on constant operating values, but on the LVRT operation where the injected converter current is depending on the phase-angle of the PCC voltage.
3) Finally, the above points are used to establish an analytical expression for $V_F^{\pm}$ during different fault types, which is directly used in the q-axes equations in (7)-(8) to formulate a reduced-order large-signal model.

V. REDUCED-ORDER LARGE-SIGNAL MODEL WITH EQUIVALENT PLL DYNAMICS

A general grid-following converter control during asymmetrical faults consists of a sequence extractor (synchronization unit), a reference current generation algorithm (outer power loops and grid code requirements), and a current controller. For this work, the sequence extractor is the block estimating $\theta_{PCC}^{\pm}$, performed by the DROGI-FLL shown in Fig. 2(b). Outer loops are neglected for this analysis and the dq-frame positive- and negative-sequence current references are directly specified based on the grid-code requirements. Finally, the converter currents are controlled using a PR controller. The following text aims to accomplish the final task of completing the reduced-order large-signal model of grid-following converters with dual-sequence current injection.

The simplified large-signal model for grid-synchronization stability assessment, shown in Fig. 11, is developed by connecting the grid-interaction model from Section IV with the employed synchronization unit, here the DSOGI-FLL. This is a closed-loop feedback system that consists of the dynamical model of the DROGI-FLL and the previously described interaction between the converter and the grid during fault conditions. Accordingly, the generality of the proposed reduced-order model is twofold: 1), the proposed model is general for any short-circuit fault condition, including both symmetrical and asymmetrical faults, and 2) since the dynamics of the synchronization unit are attached to the reduced-order structure as shown in Fig. 11, the proposed modeling approach does not require a specific synchronization unit to be used. Thus, the large-signal modeling method is also general towards the synchronization unit employed. Instead of the DROGI-FLL used here, any other method could be attached instead (e.g. PLLs, FLLs, etc.).

A. Model Validation

The proposed model is compared with a detailed switching simulation model performed in MATLABs Simulink with

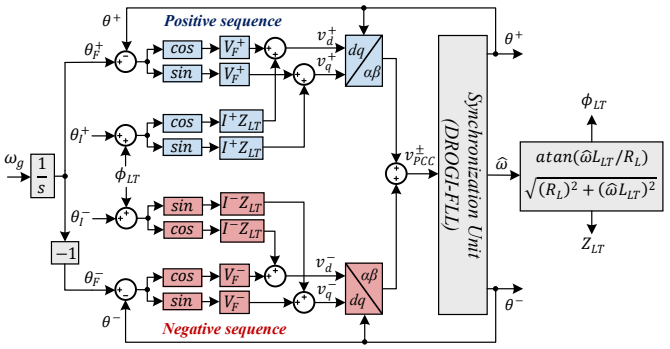

Fig. 11. The proposed simplified large-signal model for grid-synchronization stability evaluation during asymmetrical fault conditions. V_F^+ and V_F^- are obtained from Section IV based on the fault type and converter operating mode.

TABLE III
BOUNDARY OF SYNCHRONIZATION STABILITY OF THE PROPOSED MODEL AND DETAILED SIMULATION MODEL BY VARYING ω_N IN THE DROGI-FLL

Fault Type	Stable?	Proposed Model	Simulation Model
SLG	✔	$\omega_N = 34$	$\omega_N = 36$
$I^+, I^- = 1, 1$	✘	$\omega_N = 35$	$\omega_N = 37$
DLG	✔	$\omega_N = 22$	$\omega_N = 21$
$I^+, I^- = 1, 0$	✘	$\omega_N = 23$	$\omega_N = 22$
DLG	✔	$\omega_N = 18$	$\omega_N = 19$
$I^+, I^- = 1, 1$	✘	$\omega_N = 19$	$\omega_N = 20$
LL	✔	$\omega_N = 39$	$\omega_N = 42$
$I^+, I^- = 1, 0$	✘	$\omega_N = 40$	$\omega_N = 43$
LL	✔	$\omega_N = 27$	$\omega_N = 33$
$I^+, I^- = 1, 1$	✘	$\omega_N = 28$	$\omega_N = 34$

PLECS blockset of the system shown in Fig. 1. The converter is operated as grid-following with the control structure as shown in Fig. 2(a). The parameters for the simulation model and the proposed model are listed in Table I.

To test and compare the developed model against a detailed simulation model of the system, a given fault type and current injection are selected. Then the tuning of the DROGI-FLL is swept to identify the tipping point between stability and instability for that given fault condition. The DROGI-FLL has two control parameters, k, λ, which are designed as

$$k = \frac{2\omega_N}{\sqrt{2}}, \quad \lambda = \omega_N^2. \tag{35}$$

By evaluating the damping ratio of the second-order linearized model of the DROGI-FLL, one will find that $\zeta \propto \frac{1}{\omega_N^2}$. Therefore, by decreasing the natural angular frequency ω_N, the damping ratio can be increased. For the model verification, it is ω_N, which is varied to identify the boundary of stability and the critical damping ratio. Five different scenarios are tested, and the results of the proposed model and the simulation model are shown in Table III. For each case, the stability boundary of the system is identified as shown with a stable and an unstable case excited by an increase of 1 unit in ω_N. Besides the fault type, the converter current injections are shown for both sequences in per-unit.

As can be seen, the reduced-order model predicts the stability boundary well for the tested fault conditions. As expected, the proposed model is a bit conservative in the stability assessment during SLG faults as disclosed from Fig. 10. A nearly exact match is evident in the case of a DLG fault. This is convenient since this fault type represents the worst-case asymmetrical fault type.

It is noticed that the largest error occurs for the LL faults. Here, it matches the analysis from Fig. 10 that case 1 for the LL fault has a lower error compared to case 3 where current injection is performed in both sequences. For the SLG fault and especially for the LL fault, the resulting voltages at the fault location is higher compared to the DLG fault case. This implies that the assumption of neglecting the phase shift caused by the transformer will be less valid, which causes the increased error observed.

VI. Experimental Verification

To experimentally verify the presented model, the laboratory test setup shown in Fig. 12 is used. An active rectifier is used to establish the dc-link potential of the grid-connected converter under test. The grid-connected converter is a Danfoss VLT FC-302 inverter, which is being controlled using a dSPACE expansion box, including a DS1007 PPC processor board for code actuation, DS5101 digital waveform output board for PWM generations, and a DS2004 high-speed A/D board for voltage and current sensing. The PCC voltages and converter-side currents are used for actual converter control, whereas the PCC currents are only measured for visualization and plotting. The Danfoss inverter is connected to an LCL-filter and a passive impedance, which emulates the line impedance of the model. A realistic fault scenario would require to directly short one or more phases of the ac-supply to the grounding terminal of the step-up transformer. Since this draw large short-circuit currents, beyond the specifications of the laboratory equipment, the Dyn transformer is neglected for the experimental verification. Instead, the asymmetrical and symmetrical fault voltages are directly emulated at the fault location using a Chroma Regenerative Grid Simulator Model 61845. This also means that Z_g, as shown in Fig. 1, is set to zero. The remainder of the system parameters for the experimental setup are as listed in Table I.

Like for the previous model verification, ω_N is swept for different fault types and current injections to estimate the stability boundary of the system. The results of this for the proposed model, the simulation model, and the experimental setup are presented in Table IV. Here, the proposed model well matches the simulation model, with a tiny amount of conservatism compared to the experimental results. This indicates that the reduced-order model is well equipped for transient stability assessment under asymmetrical and symmetrical grid faults. The small underestimation in the stability boundary by the proposed model is caused by the non-ideal inner current controller, which adds a stabilizing effect to the system, since it slows the response a bit. The experimental cases marked in blue in Table IV represent the cases where detailed experimental waveforms are shown in Figs. 13-15. On each figure, the five sub-figures are the three-phase PCC currents,

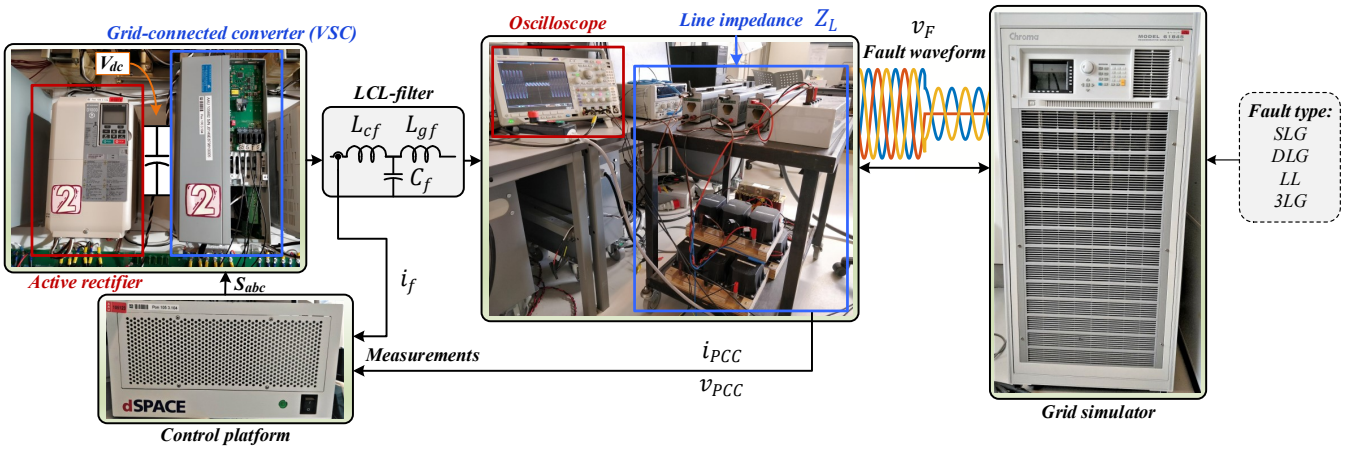

Fig. 12. The laboratory test setup used for experimental verification. A programmable grid simulator is used to generate the different grid faults, and a grid-connected converter is interfaced through a line impedance.

TABLE IV
BOUNDARY OF SYNCHRONIZATION STABILITY OF THE PROPOSED MODEL, DETAILED SIMULATION MODEL, AND THE EXPERIMENTAL TEST SETUP BY VARYING ω_N IN THE DROGI-FLL

Fault Type	Stable?	Proposed Model	Simulation	Experimental
SLG	✔	$\omega_N = 38$	$\omega_N = 40$	$\omega_N = 41$
$I^+, I^- = 1, 1$	✘	$\omega_N = 39$	$\omega_N = 41$	$\omega_N = 42$
DLG	✔	$\omega_N = 28$	$\omega_N = 28$	$\omega_N = 29$
$I^+, I^- = 1, 0$	✘	$\omega_N = 29$	$\omega_N = 29$	$\omega_N = 30$
DLG	✔	$\omega_N = 22$	$\omega_N = 22$	$\omega_N = 22$
$I^+, I^- = 1, 1$	✘	$\omega_N = 23$	$\omega_N = 23$	$\omega_N = 23$
LL	✔	$\omega_N = 37$	$\omega_N = 37$	$\omega_N = 38$
$I^+, I^- = 1, 0$	✘	$\omega_N = 38$	$\omega_N = 38$	$\omega_N = 39$
LL	✔	$\omega_N = 33$	$\omega_N = 33$	$\omega_N = 33$
$I^+, I^- = 1, 1$	✘	$\omega_N = 34$	$\omega_N = 34$	$\omega_N = 34$
3LG	✔	$\omega_N = 26$	$\omega_N = 26$	$\omega_N = 26$
$I^+, I^- = 1, 0$	✘	$\omega_N = 27$	$\omega_N = 27$	$\omega_N = 27$

the positive- and negative-sequence currents at the PCC, the estimated frequency of the DROGI-FLL, the PCC voltages, and the PCC voltage sequence components. Since the SLG fault represents the least severe asymmetrical fault from the loss of synchronization point of view ($V_F^+ = 2/3\,pu$ and $V_F^- = 1/3\,pu$), ω_N can be increased significantly before instability occurs. For the SLG case in Fig. 13(a), the boundary of stability occurs for $\omega_N = 41\,rad/s$, which results in low damping of the synchronization dynamics. This low damping is clearly observed in the weakly-damped oscillations in Fig. 13(a), which causes undesired harmonic oscillations in the injected currents. When the damping is further reduced as shown in Fig. 13(b), instability occurs where synchronization is fully lost and the system is unable to resynchronize to the grid after the fault has been cleared. For the more severe DLG fault in Fig. 14, it can be seen that system is much more damped compared to the cases in Fig. 13 and Fig. 15 since a lower ω_N (larger damping) is needed for the system to remain stable. As seen in Fig. 13-Fig. 15, besides matching the stability assessment using the proposed model, it can be observed that if synchronization is lost, the PCC voltages are not properly supported during the fault and the system might not be able to resynchronize to the grid after the fault clearance. This highlights the desire for being able to predict and avert large-signal synchronization instability during such conditions.

In addition to the transient stability evaluation, the time-domain waveform of the estimated FLL frequency of the proposed model is compared to the experimental results for the DLG fault in Fig. 14. This is shown in Fig. 16, where, despite the simplified model structure, a good match is observed in the estimated frequencies for the proposed model and the measured results. Hence, the presented reduced-order model based on the sequence-domain equivalent modeling is well capable to evaluate the stability under asymmetrical and symmetrical faults. This is also the case when considering the step-up transformer as shown in Table III. However, the neglect of the transformer phase shift is seen to cause the largest error during LL faults, whereas the results obtained for the SLG and DLG faults are accurate.

VII. CONCLUSION

The modeling of synchronization stability of grid-following converters during asymmetrical grid faults is addressed. Necessary conditions for synchronization stability are derived for both sequences frames, which is shown to be a strong tool for stability assessment. To capture the dominating dynamics of the system in respect to loss of synchronization, Thevenin equivalents in all sequence frames are derived, taking into account converter current injection in both the positive and negative-sequence frames and the fault type of interest. Based on this and the synchronizing dynamics of the DROGI-FLL, the proposed reduced-order large-signal model for grid-synchronization stability assessment is established. The proposed model is carefully verified against a detailed simulation study and an experimental laboratory set up revealing its strong stability assessment capability with a simple modeling structure. The presented modeling framework is general for any short-circuit fault type and is not restricted to a specific algorithm for sequence extraction and synchronization.

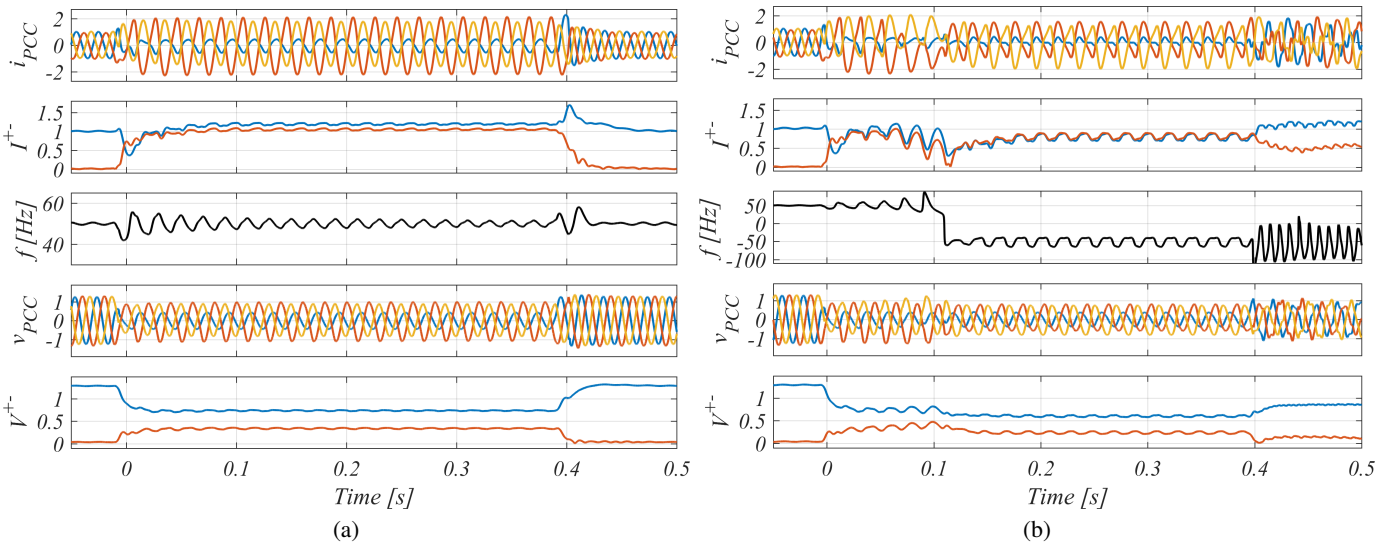

Fig. 13. **Experimental** results for an SLG fault with $I^+ = 1$ and $I^- = 1$. (a): Stable response with $\omega_N = 41\,rad/s$. (b): Unstable response with $\omega_N = 42\,rad/s$.

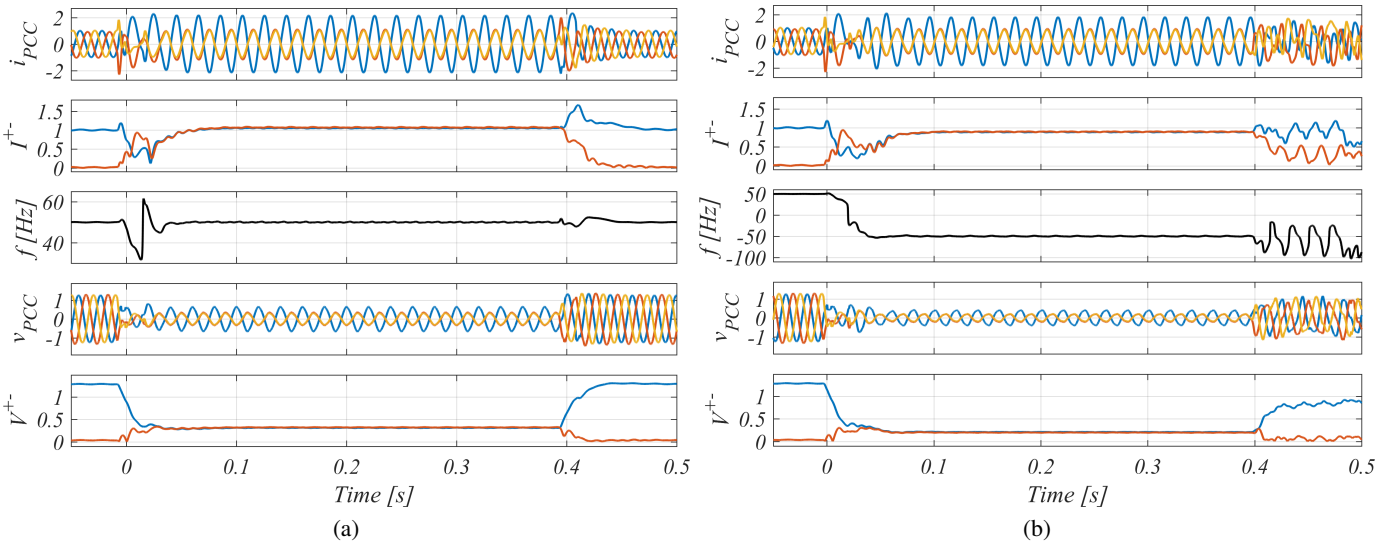

Fig. 14. **Experimental** results for a DLG fault with $I^+ = 1$ and $I^- = 1$. (a): Stable response with $\omega_N = 22\,rad/s$. (b): Unstable response with $\omega_N = 23\,rad/s$.

Accordingly, the presented model is useful in understanding the governing dynamics of synchronization stability during faults and may, with its low-order structure, be well suited for design-oriented studies or large-scale power system studies where a high-order detailed time-domain model is not feasible.

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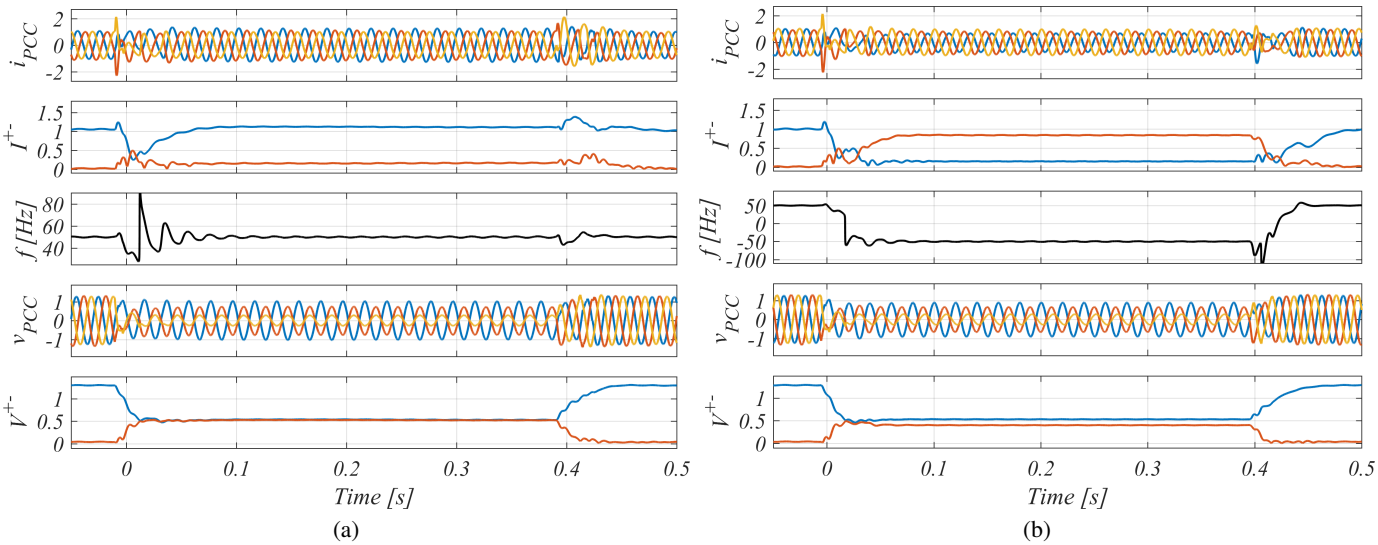

Fig. 15. **Experimental** results for an LL fault with $I^+ = 1$ and $I^- = 0$. (a): Stable response with $\omega_N = 38\,rad/s$. (b): Unstable response with $\omega_N = 39\,rad/s$.

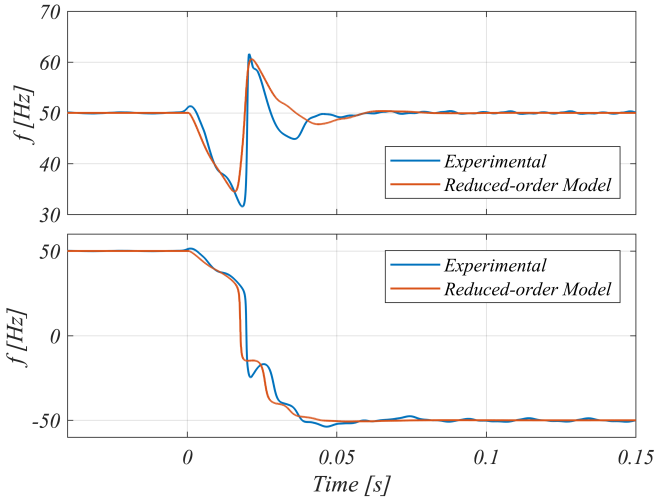

Fig. 16. Time-domain waveform comparison between the proposed reduced-order model and the experimental results for a DLG fault with $I^+ = 1$ and $I^- = 1$. The top stable responses are with $\omega_N = 22\,rad/s$. The bottom unstable responses are with $\omega_N = 23\,rad/s$.

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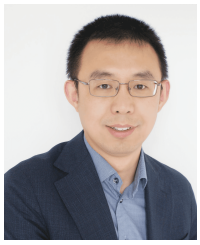

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