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Published in:
I E E E Transactions on Industrial Electronics

DOI (link to publication from Publisher):
10.1109/TIE.2020.3018073

Publication date:
2020

Document Version
Accepted author manuscript, peer reviewed version

Design, Control, and Analysis of a Novel Grid-Interfaced Switched-Boost Dual T-Type Five-Level Inverter With Common-Ground Concept

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***Abstract*- Multilevel inverters with a common-ground (CG) structure and voltage step-up feature are beneficial for transformerless grid-connected photovoltaic applications. The aim of this study is to present a novel topology of such converters with a five-level output voltage generation. The proposed topology comprises of an integrated switched-boost (SB) module and a dual T-Type (D2T) cell constructed with 10 power switches (six unidirectional and two bi-directional). An inductor in the integrated SB module is used to boost the voltage across two involved capacitors of the D2T cell. Therefore, a desirable ac voltage magnitude for the grid-connected application can be achieved over a wide range of input voltage changes. Current stress is also kept within a permissible input current range by the soft-charging operation of the involved capacitors through the inductor. A corresponding dead-beat continuous-current-control-set controller with a sinusoidal PWM modulator is implemented for controlling the real and reactive powers. The controller has an added benefit of achieving constant switching frequency for power switches. Circuit description, theoretical analyses, and comparative study are discussed. Simulation and experimental results are also presented to confirm the feasibility and correctness of the proposed topology.**

***Index Terms*- Common-grounded, Transformerless inverter, Switched-boost module, Soft charging operation.**

I. INTRODUCTION

TRANSFORMERLESS (TL) photovoltaic (PV) string inverters with the capability of either removing or mitigating the leakage current concern have been recently researched as the ubiquities solution for improving the overall efficiency of a grid-connected PV system [1]-[3]. The variable common-mode voltage (CMV) during the switching states is the main origin of the leakage current concern. This CMV is clamped across the stray capacitor between the PV panel's negative terminal and the ground. Therefore, the leakage current can be circulated within a resonant path between such a mentioned stray capacitor and the filter inductors of the inverter [3]. The conventional three-level (3L) and five-level (5L)-TL inverters derived from improved version of the full-H bridge (FB) structures have been recently strived to control the CMV during the freewheeling period. H5 [4], Optimized H5 [5], HERIC [6], different families of H6 [7]-[8], and Variant 5LH8-TL [9] inverters are the famous circuit architectures of this category.

Active Neutral Point Clamp (ANPC)-TL inverters with the integrated Flying Capacitor (FC) cell and T-Type legs have also been seen as an alternative solution to maintain a constant CMV and reduce the leakage current concern. Here, power quality enhancement of the grid-connected system can also be improved since they are able to generate higher number of inverter output voltage levels [10]-[12]. However, the conventional ANPC-TL inverters suffer from capacitors voltage balancing and the need of higher dc input voltage utilization. The static voltage gain of such converters with self-voltage balancing of the integrated FC cells is improved in [13-15] although owing to the discontinuous nature of the input current, the current stresses of the capacitive charging loop semiconductors remain still high.

Common-Ground (CG)-TL inverters have also recently emerged and can readily nullify the leakage current [16]-[25]. The basic concept of such structures is to use a virtual dc-link capacitor charged during the positive and/or zero level of the output voltage. Then, such a charged voltage of this virtual dc-link capacitor is used to supply the output through making the negative output voltage levels. Different types of two-level (2L) [16] and 3L CG-based structures [17]-[19] have used this concept, whereas by integrating the CG feature with the FC cell [20]-[21], the number of output voltage levels can be even increased up to five. Herein, still the dc input voltage utilization is the major problem since all the mentioned types of CG-based TL inverters possess a buck-type feature. Regarding this, some advanced and reduced components counts of 3L [22]-[23], and 5L [24]-[25] CG-based TL inverters have been put forward in the latest years by incorporating the switched-capacitor (SC) cell, which provide a valuable voltage boosting property. Hence, a much lower number of the PV string panels can be used as the input voltage for these types of converters.

Even though there are many propitious achievements in these advanced types of CG-based TL inverters, the discontinuous nature of the input current during the charging operation of the capacitors, and the extremely high value of the inrush current caused by the capacitive charging loop impose additional design protection and consideration. Also, owing to the longer discharging time interval of such a mentioned virtual dc link capacitor, the output voltage of the inverter is not quite smooth and symmetric in both half cycle. So, the dc-bias injection might be another problem to mitigate [24].

Having taken the above-mentioned contribution, a novel CG-based 5L-TL inverter is presented in this study. The proposed topology is comprised of a switched-boost (SB) module connecting to a dual T-Type (D2T) cell constructed with 10 power switches (six unidirectional and two bi-directional), two-dc link capacitors and a single inductor.

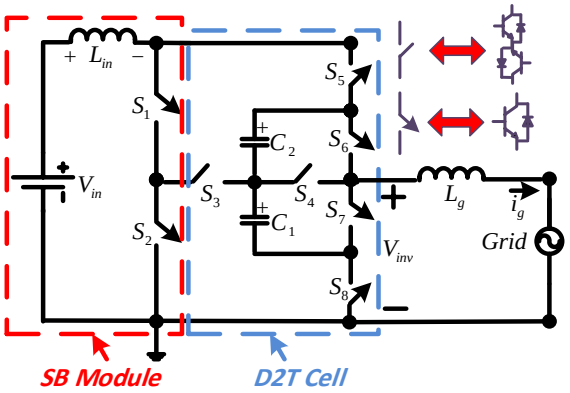

Fig. 1. The overall structure of the proposed SBD2T5L-TL inverter.

Herein, through the appropriate duty cycle adjustment of the SB module with the contribution of one power switch from the D2T cell at each instant, a valuable voltage boosting feature to cope up with the wide input voltage changes is achieved. The proposed topology is named as SBD2T5L-TL inverter and apart from the mentioned capabilities, it possesses a soft charging operation ability, which makes it an applicable topology for the PV-based grid-connected systems. Therefore, the current stresses profile of all the involved capacitors and switches can also be limited to the input dc source current. Also, since all the output voltage levels are made by the aim of the capacitors, so as opposed to the conventional CG-based TL inverters, both the half cycle of the proposed inverter's output voltage are symmetric without any dc offset/bias injection. In order to control the voltage of the dc-link capacitors and also to inject active and reactive powers to the grid, a dead-beat continuous-current-control-set (DB3CS) controller with a constant switching frequency is implemented. Rest of this paper is organized by the following Sections.

The circuit description of the proposed SBD2T5L-TL inverter is studied in Section II. The proposed modulation/control procedure is explained in Section III. The design guidelines of the passive involved elements are conducted in Section IV. Current stress analysis is given in Section V, while the comparative study with the experimental verification results are presented in Section VI and VII, respectively. Finally, some conclusions are presented in Section VIII.

II. Proposed SBD2T5L-TL Inverter

The overall circuit configuration of the proposed topology is depicted in Fig. 1. A single inductor, two unidirectional power switches (S_1 and S_2), and a single input dc voltage source, which can represent the PV string panels, are included in the integrated SB module, while four unidirectional (S_5, S_6, S_7, and S_8) and two bidirectional power switches (S_3 and S_4) with two additional dc-link capacitors (C_1 and C_2) form the D2T cell. Here, the integrated SB module acts as the conventional boost-converters [18] and therefore, with a proper switching conversion over a full cycle of the grid frequency, a boosted voltage across both the dc-link capacitors of the D2T cell within a single stage energy conversion platform can be achieved. Using these capacitors voltage, five different output voltage levels can also be made. As the grid-connected application is subject, the proposed topology is also tied to the grid via a single L-type filter. Regarding the CG connection between the null of the grid and the negative terminal of the input dc source, the concern of leakage current injection is also removed. The switching states of the proposed SBD2T5L-TL inverter are analyzed as illustrated in Fig. 2. Here, the charging loop of the capacitors is shown by the blue lines, whereas, the grid current flowing path is indicated by the red lines. Also, the green lines indicates the input inductor (L_{in}) charging flowing path. Regarding these noted notions, the circuit description of the proposed topology is discussed as follows:

1) *The zero level of the output voltage (First redundant state)*

In respect to Fig. 2(a), the zero level of the output voltage can be made by turning ON contribution of S_1, S_7, and S_8, while S_2 and S_3 have a complementary ON/OFF operation and they are in the charging path of L_{in} and C_1, respectively. Here, once S_2 is ON, the input current (i_{in}) is linearly increased to charge the L_{in}; therefore, considering V_{dc} as the input dc source, the following relation can be expressed:

$$v_{Lin} = V_{dc} \xrightarrow{S_1 and\ S_2:ON} \text{Charging of } L_{in} \quad (1)$$

where, v_{Lin} is the instantaneous voltage across the L_{in}.

Also, whenever S_3 is ON, the input current is reduced and C_1 is charged as follows:

$$V_{C1} = V_{dc} + v_{Lin} \xrightarrow{S_1, S_3 and S_8:ON} \text{Charging of } C_1 \quad (2)$$

where, V_{C1} is the steady state voltage across C_1.

So, considering d as the supposed duty cycle ratio of the involved complementary switches over the switching frequency, V_{C1} can be taken by:

$$V_{C1} = \frac{V_{dc}}{1-d} \quad (3)$$

It can be deduced that through such a mentioned current flowing path, C_2 is disconnected from the grid and the input dc source. Concerning this switching conversion, the injected grid current with unity power factor (PF) direction is passed through the anti-parallel internal power diode of S_7 and the power switch S_8, whereas as for the non-unity PF demanded by the grid, the power switch S_7 and the anti-parallel diode of S_8 are conducting.

2) *The zero level of the output voltage (Second redundant state):*

A redundant zero state is also possible as shown in Fig. 2(b). Here, S_2, S_3, and S_4 must be ON, while S_1 and S_5 have a complementary operation with each other. It is clear that once S_1 is ON, the L_{in} gets charged through the input dc source and whenever S_5 is to be ON, the charged voltage of L_{in} and the input dc voltage are pumped to C_2 and therefore C_2 is charged by (4):

$$V_{C2} = V_{dc} + v_{Lin} \xrightarrow{S_1, S_3 and S_5:ON} \text{Charging of } C_2 \quad (4)$$

where, V_{C2} is the steady state voltage across C_2.

So, with respect to (1) and (4) and with a similar principle as given for V_{C1}, V_{C2} can be obtained as:

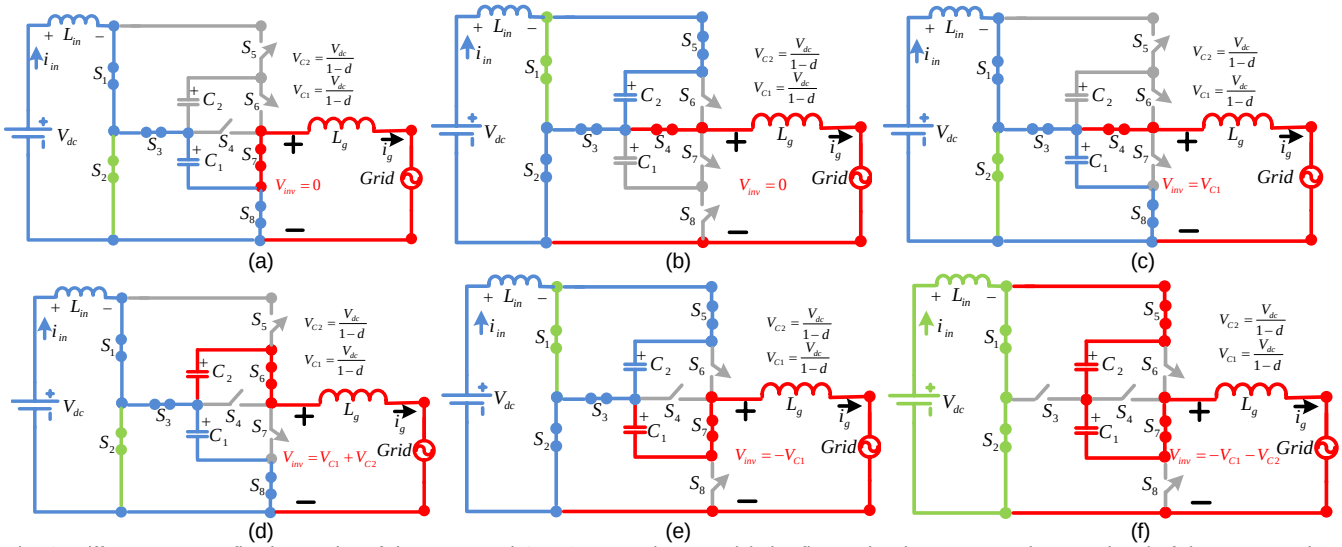

Fig. 2. Different current flowing paths of the proposed SBD2T5L-TL inverter (a) the first redundant state at the zero level of the output voltage (b) the second redundant state at the zero level of the output voltage (c) at the first positive level of the output voltage (d) at the top positive level of the output voltage (e) at the first negative level of the output voltage, and (f) at the top negative level of the output voltage.

$$V_{C2} = \frac{V_{dc}}{1-d} \quad (5)$$

Here, as opposed to the previous redundant state for the zero-level of the output voltage shown in Fig. 2 (a), C_1 is disconnected from the grid and the dc input. Also, the grid current flowing path for non-unity PF belongs to the conduction path of S_3, and S_4 associated with the power switch S_2.

3) The first positive level of the output voltage:

As shown in Fig. 3 (c), the first positive output voltage level is created by the aim of the pre-charged voltage value of C_1 and the ON state contribution of S_1, S_4, and S_8, whereas similar to the first redundant state as for the zero-level of the output voltage, S_2 and S_3 must be switched with a complementary switching scheme. So, with hindsight to (1) and (2), C_1 can still be charged to its steady state voltage as expressed in (3), while C_2 is again disconnected from the grid and the dc input supply. Here, similar to the charging path provided by the second redundant state for the zero-level of the output voltage, the reverse grid current caused by a non-unity PF condition is passed through S_3, S_4 and S_2, while C_1 can be charged from both the input dc source and the grid at the same time.

4) The top positive level of the output voltage:

As shown in Fig. 2 (d), this output voltage level is made by the contribution of both the involved capacitors and the ON state aim of S_1, S_6, and S_8. Here, to keep on the charging process of C_1 similar to the previous stage, S_2 and S_3 still must be ON/OFF with a complementary principle. So, regarding (3) and (5), the maximum value of the inverter output voltage ($V_{inv,max}$) is made as:

$$V_{inv,max} = V_{C1} + V_{C2} = \frac{2V_{dc}}{1-d} \quad (6)$$

Regarding the red and blue lines of the current flowing path shown in Fig. 2(d), it is evident that the direction of the injected grid current (i_g) is of importance for the charging/discharging operation of C_2. It is also apparent that in case of non-unity PF condition, the grid current flowing path is formed through the anti-parallel internal power diode of S_6, the capacitor C_2, and the power switches S_2 and S_3.

5) The first negative level of the output voltage:

In order to generate the first negative level of the output voltage, Fig. 2 (e) must be considered. As is clear, three power switches as S_2, S_3, and S_7 must be ON, while similar to the second redundant state of the zero-level output voltage (Fig. 2(b)), S_1 and S_5 have a complementary operation with each other. So, the output voltage of the inverter is generated by the contribution of C_1, whereas C_2 is charged to its steady state value. Here, in case of unity PF, C_1 is charged, while it would be discharged when a non-unity PF operation is demanded.

6) The top negative level of the output voltage:

Finally, the top negative level of the output voltage is constructed by the sole contribution of C_1 and C_2 as shown in Fig. 2(f), while both the integrated SB module switches are turned ON to charge the L_{in}. In this case, only two power switches of the D2T cell (S_5, and S_7) are ON, while the charging/discharging operation of both the involved capacitors depends on the direction of i_g at the unity/non-unity PF. Here, through the reverse grid current direction of non-unity PF condition, the internal anti-parallel power diode of S_5, and S_7 are reverse-biased, while they are in forward-biased when a unity PF is demanded.

Considering the above-mentioned circuit descriptions of the proposed topology, the following remarks can be stated:

1) The peak inverse voltage (PIV) of all the involved power switches is limited by the boosting feature of the proposed topology as:

$$V_{max,Si} = V_{C1} + V_{C2} = \frac{2V_{dc}}{1-d} \quad i = 1,5,6,7, and\ 8 \quad (7)$$

$$V_{max,S2} = V_{C1} = V_{C2} = \frac{V_{dc}}{1-d} \quad (8)$$

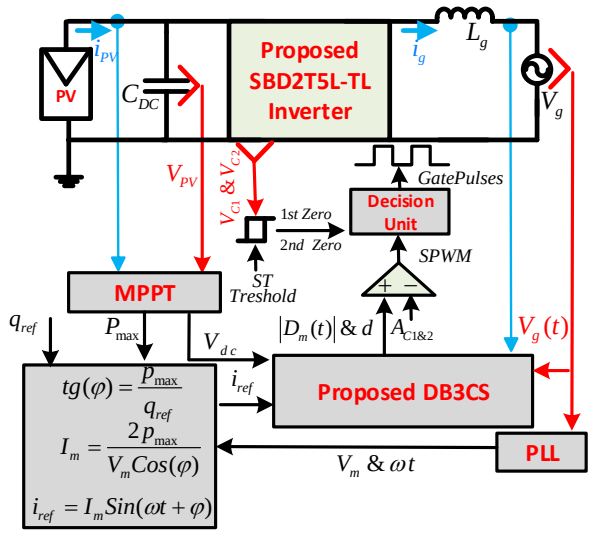

Fig. 3. The overall control block diagram of the proposed grid-connected SBD2T5L-TL inverter.

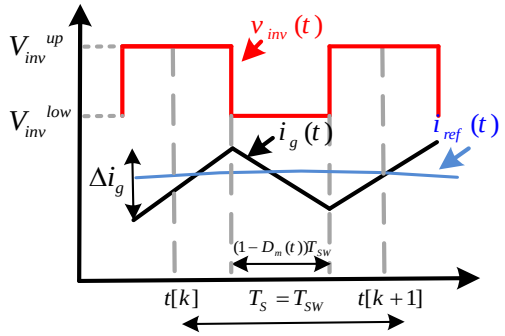

Fig. 4. The typical waveforms of the inverter output voltage and the reference/ injected grid current within a two cycles of the fixed switching frequency.

$$V_{max,S3} = V_{max,S4} = \pm V_{C1} = \pm V_{C2} = \pm\frac{V_{dc}}{1-d} \quad (9)$$

So, regarding (7)-(9), the per-unit scale of the total standing voltage (TSV) of the switches is 6.5.

2) Concerning the adjustable maximum voltage of the proposed SBD2T5L-TL inverter expressed in (6), and as for a standard local grid with the peak voltage of 311 V, only a 50 V input dc supply with $d = 0.75$ is needed to meet the minimum grid amplitude requirement. Here, similar to other boost-based converters, the duty cycle adjustment have to be in accordance with the stability standards. Following this remark, in case of having a higher range of input voltage provided by the PV-main strings panels, the aforementioned duty cycle can possess smaller values. So, the maximum value of the inverter output voltage and in consequence the PIV of all the involved switches can be maintained within a permissible range. The boundary condition of such a duty cycle changes hinges on the modulation/control process, which will be discussed in the next section.

3) The importance of L_{in} in the SB module is not only for giving a boosting property to the proposed topology within a single stage energy conversion platform, but also for the soft charging operation of the involved capacitors. So, as can be realized by the blue lines of the capacitors' charging loop in Fig. 2(a)-(e), instead of having an extremely high inrush current caused by the direct parallel connection of the capacitors to the dc supply [24], the maximum charging current of the capacitors is alleviated by the contribution of L_{in} .

III. Proposed DB3CS Principles

In grid-connected TL-inverter applications, the injected grid current waveform has to be fully controlled during the operation. Such a controlled grid current must track a pre-defined waveform of sinusoidal reference current ($i_{ref}(t)$) to properly ride through the active and reactive power injection. The overall modulation/control platform of the proposed SBD2T5L-TL inverter is on the basis of a new DB3CS principle as depicted in Fig. 3. Here, the capacitors voltage balancing issue is another aim. So, to sufficiently integrate both the redundant states provided by the zero-level of the output voltage, a Schmitt Triger (ST) block with a decision maker unit has also been used in the overall control diagram.

Herein, the maximum power point tracker (MPPT) unit with the phase-locked loop (PLL) block are needed to define $i_{ref}(t)$. In this case, any kinds of MPPT techniques like Perturb and Observe (P&O), Incremental Conductance (INC) or constant MPP voltage algorithm can also be used to extract the maximum power from the PV panel (P_{max}). Regarding this, the proposed DB3CS tries to predict the next behavior of the injected grid current based on a sampling/switching time (T_{sw}), which corresponds to the switching frequency of the involved power switches. Here, q_{ref}, $V_m$and ω, respectively, denote as the intended value of the reactive power, maximum value of the grid voltage, and the angular term of the grid frequency.

By predicting the next behavior of the injected grid current during the switching/sampling time, the proposed DB3CS approach can produce an optimal switching duty cycle signal ($D_m(t)$) to minimize the grid current prediction error. Such an optimal value of $D_m(t)$ is then transferred into the conventional sinusoidal pulse width modulation (SPWM) process to generate all the possible output voltage levels of the proposed SBD2T5L-TL inverter with a fixed value of the switching frequency.

To evaluate the detailed operation of the proposed DB3CS during a sampling/switching time interval, which is between the capturing instant time of k and (k+1), Fig. 4 can be considered. Since at each switching period, the output voltage of the inverter ($v_{inv}(t)$) is switched between two adjacent values; so, V_{inv}^{up} and V_{inv}^{low} can represent the upper and lower level of $v_{inv}(t)$ at each switching instant, respectively. Also Δi_g is the ripple current across the filter inductor (L_g) during the switching operation.

As the general relation between $v_{inv}(t)$ and the grid voltage ($v_g(t)$) that are connected with each other via L_g, the following dynamic expression can be written:

$$v_{inv}(t) = L_g\frac{di_g(t)}{dt} + v_g(t) \quad (10)$$

Here, the initial measured value of the injected grid current at the instant of k can be supposed to be $i_g(k)$, as can be found out by Fig. 4; so the next behavior of the injected grid current at the instant of (k+1) ($i_g(k+1)$) can be predicted as follows:

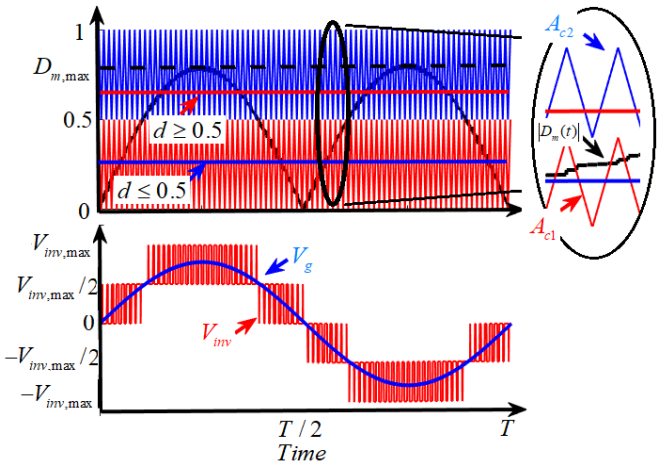

Fig. 5. Typical waveforms of the proposed controlled modulator with inverter's output voltage levels/grid voltage in SPWM process.

TABLE I
ON SWITCHING STATES OF THE PROPOSED SBD2T5L-TL INVERTER OPERATED WITH DB3CS/SPWM METHOD @ $d \leq 0.5$

$D_m(t)$ POLARITY	SPWM CONDITION	ON STATE SWITCHES	V_{inv}
POSITIVE	$\lvert D_m(t)\rvert \geq A_{C2}$& $d \geq A_{C1}$	S_1, S_2, S_6, S_8	$V_{C1}+V_{C2}$
	$\lvert D_m(t)\rvert \geq A_{C2}$& $d < A_{C1}$	S_1, S_3, S_6, S_8	
	$A_{C1} \leq \lvert D_m(t)\rvert < A_{C2}$& $d \geq A_{C1}$	S_1, S_2, S_4, S_8	V_{C1}
	$A_{C1} \leq \lvert D_m(t)\rvert < A_{C2}$& $d < A_{C1}$	S_1, S_3, S_4, S_8	
NEGATIVE	$\lvert D_m(t)\rvert \geq A_{C2}$&& $d \geq A_{C1}$	S_1, S_2, S_5, S_7	$-V_{C1}-V_{C2}$
	$A_{C1} \leq \lvert D_m(t)\rvert < A_{C2}$& $d \geq A_{C1}$	S_1, S_2, S_3, S_7	$-V_{C1}$
	$A_{C1} \leq \lvert D_m(t)\rvert < A_{C2}$& $d < A_{C1}$	S_2, S_3, S_5, S_7	
POSITIVE/ NEGATIVE	$\lvert D_m(t)\rvert < A_{C1}$& $d \geq A_{C1}$&$\Delta V_C \geq V_{ST}$	S_1, S_2, S_3, S_4	0
	$\lvert D_m(t)\rvert < A_{C1}$& $d \geq A_{C1}$&$\Delta V_C < V_{ST}$	S_1, S_2, S_7, S_8	
	$\lvert D_m(t)\rvert < A_{C1}$& $d < A_{C1}$&$\Delta V_C \geq V_{ST}$	S_2, S_3, S_4, S_5	
	$\lvert D_m(t)\rvert < A_{C1}$& $d < A_{C1}$&$\Delta V_C < V_{ST}$	S_1, S_3, S_7, S_8	

$$i_g(k+1) = i_g(k) + f_{inc}(t)D_m(t)T_{Sw} + f_{dec}(t)(1-D_m(t))T_{Sw} \quad (11)$$

where, $f_{inc}(t)$ and $f_{dec}(t)$, respectively, denoted as the positive (increasing) and negative (decreasing) slope of the $i_g(t)$ in each switching period.

Regarding (10), and Fig. 4, the $f_{inc}(t)$ and $f_{dec}(t)$ can be expressed as (12) and (13), respectively.

$$f_{inc}(t) = \frac{V_{inv}^{up} - v_g(t)}{L_g} \quad (12)$$

$$f_{dec}(t) = \frac{V_{inv}^{low} - v_g(t)}{L_g} \quad (13)$$

Having taken the fact that the ultimate aim of the proposed DB3CS method is to reach the zero steady state error between i_{ref} and $i_g(k+1)$. So we can write:

$$e = i_{ref}(t) - i_g(k+1) = 0 \quad (14)$$

Now, considering (11)-(14), the general controlled value of the $D_m(t)$ is obtained as:

$$D_m(t) = \frac{L_g(i_{ref}(t) - i_g(k)) + (v_g(t) - V_{inv}^{low})T_{Sw}}{(V_{inv}^{up} - V_{inv}^{low})T_{Sw}} \quad (15)$$

So, by neglecting the error term in (15), the function of $D_m(t)$ in the continuous time domain can be restated as:

$$D_m(t) = D_{m,max}Sin(\omega t) \quad (16)$$

where, $D_{m,max}$ is the maximum value of the optimal switching duty cycle and therefore with hindsight to the maximum output voltage of the proposed SBD2T5L-TL inverter mentioned in (6), it can be then expressed as:

$$D_{m,max} = \frac{V_m}{V_{inv,max}} = \frac{V_m(1-d)}{2V_{dc}} \quad (17)$$

Since $D_m(t)$ is always varied between -1 and 1; so to ride through the SPWM process, an absolute function of $D_m(t)$ is used and then it will be compared with two high frequency level-shifted triangular carrier waveforms ($A_{C1}$and A_{C2}). Here, to generate all the 5L of the output voltage with a fixed switching frequency operation, the amplitude of $A_{C1}$and A_{C2} is selected as (0 to 0.5) and (0.5 to 1), respectively. Also, the switching frequency of both the carrier waveforms have to be in accordance with the sampling/switching time used as for driving the $D_m(t)$.

The typical waveforms of such an SPWM process along with the 5L output voltage waveform of the proposed inverter over a grid frequency cycle (T) is illustrated in Fig. 5. Here, to select a proper value of d for the SB module switches, a boundary condition has to be found. Such a boundary condition depends on the minimum required value of the $V_{inv,max}$ expressed in (6) and the permissible minimum value of $D_{m,max}$ mentioned in (17). So, considering (6) whilst maintaining all the 5L waveform at the output voltage, the value of d must satisfy the following relation:

$$1 - \frac{2V_{dc}}{V_m} \leq d \leq 1 - \frac{V_{dc}}{2V_m} \quad (18)$$

From (18), it is revealed that the selected value of d depends on the input dc voltage available by the MPPT process and the peak voltage of the grid. Therefore, after selecting the proper value of d, it must be also compared with one of the level-shifted triangular carrier waveforms as depicted in Fig. 5. Regarding the working principle of the proposed SBD2T5L-TL and considering such a mentioned modulation/control process, the output voltage and ON switching states of the involved switches can be summarized as Table I. Here, it has been considered that the value of d is less than 0.5; so it can also be compared with A_{C1} during the SPWM process. Also, in order to select a proper zero-level of the output voltage among two existed redundant states, the voltage difference of the involved capacitors ($\Delta V_C = V_{C1} - V_{C2}$) must be measured and then it has to be compared with a threshold voltage (V_{ST}) of the employed ST unit. So, once $\Delta V_C$is to be less than V_{ST} , the first redundant state of the zero-level (See Fig. 2. (a)) is chosen to keep on charging operation of C_1, and in turn whenever ΔV_C is to be greater than V_{ST}, the second redundant state of the zero- level (See Fig. 2 (b)) is selected to maintain the voltage of C_2 in a permissible balanced range.

IV. DESIGN GUIDELINES

The input and filter inductors along with two involved capacitors are the passive elements of the proposed SBD2T5L-TL inverter. In this section, the design guidelines of such mentioned passive elements is discussed.

A. Inductors Design

In order to find out a proper value for both the input and filter side's inductors, their passing current waveform function (the

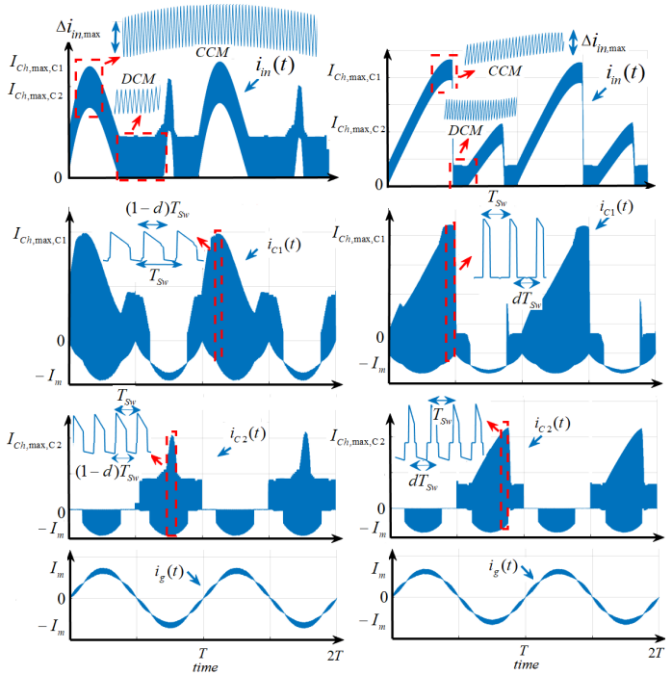

Fig. 6. The typical waveforms of the input current, capacitors currents, and the injected grid current with 10 kHz switching frequency (a) at $d \leq 0.5$ (b) at $d > 0.5$.

input current and the injected grid current) has to be derived as follows [24]-[25]:

$$i_{in}(t) = \frac{1}{L_{in}} \int_0^{dT_{Sw}} v_{Lin}(\tau) d\tau + i_{in}(0) \quad (19)$$

$$i_g(t) = \frac{1}{L_g} \int_0^{D_m(t)T_{Sw}} v_{Lg}(\tau) d\tau + i_g(0) \quad (20)$$

where, $i_{in}(0)$ and $i_g(0)$ are respectively denoted as the initial stored input, and grid current. Also, $v_{Lg}(t)$ is the voltage across the filter's inductor. So, considering the proposed control principles and the relation of (1) and (12), the required value of the input and filter's inductors can be obtained as (21) and (22), respectively:

$$L_{in} \geq \frac{V_{dc}\, d}{f_{sw} \Delta I_{in,max}} \quad (21)$$

$$L_g \geq \frac{(V_{inv,max} - V_m) D_{m,max}}{f_{sw} \Delta i_{g,max}} \quad (22)$$

where, $f_{sw}$is the switching frequency. Here, $\Delta i_{in,max}$ and $\Delta i_{g,max}$ are the maximum allowable high frequency ripple values of the input and grid currents, respectively.

B. Capacitance Determination

To determine a suitable value for the capacitance of the D2T cell capacitors, their maximum discharging time interval and the voltage difference across them (ΔV_{C1}&ΔV_{C2}) must be taken into account. Considering the longest discharging time interval of the capacitors as (α, β), the following equation can be expressed:

$$\frac{1}{C_i} \int_\alpha^\beta i_{Ci}(t) = \Delta V_{Ci} \quad i = 1, and\ 2 \quad (23)$$

where, $i_{Ci}(t)$ is the passing current through the capacitors. Considering the average value of the output power injecting to the grid (P_{Out}) and regarding (23), $i_{Ci}(t)$ can be directly relevant to the i_g through finding the discharging duty cycles of the capacitors [24], so the required capacitance of the involved capacitors can be determined as follows:

$$C_1 = \frac{P_{Out}}{V_{C1} \Delta V_{C1}} \left(\frac{2T}{3} + \frac{T}{D_{m,max}\pi} \sqrt{1 - \frac{1}{4D_{m,max}^2}} \right) \quad (24)$$

$$C_2 = \frac{P_{Out}}{V_{C2} \Delta V_{C2}} \left(\frac{2T}{3} + \frac{0.5T}{D_{m,max}\pi} \sqrt{1 - \frac{1}{4D_{m,max}^2}} \right) \quad (25)$$

Regarding (24) and (25), it is apparent that C_1 must possess higher capacitance than C_2 since it has a longer discharging cycle during the negative half cycle output voltage levels generation.

V. Input Current and Current Stress Analysis

Owing to use of SB module modulating the basis of d, the proposed SBD2T5L-TL inverter exhibits different performance from the input current and current stress viewpoints. In this section, some analysis as for addressing these are presented.

A. Input Current Analysis

In order to develop the current stress analysis of different devices in the proposed topology, the characteristic of the input current waveform is of interest. Fig. 6 (a) and (b) show the typical waveforms of the input current ($i_{in}(t)$), the passing current through the involved capacitors ($i_{C1}(t)$ and $i_{C2}(t)$) and the injected grid current ($i_g(t)$) for two cases of $d \leq 0.5$ and $d > 0.5$, respectively. Herein, the switching frequency of the described DB3CS scheme is supposed to be 10 kHz and the value of $L_{in}$is selected as the same for both the cases.

As can be observed, the nature of $i_{in}(t)$ for both the aforementioned cases is based on the integration of the Continuous Control Mode (CCM) and Discontinuous Control Mode (DCM) operation over a fundamental grid frequency. It can also be seen that the sequence of such operating Mode integration in both the cases of $d \leq 0.5$ and $d > 0.5$ is on the basis of CCM-DCM-CCM-DCM operation within an entire grid fundamental cycle. Hence, once the capacitors are charged via the input dc source and L_{in}, the CCM operation appears, while whenever none of the capacitors is getting charged, $i_{in}(t)$ possesses an DCM operation. Regarding Fig. 6 (a) and (b), it can be deduced that once the value of d is greater than 0.5 (in case of demanding higher boosting feature by the proposed SBD2C5L-TL inverter), the total duration time of the CCM and DCM operations for $i_{in}(t)$ is about 80% and 20% of a grid fundamental cycle, respectively.

By contrast, once the value of d is set on a value that is less than 0.5 (in case of demanding lower boosting feature by the proposed SBD2C5L-TL inverter), the accumulated duration of CCM and DCM operations for $i_{in}(t)$ is about 60% and 40% per each grid fundamental cycle, respectively. Such a longer duration of the DCM operation in $i_{in}(t)$ imposes higher ripple content in both the input and the injected grid current waveforms and can affect the overall efficiency of the entire system, as well.

B. Capacitors and Semiconductor Current Stress

To discuss the highest charging current demanded by the involved capacitors ($I_{Ch,max,C1}$and $I_{Ch,max,C2}$), their longest charging loop operations have to be addressed. Such a highest values of the capacitors charging currents exhibits the maximum current stress value of the involved semiconductors.

Considering the blue lines of Fig. 2 (c) and (d) and also Fig. 2 (b) and (e), it can be discerned that the longest charging interval of C_1 is between the switching cycles of the first positive and top positive output voltage levels, while as for C_2, this longest charging interval is between the zero negative and the first negative output voltage levels. So, in case of unity PF condition (the worst condition for current stress analysis), the following relation can be expressed:

$$i_{Ch,Ci}(t) = i_{in}(t) - i_g(t) \quad i = 1, and\ 2 \tag{26}$$

where, $i_{Ch,Ci}(t)$ represents the charging current of the capacitors. Regarding the working principles of the SB module incorporated into the proposed topology, $i_{in}(t)$ can be relevant to $i_g(t)$ through the following equation:

$$i_{in}(t) = \frac{2i_g(t)}{1-d} \tag{27}$$

Therefore, in respect to (26) and (27), we can write:

$$i_{Ch,Ci}(t) = \frac{1+d}{1-d} \times i_g(t) \quad i = 1, and\ 2 \tag{28}$$

On the other hand, regarding the proposed DB3CS strategy, $i_g(t)$ can be relevant to the extracted general controlled value of $D_m(t)$ as follows:

$$i_g(t) = I_m D_m(t) \tag{29}$$

where, I_m is the peak of injected grid current. Therefore, considering (16), (26)-(29), the current stress profile of both the involved capacitors during their longest charging operation time interval can be obtained as follows:

$$\begin{cases} i_{C1}(t) = I_m D_{m,max} Sin(\omega t) \times \frac{2}{1-d} & \frac{T}{4} \le \omega t \le \frac{3T}{4} \\ i_{C2}(t) = I_m D_{m,max} Sin(\omega t) \times \frac{2}{1-d} & 0 \le \omega t \le \frac{T}{4} \end{cases} \tag{30}$$

Regarding (30), the maximum current stress value of the involved capacitors can also be obtained as:

$$\begin{cases} I_{Ch,max,C1} = I_m D_{m,max} \times \frac{2}{1-d} \\ I_{Ch,max,C2} = I_m D_{m,max} \times \frac{1}{1-d} \end{cases} \tag{31}$$

From (31), it can be revealed that the maximum current stress profile of both the involved capacitors for $d > 0.5$ is slightly higher than their counterpart for $d \le 0.5$.

Regarding the abovementioned discussion and considering the current flowing path analysis conducted in Section II, the maximum current stress profile of all the involved power switches can be summarized as follows:

$$\begin{cases} i_{S1} = i_{S2} = i_{S3} = i_{S8} = I_{Ch,max,C1} \\ i_{S5} = I_{Ch,max,C2} \\ i_{S4} = i_{S6} = i_{S7} = I_m \end{cases} \tag{32}$$

Concerning (31), and (32) and regarding the calculated maximum PIV of the involved semiconductors in (7), the maximum Volt-Ampere (VA_{max}) rating of the proposed SBD2C5L-TL inverter semiconductors can be attained as follows:

$$VA_{max} = V_{dc} I_m D_{m,max} \times \frac{4}{(1-d)^2} \tag{33}$$

Taking (33) into the design consideration, the scalability of the proposed topology in reaching higher value of the output power can be deduced.

VI. Comparative Study

In order to evaluate the superiority of the proposed CG-based SBD2T5L-TL inverter over its other TL-inverter counterparts, a comparative study from different aspects is presented in this section. The comparative items are the number of active and passive involved components (with considering the pre-assumed output filter, and the input decoupling capacitor for PV applications), maximum number of ON state power switches at each switching instant, which can somehow represent the conduction losses of the switches, the ability as for boosting feature with minimum required value of the input dc voltage utilization for a standard grid-connected application, maximum number of the inverter output voltage levels, the capacitors soft charging operation capability, the reported value of the leakage current, the reactive power support ability, and the reported measured efficiency at the rated power. Here, the value of the leakage current is considered low and very low if it is less than 120 mA and 10 mA, respectively [20],[25]. The overall results of such a comparative study is summarized in Table II. As can be seen, the proposed topology, the Variant 5LH8-TL inverter presented in [9], the ANPC and ABNPC structures of [10] and [13], the CG-FC- based topologies of [20] and [21], and the CG-SC-based TL-inverters of [24] and [25] are only able to generate 5L of the output voltage levels. However, the main difference of such a mentioned 5L-TL inverter structures is the minimum dc input voltage utilization to meet the amplitude of a standard grid (with 311 V as the peak) requirement. In light of this, only a 50 V input dc source is enough to make the eight-time voltage boosting feature as for the proposed structure. Herein, none of the topologies mentioned in [9], [10] and [13] possesses the CG feature; so, still the concern of leakage current elimination is left. By contrast, although the number of switching devices of the proposed SBD2T5L-TL inverter is slightly higher than other 5L-CG-based TL-inverter counterparts, it has a valuable dynamic voltage boosting feature with an inherent soft charging nature of the involved capacitors.

As described earlier, such a soft charging operation of the capacitors helps the input current waveform to exhibit an CCM operation for a significant portion of the grid fundamental cycle. In contrast, other 5L-CG-based structures suffer from DCM characteristic of the input current waveform throughout the charging operation of the capacitors within a full cycle of the grid frequency, which results in higher conduction losses.

So, it can readily be seen that the proposed topology is applicable in higher nominal range of output power with a reasonable value of the input inrush current and a compatible value of the overall efficiency over the others. Moreover, other 5L-CG-based TL-inverters have used additional power diodes rather than the power switches as can be realized by Table II, while there is not any incorporated power diode in the proposed topology. Herein, although two bi-directional power switches have been incorporated in the proposed SBD2C5L-TL inverter, only one of them (the power switch S_3) experience the highest current stress as mentioned in (32), while such a current stress is in accordance with a permissible range of input current waveform.

Table II. A Comparative Summary Between the Proposed Topology and Different TL-Grid-Connected Inverter Structures.

Type of Converter		No. of Components				Max No. of ON-Switches	Minimum Required V_{in}/ Boosting Feature	No. of Levels	Leakage Current	Reactive Power Support	Soft Charging Capability	Reported Rated Efficiency
		S	D	C	L							
H5 [4]		5	-	2	2	3	320 V/NO	3	Low	Yes	Not Needed	98.5%@0.5kW
OH5 [5]		6	-	2	2	3	320 V/NO	3	Low	Yes	Not Needed	97.2@1kW
HERIC [6]		6	2	2	2	2	320 V/NO	3	Low	NO	Not Needed	97% @1kW
H6 [7-8]		6	2	2	2	3	320 V/NO	3	Low	Yes	Not Needed	97.4%@1kW
Variant 5LH8 [9]		8	8	1	3	1	320 V/NO	5	Very Low	Yes	NO	96.8%@500W
ANPC [10]		6	2	2	1	2	640 V/NO	5	Very Low	Yes	NO	NA@1kW
ABNPC[13]		6	2	3	1	2	320 V/Yes	5	Very Low	Yes	NO	97.8%@1.2kW
ANPC [14]		4	2	4	1	2	225 V/Yes	4	Very Low	Yes	NO	NA@1kW
CGType [18]	Type I&II	6	1	3	1	2	320 V/NO	3	Zero	Yes	NO	99.1%@800W
	Type III	6	-	3	1	2	320 V/NO	3	Zero	Yes	NO	96%@800W
CG-Type [19]		4	2	4	2	2	320 V/NO	3	Zero	Yes	NO	95.2%@500W
CG-FC-based [20]		6	-	3	1	3	320 V/NO	5	Zero	Yes	NO	97%@1kW
CG-FC-based [21]		6	1	3	1	3	320 V/NO	5	Zero	Yes	NO	95.8%@1.2kW
CG-SC-based [22]		7	1	3	1	3	160 V/Yes	3	Zero	Yes	NO	98.1%@500W
CG-SC-based [23]		6	2	3	1	3	160 V/Yes	3	Zero	Yes	NO	98.1%@500W
CG-SC-based [24-25]		7&6	1&2	3	1	3	160 V/Yes	5	Zero	Yes	NO	98.1%@600W
Proposed SBD2T5L		10	0	3	2	4	50 V/Yes	5	Zero	Yes	Yes	98.2%@1kW

Table III. Parameters used for Analysis and Measurements

Element	Type	Description
Power Switches	SCT3022AL	650 V/93 A
Gate Drivers ICs	ACPL-P343	IC Chip
Power Diodes	C5D50065D	650 V/100 A
Current/Voltage Transducer	LA55P	USM3IV
Microcontroller	FPGA-LABVIEW	RIO9607
Local Grid's Peak Voltage/ Grid Frequency	311 V/50 Hz	-
Switching Frequency	20 kHz	-
$C_1$and C_2	193 PUR-SI	$0.94mF$ & $0.47mF$
Filter's Inductor (L_g)	Ferrite Core	$2.3\ mH$
Input Inductor (L_{in})	Ferrite Core	$100\mu H$

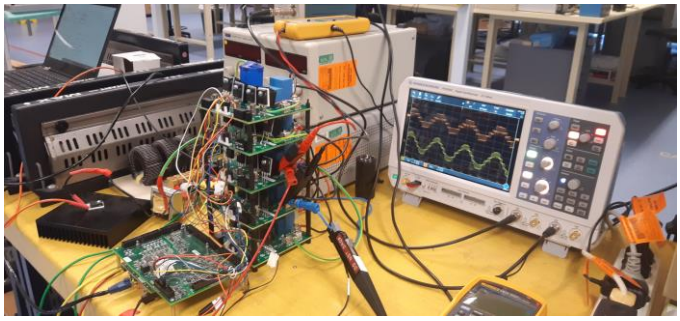

Fig. 7. Experimental setup of the proposed SBD2T5L-TL inverter.

It is also notable that all the positive and negative output voltage levels of the proposed topology are made by the dc-link capacitors as discussed earlier, while other 5L-CG-SC-based-TL inverters are using the aim of both the input dc source and the virtual dc-link voltage of the capacitors. Regarding this remark and as opposed to them, the dc-bias injection concern can be properly mitigated by the aim of the proposed topology.

VII. Verification Results and Discussion

The correctness and feasibility of the proposed SBD2T5L-grid-interfaced TL-inverter with its associated DB3CS method are verified by some simulation and laboratory measurement results in this section. The simulations results are performed by the use of both the MATLAB/SIMULINK and PLECS software, while the components used in all the measurement process have been compiled in Table III. Fig. 7 shows the hardware prototype fabricated based on five SiC CREE-based modules. Here, the passive elements have been chosen based on the presented design guidelines principles of Section IV. Moreover, the value of d is selected based on the described boundary condition of (18). Also, three feedbacks from $i_g(t)$, $v_g(t)$, and V_{dc} are required to make $D_m(t)$ of the proposed DB3CS according to (15). Regarding the boosting property of the proposed SBD2T5L-TL inverter and considering (6), $V_{inv,max}$ can be remained fixed by changing the instant value of d. This approach can address the MPPT operation of the input PV main string panels with a constant MPP voltage, where the maximum input power of the PV emulator can be remained fixed through the power balanced theory by adjusting the appropriate value of the SB module duty cycle.

Therefore, based on the maximum input voltage and input current capacity of the PV emulator, a fixed value of 400 V is selected for $V_{inv,max}$ in throughout the measurement process. Here, a 10% allowable ripple voltage has been considered for the balanced voltage of the dc-link capacitors; so regarding, the fixed value of $V_{inv,max}$ at 400 V, a value of 220 V has been chosen for V_{ST}. Since the investigation of the MPPT process is beyond the scope of this paper, an adjustable input dc source as the PV emulator has also been used.

Considering such observations, a step change in the value of the input voltage (from 50 V to 100 V in both directions) is applied, while the peak of the reference current is considered to be 5 A. So, to keep fixed $V_{inv,max}$ at 400 V, the value of d has to be dynamically changed from 0.75 to 0.5 in both the upward and downward directions. Fig. 8 (a)-(d) shows the detailed simulation results of this dynamic test, while all the 5L inverter output voltage could be generated with a 5 A peak value of the injected current to the grid. The balanced voltage of both the involved capacitors can also be seen in Fig. 8 (c), while the currents through the input dc source and the involved capacitors are shown in Fig. 8 (d). It can be confirmed that owing to the

employed SB module, the input current possesses a limited range of inrush current during the charging operation of the involved capacitors. Here, when the input voltage is 50 V ($d = 0.75$), the maximum value of the input current, which corresponds to the maximum charging current of $C_1$is around 30 A, while the maximum value of the injected grid current is 5 A. By contrast, once the input voltage goes up to 100 V ($d = 0.5$), the maximum value of the input current is around 10 A, while because of the applied power balanced theory, the peak of injected grid current is around 3.5 A. As can be seen the results are compatible with the theory presented in Section V. The current stress profiles of all the involved power switches have also been shown in Fig. 9 (a)-(d). As can be observed and according to (32), the maximum current stresses in case of $d = 0.75$ is higher than its counterpart in the case of $d = 0.5$, while only five power switches as S_1, S_2, S_3, S_5, and S_8 are tolerating this maximum value. The start-up operation of the proposed SBD2T5L-TL inverter has also been depicted in Fig. 10, while the input dc source has been fixed at 100 V and the inverter is feeding a 5 A load. As discussed in [21], a relay associated with a small paralleled resistance has been used to cope up with the start-up charging process of the involved capacitors. As can be seen, the capacitors could reach their desired balanced voltage value (200 V with $d = 0.5$) within less than two fundamental grid cycles. Herein, as for the safety procedure, the incorporated relay is bypassed after reaching the stable voltage point of the involved capacitors. So, the proposed SBD2T5L-TL inverter can be then connected to the local grid for riding through its normal loaded operation. Following this, the measured 5L output voltage of the inverter, the injected grid current and the 200 V balanced voltage of the involved capacitors are shown in Fig. 11 (a), while $i_{ref}(t)$ possesses a unity PF condition with a peak of 6 A and the input dc source is fixed at 100 V.

Fig. 11 (b) also shows the same experimental result with the presence of the grid voltage waveform at 5 A peak value of the injected grid current. As can be seen the results have a good agreement with the simulation. The reactive power support capability of the proposed TL grid-tied inverter with a peak injected grid current of 10 A and $V_{dc} = 100\,V$ can also be observed in Fig. 11 (c) and (d). As is clear all the expected output voltage levels could be properly generated without any dc bias/offset deviation, while the injected grid current can follow $i_{ref}(t)$ with a leading and lagging PF.

In order to further confirm the dynamic performance of the proposed system, the input voltage value is again kept fixed at 100 V, while a upward and downward step change (from 5 A to10 A in both directions) in the peak value of $i_{ref}(t)$at the unity PF are applied. Fig. 12 (a) and (b) can readily verify the appropriate dynamic performance of the proposed system in generating all the supposed output voltage levels and injecting the active power to the grid. Here the injected grid current THD is almost 2.2 %. Contemporary, as for the next dynamic test, the peak of $i_{ref}(t)$is kept fixed at 5 A, whereas the value of the input voltage is changed from 50 V to 120 V and from 120 V to 50 V. The related input dc voltage, the 5L inverter's output voltage, the injected grid current and the grid voltage waveforms with a robust dynamic performance in both the cases can be observed in Fig. 12 (c) and (d).

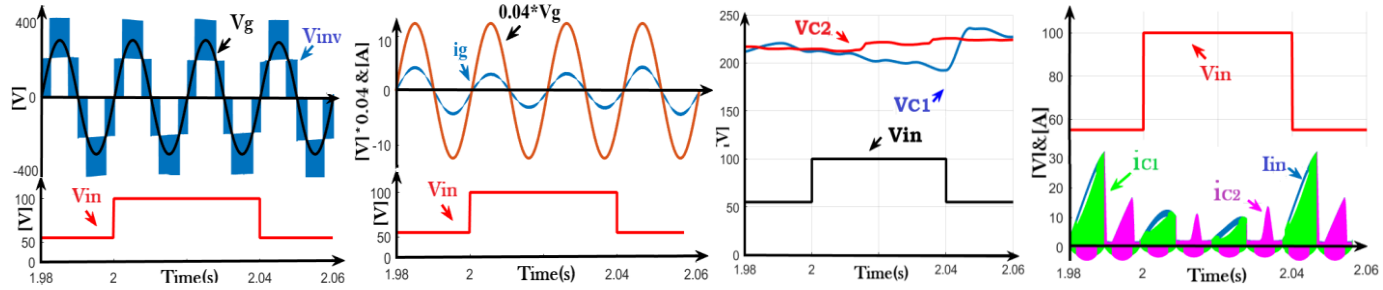

Fig. 8. Simulation results once a upward and downward step change (from 50 V to 100 V and vice versa) is applied in the input voltage: (a) 5L inverter's output voltage with the grid/input voltage (b) the injected grid current with the grid voltage and the input voltage (c) the voltage across C_1 and C_2 with the input voltage, and (d) the input current along with the capacitors passing current and the input voltage.

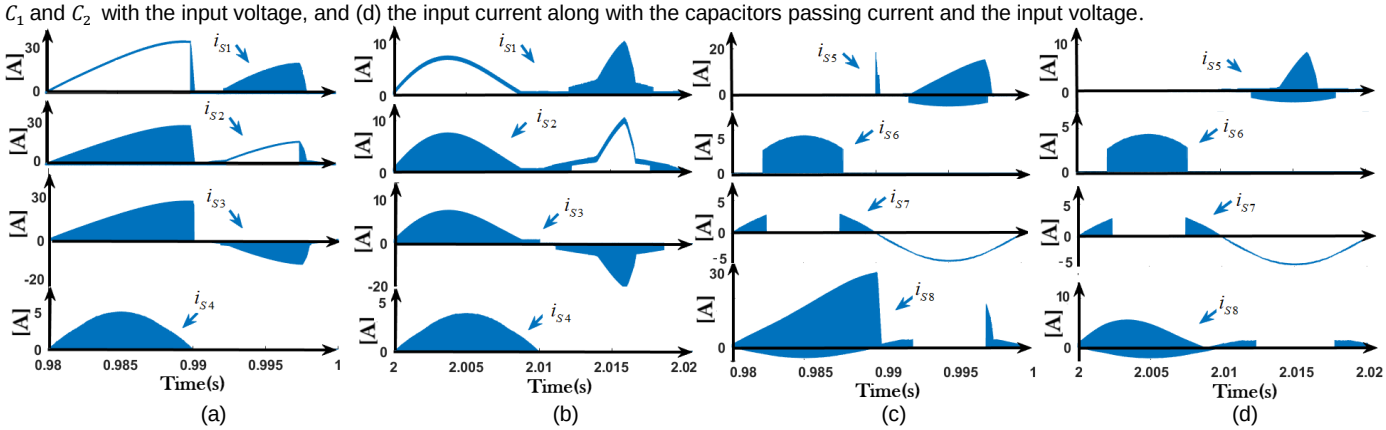

Fig. 9. Simulation results showing current stress waveforms of switches (a) S_1, S_2, S_3, S_4 at $V_{in} = 50\,V$ ($d = 0.75$) (b) S_1, S_2, S_3, S_4 at $V_{in} = 120\,V$ ($d = 0.4$) (c) S_5, S_6, S_7, S_8 at $V_{in} = 50\,V$ ($d = 0.75$) (d) S_5, S_6, S_7, S_8 at $V_{in} = 120\,V$ ($d = 0.4$).

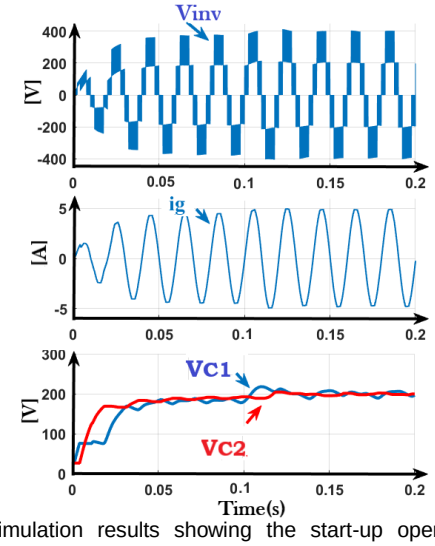

Fig. 10. Simulation results showing the start-up operation of the proposed SBD2T5L-TL inverter.

Herein to further attest such a dynamic change in the value of d, the voltage across L_{in} alongwith the 5L output voltage of the inverter with the injected grid current and the grid voltage waveforms have been also shown in Fig. 13 (a) and (b). As is clear, to keep fixed the peak of the output voltage of the inverter at 400 V, the value of d is dynamically changed between 0.75 and 0.4 in respect to the input voltage changes, while the injected grid current is quite robust and stable during the dynamic test. In this case, because of the power balanced theory and the supposed MPPT procedure with constant MPP voltage, the peak of injected grid current waveform is affected by the changes in the input voltage value. The measured PIV waveforms across all the involved power switches can also be seen in Fig. 14 (a)-(c), where the obtained results are quite accorded with the theory presented in (7)-(9). Since the peak of the proposed SBD2C5L-TL inverter has been fixed at 400 V, so the PIV of the switches are the same in both the cases of $d \leq 0.5$ and $d > 0.5$.

Finally, in respect to Table IV and using the PLECS, a thermal analysis for all the involved power switches is conducted. Here, a constant ambient temperature of 40^0 C with a uniform temperature distribution across the heat sink has been considered. Fig. 15 (a) and (b) respectively show such a junction temperature performance of the involved switches at 1 kW active power injection to the grid and when two different values of d ($d \leq 0.5$ and $d > 0.5$) are used.

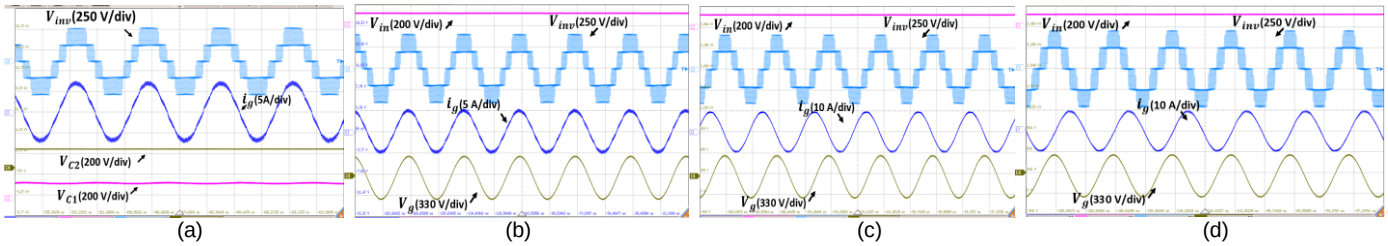

Fig. 11. Measured waveforms of the voltage across capacitors, the input voltage, 5L inverter's output voltage, the grid voltage, and the injected grid current @ $V_{in} = 100\ V$: (a) and (b) at unity PF condition (c) at leading PF, and (d) at lagging PF.

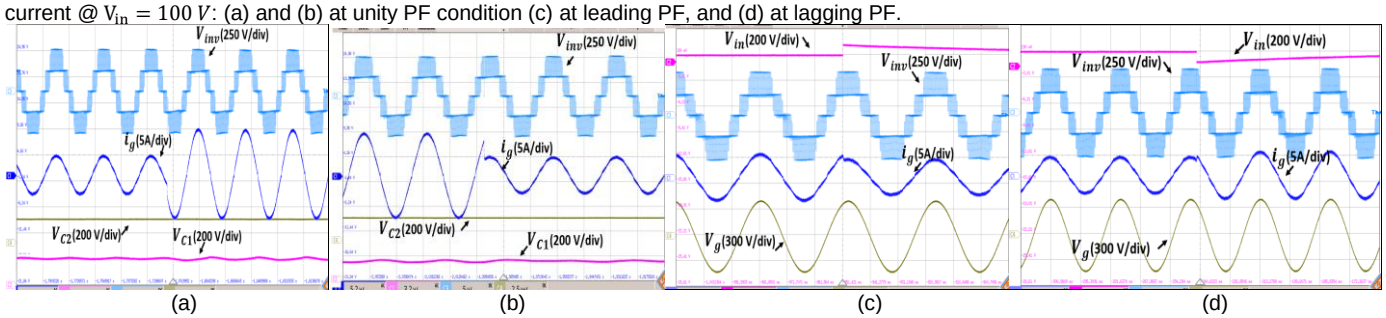

Fig. 12. Measured waveforms showing the dynamic operation (a) at unity PF and once the amplitude of the reference current is changed from 5 A to 10 A. , (b) at unity PF and once the amplitude of the reference current is changed from 10 A to 5 A (c) once the input voltage is changed from 50 V to 120 V, and (d) once the input voltage is changed from 120 V to 50 V.

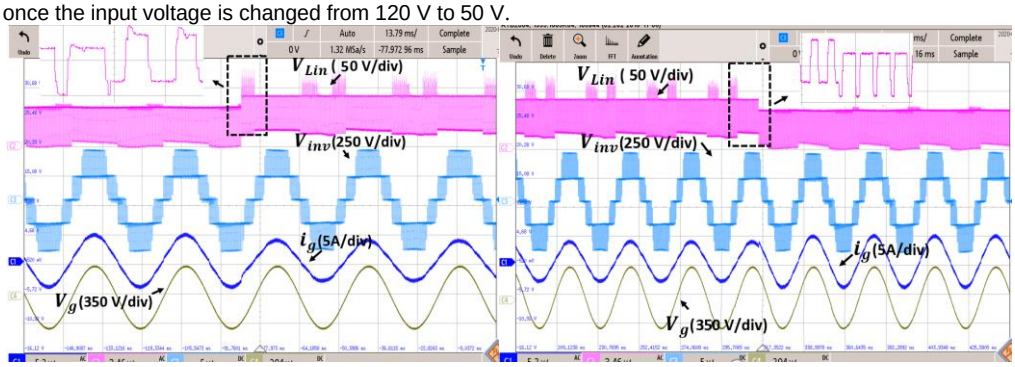

Fig. 13. The measured waveforms (a) once a upward step change in the value of the input voltage (from 50 V to 120 V) is applied (b) once a downward step change in the value of the input voltage (from 120 V to 50 V) is applied.

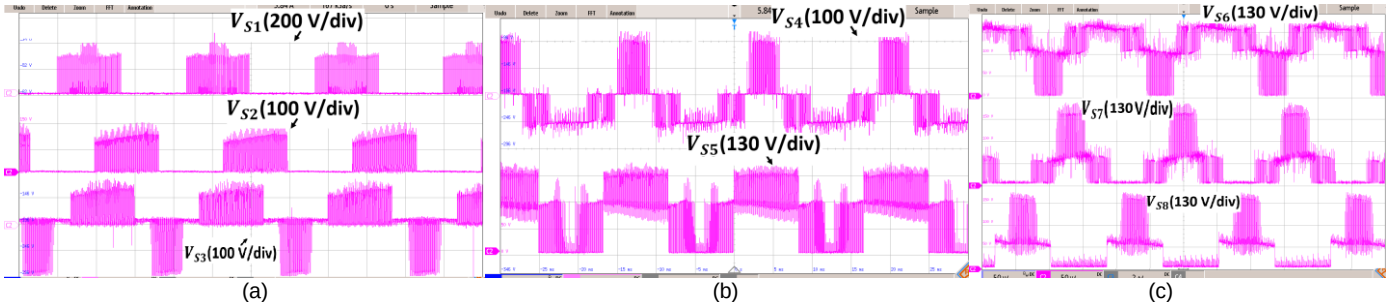

Fig. 14. Measured waveforms showing the voltage stress across (a) S_1, S_2, S_3, (b) S_4 and S_5, and (c) S_6, S_7, S_8.

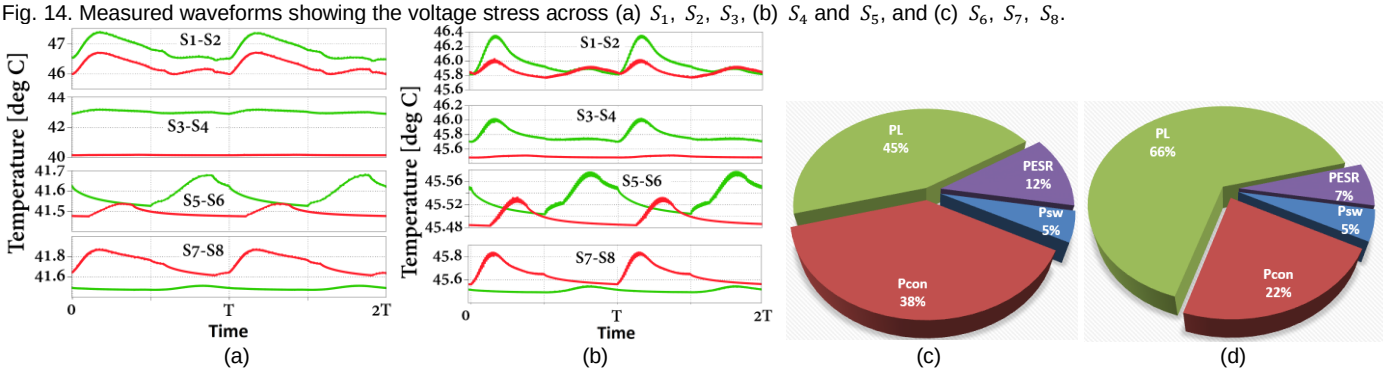

Fig. 15. Thermal and loss analysis extracted by the PLECS showing (a) junction temperature of the switches for the case of $d > 0.5$ (b) junction temperature of the switches for the case of $d \leq 0.5$,(c) loss distribution (%) for the case of $d > 0.5$, and (d) loss distribution (%) for the case of $d \leq 0.5$

From these results, it can be seen that owing to different characteristic of the input and capacitors charging currents during the CCM and DCM operations as discussed in Section V, the average junction temperature of the switches in case of $d > 0.5$ is lower than its counterpart in case of $d \leq 0.5$. Herein, the sudden jump in junction temperature of the switches can be attributed to the nature of current stress profile of each power switch. So, once the switches are in charging path of capacitive loop, their temperature increases suddenly since they should tolerate higher current stresses. Following this, the details of loss breakdown results extracted by the PLECS software at 1 kW injected power have been demonstrated in Fig. 15 (c) and (d). Herein, the total power losses of the proposed inverter include the switching loss (P_{Sw}), conduction loss of the switches (P_{Con}), inductors losses (P_L) and the equivalent series resistance (ESR) losses of the involved capacitors (P_{ESR}). Regarding the PLECS, total power losses is around 18 W and 25 W for the case of $d = 0.75$ and $d = 0.5$, respectively. As can be seen here, the major portion of the total power losses belongs to the involved inductors in both the cases of $d > 0.5$ and $d \leq 0.5$. Also, regarding the current stress analysis conducted in Section V, the conduction losses of the proposed inverter in case of $d > 0.5$ is higher than its counterpart for the cases of $d \leq 0.5$ (around 7 W for $d = 0.75$ in contrast to 5.5 W for $d = 0.5$ both at 1 kW injected active power). However, because of longer DCM operation of the input current, the inductors losses in cases of $d \leq 0.5$ is more weighted than the case of $d > 0.5$. e. g. 8.1 W in case of $d = 0.75$ in compare to 16.5 W in case of $d = 0.5$ at 1 kW injected active power. Regarding these observations, the calculated overall efficiency of the proposed SBD2T5L-TL inverter aimed by the PLECS at the above-mentioned rated power is around 98.2% and 97.5%

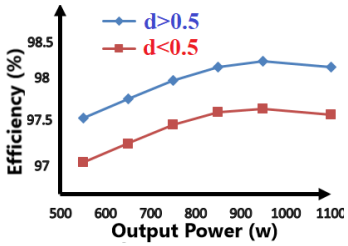

Fig. 16. Efficiency curve of the proposed SBD2T5L-TL inverter versus the output power.

for the case of $d = 0.75$ and $d = 0.5$, respectively. Details of such an overall efficiency curve versus a wide range of the injected output power can also be seen in Fig. 16, which can confirm better performance of the proposed system in case of $d > 0.5$ in contrast to $d \leq 0.5$.

VIII. Conclusion

A novel grid-interfaced SBD2T5L-TL inverter has been presented in this study. The proposed topology offers three valuable features as: 1) CG connection between the null of the grid and the negative terminal of the input voltage 2) Voltage boosting and adjustable maximum inverter output voltage capability within a wide range of input voltage changes, and 3) The inherent soft charging capability of the dc-link capacitors. These made it a suitable candidate for the PV grid-interfaced applications. To control the injected grid current waveform, a DB3CS method with the contribution of conventional level-shifted SPWM technique has also been introduced. The design guidelines of the passive elements were also developed through the definition of such a closed-loop control system. Current stress analysis of the proposed topology has been also addressed in following. Finally, a comprehensive comparative summary with the relevant simulation and experimental results have been presented to confirm the superiority and effectiveness of the proposed structure and control system.

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