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Published in:
I E E E Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2020.3007959

Publication date:
2021

Document Version
Accepted author manuscript, peer reviewed version

Three-Port High Step-Up and High Step-Down DC-DC Converter with Zero Input Current Ripple

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***Abstract*—In this paper, a non-isolated three-port DC-DC converter with high voltage conversion ratio is proposed. In the proposed converter, by changing the place of input voltage source between each of the three ports, three different single-input two-output operation modes are achieved. The input current ripple of the proposed converter is eliminated at the low voltage side for the whole range of duty cycles. The voltage conversion ratios of the proposed converter can be increased by increasing the turns ratio of second winding of coupled inductors. Moreover, the proposed converter has achieved proper output voltage regulations for all output ports, simultaneously. The proposed converter can be utilized in the renewable energy conversion systems such as in photovoltaic and fuel cells. In this study, the voltage conversion ratios of the output ports, the voltage stress on switches, the average currents of switches and inductors and the required condition for cancelling input current ripple at low voltage side are calculated theoretically. The theoretical results are verified and experimental results for 24 V input voltage and 304 V, 240 V output voltages with 400 W power are extracted for two different operation modes.**

***Index Terms*— Three-port converter, dc-dc single-input/two-output converter, high voltage gain, input current ripple cancellation, coupled-inductor based converter.**

I. INTRODUCTION

Nowadays, due to the wide use of different renewable energy sources such as photovoltaic (PV), fuel cell (FC), etc. and applying them as hybrid renewable energy sources, the multi-port DC-DC converters, have obtained more attention and play a significant role in interfacing the generated powers [1]-[4]. Generally, the applications of renewable energy sources can be divided into two main groups: off-grid or grid-connected systems. Multi-port DC-DC converters have the capability of interfacing different DC voltage levels and transfer high volume of power to the output loads, where this feature is more interesting in the renewable energy systems. For instance, in the off-grid solar home systems, multi-output converter can supply the different loads of homes with different levels of DC voltages [5]-[6]. In the case of grid-connected renewable energy sources, the different output DC voltage levels of multi-output converter are connected to DC-AC inverters, then the output ports with AC 220 V or 400 V with a frequency of 50-60 Hz are achieved and they can be delivered to the output loads [7]-[8]. As a result, increasing the voltage gain by using the minimum number of circuit elements would be preferred for the DC-DC converters. Utilizing coupled inductors in DC converters is an effective approach to increase the conversion ratio of the converter with a low number of components. In the coupled inductor-based converters, by increasing the turns ratio of the secondary winding of the coupled inductors, the voltage conversion ratios would be increased [9]-[10]. Moreover, the DC-DC converters with low or zero input current ripple would be preferred for use in the PV or FC and generally renewable energy sources [11].

The interleaved converters have the capability of reducing the input current ripple [12]-[13]. However, for example, in the interleaved two-phase converters have complicated control systems for output voltage regulation. Consequently, in the case of multi-port converters, there should be separate controllability for each of the ports and the converter should provide a constant voltage conversion ratio for the whole range of duty cycles to ease the control of the ports at the same time. On the other hand, in some cases, by using coupled inductors, the input current ripple is decreased or eliminated thoroughly [14]-[15]. The main constraint of the converters in [14] and [15] is their complicated control abilities. There are multiport DC-DC converters with three terminals and simple structures presented in [16]-[18]. The presented multiport DC-DC converters in [16] and [17] have low input current ripples in their low voltage sides, but the presented converter in [18] has higher input current ripple in its boost operation. In [19]-[23] single-input, two-output DC-DC converters are presented, which have two stepped-up voltages at their output ports. The converter in [19] has low input current ripple, but the converters in [20]-[23] have high input current ripples. However, the disadvantage of the converters in [19] –[22] is the low voltage gain which is near to the conventional DC-DC boost converter in each output port. The proposed converter in [23] is able to achieve higher voltage gains through the coupled inductor in its topology. The presented three-port DC-DC converter in [24] has low voltage gain and the converter suffers from pulsating input current. Three-port DC-DC converters with a battery as a storage in one port is presented in [25]-[29]. In [26]-[28], three-port DC-DC converters based on coupled inductors are presented. The conversion ratios of these converters are high and can be even more increased by increasing the turn ratio of the secondary winding of the utilized coupled inductors. In [29], a transformer-based three-port DC converter is presented. This converter suffers from high voltage stress on its semiconductor elements.

In this paper, a new non-isolated three-port high voltage gain DC-DC converter with zero input current ripple at low voltage side is proposed. In the proposed converter, by changing the place of input voltage source between each of the three ports, three different operations with single-input and two-output structures are achieved. The proposed converter is analyzed. Finally, the analytical results are reconfirmed by using experimental results.

Manuscript received February 3, 2020; revised March 25, 2020; accepted June. 21, 2020.

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.3007959, IEEE Transactions on Power Electronics

II. The Proposed Converter

The power circuit of the proposed converter and its equivalent power circuit using a transformer model of the coupled inductors are shown in Figs. 1(a) and 1(b), respectively. In Fig. 1(a) three-winding coupled inductor consists of the inductances L_{p1} as first winding, L_{s1} as second winding, L_{t1} as third winding, and the mutual inductances M_{ps1}, M_{pt1}, M_{st1} as the coupling inductances between two windings of coupled inductor. By using a transformer model of the coupled inductors in Fig. 1(b) it can be seen that the first coupled inductor is modeled with the magnetizing inductor of L_{m1}, which is paralleled with the transformer T_1 and placed in series with the leakage inductance of L_{k1}. The first, second and third windings of transformer T_1 has N_{p1}, N_{s1} and N_{t1} turns, respectively. The turns ratio of the second and third windings of transformer T_1 is considered as $n_{s1} = N_{s1} / N_{p1}$ and $n_{t1} = N_{t1} / N_{p1}$. The capacitors $C_{\ell 1}$, $C_{\ell 2}$, C_2 are assumed to be large enough, so, the voltages across them are considered to be constant values as $V_{C\ell 1} = V_\ell$, $V_{C\ell 2} = V_\ell$, V_{C2}, respectively. The input current ripple at low voltage side is eliminated for the whole range of duty cycles by using third winding of the coupled inductors (the windings with turns ratio of n_{t1} and n_{t2}) and the capacitors $C_{\ell 1}$ and $C_{\ell 2}$. The voltage gain of first stage is increased by using a switch-inductor circuit that includes S_{b1}, S_{a1} and the second winding of coupled inductor (the winding with turn ratio of n_{s1}). The voltage gain of second stage is increased by using a switch-capacitor-inductor circuit that includes S_{a2}, S_{b2}, S_{c2} and the second winding of coupled inductor (the winding with turn ratio of n_{s2}). Fig. 2 illustrates the theoretical waveforms of the proposed converter for duty cycle condition of $D_1 > D_2$. From Fig. 2 it can be seen that the switch S_{b1} is turned ON when the switch S_{a1} is OFF. The switches S_{a2} and S_{c2} are turned ON when switch S_{b2} is OFF. Based on Fig. 2, the proposed converter has three modes during a switching period. Note that in the analysis, the index of the parameters associated with the first (upper) module (stage) in the equations is shown with 1 and the index of the parameters associated with the second (lower) module (stage) is shown with 2. Also, $i_{Lp1} = i_{\ell 1}$ and $i_{Lp2} = i_{\ell 2}$. The proposed converter has three different operations with single-input, two-output ports as explained in the following. The voltages across all components for the boost, buck and buck-and-boost operations are the same.

A. Boost operation

In this operation, the low voltage V_ℓ is utilized as the input voltage source. The higher voltages V_{H1} and V_{H2} is selected as output loads of R_{H1} and R_{H2}. The equivalent power circuits of this operation during a switching period is shown in Fig. 3 for $D_1 > D_2$. In the boost operation, the switches of MOSFETs S_{a1}, S_{a2} and the internal diodes of MOSFETs S_{b1}, S_{b2}, S_{c2} (D_{b1}, D_{b2}, D_{c2}) are active.

B. Buck operation

In this operation, the voltage V_{H1} is considered as input voltage source and the voltages of V_{H2} and V_ℓ are considered as output ports with output resistor loads of R_{H2} and R_ℓ, respectively. The equivalent power circuits of this operation during a swathing period is shown in Fig. 4 for $D_1 > D_2$.

C. Buck-and-Boost operation

In the third operation, the voltage V_{H2} is considered as input voltage source and the voltages of V_ℓ and V_{H1} are considered as output ports with output resistor loads of R_ℓ and R_{H1}, respectively. The equivalent power circuits of this operation during a switching period is shown in Fig. 5 for $D_1 > D_2$.

The illustrations of the second modes for all operations of the proposed converter when $D_2 > D_1$ is shown in Fig. 6. Note that the equivalent circuits for the first and third modes in $D_2 > D_1$ are same as the ones for $D_1 > D_2$ in all three boost, buck and buck-and-boost operations of the converter. Also, it is considered that $V_{H1} > V_{H2} > V_\ell$.

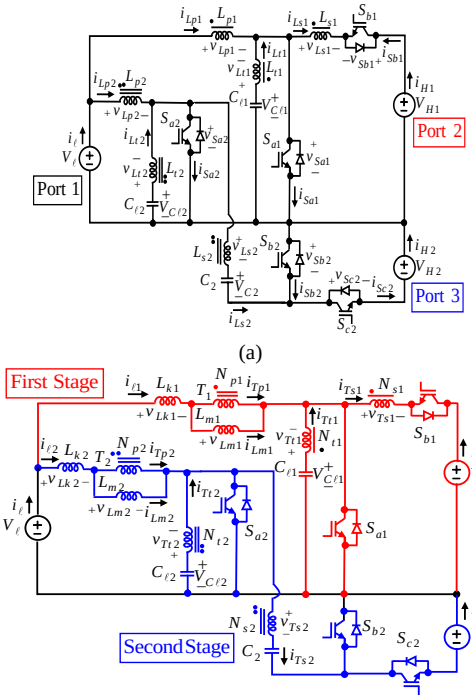

Fig. 1. Proposed three-port converter and its equivalent power circuit; (a) converter topology; (b) equivalent power circuit.

III. Analysis of The Proposed Converter

A. Analysis of First Stage circuit

In this part, the analysis of proposed converter during a switching period at the both first and second stages of the proposed converter in Fig. 1(b) is given. For simplifying the equations, the required conditions of achieving zero input current ripple at the low voltage side (i_ℓ) ($n_{t2} = n_{t1} = 1$), which are explained in details in sub-section D.

Time Interval of $0 < t < D_1 T_s$*:* During this time interval, the switch, S_{a1} is conducting, while the switch S_{b1} is OFF. This state is shown in Figs. 3(a), 3(b). Therefore, based on $n_{t1} = 1$, the voltage v_{Lm1} is equal to V_ℓ. As a result, the inductor current can be as follows:

$$i_{Lm1} = (V_\ell / L_{m1})(t - t_0) + i_{Lm1}\big|_{t=t_0} \quad (1)$$

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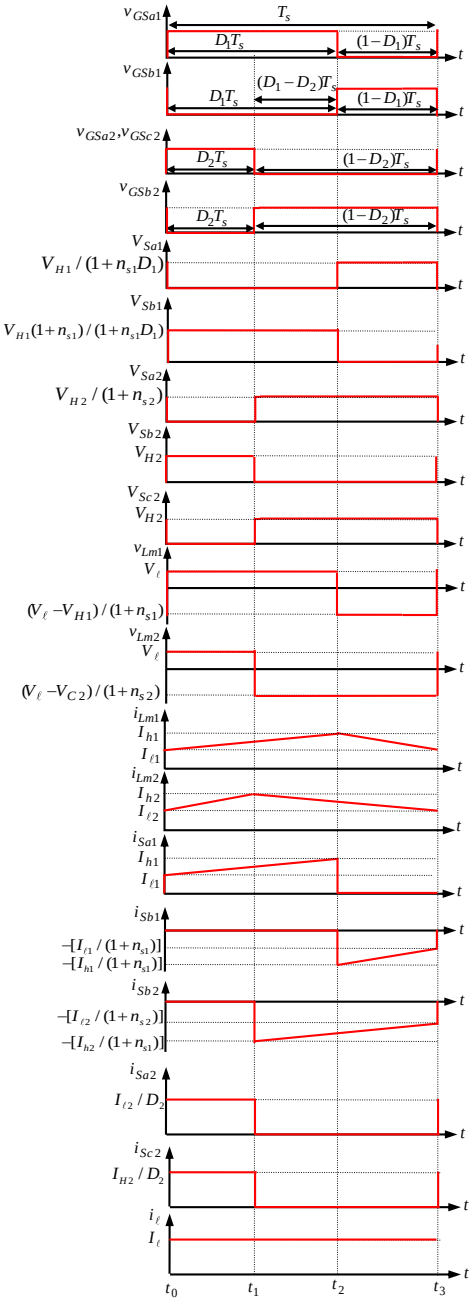


Fig. 2. Theoretical waveforms of the proposed converter during a switching period .for $D_1 > D_2$.

The relation between the windings' currents of first transformer T_1 can be written as $i_{Tt1} = -i_{Tp1} = i_{Lm1} - I_{\ell 1}$. The current of i_{Sa1} is calculated as $i_{Sa1} = i_{Lm1}$. The current of capacitor $C_{\ell 1}$ is calculated as $i_{C\ell 1} = -i_{Tt1} = I_{\ell 1} - i_{Lm1}$.

Based on Fig. 1(b), the average current of i_{Sa1} during a switching period in steady state is equal to $I_{Sa1} = I_{H1} + I_{\ell 1}$.

Time Interval of $D_1T_s < t < T_s$*:* During this time interval, the switch, S_{a1} is turned OFF, while the switch S_{b1} is ON.

This state is indicated in Fig. 3(c) and 6(a). Therefore, the voltage v_{Lm1} is calculated as $(V_\ell - V_{H1})/(1+n_{s1})$. Then, the inductor's current can be written as follows:

$$i_{Lm1} = [(V_\ell - V_{H1})/(1+n_{s1})](t-t_0)/L_{m1} + i_{Lm1}\big|_{t=D_1T_s} \quad (2)$$

Based on Fig. 1(b), the average current of i_{Sb1} during a switching period in the steady state is equal to $I_{Sb1} = I_{H1}$. The current i_{Sb1} is calculated as $i_{Sb1} = -i_{Lm1}/(1+n_{s1})$. Moreover, the current of capacitor $C_{\ell 1}$ is calculated as $i_{C\ell 1} = -i_{Tt1} = i_{Lp1} + i_{Sb1} = I_{\ell 1} - i_{Lm1}/(1+n_{s1})$.

Steady State Analysis of First Stage

In steady state, the voltage balance law for the inductor L_{m1} can be written as follows:

$$\tilde{v}_{Lm1} = D_1V_\ell + (1-D_1)(V_\ell - V_{H1})/(1+n_{s1}) = 0 \quad (3)$$

By simplifying the above equation, the first voltage conversion ratio of $G_1 = V_{H1}/V_\ell$ is obtained as follows:

$$G_1 = V_{H1}/V_\ell = (1+n_{s1}D_1)/(1-D_1) \quad (4)$$

The voltage stress on switch S_{b1} during $0 < t < D_1T_s$ and switch S_{a1} during $D_1T_s < t < T_s$ are calculated as follows:

$$V_{Sb1} = n_{s1}V_\ell + V_{H1} = V_{H1}(1+n_{s1})/(1+n_{s1}D_1) \quad (5)$$

$$V_{Sa1} = V_\ell - v_{Lm1} = V_\ell/(1-D_1) = V_{H1}/(1+n_{s1}D_1) \quad (6)$$

At the steady state, the current balance law for the capacitor $C_{\ell 1}$ can be written as follows:

$$\tilde{i}_{C\ell 1} = D_1(I_{\ell 1} - i_{Lm1}) + (1-D_1)[I_{\ell 1} - i_{Lm1}/(1+n_{S1})] = 0 \quad (7)$$

By simplifying the above equation, the average inductor current of i_{Lm1} can be obtained as follows:

$$I_{Lm1} = (1+n_{s1})(-I_{H1})/(1-D_1) \quad (8)$$

The relationship for the average currents of the first transformer T_1 at steady state considering Fig. 1(a) can be written as $I_{Tt1} + I_{Tp1} + n_{s1}I_{Ts1} = 0$. Based on Fig. 1(b), at steady state, it can be written that $I_{Tp1} = I_{\ell 1} - I_{Lm1}$, $I_{Ts1} = -I_{H1}$, $I_{Tt1} = -I_{C\ell 1} = 0$. As a result, it can be written that $I_{\ell 1} = n_{s1}I_{H1} + I_{Lm1}$. Consequently, according to (8), the average current of $I_{\ell 1}$ would be obtained as follows:

$$I_{\ell 1} = (1+n_{s1}D_1)(-I_{H1})/(1-D_1) \quad (9)$$

B. Analysis of Second Stage circuit

Interval time of $0 < t < D_2T_s$*:* During this time interval, the switches, S_{a2} and S_{c2} are conducting, while switch S_{b2} is OFF. This state is shown in Figs. 3(a) and 6(a). Therefore, considering $n_{t2} = 1$, the voltage v_{Lm2} is obtained as V_ℓ. Accordingly, the inductor current can be obtained as:

$$i_{Lm2} = (V_\ell/L_{m2})(t-t_0) + i_{Lm2}\big|_{t=t_0} \quad (10)$$

Based on Fig. 1(b), the average currents of i_{Sa2} and i_{Sc2} in steady state are calculated as $I_{Sa2} = I_{\ell 2}$ and $I_{Sc2} = I_{H2}$, respectively. The current of capacitors $C_{\ell 2}$ and C_2 are calculated as $i_{C\ell 2} = -[(1-D_2)I_{\ell 2} + I_{H2}]/D_2$ and $i_{C2} = i_{Sc2} = I_{H2}/D_2$, respectively.

Interval time of $D_2T_s < t < T_s$*:* During this time interval, the switches, S_{a2} and S_{c2} are turned OFF, while switch S_{b2} is ON. This state is shown in Figs. 3(b) and 3(c). As a result, the voltage v_{Lm2} is obtained as $(V_\ell - V_{C2})/(1+n_{s2})$. Therefore, it can be written that:

$$i_{Lm2} = [(V_\ell - V_{C2})/(1+n_{s2})](t-t_0)/L_{m2} + i_{Lm2}\big|_{t=D_2T_s} \quad (11)$$

Based on Fig. 1(b), the average current of i_{Sb2} during a switching period at steady state would be $I_{Sb2} = I_{H2}$. The currents of the second transformer is written as $i_{Tt2} = -(i_{Lp2} - i_{Lm2}) + n_{s2}i_{Sb2}$. The current of switch i_{Sb2} is calculated as $i_{Sb2} = -i_{Lm2}/(1+n_{s2})$. The current of capacitors

$C_{\ell 2}$ and C_2 are calculated as $i_{C\ell 2} = I_{\ell 2} - i_{Lm2}/(1+n_{s2})$ and $i_{C2} = I_{\ell 2} - i_{Lm2}/(1+n_{s2})$, respectively.

Steady State Analysis of Second Stage

At steady state, the voltage balance law for the inductor L_{m2} can be written as follows:

$$\tilde{v}_{Lm2} = D_2 V_\ell + (1-D_2)(V_\ell - V_{C2})/(1+n_{s2}) = 0 \quad (12)$$

By simplifying the above equation the voltage V_{C2} is obtained as follows:

$$V_{C2} = (1+n_{s2}D_2)V_\ell/(1-D_2) \quad (13)$$

The time interval of $0 < t < D_2 T_s$ is included in Figs. 3(a) and 6(a). As a result, it can be written that $V_{H2} = V_{C2} + n_{s2}V_\ell$. Consequently, the second voltage conversion ratio of $G_2 = V_{H2}/V_\ell$ is obtained as follows:

$$G_2 = V_{H2}/V_\ell = (1+n_{s2})/(1-D_2) \quad (14)$$

The voltage stress on switch S_{b2} during $0 < t < D_2 T_s$ and switches S_{a2} and S_{c2} during time interval $D_2 T_s < t < T_s$ will be as follows:

$$V_{Sb2} = n_{s2}V_\ell + V_{C2} = V_{H2} \quad (15)$$

$$V_{Sa2} = V_\ell - v_{Lm2} = V_\ell/(1-D_2) = V_{H2}/(1+n_{s2}) \quad (16)$$

$$V_{Sc2} = V_{H2} \quad (17)$$

The current balance law for the capacitor C_2 is written as follows:

$$\tilde{i}_{C2} = D_2(I_{H2}/D_2) + (1-D_2)I_{Lm2}/(1+n_{s2}) = 0 \quad (18)$$

The relationship between the average currents of second transformer T_2 at the steady state considering Fig. 1(b) is written as $I_{Tt2} + I_{Tp2} + n_{s2}I_{Ts2} = 0$. Moreover, in steady state it can be written that $I_{Tp2} = I_{\ell 2} - I_{Lm2}$, $I_{Ts2} = I_{C2} = 0$, $I_{Tt2} = -I_{C\ell 2} = 0$. As a result, it can be written that $I_{\ell 2} = I_{Lm2}$. Consequently, the average inductor current of i_{Lm2} and the average current of low voltage source (V_ℓ) can be obtained as follows:

$$I_{\ell 2} = I_{Lm2} = (1+n_{s2})(-I_{H2})/(1-D_2) \quad (19)$$

All the equations in (1)-(19) are the same for boost, buck and buck-and-boost operations of the proposed converter

C. Output Currents' Calculations

C.1. Boost Operation

In the boost operation, based on Fig. 3, the output currents I_{RH1} and I_{RH2} are equal to $I_{RH1} = -I_{H1} = V_{H1}/R_{H1}$ and $I_{RH2} = -I_{H2} = V_{H2}/R_{H2}$, respectively. The output powers should be written as $P_{H1} = V_{H1}^2/R_{H1}$, $P_{H2} = V_{H2}^2/R_{H2}$. The total output power (P_{oT}) is equal to $P_{oT} = P_{H1} + P_{H2}$.

C.2. Buck Operation

In the buck operation, based on Fig. 4, the output currents are equal to $I_{R\ell} = -I_\ell = V_\ell/R_\ell$ and $I_{RH2} = -I_{H2} = V_{H2}/R_{H2}$, respectively. The output powers would be obtained as $P_\ell = V_\ell^2/R_\ell$, $P_{H2} = V_{H2}^2/R_{H2}$. The total output power (P_{oT}) is written as $P_{oT} = P_\ell + P_{H2}$.

C.3. Buck-and boost-Operation

In buck-and-boost operation, considering Fig. 5, the output currents $I_{R\ell}$ and I_{RH1} are equal to $I_{R\ell} = -I_\ell = V_\ell/R_\ell$ and $I_{RH1} = -I_{H1} = V_{H1}/R_{H1}$, respectively. The output powers would be obtained as $P_\ell = V_\ell^2/R_\ell$, $P_{H1} = V_{H1}^2/R_{H1}$. The total output power (P_{oT}) is written as $P_{oT} = P_\ell + P_{H1}$.

D. Cancelling Input Current Ripple at the low voltage side (i_ℓ)

In this part, the required conditions of achieving zero input current ripple at the low voltage side (i_ℓ) are obtained during a switching period. According to the Fig. 1, the values of inductances L_{p1}, L_{s1}, L_{t1}, M_{ps1}, M_{pt1} and M_{st1}, can be replaced based on the used parameters in Fig. 1(b) as follows:

$$L_{p1} = L_{m1} + L_{k1},\ L_{t1} = n_{t1}^2 L_{m1},\ L_{s1} = n_{s1}^2 L_{m1},\ M_{pt1} = M_{tp1} = n_{t1}L_{m1},$$
$$M_{ps1} = M_{sp1} = n_{s1}L_{m1},\ M_{ts1} = M_{st1} = n_{t1}n_{s1}L_{m1} \quad (20)$$

In the same way, the second coupled inductor in Fig. 1(a) is modelled as Fig. 1(b). The voltages across the windings of the first coupled inductor in Fig. 1(a) can be written as follows:

$$v_{Lp1} = L_{p1}(di_{Lp1}/dt) + M_{ps1}(di_{Ls1}/dt) + M_{pt1}(di_{Lt1}/dt) \quad (21)$$

$$v_{Ls1} = M_{ps1}(di_{Lp1}/dt) + L_{s1}(di_{Ls1}/dt) + M_{st1}(di_{Lt1}/dt) \quad (22)$$

$$v_{Lt1} = M_{pt1}(di_{Lp1}/dt) + M_{st1}(di_{Ls1}/dt) + L_{t1}(di_{Lt1}/dt) \quad (23)$$

D.1. Cancelling Input Current Ripple at first stage $(i_{\ell 1})$

Time Interval of $0 < t < D_1 T_s$*:* According to Fig. 1(a), it can be seen that $i_{Ts1} = i_{Ls1} = 0$. As a result, the voltages v_{Lp1} and v_{Lt1} are equal to V_ℓ. Accordingly, considering (20) and (21), it is obtained that:

$$di_{Lp1}/dt = V_\ell(L_{t1} - M_{pt1})/(L_{t1}L_{p1} - M_{pt1}^2) \quad (24)$$

As a result, the required conditions for achieving zero input current ripple at first stage is obtained as follows:

$$L_{t1} = M_{pt1} \quad or \quad n_{t1}^2 L_{m1} = n_{t1}L_{m1} \quad or \quad n_{t1} = 1 \quad (25)$$

$$M_{pt1}^2 \neq L_{p1}L_{t1} \quad or \quad L_{k1} \neq 0 \quad (26)$$

Time Interval of $D_1 T_s < t < T_s$*:* In this state, based on Fig. 1(a), $v_{Lp1} = v_{Lt1}$, $i_{Lp1} + i_{Lt1} = i_{Ls1}$ and $v_{Ls1} + v_{Lp1} = V_\ell - V_{H1}$ are verified. Accordingly, it can be obtained that:

$$di_{Lp1}/dt = (V_\ell - V_{H1})D/(BD + AC) \quad (27)$$

As a result, the required conditions for achieving zero input current ripple at first stage, can be obtained as follows:

$$(D = L_{t1} + M_{st1} - M_{ps1} - M_{pt1} = 0)\ or\ (n_{t1} = 1) \quad (28)$$

$$(C = L_{p1} + M_{ps1} - M_{pt1} - M_{st1} \neq 0)\ or\ (L_{k1} \neq 0) \quad (29)$$

Interval time of $0 < t < D_2 T_s$*:* Considering Fig. 1(a) and $i_{Lp2} + i_{Lt2} = (I_{\ell 2}/D_2) + i_{Ls2}$, the following equations can be obtained:

$$v_{Lt2} + v_{Ls2} = v_{Ls2} + v_{Lp2} = V_\ell + V_{H1} - V_{C2} \quad (30)$$

$$di_{Lp2}/dt = (V_\ell + V_{H2} - V_{C2})D/(BD + AC) \quad (31)$$

Therefore, the required conditions for achieving zero input current ripple, is obtained as follows:

$$(D = 0)\ or\ (n_{t2} = 1)\ and\ (C \neq 0)\ or\ (L_{k2} \neq 0) \quad (32)$$

D.2. Cancelling Input Current Ripple at second stage $(i_{\ell 2})$

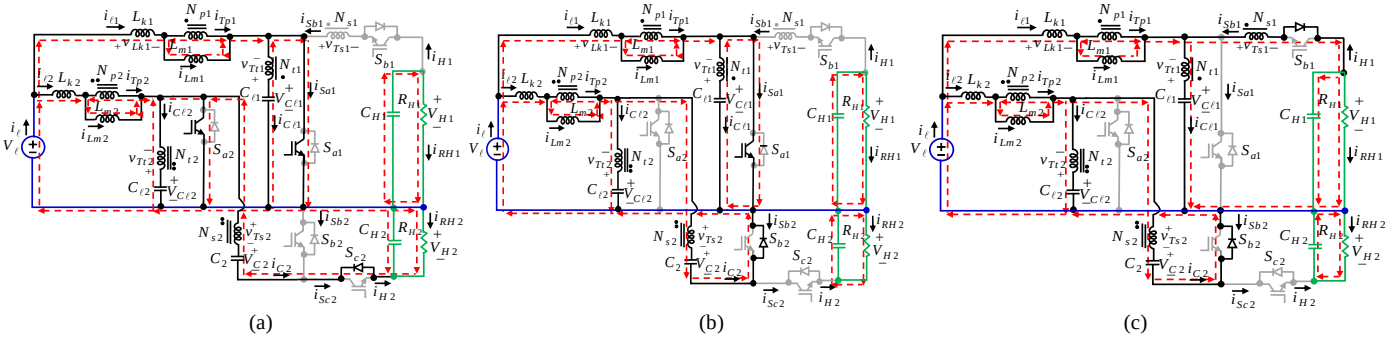
Interval time of $D_2 T_s < t < T_s$*:* During this time interval, the equation $i_{Lp2} + i_{Lt2} = i_{Ls2}$ and the following equations can be obtained:

$$v_{Lt2} + v_{Ls2} = v_{Ls2} + v_{Lp2} = V_{C2} - V_{C\ell 2} = V_\ell - V_{C2} \quad (33)$$

$$di_{Lp2}/dt = (V_\ell - V_{C2})D/(BD + AC) \quad (34)$$

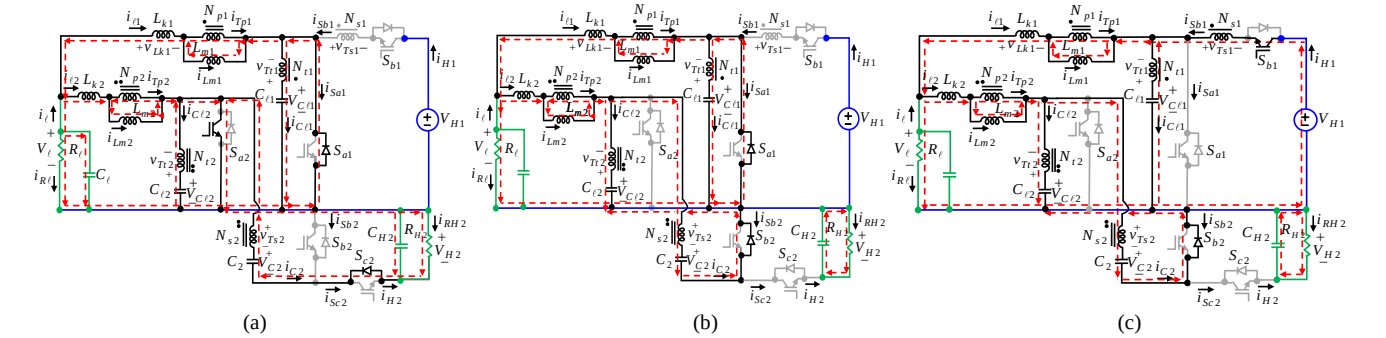
As a result, the required conditions for achieving zero input current ripple would be the same as (32). From the explanations above, zero input current ripple has been achieved for the whole range of duty cycles for all the operation modes of the converter.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.3007959, IEEE Transactions on Power Electronics



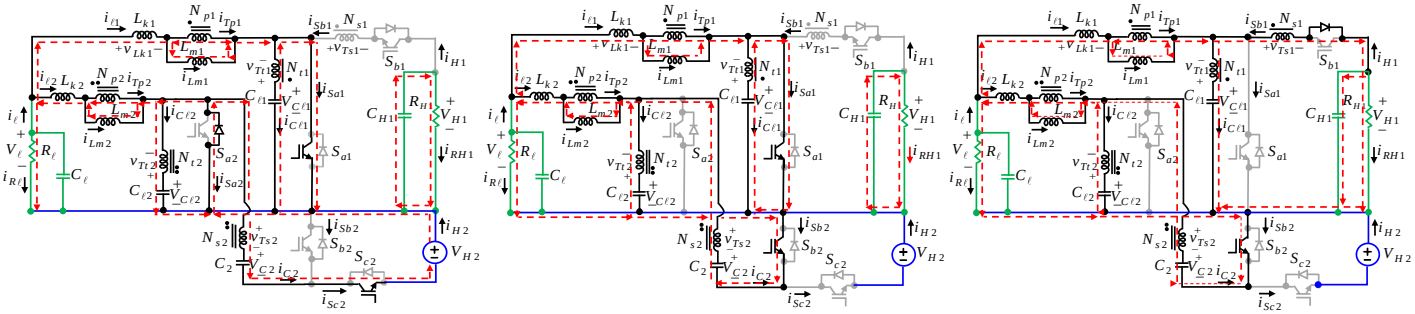
(a) (b) (c)

Fig. 3. Equivalent power circuit of the boost operation during a switching period for $D_1 > D_2$; (a) Mode 1; (b) Mode 2; (c) Mode 3.



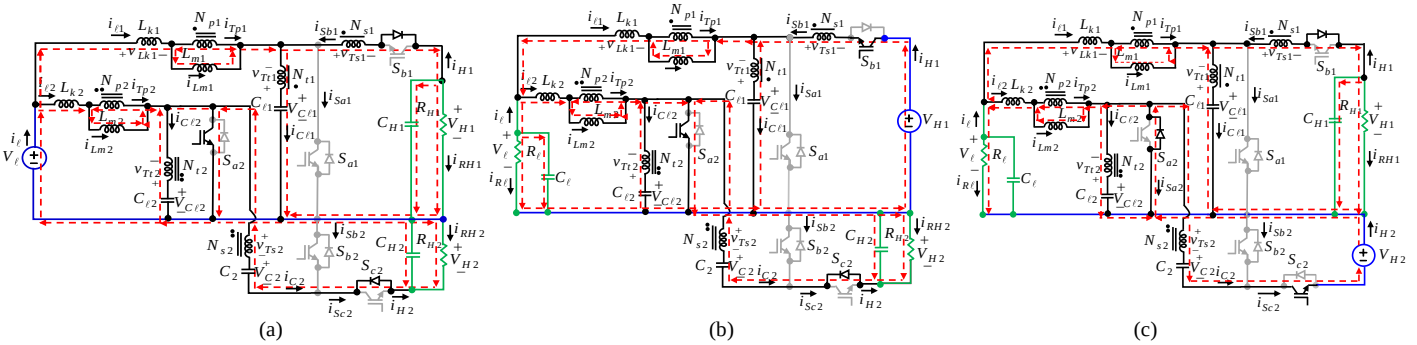
(a) (b) (c)

Fig. 4. Equivalent power circuits of buck operation during a switching period for $D_1 > D_2$; (a) Mode 1; (b) Mode 2; (c) Mode 3.



(a) (b) (c)

Fig. 5. Equivalent power circuit of buck-and-boost operation during a switching period for $D_1 > D_2$; (a) Mode 1; (b) Mode 2; (c) Mode 3.



(a) (b) (c)

Fig. 6. Equivalent power circuit of boost, buck, buck-and-boost operations during Mode 2 for $D_2 > D_1$; (a) boost operation; (b) buck operation; (c) buck-and-boost operation.

E. Design Considerations

In continuous conduction mode (CCM) operation of the proposed converter, the average values of the currents passing through the inductances L_{m1} and L_{m2} have to be higher than half of their current ripples $[I_{Lm} > (\Delta I_{Lm} / 2)]$. Consequently, the following inequalities has to be verified.

$$L_{m1} > D_1(n_{s1}D_1 + 1)V_\ell / [2(1+n_{s1})I_\ell f_s] \quad (35)$$

$$L_{m2} > (V_\ell D_2 T_s) / [2(I_{\ell 2})] = (D_2 / 2f_s)(V_\ell / I_{\ell 2}) \quad (36)$$

On the other hand, in practice, the illustrated circuit in Fig. 1(a) for the proposed converter is used and the value of the inductances of coupled inductors should be specified to achieve CCM operation and cancellation of input currents ripple. According to (20) and considering $n_{t2} = n_{t1} = 1$, $L_{k1} \neq 0$ and $L_{k2} \neq 0$ for achieving ripple free input currents and CCM operation, the inductances of coupled inductors in Fig. 1(a) based on parameters of $L_{k1}, n_{s1}, n_{t1}, L_{m1}, n_{s2}, n_{t2}, L_{m2}$ and L_{k2} can be simplified as follows:

$$\begin{aligned} &L_{p1} = L_{m1} + L_{k1} = L_{m1} / K_1^{\,2},\ L_{S1} = n_{s1}^{\,2} L_{m1}, L_{t1} = L_{m1} \\ &M_{pt1} = M_{tp1} = L_{m1}, M_{ps1} = M_{sp1} = M_{st1} = M_{ts1} = n_{s1} L_{m1} \end{aligned} \quad (37)$$

$$\begin{aligned} &L_{p2} = L_{m2} + L_{k2} = L_{m2} / K_2^{\,2},\ L_{s2} = n_{s2}^{\,2} L_{m2},\ L_{t2} = L_{m2} \\ &M_{pt2} = M_{tp2} = L_{m2}, M_{ps2} = M_{sp2} = M_{st2} = M_{ts2} = n_{s2} L_{m2} \end{aligned} \quad (38)$$

where K_1 and K_2 are coupling coefficients of the coupled inductors which are defined as $K_1=\sqrt{L_{m1}/(L_{k1}+L_{m1})}$ and $K_2=\sqrt{L_{m2}/(L_{k2}+L_{m2})}$, where in practice $0\ll K_1,K_2\le 1$. By considering the hold-up time required for step-load response, voltage ripple across each of the output capacitors (ΔV_{Co}) and voltage ripple caused by the Equivalent Series Resistance (ESR) of the output capacitors $\Delta V_{o1}=\Delta V_{Co1}+\Delta V_{Co-ESR}=\Delta V_{Co1}+r_{Co1}\Delta I_{Co1}$. As a result, the minimum value of capacitors can be calculated as given in Table I.

F. Small Signal analysis and Controlling system for Boost Operation of the Proposed Converter

According to Fig. 3, it is assumed that the inductor currents i_{Lk1}, i_{Lm1}, i_{Lk2} and i_{Lm2}, capacitor voltages $v_{C\ell1}$, $v_{C\ell2}$, v_{CH1}, v_{C2} and v_{CH2} are the state variables. The input voltage source v_ℓ is defined by source vector u_{in}. The output voltages are v_{CH1} and v_{CH2} which should be regulated. Accordingly, the state matrixes as follows:

$$sX = AX + B_0\tilde{v}_\ell + B_1\tilde{d}_1 + B_2\tilde{d}_2 \tag{39}$$

The state matrix A and matrixes B_1, B_2 are obtained as follows:

$$X=\begin{bmatrix}\tilde{i}_{Lk1}\\ \tilde{i}_{Lm1}\\ \tilde{v}_{C\ell1}\\ \tilde{v}_{CH1}\\ \tilde{i}_{Lk2}\\ \tilde{i}_{Lm2}\\ \tilde{v}_{C\ell2}\\ \tilde{v}_{C2}\\ \tilde{v}_{CH2}\end{bmatrix},\ B_0=\begin{bmatrix}1/L_{k1}\\0\\0\\0\\1/L_{k2}\\0\\0\\0\\0\end{bmatrix},\ B_1=\begin{bmatrix}0\\(n_{s1}V_\ell+V_{H1})/(1+n_{s1})/L_{m1}\\-I_{Lm1}[n_{s1}/(1+n_{s1})]/C_{\ell1}\\-I_{Lm1}/(1+n_{s1})/C_{H1}\\0\\0\\0\\0\\0\end{bmatrix} \tag{40}$$

$$B_2=\begin{bmatrix}0\\0\\0\\0\\0\\(n_{s2}V_\ell+V_{C2})/(1+n_{s2})/L_{m2}\\\dfrac{-I_{Lm2}n_{s2}}{(1+n_{s2})C_{\ell2}}+\dfrac{n_{s2}(V_{CH2}-V_{C2}-n_{s2}V_\ell)}{r_CC_{\ell2}}\\\dfrac{\dfrac{I_{Lm2}}{(1+n_{s2})}+(V_{CH2}-V_{C2}-n_{s2}V_\ell)/r_C}{C_2}\\(-V_{CH2}+V_{C2}+n_{s2}V_\ell)/r_C/C_{H2}\end{bmatrix},\ A=\begin{bmatrix}0&0&-1/L_{k1}&0&0&0&0&0&0\\0&0&\dfrac{1+n_{s1}D_1}{(1+n_{s1})L_{m1}}&\dfrac{-(1-D_1)}{(1+n_{s1})L_{m1}}&0&0&0&0&0\\\dfrac{1}{C_{\ell1}}&\dfrac{-(1+n_{s1}D_1)}{(1+n_{s1})C_{\ell1}}&0&0&0&0&0&0&0\\0&\dfrac{1-D_1}{(1+n_{s1})C_{H1}}&0&\dfrac{-1}{R_{H1}C_{H1}}&0&0&0&0&0\\0&0&0&0&0&0&-1/L_{k2}&0&0\\0&0&0&0&0&0&\dfrac{1+n_{s2}D_2}{(1+n_{s2})L_{m2}}&\dfrac{-(1-D_2)}{(1+n_{s2})L_{m2}}&0\\0&0&0&0&\dfrac{1}{C_{\ell2}}&\dfrac{-(1+n_{s2}D_2)}{(1+n_{s2})C_{\ell2}}&\dfrac{-n_{s2}{}^2D_2}{r_CC_{\ell2}}&\dfrac{-n_{s2}D_2}{r_CC_{\ell2}}&\dfrac{n_{s2}D_2}{r_CC_{\ell2}}\\0&0&0&0&0&\dfrac{1-D_2}{(1+n_{s2})C_2}&\dfrac{-n_{s2}D_2}{r_CC_2}&\dfrac{-D_2}{r_CC_2}&\dfrac{D_2}{r_CC_2}\\0&0&0&0&0&0&\dfrac{n_{s2}D_2}{r_CC_{H2}}&\dfrac{D_2}{r_CC_{H2}}&-\left(\dfrac{D_2}{r_C}+\dfrac{1}{R_{H2}}\right)\dfrac{1}{C_{H2}}\end{bmatrix} \tag{41}$$

TABLE I MINIMUM ESTIMATED VALUES OF CAPACITORS

$C_{\ell1\_\min}$	$D_1(-n_{s1})(-I_{H1})/\left[0.01V_{C\ell1}-r_{C\ell1}\dfrac{n_{s1}(-I_{H1})}{(1-D_1)}\right]f_s$
$C_{\ell2\_\min}$	$n_{s2}(-I_{H2})/\{[0.01V_{C\ell2}-r_{C\ell2}n_{s2}(-I_{H2})/[(1-D_2)D_2]]f_s\}$
$C_{2\_\min}$	$-I_{H2}/\{[0.01V_{C2}-r_{C2}(-I_{H2})/[D_2(1-D_2)]]f_s\}$
$C_{H1-\min}$	$C_{H1\_ESR}=D_1I_{H1}/\{[0.01V_{CH1}-r_CI_{H1}/(1-D_1)]f_s\}$ $C_{H1\_THT}=\dfrac{1}{0.01R_{H1}(0.1f_s)}$, $C_{H1-\min}=\max(C_{H1\_ESR},C_{H1\_THT})$
$C_{H2-\min}$	$C_{H2\_ESR}=\dfrac{(1-D_2)I_{H2}}{[0.01V_{CH2}-r_C(-I_{H2})/D_2]f_s}$ $C_{H2\text{-}THT}=\dfrac{1}{0.01R_{H2}(0.1f_s)}$, $C_{H2-\min}=\max(C_{H2}\vert_{ESR},C_{H2}\vert_{THT})$

As a result, the transfer functions of the output voltages v_{CH1} v_{CH2} are obtained as follows:

$$G_1(s)=\left.\frac{\tilde{v}_{CH1}}{\tilde{d}_1}\right|_{\tilde{v}_\ell=0}=\frac{G_{v_{CH1}-d1}(s)}{G_p(s)}=C_1B_1(sI-A)^{-1} \tag{42}$$

$$G_2(s)=\left.\frac{\tilde{v}_{CH2}}{\tilde{d}_2}\right|_{\tilde{v}_\ell=0}=\frac{G_{v_{CH2}-d2}(s)}{G_p(s)}=C_2B_2(sI-A)^{-1} \tag{43}$$

where;

$$C_1=[0\ \ 0\ \ 0\ \ 1\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0] \tag{44}$$

$$C_2=[0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 1] \tag{45}$$

Therefore, by adjusting the PI parameters K_{p1} and K_{i1} of the voltage loop controllers, the closed-loop system of the proposed converter which is shown in Fig. 7, can achieve a better stability performance.

$$G_{c1}=K_{p1}+K_{i1}/s=0.00001+0.012/s \tag{46}$$

$$G_{c2}=K_{p2}+K_{i2}/s=0.00001+0.016/s \tag{47}$$

In order to generate the drive signals for S_{a1} and S_{a2} in Fig. 7 the PWM technique is used and D_1 and D_2 are respectively compared with the sawtooth wave *Vt*. When D_1 is higher than V_t, S_{a1} is in on-state. Moreover, S_{a2} is in on-state when D_2 is larger than V_t.

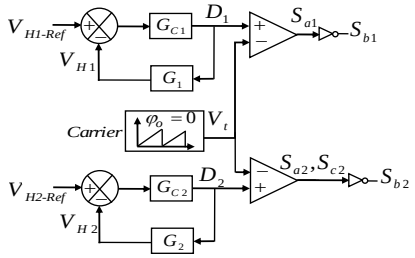


Fig .7. Closed loop controller of the output voltages for the proposed converter in boost operation.

IV. COMPARISON RESULTS

For comparing the proposed converter and the conventional multi-port converters, the DC characteristics including voltage conversion ratio of first output port (G_{port-1}), second output port (G_{port-2}), total voltage gain (G_T), the total normalized maximum voltage stresses on the switches and diodes $[\Sigma(V_S+V_D)_{\max}/V_{o\_\max}]$, number of switches (N_S), diodes (N_D), inductors (N_I), capacitors (N_C), coupled-inductors (N_{CI}) the total components number (N_T), input current ripple (Δi_i), the common ground of the ports and size of compared converters are summarized in Table II.

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TABLE II COMPARISON OF HIGH VOLTAGE GAIN SINGLE-INPUT/DUAL-OUTPUT CONVERTERS

DC-DC Converters	$G_{port\_1}=V_{o1}/V_i$	$G_{port\_2}=V_{o2}/V_i$	G_T	$\Sigma(V_S+V_D)_{max}/V_{o\_max}$	N_S	N_D	N_I	N_C	N_{CI}	N_T	Δi_i	⏚	Size
[2]	$1/(1-D)$	$1/D$	$[1/(1-D)]+1/D$	3	3	-	2	4	2	11	Low	Yes	Medium
[3-A]	$1/(1-D)$	$-1/(1-D)$	$2/(1-D)$	4	1	3	1	3	-	8	Low	Yes	Small
[3-B]	$1/(1-D)$	$2/(1-D)$	$3/(1-D)$	5/2	1	3	1	3	-	8	Low		Small
[3-C]	$1/(1-D)$	$(2-D)/(1-D)$	$(3-D)/(1-D)$	$4/(1-D)$	1	3	1	3	-	8	High		Small
[6]	$2N/(1-D)$	$D/(1-D)$	$(2n+D)/(1-D)$	$2+(2/n)$	4	3	-	3	2	12	High	No	Big
[16]	$D/(1-D)$	$\simeq D/(1-D)$	$2D/(1-D)$	$3/D$	2	1	3	3	-	9	Low	Yes	Medium
[17]	$\simeq 1/(2D)$	$\simeq 1/(2D)$	$\simeq 1/D$	6	2	2	1	2	-	7	Low	No	Medium
[18]	$\simeq 1/D$	$1/D$	$2/D$, $0<D<0.5$	3	3	3	1	3	-	10	High	Yes	Big
[19]	$1/(2-2D)$ $0.5<D<1$	$(1-D)/(2-2D)$ $0.5<D<1$	$(2-D)/(2-2D)$ $0.5<D<1$	3	4	2	2	3	-	11	Equal to zero	No	Medium
[23]	$1/(1-D)$	$1/(1-D)$	$2/(1-D)$	4	2	2	-	2	1	7	low	No	Medium
Proposed converter	$(n_{s1}D+1)/(1-D)$	$(n_{s2}+1)/(1-D)$	$(n_s+n_sD+2)/(1-D)$	$2/(n_s+1)+3$	5	-	-	6	2	13	Equal to zero	Depending on the application	Medium

To achieve a fair comparison DC-DC single-input, dual-output converters are selected to compare with the proposed converter. Please, note that the proposed converter shares the same negative polarity among two ports of 1 and 2 but for one of the ports (Port 3) it shares the positive polarity with other two ports which means that the polarity of the voltage in Port 3 is reversed. As a result, depending on the application of the proposed converter whether the Port 3 is going to supply an inverter there would be no polarity consideration but in the case of DC loads the polarity of the third port is reverse from other two ports. Considering Table II and turn ratio of coupled inductors $n=4$, Figs. 8(a)-8(d) are plotted. Fig. 8(a) shows the ratio of total voltage gain (G_T) versus duty cycle, which demonstrates that the proposed converter can provide higher voltage gain. Fig. 8(b) shows the ratio of total voltage gain over the total components number (G_T/N_T) versus duty cycle. Based on Fig. 8(b), the proposed converter performs better than other compared converters considering the number of utilized components. G_T in the SIDO converters is defined as $G_T=V_{o1}/V_i+V_{o2}/V_i$. Fig. 8(c) shows that the ratio of G_T/N_S in the proposed converter is higher than the compared converters. Fig. 8(d) shows the ratio of $\Sigma(V_{S\_max}+V_{D\_max})/V_{o\_max}$, which the proposed converter has the medium value comparing to other compared converters.

In Fig. 9, the power density of the proposed converter comparing to other multiport converters is illustrated. From Fig. 9(a), the proposed converter is third from the aspect of power density and the power extracted from every cm^3 unit of the converter. Note that to achieve the results of Fig. 9, the converters are considered to be operated in the power of 250W. Also, Fig. 9(b) shows the volume of the compared converters considering the contributions of the elements in the total size of the converters and neglecting the extra accessories and spaces for measurements. From Fig. 9(b), the proposed converter has medium size among other compared multiport DC converters. Moreover, considering Table II the input current ripple is equal to zero in the proposed converter, which is not the same for other compared converters.

V. EXPERIMENTAL RESULTS

In this part, the theoretical analysis is reconfirmed by using experimental results for two operations of the proposed converter. The values of used parameters in the experimental prototype are given in Table III.

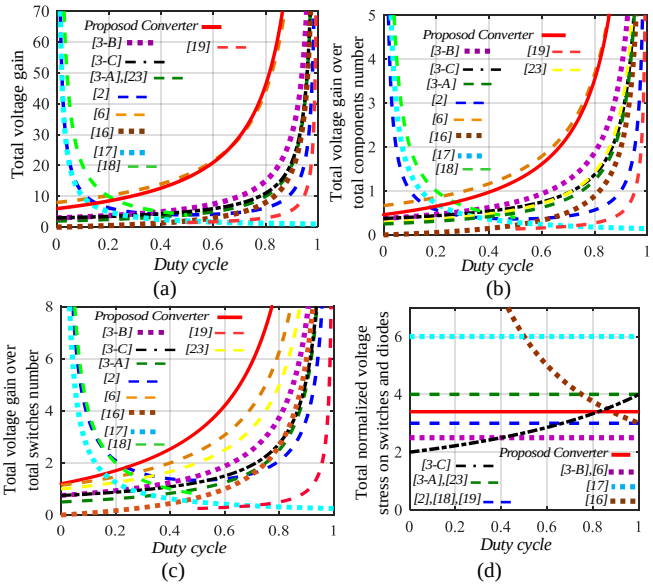

Fig. 8. The comparison results versus duty cycle *(D)*; (a) total voltage gain; (b) total voltage gain over the total component number; (c) total voltage gain over the number of switches; (d) total normalized voltage stress on switches and diodes.

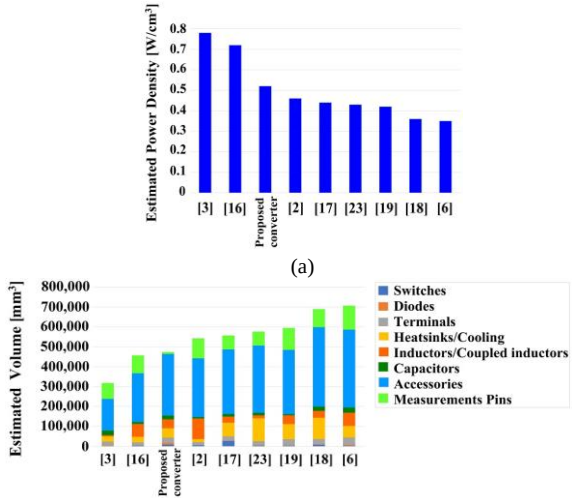

Fig. 9. The comparison results; (a) the estimated power density per $[W/cm^3]$, (b) the estimated volume per $[mm^2]$.

A. Boost operation of the proposed converter

In the practical prototype of proposed converter for this operation, two output loads of $R_{H1}=370\,\Omega$ and $R_{H2}=380\,\Omega$, a low input voltage of $V_\ell=24\,V$ as source are used.

The total output power of the boost operation of the proposed converter based on Table IV, is equal to $P_{oT} = P_{H1} + P_{H2} = 401W$. Measured results shown in Figs. 10 and 11 for this operation of the converter. First and second stages can be compared with the values listed in Table IV. A comparison shows that the experimental results confirm the theoretical results to a great extent. Both two output voltages can be controlled simultaneously to an acceptable extent as shown in Fig. 12. The output voltages regulation under variation of the input voltage, increasing suddenly from 24 V to 34 V and dropping to 14 V are extracted.

TABLE III EXPERIMENTAL PARAMETERS

Voltages	$V_\ell / V_{H1} / V_{H2} = 24V / 304V / 240V$
Output Powers	For boost operation: $P_{H1} / P_{H2} = 250W / 151W$ For buck operation: $P_\ell / P_{H2} = 250W / 150W$
Duty cycles/Frequency	$D_1 = 0.7$, $D_2 = 0.6$, $f_s = 50\,kHz$
Capacitors	$C_{\ell 1} = 220\mu F$, $C_{\ell 2} = C_2 = 100\mu F$
Output capacitors	For boost operation: $C_{H1} = C_{H2} = 100\mu F$ For buck operation: $C_\ell = C_{H2} = 100\mu F$ For buck and boost operation: $C_\ell = C_{H1} = 100\mu F$
Inductors	$L_{m1} = L_{m2} = 150\,\mu H$, $L_{k1} = L_{k2} = 10\mu H$ $n_{S1} = 4$, $n_{S2} = 3$, Type: Toroid TDK PC40-T72
Switches/Diodes	$S_{a1}, S_{a2}, S_{b1}, S_{b2}, S_{c2}$: IPW60R017C7 Reverse parallel diodes: DSEI 120
Loads	$R_{H1} = 370\,\Omega$, $R_{H2} = 380\,\Omega$ for boost operation $R_\ell = 2.3\,\Omega$, $R_{H2} = 380\,\Omega$ for buck operation

TABLE IV CALCULATED THEORETICAL VALUES FOR BOOST OPERATION

The capacitors values considering $r_C = 0.05\Omega$	$C_{\ell 1\_min} = 149\,\mu F$, $C_{2\_min} = 8.13\,\mu F$, $C_{\ell 2\_min} = 24.5\,\mu F$, $C_{H1\_min} = 54\,\mu F$, $C_{H2\_min} = 52.6\,\mu F$
L_{m1} and L_{m2}	$L_{m1} > 12.3\,\mu H$, $L_{m2} > 22.85\,\mu H$
First stage's voltages	$V_{H1} = 304V$, $V_{Sa1} = 80V$ during $(1-D_1)T_s$ $V_{Sb1} = 400V$ during D_1T_s
First stage's currents ($I_{\ell 1}$, I_{Lm1}, $-I_{H1}$)	$I_{\ell 1} = 10.38\,A$, $I_{Lm1} = 13.66\,A$, $-I_{H1} = V_{H1} / R_{H1} = 0.82\,A$ $I_{Sa1} = I_{Lm1} = 13.66\,A$ during D_1T_s $I_{Sb1} = -I_{Lm1} / (1+n_{s1}) = -2.73\,A$ during $(1-D_1)T_s$
Output power	$P_{H1} = V_{H1}^2 / R_{H1} = 250\,W$
Second stage's voltages	$V_{H2} = 240V$, $V_{C2} = 168V$, $V_{Sc2} = 300V$ during $(1-D_2)T_s$ $V_{Sa2} = 60V$ during $(1-D_2)T_s$, $V_{Sb2} = 240V$ during D_2T_s
Second stage's currents ($I_{\ell 2}$, I_{Lm2} , $-I_{H2}$)	$I_{\ell 2} = I_{Lm2} = 6.3\,A$, $I_{o2} = -I_{H2} = V_{H2} / R_{H2} = 0.63\,A$ $i_{Sa2} = I_{\ell 2} / D_2 = 10.5\,A$ during D_2T_s $i_{Sb2} = 1.575\,A$ during $(1-D_2)T_s$ $i_{Sc2} = I_{H2} / D_2 = -1.05\,A$ during D_2T_s
Output power	$P_{H2} = V_{H2}^2 / R_{H2} = 151W$

B. Buck operation of the Proposed converter

In the practical prototype of proposed converter for this operation, two output loads of $R_{H2} = 380\,\Omega$ and $R_\ell = 2.3\,\Omega$ are supplied by using the high input voltage source of $V_{H1} = 304\,V$. In this operation, the voltage stress on switches, V_{H2} , V_{C2} , are same as in boost operation. The output power is equal to $P_{oT} = P_\ell + P_{H2} = 401W$. The average value of currents $I_{\ell 2}$, output current of I_{o2} and the average currents of switches in the second stage are calculated to be the same as boost operation. Therefore, theoretical results that are listed in Table V and experimental results are shown in Fig. 13 to verify each other. Note that the rest of the values of the theoretical analysis, which are not provided in Table V are the same as the ones in Table IV.

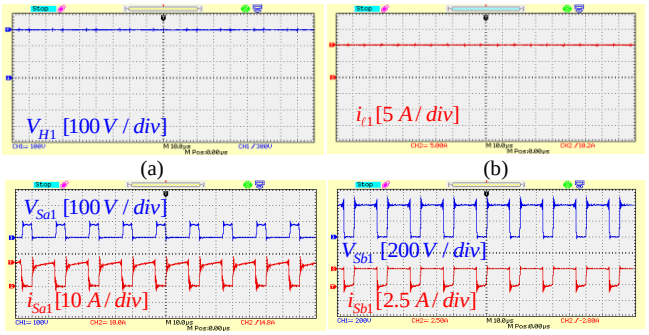

Fig. 10. Voltages and currents of first stage for boost operation.

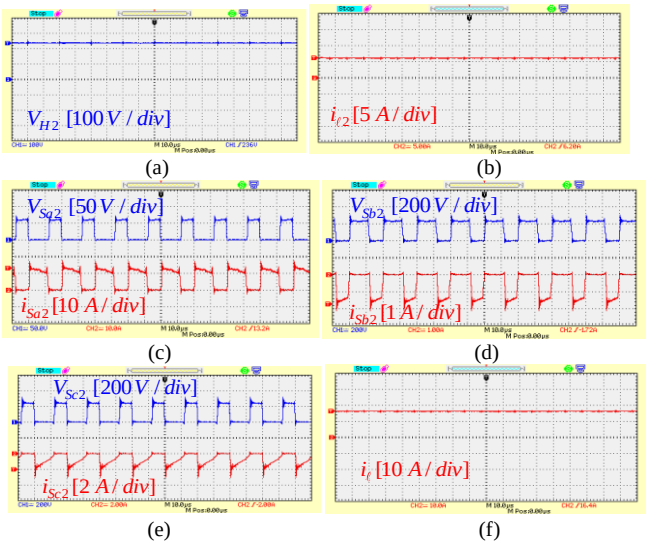

Fig. 11. Voltages and currents of second stage for boost operation.

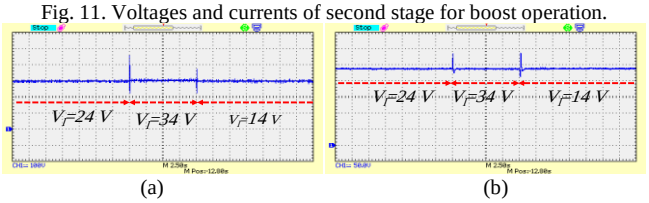

Fig. 12. Output voltages regulation and dynamic response under the input voltage variation for boost operation; (a) V_{H1} ; (b) V_{H2} .

C. Efficiency of the Proposed converter

In boost operation, the power loss calculation is done for the output power equal to $P_{oT} = 400\,W$. where, $P_{H1} = 250\,W$ and $P_{H2} = 150\,W$. Therefore, the total power loss is obtained as $P_{Loss} = 24.8444W$. In the buck operation, the power loss calculation is done for the output power equal to $P_{oT} = 400\,W$. where, $P_\ell = 250\,W$ and

$P_{H2}=150\,W$. Therefore, the total power loss is obtained as $P_{Loss}=39.6058W$. In buck-and-boost operation, the power loss calculation is done for the output power equal to $P_{oT}=400\,W$. where, $P_{\ell}=250\,W$ and $P_{H2}=150\,W$. Therefore, the total power loss is obtained as $P_{Loss}=42.81W$. As a result, the power loss distribution among the different components for three operations is shown in Fig. 14. The theoretical calculated and experimental efficiency curves of proposed converter versus output power are plotted as illustrated in Fig. 15 (a) for three operations where, in this figure the output power ranges in the boost operation are as $0<P_{H1}<250\,W$ and $0<P_{H2}<150\,W$. Moreover, in Fig. 15 (b), the output powers ranges for buck operation are as $0<P_{\ell}<250\,W$ and $0<P_{H2}<150\,W$. Furthermore, in Fig. 15 (c), the output power ranges for buck-and-boost operation are considered as $0<P_{\ell}<250\,W$ and $0<P_{H1}<150\,W$. The experimental prototype of the converter is shown in Fig. 15 (b).

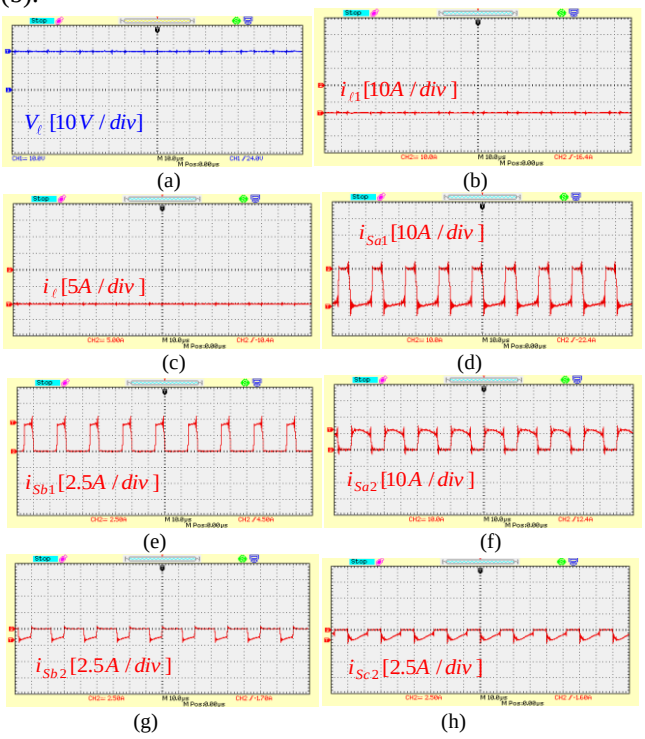

Fig. 13. Experimental results for buck operation.

VI. Conclusion

In this paper, a three-port DC-DC converter with three functions and high voltage conversion ratios was proposed. The proposed converter can be applied for supplying loads such as batteries, automobile headlamps, uninterruptible power supplies (UPS), DC motor drives, green houses, etc. Also, it can be an interface of inverters to supply ac loads. The proposed converter has the merit of achieving the zero-input current ripple at the low voltage side for the whole range of operating duty cycles comparing to the other recently single input/two output converters. The ratio of total voltage gain over the total component number in the proposed converter is higher than the other recently presented converters. The zero-input current ripple capability makes the proposed converter applicable in renewable energy conversion units. In this study, the converter is analyzed theoretically for a switching period and the analysis are confirmed by the experimental results for a prototype with specifications of 24V/304V, 240V and 400W.

TABLE V Calculated Theoretical Values for Buck Operation

First stage's voltages	$V_{\ell}=24\,V$, $V_{Sa1}=80\,V$ $during\,(1-D_1)T_s$, $V_{Sb1}=400\,V$ $during\,D_1T_s$
First stage's currents ($I_{\ell 1}$, I_{Lm1} , $-I_{H1}$)	$-I_{\ell}=-V_{\ell}/R_{\ell}=10.43\,A$, $I_{H1}=P_{H1}/V_{H1}=1.31\,A$, $I_{Lm1}=-21.98\,A$, $I_{\ell 1}=-16.59\,A$ $I_{Sa1}=I_{Lm1}=-21.98\,A$ $during\,D_1T_s$ $I_{Sb1}=-I_{Lm1}/(1+n_{s1})=4.4\,A$ $during\,(1-D_1)T_s$
Output power	$P_{\ell}=V_{\ell}^{\,2}/R_{\ell}=250W$

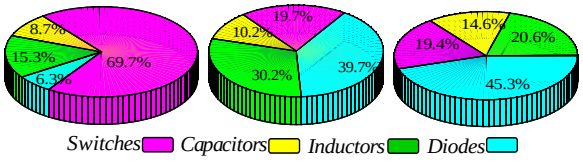

Fig. 14 Power loss distribution with for $P_{oT}=400\,W$; (a) boost operation; (b) buck operation; (c) buck-and-boost operation.

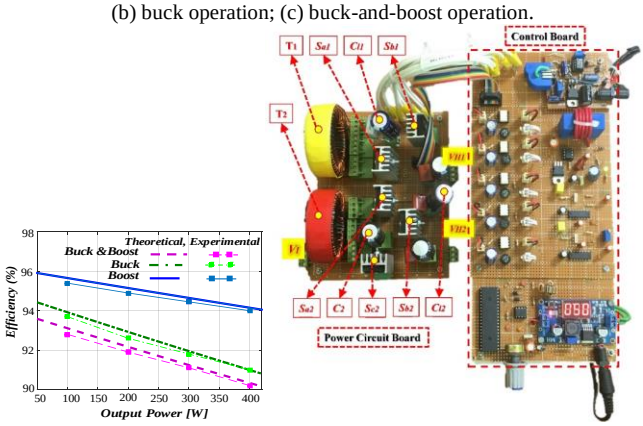

Fig. 15. Experimental and theoretical efficiency of proposed converter versus output power and implemented prototype of the proposed converter; (a) efficiency; (b) implemented prototype.

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