Investigation of Switching Oscillations for Silicon Carbide MOSFETs in Three-Level Active Neutral-Point-Clamped Inverters

Chen, Mengxing; Pan, Donghua; Wang, Huai; Wang, Xiongfei; Blaabjerg, Frede

Published in:
IEEE Journal of Emerging and Selected Topics in Power Electronics

DOI (link to publication from Publisher):
10.1109/JESTPE.2020.3014742

Publication date:
2020

Document Version
Accepted author manuscript, peer reviewed version

Investigation of Switching Oscillations for Silicon Carbide MOSFETs in Three-Level Active Neutral-Point-Clamped Inverters

Mengxing Chen, *Student Member, IEEE,* Donghua Pan, *Member, IEEE,* Huai Wang, *Senior Member, IEEE,* Xiongfei Wang, *Senior Member, IEEE,* and Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—This paper investigates the multi-frequency switching oscillations of silicon carbide (SiC) MOSFETs in three-level active neutral-point-clamped (3L-ANPC) inverters under three typical commutation modes (i.e., the full mode, outer mode, and inner mode). Multiple switching-oscillation components with various frequencies are identified theoretically for both the full-mode and outer-mode commutations, due to their switching-loop diversities. Oppositely, the inner mode exhibits a single oscillation component as only one switching loop is involved. Three types of double-pulse tests (DPTs) are conducted on a 3L-ANPC inverter demonstrator with SiC MOSFETs, and the switching-oscillation components are extracted accordingly, which match well with the theoretical derivations. Moreover, other switching characteristics closely related, i.e., the oscillation peaks, current overshoots, capacitive charges, and switching energies, are studied and benchmarked according to the DPT results. It is concluded that the full-mode and outer-mode commutations share similarities in terms of switching oscillations, current overshoots, capacitive charges, and turn-on energies. The theoretical findings from this work provide a comprehensive knowledge of the multi-frequency oscillation mechanisms associated with fast-switched 3L-ANPC inverters. Accordingly, the critical parasitic-components are identified, and specific design considerations are proposed to achieve switching-performance improvements.**

***Index Terms*—Active neutral-point-clamped (ANPC) inverter, double pulse test (DPT), multi-frequency switching oscillation, silicon carbide (SiC) MOSFET, switching loops.**

I. Introduction

OVER the past decade, the evolution of power electronic converter has been extensively driven by semiconductor devices manufactured by wide bandgap (WBG) materials [1]–[3], i.e., the gallium nitride (GaN) and silicon carbide (SiC) [4]. One of the most popular WBG devices is the SiC MOSFET, as it nicely fits into the need of 1.2–3.3 kV blocking voltage in numerous applications, e.g., grid-connected inverters [5], uninterruptible power supplies [6], [7], railway traction converters [8], and electric vehicles [9], [10].

As a WBG device, the SiC MOSFET features several superiorities in comparison with the silicon (Si) IGBT, e.g., high-temperature operation capability [4], enhanced electric field [11], and compact die area. More importantly, the faster switching speed, as well as the strengthened dv/dt and di/dt capabilities, are achievable by using the SiC MOSFET [3]. However, the increasing switching speed poses new challenges from the following perspectives: a) the robustness margin shall be ensured in terms of the overvoltage and gate-oxide failures [12]; b) the electro-magnetic interference (EMI) filters should be properly sized and optimized to cope with more switching noises [7], [13]; c) the circuit layout becomes more critical in order to fully utilize the switching capabilities of SiC MOSFETs. Hence, the switching characterization becomes essential for the performance evolution and design iteration of the SiC MOSFET based power electronic converters.

The switching behaviors of SiC MOSFETs in discrete-devices and half-bridge circuits have been intensively discussed in prior-art [14]–[22]. The experimental methodologies for switching characterization of SiC MOSFET were introduced in [14], [15]. The switching performance of a discrete SiC MOSFET was evaluated in [16], and these SiC switching characteristics in half-bridge circuits were assessed in [17]–[19]. Furthermore, theoretical models have been developed for the switching-behavior predictions [20]–[22]. A loss model of SiC MOSFET was proposed in [20] for high-frequency applications. The switching oscillation of SiC MOSFET was modeled and analyzed in [21], [22]. Nevertheless, the above-mentioned studies focus on discrete-devices or half-bridge circuits, and their conclusions may not be directly applicable to three-level (3L) converters. The line-frequency devices in 3L converters can introduce extra switching loops, which may affect switching behaviors such as commutation losses, device stresses, and switching oscillations.

In recent years, the three-level active neutral-point-clamped (3L-ANPC) inverter has become an active and important research topic, as it can actively re-shape the loss and thermal distributions among power semiconductors by manipulating ANPC commutation modes [23]–[27]. Three typical commutation modes (i.e., the full mode, outer mode, and inner mode) for the 3L-ANPC inverter were first introduced in [24]. The conventional switching loops and switching behaviors associated with the three commutation modes were studied in [26], [27], which were based on a Si-IGBT switched 3L-ANPC inverter. Recently, the applications of SiC MOSFETs in 3L-ANPC inverters have been reported in literatures with performance improvements [28]–[34], and more characteristics

Manuscript received April 13, 2020; revised June 25, 2020; accepted August 1, 2020. This work is supported by Innovation Fund Denmark under Grant 5185-00006B (HER-SiC). This paper was presented in part at the IEEE 10th International Conference on Power Electronics–ECCE Asia (ICPE 2019–ECCE Asia), Busan, Korea, May 27–30, 2019. (Corresponding author: Mengxing Chen)

The authors are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: mec@et.aau.dk; pan.dh@outlook.com; hwa@et.aau.dk; xwa@et.aau.dk; fbl@et.aau.dk).

regarding the switching behavior of SiC MOSFETs were explored in [35]–[39]. Specifically, the extra junction capacitance and the secondary switching loop introduced by line-frequency devices in 3L-ANPC inverters were identified in [36] under both the outer and inner commutations. Due to the multiple switching loops and high dv/dt and di/dt, the commutation of SiC MOSFET in 3L-ANPC inverters introduces multiple switching-oscillation components, which engender voltage overshoots during switching transients. Additionally, these oscillation components with different frequencies can significantly deteriorate the EMI performance.

In literature [37], the multi-switching loop induced over-voltage issues on line-frequency switches (under both the outer and inner commutations) were introduced. Furthermore, an analytical model for these multi-switching loop induced voltage overshoots in 3L-ANPC inverters was established in [38], which focuses on the outer-mode commutation. To reduce these risky voltage overshoots, a layout-optimized busbar design and a control method were proposed in [39] and [40], respectively. However, the aforementioned studies did not provide knowledge regarding the multi-frequency switching oscillations associated with the 3L-ANPC inverter. References [36]–[40] concentrate on the over-voltage amplitudes of switches and their mitigation methods, while the investigation of switching oscillations from a frequency perspective is still missing. Moreover, as the distributions of these oscillation frequencies are intensively dependent on the commutation modes, a comprehensive understanding of the multi-frequency mechanisms is highly demanded for a reliable and low-EMI operation of the 3L-ANPC inverter with SiC MOSFETs.

The key contribution of this paper focuses on studying the multi-frequency switching oscillations of SiC MOSFETs under the three representative ANPC commutation modes. A SiC MOSFET module and a 3L-ANPC inverter phase-leg are introduced in Section II. A simplified parasitic model of the 3L-ANPC phase-leg is developed based on finite-element method (FEM) simulations. Then, the three 3L-ANPC commutation modes and their equivalent switching circuits are discussed in Section III, and multiple switching-oscillation components are identified accordingly. Specific double pulse test (DPT) configurations are discussed in Section IV, and the DPT waveforms under the three commutation modes are presented. Then, the switching-oscillation components extracted from DPT waveforms, i.e., the experimental frequency-spectrum, are discussed in Section V, and the theoretical derivations of switching oscillations are validated under each 3L-ANPC commutation mode. Other switching characteristics closely related, i.e., oscillation peaks, current overshoots, capacitive charges, and switching energies, are studied and benchmarked in Section VI. Additionally, specific design considerations are proposed to achieve performance improvements. Finally, conclusions are drawn in Section VII.

II. Parasitic Model of 3L-ANPC Phase-Leg with SiC MOSFET Modules

A. SiC MOSFET Module

Contemporarily, the SiC MOSFET modules are under intensive development; however, the commercial SiC-based 3L-ANPC module is rarely available in the market. The half-bridge SiC module APTMC120AM55CT1AG from Microsemi is adopted as the building block of the 3L-ANPC phase-leg. The device is rated at 1200 V and 42 A [41]. As demonstrated in Fig. 1(a), the half-bridge module contains two pairs of SiC MOSFET die with the reverse SiC Schottky barrier diode (SBD) die, which are symbolized as the upper and lower MOS/SBDs in Fig. 1(b), respectively.

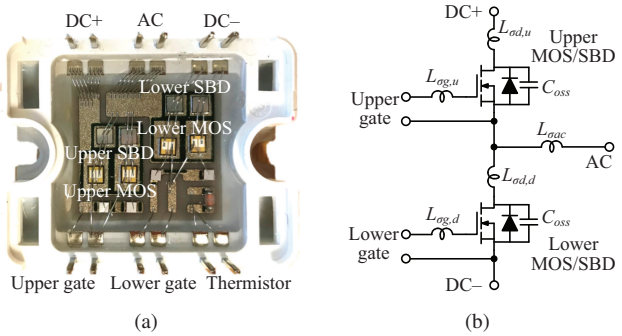


Fig. 1. Top view and circuit diagram of the SiC half-bridge module APTMC120AM55CT1AG from Microsemi. (a) Top view. (b) Module-level circuit diagram.

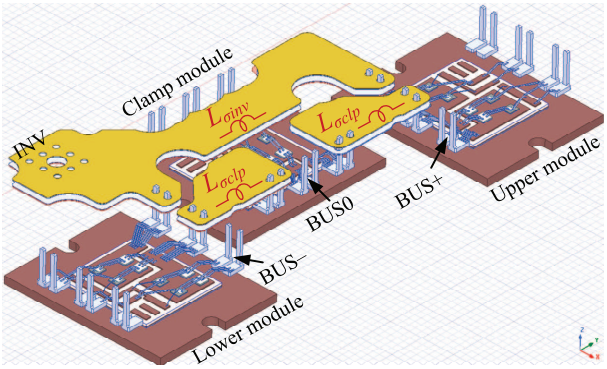
TABLE I
Extracted Parasitic Inductances and Resistances of the SiC Half Bridge Module. (Obtained at 1 MHz)

Category		Symbol	Inductance (nH)	Resistance (mΩ)
AC terminal		$L_{\sigma ac}$	6.0	1.0
Upper device	gate	$L_{\sigma g,u}$	9.4	6.5
	drain+source	$L_{\sigma d,u}$	10.0	3.7
Lower device	gate	$L_{\sigma g,d}$	12.0	8.7
	drain+source	$L_{\sigma d,d}$	12.9	3.8
PCB trace		$L_{\sigma clp}$	5.2	1.0
		$L_{\sigma inv}$	34.1	5.6
Busbar		$L_{\sigma bus}$	3.6	—

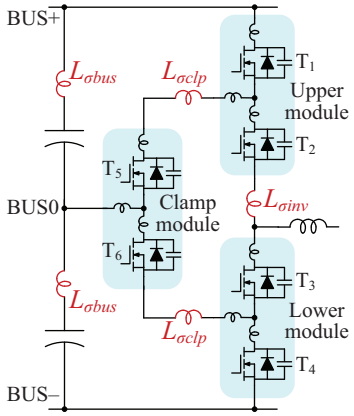
In order to interconnect the dies with the power terminals, bond wires and copper planes are applied in the SiC MOSFET module, which inevitably introduces parasitic inductances and alters the switching characteristics to some extent. FEM simulations (ANSYS/Q3D) are performed to extract the parasitic inductances of the half-bridge module. As illustrated in Fig. 1(b), $L_{\sigma g,x}$ (x = u or d) and $L_{\sigma ac}$ stand for the parasitic inductor located at the gate and ac terminals, respectively. The parasitic inductors introduced by drain and source connections are simplified as a single component $L_{\sigma d,x}$ (x = u or d). The inductance values joint with their series resistances measured at 1 MHz are summarized in Table I. Various inductance values are identified, and they are dependent on geometries of the conductors.

B. 3L-ANPC Phase-Leg

As shown in Figs. 2(a) and 2(b), the ANPC phase-leg is assembled by three aforementioned half-bridge modules, which are denoted as the upper module, clamp module, and lower module, respectively. Doing so, the ANPC phase-leg is capable



(a)



(b)

Fig. 2. Physical layout and simplified parasitic model of the 3L-ANPC phase-leg. (a) Physical layout. (b) Circuit diagram of the simplified parasitic model including parasitic inductances induced by both the module packaging and PCB traces.

of bearing a dc-bus voltage of 1500 V. A four-layer printed circuit board (PCB) is designed to interconnect the three half-bridge modules. It also introduces unavoidable routing inductances to the switching loop, although special efforts have been taken to minimize the loop areas.

The variables of $L_{\sigma clp}$ and $L_{\sigma inv}$ represent the PCB routing inductances of the neutral-tap connection and ac output connection, respectively. These PCB induced parameters are also obtained by FEM simulations, which are illustrated in Table I. It is noted that the neutral-tap inductance $L_{\sigma clp}$ (5.2 nH) is comparable with the ones caused by the module packaging, while the inductance $L_{\sigma inv}$ (34.1 nH) is relatively higher due to its unique geometry.

C. PCB Busbar and Hybrid Capacitor Bank

The dc rails of the 3L-ANPC phase-leg, i.e., BUS+, BUS0, and BUS–, are connected to the top layer, the dual-mid layers, and the bottom layer of the four-layer PCB busbar, respectively. Moreover, a 1500-V hybrid capacitor bank with both aluminum electrolytic capacitors (Al-Caps) and metalized polypropylene film capacitors (MPPF-Caps) is implemented [42].

It is noted that the capacitor's equivalent-series-inductance (ESL) and busbar routing inductance should also be counted into the switching loop. In order to minimize the routing inductance, the PCB layer stack is designed to have the maximum overlap, and the technique of magnetic-field cancellation is utilized for the capacitor-bank layout [43]. Furthermore, external snubber capacitors with superior high-frequency performance are embedded. Overall, the capacitor-bank ESL joint with the routing inductance is estimated to be 3.6 nH, which is simplified as the single busbar inductance $L_{\sigma bus}$.

TABLE II
SWITCHING STATES OF THE 3L-ANPC PHASE-LEG [24].

States	T_1	T_2	T_3	T_4	T_5	T_6
–	0	0	1	1	1	0
0L2	0	0	1	0	0	1
0L1	1	0	1	0	0	1
0F	0	1	1	0	1	1
0U1	0	1	0	1	1	0
0U2	0	1	0	0	1	0
+	1	1	0	0	0	1

III. INVESTIGATIONS OF SWITCHING OSCILLATIONS OF THE 3L-ANPC PHASE-LEG

In this section, the switching oscillations of the 3L-ANPC phase-leg under the full-mode, outer-mode, and inner-mode commutations are investigated. The 3L-ANPC switching states will be introduced first, as listed in Table II [24].

During the "–" state, both switches T_3 and T_4 are turned on to conduct the load current to the negative bus rail. Meanwhile, the switch T_5 is turned on to equalize the voltage stress between switches T_1 and T_2. Analogously, during the "+" state T_1 and T_2 conduct the load current to the positive bus rail, and switch T_6 is utilized to equalize the voltage stress between T_3 and T_4. Besides, by turning on T_3 and T_6, the load current is conducted through the lower neutral path in both directions; meanwhile, T_1 can be in either OFF or ON state, resulting in two switching states "0L2" and "0L1", respectively. Similarly, the load current is conducted through the upper path of the neutral path if both T_2 and T_5 are turned on, and T_4 can be in either OFF or ON state, which determines the two switching states "0U2" and "0U1", respectively. In order to diminish the conduction loss, the load current can also conduct through both the upper and lower paths of the neutral tap by turning on T_2, T_3, T_5, and T_6 simultaneously. This pattern is noted as the full-clamping state "0F".

Therefore, multiple possibilities of commutations could happen between one of the active states ("–" and "+") and one of the clamping states ("0L2", "0L1", "0U1", "0U2", and "0F"), which leads to several different 3L-ANPC commutation modes. Without losing its generality, the switching-oscillation mechanisms of three representative commutation modes, i.e., the full mode, outer mode, and inner mode, will be illustrated in the following sub-sections.

A. Full-Mode Commutation ("– ↔ 0F" and "+ ↔ 0F")

The full-mode commutation was first indicated in [24], and further studied in [27], [28]. Transitions "– ↔ 0F" and

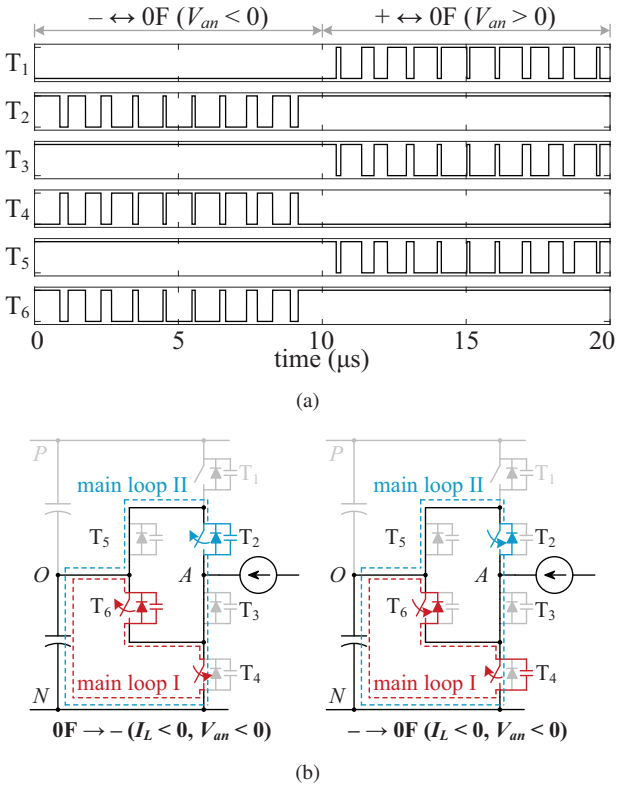


Fig. 3. Full-mode commutation of the 3L-ANPC phase-leg. (a) Gating signals. (b) Circuit diagrams during transitions "0F → –" and "– → 0F".

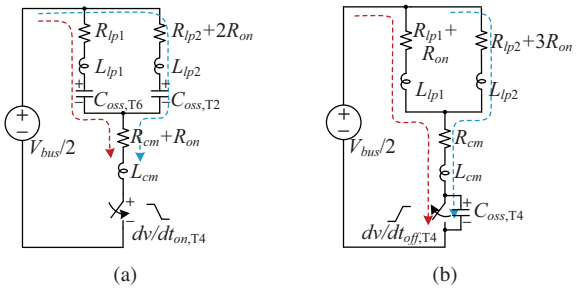


Fig. 4. Equivalent switching circuits of the full-mode commutation. (a) Equivalent switching circuit during transition "0F → –". (b) Equivalent switching circuit during transition "– → 0F".

TABLE III
SWITCHING-LOOP ASSOCIATED PARASITIC PARAMETERS EXTRACTED FROM ANSYS/Q3D.

Symbol	Inductance (nH)	Resistance (mΩ)	Capacitance (pF)
L_{lp1}, R_{lp1}	24.1	5.8	–
L_{lp2}, R_{lp2}	78.2	18.8	–
L_{lp3}, R_{lp3}	40.8	10.4	–
L_{cm}, R_{cm}	22.5	4.8	–
R_{on}	–	49	–
$C_{oss,Tx}$ (x = 1–6)	–	–	270 @ 500 V

"+ ↔ 0F" are achieved during the negative and positive cycles, respectively. Both the upper and lower paths of the neutral tap conduct during the clamping state "0F", which is accomplished by turning on switches T_2, T_3, T_5, and T_6 simultaneously. The gating signals and circuit diagrams of the full-mode commutation are depicted in Figs. 3(a) and 3(b) respectively. For simplification, only the operating principle during the negative cycle is elaborated. As demonstrated in Fig. 3(a), the outer switch T_4 is switched to be sinusoidal during the negative cycle. Meantime, T_2 and T_6 share identical switching signals, which operate complementarily with T_4. The load current commutates between the active phase arm and both the upper and lower neutral paths. As a result, the full-mode commutation involves dual switching loops, as they are indicated as the main loop I and main loop II in Fig. 3(b).

The equivalent switching circuits for transitions "0F → –" and "– → 0F" are illustrated in Figs. 4(a) and 4(b), respectively. L_{lpx} and R_{lpx} (x = 1 or 2) denote the inductance and resistance of the switching loop x. Additionally, L_{cm} and R_{cm} are the common inductance and resistance shared by the main loops I and II, and R_{on} denotes the on-state resistance of the SiC MOSFET. These parameters are listed in Table III, which are obtained according to the parasitic model studied in Section II. It is noted that the loop inductance and resistance of loop II (i.e., L_{lp2} and R_{lp2}) are significantly larger than these of the loop I (i.e., L_{lp1} and R_{lp1}) owing to the difference in loop length.

During the turn-on transient of T_4 (i.e., the transition "0F → –"), the output capacitors of T_6 and T_2 are charged through loops I and II, respectively, as it is illustrated in Fig. 4(a). Therefore, the capacitive current flowing through T_4 contains both these through $C_{oss,T6}$ and $C_{oss,T2}$. Moreover, a dual-frequency oscillation shall be incurred due to the multiple switching loops. The impedance curve of the equivalent switching circuit during the transition "0F → –" is exhibited in Fig. 5(a). Two oscillation frequencies of 29.4 MHz and 49.4 MHz can be identified, which are dominated by loop II and loop I, respectively. Theoretically, the two oscillation frequencies of $f_{osc1}^{0F\to-}$ and $f_{osc2}^{0F\to-}$ can be obtained by letting the imaginary part of the total impedance to be zero:

$$f_{osc1,osc2}^{0F\to-} = \frac{1}{2\pi}\cdot\sqrt{\frac{L_{lp1}+L_{lp2}+2L_{cm}\pm\sqrt{(L_{lp1}-L_{lp2})^2+(2L_{cm})^2}}{2C_{oss}\cdot(L_{lp1}L_{lp2}+L_{lp1}L_{cm}+L_{lp2}L_{cm})}} \quad (1)$$

where C_{oss} denotes the device output capacitance with drain-source voltage being 500 V, which equals to 270 pF in this work.

During the turn-off transient of T_4 (i.e., the transition "– → 0F"), the output capacitance of T_4 (i.e., $C_{oss,T4}$) is charged by one part of the load current, while both $C_{oss,T2}$ and $C_{oss,T6}$ are discharged through the other part of load current, simultaneously. After the drain-source voltage of T_4 reaches V_{bus}/2 and the phase current is fully transferred to T_2 and T_6, the switching oscillation is initiated through the parallel path formed by loops I and II, as it is illustrated in Fig. 4(b). The single oscillation frequency of 47.9 MHz can be identified from Fig. 5(b). The oscillation frequency of $f_{osc}^{-\to0F}$ can also

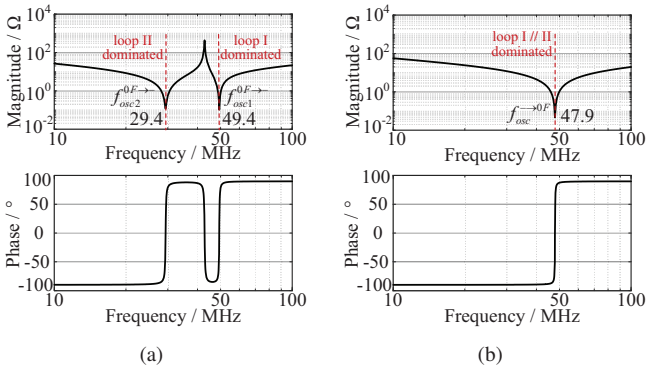


Fig. 5. Circuit impedance analysis of the full-mode equivalent switching circuit. (a) Magnitude and phase during transition "0F → –". (b) Magnitude and phase during transition "– → 0F".

be derived by:

$$f_{osc}^{-\to 0F} = \frac{1}{2\pi \cdot \sqrt{L_{tot}^{-\to 0F} \cdot C_{oss}}} \tag{2}$$

$$L_{tot}^{-\to 0F} = \frac{L_{lp1} L_{lp2}}{L_{lp1} + L_{lp2}} + L_{cm} \tag{3}$$

where $L_{tot}^{-\to 0F}$ denotes the total loop inductance in equivalence during the transition "– → 0F", which counts to be 40.9 nH. It is regarded that the components of L_{lp1} and L_{lp2} are in parallel during the T_4's turn-off oscillation period. Hence, a reduced voltage stress can be expected on switch T_4.

B. Outer-Mode Commutation ("– ↔ 0L2" and "+ ↔ 0U2")

The outer-mode commutation consists of transitions "– ↔ 0L2" and "+ ↔ 0U2" during the negative ($V_{an} < 0$) and positive cycles ($V_{an} > 0$), respectively. The gating signals and circuit diagrams are illustrated in Figs. 6(a) and 6(b), respectively. During the negative cycle, the outer switch T_4 is modulated to be sinusoidal, while the clamping switch T_6 operates complementarily. Simultaneously, the other clamping device T_5 switches identically with T_4 to equalize the voltage stresses between the non-active switches T_1 and T_2. Turning T_5 off during the "–" state also serves to ensure that the phase current will not commutate through the non-neighboring neutral path, i.e., the upper neutral-path enclosing T_5. Therefore, the load current only commutates between the active phase-arm and its neighboring neutral path, and the main loop I is identified as the major switching loop, which is depicted as the red dashed line in Fig. 6(b). Moreover, the outer mode exhibits two capacitive loops, i.e., the capacitive (capaci.) loop II (or II') and capaci. loop III in Fig. 6(b). Although these capacitive loops do not carry load current, they can also create additional switching-oscillation components.

This can be explained from the equivalent switching circuit of "0L2 → –" (the turn-on transient of T_4) as it is demonstrated in Fig. 7(a). L_{lp3} and R_{lp3} are the parasitic inductance and resistance of the capacitive loop III. The equivalent switching circuit of "0L2 → –" resembles that of the full-mode commutation "0F → –". The output capacitors

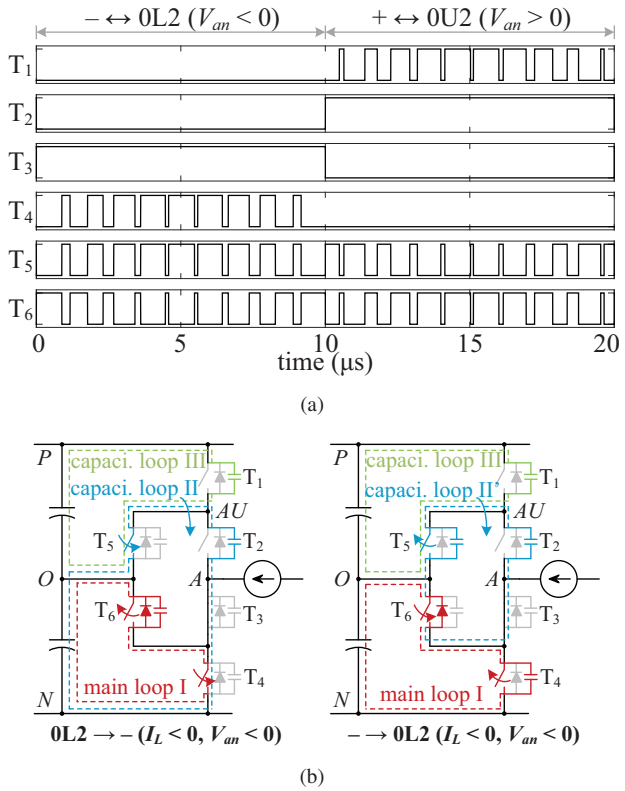


Fig. 6. Outer-mode commutation of the 3L-ANPC phase-leg. (a) Gating signals. (b) Circuit diagrams during transitions "0L2 → –" and "– → 0L2".

of T_6 and T_2, i.e., $C_{oss,T6}$ and $C_{oss,T2}$, are charged through the main loop I and capaci. loop II simultaneously, although T_2 carries no load current during the outer-mode commutation. The output capacitor of T_1 (i.e., $C_{oss,T1}$) will be charged till $V_{ds,T1} = V_{bus}/2$ when T_5 is switched on, which creates the capacitive loop III. Nevertheless, the existence of loop III will not affect the switching characteristics of other devices, since loop III is self-closed, and the potential of node *AU* [see Fig. 7(a)] remains constant as $V_{bus}/2$ once T_5 is turned on. As it is given in Fig. 8(a), the impedance feature of the switching circuit during "0L2 → –" is identical to that during "0F → –", and the two oscillation frequencies of $f_{osc1}^{0L2\to-}$ = 29.4 MHz and $f_{osc2}^{0L2\to-}$ = 49.4 MHz can be obtained by:

$$f_{osc1,osc2}^{0L2\to-} = f_{osc1,osc2}^{0F\to-} = \frac{1}{2\pi} \cdot \sqrt{\frac{L_{lp1} + L_{lp2} + 2L_{cm} \pm \sqrt{(L_{lp1} - L_{lp2})^2 + (2L_{cm})^2}}{2C_{oss} \cdot (L_{lp1}L_{lp2} + L_{lp1}L_{cm} + L_{lp2}L_{cm})}} \tag{4}$$

The equivalent switching circuit of transition "– → 0L2" (the turn-off transient of T_4) is demonstrated in Fig. 7(b). As $C_{oss,T4}$ is charged by the load current and starts to block the dc voltage of $V_{bus}/2$, the potential of node *AU* becomes higher than $V_{bus}/2$ (equals to $V_{bus}/2 + V_{ds,T2}$ in respect to BUS–). This is followed by a capacitive discharge of $C_{oss,T2}$ and $C_{oss,T1}$ through capacitive loops II' and III respectively, which will be terminated until the steady state "0L2" is reached with:

$$V_{ds,T2}^{0L2} = V_{ds,T5}^{0L2} = V_{bus}/2 - V_{ds,T1}^{0L2}. \tag{5}$$

It is noted that the output capacitance values of T_1, T_2, and T_5 during the state "0L2" can be greater than C_{oss} = 270 pF, as their drain-source voltages (i.e., $V_{ds,T1}^{0L2}$, $V_{ds,T2}^{0L2}$, and $V_{ds,T5}^{0L2}$) are lower than V_{bus}/2.

A full derivation of the circuit impedance for "– → 0L2" is given in (6), where the inductance of loop III is also considered. However, letting the imaginary part of $Z_{detail}^{-\rightarrow 0L2}$ to be zero will engender a high-order equation (greater than second order), which makes the analytical solution unsolvable. Therefore, a simplification is made by omitting L_{lp3} and R_{lp3}, so that $C_{oss,T1}$ can be assumed to be in parallel with $C_{oss,T5}$. The circuit impedance after the simplification can be re-written as (7). Then, the dual oscillation frequencies can be derived as (8), where

$$k_c = \frac{C_{oss,T1} + C_{oss,T5}}{C_{oss,T1} + C_{oss,T2} + C_{oss,T5}} \tag{9}$$

$$L_{mix} = \sqrt{L_{lp1}L_{lp2} + L_{lp1}L_{cm} + L_{lp2}L_{cm}} \tag{10}$$

$$C_{oss,T4} = C_{oss}. \tag{11}$$

In (8)-(10), the output capacitances of T_1, T_2, and T_5 are separately modeled, as they can be dependent on the C_{oss}-V_{ds} characteristics, charging currents, and timing during the "– → 0L2" transient. This C_{oss} difference among T_1, T_2, and T_5 can slightly shift the oscillation frequencies to lower levels. Nevertheless, deriving the accurate V_{ds} and C_{oss} distributions among T_1, T_2, and T_5 requires further deep and sensitive studies. To simplify, an approximation can be made by assuming $C_{oss,T1}$ = $C_{oss,T2}$ = $C_{oss,T5}$ = C_{oss}. Thereafter, the impedance comparison between $Z_{detail}^{-\rightarrow 0L2}$ (full derivation) and $Z_{simp}^{-\rightarrow 0L2}$ (simplified derivation) are exhibited in Fig. 8(b), where $Z_{detail}^{-\rightarrow 0L2}$ and $Z_{simp}^{-\rightarrow 0L2}$ are represented by the dotted and solid curves, respectively. It can be concluded that the simplified derivation is able to characterize the dual oscillation components at 33.6 and 50.9 MHz with satisfactory accuracy, which can also be calculated from (8)-(11). Although the oscillation component at 97.5 MHz is omitted by the simplification (see the impedance curves of $Z_{detail}^{-\rightarrow 0L2}$ and $Z_{simp}^{-\rightarrow 0L2}$), its resonance energy can be significantly attenuated by the loop resistance at this high-frequency range.

C. Inner-Mode Commutation ("– ↔ 0U1" and "+ ↔ 0L1")

The inner mode involves transitions of "– ↔ 0U1" and "+ ↔ 0L1" during the negative and positive cycles, respectively. The gating signals and circuit diagrams of inner-mode commutation are depicted in Figs. 9(a) and 9(b), respectively. The inner mode only operates the switches T_2 and T_3 to be sinusoidal, while other devices conduct per half line-cycle. Then the load current only commutates between the active phase-arm and its non-neighboring neutral path. It can be concluded that only a single switching loop, i.e., the main loop II, is involved during the inner-mode commutation, and no capacitive loop exists as potentials of non-active devices are naturally clamped to dc-bus rails (either P, O, or N).

The equivalent switching circuits for transitions "0U1 → –" (the turn-on transient of T_3) and "– → 0U1" (the turn-off transient of T_3) are depicted in Figs. 10(a) and 10(b), respectively, which are identical except for the junction output capacitor involved (either $C_{oss,T2}$ or $C_{oss,T3}$). An impedance analysis of the inner-mode switching circuit for both transitions "0U1 → –" and "– → 0U1" is depicted in Fig. 11. A single oscillation frequency of $f_{osc}^{-\leftrightarrow 0U1}$ = 30.5 MHz is identified, which can be obtained by:

$$f_{osc}^{-\leftrightarrow 0U1} = \frac{1}{2\pi \cdot \sqrt{L_{tot}^{-\leftrightarrow 0U1} \cdot C_{oss}}} \tag{12}$$

$$L_{tot}^{-\leftrightarrow 0U1} = L_{lp2} + L_{cm} \tag{13}$$

where $L_{tot}^{-\leftrightarrow 0U1}$ (= 100.7 nH) is the total loop inductance of both inner-mode transitions "0U1 → –" and "– → 0U1".

It is noted the inner mode features a single loop-inductance with a significant value, since its switching loop (i.e., the loop II) contains four switches and it is significantly longer than these of the full mode and outer mode. Moreover, the capacitive charge of inner mode can be notably relieved compared to other commutation modes, as only a single junction output capacitance is involved.

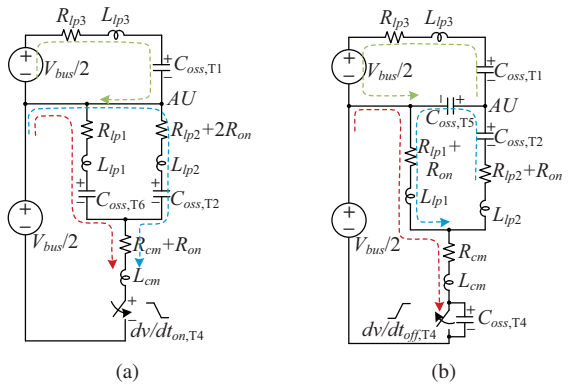
D. Summary

The switching loops and their associated oscillation frequencies under the three commutation modes are summarized in

$$Z_{detail}^{-\rightarrow 0L2} = \frac{1}{\frac{1}{\frac{1}{\frac{1}{j\omega C_{oss,T1}} + j\omega L_{lp3} + R_{lp3}} + j\omega C_{oss,T5}} + \frac{1}{j\omega C_{oss,T2}} + j\omega L_{lp2} + R_{lp2} + R_{on}} + \frac{1}{R_{lp1} + R_{on} + j\omega L_{lp1}} + R_{cm} + j\omega L_{cm} + \frac{1}{j\omega C_{oss,T4}} \tag{6}$$

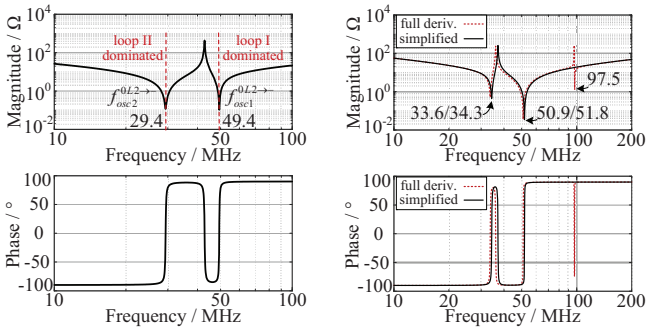
$$Z_{simp}^{-\rightarrow 0L2} = \frac{1}{\frac{1}{\frac{1}{j\omega(C_{oss,T1}+C_{oss,T5})} + \frac{1}{j\omega C_{oss,T2}} + j\omega L_{lp2} + R_{lp2} + R_{on}} + \frac{1}{R_{lp1} + R_{on} + j\omega L_{lp1}} + R_{cm} + j\omega L_{cm} + \frac{1}{j\omega C_{oss,T4}} \tag{7}$$

$$f_{osc1,osc2}^{-\rightarrow 0L2} = \frac{1}{2\pi} \cdot \sqrt{\frac{\frac{L_{lp1}+L_{cm}}{C_{oss,T2}} + \frac{k_c(L_{lp1}+L_{lp2})}{C_{oss,T4}} \pm \sqrt{(\frac{L_{lp1}+L_{cm}}{C_{oss,T2}})^2 + (\frac{k_c(L_{lp1}+L_{lp2})}{C_{oss,T4}})^2 + \frac{2k_c({L_{lp1}}^2 - {L_{mix}}^2)}{C_{oss,T2} \cdot C_{oss,T4}}}}{2k_c \cdot L_{mix}^2}} \tag{8}$$



(a) (b)

Fig. 7. Equivalent switching circuits of the outer-mode commutation. (a) Equivalent switching circuit during transition "0L2 → –". (b) Equivalent switching circuit during transition "– → 0L2".



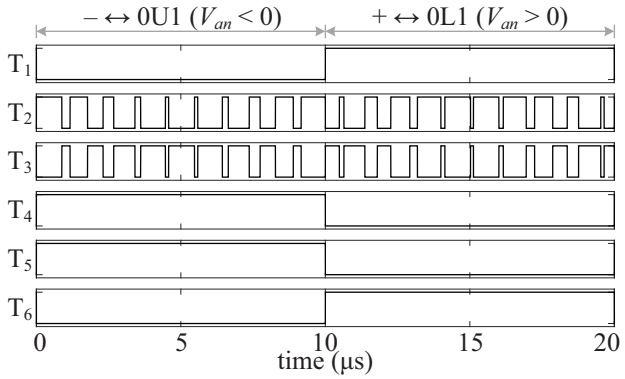
(a) (b)

Fig. 8. Circuit impedance analysis of the outer-mode equivalent switching circuit. (a) Magnitude and phase during transition "0L2 → –". (b) Magnitude and phase during transition "– → 0L2".

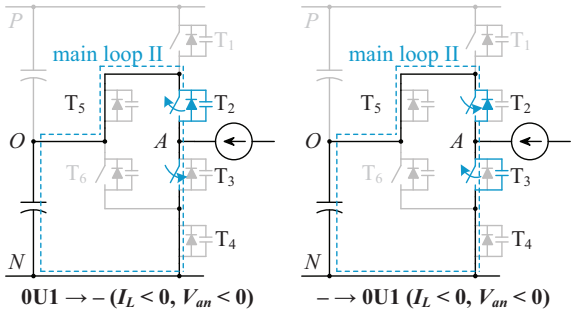
Table IV. It can be observed that the full-mode and outer-mode commutations feature homogeneous characteristics during the turn-on transient of T_4 (i.e., transitions of "0F → –" and "0L2 → –"), as dual oscillation frequencies of 29.4 MHz and 49.4 MHz can be derived. The "– → 0F" transient of the full-mode commutation (i.e., the turn-off transient of T_4) exhibits a single switching-oscillation at 47.9 MHz as loops I and II are regarded to be combined in parallel. Nevertheless, the transition "– → 0L2" of the outer-mode commutation is more complicated as it involves main loop I and capacitive loops II' and III. Three oscillation frequencies of 34.3 MHz, 51.8 MHz, and 97.5 MHz can be obtained based on the full derivation from (6). On the other hand, the inner mode features the most straightforward switching characteristic, as a single switching loop is concerned for both transients "0U1 → –" and "– → 0U1". A single oscillation component at 30.5 MHz is calculated accordingly.

IV. Experimental Assessments of Switching Characteristics for SiC MOSFETs in 3L-ANPC Inverters

In order to evaluate the switching oscillations and other switching characteristics of the SiC MOSFETs in the 3L-ANPC inverter, the standard DPTs are performed under the full-mode, outer-mode, and inner-mode commutations. In this section, the DPT setup is illustrated first, and the switching

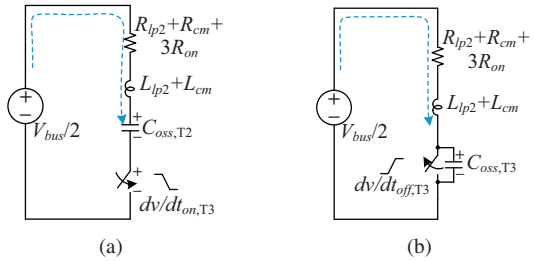


(a)



(b)

Fig. 9. Inner-mode commutation of the 3L-ANPC phase-leg. (a) Gating signals. (b) Circuit diagrams during transitions "0U1 → –" and "– → 0U1".



(a) (b)

Fig. 10. Equivalent switching circuits of the inner-mode commutation. (a) Equivalent switching circuit during transition "0U1 → –". (b) Equivalent switching circuit during transition "– → 0U1".

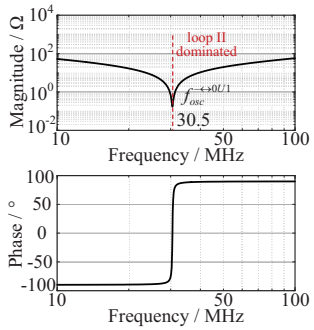


Fig. 11. Circuit impedance analysis of the inner-mode equivalent switching circuit during during transitions of "0U1 → –" and "– → 0U1".

TABLE IV
SUMMARY OF SWITCHING LOOPS AND OSCILLATION FREQUENCIES UNDER THE THREE 3L-ANPC COMMUTATION MODES.

Modes	Loops involved	Symbols	Oscillation frequencies
Full	Main I, II	$f_{osc1}^{0F\rightarrow -}$, $f_{osc2}^{0F\rightarrow -}$	29.4, 49.4 MHz
		$f_{osc}^{-\rightarrow 0F}$	47.9 MHz
Outer	Main I and capaci. II, III	$f_{osc1}^{0L2\rightarrow -}$, $f_{osc2}^{0L2\rightarrow -}$	29.4, 49.4 MHz
		$f_{osc1}^{-\rightarrow 0L2}$, $f_{osc2}^{-\rightarrow 0L2}$	34.3, 51.8 , 97.5 MHz
Inner	Main II	$f_{osc}^{-\leftrightarrow 0U1}$	30.5 MHz

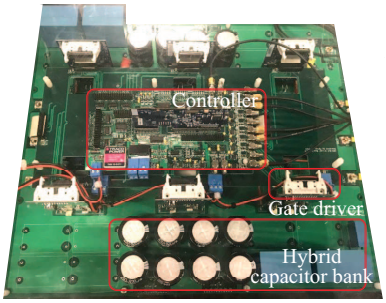


Fig. 12. Top view of a 1500-V SiC-based 3L-ANPC inverter demonstrator.

TABLE V
EQUIPMENT USED FOR DOUBLE PULSE TEST (DPT).

Category	Manufacturer	Model
DC source	Elektro-Automatik	PSI-800-3U-HS-PV
Load inductor	—	190 μH
Controller	Texas Instrument	TMS320F28379D
Gate driver	CREE/Wolfspeed	CGD15HB62P1
SiC module	Microsemi	APTMC120AM55CT1AG
Passive probe	Lecroy	PP019 and PPE 2kV
Differential probe	Tektronix	P5200A
Current transducer	PEM	CWTUM/6/R

waveforms of the three commutation modes are then exhibited.

A. DPT Setup

A 3L-ANPC inverter demonstrator is implemented as shown in Fig. 12 by adopting the structural design illustrated in Section II, which is tested as the DPT setup. A hybrid capacitor bank utilizing both Al-Caps and MPPF-Caps is also implemented. A four-layer laminated PCB integrates both the dc bus and the aforementioned ANPC phase-leg. The equipment used for DPT are listed in Table V. A 1500-V dc-source PSI-800-3U-HS-PV is applied to energize the dc bus (from BUS+ to BUS–). CREE's SiC MOSFET driver CGD15HB62P1 is used, and the fixed gate voltages of +20 V and –5 V are utilized. A 190 μH load inductor is implemented using 1.6 mm Litz wire and dual sendust powder cores.

The fundamental principles of the DPT can be seen in details in [44]. The BUS– rail and the oscilloscope are grounded, and only negative-cycle commutations "– ↔ 0F", "– ↔ 0L2", and "– ↔ 0U1" are tested as the representatives of the full-mode, outer-mode, the inner-mode commutations, respectively. Three different DPT configurations are implemented to simulate the switching behaviors of the three commutation modes under sinusoidal load currents, which are demonstrated in Figs. 13(a), 13(b), and 13(c), respectively. The gate-source and drain-source voltages of T_4 (i.e., $V_{gs,T4}$ and $V_{ds,T4}$) are measured using Lecroy's passive probes PP019 and PPE-2kV, respectively. Other voltage waveforms of $V_{gs,T3}$, $V_{ds,T2}$, $V_{ds,T3}$ and $V_{ds,T6}$ are captured by differential probes P5200A as they have floating potentials to the earth. The drain currents of switches T_3 and T_4 (i.e., $I_{d,T3}$ and $I_{d,T4}$) are measured using PEM's current transducers CWTUM/6/R.

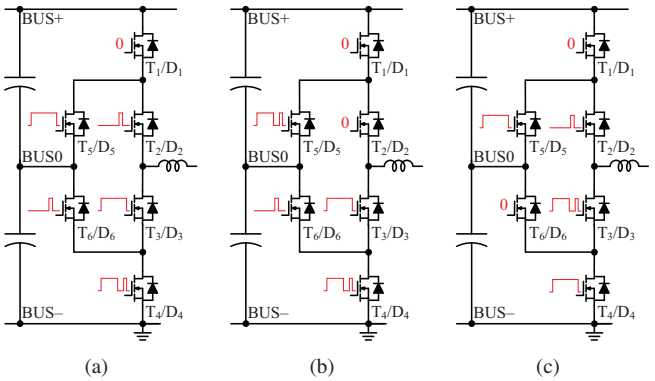


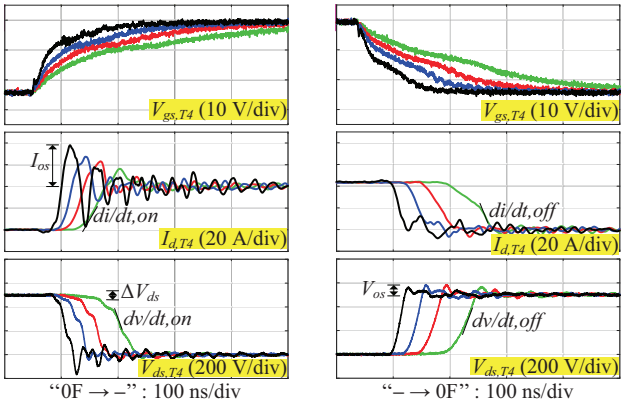
Fig. 13. Double-pulse configurations for the 3L-ANPC phase-leg under the three commutation modes. (a) The full mode "– ↔ 0F". (b) The outer mode "– ↔ 0L". (c) The inner mode "– ↔ 0U1".

B. Transient Switching Waveforms

Multiple DPTs are performed under the rated condition of V_{bus} = 1000 V and I_L = –40 A. An external capacitance $C_{gs,ext}$ = 3.3 nF is applied to the gate-source terminal of each SiC MOSFET to mitigate the cross-talking issue [45], [46]. Multiple external gate resistances (i.e., $R_{g,ext}$ = 5.5 Ω, 11 Ω, 16 Ω, and 25 Ω) are tested to evaluate the switching performances under switching-speed variations.

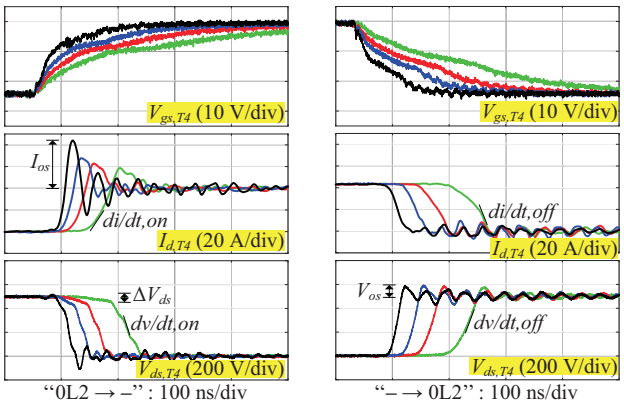
The transient switching waveforms of the gate-source voltage V_{gs}, the drain current I_d, and the drain-source voltage V_{ds}, of the active switch under the three commutation modes (i.e., T_4 for the full mode and outer mode, and T_3 for the inner mode) are captured and presented in Figs. 14, 15, and 16. The voltage and current waveforms captured under $R_{g,ext}$ = 5.5 Ω, 11 Ω, 16 Ω, and 25 Ω are depicted as curves in black, blue, red, and green, respectively. The slew rates of drain-source voltages (i.e., the dv/dt) are in the range from 37.0 V/ns to 10.9 V/ns, as the $R_{g,ext}$ varies from 5.5 Ω to 25 Ω. Concurrently, the slew rates of drain currents (i.e., the di/dt) are in the range from 4.3 A/ns to 1.0 A/ns.

In general, the voltage and current slew rates decrease with the increase of the external gate resistance, while the switching delay increases. Due to the high switching-speed of the SiC MOSFET, drain-current overshoots and oscillations are observed during the turn-on transients. Similarly, voltage overshoots with significant switching oscillations are exhibited during the turn-off transients. The detailed analysis and com-



(a) (b)

Fig. 14. Full-mode commutation waveforms under the conditions of V_{bus} = 1000 V, I_L = –40 A, $R_{g,ext}$ = 5.5 Ω, 11 Ω, 16 Ω, and 25 Ω, and $C_{gs,ext}$ = 3.3 nF. (a) Turn-on waveforms of $V_{gs,T4}$, $I_{d,T4}$, and $V_{ds,T4}$. (b) Turn-off waveforms of $V_{gs,T4}$, $I_{d,T4}$, and $V_{ds,T4}$.



(a) (b)

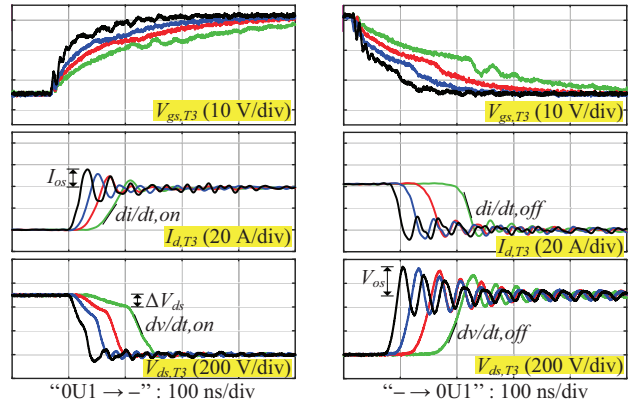
Fig. 15. Outer-mode commutation waveforms under the conditions of V_{bus} = 1000 V, I_L = –40 A, $R_{g,ext}$ = 5.5 Ω, 11 Ω, 16 Ω, and 25 Ω, and $C_{gs,ext}$ = 3.3 nF. (a) Turn-on waveforms of $V_{gs,T4}$, $I_{d,T4}$, and $V_{ds,T4}$. (b) Turn-off waveforms of $V_{gs,T4}$, $I_{d,T4}$, and $V_{ds,T4}$.

parison of switching oscillations and other characteristics will be discussed in the following sections.

V. Analysis of Experimental Results I: Switching Oscillations

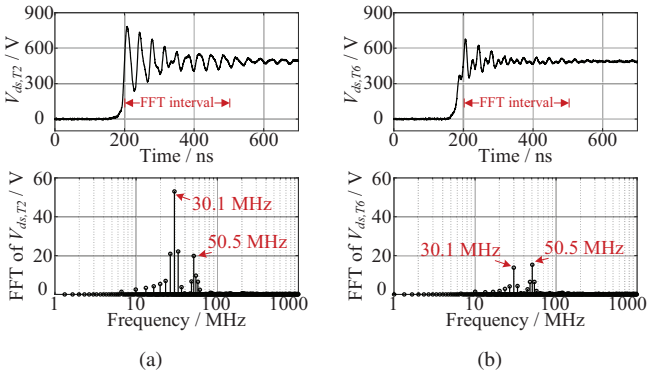
In this section, fast Fourier transform (FFT) analyses are conducted on the switching waveforms of drain-source voltages (i.e., $V_{ds,Tx}$, x = 2, 3, 4, and 6) under the DPT condition of V_{bus} = 1000 V, I_L = –40 A, $R_{g,ext}$ = 5.5 Ω, and $C_{gs,ext}$ = 3.3 nF. Subsequently, the equivalent switching circuits and switching oscillations studied in Section III are validated. The FFT results of $V_{ds,Tx}$ for the three commutation modes will be discussed respectively in the following sub-sections.

It should be pointed out that the drain-current measurements are not utilized to characterize the switching oscillations in this section, as the current transducer features a limited bandwidth of 30 MHz. Although the differential voltage probe P5200A features a bandwidth of 50 MHz, its frequency identifications



(a) (b)

Fig. 16. Inner-mode commutation waveforms under the conditions of V_{bus} = 1000 V, I_L = –40 A, $R_{g,ext}$ = 5.5 Ω, 11 Ω, 16 Ω, and 25 Ω, and $C_{gs,ext}$ = 3.3 nF. (a) Turn-on waveforms of $V_{gs,T3}$, $I_{d,T3}$, and $V_{ds,T3}$. (b) Turn-off waveforms of $V_{gs,T3}$, $I_{d,T3}$, and $V_{ds,T3}$.



(a) (b)

Fig. 17. Time-domain waveforms and frequency spectrums for the full-mode commutation "0F → –" under the DPT condition of V_{bus} = 1000 V, I_L = –40 A, $R_{g,ext}$ = 5.5 Ω, and $C_{g,ext}$ = 3.3 nF. (a) $V_{ds,T2}$ during "0F → –". (b) $V_{ds,T6}$ during "0F → –".

near 50 MHz are still valid, as the probe will not introduce a frequency shift to the measurements.

A. FFT Results of Full-Mode Commutation

For the "0F → –" transient of full-mode commutation, the switching waveforms of $V_{ds,T2}$ and $V_{ds,T6}$ are utilized for the FFT analysis. The frequency spectrums of $V_{ds,T2}$ and $V_{ds,T6}$ as well as time-domain waveforms are depicted in Figs. 17(a) and 17(b) respectively (as black solid lines). A 300-ns time interval is sampled for the FFT analysis, which starts from the instant that $V_{ds,T2}$ (or $V_{ds,T6}$) first crosses V_{bus}/2. A Hamming window function is used to prevent spectral leakages. To validate these voltage measurements by the differential probe P5200A, LTspice simulation results of $V_{ds,T2}$ and $V_{ds,T6}$ in both time- and frequency-domain are also exhibited in Fig. 17 (as red dashed lines). Simulation waveforms of both $V_{ds,T2}$ and $V_{ds,T6}$ can match with their experimental results, and identical oscillation components can be found from their frequency spectrums.

The measured oscillation frequencies and the errors versus their theoretical expectations are summarized in Table VI. It

TABLE VI
FFT RESULTS OF MEASURED DRAIN-SOURCE VOLTAGES UNDER THREE 3L-ANPC COMMUTATION TYPES.

Commutation types		V_{ds} studied	Oscillation frequencies	Theoretical errors
Full	"0F → –"	$V_{ds,T2}$	30.1 & 50.5 MHz	0.7 & 1.1 MHz
		$V_{ds,T6}$	30.1 & 50.5 MHz	0.7 & 1.1 MHz
	"– → 0F"	$V_{ds,T4}$	44.3 MHz	3.6 MHz
Outer	"0L2 → –"	$V_{ds,T6}$	29.9 & 49.9 MHz	0.5 MHz
	"– → 0L2"	$V_{ds,T4}$	32.8 & 52.4 MHz	1.5 & 0.6 MHz
Inner	"0U1 → –"	$V_{ds,T2}$	29.7 MHz	2.6 MHz
	"– → 0U1"	$V_{ds,T3}$	28.3 MHz	2.2 MHz

is observed that a single switch may have multiple oscillation components, although it is enclosed in a single loop. This phenomenon can be explained by the mutual-interference effect between loops. Specifically, dual oscillation frequencies of 30.1 and 50.5 MHz can be obtained from both $V_{ds,T2}$ and $V_{ds,T6}$. The theoretical expectations discussed in Section III (i.e., 29.4 and 49.4 MHz) deviate with these obtained by experiment by 0.7 and 1.1 MHz, respectively, which are induced by estimation errors on loop inductance and device output capacitance. Regarding oscillation magnitudes on $V_{ds,T2}$, the low-frequency oscillation (i.e., 30.1 MHz) is more significant than its high-frequency counterpart (i.e., 50.5 MHz). Since switch T_2 is enclosed by loop II, which features higher inductive energy (L_{lp2} = 78.2 nH) and dominates the low-frequency oscillation at 30.1 MHz. On the other hand, the magnitudes of high-frequency oscillations on $V_{ds,T6}$ are significantly reduced, as loop I (which encloses T_6) has less inductive energy (L_{lp1} = 24.1 nH). The low-frequency component exhibits comparable oscillation amplitude on $V_{ds,T6}$.

The frequency spectrum of $V_{ds,T4}$ and its time-domain waveform during the "– → 0F" transient are exhibited in Fig. 18. It can be observed that the oscillation amplitudes of $V_{ds,T4}$ (i.e., the voltage overshoot) may be neglected compared to these of $V_{ds,T2}$ and $V_{ds,T6}$ (during T_4's turn-on transient). As it is discussed in Section III-A, the inductance components of L_{lp1} and L_{lp2} can be regarded to be in parallel connection during T_4's turn-off transient. Due to this paralleling effect, The equivalent loop inductance during T_4's turn-off transient is significantly reduced, and lower oscillation amplitude shall be expected. On the other aspect, the drain-current di/dt during T_4's turn-on transient is greater than that during its turn-off transient, as one identical gate resistance $R_{g,ext}$ = 5.5 Ω is adopted for both the turn-on and turn-off intervals.

Three oscillation components are identified in Fig. 18 with oscillation frequencies of 34.9, 44.3, and 60.1 MHz. The theoretical derivation successfully predicts the middle oscillation frequency of 44.3 MHz with an error of 3.6 MHz (as noted in Table VI), while the oscillation components at 34.9 MHz and 60.1 MHz are omitted as they are engendered by the asymmetrical turn-on of SBDs of T_2 and T_6, which can not be characterized by the theoretical derivation. To elaborate this issue, Fig. 19 exhibits the simulated diode-forward-current I_f and drain-source-voltage V_{ds} waveforms of T_2 and T_6 during

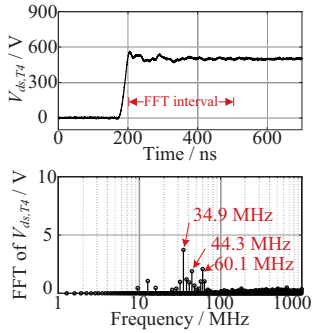


Fig. 18. Time-domain waveform and frequency spectrum of $V_{ds,T4}$ for the full-mode commutation "– → 0F" under the DPT condition of V_{bus} = 1000 V, I_L = –40 A, $R_{g,ext}$ = 5.5 Ω, and $C_{g,ext}$ = 3.3 nF.

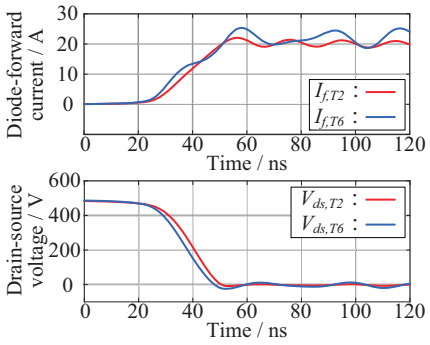


Fig. 19. The diode-forward currents I_f and drain-source voltages V_{ds} of T_2 and T_6 during the full-mode transition "– → 0F".

the full-mode transition "– → 0F". Due to the more significant inductance of loop II (i.e., $L_{lp2} > L_{lp1}$), the turn-on operation of T_2's SBD is delayed compared with that of T_6's SBD during the interval of 20–60 ns. Furthermore, $I_{f,T6}$ exhibits a higher di/dt than $I_{f,T2}$ during the simulation interval of 20–40 ns, and it starts to oscillate before the complete conduction of T_2's SBD. In such circumstance, other unexpected oscillation components can be activated.

B. FFT Results of Outer-Mode Commutation

The spectrum of $V_{ds,T6}$ during the transient "0L2 → –" is depicted in Fig. 20(a). As the equivalent switching circuit of outer-commutation "0L2 → –" resembles that of the full-commutation "0F → –", the frequency spectrum of $V_{ds,T6}$ during "0L2 → –" exhibits analogous oscillation frequencies (i.e., 29.9 and 49.9 MHz) and magnitudes as these of $V_{ds,T6}$ during "0F → –". A frequency error of 0.5 MHz is observed between the experimental analyses and theoretical expectations.

Regarding the "– → 0L2" transient, the frequency spectrum of $V_{ds,T4}$ is different from that during the "– → 0F" transient, as it is depicted in Fig. 20(b). Dual oscillation frequencies of 32.8 and 52.4 MHz can be identified accordingly. Besides, the voltage oscillation magnitudes become more significant than these during "– → 0F", especially the low-frequency one at 32.8 MHz. The oscillation component at 97.5 MHz is missing from the frequency spectrum of $V_{ds,T4}$, as its resonance energy is limited and can be significantly attenuated by the loop resistance at this high-frequency range.

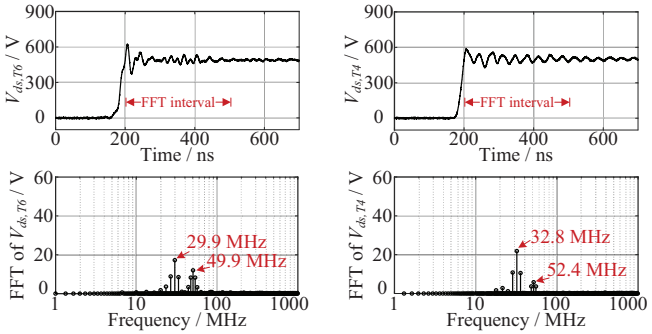


Fig. 20. Time-domain waveforms and frequency spectrums for the outer-mode commutations "0L2 → –" and "– → 0L2" under the DPT condition of V_{bus} = 1000 V, I_L = –40 A, $R_{g,ext}$ = 5.5 Ω, and $C_{g,ext}$ = 3.3 nF. (a) $V_{ds,T6}$ during "0L2 → –". (b) $V_{ds,T4}$ during "– → 0L2".

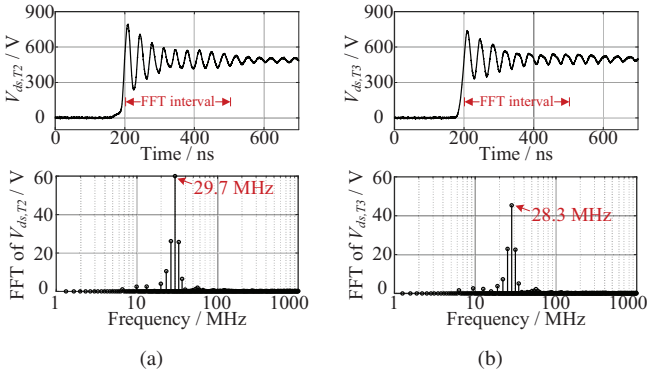


Fig. 21. Time-domain waveforms and frequency spectrums for the inner-mode commutations "0U1 → –" and "– → 0U1" under the DPT condition of V_{bus} = 1000 V, I_L = –40 A, $R_{g,ext}$ = 5.5 Ω, and $C_{g,ext}$ = 3.3 nF. (a) $V_{ds,T2}$ during "0U1 → –". (b) $V_{ds,T3}$ during "– → 0U1".

C. FFT Results of Inner-Mode Commutation

The frequency spectrums and time-domain waveforms of $V_{ds,T2}$ during "0U1 → –" and $V_{ds,T3}$ during "– → 0U1" are exhibited in Figs. 21(a) and 21(b) respectively. As it is illustrated in Section III, a single oscillation frequency can be found from each commutation transient. Specifically, the oscillation components at 29.7 and 28.3 MHz can be identified from Figs. 21(a) and 21(b) respectively (with frequency errors of 2.6 and 2.2 MHz compared to theoretical expectations). Additionally, the oscillation amplitudes of both $V_{ds,T2}$ and $V_{ds,T3}$ during the inner commutations are comparable with that of $V_{ds,T2}$ during the full commutation. A comparison of the oscillation peaks (i.e., voltage overshoots) of $V_{ds,Tx}$ (x = 2, 3, 4, and 6) under the three commutation types will be studied in the following section.

VI. Analysis of Experimental Results II: Other Switching Characteristics and Design Considerations

With the differences in terms of switching loops, the three commutation modes also feature differences on other switching characteristics such as voltage overshoot, current overshoot, capacitive charge, and switching energy. These switching characteristics are exhibited and benchmarked in this section. Then, design guidelines specified for different commutation modes are proposed.

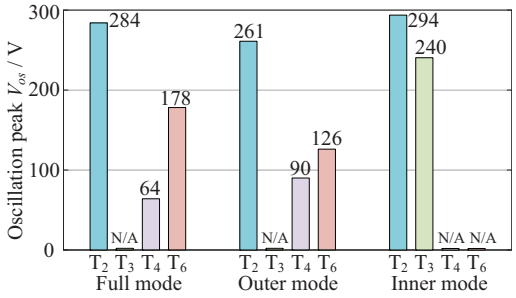


Fig. 22. Comparison of voltage overshoots V_{os} (oscillation peaks) on T_2, T_3, T_4, and T_6 under the DPT condition of V_{bus} = 1000 V, I_L = –40 A, $R_{g,ext}$ = 5.5 Ω, and $C_{g,ext}$ = 3.3 nF.

A. Drain-Source Voltage Overshoots (Oscillation Peaks)

A comparison of voltage overshoots V_{os} (i.e., oscillation peaks) exposed on switching devices T_2, T_3, T_4, and T_6 under the DPT condition of V_{bus} = 1000 V, I_L = –40 A, $R_{g,ext}$ = 5.5 Ω, and $C_{gs,ext}$ = 3.3 nF is indicated in Fig. 22. It is noted that inner switches T_2 and T_3 (T_3 is only applicable for the inner-mode commutation) suffer the greatest voltage overshoots of V_{os} = 240–294 V, since they are enclosed by the loop II with high loop-inductance (L_{lp2} + L_{cm} = 100.7 nH), which leads to elevated voltage overshoots according to:

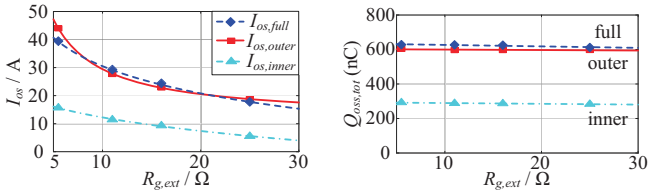
$$V_{os} = L_{loop} \cdot di/dt_{off} \tag{14}$$

where L_{loop} and di/dt_{off} denote the overall loop inductance and turn-off slew rate of device current, respectively. It has also been obtained that these high-voltage overshoots on inner devices are dominated by oscillation components with the low-frequency range from 28.3 to 30.1 MHz.

In contrast, the clamping device T_6 exhibits lower voltage stresses for both full and outer modes (V_{os} = 126–178 V), as it is involved in the loop I with L_{lp1} + L_{cm} = 46.6 nH. Moreover, the active switch T_4 features the lowest voltage-overshoot of V_{os} = 64–90 V for the full and outer commutations.

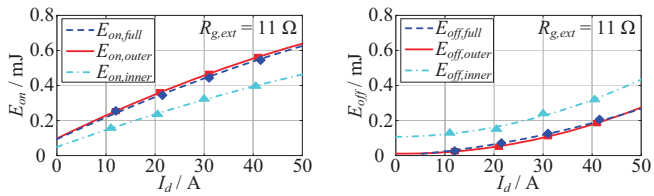
B. Drain-Current Overshoots and Total Capacitive Charges

During turn-on transients, the SiC MOSFET is characterized by a significant drain current overshoot, which is caused by the capacitive charges contributed by C_{oss} of the complementary devices. As it is exhibited in Fig. 23(a), the drain current overshoots I_{os} exhibit dependencies on both the commutation type and external gate resistance. The inner mode features the minimum I_{os}, while the outer mode and full mode reveal I_{os} amplitudes higher than 40 A under the condition of $R_{g,ext}$ = 5.5 Ω. This variation is caused by differences in the total capacitive charge during the turn-on transient. For the full-mode and outer-mode commutations, $C_{oss,T2}$ and $C_{oss,T6}$ shall be charged to $\frac{1}{2}\cdot V_{bus}$ during the turn-on transient of switch T_4 (i.e., "0F → –" and "0L2 → –", respectively).



(a) (b)

Fig. 23. Measured turn-on drain current overshoots and total capacitive charges of the full-mode, outer-mode, and inner-mode commutations under the DPT condition of V_{bus} = 1000 V and I_L = –40 A. (a) Turn-on drain current overshoots I_{os}. (b) Total capacitive charges $Q_{oss,tot}$.



(a) (b)

Fig. 24. Measured turn-on and turn-off switching energies of the full-mode, the outer-mode, and the inner-mode commutations under V_{bus} = 1000 V, $R_{g,ext}$ = 11 Ω, and $C_{g,ext}$ = 3.3 nF. (a) Turn-on switching energies E_{on}. (b) Turn-off switching energies E_{off}.

Considering the non-linearity of C_{oss}, the total capacitive charge $Q_{oss,tot}$ of the full-mode and outer-mode commutations are calculated as 599.8 nC according to:

$$Q_{oss,tot}^{0F\rightarrow -},\, Q_{oss,tot}^{0L2\rightarrow -} = \int_0^{\frac{1}{2}\cdot V_{bus}} \left(C_{oss,T2} + C_{oss,T6}\right)\, dv \quad (15)$$

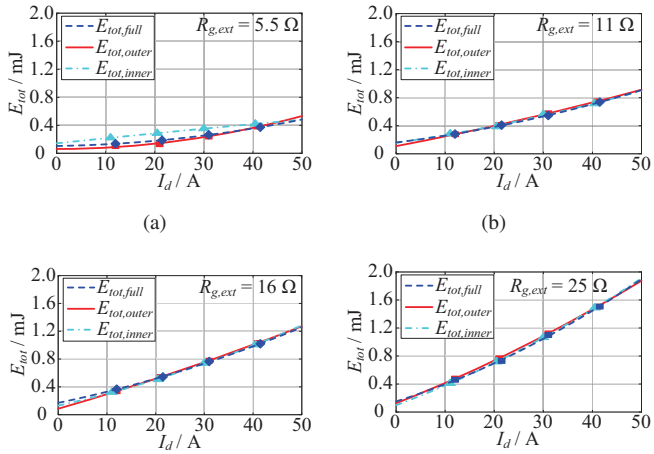
Furthermore, as only $C_{oss,T2}$ is charged during the inner-mode commutation "0U1 → –", the capacitive charge of inner mode is derived as 299.9 nC by:

$$Q_{oss,tot}^{0U1\rightarrow -} = \int_0^{\frac{1}{2}\cdot V_{bus}} C_{oss,T2}\, dv \quad (16)$$

The total capacitive charge $Q_{oss,tot}$ can also be measured by integrating the transient drain-current overshoots during the turn-on interval of the active switch. Fig. 23(b) exhibits those measured $Q_{oss,tot}$ with respect to the external gate resistance $R_{g,ext}$ under the DPT condition of V_{bus} = 1000 V and I_L = –40 A. It can be obtained that the measured $Q_{oss,tot}$ can be regarded as being independent of $R_{g,ext}$. Additionally, the full mode and outer mode exhibit twice the $Q_{oss,tot}$ featured by the inner-mode commutation, both of which match with the theoretical derivations from (12) and (13).

C. Switching Energies

The turn-on and turn-off switching energies E_{on} and E_{off} of the active switch under the DPT condition of V_{bus} = 1000 V and $R_{g,ext}$ = 11 Ω are exhibited in Figs. 24(a) and 24(b), respectively, which are calculated by integrating the term $I_{d,Tx} \times V_{ds,Tx}$ during switching transients. It is noted that the current probe CWTUM/6/R features a peak di/dt of 70 A/ns, which is capable of capturing the rising/falling slope of the drain current. Moreover, a deskew process is performed to align the drain-current and drain-source-voltage waveforms. It can be observed that the full mode and outer mode exhibit excessive turn-on energies (e.g., $E_{on,full}$ = 550 μJ and $E_{on,outer}$ = 560 μJ under I_d = 40 A) compared to that of the inner mode ($E_{on,inner}$ = 390 μJ), as parts of energies stored in $C_{oss,T2}$ and $C_{oss,T6}$ shall be counted in both $E_{on,full}$ and $E_{on,outer}$. On the other hand, their turn-off energies $E_{off,full}$ and $E_{off,outer}$ are relieved compared to $E_{off,inner}$, since the energies stored in $C_{oss,T2}$ and $C_{oss,T6}$ are released during the turn-off transient of T_4 and cause a reduction on $E_{off,full}$ and $E_{off,outer}$.



(a) (b) (c) (d)

Fig. 25. Measured total switching energies E_{tot} of the outer-mode, the inner-mode, and the full-mode commutations. (a) $R_{g,ext}$ = 5.5 Ω. (b) $R_{g,ext}$ = 11 Ω. (c) $R_{g,ext}$ = 16 Ω. (d) $R_{g,ext}$ = 25 Ω.

Additionally, the total switching energies per cycle (E_{tot} = E_{on} + E_{off}) under $R_{g,ext}$ = 5.5 Ω, 11 Ω, 16 Ω, and 25 Ω are shown in Figs. 25(a), 25(b), 25(c), and 25(d), respectively. Overall, the total switching energies E_{tot} of the three commutation modes are comparable under $R_{g,ext}$ = 11 Ω, 16 Ω, and 25 Ω. Nevertheless, under the condition of $R_{g,ext}$ = 5.5 Ω, the E_{tot} of inner mode exceeds these of the full mode and outer mode by 40–100 μJ throughout the drain-current range of 10–40 A. This can be explained since the switching speed of inner mode can be limited by its more significant loop inductance (contributed by main loop II), especially under a low gate resistance condition (e.g., $R_{g,ext}$ = 5.5 Ω).

D. Summaries and Design Considerations

As a summary, switching characteristics of the three commutation modes obtained from DPTs are listed in Table VII, which reveals details in terms of switching oscillations, current overshoots, switching energies, and capacitive charges. It can be concluded that the full mode and outer mode have several similarities, as both of them feature multiple switching loops and oscillation components, as well as excessive current overshoots, switching energies, and capacitive charges. Nevertheless, all of the three types of commutation will induce critical lower-frequency (28.3–30.1 MHz) oscillation peaks on

TABLE VII
SUMMARY OF SWITCHING CHARACTERISITICS OF SIC MOSFETS IN THE 3L-ANPC DEMONSTRATOR.

Commutation types		Oscillation frequencies In Table IV	Critical Oscillations In Fig. 22	Current overshoots In Fig. 23(a)	Switching energies In Fig. 24	Capacitive charges In Fig. 23(b)
Full	"0F → –"	30.1 & 50.5 MHz	T_2 @ 284V, 30.1MHz	39 A	550 μJ	599.8 nC
	"– → 0F"	44.3 MHz	—	—	200 μJ	($Q_{oss,T2}$ + $Q_{oss,T6}$)
Outer	"0L2 → –"	29.9 & 49.9 MHz	T_2 @ 261V, 29.9MHz	44 A	560 μJ	599.8 nC
	"– → 0L2"	32.8 & 52.4 MHz	—	—	190 μJ	($Q_{oss,T2}$ + $Q_{oss,T6}$)
Inner	"0U1 → –"	29.7 MHz	T_2 @ 294V, 27.9MHz	16 A	390 μJ	299.9 nC
	"– → 0U1"	28.3 MHz	T_3 @ 240V, 28.3MHz	—	320 μJ	($Q_{oss,T2}$)

inner switches T_2 and T_3, due to the extra inductance within loop II. According to the knowledge of switching oscillations and other commutation characteristics, the following design considerations can be recognized:

1) For the switching-loop design of a 3L-ANPC inverter, special efforts should be paid on minimizing the inductance of loop II, especially the PCB inductance $L_{\sigma inv}$ exhibited in Fig. 2, to lessen the oscillation peaks exposed on the inner switches T_2 and T_3.
2) For the full-mode and outer-mode operations, the EMI filters should be designed to perform sufficient attenuation for oscillation peaks at both frequency ranges (i.e., 29.9–32.8 MHz and 49.9–52.4 MHz for this work). Specific efforts should be paid on the lower frequency range of 29.4–34.3 MHz, as it features higher oscillation magnitudes. For the inner-mode operation, the EMI filter should be able to perform sufficient noise attenuation at 28.3–29.7 MHz, as significant oscillation magnitude is identified within this frequency band.
3) For the device-selection of inner and clamping switches (i.e., T_2, T_3, T_5, and T_6) under both the full-mode and outer-mode commutations, special attention should be paid on the value of device output capacitance C_{oss}, as well as the junction capacitance of the external diode.
4) In particular, the FEM simulations, e.g., the ANSYS/Q3D or Maxwell, can be a promising method for the evaluation and iteration of the design. Moreover, the technique of magnetic-field cancellation can be utilized for the mitigation of parasitic inductance [43].

VII. CONCLUSION

This paper focuses on investigations of the multi-frequency switching-oscillations of SiC MOSFETs in 3L-ANPC inverters under three typical commutation modes (i.e., the full mode, outer mode, and inner mode). It is found that both the full mode and outer mode involve multiple loops during commutation transients, and different switching-oscillation components with various frequencies can be induced due to this switching-loop diversity. On the contrary, the inner-mode commutation features single switching oscillation at a lower frequency, since it is associated with only one switching loop. Based on the analyses of the equivalent switching circuits using FEM extracted parasitic parameters, these oscillation frequencies for the three commutation modes are identified.

Multiple switching-oscillation components are verified through DPT results obtained under the three commutation modes. For the full-mode and outer-mode commutations, various oscillation components with a frequency range from 29.9 MHz to 54.4 MHz are reported from experimental measurements. On the other hand, only one oscillation component can be identified from the DPT results of the inner-mode commutation. The oscillation frequencies derived by theory match well with these measured by experiments with reasonable errors from 0.5 MHz to 3.6 MHz.

Furthermore, other switching characteristics close related, i.e., the oscillation peaks, current overshoots, capacitive charges, and switching energies, are studied and benchmarked based on DPT results. It is obtained that the inner devices T_2 and T_3 suffer the most significant oscillation peaks for all commutation modes, as they are enclosed by loop II with a high inductance (L_{lp2} = 78.2 nH). Additionally, the full mode and outer mode exhibit several similarities, both of them have excessive current overshoots, switching energies, and capacitive charges.

Last yet not least, several design considerations are proposed for each commutation mode. It is pointed out that special effort should be paid on minimizing the inductance of loop II, especially the PCB inductance of $L_{\sigma inv}$. Accordingly, balancing the inductance components contributed by loops I and II (i.e., L_{lp1} and L_{lp2}) helps to release the design burden of the EMI filter. Special attention should also be paid on the value of device output capacitance C_{oss} when the 3L-ANPC inverter operates under both the full mode and outer mode.

REFERENCES

[1] B. J. Baliga, "Trends in power semiconductor devices," *IEEE Trans. Electron Devices*, vol. 43, no. 10, pp. 1717–1731, Oct. 1996.
[2] C. E. Weitzel, J. W. Palmour, C. H. Carter, K. Moore, K. K. Nordquist, S. Allen, C. Thero, and M. Bhatnagar, "Silicon carbide high-power devices," *IEEE Trans. Electron Devices*, vol. 43, no. 10, pp. 1732–1741, Oct. 1996.
[3] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.
[4] X. She, A. Q. Huang, O. Lucia, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017.
[5] H. Zhang and L. M. Tolbert, "Efficiency impact of silicon carbide power electronics for modern wind turbine full scale frequency converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 21–28, Jan. 2011.

[6] N. Epp, C. Schulte-Overbeck, Z. Cao, M. Lemke, and L. Heinemann, "Sic improves switching losses, power density and volume in ups," in *Proc. PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2016, pp. 1–8.

[7] S. Ohn, J. Yu, P. Rankin, B. Sun, R. Burgos, D. Boroyevich, H. Suryanarayana, and C. Belcastro, "Three-terminal common-mode emi model for emi generation, propagation, and mitigation in a full-sic three-phase ups module," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8599–8612, Sep. 2019.

[8] J. Fabre, P. Ladoux, and M. Piton, "Characterization and implementation of dual-sic mosfet modules for future use in traction converters," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4079–4090, Aug. 2015.

[9] A. K. Morya, M. C. Gardner, B. Anvari, L. Liu, A. G. Yepes, J. Doval-Gandoy, and H. A. Toliyat, "Wide bandgap devices in ac electric drives: Opportunities and challenges," *IEEE Trans. Transp. Electrific.*, vol. 5, no. 1, pp. 3–20, Mar. 2019.

[10] S. Jahdi, O. Alatise, C. Fisher, L. Ran, and P. Mawby, "An evaluation of silicon carbide unipolar technologies for electric vehicle drive-trains," *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 2, no. 3, pp. 517–528, Sep. 2014.

[11] J. Wang, T. Zhao, J. Li, A. Q. Huang, R. Callanan, F. Husna, and A. Agarwal, "Characterization, modeling, and application of 10-kv sic mosfet," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 1798–1806, Aug. 2008.

[12] D. Sadik, K. Kostov, J. Colmenares, F. Giezendanner, P. Ranstad, and H. Nee, "Analysis of parasitic elements of sic power modules with special emphasis on reliability issues," *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 988–995, Sep. 2016.

[13] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An experimental investigation of the tradeoff between switching losses and emi generation with hard-switched all-si, si-sic, and all-sic device combinations," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2393–2407, May 2014.

[14] Z. Zhang, "Characterization and realization of high switching-speed capability of sic power devices in voltage source converter," Ph.D. dissertation, Univ. of Tennessee, Knoxville, TN, 2015.

[15] Z. Zhang, B. Guo, F. F. Wang, E. A. Jones, L. M. Tolbert, and B. J. Blalock, "Methodology for wide band-gap device dynamic characterization," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9307–9318, Dec. 2017.

[16] S. Hazra, A. De, L. Cheng, J. Palmour, M. Schupbach, B. A. Hull, S. Allen, and S. Bhattacharya, "High switching performance of 1700-v, 50-a sic power mosfet over si igbt/bimosfet for advanced power conversion applications," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4742–4754, Jul. 2016.

[17] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-v, 60-a sic mosfet multichip phase-leg module for high-temperature, high-frequency applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2307–2320, May 2014.

[18] S. Hazra, S. Madhusoodhanan, G. K. Moghaddam, K. Hatua, and S. Bhattacharya, "Design considerations and performance evaluation of 1200-v 100-a sic mosfet-based two-level voltage source converter," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4257–4268, Sep. 2016.

[19] B. N. Torsæter, S. Tiwari, R. Lund, and O. Midtgård, "Experimental evaluation of switching characteristics, switching losses and snubber design for a full sic half-bridge power module," in *Proc. 2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Jun. 2016, pp. 1–8.

[20] X. Li, J. Jiang, A. Q. Huang, S. Guo, X. Deng, B. Zhang, and X. She, "A sic power mosfet loss model suitable for high-frequency applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8268–8276, Oct. 2017.

[21] T. Liu, R. Ning, T. T. Y. Wong, and Z. J. Shen, "Modeling and analysis of sic mosfet switching oscillations," *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 747–756, Sep. 2016.

[22] Z. Zhang, B. Guo, and F. Wang, "Evaluation of switching loss contributed by parasitic ringing for fast switching wide band-gap devices," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9082–9094, Sep. 2019.

[23] X. Yuan, H. Stemmler, and I. Barbi, "Investigation on the clamping voltage self-balancing of the three-level capacitor clamping inverter," in *Proc. 30th Annual IEEE Power Electronics Specialists Conference. Record. (Cat. No.99CH36321)*, vol. 2, Jul. 1999, pp. 1059–1064.

[24] T. Bruckner, S. Bernet, and H. Guldner, "The active npc converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 855–868, Jun. 2005.

[25] O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, and R. Teodorescu, "Converter structure-based power loss and static thermal modeling of the press-pack igbt three-level anpc vsc applied to multi-mw wind turbines," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2505–2515, Nov. 2011.

[26] Y. Jiao, S. Lu, and F. C. Lee, "Switching performance optimization of a high power high frequency three-level active neutral point clamped phase leg," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3255–3266, Jul. 2014.

[27] Y. Jiao and F. C. Lee, "New modulation scheme for three-level active neutral-point-clamped converter with loss and stress reduction," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5468–5479, Sep. 2015.

[28] D. Barater, C. Concari, G. Buticchi, E. Gurpinar, D. De, and A. Castellazzi, "Performance evaluation of a three-level anpc photovoltaic grid-connected inverter with 650-v sic devices and optimized pwm," *IEEE Trans. Ind. Appl.*, vol. 52, no. 3, pp. 2475–2485, May 2016.

[29] Q. Guan, C. Li, Y. Zhang, S. Wang, D. D. Xu, W. Li, and H. Ma, "An extremely high efficient three-level active neutral-point-clamped converter comprising sic and si hybrid power stages," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8341–8352, Oct. 2018.

[30] T. B. Soeiro, K. Park, and F. Canales, "High voltage photovoltaic system implementing si/sic-based active neutral-point-clamped converter," in *Proc. IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2017, pp. 1220–1225.

[31] J. He, D. Zhang, and D. Pan, "An improved pwm strategy for "sic+si" three-level active neutral point clamped converter in high-power high-frequency applications," in *Proc. 2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 5235–5241.

[32] D. Zhang, J. He, and D. Pan, "A megawatt-scale medium-voltage high-efficiency high power density "sic+si" hybrid three-level anpc inverter for aircraft hybrid-electric propulsion systems," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 5971–5980, Nov. 2019.

[33] H. Gui, Z. Zhang, R. Chen, R. Ren, J. Niu, H. Li, Z. Dong, C. Timms, F. Wang, L. M. Tolbert, B. J. Blalock, D. Costinett, and B. B. Choi, "Development of high-power high switching frequency cryogenically cooled inverter for aircraft applications," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5670–5682, June 2020.

[34] F. Wang, R. Chen, H. Gui, J. Niu, L. Tolbert, D. Costinett, B. Blalock, S. Liu, J. Hull, J. Williams, T. Messer, E. Solodovnik, D. Paschedag, V. Khozikov, C. Severns, and B. Choi, "Mw-class cryogenically-cooled inverter for electric-aircraft applications," in *Proc. 2019 AIAA/IEEE Electric Aircraft Technologies Symposium (EATS)*, Aug. 2019, pp. 1–9.

[35] M. Chen, D. Pan, H. Wang, X. Wang, F. Blaabjerg, and W. Wang, "Switching characterization of sic mosfets in three-level active neutral-point-clamped inverter application," in *Proc. 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, May 2019, pp. 1793–1799.

[36] B. Liu, R. Ren, E. A. Jones, H. Gui, Z. Zhang, R. Chen, F. Wang, and D. Costinett, "Effects of junction capacitances and commutation loops associated with line-frequency devices in three-level ac/dc converters," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6155–6170, July 2019.

[37] R. Ren, Z. Zhang, B. Liu, R. Chen, H. Gui, J. Niu, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, "Multi-commutation loop induced over-voltage issue on non-active switches in fast switching speed three-level active neutral point clamped phase leg," in *Proc. 2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 1328–1333.

[38] H. Gui, R. Chen, Z. Zhang, J. Niu, R. Ren, B. Liu, L. M. Tolbert, F. F. Wang, D. Costinett, B. J. Blalock, and B. B. Choi, "Modeling and mitigation of multiloops related device overvoltage in three-level active neutral point clamped converter," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7947–7959, 2020.

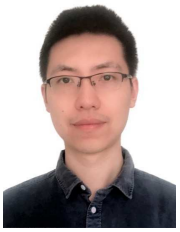
[39] H. Gui, R. Chen, Z. Zhang, J. Niu, L. M. Tolbert, F. Wang, D. Costinett, B. J. Blalock, and B. B. Choi, "Methodology of low inductance busbar design for three-level converters," *IEEE J. Emerging Sel. Topics Power Electron.*, pp. 1–1. DOI: 10.1109/JESTPE.2020.2 999 403, 2020.

[40] H. Gui, Z. Zhang, R. Chen, R. Ren, J. Niu, B. Liu, H. Li, Z. Dong, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, "A simple control to reduce device over-voltage caused by non-active switch loop in three-level anpc converters," in *Proc. 2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 1337–1343.

[41] *APTMC120AM55CT1AG Datasheet*, Microsemi, Jun. 2013, rev. 1.

[42] M. Chen, H. Wang, H. Wang, F. Blaabjerg, X. Wang, and D. Pan, "Reliability assessment of hybrid capacitor bank using electrolytic- and film-capacitors in three-level neutral-point-clamped inverters," in *Proc. 2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2019, pp. 2826–2832.

[43] *Design Considerations for Designing with Cree SiC Modules: Part 2. Techniques for Minimizing Parasitic Inductance*, Cree, Inc., 2013.
[44] U. Nicolai and A. Wintrich, "Determining switching losses of semikron igbt modules," SEMIKRON GmbH, Nuremberg, Germany, Tech. Rep. AN 1403, Aug. 2014.
[45] S. Jahdi, O. Alatise, J. A. Ortiz Gonzalez, R. Bonyadi, L. Ran, and P. Mawby, "Temperature and switching rate dependence of crosstalk in si-igbt and sic power modules," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 849–863, Feb. 2016.
[46] Z. Zhang, J. Dix, F. F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, "Intelligent gate drive for fast switching and crosstalk suppression of sic devices," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9319–9332, Dec. 2017.



Mengxing Chen (S'16) received his B.E. and M.E. degrees in electrical engineering from Shandong University, Jinan, China, in 2014 and 2017, respectively. He is currently working toward the Ph.D. degree with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. He was a Visiting Scientist with the Fraunhofer Institute for Reliability and Microintegration IZM, Berlin, Germany, from Jan. to Mar. 2020.

His research interests include the reliability of power electronics, Silicon Carbide (SiC) based power converters, and multilevel converters. Mengxing Chen was the recipient of the IEEE Southern Power Electronics Conference (SPEC) 2018 Best Paper Award.

Donghua Pan (S'12-M'15) received the B.S. and Ph.D. degrees in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2010 and 2015, respectively.

Since September 2017, he has been with Aalborg University, Aalborg, Denmark, where he is currently a Postdoctoral Fellow with the Department of Energy Technology. His research interests include magnetic integration techniques, modeling and control of grid-connected converters, and wide bandgap power conversion systems.

He was the recipient of the Outstanding Reviewer Award of IEEE TRANSACTIONS ON POWER ELECTRONICS in 2017 and the Best Paper Award at IEEE SPEC 2018.

Huai Wang (M'12, SM'17) received the B.E. degree in electrical engineering, from Huazhong University of Science and Technology, Wuhan, China, in 2007 and the Ph.D. degree in power electronics, from the City University of Hong Kong, Hong Kong, in 2012. He is currently Professor with the Center of Reliable Power Electronics (CORPE), Department of Energy Technology at Aalborg University, Denmark. He was a Visiting Scientist with the ETH Zurich, Switzerland, from Aug. to Sep. 2014, and with the Massachusetts Institute of Technology (MIT), USA, from Sep. to Nov. 2013. He was with the ABB Corporate Research Center, Switzerland, in 2009. His research addresses the fundamental challenges in modelling and validation of power electronic component failure mechanisms, and application issues in system-level predictability, condition monitoring, circuit architecture, and robustness design.

Dr. Wang received the Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society in 2016, and the Green Talents Award from the German Federal Ministry of Education and Research in 2014. He is currently the Chair of IEEE PELS/IAS/IES Chapter in Denmark. He serves as an Associate Editor of IET Electronics Letters, IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, and IEEE TRANSACTIONS ON POWER ELECTRONICS.

Xiongfei Wang (S'10-M'13-SM'17) received the B.S. degree from Yanshan University, Qinhuangdao, China, in 2006, the M.S. degree from Harbin Institute of Technology, Harbin, China, in 2008, both in electrical engineering, and the Ph.D. degree in energy technology from Aalborg University, Aalborg, Denmark, in 2013.

Since 2009, he has been with the Department of Energy Technology, Aalborg University, where he became an Assistant Professor in 2014, an Associate Professor in 2016, a Professor and Research Program Leader for Electronic Power Grid (eGrid) in 2018, and the Director of Aalborg University-Huawei Energy Innovation Center in 2020. He is also a Visiting Professor of power electronics systems with KTH Royal Institute of Technology, Stockholm, Sweden. His current research interests include modeling and control of grid-interactive power converters, stability and power quality of power-electronic-based power systems, active and passive filters.

Dr. Wang was selected into Aalborg University Strategic Talent Management Program in 2016. He has received six IEEE Prize Paper Awards, the 2016 Outstanding Reviewer Award of IEEE TRANSACTIONS ON POWER ELECTRONICS, the 2018 IEEE PELS Richard M. Bass Outstanding Young Power Electronics Engineer Award, the 2019 IEEE PELS Sustainable Energy Systems Technical Achievement Award, and the 2019 Highly Cited Researcher by Clarivate Analytics (former Thomson Reuters). He serves as a Member at Large for Administrative Committee of IEEE Power Electronics Society in 2020-2022, and as an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.

Frede Blaabjerg (S'86–M'88–SM'97–F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications.

He has received 32 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019 and the 2020 IEEE Edison Medal. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019-2020 he serves a President of IEEE Power Electronics Society. He is Vice-President of the Danish Academy of Technical Sciences too. He is nominated in 2014-2019 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.