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An Improved *di/dt*-RCD Detection for Short-Circuit Protection of SiC MOSFET

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***Abstract*-Silicon Carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) has a smaller short-circuit tolerance, and hence requires faster and more accurate short-circuit protection. One prospective method is to combine fast *di/dt* detection with an integration circuit. The former is for detecting the extremely fast increase of short-circuit current, while the latter is for generating a scaled copy of the short-circuit current for comparison with a threshold. The integration is almost always performed with a resistive-capacitive (RC) low-pass filter due to its simplicity. However, it does not produce consistent results under different load and fault conditions, which can, in turn, cause the detection to fail. An alternative *di/dt*-RCD (RC + diode) protective circuit has therefore been proposed to offer more accurate and consistent results, irrespective of the fault types. Design equations for the circuit have been derived for implementing an experimental setup, from which results have proven the effectiveness of the proposed *di/dt*-RCD protection.**

***Index Terms*—short-circuit protection, SiC MOSFET, Kelvin-source, Gate-driver**

I. Introduction

SiC MOSFET has been designed to replace silicon (Si) insulated gate bipolar transistor (IGBT) in some applications, where high temperature resistance, voltage resistance and switching speed are essential [1] [2]. But, with SiC MOSFET, short-circuit protection will become more complex because of three reasons. Firstly, with a higher switching frequency, SiC MOSFET operates in an environment with more severe electromagnetic interferences (EMIs) from other devices. This may cause errors in the control and gating signals, leading to a short-circuit fault [1]. Secondly, with a higher short-circuit current but a smaller chip size, SiC MOSFET has a shorter short-circuit withstand time [2] [3]. In other words, its short-circuit detection must be (completed) much faster. Thirdly, as operating temperature changes, static characteristics of the SiC MOSFET can vary more significantly.

Direct adoption of an existing IGBT protective technique, including detection of its desaturation, gate charge, sampling resistance, current magnitude and / or rate of change *di/dt*, will therefore not always function as intended, when used with a SiC MOSFET [3]-[6]. Particularly, with the most widely used detection of desaturation, short-circuit protection of a SiC MOSFET will face two problems. The first problem is related to the usual blanking time required for detecting desaturation, which will undoubtedly slow down the protection. The second problem is related to the earlier mentioned static characteristic variations of a SiC MOSFET with temperature. Such variations can make it tougher to find a desaturation point for the SiC MOSFET, which in turn, renders its detection to be less reliable [5].

As for detecting gate charge to protect a SiC MOSFET, its speed of response can be very fast, but it does not work well when detecting the so-called fault under load (FUL) [5] [7]. Moreover, Miller capacitance of a SiC MOSFET is noticeably smaller than that of an IGBT. It is therefore difficult to distinguish between a short circuit and a normal condition [5]. Some tradeoffs also exist with detecting current magnitude or sampling resistance for protecting the SiC MOSFET. On one hand, they exhibit high accuracy and speed, but on the other hand, they incur either an expensive high-precision current sensor or a lossy sampling resistor. Detection of current magnitude or sampling resistance has therefore been rarely suggested for short-circuit protection of a SiC MOSFET [5].

The other option is to detect rate of change of current flowing through parasitic inductance of the SiC MOSFET. The detected *di/dt* can then be processed by a simple resistive-capacitive (RC) low-pass filter to restore the fast-changing current for comparing with a specified threshold. These, supported by appropriate latching and shutting-down logics, offer a simple protective circuit with both fast response and immunity towards temperature variations [3] [6]. It is thus a better alternative, as compared to the other described options. However, it encounters some problems when detecting FUL, which presently have not been resolved well in the literature [4] [5]. This paper therefore targets to clearly identify the FUL source of problems in Section II, before proposing a simple *di/dt*-RCD (RC + diode) solution in Section III. Section IV then describes experimental results, from which a conclusion can be drawn for finalizing the paper in Section V.

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II. Traditional *di/dt* Protection and its Problems

The operating principles of traditional *di/dt* short-circuit protection are first introduced, from which FUL problems can swiftly be brought out through some simple illustrative waveforms.

A. Operating principles

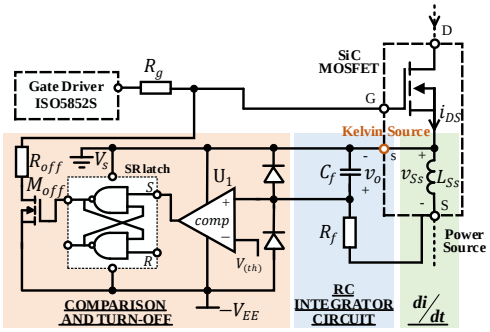

Fig. 1. *di/dt*-RC protective circuit.

A typical *di/dt*-RC detection circuit for protecting SiC MOSFET is shown in Fig. 1. It consists of three parts named from right to left as the differential part (green), integral part (blue), and "comparison and turn-off" part (pink). In the differential part, voltage v_{Ss} across parasitic inductance L_{Ss} between Kelvin- and power-source terminals of the SiC MOSFET has been measured to obtain the derivative of the drain-source current i_{DS}:

$$v_{Ss} = L_{Ss}\frac{di_{DS}}{dt} \tag{1}$$

where L_{Ss} can be calibrated during manufacturing by performing a double-pulse test with high precision probes for measuring v_{Ss} and i_{DS}, and then using (1) to find L_{Ss} [3].

As for the second integral part, it usually includes a passive RC low-pass filter for performing high-frequency integration only. The purpose is to restore the sharp-rising current i_{DS} from the measured di_{DS}/dt during a short-circuit fault. A related high-frequency transfer function ($sR_fC_f >> 1$) can be expressed as:

$$\frac{v_o(s)}{i_{DS}(s)} = \frac{-sL_{Ss}}{sR_fC_f+1} \approx \frac{-L_{Ss}}{R_fC_f} \tag{2}$$

where R_f, C_f and $v_o(s)$ are resistance, capacitance and output voltage of the RC filter, respectively. Output $v_o(s)$ is thus a restored copy of $i_{DS}(s)$ during fault, but scaled by $-L_{Ss}/(R_fC_f)$.

The restored $v_o(s)$ is then inputted to the third "comparison and turn-off" part. More precisely, v_o connects to the positive terminal of a comparator, whose negative terminal connects to a specified threshold voltage $V_{(th)}$. This threshold decides the short-circuit level to protect against, and must hence be similarly scaled according to (2). The remaining SR latch, switch M_{off} and resistor R_{off} are then for implementing the required shutdown, after the comparator confirms the occurrence of a short-circuit fault.

B. Problems with RC integration despite simplicity

The RC integrator is for restoring current waveform from its derivative, which in Fig. 1 is sensed through measuring the voltage across parasitic inductance L_{Ss}. Its simplicity and fast response have helped greatly with compact packaging and lowering costs, while offering protection to the SiC MOSFET. However, it does not function properly under certain circumstances, which become obvious, after clarifying two short-circuit scenarios mentioned in [7].

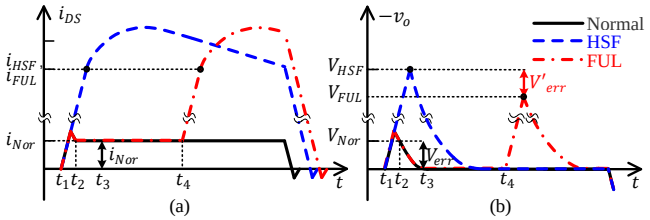

Fig. 2. Typical (a) i_{DS} and (b) $-v_o$ waveforms associated with *di/dt*-RC circuit under normal, HSF and FUL operating conditions.

The first scenario happens when the protective circuit of a SiC MOSFET senses a short-circuit fault at the instant of turning on the device. This is called a hard switch fault (HSF), detected by the protective circuit of an initially blocking device that has initiated the fault. The second scenario occurs when the device has not caused a fault at its turn-on, and is hence conducting properly. Its protection circuit however subsequently senses a fault caused by the turning on of another device. The protective circuit of the conducting device has therefore sensed a fault under load (FUL) [7]. Both fault scenarios are likely to occur, meaning the same protective circuit for a device must flag a fault, regardless of which type of fault has occurred.

More details about both scenarios can be extracted from Fig. 2, where waveforms of i_{DS} and v_o have been drawn for both normal and fault conditions. In case of a HSF occurring at time t_1, the device must turn off whenever its rising current i_{DS} reaches i_{HSF} marked in Fig. 2(a). This has been ensured by its protective RC integrator, whose output v_o rises until it reaches the threshold V_{HSF} in Fig. 2(b), which according to (2), is a scaled copy of i_{HSF}. After which, both i_{DS} and v_o return to zero along differently shaped trajectories, which are expected since the return of i_{DS} is more gradual (no longer high frequency), and hence cannot be tracked closely by the RC integrator.

On the other hand, if there is no fault at t_1, the device continues to conduct its nominal current $i_{DS} = i_{Nor}$, after a rapid increase and a small overshoot between t_1 and t_2. The initial short trajectory has been tracked accurately by v_o of the RC integrator, but after t_2, v_o can no longer track i_{Nor} with almost zero derivative. Integral v_o eventually reaches zero at t_3, which in Fig. 1, is equivalent to C_f discharging fully through L_{Ss} and R_f. Despite that, the device continues to conduct i_{Nor} until t_4, at which another device turns on and causes a FUL. Current i_{DS} then rises from i_{Nor} to i_{FUL}. For the same short-circuited device, i_{FUL} should ideally equal to i_{HSF}, as shown in Fig. 2(a). However, at the output of the RC integrator, v_o rises from zero to V_{FUL}, which as seen from Fig. 2(b), is not equal to V_{HSF}. Instead, it is smaller by error V'_{err} ($\approx V_{err}$), which from (2), will vary with i_{Nor}.

To still turn off the conducting device, the triggering threshold must hence be reset to V_{FUL}. In other words, the protective circuit in Fig. 1 must have two $V_{(th)}$ with one threshold at V_{HSF} for HSF and another at V_{FUL} for FUL. This can be challenging to design, especially since V_{FUL} varies with i_{Nor}, which in turn, varies with the connecting loads.

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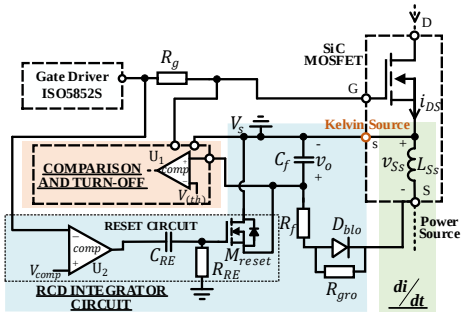


Fig. 3. Proposed *di/dt*-RCD protective circuit.

III. Proposed Simple RCD Integrator

To avoid V'_{err} in Fig. 2 and its load dependency, the voltage v_o across C_f of the protective circuit in Fig. 1 must be prevented from discharging fully, whenever the SiC MOSFET being protected is conducting its nominal current i_{Nor}. A simple solution is to use proposed RCD integrator as shown in Fig. 3. The new integrator adds a diode D_{blo}, a large ground resistance R_{gro} and a reset circuit to the original RC integrator. Their roles are described below.

A. Diode D_{blo}

Diode D_{blo} does not affect the protective circuit of a device, whenever that device turns on and causes a HSF at t'_1 in Fig. 4(a). The response of the RCD integrator in Fig. 4(b) during HSF therefore remains the same as that of the RC integrator in Fig. 2(b). However differences surface during FUL. To illustrate, the device turning on at t'_1 is assumed to not trigger a HSF in Fig. 4(a). Its current therefore stabilizes at i_{Nor}, after the usual short initial current rise and small overshoot. This pattern, including the stabilization at i_{Nor}, has precisely been tracked by the output v_o of the RCD integrator, as shown in Fig. 4(b). In other words, v_o of the RCD integrator does not fall to zero, unlike the RC integrator, whose response has also been repeated in Fig. 4(b) for an easier comparison. This is possible, because of D_{blo} blocking v_o across C_f from discharging in Fig. 3 (if ground resistance R_{gro} is large enough as explained later).

Subsequently, with a FUL occurring at t'_4, v_o begins to rise to threshold $V_{FUL\_RCD} = V_{HSF\_RCD}$, as i_{DS} increases to $i_{FUL} = i_{HSF}$. The same threshold can therefore be set for detecting both HSF and FUL with the latter no longer influenced by the loads. Such performance can further be enhanced by choosing D_{blo} with a smaller loss to avoid raising charging speed of C_f unnecessarily. This then avoids major changes to the detection threshold and other parameters. It is thus important to choose D_{blo} as a schottky diode with low junction voltage, low reverse-recovery current and fast switching. The chosen diode must also have appropriate rated forward current, which according to Fig. 3, can peak at:

$$i_{RCD\_P} = \frac{V_{Ss\_P}}{R_f} \tag{3}$$

where V_{Ss_P} represents peak voltage detected across L_{Ss}.

B. Reset circuit

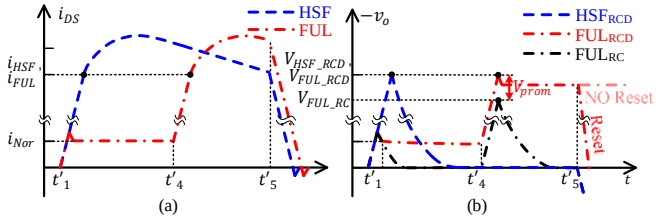


Fig. 4. Typical (a) i_{DS} and (b) $-v_o$ waveforms associated with *di/dt*-RCD and *di/dt*-RC circuits under HSF and FUL operating conditions.

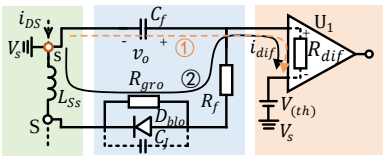


Fig. 5. Differential, integral and logic parts of *di/dt*-RCD detection.

Despite its advantage with detecting FUL, diode D_{blo} prevents C_f from discharging or resetting, whenever the driver turns off the SiC device, as shown in Fig. 4(b). Voltage v_o across C_f will then not rise correctly from zero at the start of the next switching cycle. This can cause incorrect triggering of short-circuit protection. To avoid such occurrence, an explicit reset circuit must be inserted to null v_o across C_f upon turning off the protected device. The inserted reset circuit can be viewed from Fig. 3, where a second comparator U_2 can explicitly be seen. Terminals of U_2 are tied to the gate driver and a reset threshold V_{comp} = 0 V. Therefore, whenever the driver turns off the SiC device, U_2 outputs a positive voltage V_p = 15 V.

This voltage, upon fed through a CR high-pass filter, gives rise to a short positive pulse for turning on reset switch M_{reset} for a time duration t_{reset} expressed as:

$$t_{reset} \approx -R_{RE}\left(C_{RE}+C_{M\_RE}\right)\ln\left(\frac{V_{GS(th)\_M\_RE}\left(C_{RE}+C_{M\_RE}\right)}{V_p C_{RE}}\right) \tag{4}$$

where C_{RE} and R_{RE} are capacitance and resistance of the high-pass filter, and C_{M_RE} and $V_{GS(th)\_M\_RE}$ are input capacitance and threshold voltage of M_{reset}. Duration t_{reset} in (4) should additionally be long enough for M_{reset} to respond, while not affecting the readying of the next short-circuit detection for the main SiC device. Moreover, to avoid affecting the RCD integral circuit, R_{RE} should connect to the gate-drain of reset MOSFET M_{reset}, instead of its gate-source. This does not affect operation of M_{reset}, since the difference between its drain and source voltages is only v_o, which usually is 1~2 V.

C. Ground resistance R_{gro}

Ground resistance R_{gro} is needed to prevent false short-circuit detection. To better illustrate this, the RCD integrator has been enlarged as shown in Fig. 5, where the usual differential mode input resistance R_{dif} within comparator U_1 has also been shown. This resistance unintentionally closes a current loop ① consisting of a voltage source for setting threshold $V_{(th)}$, C_f and R_{dif}. It is therefore possible for C_f to charge to $V_{(th)}$, which in turn, signals a false short-circuit. A suggested precaution is to insert a ground resistance R_{gro} for forming an alternative shunt current loop ②. Voltage v_o across C_f can then be approximated as:

$$V_o \approx V_{(th)} \frac{R_{gro}+R_f}{R_{gro}+R_f+R_{dif}} \quad (5)$$

according to Fig. 5, and noting the dc voltage of L_{Ss} and dc current of C_f are both zero.

It is thus essential to choose $R_{gro} << R_{dif}$ to prevent v_o from reaching $V_{(th)}$. Additionally, R_{gro} must be large enough to avoid cancelling the effects of diode D_{blo}, which fortunately can easily be met, since R_{dif} is always very big. Nonetheless, with R_{gro}, v_o across C_f can still discharge slightly, after safely turning on the SiC device at t'_1 in Fig. 4(b). Its minimum value, before the device turns off, with reference to its value at t'_1 can, then, be expressed as:

$$\delta \approx e^{\frac{-1}{(R_{gro}+R_f)C_f f}} \quad (6)$$

where f is the switching frequency of the SiC MOSFET. To summarize, R_{gro} must be chosen to provide a satisfactory tradeoff between (5) and (6).

D. *Possible oscillations in* SiC MOSFET *current* i_{DS}

Although Fig. 4(a) shows i_{DS} overshooting only slightly, after the protected SiC MOSFET turns on successfully at t'_1, there may additionally be some high-frequency oscillations in practice. These oscillations are mostly caused by L_{Ss} and the junction capacitance C_j of D_{blo} in Fig. 5, which when integrated, can cause v_o to oscillate. To minimize such oscillations, an extra small capacitor can be connected in parallel with D_{blo}, even though it is not necessary for the implemented experimental setup. Also important to note is once D_{blo} turns on fully, the added small capacitor is shorted and will hence not influence the RCD integration.

IV. Experimental Setup and Results

An experimental setup with a phase-leg for performing double-pulse test (DPT) has been implemented, as shown in Fig. 6. Its purpose is to test the proposed *di/dt*-RCD detection when used to protect the lower 30-A SiC MOSFET against FUL and HSF. The test sequence begins with DPT performed on the lower MOSFET, after which the upper switch is turned on during the second pulse to imitate a FUL. As for HSF, the process is simply to turn on the upper switch, followed by the lower switch. For both tests, the chosen or measured parameters are C_f = 470 pF, R_f = 300 Ω, L_{Ss} ≈ 3 nH and R_{gro} = 30 kΩ, which according to (2), give a scaling factor of i_{DS} / v_o ≈ -47. It implies that with a threshold of $V_{(th)}$ = -1.8 V set for comparator U_1 in Fig. 1 and Fig. 3, the smallest short-circuit current that can correctly activate the protection circuit is about 84.6 A (calculated threshold current).

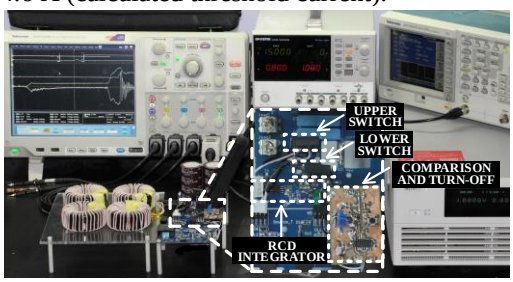
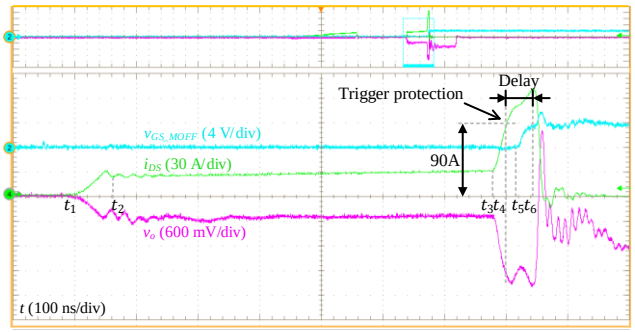
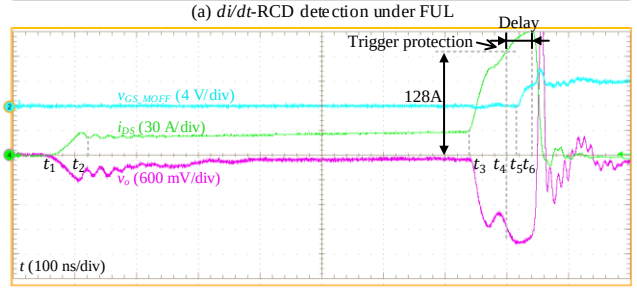


Fig. 6. Experimental hardware for validating protection circuits.

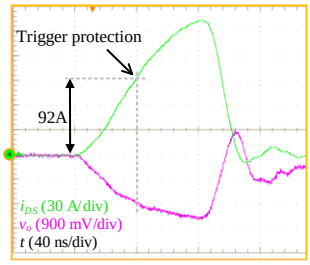
A. *Protection against FUL*



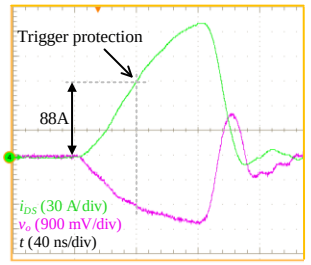
(a) *di/dt*-RCD detection under FUL



(b) *di/dt*-RC detection under FUL



(c) *di/dt*-RCD detection under HSF



(d) *di/dt*-RC detection under HSF

Fig. 7. Measurement results obtained with *di/dt* detection.

Obtained results are then shown in Fig. 7(a) and (b) for the proposed RCD and usual RC integrators, respectively. In both figures, time t_1-t_2 shows the smooth turning on of the lower MOSFET upon applying the second test pulse. At t_3, the upper switch from the same phase-leg is intentionally turned on to initiate a FUL, causing i_{DS} of the lower MOSFET and output v_o of each protective integrator to rise in magnitude. At t_4, protection is triggered upon v_o reaching threshold $V_{(th)}$ = -1.8 V, but for the RCD integrator, t_4 has a smaller value or happens earlier. Correspondingly, i_{DS} reaches 90 A with the RCD integrator, but much higher at 128 A with the RC integrator. To further distinguish these values from the calculated threshold current of 84.6 A, corresponding i_{DS} when v_o reaches -1.8 V is marked as "Trigger protection" current in Fig. 7. Then, at t_5 after 16 ns of logic delay, gate voltage v_{GS_MOFF} of the shutdown switch M_{off} in Fig. 1 (also used in Fig. 3 but not explicitly shown) starts to rise to initiate the protection. At t_6, switch M_{off} has been fully turned on, causing the protected lower SiC MOSFET to turn off. During the period from t_4 to t_6, it can also be seen that the increase of i_{DS} with *di/dt*-RC detection is smaller than that with *di/dt*-RCD detection. This is due to the SiC MOSFET gradually transiting from its ohmic to active region, which in turn, causes its rate of short-circuit current increase to drop.

The recorded magnitudes and times for both integrators have subsequently been summarized in Table I, from which it

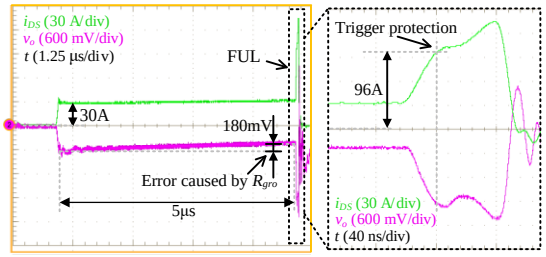


Fig. 8. Error caused by R_{gro} in *di/dt*-RCD detection.

TABLE I. RC VERSUS RCD INTEGRATION

Integrating circuit	Calculated threshold current	Trigger protection current (t_d)	Detection error	Clamped current (t_s)	Total time
RC	84.6 A	128 A	51.3%	150 A	100 ns
RCD	84.6 A	90 A	6.4%	132 A	60 ns

can be seen that the proposed RCD integrator reduces the detection error from 51.3% to 6.4% and the protection time from 100 ns to 60 ns, when tested with a FUL. These are possible, since the proposed RCD integrator is not prone to measurement error related to the load-dependent nominal current $i_{DS} = i_{Nor}$, as explained in Section III.

It should however be noted that R_{gro} in parallel with diode D_{blo} can cause the RCD integration to generate an error, which according to (6), varies with switching frequency of the SiC device. It is therefore necessary to specify a switching frequency, which if set at 200 kHz for a current of 30 A, results in a reduction of v_o by 190.8 mV (29.9%) at the end of a 5-µs switching period. Corresponding experimentally measured detection error caused by R_{gro} can be read from Fig. 8. The reduction of v_o read is 180 mV at the end of a 5-µs period. This is not very different from the theoretical value of 190.8 mV. Subsequently, after introducing a FUL, the total current detection error increases from 6.4% to 13.5%, which in terms of trigger protection current, increases from 90 A in Fig. 7(a) to 96 A in Fig. 8. Both currents are not very different, since a 180-mV error in v_o is seriously not significant, as compared to the 1.8-V threshold voltage.

B. Protection against HSF

Fig. 7(c) and (d) show results obtained with both *di/dt*-RC and *di/dt*-RCD schemes when experiencing a HSF. The results confirm that both schemes exhibit similar performances, in accordance to Subsection II(B).

C. Practical application issues

Physically, the proposed *di/dt*-RCD scheme requires a device with a Kelvin source. It should therefore protect a power module or a 4-pin discrete device. With the chosen device, its parasitic inductance L_{Ss} should be measured, following the method described in the first paragraph of Subsection II(A) or in [3]. In most cases, such measurement only needs to be performed once. Subsequently, a simple reset circuit must be inserted to the *di/dt*-RCD scheme, which certainly increases complexity slightly, but is definitely a simple way for enhancing FUL short-circuit detection. Lastly, with a low switching frequency, even though not common with a SiC MOSFET, accuracy of the *di/dt*-RCD detection can be ensured by choosing a larger differential mode input resistance R_{dif} for comparator U_1. This then permits R_{gro} to be set higher.

V. CONCLUSION

In the paper, an accurate *di/dt*-RCD protective circuit has been proposed for protecting SiC MOSFET under both Hard Switch Fault (HSF) and Fault Under Load (FUL). Theories and experiments have proven that the included RCD integrator can solve the problem of requiring different HSF and FUL thresholds for detecting the same short-circuit current or detecting different HSF and FUL currents with the same comparative threshold. Compared with the existing *di/dt*-RC circuit, the proposed *di/dt*-RCD circuit is more promising. Because existing *di/dt*-RC circuits either needs to detect a much higher FUL current or demands different load-varying thresholds.

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