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Generalized Switch Current Stress Reduction Technique for Coupled-Inductor based Single Switch High Step-Up Boost Converter

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***Abstract*—Coupled inductor based boost converters suffer from high switch current stress in steady state and transient due to less self-inductance value in their winding. In this work, a generalized switch current stress reduction technique is proposed by modifying circuit topology of coupled inductor based high step up boost converter (CIHBC). This is achieved by half cycle resonating branch utilizing inductance of coupled inductor. Further, applying the concept, a coupled inductor boost converter is proposed for achieving high step-up ratio with low switch current and voltage stress. The operation of the proposed converter using resonating branch is discussed in both continuous and discontinuous conduction mode. The theoretical findings are verified through simulation study in PSIM 9.1.1. A prototype converter of 100W output power is designed to prove the concept and for performance analysis of the proposed converter.**

***Index Terms*— Current Stress, Coupled Inductor, High Step-up Boost Converter**

I. Introduction

Currently high step-up DC-DC converters are widely used as an interface converter in renewable sources like photovoltaic (PV), fuel cell and in energy storage system [1]-[3]. Conventional boost converters are not suitable in these applications as extreme high duty-ratio is required [4] to meet the high gain, which increases the conduction loss. Again, at high duty ratio, the problem of diode reverse recovery and electromagnetic interference (EMI) increases significantly [5]. Therefore, to achieve high step-up ratio and efficiency at low duty cycle, there are many boosting techniques like switched capacitor, voltage multiplier cell, interleaved structures has been proposed [6-7]. However, all these voltage lifting techniques suffer from large number of capacitor and power diode usage, which increases the loss and degrades efficiency.

In recent years, coupled inductor based boosting technique [8-9] has emerged utilizing magnetic coupling and has promising two-degree solution of voltage lifting. But the leakage inductance creates voltage spikes and increases the switch voltage stress. Active and passive clamp based coupled inductor boost converter circuit eliminates voltage spikes due to leakage inductance [10-11]. The application of voltage multiplier cell and switched capacitor cell in coupled inductor-based boost converter are also found in literature to minimize the leakage inductance effect with further enhancement in voltage gain [12-13]. But the input current ripple of these converters is high, which makes difficult to track maximum power point (MPP) in PV application. Interleaving technique in coupled inductor-based boost converter minimize input current ripple [14]. Therefore, various high step-up coupled inductor based boost converter topologies evolved which ensures high efficiency operation with low input current ripple [15-21]. But all these topologies use two current paths during switch "*ON*" time to store energy either in inductor or in capacitor or both. Even though the rms current is small, the cumulative current through the switch creates extremely high peak current at the beginning or at the end of the turn '*ON*' time of the switch. An example implementation of such topology is shown in Fig. 1 (a) [19], where there are two current paths during the main switch '*ON*' time. This creates large switch current stress at the end of switch '*ON*' time. Such high current stress is a common problem to all high step-up coupled inductor boost converter [22]. This is one of the major reasons of non-reliable converter operation and fault. In addition, this requires an expensive high current rating device. Considering this problem, an extra L-D network-based solution is proposed in Fig. 1(b) [24], where the peak of the current at the end of the switch '*ON*' time is reduces significantly, as shown in Fig. 1 (c).

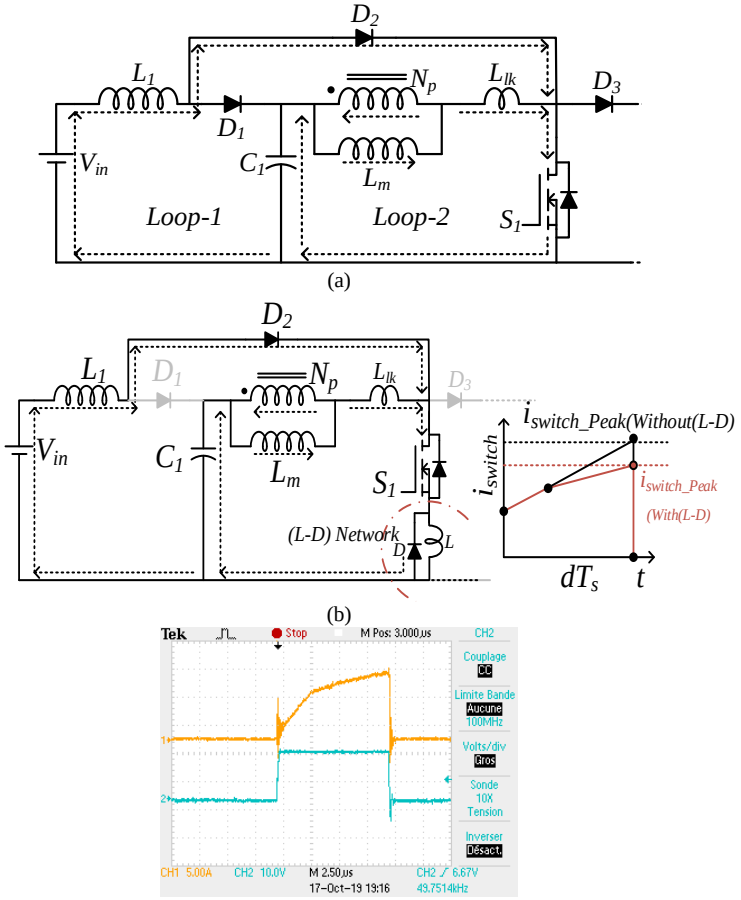

Fig. 1. Converter configuration of (a) switch '*ON*' time circuit by S.-M. Chen *et al.* [19] (b) modified circuit proposed by TR Choudhury *et al.* [24], and (c) Main Switch current [24].

However, this technique suffers from generality as well as it degrades converter voltage gain and efficiency. The energy trapped during switch '*ON*' time in extra L-D network is wasted during switch '*OFF*' time. This reduces the efficiency and also increases the component counts.

In this paper a generalized half cycle resonating branch utilizing coupled inductor is proposed to minimize switch current stress. No extra components are used in modifying the coupled inductor circuit topology. This technique requires modification in existing topologies in literature. Finally, a coupled inductor boost converter is proposed using resonating branch which effectively improve voltage gain, efficiency and switch current stress.

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II. Circuit Topology For Switch Current Stress Reduction

The switch current stress reduction (SCSR) technique can be achieved by changing existing circuit topology and without adding any extra circuit element and keeping the good traits of the original circuit. The high step-up coupled inductor-based boost converters have common interlink, which provides multiple energy storing path during switch '*ON*' time. Minimum two current paths are utilized to achieve high boosting factor as proposed in shown in Figs. 2 (a) & (b) [21] and [22] respectively.

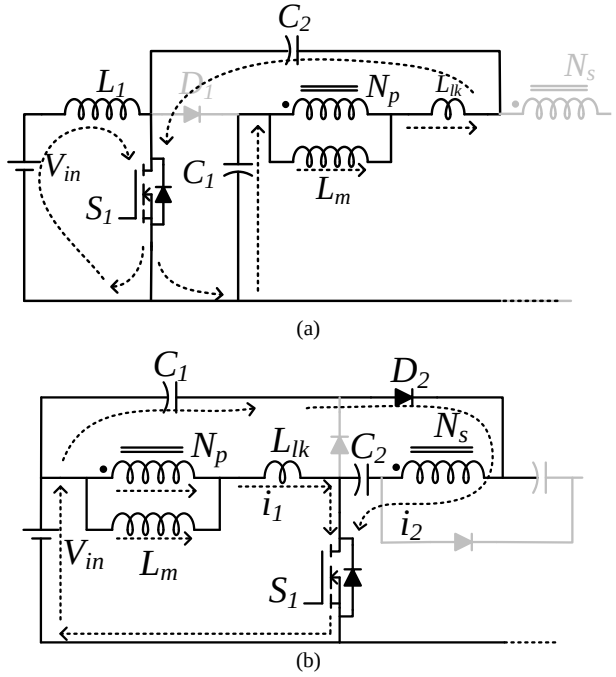

Fig. 2. Converter configuration of (a) switch '*ON*' time circuit by Y. Zheng *et al*. [22], and (b) switch '*ON*' time circuit by Y. Hsieh *et al*. [21].

Generally, all the coupled inductor-based boost converters in literature follow increasing switch current during '*ON*' time as shown in Fig. 3 (a). The increment in the current slope during '*ON*' time can be restricted by using L-D branch [24] in series with the main switch as shown in Fig. 3 (a) and (b).

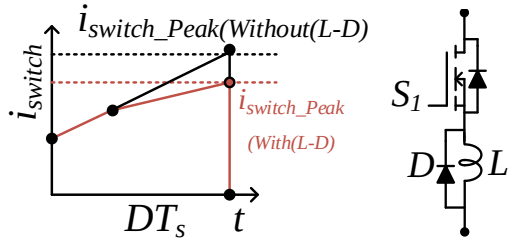

Fig. 3. Typical switch current waveform (a) with and without L-D network, and (b) main switch with L-D network.

But in this approach, the main problem is the energy stored during on time is entirely wasted in the diode and inductor. In addition, to limit switch current stress below critical level inductor (L) size should be high. High inductor value can limit rise of switch current but increased ½ Li^2 energy and I^2R loss in the L-D loop degrade the voltage gain and efficiency.

The alternative solution to this problem is to shape the second loop current so that the peak switch current can be minimized. For this capacitor used in second loop can be utilized. In this article half cycle resonating branch is used to store energy during '*ON*' time as shown in Fig. 4 (a) & (b). In this approach the second loop current follow sinusoidal pattern and its maximum value depends on the values of loop elements. Two capacitors (C_1, C_2) diode (D_2) switch (S_1) and coupled inductor secondary inductance (L_2) during '*ON*' time forms a resonating branch. Capacitor C_1 make diode D_2 forward biased assisted by secondary inductance (L_2) and capacitor C_2 stores energy. This branch continues to circulate current through main switch till diode D_2 is forward biased or main switch is '*ON*'. The current equation i_2 can be derived as,

$$i_2 = v_{C_1}\sqrt{\frac{C_{eq}}{L_2}}\sin(\omega_r t) \text{ where } C_{eq} = \frac{C_1 C_2}{C_1 + C_2}, \quad (1)$$

$$T_r = \frac{1}{\omega_r} = 2\pi\sqrt{L_2 C_{eq}} \text{ and } t_r = \pi\sqrt{L_2 C_{eq}}$$

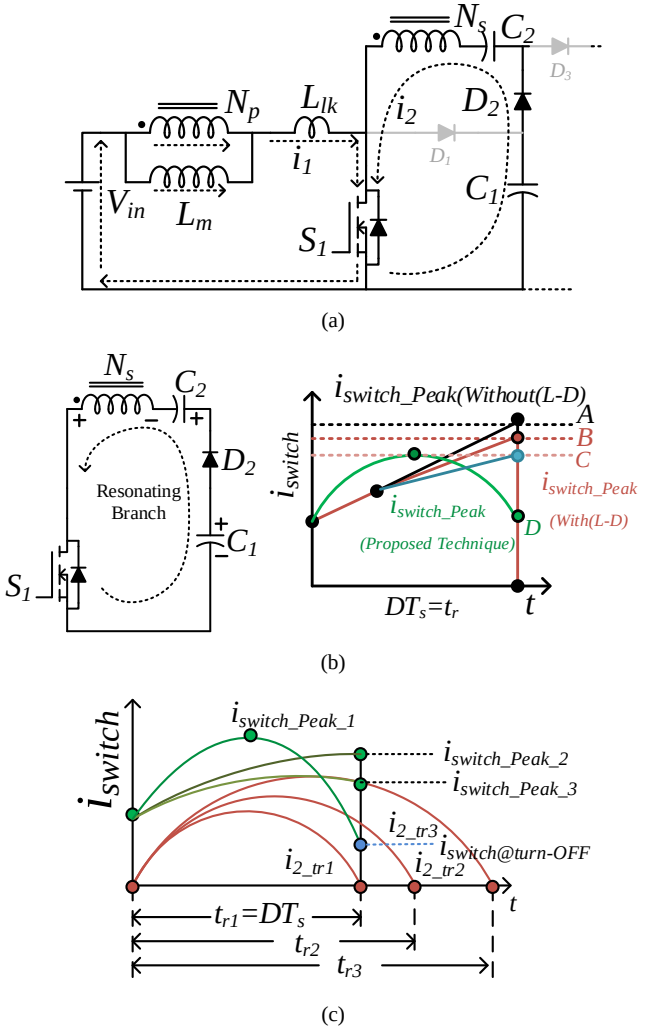

Fig. 4. Proposed circuit solution: (a) switch 'ON' time converter circuit, (b) resonating branch and switch current waveform, and (c) switch current waveform with resonating current characteristics.

Now, if switch '*ON*' time DT_s is made equal to t_r (half cycle resonating time) or vice versa, the switch current value is minimum at turn '*OFF*' instant and current stress ($i_{switch\_peak\_1}$) reduction range starts as shown in Fig. 4 (c).

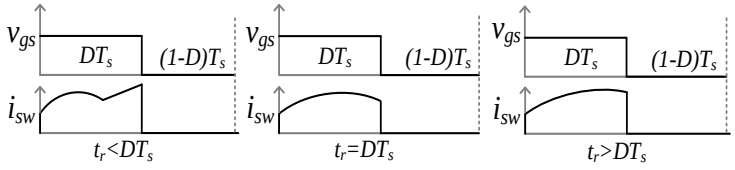

Fig. 5. Switch current stress for different resonating time (t_r) with respect to switch '*ON*' (DT_s) time.

Current stress reduction further improves i.e. $i_{switch\_peak\_3} < i_{switch\_peak\_2} < i_{switch\_peak\_1}$ for $t_r > DT_s$ as shown in Fig. 4 (c). But if $t_r < DT_s$ the switch current stress reduction fails and

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current stress behaviour resembles to fly back converter as shown in Fig. 5. For very low t_r value voltage gain drops rapidly as sufficient energy could not be stored during the switch '*ON*' time. Thus, in proposed technique designing t_r value is important to maintain low switch current stress. The proposed technique can be applied to any coupled inductor based high step-up boost converter after topological modification. Applying the circuit concept, a new coupled inductor based high step-up boost converter is proposed as shown in Fig. 6.

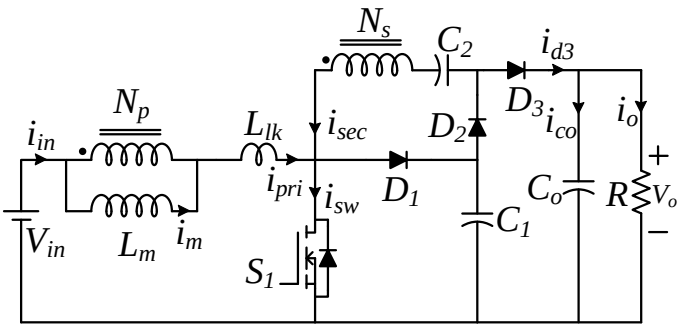

Fig. 6. Proposed coupled-inductor based boost (PCB) converter using resonating branch.

III. Proposed Converter Operation

The proposed converter as shown in Fig. 6 comprises of one coupled inductor, three diodes, three capacitors and a power electronic switch. The coupled inductor is modelled as ideal transformer with magnetizing inductance L_m and leakage inductance L_{lk}. In order to simplify the analysis, the following conditions are assumed.

(a) The capacitor voltage ripple is considered to be small and negligible.
(b) All power electronics switches are considered to be ideal.
(c) The coefficient of coupling (k) of coupled inductor is considered as $\frac{L_m}{L_m + L_{lk}}$ and the turns ratio is $n = \frac{N_s}{N_p}$

The analysis of the converter is done in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) discussed below.

A. CCM Operation

The operating principle of the proposed converter is divided into four modes as per power flow in CCM. Fig. 7 shows the key waveforms of the proposed converter and Fig. 8 indicates the circuit diagram of each mode.

Mode 1 [t_0-t_1]: In this mode the main switch (S_1) is '*ON*' and capacitor C_1 is discharging through D_2, C_2, and S_1. The discharging current is i_{sec} as shown in Fig. 8 (a). The current will circulate till D_2 is in forward biased. The leakage inductance is negligible compared to magnetizing inductance. The constant load current is supplied by the output capacitor C_0. The magnetizing current (i_m) increased gradually. The switch current is the summation of discharging current (i_{d2}) and primary current (i_{pri}) as shown in Fig. 8 (a). In this mode the voltage and current equation can be written as,

$$v_{in} = v_{Lm} + v_{lk} \tag{2}$$

$$v_{c_2} = n v_{Lm} + v_{c_1} \tag{3}$$

$$-i_{c_1} = i_{c_2} = i_{sec} = v_{c_1}\sqrt{\frac{C_{eq}}{L_2}}\sin(\omega_r t) \tag{4}$$

Where, $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$, $T_r = \frac{1}{\omega_r} = 2\pi\sqrt{L_2 C_{eq}}$ and $t_r = \pi\sqrt{L_2 C_{eq}}$

$$i_{in} = i_{primary}\,,\ -i_{c_0} = i_0 \tag{5}$$

$$i_{sw} = i_{pri} + i_{sec} = i_m + (n+1) i_{sec} \tag{6}$$

Mode 2 [t_1-t_2]: At t_1 the main switch (S_1) is OFF. The polarity of V_{lk} changes which make D_1 forward bias and energy stored in the leakage inductance (L_{lk}) is transferred to capacitor C_1 in this mode [2]. The load current is supplied by the output capacitor C_0. In this mode the voltage across C_2 is constant.

$$v_{in} + v_{Lm} + v_{lk} = v_{c_1} \tag{7}$$

The time of released energy [2] $t_{c1}=t_3-t_1=2(1-D)/(n+1)$ (8)

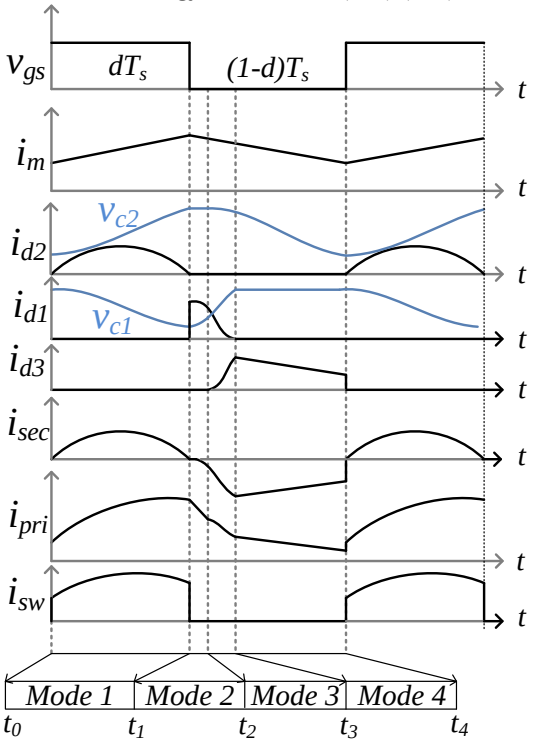

Fig. 7. Key waveform of proposed converter in CCM.

Mode 3 [t_2-t_3]: This mode starts after t_2. The current through diode D_1 starts decreasing and D_3 is in forward biased in this mode. The output capacitor C_0 is in charging mode. Magnetizing current starts decreasing. D_2 is reversed biased. Capacitor C_2 starts discharging through D_3 to the load. Voltage across capacitor C_1 is rising till D_1 is forward biased. The voltage and current equations in this mode are

$$v_{in} + v_{Lm} + v_{lk} = v_{c_1} \tag{9}$$

$$v_{c_1} + n v_{Lm} + v_{c_2} = v_0 \tag{10}$$

$$i_{d_3} = i_{sec} = i_{c_0} + i_0 \tag{11}$$

$$i_{pri} = i_{sec} + i_{c_1} \tag{12}$$

Mode 4 [t_3-t_4]: This mode starts after t_3. In this mode diode D_1 is reverse biased. Capacitor (C_0) is in charging condition. Magnetizing current (i_m) falls at a constant rate. The diode D_3 current is same as coupled inductor secondary current (i_{sec}). The diode D_3 current (i_{d3}) is the summation of capacitor current and load current. In this mode voltage and current equations are,

$$v_{c_1} + n v_{Lm} + v_{c_2} = v_0 \tag{13}$$

$$i_{d_3} = i_{sec} = i_{c_0} + i_0 \tag{14}$$

$$i_m - n i_{sec} = i_{pri} \tag{15}$$

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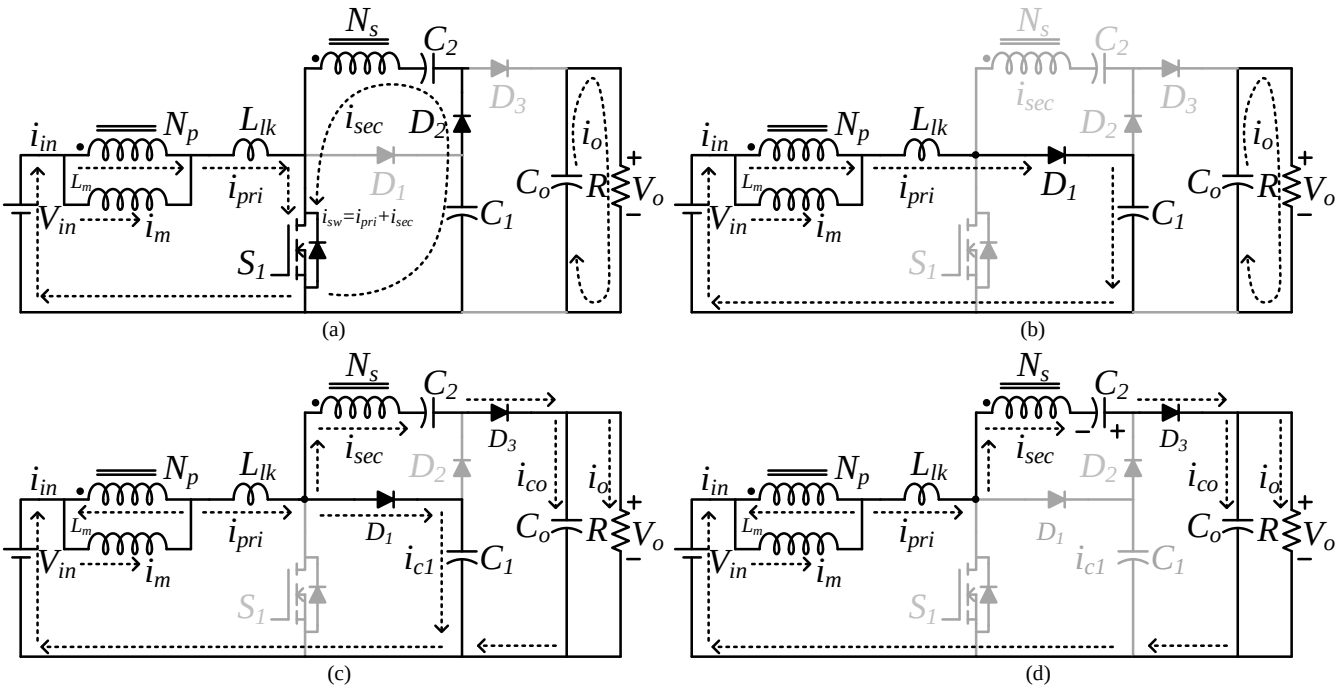

Fig. 8. Operation of proposed converter in CCM: (a) Mode 1 [t_0-t_1] (b) Mode 2 [t_1-t_2] (c) Mode 3 [t_2-t_3] (d) Mode 4 [t_3-t_4].

B. DCM Operation

The operating mode of the converter in discontinuous mode in a switching cycle is shown in Fig. 9 through key waveforms. There are five modes in a switching period (T_s).

Mode 1 [t_0-t_1]:

This mode starts when main switch is '*ON*' as shown in Fig. 8(a). The magnetizing current (i_m) is increasing linearly. The discharging current (i_{d2}) flows from C_1 , C_2, D_2 and S_1.This current charges capacitor C_2. This current flows till diode D_2 is forward biased.

Mode 2 [t_1-t_2]:

This mode starts when main switch is turned '*OFF*', diode D_2, D_3 are reverse biased. The stored energy in leakage inductance is transferred to capacitor C_1 through diode D_1. This mode ends when D_3 starts conducting and current through C_1 starts decreasing. Magnetizing current (i_m) decreases linearly.

Mode 3 [t_2-t_3]:

In this mode current through C_1 starts falling and D_3 is in conduction. D_2 is reverse biased as shown in Fig. 8 (c). Capacitor C_2 starts discharging through D_3 to load.

Mode 4 [t_3-t_4]:

In this mode capacitor C_2 is fully discharged and magnetizing current (i_m) falls to zero value as shown in Fig. 8(d)

Mode 5 [t_4-t_5]:

In this mode the load current is supplied by the output capacitor C_0. The primary current as well as magnetizing current is zero. All diodes are turned '*OFF*' in this mode.

IV. Proposed Converter analysis In Steady State

A. Voltage Gain in CCM and DCM:

In mode 1 form Fig. 8(a) the following voltage equations are obtained where V_{Lm}, V_{Lk}, V_{L2} are primary voltage, leakage inductance voltage and secondary voltage respectively.

$$v_{\mathrm{Lm}} = v_{\mathrm{L1}} = \frac{L_{\mathrm{m}}}{L_{\mathrm{m}}+L_{\mathrm{lk}}} v_{\mathrm{in}} = k v_{\mathrm{in}} \tag{16}$$

$$v_{\mathrm{Lk}} = \frac{L_{\mathrm{lk}}}{L_{\mathrm{m}}+L_{\mathrm{lk}}} v_{\mathrm{in}} = (1-k) v_{\mathrm{in}} \tag{17}$$

$$v_{\mathrm{L2}} = nk v_{\mathrm{in}} \tag{18}$$

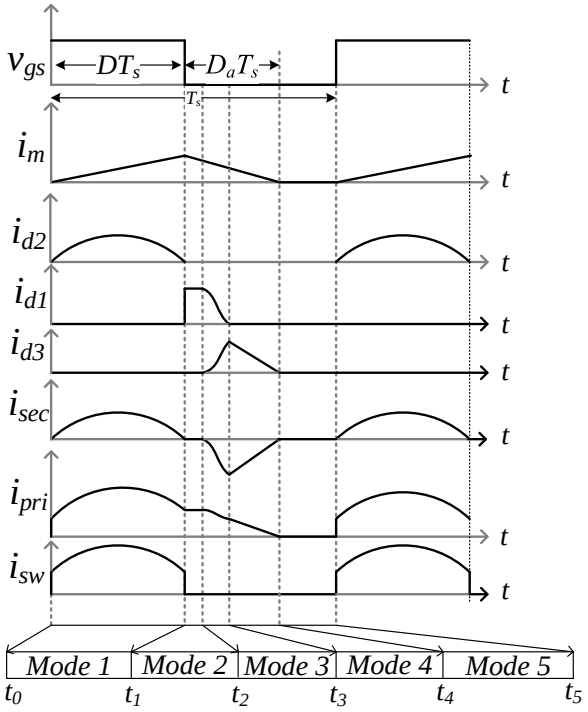

Fig. 9. Key waveform of proposed converter in DCM:

Applying volt-sec balance in coupled inductor primary and secondary inductance the output voltage and capacitor voltage equation is derived in CCM.

$$v_{C_1} = \frac{2\mathrm{D}(k\text{-}1)+(2\text{-}k)}{1\text{-D}} v_{\mathrm{in}} \tag{19}$$

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$$v_{C_2} = \left(nk + \frac{2D(k\text{-}1)+(2\text{-}k)}{1\text{-}D} \right) v_{in} \tag{20}$$

$$v_{C0} = v_0 = \frac{nk+4D(k-1)+2(2-k)}{1\text{-}D} v_{in} \tag{21}$$

Taking coefficient of coupling k=1, the voltage gain of the proposed converter in CCM is derived from equation. (21).

$$M_{CCM} = \frac{v_o}{v_{in}} = \frac{n+2}{1\text{-}D} \tag{22}$$

$$v_{C_1} = \frac{v_{in}}{1\text{-}D},\ v_{C_2} = \left(n + \frac{1}{1\text{-}D} \right) v_{in} \tag{23}$$

The converter voltage gain (M_{CCM}) is shown in Fig. 10 for different coefficient of coupling (k).

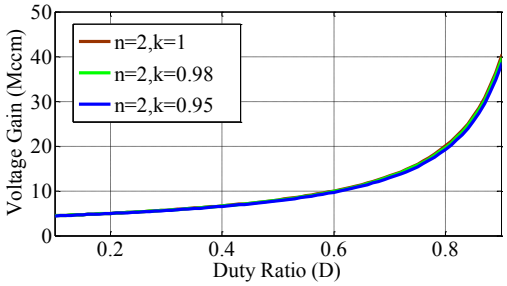

Fig. 10. Voltage gain of proposed converter in CCM for different coefficient of coupling (k)

The voltage gain (M_{CCM}) in CCM is compared with other existing topologies in literature as shown in Fig. 11.

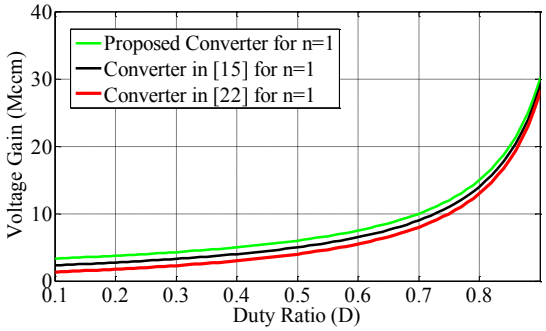

Fig. 11. Voltage gain comparison of converter in CCM @k=1 and n=1

Similarly, the voltage gain in DCM mode can be derived for k=1,

$$M_{DCM} = \frac{(n+2)(D+D_a)}{D_a} \tag{24}$$

From (24) the duty cycle D_a can be derived which is,

$$D_a = \frac{v_{in}(n+2)D}{v_{in}(n+2)\text{-}v_o} \tag{25}$$

From the voltage gain in DCM the boundary condition between CCM and DCM can be derived which is shown in Fig. 12. The voltage gain (24) in DCM can be rewritten as,

$$M_{DCM} = \frac{n+2}{2} + \sqrt{\frac{(n+2)^2}{4} + \frac{D^2}{2\tau_{Lm}}} \tag{26}$$

$\tau_{Lm} = \frac{L_m}{RT_s}$ is the magnetizing inductor normalized time constant.

Therefore, the time constant at boundary condition (D_a=1-D) is,

$$\tau_{Lmb} = \frac{D(1\text{-}D)^2}{2(n+2)^2} \tag{27}$$

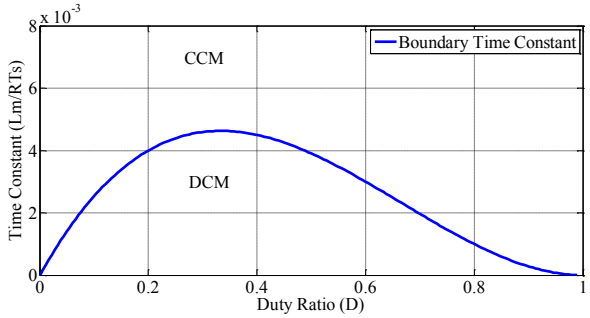

Fig. 12. Boundary condition of the converter at n=2

B. Voltage Stress in CCM:

The switch voltage stress (V_{sw}) of the converter is

$$v_{Sw} = \frac{v_{in}}{1\text{-}D} = \frac{v_0}{n+2} \tag{28}$$

Similarly, the diode voltage stress converter is

$$v_{D1} = \frac{v_0}{n+2} \text{ and } v_{D2} = v_{D3} = \frac{n+1}{n+2} v_0 \tag{29}$$

The comparison of voltage stress is listed in Table-I.

TABLE I
COMPARISON OF VOLTAGE STRESS

	Proposed	[15]	[22]	[25]
Switch Voltage	$\frac{v_0}{n+2}$	$\frac{n+M}{(1+2n)M} v_0$	$\frac{n+1+M}{(n+2)M} v_0$	$\frac{n+M}{(n+1)M} v_0$
Diode voltage	$\frac{n+1}{n+2} v_0$	$\frac{n(n+M)}{(1+2n)M} v_0$	$\frac{(n+1)(n+1+M)}{(n+2)M} v_0$	$\frac{n(n+M)}{(n+1)M} v_0$

Therefore, low voltage switch rating can be selected which has low on state resistance and conduction loss can be minimized. The comparison of normalized switch voltage stress is shown in Fig. 13. The switch voltage stress of the converter is less.

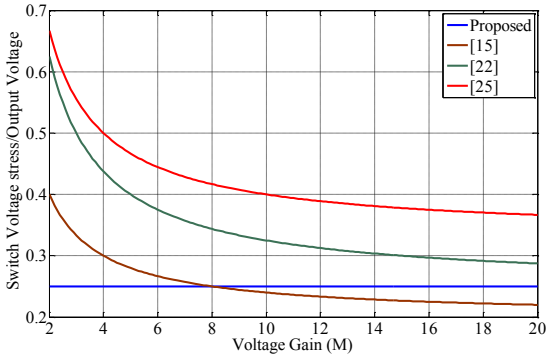

Fig. 13. Switch voltage stress comparison of converter in CCM @k=1 and n=2

C. Current Stress in CCM:

By applying the charge balance for the output capacitor (C_o) the average magnetizing current can be derived in CCM.

$$i_m = \frac{v_o(n+1)}{(1\text{-}D)R} = \frac{v_{in}(n+1)(2+n)}{(1\text{-}D)^2 R} \tag{30}$$

The peak value of the magnetizing current (i_{Lm}) is

$$i_{m\_Peak} = i_m + \frac{\Delta i_m}{2} = \frac{v_{in}(n+1)(2+n)}{(1\text{-}D)^2 R} + \frac{v_{in} DT_s}{2L_m} \tag{31}$$

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Therefore, the average switch current (i_{sw}) during ON time is

$$i_{sw} = i_m + (n+1)i_{sec} = \frac{v_{in}(n+1)(2+n)}{(1\text{-}D)^2 R} + (n+1)i_{sec} \quad (32)$$

Where $i_{sec} = i_2 = \frac{v_{in}}{1-D}\sqrt{\frac{C_{eq}}{L_2}}\sin\left(\frac{1}{\sqrt{L_2 C_{eq}}}t\right)$

As discussed earlier if the resonating current (i_{sec}) value is maintained zero at the end of ON time i.e. $DT_s = \pi\sqrt{L_2 C_{eq}} = t_r$, then the switch current (i_{sw}) value is minimum at turn OFF instant and switch current stress reduction range starts. The switch current at switch OFF transition will be same as peak current of magnetizing current (i_{Lm}) as shown in Fig. 14.

$$i_{sw}\big|_{t=DT_s} = \frac{v_{in}(n+1)(2+n)}{(1\text{-}D)^2 R} + \frac{v_{in}DT_s}{2L_m} \quad (33)$$

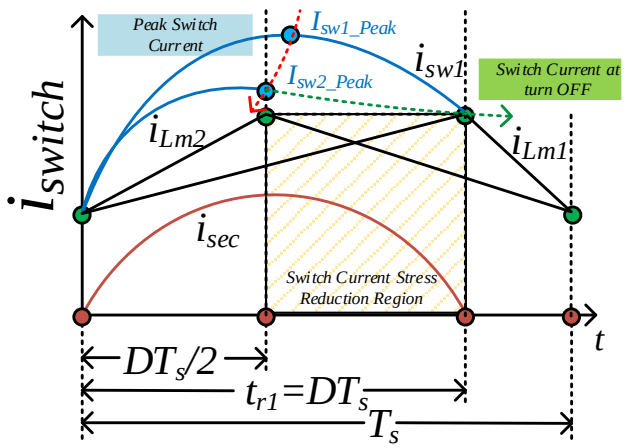


Fig. 14. Switch current stress reduction region of converter in CCM

From the Fig. 14 it is clear that switch current value at turn OFF time is minimum when $t_{r1}=DT_s$ as i_{sec} is zero and the peak switch current can be minimized within $DT_s/2 \le t \le DT_s$.

This is the operating region where switch current stress can be effectively minimized. As discussed in Section-II, in this technique no extra circuit element is used and it do not reduce voltage gain and efficiency of the converter.

Applying analytical method in the equivalent circuit shown in Fig. 8 (a) the switch current of the proposed converter can be derived. The switch current (i_{sw}) is

$$i_{sw}(t) = \frac{v_{in}}{L_m + L_{lk}}t + \frac{L_m}{L_m + L_{lk}} i_m(t) + \frac{v_{in}}{1-D}\sqrt{\frac{C_{eq}}{L_2}}\sin\left(\frac{1}{\sqrt{L_2 C_{eq}}}t\right) \quad \text{for } t>0 \quad (34)$$

The value of the switch current is minimum at $t_r = DT_s$. For duty ratio of 0.7, $t_r = 0.7T_s$ is the point where the switch current value at turn off instant is minimum. The effective peak switch current minimization starts from $0.25T_s$ to $0.7T_s$ as shown in Fig. 15. This region is the effective switch current stress reduction region using secondary resonating branch.

This technique is compared with L-D based solution [24] in p.u. From the Fig. 15 it is clear that switch current stress can be minimized using proposed technique.

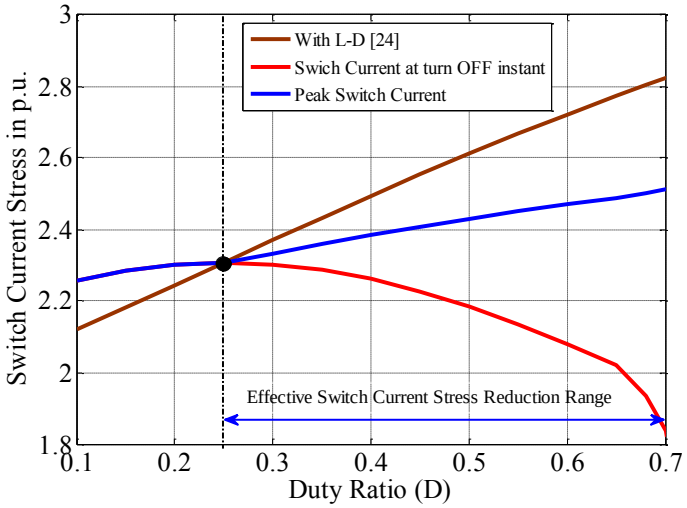
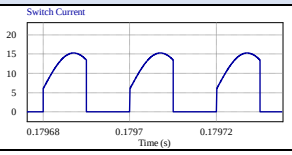
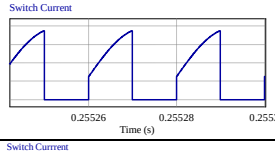
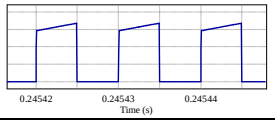


Fig. 15. Switch current stress comparison with L-D based solution [24].

The advantages of the proposed technique over L-D based solution are (a) Switch current reduction in the higher duty-ratio operating region, (b) no extra circuit element, (c) no adverse effect on the voltage gain and efficiency.

Switch current stress comparison of single switch coupled inductor-based boost converter is shown in Table-II.

TABLE II
COMPARISON OF SWITCH CURRENT STRESS

Topology	Peak Switch Current	Switch RMS Current	Current Waveform	Switch Selection @ 200W	SCSR
Proposed	$\cong \frac{v_{in}(n+1)(2+n)}{(1\text{-}D)^2 R} + \frac{v_{in}}{1-D}\sqrt{\frac{C_{eq}}{L_2}}$	$\cong \frac{(n+2)\sqrt{D}}{(1\text{-}D)} i_o \sqrt{1+\frac{1}{12}\left(\frac{\Delta i_m}{i_o}\right)^2\left(\frac{1-D}{n+3}\right)^2}$		FQP34N20 V_{ds}=200V, R_{ds}=0.075Ω Id=31A.	YES
[15]	$\frac{v_{in}(n+1+nD)^2}{(1\text{-}D)^2 R} + \frac{v_{in}DT_s}{2L_m}$	$\approx \frac{(1+n+nD)\sqrt{D}}{(1\text{-}D)} i_o \sqrt{1+\frac{1}{3}\left(\frac{\Delta i_m}{i_o}\right)^2\left(\frac{1-D}{1+n+nD}\right)^2}$		IRFB4410ZPBF V_{ds}=100V, R_{ds}=0.072Ω Id=97A	NO
[22]	$\frac{v_{in}(1+(n+1)D)^2}{(1\text{-}D)^2 R} + \frac{v_{in}(n+1)(1+(n+1)D)}{(1\text{-}D)R} + \frac{v_{in}DT_s}{2L_m} + \frac{v_{in}DT_s}{2L_1}$	$\approx \frac{(n+2)\sqrt{D}}{(1\text{-}D)} i_o$		IPA075N15N3 V_{ds}=150V, R_{ds}=0.0075Ω Id=43A.	NO

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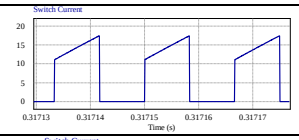
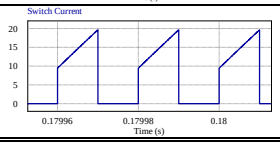
[25]	$\frac{v_{in}(1+nD)^2}{(1-D)^2R}+\frac{v_{in}n(1+nD)}{(1-D)R}+\frac{v_{in}DT_s}{2L_m}+\frac{v_{in}DT_s}{2L_l}$	$\cong\frac{(n+1)\sqrt{D}}{(1-D)}i_o\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_m}{i_o}\right)^2}$		FQP34N20 V_{ds}=200V, R_{ds}=0.075Ω Id=31A.	NO
[24]	$\frac{v_{in}(1+nD)}{(1-D)^4R}+\frac{v_{in}(n+1)(1+nD)}{(1-D)^3R}+\frac{v_{in}DT_s}{2(1-D)L_m}+\frac{v_{in}DT_s}{2L_l}$	$\approx\frac{(nD+n+2)\sqrt{D}}{(1-D)}i_o\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_m}{i_o}\right)^2}$		IRF640 V_{ds}=200V,R_{ds} =0.18Ω Id=18A.	YES

The comparison of other coupled inductor based converter with current proposal is performed at 200W. The base current for normalizing process is considered as 6 A. The peak switch current without L-D circuit [19] at 0.5 duty ratio and 200 W condition is 19.6 A. The same peak switch current is decreased to 15.6A using L-D based circuit where L value is 12µH and converter operated at 50 kHz. The magnetizing inductance is 75µH.

The operating condition of the proposed converter should be $t_r>DT_s$ to minimize switch current stress effectively as shown in Fig. 15. Therefore, to meet switch current stress reduction range up to 0.7 duty ratio, the critical condition is $0.7Ts=t_r$. For switching frequency 50 kHz the half cycle resonating time (t_r) is 14µSec. The secondary side inductance (L_r) is 1.78µH and therefore the C_r value can be derived from $t_r=\pi\sqrt{L_rC_r}$ which is 11µF. The capacitor values of C_1, C_2 are selected to be 25µF and 20µF to meet $C_r=\frac{C_1C_2}{C_1+C_2}$. With these values simulation study is performed to verify switch current stress reduction range and compare with L-D based solution as mentioned in Fig. 15 and Table-II.

D. RMS Current Comparison:

The proposed half cycle resonant branch utilizing coupled inductor inductance does not increase the RMS value of the switch current. This can be theoretically demonstrated through graphical as well as mathematical formulation from switch current waveform as shown in Fig. 16.

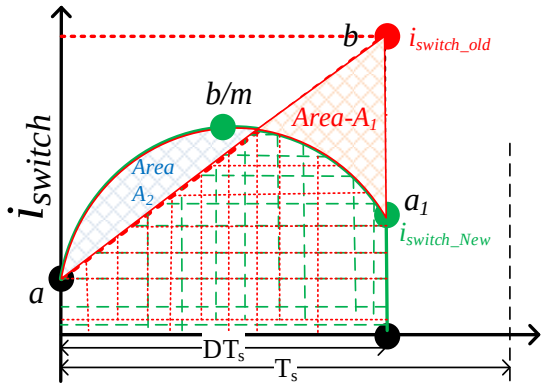


Fig. 16. Switch current waveform of conventional [19] and proposed converter during turn- 'ON' time.

In Fig.16, the modified current waveform can be approximated as shifted sinusoidal waveform compared to trapezoidal shape for conventional converter [19], [15], and [22] as shown in Fig.16. The area A_1 in Fig. 16 is the reduction whereas area A_2 is the addition. Assuming the peak current is reduced by factor 'm' where 'a' and 'a_1' are approximately same, the expression for RMS current for the modified waveform is given by,

$$I_{1rms}=\sqrt{D\left(a^2+\frac{1}{2}\left(\frac{b}{m}-a\right)^2+\frac{4a}{\pi}\left(\frac{b}{m}-a\right)\right)} \quad (35)$$

And for the existing trapezoidal wave the RMS current is

$$I_{2rms}=\frac{1}{\sqrt{3}}\sqrt{D\left(a^2+ab+b^2\right)} \quad (36)$$

Therefore, for lower value of RMS current in the proposed waveform,

$$I_{2rms}\geq I_{1rms} \quad (37)$$

From, the inequality criterion of (37) the peak current scaling factor (m) value can be mathematically derived which is 1.22. Therefore, 19 % reduction in peak current confirms equal RMS current or less as per Fig. 16. However, the starting point of switch current value 'a' is usually more in existing schemes compared to current proposal as shown in Table-II, which can be more advantageous. On the other hand, if ending point 'a_1' is higher from 'a' the reduction factor may increase from 1.22 value. Thus, it can be inferred that the RMS value of current for the existing scheme can be definitely reduced as the peak current is usually reduced by more than 20% from the existing schemes.

E. Diode, Capacitor and Coupled Inductor Winding Current:

Diode average, RMS currents can be calculated from Fig. 7 in CCM. The average value (38) of the diode D_3 is same as average load current (I_o).

$$i_{d3}=i_o \quad (38)$$

The RMS value of diode D_3 is

$$i_{d3}=i_{sec}\sqrt{1\text{-}D\text{-}D_b} \quad (39)$$

Where D_b is derived from charge balance equation of simplified capacitor current waveforms shown in Fig. 17.

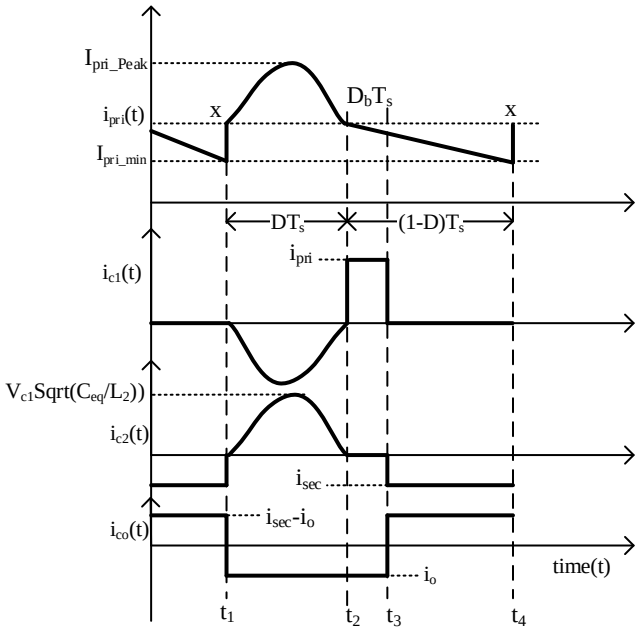


Fig. 17. Simplified capacitor current waveform and primary winding current of coupled inductor.

$$D_b=\frac{v_{c1}D}{2\pi i_o}\sqrt{\frac{C_{eq}}{L_2}}\left(1-\cos\left(2\pi D\right)\right)\times\left(\frac{1-D}{n+2}\right) \quad (40)$$

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The average and RMS current of diode D_2 is derived as shown in equation (41) and (42) respectively.

$$i_{d2(avg)} = \frac{v_{c1}}{\pi}\sqrt{\frac{c_{eq}}{L_2}} \tag{41}$$

$$i_{d2(RMS)} = \sqrt{\frac{1}{T_s}\int_0^{DT_s}\left(v_{c1}\sqrt{\frac{c_{eq}}{L_2}}\sin\left(\frac{2\pi}{T_s}t\right)\right)^2 dt} \tag{42}$$

The average and RMS current of diode D_1 is derived as shown in equation (43) and (44) respectively.

$$i_{d1(avg)} \cong \frac{n+2}{1\text{-}D} i_0 D_b \tag{43}$$

$$i_{d1(RMS)} \cong \frac{n+2}{1\text{-}D} i_0 \sqrt{D_b} \tag{44}$$

The RMS current (45) of the primary winding of the coupled inductor is given by

$$i_{pri(RMS)} = \sqrt{\left[\begin{array}{l}(x^2 + x(x - I_{pri\_min})(1-D) + \frac{(x - I_{pri\_min})^2}{3}(1-D) + \\ + \frac{v_{c1}}{\pi}\sqrt{\frac{c_{eq}}{L_2}}(1-\cos(2\pi D)) + \frac{v_{c1}^2}{2\pi^2}\frac{c_{eq}}{L_2}D - \frac{\sin 4\pi D}{4\pi})\end{array}\right]} \tag{45}$$

Where, $x \cong \frac{n+2}{1\text{-}D} i_0$

Similarly, RMS current (46) of the secondary winding of the coupled inductor is given by

$$i_{sec(RMS)} = \sqrt{i_{sec}^2 \times (1\text{-}D\text{-}D_b) + \frac{v_{c1}^2}{2\pi^2}\frac{c_{eq}}{L_2}D - \frac{\sin 4\pi D}{4\pi}} \tag{46}$$

The RMS current of capacitors C_2, C_1 and C_3 are mentioned in equation (47), (48) and (49) respectively.

$$i_{C_2(RMS)} = \sqrt{i_{sec}^2 \times (1\text{-}D\text{-}D_b) + \frac{v_{c1}^2}{2\pi^2}\frac{c_{eq}}{L_2}D - \frac{\sin 4\pi D}{4\pi}} \tag{47}$$

$$i_{C_1(RMS)} = \sqrt{I_{pri\_min}^2 \times (D_b) + \frac{v_{c1}^2}{2\pi^2}\frac{c_{eq}}{L_2}D - \frac{\sin 4\pi D}{4\pi}} \tag{48}$$

$$i_{C_o(RMS)} = \sqrt{i_o^2 \times (D+D_b) + (i_{sec} - i_o)^2 (1\text{-}D\text{-}D_b)} \tag{49}$$

V. Simulation And Experimental Results

The proposed converter is simulated in PSIM 9.1.1 and tested to check the performance using parameters of 100 W prototype hardware as mentioned in Table-III. The switching frequency is 50 kHz of the proposed converter. The voltage gain of the proposed DC-DC converter changes from ideal gain due to parasitic elements. The voltage gain (50) of the converter taking parasitic elements is,

$$\frac{v_o}{v_{in}} = \frac{\frac{2+n}{1\text{-}D} - \frac{2v_d}{v_{in}}}{1 + \frac{1}{1\text{-}D}\left(A\frac{r_{pri}}{R_L} + B\frac{r_{sec}}{R_L} + C\frac{r_{sw}}{R_L} + D\frac{r_{d1}}{R_L} + E\frac{r_{d2}}{R_L} + F\frac{r_{d3}}{R_L}\right)} \tag{50}$$

Where, the parasitic parameters of the converter are: r_{pri}=18mΩ, r_{sec}=24mΩ, r_{sw}=35mΩ, r_{d1}, r_{d2}, r_{d3}=12mΩ, V_{in}=12V, V_d=0.61V, n=2, R_L=51.84Ω @ 100W and R_L=86.4Ω @ 60W.

The coefficients of voltage gain are:

$$A = \frac{2(2+n)}{1-D},\ B = n^3(1-D) + \frac{n^2(2+n)}{1-D},\ D = \frac{2+n}{1-D},\ F = \frac{2+n}{1-D}$$

$$E = n, \text{ and } C = n(1-D) + \frac{D(2+n)}{1-D}.$$

The voltage gain of the proposed converter is plotted ideally (22) as well as by taking the parasitic values (50) as mentioned and shown in Fig. 18. (a). The practical reading of output voltage is matched with the voltage gain taking parasitic values as shown in Fig. 18 (b).

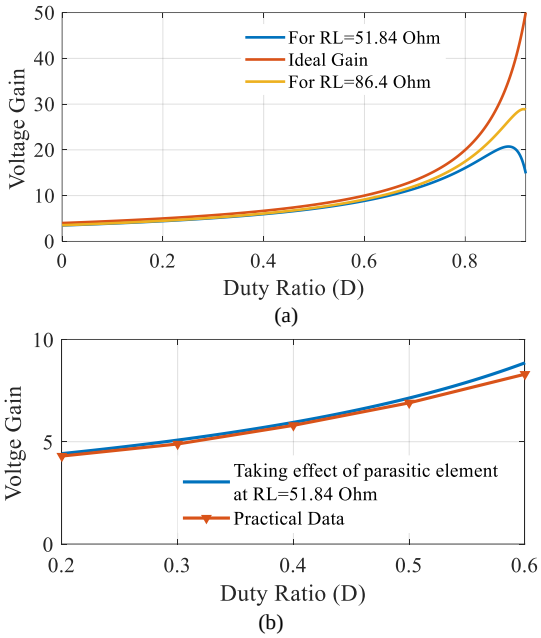

Fig. 18. Proposed DC-DC converter (a) voltage gain taking parasitic values with different load, and (b) voltage gain comparison with parasitic values and practical data.

Duty cycle is from 0.4-0.6 to verify different switch current and stress reduction which is the inherent feature of this converter. The half cycle resonating branch current timing is main important so that for almost entire operating region the switch current reduction is possible without sacrificing the voltage gain and efficiency.

TABLE-III
SIMULATION AND HARDWARE PARAMETERS

Converter Specification		
Input Voltage = 12 V	Power Output = 100 W	Output Voltage = 72 V
Duty Ratio = 0.5	Switching Frequency=50 kHz	Load Resistance = 50 Ω
Design Parameters	**Value**	**Part Number**
Coupled Inductor	L_m = 44 µH, Turns Ratio 25:25 (n = 1), $L_{leakage}$ = 8.26 µH	Ferrite Core PQ 32/30
Switch (S_1)	FQP34N20 (V_{ds} = 200 V, R_{ds} = 0.075 Ω, I_d=31 A.) @ 200W	FQP34N20
Diodes (D_1, D_2, D_3)	FRD	IN5401
Capacitor C_1	10 uF	
Capacitor C_2	1.3 uF	
Capacitor C_o	100 uF	

As discussed in previous section, the converter operation is divided into two main sections i.e. CCM and DCM. The Switch current reduction is tested in CCM as well as in DCM. In CCM the switch current reduction is again divided into three subsections which are (a) $DT_S < t_r$ (b) $DT_S = t_r$ (c) $DT_S > t_r$. In all three modes, the switch current reduction is effectively achieved in (a) $DT_S < t_r$ (b) $DT_S = t_r$ as shown in simulation result in Fig. 19.

Simulation was carried out taking switching time is 20µs. At D = 0.5 and $DT_s = t_r$ the switch current value is minimum at turn OFF instant as shown in Fig. 19 (a).

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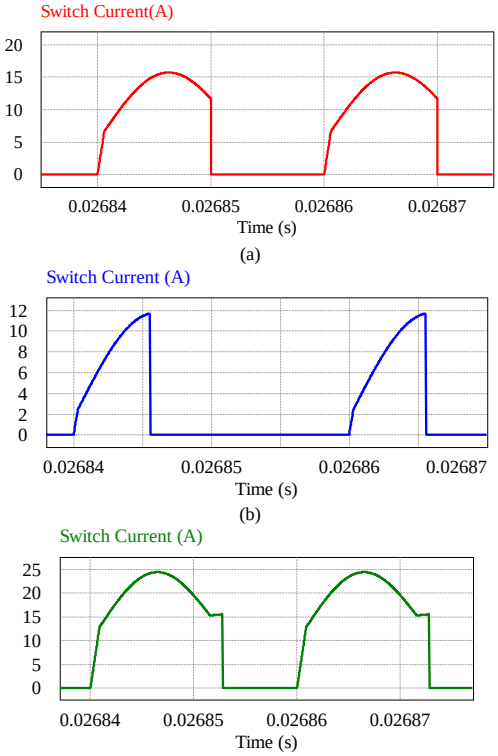
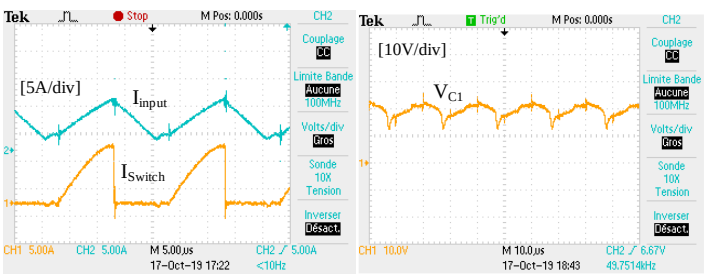
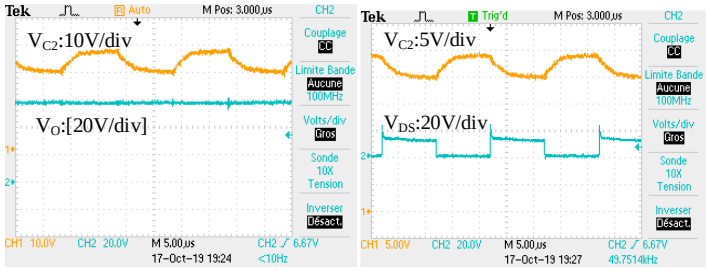


Fig. 19. Switch Current in CCM (a) for [$DT_S = t_r$] (b) for [$DT_S < t_r$] (c) for [$DT_S > t_r$].

For $DT_S<t_r$ the switch current stress is low as shown in Fig. 19 (b) but for $DT_S>t_r$ the switch current stress is almost same with other topologies which is shown in Fig. 19 (c). Therefore, selection of t_r should be such that in the operating duty range i.e. 0.4-0.7 the converter on time is exactly same as t_r or less than t_r. As the switching time is 20µSec. For 0.5 duty ratio at $DT_s = t_r$, the half cycle resonating time is 10 µs. Therefore, from equation, $t_r = \pi\sqrt{L_2 C_{eq}}$ the equivalent capacitor is determined. By increasing the capacitance (C_{eq}) value t_r can be increased. Taking C_1, C_2 10 uF the resonating time is increased to check the switch current during $DT_s < t_r$. condition. Prototype of 100 W converter is designed and tested at 0.5 duty ratio. For 12 V input the switch voltage stress is around 24 V as shown in Fig. 20 (d) for D = 0.5, n = 1 and $DT_s < t_r$. The input current, switch current under this condition is shown in Fig. 20 (a) which shows a good match with the simulation. The capacitor voltages V_{C1} ,V_{C2} are shown in Figs 20 (b) and (c) respectively which matches with calculated value as per equation (23) and simulation.

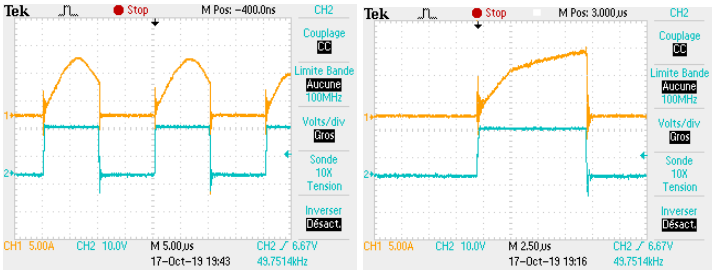


(a). (b)

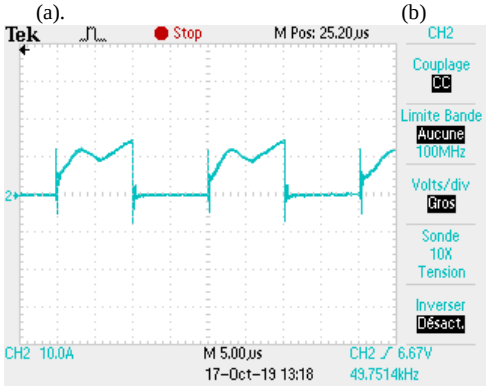


(c). (d)

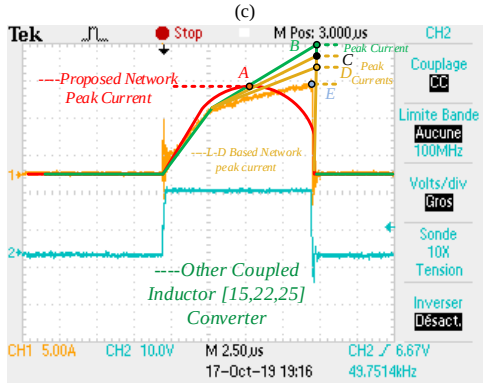
Fig. 20. Proposed Converter operation in CCM at ($DT_S<t_r$) (a) Input current and Switch current (b) Capacitor Voltage V_{c1} (c) Capacitor Voltage V_{c2} and output voltage V_o.(d) Switch voltage V_D.



(a). (b)



(c)



(d)

Fig. 21. Switch current waveform of (a) proposed converter (5A/div) in CCM at $DT_S=t_r$ (b) L-D network (5A/div) solution [24] (c) proposed converter (10A/div) in CCM at $DT_S>t_r$, and (d) comparison of switch current stress [A-Proposed technique peak, B-Peak current of coupled inductor boost, C, D, E-Peak current (5A/div) with increasing inductance value L-D network-based solution.

Again, at C_1 10µF and C_2 at 1.3µF the resonating time t_r can be made exactly same as 10µsec. Therefore, $DT_s=t_r$ can be achieved at 0.5 duty ratio at 50 kHz. At this condition the switch current value at turn OFF instant is minimum but stress is greater than $DTs<t_r$ condition as shown in Fig. 21 (a). For L-D based solution of switch current stress reduction depends on value of inductance. For larger inductance switch current stress is less and same as current proposal as shown (point A, E) in Fig. 21 (d). But for low inductance value the peak switch current is more (Point C, D) than current proposal as shown in Fig. 21 (d). The switch current at turn OFF transient is more compared to current proposal. The prototype converter is designed for

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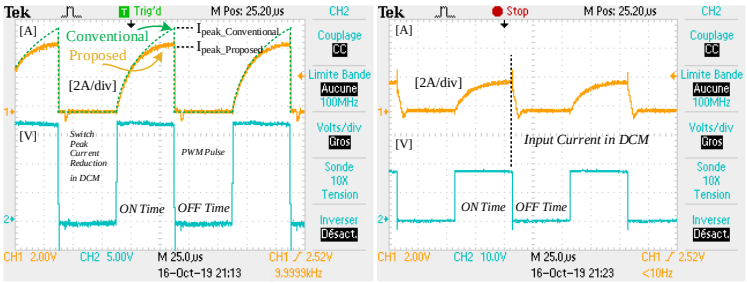
100W. The input voltage is 12V and in the ideal condition the average input current is 100/12=8.33 A. Therefore, the base value of current is considered as 8.5 A for calculation and comparison of peak current in the manuscript. The base inductor value is L_m=44µH as mentioned in Table-III. For comparison with L-D based solution, the converter proposed in [24] is operated at 100W and in same input voltage, duty ratio (D=0.5) where the initial L value is 10.5µH at 50 kHz is mentioned in Table-IV.

TABLE-IV
COMPARISON OF SWICH CURRENT REDUCTION METHOD

L-D Based Solution	Peak Switch Current @ Duty (D)= 0.5	Voltage gain and Efficiency (η) Decrement
For L = 0.24 p.u.	1.5 p.u.	Gain= 5-6%, η=4-5%
For L = 0.14 p.u.	1.8 p.u.	Gain=3-5%, η=3%
For L = 0.10 p.u.	≈2.6 p.u.	Gain= 2-3%, η=2.5%
Current Proposal	Peak Switch Current @ Duty (D)= 0.5	Voltage gain and Efficiency (η) Decrement
At $DT_s=t_r$	1.54 p.u.	No Decrement
At $DT_s<t_r$	1.37 p.u.	No Decrement
At $DT_s>t_r$	2.81 p.u.	Switch current reduction fails

But in the current topology if $DT_s>t_r$ then the current stress reduction fails as shown in Fig. 21 (c). Therefore, designing circuit element of C_1 and C_2 with coupled inductor secondary inductance is very important to achieve true switch current reduction with the operating duty range i.e. 0.4-0.7. The current proposal no extra element is used as well as voltage gain and efficiency are not hampered.

From Fig. 15 theoretically it is derived that from 0.25 to 0.7 duty ratio the switch current stress reduction is possible without wasting extra energy like using L-D network and voltage gain loss. The switch current reduction is also valid for DCM operation of the converter. Converter proposed in [19] is considered as conventional for comparison with current proposal at DCM. From Fig. 22 it is clear that in the DCM the switch current peak value is less.

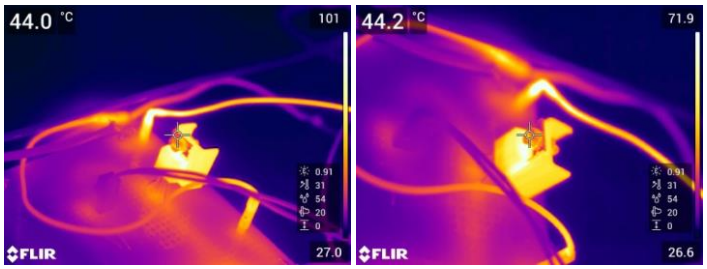


(a). (b)

Fig. 22. Converter operation in DCM at ($DT_S<t_r$) (a) switch current (b) input Current. @ 10 kHz.

RMS current is the dominating factor while determining loss and efficiency for any converter. The RMS current of the current proposal is comparable with L-D based solution [24] and other topologies. Thermal image of the main switch is captured using thermal imager to show the closeness of RMS current between current proposal and L-D based solution [24] at rated 100W condition as shown in Fig. 23 (a) and (b)

Theoretical loss calculation is performed on proposed DC-DC converter at 100W based on selected components summarized in Table-III to estimate losses, efficiency and shown in Fig. 24. Losses in coupled inductor and diode is more in the loss distribution.



(a). (b)

Fig. 23. Thermal image of switch in (a) L-D based switch current stress reduction proposed in [24] (b) proposed DC-DC converter.

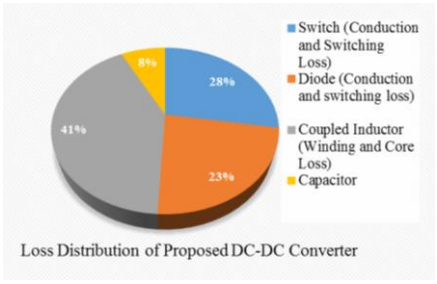


Fig. 24. Loss distribution of proposed DC-DC converter.

Based on the theoretical calculation [26] taking hardware components as mentioned in Table-III, estimated efficiency is compared to measured efficiency at different power points through power quality analyser APLAB-PQA2100E as shown in Fig. 25. The difference between theoretical estimated efficiency and practical measurement is due to ignorance of different circuital parameters like skin effect, proximity effect, exact transient time for switching events etc. Current waveforms are also considered as ideal for theoretical calculation which create differences in measured and calculated efficiency.

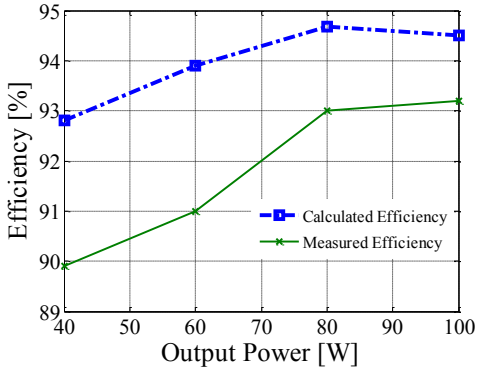


Fig. 25. Estimated and measured efficiency of the proposed DC-DC converter.

At 100W, the measured efficiency is 93.2%. Better-graded wires can be used in the inductor to further improve the efficiency. The discrepancy is caused by ignoring the leakage inductance, small-ripple assumption and measurement error. Efficiency comparison with other converter as shown in Fig. 26 is also performed to show that there is no sacrifice on efficiency especially when compared with proposal [24]. The converter in [22] has better efficiency i.e. ≈1% compared to current proposal. However, this difference is marginal and current proposal is better in terms of voltage gain, switch current stress minimization.

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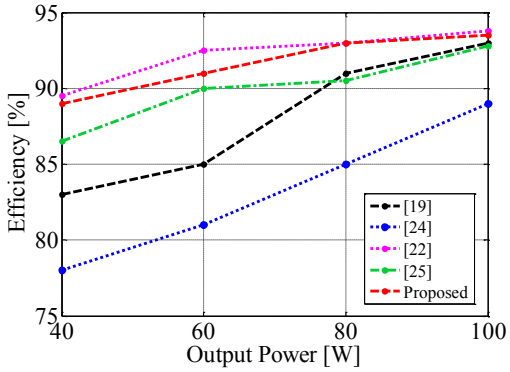

Fig. 26. Efficiency of the proposed converter operation in CCM at ($DT_S<t_r$) and 50 kHz.

VI. Conclusion

Generally, in a single switch type high step-up coupled inductor based boost converter, multi loop current paths are used to lift the voltage gain particularly at a duty less than 0.5. This increase the switch current stress due to low inductance of the coupled inductor. Considering this, a half cycle resonating branch is introduced in this article to utilize the inductance of the coupled inductor without increasing the circuit component and complexity. This improves the current stress on the main switch of the coupled inductor based single switch high step-up boost converter. This technique can be used to modify all the existing circuit topologies, resulting in the better performance in terms of voltage gain, efficiency and current stress. The measured efficiency of an example DC-DC converter is 93.2% at 100W, which is close to the proposal [22].

Additionally, the proposed technique performs superior than [24] as it can reduce the current stress up to 22% without sacrificing the voltage gain and efficiency. Moreover, this technique does not increase the RMS current, which improves the converter life span and reliability.

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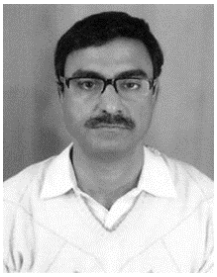

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