Multisampling Method for Single-Phase Grid-Connected Cascaded H-Bridge Inverters

Ma, Junpeng; Wang, Xiongfei; Blaabjerg, Frede; Song, Wensheng; Wang, Shunliang; Liu, Tianqi

Published in:
IEEE Transactions on Industrial Electronics

DOI (link to publication from Publisher):
10.1109/TIE.2019.2947864

Publication date:
2020

Document Version
Accepted author manuscript, peer reviewed version

Multi-Sampling Method for Single-Phase Grid-Connected Cascaded H-bridge Inverters

Junpeng Ma, *Member*, *IEEE*, Xiongfei Wang, *Senior Member*, *IEEE*, Frede Blaabjerg, *Fellow*, *IEEE*, Wensheng Song, *Member*, *IEEE,* Shunliang Wang, *Member*, *IEEE*, Tianqi Liu, *Senior Member*, *IEEE.*

***Abstract*—This paper proposes a multi-sampling method for single-phase grid-connected cascaded H-bridge (CHB) multilevel inverters with the phase-shifted carrier pulsewidth modulation (PSC-PWM) in order to reduce the time delay involved in the control loop and increase the control bandwidth. In this method, the controlled variables are sampled not only at the peak and the valley of all triangular carriers, but also at the intersection points of all phase-shifted carriers and inverted ones, which enables a minimum unity sampling interval without detecting the current ripple caused by the switching action and breaking the voltage-second balance in the modulation process. The bandwidth of the current control loop based on the proposed sampling method is illustrated and compared to other traditional sampling methods. The analysis shows that the system effectively reduces the time delay involved in the control loop and improves the bandwidth of the control loop. Finally, a downscale test platform of the single-phase grid-connected CHB multilevel inverter with an inductance (L)-filter is built to verify the effectiveness of the proposed method.**

***Index Terms*—Bandwidth, multi-sampling method, multilevel converter, phase-shifted carrier, pulsewidth modulator.**

I. Introduction

The phase-shifted carrier pulsewidth modulation (PSC-PWM) has been widely applied in the cascaded H-bridge (CHB) multilevel converters [1]. In the digital implementation of the carrier-based PWM, the regular sampling method is commonly used to sample the current and voltage at the peak and/or valley of the triangular carrier [2]-[4]. In order to avoid the loss of the duty cycle, one sampling interval is generally reserved for updating the duty-cycle [5]. Consequently, there is a time delay introduced by such a digital computation and PWM, which reduces the bandwidth of the current control loop [6], [7], and adds the negative damping to external electrical systems [8], [9].

Various control methods have been proposed to compensate the time delay [10]-[12]. In [13], [14], the predictive deadbeat control is proposed to compensate the time delay. However, this method depends on the model accuracy of the converter. A real-time computation method with dual sampling mode is proposed to eliminate the computational delay [15], yet there still is a PWM delay of a quarter switching interval.

Alternatively, the multi-sampling method provides an attractive way to reduce the time delay of the digital control system [4], [7]. The multi-sampling controller detects the controlled variables and updates the duty cycle multiple times in one PWM triangular carrier period to reduce the time delay. However, there are a few drawbacks with the traditional multi-sampling methods: 1) The current ripple caused by the switching action will be measured and introduced into the control loop by the multi-sampling method [16], [17], which consequently deteriorates the dynamic performance of the control system. 2) The multiple switching events may take place since the duty cycle is updated multiple times during one triangular carrier period [7], and this phenomenon will increase the switching frequency.

In [18], a comprehensive analysis of the multi-sampling method for a three-phase two-level inverter with an LCL filter is presented, and the bandwidth of the closed-loop control system is significantly improved by this method, but the drawbacks mentioned above are not overcome. A ripple filter is reported in [18] to suppress the current ripples caused by the multi-sampling method, but the dynamic response of the control system is limited by the filter. A multi-sampling method is thus developed to sample the averaged current and voltage four times within one switching period [19], and the time delay in the control loop is consequently reduced. Yet, this method cannot be applied in multilevel converters. The multi-sampling method in [20] is proposed for multilevel converters, yet the signal is merely measured at the peak and valley of each triangular carrier, restraining the dynamics of multilevel converters.

Manuscript received December 2, 2018; revised April 17, 2019; accepted for publication September 29, 2019. This work was supported in part by the National Natural Science Foundation of China under Project 51707126, in part by the Fundamental Research Funds for the Central Universities under Project 20822041C4003. Recommended for publication by Associate Editor XXXX. (Corresponding author: Xiongfei Wang.)

J. Ma, S. Wang, and T. Liu are with College of Electrical Engineering, Sichuan University, Chengdu 610031, China (e-mail: junpeng_ma@163.com; slw_scu@163.com; tqliu@scu.edu.cn).

X. Wang and F. Blaabjerg are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: xwa@et.aau.dk; fbl@et.aau.dk)

W. Song is with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu 610031, China (songwsh@swjtu.edu.cn)

This paper presents first a comprehensive analysis of the phenomena for the current ripple brought by the multi-sample method for single-phase grid-connected multilevel cascaded H-bridge inverters with PSC-PWM. Then, a multi-sampling method with the minimum sampling interval is proposed to sample the current and voltage without detecting the current ripple caused by the switching action and breaking the voltage-second balance in the modulation process. It effectively reduces the time delay and improves the bandwidth of the closed-loop control system.

II. System Description

A. The single-phase CHB inverter

Fig. 1 shows the topology of a single-phase grid-connected CHB multilevel inverter with a digital current controller, where u is the grid voltage, and L and R are the filter inductance and its equivalent resistance, respectively. v_x is the output voltage of two-level H-bridge inverters in cell x, and all cells are connected in series. The synthesized voltage v is the sum of all individual cell outputs. u_{dcx} represents a constant dc-link voltage of the converter cell x. S_{xyp} and S_{xyn} represent the switching devices in leg y of the cell x, where $y = a, b$, and $x = 1, 2...N$. In this paper, two cascaded converter cells are considered.

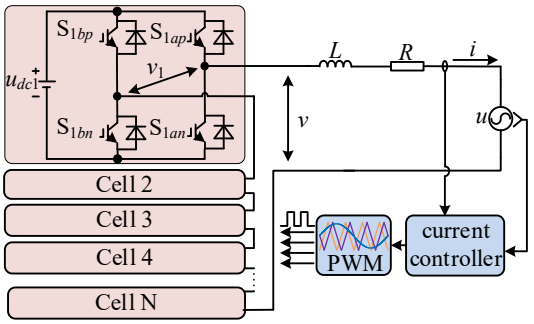


Fig. 1. A single-phase CHB multilevel inverter with a digital current controller.

The resistance R is usually small, which is ignored for simplicity. The Kirchhoff voltage law (KVL) is adopted to analyze voltage across the inductor L, and the voltage equation is shown as

$$L\frac{di}{dt} = v - u. \tag{1}$$

The output voltage of the cell x can be described as

$$v_x = v_{xa} - v_{xb} \tag{2}$$

where the output voltage v_{xa} and v_{xb} of the leg a and leg b in cell x are defined as

$$v_{xa} = -v_{xb} = \frac{v_x}{2}. \tag{3}$$

The switching function G_{xy} is defined as

$$G_{xy} = \begin{cases} 1 & S_{xyp} \text{ is on and } S_{xyn} \text{ is off} \\ 0 & S_{xyp} \text{ is off and } S_{xyn} \text{ is on} \end{cases} \tag{4}$$

where x=1, 2…N, and y=a, b. The output voltage for the leg is the half of that for the cell, which is shown in (3). Therefore, the output voltage v_{xa} and v_{xb} in different switching state is expressed as

$$v_{xy} = \begin{cases} u_{dcx}/2 & G_{xy}=1 \\ -u_{dcx}/2 & G_{xy}=0 \end{cases} \tag{5}$$

The output voltage of the inverter can be described as

$$v = \sum_{x=1}^{N} v_x = \sum_{x=1}^{N} (v_{xa} - v_{xb}) = \sum_{x=1}^{N} v_{xa} - \sum_{x=1}^{N} v_{xb} \tag{6}$$

Assuming that the rated power of each converter cell is the same, the modulating voltage of each cell satisfies

$$v_x^* = \frac{v^*}{N} \tag{7}$$

where v^* is the modulating wave calculated by the digital controller. If the dc voltage source of each cell is not enough stiff, the voltage balancing method need to be applied to balance the dc-link voltage. It can be achieved by modifying v_x^* for cell x [21].

The normalized modulating wave for cell x, which feeds into the modulator, is defined as

$$\underline{v}_x = \frac{v_x^*}{(u_{dcx}/2)} = \frac{1}{(u_{dcx}/2)}\frac{v^*}{N}. \tag{8}$$

The normalized modulating wave of the leg a and the leg b in cell x is defined as

$$\underline{v}_{xa} = -\underline{v}_{xb} = \frac{\underline{v}_x}{2}. \tag{9}$$

PSC-PWM is usually used to generate the driving pulses of the CHB inverter. The shifted phase of the triangular carrier C_x for the cell x relative to that for cell 1 is expressed as

$$\alpha_x = \frac{(x\text{-}1)\pi}{N} \tag{10}$$

where x = 1…N. Taking two-cells CHB converter as an example, the shifted phase of the triangular carriers for cell 1 and cell 2 respectively are 0º and 90º.

B. Traditional digital sampling method

For simplification, the digital sampling method and modulation timing for one cell H-bridge is described as follows.

Fig. 2 shows the traditional digital sampling in one-cell H-bridge inverter. the voltage and current are sampled at the peak and valley of the triangular carrier, and then the control program is computed according to the sampled voltage and current in the digital microcontroller. After finishing computation of the control program, the modulating wave $\underline{v}_{1a}$ and $\underline{v}_{1b}$ are obtained, and $\underline{v}_{1a}$ and $\underline{v}_{1b}$ are updated in the next peak or valley of the triangular carrier. Therefore, the modulating wave is updated after one sampling interval of signal sampling instant, and a unit delay will be introduced into the control loop. The updated modulating wave will be held during each sampling interval, and they hereby are a constant value in one sampling interval. These constant modulating waves will be compared to the triangular carrier, and if the modulating wave is more than the triangular wave, the output of the modulator is high. On the contrary, the output of the modulator is low. According to this modulating principle, the output voltage v_{1a} and v_{1b} of leg a and leg b and the output voltage v_1 of the H-bridge are generated.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2947864, IEEE Transactions on Industrial Electronics

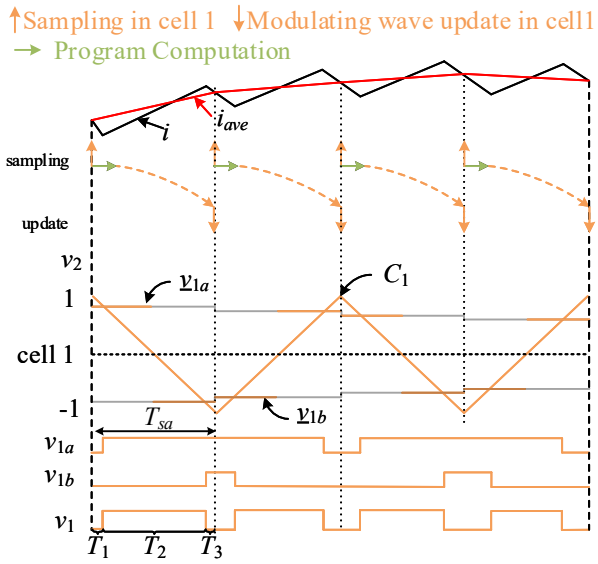


Fig. 2. Traditional digital sampling in one-cell H-bridge inverter.

As shown in Fig. 2, the output voltage v_1 is divided into three segments during one sampling interval, and corresponding vectors respectively are V_1, V_2, V_3, whose durations in one sampling interval are T_1, T_2, and T_3 in one sampling interval. And these durations satisfy

$$T_1+T_2+T_3=T_{sa} \tag{11}$$

In Fig. 2, according to the property of similar triangles, the duration T_1 and T_3 during the interval between the instant k to instant k+1 satisfy

$$\begin{cases} \dfrac{1-v_{1a}}{1-(-1)}=\dfrac{T_1}{T_{sa}} \\ \dfrac{1+v_{1b}}{1-(-1)}=\dfrac{T_3}{T_{sa}} \end{cases} \tag{12}$$

Substituting (8), (9) into (12), combining with (11), it can be derived as

$$\begin{cases} T_1=T_3=\dfrac{1}{2}T_{sa}-\dfrac{v_1^*}{2u_{dc1}}T_{sa} \\ T_2=\dfrac{v_1^*}{u_{dc1}}T_{sa} \end{cases} \tag{13}$$

According to (13), the integral output voltage v_1 of the H-bridge within one sampling interval satisfies

$$\int_0^{T_{sa}} v_1 dt=T_1V_1+T_2V_2+T_3V_3=T_2V_2=\frac{v_1^*}{u_{dc1}}T_{sa}u_{dc1}=v_1^*T_{sa} \tag{14}$$

Actually, in any pulsewidth modulation process, the integral of the output voltage of the inverter within one sampling interval is equal to the integral of the modulating wave within one sampling interval. It can be expressed as

$$\int_{kT_{sa}}^{(k+1)T_{sa}} v dt=\sum_{i=1}^{m}T_iV_i=\int_{kT_{sa}}^{(k+1)T_{sa}} v^* dt=v^*T_{sa} \tag{15}$$

where T_i is the duration for the output voltage vector V_i of the inverter during one sampling interval. m is the number of the voltage vector within one sampling interval. and the output voltage $v^*$is held within one sampling interval.

The equation (15) shows that voltage-second value between the output voltage of the inverter and the modulating wave is balanced within one sampling interval. If (15) is not satisfied within one sampling interval, the voltage-second balance is broken and the output voltage will not track the modulating wave within one sampling interval. Therefore, the design of the sampling method must guarantee the voltage-second balance shown in (15).

C. Traditional multi-sampling method

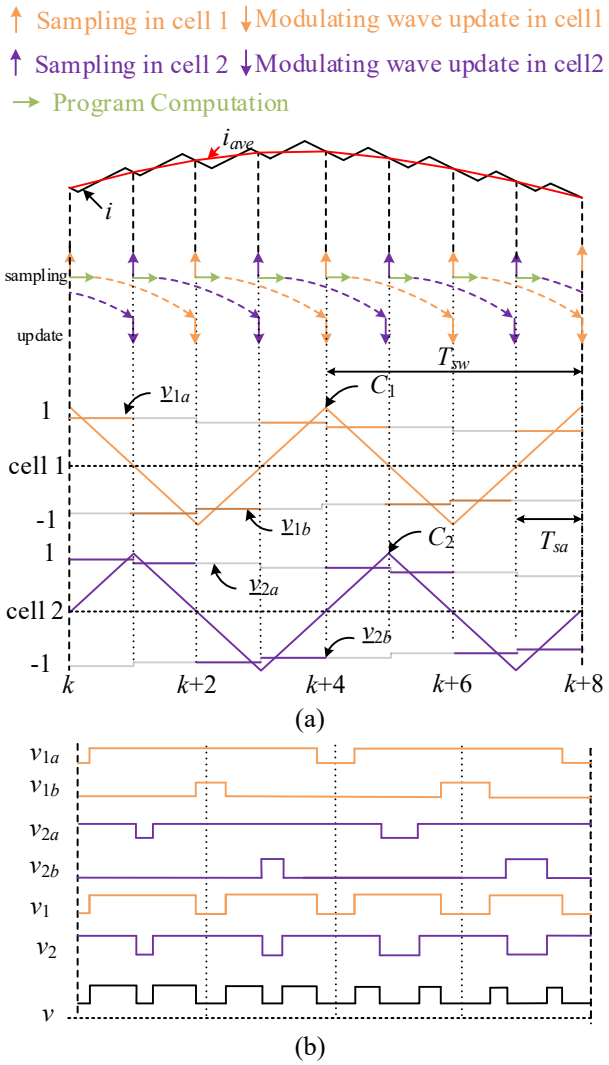


Fig. 3. Current waveform and pulse patterns using a traditional multi-sampling method. (a) the sampling process and modulation, and (b) the pulse pattern.

Fig. 3 depicts a conventional multi-sampling process for the two-cell cascaded converter. T_{sw} is the switching interval, which is four times the sampling interval T_{sa}. i_{ave} presents the ideal current without current ripple, assuming that the inverter can output the modulating voltage v^*, As shown in Fig. 3(a), the current is sampled at the peak and valley of the triangular carrier for cell x and at the same instant, the modulating wave v_x for cells is updated. As an example, as shown in Fig. 3(a), the modulating waves v_1 and v_2 are calculated at the instant k and

k+1, respectively, but are updated at the instant k+2 and k+3, respectively. During the instant k to the instant k+1, the modulating wave v_{1a} traverse the triangular carrier C_1 once, and the modulating wave v_{2a} traverses the triangular carrier C_2 once. Therefore, during this sampling interval, there are two times switching actions in the converter cell 1 and cell 2, as shown in Fig. 3(b). In this method, the sampling frequency is four times the switching frequency. It determines the Nyquist frequency, which is equal to the twice switching frequency.

Based on (1), the accrual current i and the average current i_{ave} within each sampling interval can be expressed as

$$\begin{cases} i(t)=\int_{kT_{sa}}^{t}\frac{v-u}{L}dt+i(k). \\ i_{ave}(t)=\int_{kT_{sa}}^{t}\frac{v^{*}-u}{L}dt+i(k). \end{cases} \tag{16}$$

According to voltage-second balance principle expressed in (15), It can be expressed as

$$\int_{kT_{sa}}^{(k+1)T_{sa}}v^{*}dt=\int_{kT_{sa}}^{(k+1)T_{sa}}vdt \tag{17}$$

From (16) and (17), at the peak and valley of the triangular carriers, the sampled current can be expressed as

$$\begin{aligned} i(k+1)&=\int_{kT_{sa}}^{(k+1)T_{sa}}\frac{v-u}{L}dt+i(k) \\ &=\int_{kT_{sa}}^{(k+1)T_{sa}}\frac{v^{*}-u}{L}dt+i(k)=i_{ave}[(k+1)T_{sa}]. \end{aligned} \tag{18}$$

Based on (18), the sampled current is equal to the average current at every sampling instant. Hence, with the traditional sampling method shown in Fig. 3, the average current is measured and the current ripple is effectively suppressed.

III. MULTI-SAMPLING METHOD

A. Sampling sequence

In contrast to the traditional method, the proposed sampling method samples the current and voltage not only at the peak and the valley of all triangular carriers C_x, but also at the intersection points of all triangular carriers and inverse ones C_x'. Meanwhile, the duty cycle is updated at those time instants, which is depicted in Fig. 4.

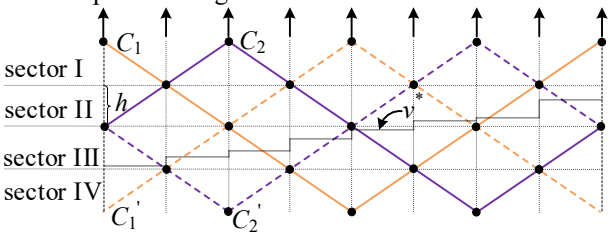


Fig. 4. Distribution of sampling point in one switching interval.

As shown in Fig. 4, the amplitude and period of the triangular carrier are divided into four sectors and eight intervals. In general, there are 2N sectors and 4N intervals in N-cells CHB converter by using the proposed sampling method, and h is the width of one sector, which can be expressed as

$$h=1/\mathrm{N} \tag{19}$$

and the sampling period is expressed as

$$T_{sa}=\frac{T_{sw}}{4N}. \tag{20}$$

The sampling frequency will increase with the number of the cascaded converter cells. Therefore, the bandwidth of the closed-loop system can be increased accordingly.

B. The suppression of the current ripple

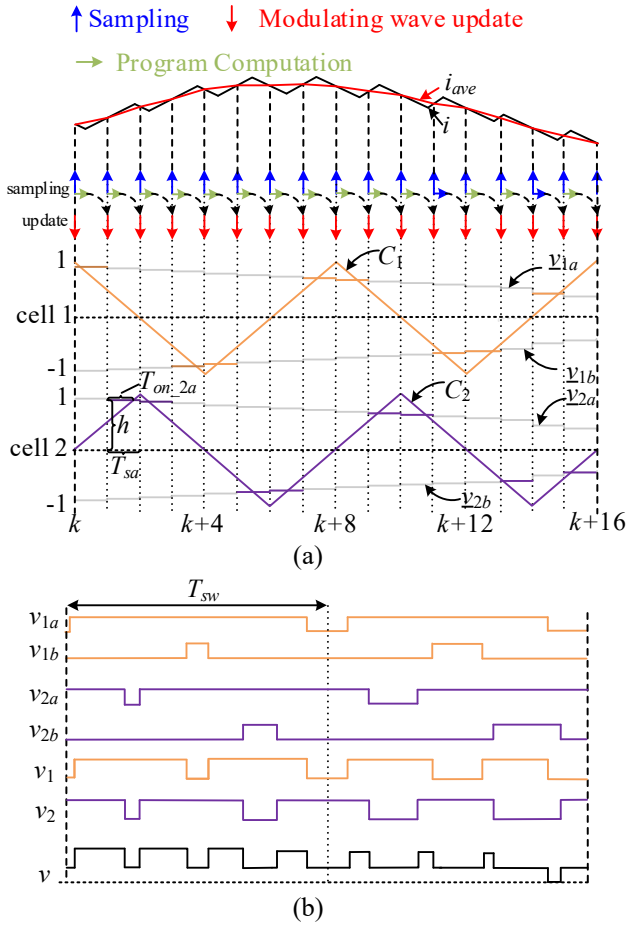


Fig. 5. Current waveform and pulse pattern with the proposed sampling method. (a) Sampling and modulation, and (b) Pulse pattern.

Fig. 5 illustrates the current waveform, the update of the modulating wave, and PWM pattern based on the proposed sampling method. Compared to the traditional sampling method in Fig. 3, the sampling interval is reduced by the proposed method. There is at least one modulating wave v_{xy} for the leg y in cell x, which will pass through triangular carriers C_x and generate a desired rising or falling edge within one sampling interval. Taking the second interval in Fig. 5(a) as an example, the modulating wave v_{2a} passes through the triangular carrier C_2 for cell 2, according to the property of similar triangles, the duration T_{on_2a} of G_{2a} equal to 1 satisfies

$$\frac{T_{on\_2a}}{T_{sa}}=\frac{v_{2a}}{h}. \tag{21}$$

Substituting (8), (9) and (20) into (21), in the first sampling interval of Fig. 5(a), the relationship between the calculated modulating wave v^{*} and actual output voltage v can be expressed as

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2947864, IEEE Transactions on Industrial Electronics

$$\int_{kT_s}^{(k+1)T_{sa}} v dt = \int_{kT_s}^{(k+1)T_{sa}} (\sum_{x=1}^{N} v_{xa} - \sum_{x=1}^{N} v_{xb}) dt = \int_{kT_s}^{(k+1)T_{sa}} v_{2a} dt = u_{dc2} T_{on\_2a} = v^* T_{sa}. \quad (22)$$

which indicates that with the proposed sampling method, the voltage-second balance expressed in (15) is guaranteed during one sampling interval.

Similar to (18), combining with (22), the sampled current can be expressed as

$$i(k+1) = \int_{kT_{sa}}^{(k+1)T_{sa}} \frac{v^* - u}{L} dt + i(k) = i_{ave}[(k+1)T_{sa}]. \quad (23)$$

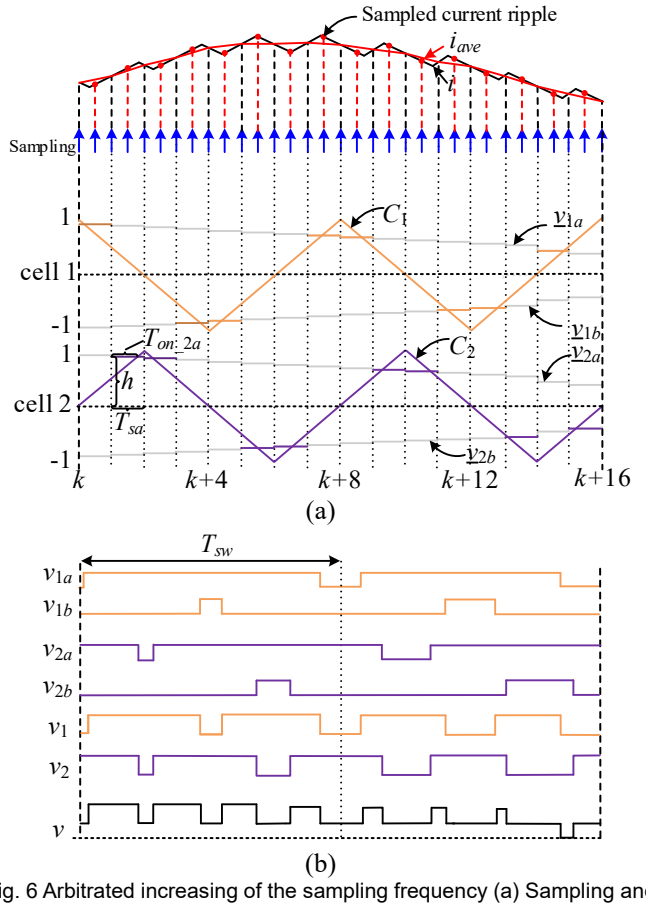


Fig. 6 Arbitrated increasing of the sampling frequency (a) Sampling and modulation, and (b) Pulse pattern

It can be seen from (23) that the sampled current is equal to the average current at the sampling instant and does not include any current ripple caused by the switching action. For any other sampling intervals, the same conclusion, which is elaborated in (23), can also be drawn. Therefore, the average current can be easily sampled by the proposed method without using any filters

Increasing the sampling frequency can certainly reduce the time delay of the current control loop and consequently widen the control bandwidth. However, the sampling frequency cannot be arbitrarily increased. If the sampling instants are inappropriately distributed, the current ripples caused by the switching action of the converter will be sampled and propagated into the control loop, which is illustrated in Fig. 6.

C. The Unity sampling interval

According to (15), the voltage-second balance is related to the sampling interval T_{sa}. Therefore, inappropriate design of sampling interval will cause voltage-second unbalance.

Fig. 7 shows the case of voltage-second unbalance in the condition of reducing the sampling interval. During the instant k to k+2, the proposed sampling method is used to sample signal, the sampling interval is T_{sa1}, after the instant k+2, the sampling instant is reduced to T_{sa2}. Taking the interval from the instant k+2 to the instant k+3 as an example, there is no switching action provided that the modulating wave is located in the dashed region, which means the voltage-second balance expressed in (15) is broken in dashed regions. Consequently, in dashed regions, the output voltage of the inverter cannot track the modulating wave, and it will deteriorate control precision. Yet, In the interval from the instant k to instant k+2 in Fig. 7, the proposed sampling method is applied, and the voltage-second balance is always satisfied for the reason that there always is an intersection point between the carriers and the modulating wave and the desired driving pulse can be generated.

If the sampling interval is slightly increased shown in Fig. 8, there will not be switching action when the modulating wave is located in the dashed region, and the voltage-second unbalance also exists in the modulation process. Therefore, the slightly increasing the sampling period also deteriorates the control performance.

It can be seen from Fig. 7 and Fig. 8 that the voltage-second unbalance in the modulation process will arise provided that the sampling event does not happen at the instant of the peak, valley of the carriers and the intersection point of the carriers and inverse ones. Therefore, the sampling interval must be the integer times of that in the proposed sampling method for guaranteeing the voltage-second balance in each sampling interval.

It is worth mentioning that the proposed method leads to a minimum sampling interval, which is defined as the unity sampling interval hereafter, without breaking the voltage-second balance and sampling the current ripple caused by the switching action. In essential, the sampling period of all the existing sampling methods for single-phase PSC-PWM converters can be expressed based on the unity sampling interval, and thus a generalized derivation of the sampling period for PSC-PWM converters can be given by

$$T_{sa} = M \frac{T_{sw}}{4N} \quad (24)$$

where M=1, 2, 3…, implying that the sampling interval must be integer multiples of the unity sampling interval. Otherwise, the output voltage of the inverter will not track reference modulating wave calculated by the controller in each sampling interval. Therefore, given a PSC-PWM converter with the known cell number, switching frequency and the required computational time, the sampling period can be determined by choosing a proper value of M.

Especially, the single-sampling mode [22], double-sampling mode [15], and quadruple-sampling mode [19] for the single-phase two-level converter corresponds to the case of M=4 and N=1, M=2 and N=1, and M=1 and N=1, respectively. Fig. 9 shows the comparison of the different sampling methods,

which proves that the traditional sampling interval always is the integer times of the unity sampling interval.

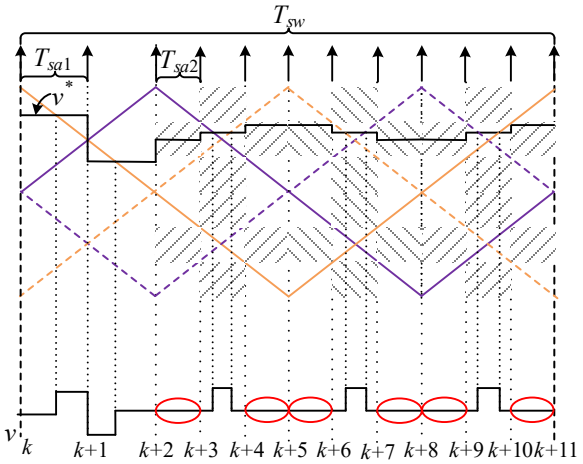


Fig. 7. The voltage-second unbalance in the condition of reducing the sampling interval.

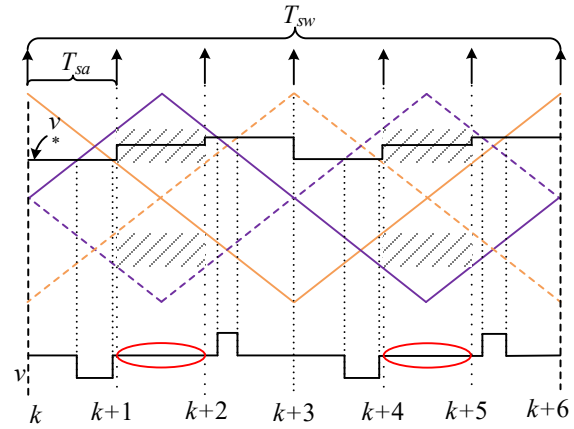


Fig. 8. The voltage-second unbalance in the condition of increasing the sampling interval.

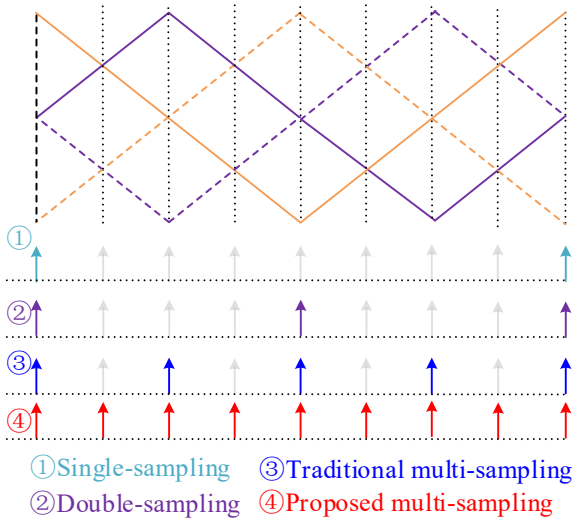


Fig. 9. Different sampling sequence.

IV. Analysis of Current Control Loop with The Different Sampling Method

A. Critical proportional gain analysis

Considering the parasitic resistor, The Kirchhoff voltage law (KVL) is adopted to analyze voltage across the inductor L, and the voltage equation is expressed as

$$L\frac{di}{dt} = v - Ri - u. \tag{25}$$

Therefore, the transfer function $G_m(s)$ of v to i in the s-domain can be derived as

$$G_m(s) = \frac{i(s)}{v(s)} = \frac{1}{Ls + R}. \tag{26}$$

In the modulation process, the modulating wave is held during each sampling interval, and the Zero-order hold(ZOH) discretization method hereby usually is used to discrete the s-domain model of the power electronics converters modulated by the pulsewidth modulation. ZOH discretization method is expressed as

$$G_m(z) = (1 - z^{-1})\mathcal{Z}\left(\frac{G_m(s)}{s}\right). \tag{27}$$

Substituting (26) into (27), the z-domain model of the single-phase inverter with L-filter can be derived as

$$G_m(z) = \frac{(1 - e^{-\frac{R}{L}T_{sa}})}{R(z - e^{-\frac{R}{L}T_{sa}})}. \tag{28}$$

where the sampling interval T_{sa} is defined as

$$T_{sa} = M\frac{T_{sw}}{4N} \tag{29}$$

where N is the cell number and M=1 for the proposed sampling method.

If R approaches zero, $G_m(z)$ will be simplified as

$$G_m(z) = \frac{T_{sa}}{L}\frac{1}{z - 1} \tag{30}$$

Fig. 10 shows the block diagram of the current control loop, and the open loop transfer function can be derived as

$$G_o(z) = G_c(z)G_d(z)G_m(z). \tag{31}$$

where $G_d(z)=z^{-1}$, which is the unit delay due to the computation of the control method in the digital microcontroller. $G_c(z)$ is the transfer function for the current controller, which could be proportional controller, proportional-integral(PI) controller or proportional resonant(PR) controller, etc. for the grid-connected converter, the PR controller usually is applied to achieve the current control without steady-state error. In this paper, the PR control is used to analyze the control loop performance in this paper.

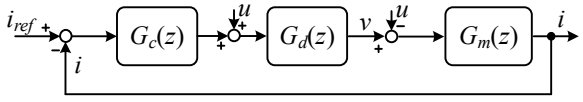


Fig. 10 Block diagram of the current control loop.

The s-domain transfer function of the PR controller is expressed as

$$G_c(s) = K_p + \frac{2K_i s}{s^2 + w_0^2}. \tag{32}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2947864, IEEE Transactions on Industrial Electronics

where ω_0 is the fundamental angular frequency. The discrete transfer function of the ideal PR controller can be derived as

$$G_c(z) = \mathcal{Z}[G_c(s)] = K_p + \frac{4K_i}{T_{sa}(\omega_0^2 + \frac{4}{T_{sa}^2})} \frac{z^2 - 1}{z^2 + 2\gamma z + 1}. \quad (33)$$

where

$$\gamma = (\omega_0^2 - \frac{4}{T_{sa}^2})/(\omega_0^2 + \frac{4}{T_{sa}^2}) \quad (34)$$

The bode diagram of the open loop transfer function G_o with different parasitic resistances is shown as Fig. 11. It can be seen that the parasitic resistance has less effect on the open loop transfer function in the high-frequency band, and the bandwidth f_{bw} of the control loop is almost identical with different parasitic resistances. Therefore, the parasitic resistor can be ignored for simplifying the analysis of the control loop bandwidth.

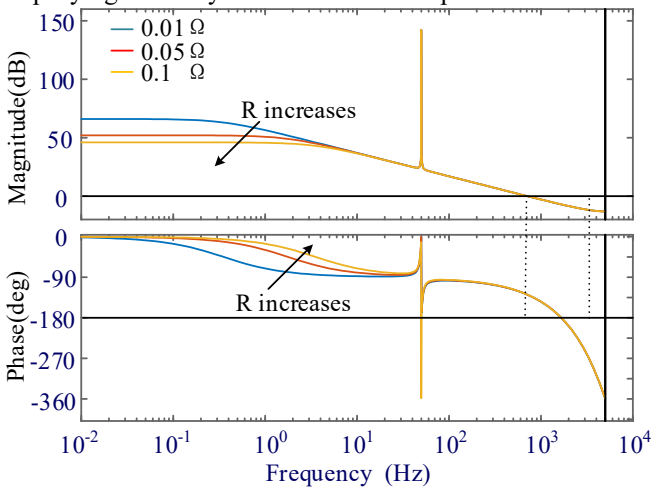


Fig. 11 Bode diagram of the open loop transfer function with different parasitic resistances.

Fig. 12 shows the bode diagram of the open loop transfer function with the proportional controller and PR controller. It can be seen than the frequency responses with the proportional controller and PR controller are almost identical except for the resonance point around the fundamental frequency. Therefore, the resonance component in the PR controller can be ignored for analysis of the controller bandwidth.

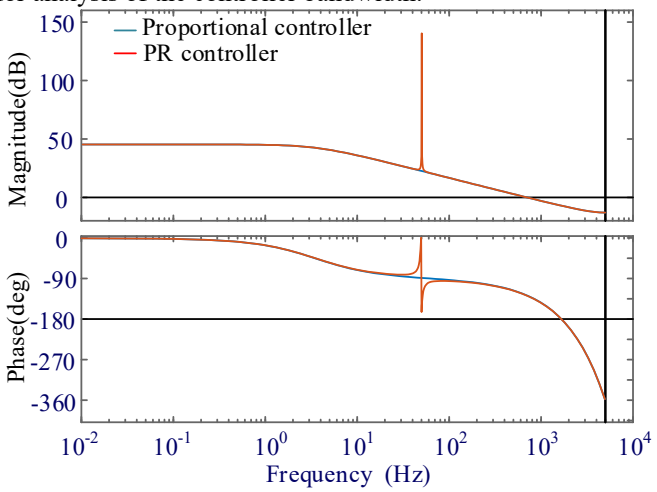


Fig. 12. Bode diagram of the open loop transfer function with proportional controller and PR controller.

As mentioned above, the proportional controller is considered and the parasitic resistor can be ignored for analysis of the control loop bandwidth. Therefore, according to (30) and (31), the open loop transfer function can be derived as

$$G_o(z) = K_p \frac{T_{sa}}{L} \frac{z^{-1}}{z-1} = K_p \frac{M}{4N} \frac{T_{sw}}{L} \frac{z^{-1}}{z-1}. \quad (35)$$

For analyzing the frequency response of the control loop, the symbol z in transfer function (35) is replaced by (36). The frequency response of the current control loop is consequently represented by (37).

$$z = e^{j\omega T_{sa}} \quad (36)$$

$$G_o(e^{j\omega T_{sa}}) = \frac{M}{8N} \frac{T_{sw}}{L} \frac{K_p}{\left|\sin(\frac{M}{8N}\omega T_{sw})\right|} e^{-j\varphi} \quad (37)$$

where the phase φ is expressed as

$$\varphi = \frac{\pi}{2} + \frac{3M}{8N}\omega T_{sw} \quad (38)$$

which is the phase response at the different frequencies.

The phase crossover frequency f_{cr} satisfies that φ=0, and f_{cr} is hereby derived as

$$f_{cr} = \frac{2N}{3M} f_{sw}. \quad (39)$$

Based on (37) and (39), the critical proportional gain can be solved as

$$K_{cr} = \frac{4N}{M} L f_{sw}. \quad (40)$$

The phase crossover frequency and the critical proportional gain by using different sampling methods for one-cell and N-cell topologies with PSC-PWM are listed in Table I.

TABLE I
PHASE CROSSOVER FREQUENCY AND THE CRITICAL PROPORTIONAL GAIN OF THE CURRENT CONTROL WITH DIFFERENT SAMPLING METHODS

Topology	N	M	Sampling method	f_{cr}	K_{cr}
Single H-bridge	1	4	Single-sampling [22]	$1/6f_{sw}$	Lf_{sw}
Single H-bridge	1	2	Double-sampling [4]	$1/3f_{sw}$	$2Lf_{sw}$
Single H-bridge	1	1	Quartic-sampling [19]	$2/3f_{sw}$	$4Lf_{sw}$
N cells CHB	N	2	Traditional multi-sampling [20]	$N/3f_{sw}$	$2NLf_{sw}$
N cells CHB	N	1	Proposed multi-sampling	$2N/3f_{sw}$	$4NLf_{sw}$

B. Control bandwidth improvement

The gain margin of the current controller can be expressed as

$$GM = -20\lg|G_o(e^{j2\pi f_{cr}T_{sa}})| = -20\lg[\frac{M}{8N}\frac{T_{sw}}{L}\frac{K_p}{\left|\sin(\frac{M}{8N}2\pi f_{cr}T_{sw})\right|}] \quad (41)$$

Substituting (39) into (41), the gain margin with the traditional and proposed methods can be expressed as

$$\begin{cases} GM_t = -20\lg\dfrac{M_t T_{sw} K_{p\_t}}{4NL} \\ GM_p = -20\lg\dfrac{M_p T_{sw} K_{p\_p}}{4NL} \end{cases} \quad (42)$$

where GM_t and GM_p are the gain margin in the traditional sampling method and the proposed sampling method. K_{p_t} and K_{p_p} are the proportional gain of the traditional method and the proportional method, respectively. When the gain margin in the traditional sampling method is the same as that in the proposed sampling method, it can be deduced as

$$M_t K_{p\_t} = M_p K_{p\_p} = \lambda \tag{43}$$

which indicates that the proportional gain will proportionally increase with the reduction of M if the gain margin maintains constant.

According to (35), the closed-loop transfer function of the current control loop can be expressed as

$$G_{\mathrm{cl}}(z) = \frac{G_o(z)}{1+G_o(z)} = \frac{K_p \frac{M}{4N}\frac{T_{sw}}{L} z^{-1}}{K_p \frac{M}{4N}\frac{T_{sw}}{L} z^{-1} + (z-1)} \tag{44}$$

Based on the classical definition of the bandwidth of the control loop [23], the bandwidth is the frequency at which the magnitude for the frequency response of the closed-loop control system drops to 70.7% (or 3dB) of its zero-frequency value. The bandwidths of the control loop f_{bw_t} and f_{bw_p} in the traditional method and the proposed method respectively satisfy

$$\begin{cases} 20\lg|G_{\mathrm{cl}}(e^{j2\pi f_{bw\_t} T_{sa}})| - 20\lg|G_{\mathrm{cl}}(e^{j2\pi 0})| = -3\mathrm{dB} \\ 20\lg|G_{\mathrm{cl}}(e^{j2\pi f_{bw\_p} T_{sa}})| - 20\lg|G_{\mathrm{cl}}(e^{j2\pi 0})| = -3\mathrm{dB} \end{cases} \tag{45}$$

where T_{sa_t} and T_{sa_p} respectively are the sampling period of the traditional method and the proposed method.

Substituting (43) and (44) into (45), the relationship between the control bandwidth with the traditional method and that with the proposed method can be expressed as

$$\begin{aligned} &(4+\frac{\lambda T_{sw}}{NL})\sin(\pi f_{bw\_p}\frac{1}{4N}T_{sw})^2 - \frac{\lambda T_{sw}}{NL}\sin(2\pi f_{bw\_p}\frac{1}{4N}T_{sw})^2 \\ &= (4+\frac{\lambda T_{sw}}{NL})\sin(\pi f_{bw\_t}\frac{M}{4N}T_{sw})^2 - \frac{\lambda T_{sw}}{NL}\sin(2\pi f_{bw\_t}\frac{M}{4N}T_{sw})^2 \end{aligned} \tag{46}$$

Based on (46), it can be deduced as

$$f_{bw\_p} = f_{bw\_t} M \tag{47}$$

Therefore, the bandwidth of the control loop with the proposed sampling method is M times that with the traditional sampling method if the gain margin maintains invariant. It implies that the reduction of sampling interval in the proposed sampling method will improve the bandwidth of the control loop.

According to Table I, $M = 2$ in the traditional multi-sampling method indicates that the control bandwidth of the proposed sampling method is twice that of the traditional multi-sampling method. Moreover, the bandwidth with the proposed method is $4N$ and $2N$ times that with the traditional single-sampling and double-sampling methods, which means that the control bandwidth with the proposed method will be obviously increased compared to the traditional sampling method in the single-phase N-cell cascaded H-bridge inverter.

V. Simulation and Experiment

The simulation results and the scaled-down experimental test of 2-cell CHB are executed to verify the correctness of the theoretical analysis. The parameter of the simulation and the experimental test is shown in Table II, where PR controller parameters K_p and K_i can guarantee the stability of the control loop both in the traditional method and the proposed method. In the simulation and experimental test, the digital signal processor TMS320F28335 is used as the micro-controller, and the sampling interval is set as 100 μs, 200 μs for the proposed and traditional multi-sampling method, respectively.

TABLE II
Simulation and Experimental Parameter

Parameter	Value
The dc-link voltage of each cell	120 V
The grid voltage (RMS)	100 V
Switching frequency/Carrier frequency	1250 Hz
The parameter K_p in the PR controller	18 Ω
The parameter K_i in the PR controller	200 Ω

The filtered inductor is set to 5 mH for effectively suppressing the harmonics of the line current. According to the circuit parameter shown in Table II and K_{cr} and f_{cr} in Table I, the critical proportional gains for the single-sampling method, double-sampling method, traditional multi-sampling method and the proposed multi-sampling method are shown in Table III.

TABLE III
Critical Proportional Gain for Different Sampling Method

Method	Single-sampling	Double-sampling	Traditional multi-sampling	Proposed multi-sampling
K_{cr} (Ω)	6.25	12.5	25	50

A. Simulation results

Fig. 13 shows the simulation results of the traditional method and the proposed method in the steady state. the PR control is applied both in the traditional multi-sampling method and the proposed multi-sampling method. The simulation results show that the proposed method and the traditional method can obtain identical steady state performance.

Fig. 14 shows the simulation results in the unstable state with different multi-sampling methods. The proportional gain K_p is changed from 20 Ω to 30 Ω, where the theoretical critical gain is 25 Ω, with the traditional multi-sampling method. It can be seen that the line current becomes unstable when the proportional gain is more than the critical gain. Similarly, in the proposed multi-sampling method, when the proportional gain K_p is changed from 45 Ω to 55 Ω, which is more than the critical gain (50 Ω), the current control loop also becomes unstable. The simulation results verify the correctness of the theoretical analysis for the critical gain in different multi-sampling method. Due to the increase of the sampling frequency and the decrease of the time delay in the control loop with the proposed multi-sampling method, the critical gain in the proposed method is obviously larger than that in the traditional method, which implies that the gain margin is improved in the proposed multi-sampling method.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2947864, IEEE Transactions on Industrial Electronics

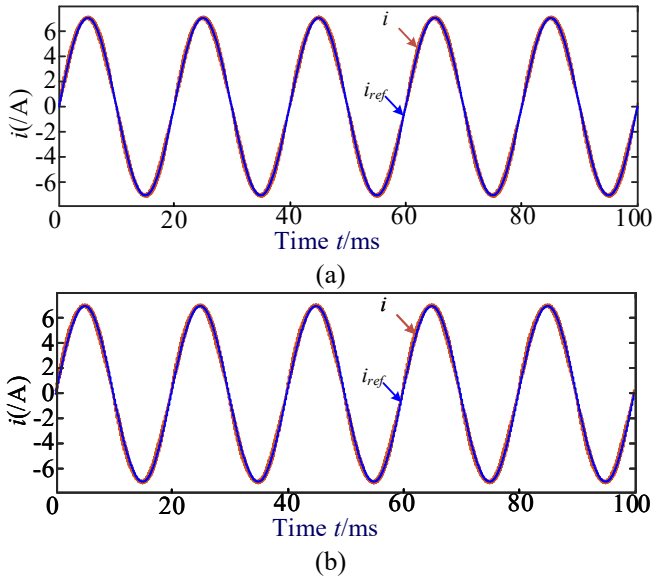


Fig. 13. Simulation results in the steady state with different multi-sampling methods. (a) the traditional multi-sampling method. (b) the proposed multi-sampling method.

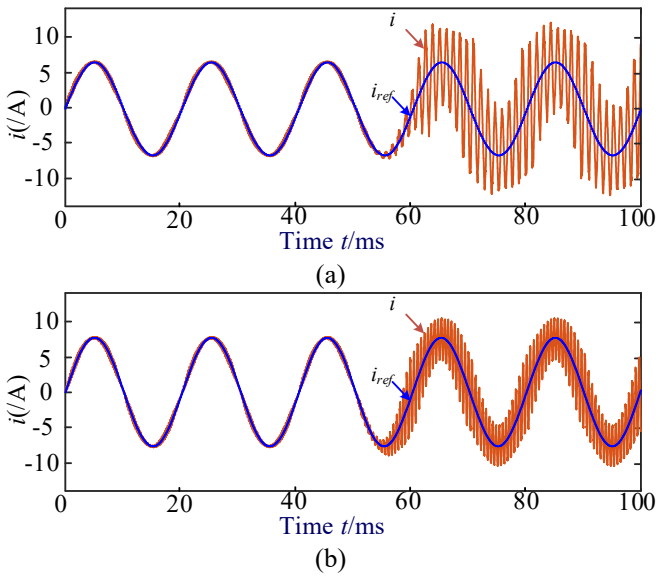


Fig. 14. Simulation results in the unstable state with different sampling methods. (a) the traditional multi-sampling method. (b) the proposed multi-sampling method.

Fig. 15 shows the simulation results in the condition of the sudden change of the reference current with the traditional sampling method and the proposed sampling method. It can be seen that there is obvious overshoot when the amplitude of the reference current is suddenly changed from 4A to 8A with the traditional sampling method, but there is no overshoot with the same controller parameters by using the proposed sampling method. The simulation results verify that the dynamic performance of the proposed method is better than that of the traditional method.

Fig. 16 shows the simulation results in the condition of the sudden change of the grid voltage amplitude with the different sampling method. It can be seen that the voltage sag has less effect on the line current with the proposed sampling method compared to the traditional sampling method since the time delay in the control loop is reduced by using the proposed multi-sampling method.

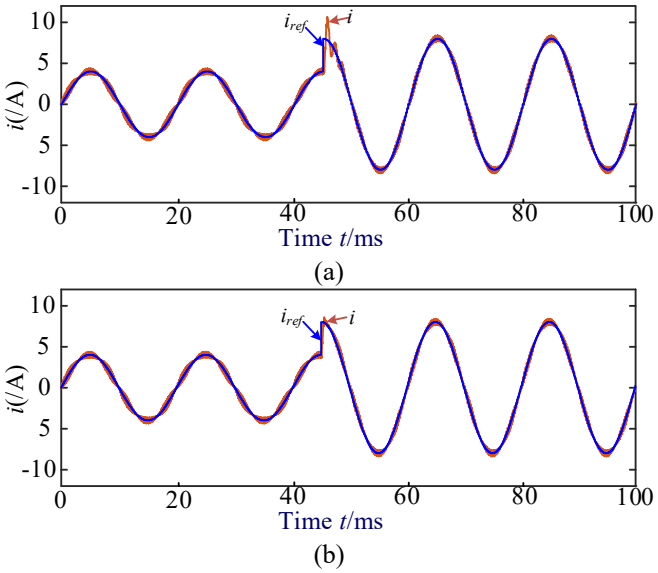


Fig. 15. Simulation results in the condition of the sudden change of reference current. (a) the traditional multi-sampling method. (b) the proposed multi-sampling method.

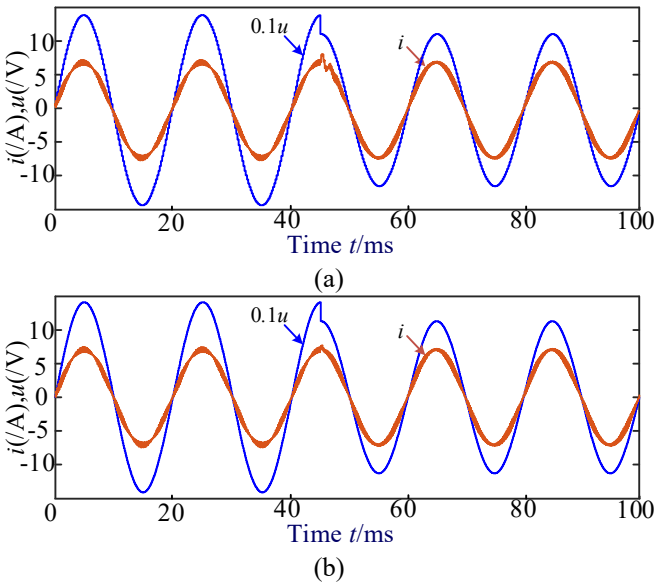


Fig. 16. The simulation results in the condition of the sudden change of the grid voltage amplitude. (a) the traditional multi-sampling method. (b) the proposed multi-sampling method.

Fig. 17 shows the simulation results in the condition of the sudden change of the dc-side voltage with the different sampling method. It can be seen that the dc-link voltage sudden change has a slight effect on the line current both in the traditional sampling method and the proposed method, but the distortion of the line current due to the sudden change of the dc-link is smaller with the proposed sampling method compared to the traditional sampling method.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2947864, IEEE Transactions on Industrial Electronics

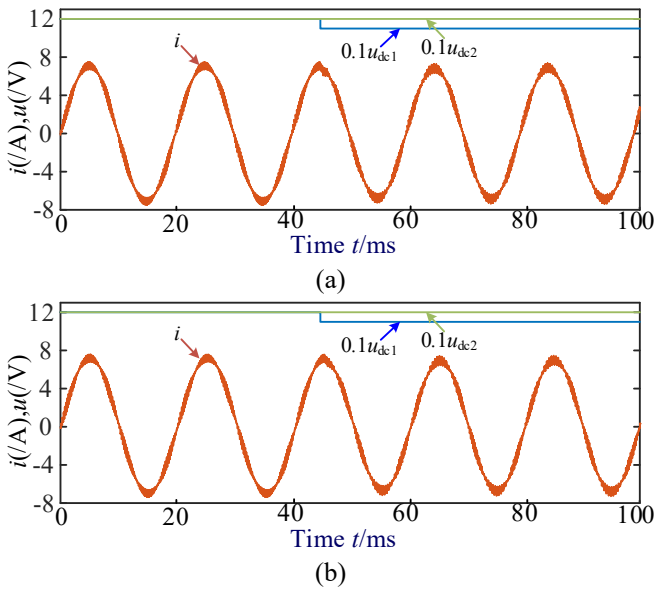


Fig. 17. The simulation results in the condition of the sudden change of the dc-link voltage. (a) the traditional multi-sampling method. (b) the proposed multi-sampling method.

B. Experimental results

Fig. 18(a) and Fig. 18(b) show the measured inverter current in the traditional multi-sampling method with same parameters of the PR controller. It can be seen that the steady status results of the experimental test in the traditional method and the proposed method are almost same, which is similar to the simulation results.

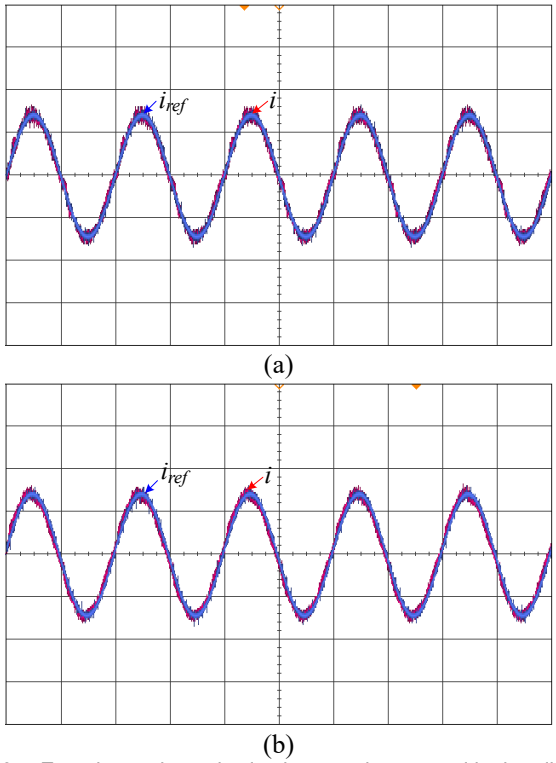


Fig. 18. Experimental results in the steady state with the different multi-sampling methods. (a) the traditional multi-sampling method. (b) the proposed multi-sampling method. (*i*: 5 A/div, Time: 10 ms/div).

Fig. 19(a) shows that the current controller in the traditional multi-sampling method becomes unstable with the increase of the proportional gain from 20 Ω to 30 Ω. In the proposed multi-sampling method shown in Fig. 19(b), the resonance will happen if the proportional gain increases from 45 Ω to 55 Ω. The experimental results are coincident with theoretical analysis.

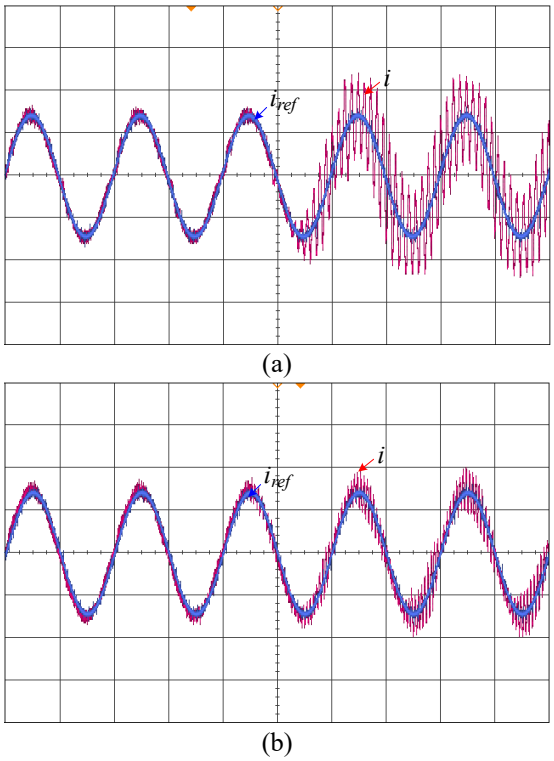
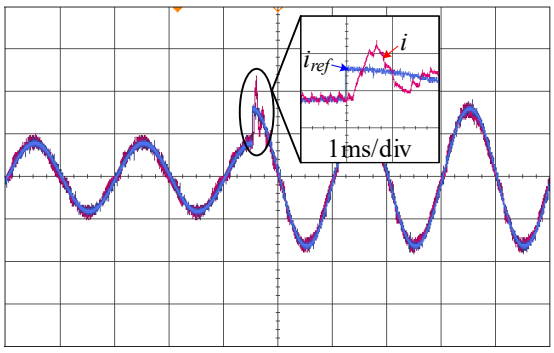
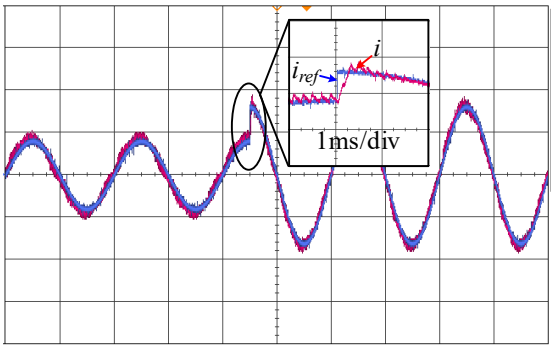


Fig. 19. Experimental results in the unstable state with the different sampling method. (a) the traditional multi-sampling method. (b) the proposed multi-sampling method. (*i*: 5 A/div, Time: 10 ms/div).

Fig. 20 shows experimental results in the condition of the sudden change of the line current. The parameters of PR controller in the experimental test the the same with that in the simulation. The grid current will faster track its reference with a smaller overshoot in the proposed multi-sampling method compared to the traditional multi-sampling method. It verifies that the bandwidth of the control loop is improved in the proposed sampling method.



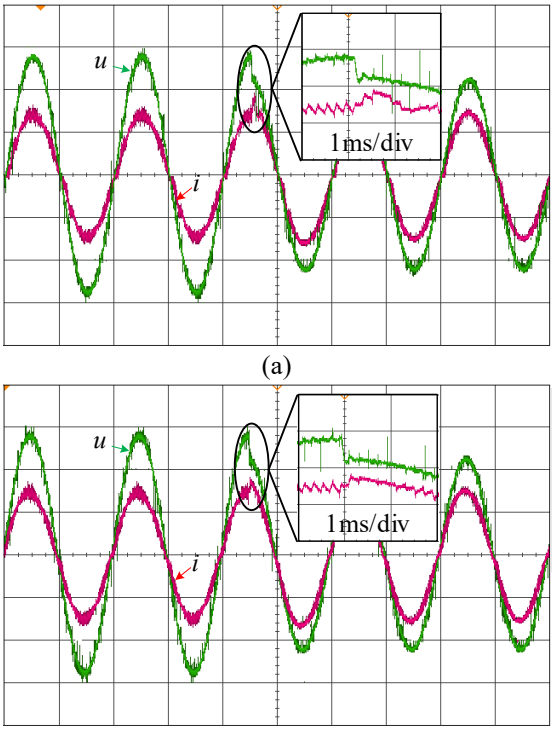
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2947864, IEEE Transactions on Industrial Electronics



(b)

Fig. 20. Experimental results in the condition of the sudden change of reference current. (a) the traditional multi-sampling method. (b) the proposed multi-sampling method. (*i*: 5 A/div, Time: 10 ms/div).

Fig. 21 shows experimental results in the gird voltage sag condition. In this case, the grid current distortion in the proposed method is smaller than that in the traditional method, and the grid current faster recover in the proposed method in contrast with the traditional method. The experimental results also verify that the bandwidth of the control loop in the proposed sampling method is larger than that in the traditional method.

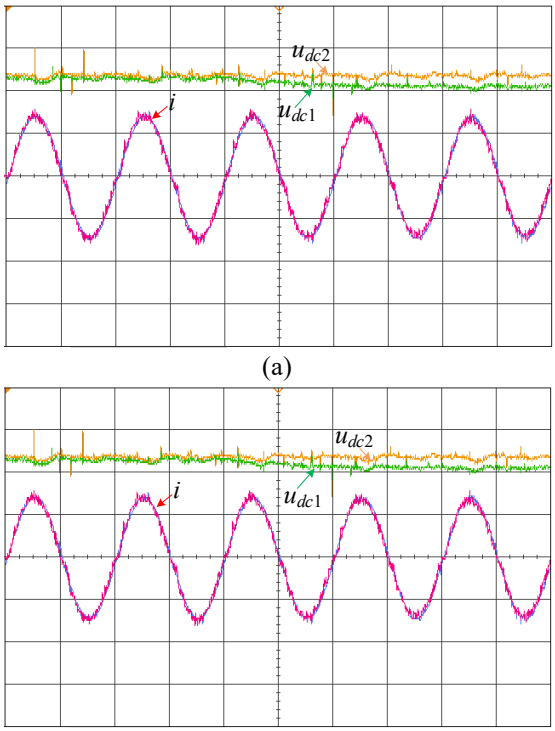


(a)

(b)

Fig. 21. Experimental results in the condition of the sudden change of the grid voltage amplitude. (a) the traditional multi-sampling method. (b) the proposed multi-sampling method. (*u*: 50 V/div, *i*: 5 A/div, Time: 10 ms/div).

Fig. 22 shows experimental results in the condition of the dc-link voltage sudden change, where since there exists the output impedance in the DC source supply, the dc-link voltage is not a constant value, and the sudden change of the dc-link voltage is not ideal. However, it can be seen from this experimental test that the effect of the dc-link voltage change on the grid current is slight both in the traditional method and the proposed method. the experimental results are similar to the simulation results shown in Fig. 17.



(a)

(b)

Fig. 22. Experimental results in the condition of the sudden change of the dc-link voltage. (a) the traditional multi-sampling method. (b) the proposed multi-sampling method. (u_{dc1} ,u_{dc2}: 50 V/div, *i*: 5 A/div, Time: 10 ms/div).

VI. Conclusion

This paper has proposed a multi-sampling method for single-phase grid-connected CHB multilevel converters modulated by PSC-PWM. From the theoretical analysis and the experimental verification, following conclusions can be drawn: 1) Compared to traditional sampling methods, the proposed sampling method can effectively reduce the time delay and improve dramatically the bandwidth of the current control loop. 2) The proposed sampling method can achieve the minimum sampling interval, which can always satisfy voltage-second balance in the modulation process and avoid sampling the current ripple caused by the switching action. The sampling interval for traditional sampling methods, which can avoid breaking the voltage-second balance in the modulation process, is the integer times of that for the proposed sampling method.

References

[1] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858-867, Aug. 2002.

[2] S. Rojas and A. Gensior, "Instantaneous average prediction of the currents in a PWM-controlled two-level converter," *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 397-406. 2019.

[3] F. Chen, "Weighted double sampling to obtain the average value of triangular current for accurate droop control in DC power distribution systems," *IEEE Trans. Ind. Electron*., vol. 66, no. 11, pp. 8733-8740. 2019.

[4] S. Buso and P. Mattavelli, *Digital control in power electronics*, 2nd ed., San Rafael, CA, USA: Morgan & Claypool, 2015.

[5] L. Corradini and P. Mattavelli, "Analysis of multiple sampling technique for digitally controlled dc-dc converters," in *IEEE Power Electron. Specialists Conf.*, Jun. 2006, pp. 1-6.

[6] X. Wang, F. Blaabjerg, and P. C. Loh, "Grid-current-feedback active damping for LCL resonance in grid-connected voltage-source converters," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 213-223, Jan. 2016.

[7] X. Wang, P. C. Loh, and F. Blaabjerg, "Stability analysis and controller synthesis for single-loop voltage-controlled VSIs," *IEEE Trans. Power Electron.*, vol. 1, no. 99, pp. 1-1, Mar. 2017.

[8] X. Wang, F. Blaabjerg, and P. C. Loh, "Passivity-based stability analysis and damping injection for multiparalleled VSCs with LCL filters," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8922-8935. 2017..

[9] L. Harnefors, L. Zhang, and M. Bongiorno, "Frequency-domain passivity-based current controller design," *IET Power Electron.*, vol. 1, no. 4, pp. 455-465. 2008.

[10] P. Zanchetta, D. B. Gerry, V. G. Monopoli, J. C. Clare, and P. Wheeler, "Predictive current control for multilevel active rectifiers with reduced switching frequency," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 163-172, Jan. 2008.

[11] W. Kai and M. Ferdowsi, "Reducing computational time delay in digital current-mode controllers for dc-dc converters," in *Proc. IEEE 30th Inter. Tele. Energy Conf.*, Sep. 2008, pp. 1-4.

[12] B. S. Nesimioglu and M. T. Soylemez, "Calculation of all gains providing time-delay independent stability via root locus," in *Proc. 2014 Inter. Conf. on Control, Decision and Inform. Tech.*, Nov. 2014, pp. 566-571.

[13] M. Oettmeier, C. Heising, V. Staudt, and A. Steimel, "Dead-beat control algorithm for single-phase 50-kw AC railway grid representation," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1184-1192, May. 2010.

[14] P. Jintakosonwit, H. Fujita, and H. Akagi, "Control and performance of a fully-digital-controlled shunt active filter for installation on a power distribution system," *IEEE Trans. Power Electron.*, vol. 17, no. 1, pp. 132-140, Jan. 2002.

[15] D. Yang, X. Ruan, and H. Wu, "A real-time computation method with dual sampling mode to improve the current control performance of the LCL-type grid-connected inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4563-4572, Jul. 2015.

[16] L. Corradini, P. Mattavelli, E. Tedeschi, and D. Trevisan, "High-bandwidth multisampled digitally controlled DC-DC converters using ripple compensation," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1501-1508. 2008.

[17] L. Corradini, E. Tedeschi, and P. Mattavelli, "Advantages of the symmetric-on time modulator in multiple-sampled digitally controlled DC-DC converters," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2007, pp. 1974-1980.

[18] X. Zhang, P. Chen, C. Yu, F. Li, H. T. Do, and R. Cao, "Study of current control strategy based on multi-sampling for high-power grid-connected inverters with LCL-filter," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5023-5034, Jul. 2016.

[19] H. Fujita, "A single-phase active filter using an H-Bridge PWM converter with a sampling frequency quadruple of the switching frequency," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 934-941, Jul. 2009.

[20] M. Odavic, V. Biagini, M. Sumner, P. Zanchetta, and M. Degano, "Multi-sampled carrier-based PWM for multilevel active shunt power filters for aerospace applications," in *Proc. IEEE Energy Convers. Congr. and Expo. (ECCE)*, Sep. 2011, pp. 1483-1488.

[21] Z. Liu, B. Liu, S. Duan, and Y. Kang, "A novel DC capacitor voltage balance control method for cascade multilevel statcom," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 14-27. 2012.

[22] W. Song, X. Feng, and K. M. Smedley, "A carrier-based PWM strategy with the offset voltage injection for single-phase three-level neutral-point-clamped converters," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1083-1095, Aug. 2013.

[23] F. Golnaraghi and B. C. Kuo, *Automatic control systems*, 9th, USA: Wiley, 2009, pp. 412.

Junpeng Ma (S'15, M'18) received the B.S. degree and the Ph.D. degree from Southwest Jiaotong University in 2013 and 2018, respectively.

He was as a guest Ph.D. student at Aalborg University during Nov. 2017 to May 2018. Now, He is an associate research fellow in College of Electrical Engineering, Sichuan University.

His research topics include the modeling and control of grid-connected multilevel converters applied in the traction drive system, the new energy field, and the HVDC system.

In 2019, He received the best paper award at IEEE CIEEC.

Xiongfei Wang (S'10-M'13-SM'17) received the B.S. degree from Yanshan University, Qinhuangdao, China, in 2006, the M.S. degree from Harbin Institute of Technology, Harbin, China, in 2008, both in electrical engineering, and the Ph.D. degree in energy technology from Aalborg University, Aalborg, Denmark, in 2013.

Since 2009, he has been with the Department of Energy Technology, Aalborg University, where he became Assistant Professor in 2014, Associate Professor in 2016, Professor and Research Program Leader for Electronic Power Grid (eGrid) in 2018. His current research interests include modeling and control of grid-interactive power converters, stability and power quality of power electronic based power systems, active and passive filters.

Dr. Wang was selected into Aalborg University Strategic Talent Management Program in 2016. He received six IEEE prize paper awards, the 2016 outstanding reviewer award of IEEE TRANSACTIONS ON POWER ELECTRONICS, the 2018 IEEE PELS Richard M. Bass Outstanding Young Power Electronics Engineer Award, the 2019 IEEE PELS Sustainable Energy Systems Technical Achievement Award, and the 2019 Highly Cited Researcher in the Web of Science. He serves as an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.

Frede Blaabjerg (S'86–M'88–SM'97–F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 500 journal papers in the fields of power electronics and its applications. He is the co-author of two monographs and editor of 6 books in power electronics and its applications.

He has received 24 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014 and the Villum Kann Rasmussen Research Award 2014. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018.

He is nominated in 2014, 2015, 2016 and 2017 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world. In 2017 he became Honoris Causa at University Politehnica Timisoara (UPT), Romania.

Shunliang Wang (M'18) received the B.S. and Ph.D. degrees in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2010 and 2016, respectively.

From 2017 to 2018, he was a Visiting Scholar in the Department of Energy Technology, Aalborg University, Denmark. He is currently an Associate Research Fellow in the College of Electrical Engineering, Sichuan University. His current research interests include digital control and modulation of power converters in high voltage direct current, and railway traction systems.

Dr. Wang received the best paper award at IEEE CIEEC 2019.

Wensheng Song (M'13**)** received the B.S. degree in electronic and information engineering, the Ph.D. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2006 and 2011, respectively, where he is currently a Professor in the school of Electrical Engineering.

From Sep. 2009 to Sep. 2010, he was a visiting scholar with the department of electrical engineering and computer science, University of California, Irvine, USA. From Jul. 2015 to Dec. 2015, he was a visiting scholar at University of Alberta, Edmonton, Canada. His current research interests include digital control and modulation methods of electrical AC-DC-AC railway traction drive systems, and multilevel converters.

Tianqi Liu (SM'16) received the B.S. and the M.S. degrees from Sichuan University, Chengdu, China, in 1982 and 1986, respectively, and the Ph.D. degree from Chongqing University, Chongqing, China.

She is currently a Professor with College of Electrical Engineering, Sichuan University. Her main research interests include power system analysis and stability control, HVDC, optimal operation, dynamic security analysis, dynamic state estimation, and load forecast.