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Virtual-Flux-Based Passivation of Current Control for Grid-Connected VSCs

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***Abstract*—This letter proposes a passivity-based current control scheme for voltage-source converters, featuring a virtual-flux-based damper and a passive output admittance with a wide range of time delay involved in the current control loop. The admittance modeling and experimental tests validate the effectiveness of the approach.**

***Index Terms*—Passivity, stability, current control, delay.**

I. Introduction

The harmonic stability caused by the dynamic interactions of voltage-source converters (VSCs) and the electrical grid is threatening the security of electricity supply [1]. The varying topologies and conditions of power systems further challenge the analysis and mitigation of harmonic instability [2].

The passivity-based control of VSCs recently emerges as a promising way to tackle the instability challenge [3]. The concept of passivity in the frequency domain implies that the real part of the output admittance of VSC, i.e. Y_{VSC}, is nonnegative [4], which ensures that VSC will not destabilize the power system [5]. It has been recently found that the high-frequency (e.g. from 200 Hz up to the Nyquist frequency) characteristic of Y_{VSC} is dominated by the current control (CC) loop [3], and the time delay involved in the CC loop is identified as the main cause for the negative-real-part of Y_{VSC} in the high frequency range [5]-[7].

Considering that the time delay is typically one and a half sampling period ($1.5T_s$) in digital control systems [8], several active damping schemes have been developed to minimize the negative-real-part region [5]-[6]. However, only the method reported in [5] can ensure the nonnegative real part of Y_{VSC} up to the Nyquist frequency, yet it requires the use of a voltage derivative term (namely dev_AD) in the voltage feedforward loop, which is sensitive to high-frequency noise. Moreover, the time delay in the control of modular multilevel converters and, particularly in the high-voltage direct-current systems, can be much longer than $1.5T_s$, ranging from $3T_s$ to $6T_s$, due to the complexity in the control of thousands of submodules [9]. As will be revealed in this letter, the dev_AD method fails to ensure the passivity of Y_{VSC} when the delay is longer than $1.5T_s$.

To address the passivity of the CC loop with a wide range of time delay, a virtual-flux-based active damping (VF_AD) method is proposed in this letter. The approach is easy to implement and fully removes time delay terms in Y_{VSC}, which guarantees its passivity with any time delay in the CC loop. The small-signal modeling and experimental tests are presented, which corroborate the effectiveness of the proposed method.

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II. Passivity-Based Analysis of Current Control

A. Grid-Connected Voltage-Source Converter

Fig. 1(a) shows the single-line diagram of a grid-connected three-phase VSC with the CC implemented in the $\alpha\beta$-frame. L_f is the filter inductor and Z_g represents the grid impedance. v_{PCC} and i_{PCC} are the voltage and current at the point of common coupling (PCC) of VSC, respectively. i_{dqref} and $i_{\alpha\beta ref}$ are current references in the dq- and $\alpha\beta$-frame, respectively. The CC loop is used to control the output current of VSC (which is equal to i_{PCC}) to follow its reference. Since the focus of this letter is the passivity of the CC loop, the phase-locked loop (PLL) is designed with a low bandwidth to avoid the low-frequency instability [1], and a constant dc-link voltage can also be assumed, which is justified by:

1) The dc-link voltage is controlled by the direct voltage control (DVC) loop to generate i_{dref}. The bandwidth of the DVC is usually well below the fundamental frequency [3].

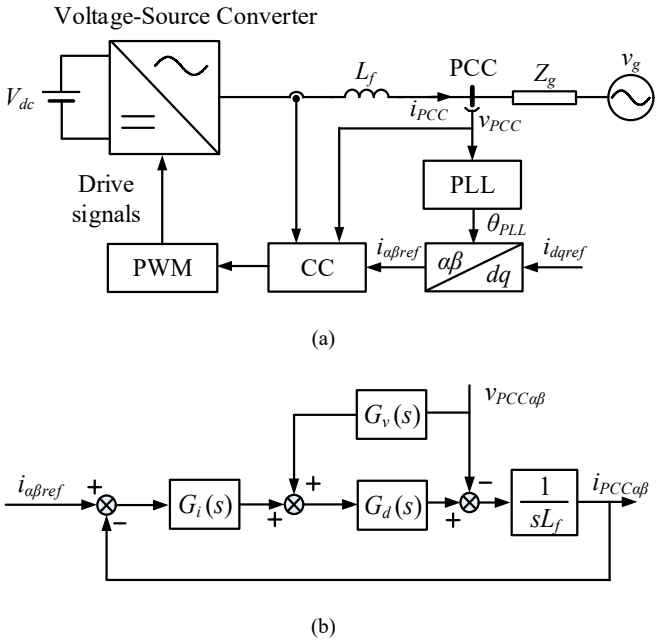

Fig. 1. Grid-connected VSC with the CC implemented in the $\alpha\beta$-frame. (a) System diagram. (b) CC diagram.

Hence, the dc-link voltage ripple is attenuated by the DVC and will not be reflected in i_{dref}.

2) The dc-link voltage ripple compensation is usually adopted in the pulse width modulation (PWM) [10], with which, the dc-link voltage ripple would not affect the dynamics of the ac voltage and current of VSC [10].

Fig. 1(b) illustrates the block diagram of the used $\alpha\beta$-frame CC. $G_i(s)$ denotes the proportional + resonant (PR) current controller. $G_d(s)$ represents the transfer function of the time delay, i.e., $G_d(s)=e^{-sTd}$, where T_d is the time delay [3]. $G_v(s)$ is the active damping controller based on the feedforward of the PCC voltage.

Based on Fig. 1(b), the output current of VSC can be expressed as [5]

$$i_{PCC\alpha\beta}=\underbrace{\frac{G_i(s)e^{-sT_d}}{sL_f+G_i(s)e^{-sT_d}}}_{H(s)}i_{\alpha\beta ref}-\underbrace{\frac{1-G_v(s)e^{-sT_d}}{sL_f+G_i(s)e^{-sT_d}}}_{Y_{VSC}(s)}v_{PCC\alpha\beta}. \quad (1)$$

where $H(s)$ is the closed-loop transfer function between $i_{\alpha\beta ref}$ and $i_{PCC\alpha\beta}$, and $Y_{VSC}(s)$ is the output admittance of VSC with the CC loop.

It is known from [5] that the stability of VSCs connected with the passive grid impedance can be guaranteed if 1) $H(s)$ is stable, and 2) $Y_{VSC}(s)$ is passive. While 1) can be easily guaranteed by properly tuning the PR controller parameters, the passivity of $Y_{VSC}(s)$ required by 2) is hard to achieve, due to the impact of the time delay, which will be detailed in the following part. The main circuit and controller parameters used in the following analysis and experimental tests are given in Table I.

TABLE I
MAIN CIRCUIT AND CONTROLLER PARAMETERS

SYMBOL	DESCRIPTION	VALUE (P.U.)
V_{PCC}	PCC voltage (RMS value)	110 V (1 p.u.)
P	Power rating of the VSC	3 kW (1 p.u.)
f_g	Grid frequency	50 Hz (1 p.u.)
L_f	Filter inductance	3 mH (0.08 p.u.).
f_{sw}	Switching frequency	10 kHz (20 p.u.)
T_s	Sampling (control) period	100 μs (0.05 p.u.)
T_d	Time delay in the CC loop	3.5T_s (0.175 p.u.)
K_p	P gain of the PR controller	0.37 p.u.
K_r	R gain of the PR controller	22.1 p.u.

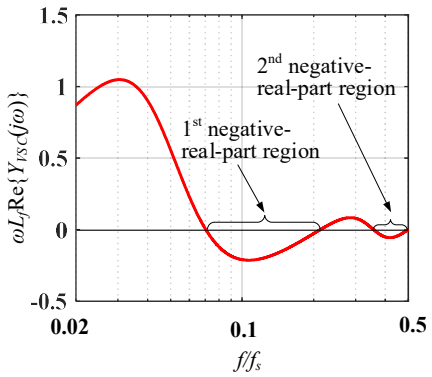

Fig. 2. Re$\{Y_{VSC}(j\omega)\}$ with PR controller only and T_d=3.5T_s.

B. Passivity-Based Analysis

1) With PR controller only

First, only the current controller without the active damping, i.e. $G_v(s)$=0, is considered. Since the R controller is merely designed to eliminate the steady-state current tracking error at the grid fundamental frequency, it can be neglected when analyzing the high-frequency characteristic of Y_{VSC} [6]. Hence, $G_i(s)$ can be simplified as the proportional gain, i.e., $G_i(s)\approx K_p$. Consequently, $Y_{VSC}(s)$ can be simplified as:

$$Y_{VSC}(s)=\frac{1}{sL_f+K_pe^{-sT_d}}. \quad (2)$$

Substituting '$s=j\omega$' into (2), the real part of $Y_{VSC}(s)$, i.e. Re$\{Y_{VSC}(j\omega)\}$ can be obtained as

$$\mathrm{Re}\{Y_{VSC}(j\omega)\}=\frac{K_p\cos(\omega T_d)}{(\omega L_f-K_p)^2+2\omega L_fK_p[1-\sin(\omega T_d)]}. \quad (3)$$

Since the denominator of (3) is always larger than zero, the sign of Re$\{Y_{VSC}(j\omega)\}$ is determined by the numerator. The frequency range of the negative-real-part region can be obtained by solving $K_p\cos(\omega T_d)<0$, which leads to

$$f_{neg\_real}\in\left(\frac{n+0.25}{T_d},\frac{n+0.75}{T_d}\right),\ n\in\mathbb{N}. \quad (4)$$

For T_d =1.5T_s, the frequency range of the single negative-real-part region within the Nyquist frequency is obtained by substituting n=0 into (4), which leads to $f_{neg\_real}\in(f_s/6,f_s/2)$ [5]-[7].

However, when the time delay T_d is increased, there tends to be multiple negative-real-part regions below the Nyquist frequency. For T_d =3.5T_s considered in this letter, n=0 and 1 lead to two negative-real-part regions with frequency ranges $f_{neg\_real}\in(f_s/14,\ 3f_s/14)\cup(5f_s/14,\ f_s/2)$, as illustrated in Fig. 2, where Re$\{Y_{VSC}(j\omega)\}$ is normalized by multiplying ωL_f to obtain dimensionless values [5] .

2) PR controller plus dev_AD

The dev_AD scheme reported in [5] is used to eliminate the negative-real-part region. By selecting $G_v(s)=K_{ad}s$, Re$\{Y_{VSC}(j\omega)\}$ is expressed as

$$\mathrm{Re}\{Y_{VSC}(j\omega)\}=\frac{\cos(\omega T_d)(K_p-\omega^2K_{ad}L_f)}{(\omega L_f-K_p)^2+2\omega L_fK_p[1-\sin(\omega T_d)]}. \quad (5)$$

where $K_{ad}=4T_d^2K_p/(\pi^2L_f)$. The term $(K_p-\omega^2K_{ad}L_f)$ in the numerator becomes negative at the same frequency as the term $\cos(\omega T_d)$, i.e. $\omega=\pi/(2T_d)$, which removes the 1st negative-real-part region in Fig. 2 [5]. However, it should be noted that $(K_p-\omega^2K_{ad}L_f)<0$ always holds for $\omega>\pi/(2T_d)$, which leads to Re$\{Y_{VSC}(j\omega)\}<0$ whenever the term $\cos(\omega T_d)$ is positive. The frequency range of negative-real-part regions can be calculated as $f_{neg\_real}\in((n+0.75)/T_d,\ (n+1.25)/T_d)$, $n\in\mathbb{N}$. Such negative-real-part regions are above the Nyquist frequency if T_d =1.5T_s,

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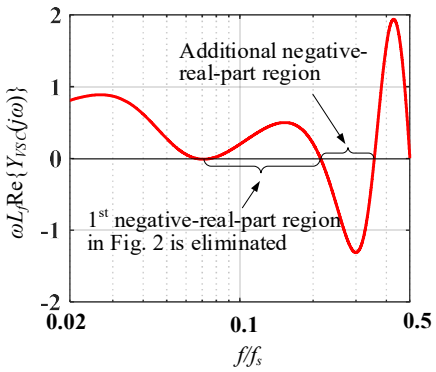

Fig. 3. $\mathrm{Re}\{Y_{VSC}(j\omega)\}$ with PR controller plus dev_AD and T_d=3.5T_s.

and hence, are not considered in [5]. Yet, they are within the Nyquist frequency if the time delay in the CC loop is longer than 1.5T_s. Fig. 3 illustrates $\mathrm{Re}\{Y_{VSC}(j\omega)\}$ with T_d=3.5T_s. It is clear that the additional negative-real-part region is introduced even though the 1st negative-real-part region in Fig. 2 is eliminated.

III. Virtual-Flux-Based Active Damping

A. General Idea

It can be observed from (1) that the delay terms appear both in the numerator and denominator of $Y_{VSC}(s)$, which can be cancelled out with each other by selecting $G_v(s) = -K_p/(sL_f)$, i.e.,

$$Y_{VSC}(s)=\frac{1-G_v(s)e^{-sT_d}}{sL_f\left(1+\frac{K_p}{sL_f}e^{-sT_d}\right)}=\frac{1+\frac{K_p}{sL_f}e^{-sT_d}}{sL_f\left(1+\frac{K_p}{sL_f}e^{-sT_d}\right)}=\frac{1}{sL_f} \quad (6)$$

.

Since the integral of the PCC voltage leads to the virtual flux (VF) [11], the proposed method is here named as VF_AD. It is known from (6) that the VF_AD scheme fully eliminates the impact of the time delay. The output admittance of VSC with the CC loop is shaped as the filter reactance, and is always passive.

Remark 1: After using the proposed VF_AD, the anti-voltage disturbance capability of VSC is solely determined by the passive filter, and is decoupled from the proportional gain of the current controller. To further improve the harmonic voltage disturbance rejection capability of VSC, the additional harmonic controllers/filters need to be added in the current controller as well as the PCC voltage-feedforward loop. The relevant research works can be found in [12]-[13], where the harmonic controllers/filters need to be properly tuned to avoid jeopardizing the passivity of the CC loop [12]-[13].

Remark 2: $Y_{VSC}(s)$ with the dq-frame CC can be obtained from (1) by applying the frequency translation, i.e., $s \rightarrow s-j\omega_g$, to $G_i(s)$ [14]. However, the high-frequency negative-real-part of $Y_{VSC}(s)$ is mainly determined by the proportional gain of $G_i(s)$, which is not affected by the frequency translation [5]. Hence, the proposed VF_AD can also be implemented in the dq-frame CC by adding the active damping term after the dq to $\alpha\beta$ transformation of the CC output.

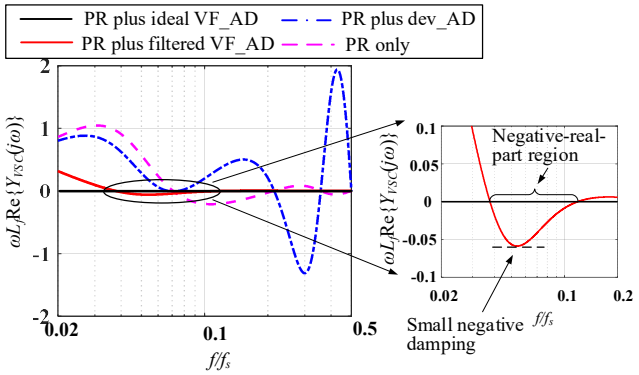

Fig. 4. $\mathrm{Re}\{Y_{VSC}(j\omega)\}$ with different control schemes and T_d=3.5T_s. Solid black line: PR controller plus ideal VF_AD. Solid red line: PR controller plus filtered VF_AD. Dashed-dotted line: PR controller plus dev_AD. Dashed line: PR controller only.

B. Practical Implementation

Several modifications are required for implementing the VF_AD scheme in practice. First, the integrator in $G_v(s)$ introduces a high gain at the fundamental frequency, which affects the current tracking performance. This side effect can be avoided by adding a notch filter in $G_v(s)$, which is expressed as

$$G_{notch}(s)=\frac{s^2+\omega_g^2}{s^2+2\omega_c s+\omega_g^2}. \quad (7)$$

where ω_g represents the grid fundamental frequency, $\omega_c = \pi$ rad/s is selected to guarantee the adaptation of $G_{notch}(s)$ to the variation of ω_g in the range of ±0.5 Hz. It is worth mentioning that the notch filter only affects system dynamics around the fundamental frequency, and thus, has little impact on the high-frequency characteristic of Y_{VSC}.

Second, the voltage sensor may have a small dc offset, and it can lead to a large dc bias in the VF due to the infinite dc gain of the pure integrator in $G_v(s)$, which finally causes the malfunction of VSC [11]. The typical solution is the use of a low pass filter (LPF) $1/(s+\omega_f)$ to mimic the pure integrator $1/s$ while avoiding its infinite dc gain, where ω_f is the cut-off frequency of the LPF. The smaller ω_f yields better emulation of the integrator, but worsen the dynamic performance. Hence, a tradeoff is needed for selecting ω_f. It is known from (4) that the delay-induced negative-real-part region starts from $f_{critical}$ =$1/(4T_d)$. In order to guarantee a good approximation of the integrator in the frequency range beyond $f_{critical}$, ω_f =$0.05\cdot(2\pi f_{critical})$ is selected in this letter. Hence, the practical implementation of $G_v(s)$ is modified as

$$G_{v\_pra}(s)=-\frac{K_p}{L_f}\frac{1}{s+\omega_f}G_{notch}(s). \quad (8)$$

Fig. 4 shows a comparison of $\mathrm{Re}\{Y_{VSC}(j\omega)\}$ with different control schemes. It can be clearly observed that the negative-real-part region is fully eliminated by using the ideal VF_AD given by (6). Yet, a negative-real-part region still remains with the filtered VF_AD given by (8), due to the adoption of the LPF instead of the pure integrator in $G_v(s)$, as the zoom-in figure shown in Fig. 4. Nevertheless, the magnitude of the negative $\mathrm{Re}\{Y_{VSC}(j\omega)\}$ is significantly reduced by using the

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filtered VF_AD compared with the existing methods (i.e., the PR controller only and the PR controller plus dev_AD). In practice, such a small negative damping of VSC is usually mitigated by the parasitic resistance of the passive-network, and hence, will not destabilize the system [7].

C. Robustness Analysis

It is known from (8) that implementing the filtered VF_AD requires the knowledge of L_f, whose actual value (L_{f_actual}) might have ±10% deviation from its nominal value ($L_{f\_nominal}$) due to the component tolerance [15].

Fig. 5 shows a comparison of $\mathrm{Re}\{Y_{VSC}(j\omega)\}$ with the filtered VF_AD by considering ±10% variations of L_f. It can be seen that the negative-real-part regions are changed when $L_{f\_actual} \neq L_{f\_nominal}$, but their magnitudes are still much smaller compared with the case where the VF_AD is not used, as the blue and black dash-dotted lines shown in Fig. 5. Therefore, the proposed VF_AD performs robustly in keeping a small negative $\mathrm{Re}\{Y_{VSC}(j\omega)\}$ against filter inductance variations.

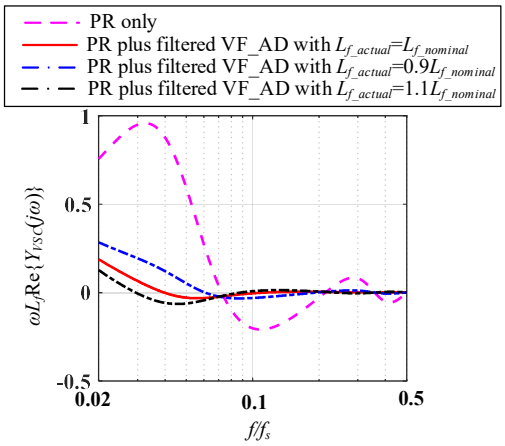


Fig. 5. Robustness analysis of the filtered VF_AD against filter inductance variations. Dashed line: PR controller only. Solid line: PR controller plus filtered VF_AD with $L_{f\_actual} = L_{f\_nominal}$. Blue dashed-dotted line: PR controller plus filtered VF_AD with $L_{f\_actual} = 0.9L_{f\_nominal}$. Black dashed-dotted line: PR controller plus filtered VF_AD with $L_{f\_actual} = 1.1L_{f\_nominal}$.

IV. Experimental Results

To verify the effectiveness of the proposed method. The experimental tests are carried out by using a VSC with parameters in Table I. The grid impedance is represented by the *CL* filter, with which, the grid resonance frequency can be freely tuned by changing the grid capacitance C_g and grid inductance L_g.

Fig. 6 (a) plots output admittances of VSC with different control schemes and the grid admittance with L_g= 6 mH and C_g=10μF. It can be seen that the grid admittance intersects VSC admittance in its negative-real-part region if only the PR controller is used in the CC loop, which leads to -10° phase margin (PM). Hence, the system will be unstable. Nevertheless, the system can still be stabilized by adding the dev_AD and the VF_AD. These theoretical analyses are further verified by experimental tests shown in Fig. 7. To avoid the possible damage, the VSC will be blocked in the experiment if the oscillation is amplified, as shown in Fig. 7(a).

Fig. 6 (b) plots output admittances of VSC with different control schemes and the grid admittance with L_g= 6 mH and C_g=4μF. Due to the reduced grid capacitance, the grid admittance intersects with VSC admittance at the higher frequency, which falls into its negative-real-part region if only the PR controller, or PR controller plus dev_AD is used in the CC loop. Therefore, VSC will be unstable with these two control schemes. Yet, VSC can still be stabilized by using the proposed VF_AD, thanks to the widened nonnegative-real-part region. These stability analyses are further verified by the experimental tests given by Fig. 8.

V. Conclusion

This letter has proposed a virtual-flux-based active damping that fully eliminates the destabilization effect of the time delay in the current control loop. The output admittance of VSC is shaped as the passive reactance by using the proposed method, with which, the stability robustness of VSC with a wide range of grid impedance is enhanced. The experimental tests are carried out to corroborate the effectiveness of the proposed method.

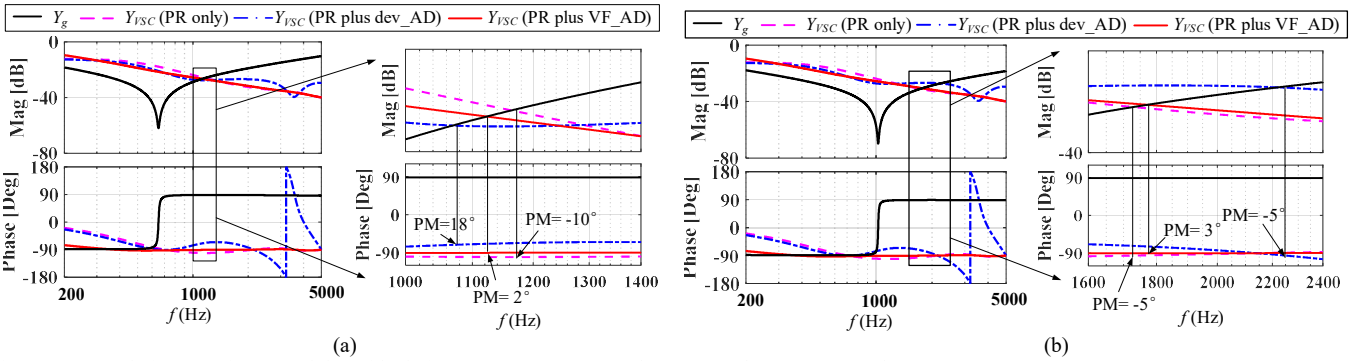
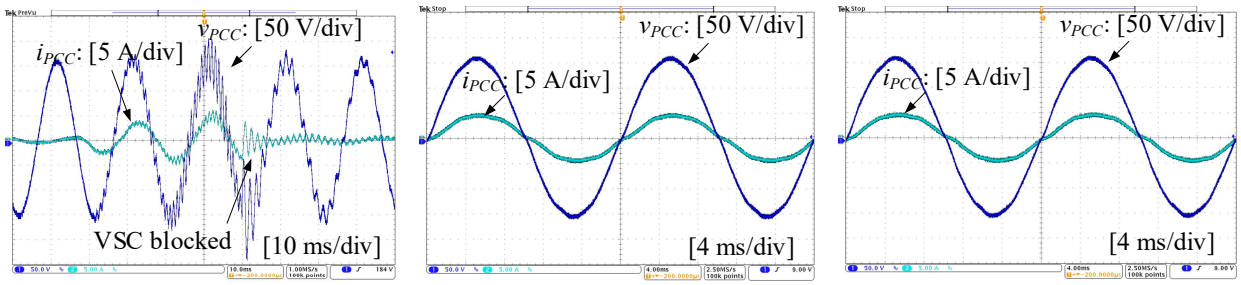
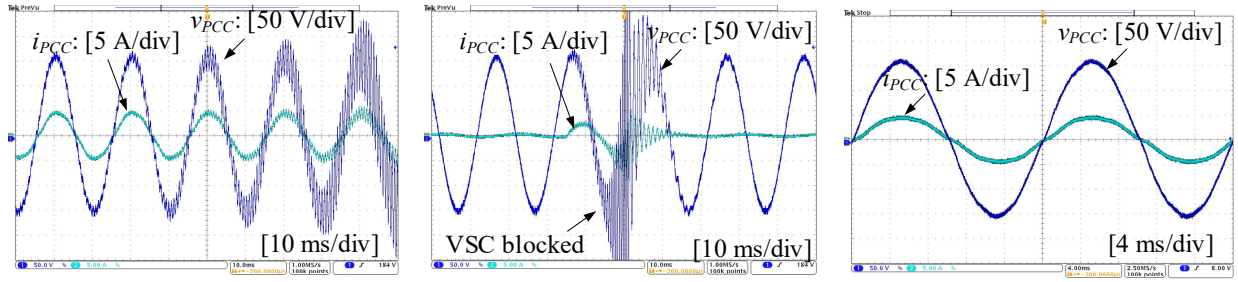


Fig. 6. Output admittance of VSC and the grid admittance. (a) L_g= 6 mH and C_g=10μF. (b) L_g= 6 mH and C_g= 4μF.



(a) (b) (c)

Fig. 7. Experimental results with L_g= 6 mH and C_g=10μF. (a) PR controller only, unstable. (b) PR controller plus dev_AD, stable. (c) PR controller plus VF_AD, stable.



(a) (b) (c)

Fig. 8. Experimental results with L_g= 6 mH and C_g=4μF. (a) PR controller only, unstable. (b) PR controller plus dev_AD, unstable. (c) PR controller plus VF_AD, stable.

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