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An Input Power-Aware Maximum Efficiency Tracking Technique for Energy Harvesting in IoT Applications

Sanad Fares Yousef Kawar

SANTA CLARA UNIVERSITY

Department of Electrical and Computer Engineering

Date: August 18, 2020

I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY

Sanad Fares Yousef Kawar

ENTITLED

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BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY IN ELECTRICAL ENGINEERING

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By

Sanad Fares Yousef Kawar

Dissertation

Submitted in Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy
in Electrical Engineering
in the School of Engineering at
Santa Clara University, 2020
Santa Clara, California

Dedication

To my wife, Heidi, for walking this journey with me, celebrating its joys and enduring its challenges.

To my son, Fares, who was born one week before I defended this dissertation, ushering in a new season in our lives.

To my parents, Fares and Ibtissam, for all the time, effort, and resources they have invested in me throughout the years.

To my brother, Zaid, for believing in me and supporting me and for always standing by my side.

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I cannot leave SCU without acknowledging Campus Ministry. Working with them as a Spirituality Facilitator allowed me to experience SCU's mission of educating the whole person. I genuinely appreciate the supportive community I was a part of and the resources

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Last but certainly not least, I would like to express my deepest appreciation to my family for their relentless support. I am sincerely grateful to my wife Heidi, who has moved across the world with me to pursue this, for her unwavering spiritual, emotional, and practical support that enabled me to complete this work. I could not have come this far without her selfless care and sacrifices. I'm also deeply indebted to my parents, Fares and Ibtissam, and my brother, Zaid, for always believing in me and for their unparalleled encouragement, support, and prayers. I would also like to extend my sincere thanks to my grandmother, Insaf, my parents-in-law, Jamal and Laila, my brothers-in-law, sisters-in-law, uncles and their families for their support and prayers. Above all, I am thankful to God for His faithfulness, for blessing me with this opportunity and giving me the grace, guidance, and strength to persevere to the finish line.

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ABSTRACT

The Internet of Things (IoT) enables intelligent monitoring and management in many applications such as industrial and biomedical systems as well as environmental and infrastructure monitoring. As a result, IoT requires billions of wireless sensor network (WSN) nodes equipped with a microcontroller and transceiver. As many of these WSN nodes are off-grid and small-sized, their limited-capacity batteries need periodic replacement. To mitigate the high costs and challenges of these battery replacements, energy harvesting from ambient sources is vital to achieve energy-autonomous operation. Energy harvesting for WSNs is challenging because the available energy varies significantly with ambient conditions and in many applications, energy must be harvested from ultra-low power levels.

To tackle these stringent power constraints, this dissertation proposes a discontinuous charging technique for switched-capacitor converters that improves the power conversion efficiency (PCE) at low input power levels and extends the input power harvesting range at which high PCE is achievable. Discontinuous charging delivers current

to energy storage only during clock non-overlap time. This enables tuning of the output current to minimize converter losses based on the available input power. Based on this fundamental result, an input power-aware, two-dimensional efficiency tracking technique for WSNs is presented. In addition to conventional switching frequency control, clock non-overlap time control is introduced to adaptively optimize the power conversion efficiency according to the sensed ambient power levels.

The proposed technique is designed and simulated in 90nm CMOS with post-layout extraction. Under the same input and output conditions, the proposed system maintains at least 45% PCE at 4μW input power, as opposed to a conventional continuous system which requires at least 18.7μW to maintain the same PCE. In this technique, the input power harvesting range is extended by 1.5x.

The technique is applied to a WSN implementation utilizing the IEEE 802.15.4-compatible GreenNet communications protocol for industrial and wearable applications. This allows the node to meet specifications and achieve energy autonomy when deployed in harsher environments where the input power is 49% lower than what is required for conventional operation.

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CHAPTER 1

INTRODUCTION

1.1 Motivation and Challenges

The Internet of Things (IoT) enables intelligent monitoring and management in many applications. This includes industrial and biomedical systems as well as environmental and infrastructure monitoring [1]–[5]. The value of IoT perceived by the end users comes from services it can deliver, which are primarily based on software for data collection and the integration of cloud services and applications [6]. However, to enable these applications, IoT requires a vast infrastructure that must be implemented reliably on both the software and hardware levels [7]. This includes system-level software and network/server infrastructure as well as wireless sensor network (WSN) nodes, equipped with integrated sensors, actuators, a microcontroller, and transceiver [6], [8], [9].

Figure 1.1 shows a simplified, three-layer model of IoT architecture [10]. The physical objects layer consists of WSN nodes. The network layer is in charge of transferring the data using various communication standards and protocols. Finally, the

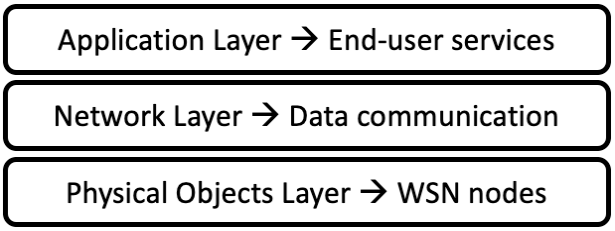

Figure 1.1 IoT three-layer architecture [10]

application layer provides various services to the end user.

In the physical objects layer, there are many challenges rising from the requirements for WSN nodes to be small-sized and off-grid. For example, the implantable intraocular device in [2] measures 5mm x 5mm x 1.5mm. The required small form-factor results in limited-capacity batteries that need periodic replacement. This is becoming increasingly challenging and costly as IoT scales up to the predicted 24.9 billion connections by 2025 [11]. Additionally, in many applications, such as manufacturing and agriculture, WSNs are deployed within a local network setting where nodes send data to a server not necessarily connected to the internet [12]. Whether WSN nodes are within the context of IoT or not, maintenance remains challenging. Thus, increasing lifetime and ultimately achieving energy autonomy in WSNs is of utmost importance [13], [14].

To enable energy-autonomous operation, energy harvesting from ambient sources is necessary to recharge on-board energy storage such as batteries and supercapacitors. Energy can be harvested from DC sources such as solar, indoor light, and thermal. AC sources such as vibration and RF sources may also be used [15]–[19]. However, the harvested voltage is often below 0.6V, which is too low to charge batteries or power CMOS circuits and will require boosting to a higher voltage [15], [20].

Furthermore, there are two main challenges in harvesting energy for WSN nodes. First, the available energy is environment-dependent and can vary significantly with ambient conditions. For example, a 2.6mm x 3mm solar cell may produce 20nW-200μW depending on illuminance. Second, in many applications, nodes are deployed in harsh environments and energy must be harvested from ultra-low power levels. In industrial applications, for instance, WSNs rely on harvested energy in dark indoor environments,

which can be as low as 15µW [21], [22]. In biomedical applications, a 1mm^2 solar cell harvests less than 8.3µW [2]. In biological sensing and infrastructure monitoring applications, for instance, ambient power levels can be in the pW to nW range due to quiet, dark, and cold environments [23].

To tackle these stringent power constraints, a power management unit (PMU) that includes maximum power point tracking (MPPT), such as in Figure 1.2, is vital. A DC-DC up-converter boosts the harvested voltage and delivers power to the energy storage (ES), such as a battery or a supercapacitor [5]. The MPPT subsystem adjusts the converter in order to achieve the highest power conversion efficiency (PCE). Another DC-DC converter along with a voltage regulator provide the final regulated voltage to the IoT sensors and system-on-chip (SoC).

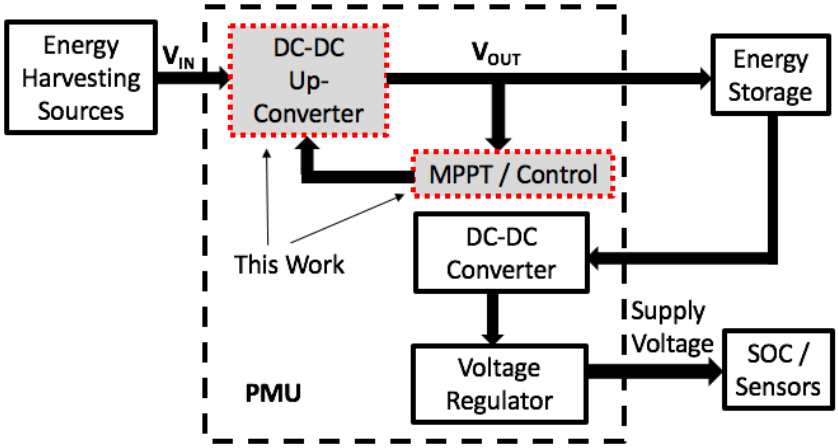

Figure 1.2 Power management unit block diagram

WSN nodes are size-constrained in many applications [2], [24]. Therefore, for WSN PMUs, fully-integrated, switched-capacitor (SC), or charge pump (CP) based up-converters are preferred over boost converters, because the latter requires a large off-chip

inductor [24]–[26]. Conventional, one dimensional, MPPT schemes for SC converters tune the switching frequency (f_{SW}) in order to achieve the best PCE, for example by implementing a hill-climbing algorithm such as in [8], [27]. However, due to limitations in SC converters, this approach results in high efficiency only for a limited range of input power (P_{IN}), referred to as the harvesting range [23], [28]. Consequently, it is challenging to achieve good power conversion efficiency across the large variation of available input power in energy-harvested IoT applications, particularly at ultra-low P_{IN} values.

1.2 Contributions

To overcome the limited harvesting range in conventional MPPT, a two-dimensional (2D) maximum efficiency tracking technique is presented in this work that enables a wider harvesting range. To achieve that, a charging technique for SC converters is proposed in order to discontinuously deliver current to energy storage, only during clock non-overlap time (t_{NOL}) [29]. This introduces a control variable that adjusts the average output power in order to improve power conversion efficiency at low input power. The proposed scheme is capable of periodically sensing the available input power in a given environment and dynamically optimizing power conversion efficiency based on that information. This enables high-efficiency operation at considerably lower input power and allows the system to achieve a wide harvesting range. This is especially valuable in IoT applications that deploy WSN nodes in harsh environments, where ambient power levels vary considerably and can be very low. The system also tunes f_{SW} to deliver the maximum output power.

1.3 Dissertation Outline

This dissertation is organized as follows: Chapter 2 discusses relevant IoT applications and a system-level overview of WSN nodes and their power requirements. In Chapter 3 the fundamentals of SC converter operation are examined, including their output impedance and power losses. Chapter 4 presents a review of key innovative techniques in recent energy harvesting and MPPT literature.

Chapter 5 details the theoretical basis of the proposed discontinuous charging and explains how it enables higher efficiency at lower input power levels. Chapter 6 presents Matlab and circuit models that capture the operation and power losses of discontinuous charging. Chapter 7 discusses the proposed 2D maximum efficiency tracking technique including its circuit implementation and how it dynamically optimizes power conversion efficiency to input power levels. Chapter 8 presents the simulation results including functional and transient simulations as well as efficiency characterization and system performance over process, voltage, and temperature (PVT) variations. Additionally, it discusses the system's physical layout, area, and post-layout RC-extracted simulation results. In Chapter 9, the proposed technique is applied to an indoor WSN implementation for industrial and wearable applications, to show how it enables energy autonomy in a scenario where that would not be possible otherwise. In Chapter 10, the performance of the proposed technique is summarized and compared to recent literature. Finally, Chapter 11 concludes this work and discusses future work.

Appendix A shows the transistor-level circuit schematics and full system testbench using Synopsys Custom Compiler and Appendix B includes the Matlab model code.

CHAPTER 2

WSN APPLICATIONS AND POWER REQUIREMENTS

In this chapter, examples of IoT applications that can benefit from low-power energy harvesting for WSNs are discussed. Additionally, WSN system-level overview and power consumption are discussed to provide context for the required power levels in energy harvested IoT applications.

2.1 Low Power IoT Applications

IoT spans various industries, including agriculture, automotive, and consumer electronics. Additional applications include smart grids, cities, and buildings. In many cases, sufficient energy is available to harvest. However, in applications such as healthcare, infrastructure monitoring, industrial applications as well as animal and environmental monitoring, WSN nodes can face harsh environments with ultra-low power levels available to harvest from. Such applications can benefit the most from the technique presented in this dissertation and are thus discussed below to provide background for this work.

Infrastructure monitoring involves sensing the structural health of critical civil, military, and aerospace structures in order to detect damage in early stages. Examples of such structures include bridges, buildings, aerial vehicles as well as tanks and oil rigs [30]. Additionally, the health of transmission lines and substations can be monitored [1], [31]. Some structures, such as military planes, require daily monitoring, whereas other structures,

such as bridges, can be monitored less frequently [30]. Due to the placements of WSN nodes in infrastructure monitoring, nodes may be hidden in inaccessible locations and must operate reliably for decades [5]. It is often dark, and can be quiet and cold which results in very low ambient power levels available for harvesting [23].

In environmental and animal monitoring applications, WSN nodes can be used to monitor the quality of natural resources, such as water pollution levels. WSN nodes can also play a key role in the early detection and prevention of forest fires [32]. Biological sensing can be used for animal health management. For instance, a timely diagnosis of diseases in dairy cattle and poultry farms can be provided by monitoring glucose levels, proteins, or enzymes in the bloodstream. Additionally, sensors and wearables can be implanted on animals to test for harmful compounds such as antibiotic residues. It is also possible to measure body temperature and detect the presence of viruses and pathogens [33]. For wildlife animals, such as zebras and turtles, the activity and living conditions can be monitored by tracking their motion and location in order to study their habitats, migration patterns, and group sizes [34]. Placing sensor nodes on moving animals can limit ambient powers to ultra-low power levels. For example, animals can stay in the shade for a long period of time. Additionally, some animals such as turtles can move into the water [34]. Hence, nano-generators and biofuel cells can harvest power in the pW-nW range in some conditions [23].

In healthcare, implantable medical devices and IoT wearables can be used to constantly monitor vital signs such as pulse, blood pressure, and ECG signals of persons at risk such as the elderly [35]–[37]. They can also be used to detect falls in elderly patients and help patients manage chronic conditions and recover from injuries or

surgeries [6], [38]. For example, artificial pancreases, which are implanted glucose monitors wirelessly connected to insulin pumps, can ease the life of many type-1 diabetic patients. Post-surgery sensors can be used to detect changes in pH or white blood cell concentrations to prevent infections. Moreover, future pace-makers will consist of sensing and pacing devices implanted in the heart and wirelessly connected to each other to enable advanced cardiac resynchronization therapy [39]. In the context of these biomedical applications, small footprint is important and harvested power levels can be very low. For example in [2], a $1mm^2$ solar cell harvests 3.7nW to 8.3μW when illuminance is between 100lx and 100klx.

In industrial applications, WSNs enable automation by increased sensing to allow optimal control of the process and to improve product quality while reducing energy consumption. WSNs can also be used for airflow management in industrial facilities by monitoring microclimates in order to facilitate control, reduce hotspots and energy waste and consequently reduce operation costs. In industrial applications, WSNs are often placed in dark indoor environments where harvested power levels are below 15μW [21], [22].

In the applications discussed above, the harsh conditions and ultra-low ambient power level pose challenges on harvesting energy with high PCE. Thus, many works in recent literature focus on improving PCE for input power levels that are as low as possible, as will be discussed in Chapter 4.

2.2 WSN System-Level Overview and Power Consumption

IoT is an evolving field with a vast number of applications that utilize different standards and protocols. Hence, power specifications for energy harvesting and WSN power management circuits vary. To understand the power levels consumed by WSN nodes,

Figure 2.1 shows a generic WSN node block diagram [10], [40]. Sensors periodically provide data to a microcontroller (μC) to be processed, then communicated via a transceiver. The PMU receives harvested energy from the source and delivers it to energy storage as well as other blocks in the system.

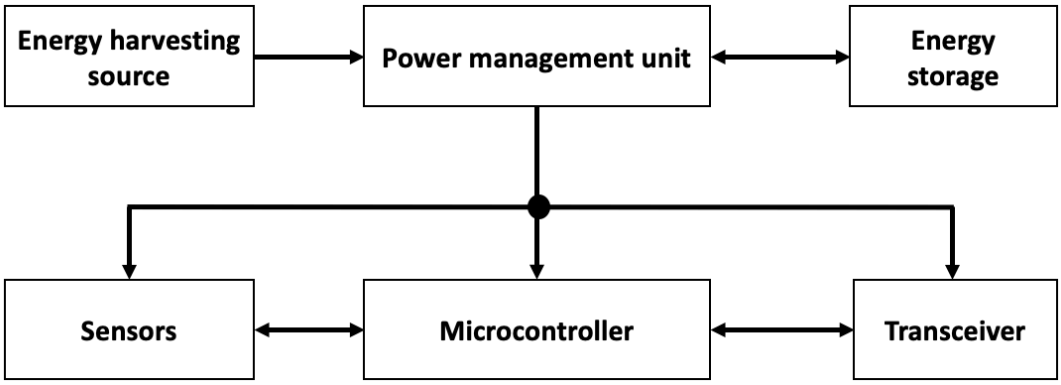

Figure 2.1 Generic WSN node block diagram

When in operation, WSN nodes require tens to hundreds of mA [10], [41]. For example, the implantable ultrasonic medical IoT system in [39], consumes 10-26mA. In [42], a WSN node for environmental sensing in agricultural fields consumes 16-24mA. The traffic monitoring WSN node in [41] consumes 88-231mA.

The power consumption is primarily dominated by the transceiver, followed by the microcontroller. For example, the microcontroller and transceiver shown in [10] burn 756μA and 148mA, respectively. In [43], the receiver consumes 35.28mA. If operated continuously, even ultra-low power designs such as the Arm Cortex-M3 microcontroller and the transceiver utilized in [40], [44], would burn 400μA and 3.7mA, respectively [45], [46].

Despite these power levels, WSNs are deployed in harsh environments where available power for harvesting is very low. For example, many works in recent energy harvesting literature focus on achieving higher power conversion efficiency at input powers lower than 50μW, as will be discussed in Chapter 4 [8], [47], [48]. Hence, when WSN nodes are active, they consume power that is orders of magnitude higher than what is provided by energy harvesting. This presents a challenge to achieving energy autonomy in WSN nodes [10].

To achieve energy-autonomous WSN nodes that can operate in environments with low ambient power, power cycling or duty cycling the system is key [49]. In power cycling, a system is active only for a fraction of the time and remains off or in sleep mode otherwise [50]. As the system consumes very little energy during sleep, this allows WSN nodes to save power [51]. Typically, WSN nodes remain in sleep mode for more than 99% of the time, allowing the average power to approach the low values consumed during sleep [22]. In [52] for example, the power consumption of main activities for an industrial WSN node is reported, as shown in Table 2.1. The power consumption during radio transmission is 29.52mW. However, the system remains in standby for 99.9% of the time and only turns on for 65ms/minute. Hence, the average power consumption is 36μW.

Table 2.1 Power consumption by activity for industrial WSN in [52] (modified)

Activity	**Activity Duration (ms)**	**Power Consumption (mW)**
Standby	-	0.008
Radio receive	50	18.76
Radio transmit	5	29.52
Sensor polling	10	10.27

One protocol used for long-range communications in IoT is the LoRaWAN communications protocol. LoRaWAN is based on low-power wide-area (LPWA) technology capable of communicating over tens of kilometers [53]. For example, a LoRaWAN-based infrastructure health monitoring WSN is presented in [5]. The transmitter used in this system consumes 119mW when active and the system requires 214mJ of energy for a complete cycle to sense, process, and transmit data. However, each cycle takes 2.13s and for low power, the system can be activated every 4 hours. For the remaining time, the system is completely powered off and leakage power during that time is not reported. Hence, the average power consumption can be calculated to be approximately 15μW.

For short and mid-range IoT communication, Bluetooth Low Energy (BLE) is a popular standard [54], [55]. As defined in the physical layer of the BLE standard, a frequency band and bit rate of 2.4GHz and 1MHz are used, respectively. The transmitter power is specified as -20dBm to +10dBm [56]. Due to the low-power requirements for the transmitter, which commonly dominates power consumption in WSN nodes, BLE is suitable for ultra-low power applications such as environmental monitoring and biomedical WSN nodes [37], [57]. For example, in [58], a BLE transmitter for environmental monitoring applications consumes 3.97mA when active and 5.2nW during sleep. In [38], a BLE transmitter is designed for wearable temperature sensing and free-fall detection applications. The transmitter consumes 724μW when active and is enabled once per minute Hence the average power consumption is 20.6μW.

Another technology for short ranges is Near-field Communication (NFC), which allows wireless communication between devices using the 13.56MHz frequency band [59].

Compared to other wireless communication standards, NFC offers a few advantages. First, NFC provides a quick and easy way to obtain data from sensors by simply approaching the reader to the tag, without the need to pair the devices. NFC is also cheaper because it has the capability of storing data without the use of microcontrollers or external memories. This results in lower cost, complexity and power consumption [60]. Moreover, NFC can enable battery-less operation by harvesting energy from magnetic field induction between the reader and tag antenna during communication [61]. NFC is commonly used in agriculture and livestock applications as well as biomedical devices [59]–[62]. For example, the NFC system in [59] is designed for wearable and implantable devices and consumes 10-19.8mW when active. In [63] , a battery-less NFC system for chronic wound monitoring consumes 3.9mA when active.

Many WSNs define their communication protocol using the IEEE 802.15.4 standard for low data-rate, low-power, and low-complexity short-range radio frequency transmissions. One example is the GreenNet protocol [21], [22]. For instance, a GreenNet-based WSN implementation is described in [22] for industrial and wearable applications in dark indoor environments. GreenNet utilizes the IEEE 802.15.4 energy-saving beacon mode, where nodes are synchronized with periodic beacons and can only wake up at specific instances to communicate [21]. The beacon mode settings are defined using the beacon order parameter (BO), which configures the interval between beacon transmissions (BI). The node remains in sleep mode between beacon intervals. In [22], the power consumption of each activity is detailed, as shown in Table 2.2. A full cycle requires 569.69μJ. During sleep, the node consumes 3.58μA.

Table 2.2 Power consumption during beacon reception/data transmission in one cycle of the GreenNet node with beacon-enabled mode [22] © 2020 IEEE

Activity	Activity Duration (ms)	Current Consumption (mA)	Energy (µJ)
µC Initialization	3.5	1.42	14.91
Sensor Data Acquisition	4.2	5.34	67.28
Preparation to Sleep	1.2	5.7	20.51
Inactivity	17	0.36	18.16
µC initialization	3.2	1.44	13.82
Preparation for beacon receiving	3	5.22	46.94
Radio set-up	0.7	6.23	13.08
Radio receive, sensing for a beacon	2.9	8.54	74.33
Radio receive, beacon header	1.5	7.12	32.04
Radio receive, beacon payload	1.8	8.46	45.66
Preparation to transmit	1.4	6.76	28.41
Transmit data package	4	11.56	138.72
Radio receive, waiting for acknowledge	1.4	8	33.6
Radio off, preparation to sleep	1.3	5.7	22.21
Total	47.1	-	569.69

The BO and corresponding BI values are shown in Table 2.3, along with the average current required for each BO, where the higher the BO/BI value, the lower the power required by this GreenNet-based WSN [22]. Depending on how often the system is activated, average power consumption can be as high as 12.36mW and as low as 4.33µW. Since GreenNet is designed for WSN nodes operating in dark indoor environments and capable of achieving ultra-low power levels, this system will be further discussed in Chapter 9 and will be used to demonstrate how the proposed technique enables energy-

autonomous operation. This work can be similarly utilized with other low-power communication standards/protocols.

In conclusion, while WSN nodes consume tens to hundreds of mA when active, they remain in sleep mode for more than 99% of the time. This allows their average power consumption to be in the order of tens of μW or less. Hence, harvesting energy efficiently at these power levels is vital to replenish energy storage and achieve energy-autonomous WSN nodes.

Table 2.3 Current consumption for different BO parameter values of IEEE 802.15.4-compatible GreenNet WSN node [22] © 2020 IEEE

BO	**BI (s)**	**Average Current (μA)**
0	0.02	12363.06
1	0.03	6181.53
2	0.06	3091.6
3	0.12	1547.59
4	0.25	775.59
5	0.49	389.58
6	0.98	196.58
7	1.97	100.08
8	3.93	51.83
9	7.86	27.71
10	15.73	15.64
11	31.46	9.61
12	62.91	6.6
13	125.83	5.09
14	251.66	4.33

CHAPTER 3

SWITCHED-CAPACITOR CONVERTER FUNDAMENTALS

In order to understand the proposed technique and how it enables energy-autonomous operation in WSNs, switched-capacitor converters must first be analyzed. In this chapter, the fundamentals of switched-capacitor converter operation are presented, including a detailed analysis of their output impedance, power losses, and power conversion efficiency.

3.1 Ideal Voltage Doubler Operation

Figure 3.1 (a) shows an SC voltage doubler model that will be referenced in the analysis in this chapter [64]. During one clock period (T), the circuit operates in two phases as shown in Figure 3.1 (b), where D and t_{NOL} are the clock duty cycle and the non-overlap time, respectively. During phase 1 (ϕ_1), shown in Figure 3.2 (a), the flying capacitor (C_{FLY}), is connected in parallel to the input source. This charges C_{FLY} to a voltage V_{IN}. During

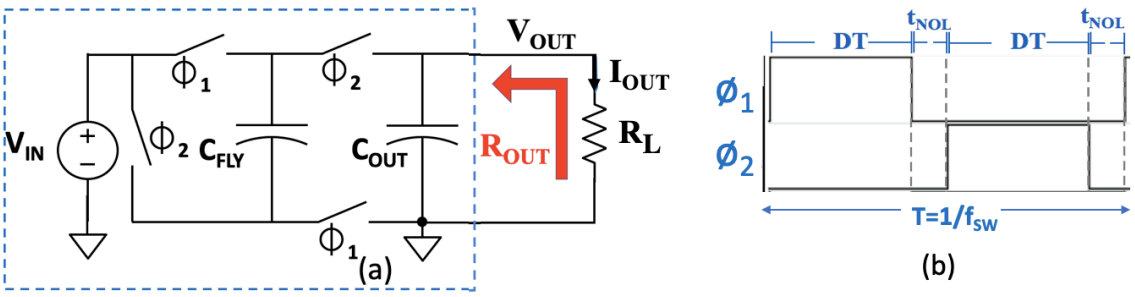

Figure 3.1 (a) Ideal SC voltage doubler. (b) Non-overlapping clock waveforms.

phase 2 (ϕ_2), shown in Figure 3.2 (b), V_{IN} is connected to the bottom plate of C_{FLY} which charges the bottom plate to V_{IN}. This effectively pumps the top plate to twice V_{IN}. Thus, the output capacitor (C_{OUT}) and output voltage (V_{OUT}) are ideally charged to twice V_{IN}. ϕ_1 and ϕ_2 must be non-overlapping to avoid lossy discharge of capacitors [64]. During all phases of operation, C_{OUT} remains connected to the load circuitry or energy storage and supplies current continuously. The following subsections discuss the output impedance and the power losses associated with this circuit.

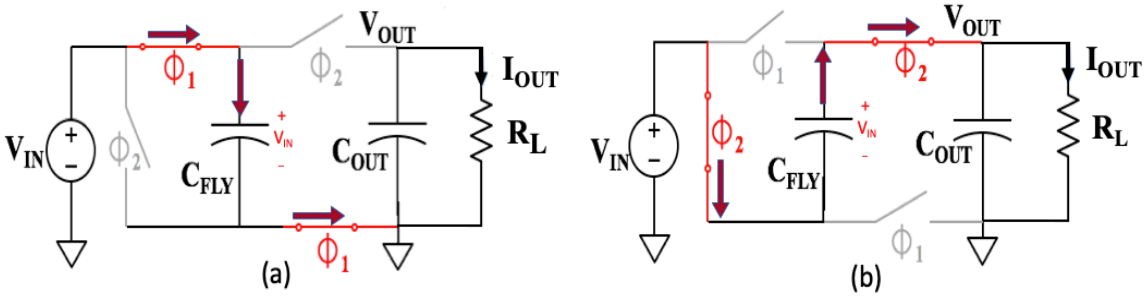

Figure 3.2 (a) Operation during Phase 1 (b) Operation during Phase 2.

3.2 Switched-Capacitor Converter Impedance Analysis

When no load is present, the converter in Figure 3.1 (a) provides an ideal DC voltage of $2V_{IN}$. However, under load conditions the voltage drop due to the converter's equivalent output impedance (R_{OUT}) reduces V_{OUT}. R_{OUT} models two components. The first is the effective resistance due to capacitor charge redistribution (R_{CHARGE}), which occurs due to the capacitor periodically charging and discharging to supply the output current [65]–[67]. It is inversely proportional to the converter's switching frequency as shown in (3.1) and is dominant at slower switching frequencies [64], [68]. In this analysis, C_{OUT} is

assumed to be much larger than C_{FLY} in order to minimize ripples in V_{OUT} and is not included in (3.1) [29], [67], [69].

$$R_{CHARGE} = \frac{1}{f_{SW} C_{FLY}} \tag{3.1}$$

Equation (3.1) can be understood by analyzing the simple switched-capacitor circuit in Figure 3.3, where V_1 and V_2 are DC voltage sources, and C_{FLY} is the flying capacitor [70]. During ϕ_1, the capacitor is charged to voltage V_1. During ϕ_2, the capacitor is charged to voltage V_2. The change in capacitor charge over one clock period (T), is a function of the capacitor value and the voltage difference as shown in (3.2). Hence, the equivalent average current (I_{avg}) delivered between V_1 and V_2 due to this charge transfer can be found as shown in (3.3). Since the average current is also a function of the voltage difference and resistance according to Ohm's law as shown in (3.4), R_{CHARGE} in (3.1) can be found by equating (3.3) and (3.4) and rearranging the resulting equation [70].

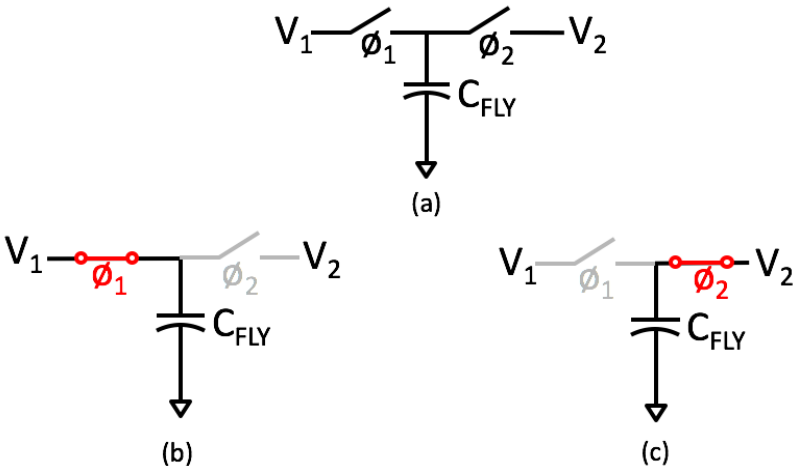

Figure 3.3 Switched-Capacitor circuit. (b) Operation during phase 1.(c) Operation during phase 2

$$\Delta Q = C_{FLY}\Delta V = C_{FLY}(V_1 - V_2) \tag{3.2}$$

$$I_{avg} = \frac{\Delta Q}{\Delta t} = \frac{C_{FLY}(V_1 - V_2)}{T} \tag{3.3}$$

$$I_{avg} = \frac{\Delta V}{R_{CHARGE}} = \frac{(V_1 - V_2)}{R_{CHARGE}} \tag{3.4}$$

The second component is the conduction loss of MOSFET switches (R_{COND}). Since each MOSFET switch is on for only part of the period, i.e. its duty cycle, R_{COND} is a function of D and switch resistance (R_{SW}). To demonstrate the dependence of R_{COND} on D, Figure 3.4 shows the current waveform through one of the switches (I_{SW}). The average current through this switch ($I_{SW\text{-}avg}$) is shown in (3.5). Hence, the average conduction loss of one switch (R_{CONDi}) is given by (3.6). The total conduction loss is therefore a summation of the average conduction loss of each switch as shown in (3.7) and is dominant at higher f_{SW} when R_{CHARGE} becomes negligible [68].

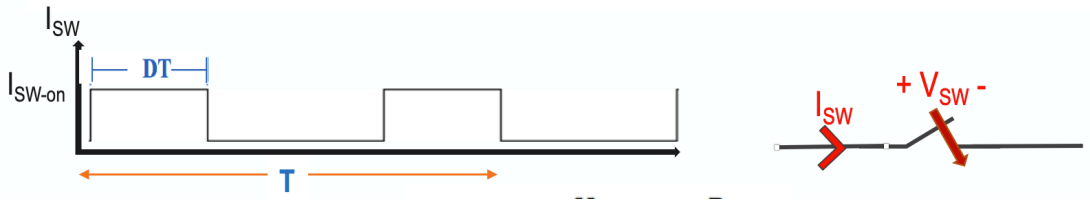

Figure 3.4 MOSFET switch current waveform

$$I_{SW-avg} = DI_{SW-on} \tag{3.5}$$

$$R_{COND_i} = \frac{V_{SW}}{DI_{SW-on}} = \frac{R_{SWi}}{D} \tag{3.6}$$

$$R_{COND} = \sum_i \frac{R_{SWi}}{D} \tag{3.7}$$

A Euclidean norm approximation is used to find the total R_{OUT} as shown in (3.8) [69]. Hence, the output voltage is given by (3.9), where $I_{OUT\text{-}avg}$ is the average output current, R_L is the load resistance and *n* is the voltage conversion ratio and is equal to 2 for a voltage doubler.

$$R_{OUT} = \sqrt{{R_{CHARGE}}^2 + {R_{COND}}^2} \tag{3.8}$$

$$\begin{aligned} V_{OUT} = nV_{IN} - I_{OUT-avg}R_{OUT} &= nV_{IN} - \frac{V_{OUT}}{R_L}R_{OUT} \\ &= \frac{nV_{IN}}{1 + \frac{R_{OUT}}{R_L}} \end{aligned} \tag{3.9}$$

3.3 Power Losses and Efficiency Analysis

Three power losses are defined for a switched-capacitor converter [47]. The first occurs due to the output current passing through R_{OUT} (P_{ROUT}), as defined in (3.10). P_{ROUT} is the dominant loss at lower f_{SW} due to R_{OUT}'s inverse relationship with f_{SW}.

$$P_{ROUT} = [I_{OUT-avg}]^2 R_{OUT} \tag{3.10}$$

Furthermore, there are two parasitic losses (P_{PAR}). The first is the parasitic switching loss (P_{SW}), which occurs due to driving the total gate capacitances of the MOSFET switches (C_{GGtot}) [69]. This loss is always a source of dynamic power consumption in any switching CMOS circuit including digital CMOS circuits [71]. Figure 3.5 presents an equivalent circuit that will be used to derive P_{SW}, where C_{GGtot} represents the total MOSFET gate capacitances. The gate capacitance is assumed constant in this analysis because when

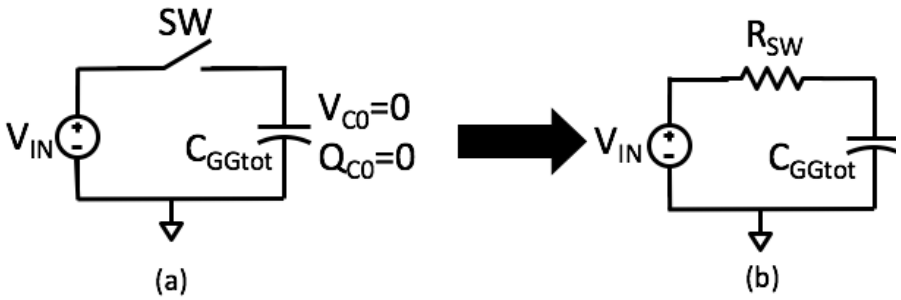

Figure 3.5 Parasitic switching loss equivalent circuit: (a) Initial conditions (b) Capacitor charging

switches are on in the voltage doubler of Figure 3.1, they are held in a rather constant operating point for a given input voltage. Initially, the capacitor C_{GGtot} has no voltage or charge on it. When the switch closes, the capacitor is charged and the energy stored is shown in (3.11). However, the energy that the voltage source provided is given by (3.12). Thus, while charging C_{GGtot}, the energy lost is shown in (3.13). When discharging the capacitor, the energy stored in C_{GGtot}, shown in (3.11), will be discharged to ground and therefore also lost. Hence, during one clock period, the parasitic switching loss is proportional to switching frequency and is given by (3.14) [64], [72].

$$E_{C_{GG}-stored} = \frac{1}{2} C_{GGtot} {V_{IN}}^2 \tag{3.11}$$

$$E_{IN} = \int_0^T V_{IN} I = V_{IN} \int_0^T I = C_{GGtot} Q = C_{GGtot} {V_{IN}}^2 \tag{3.12}$$

$$E_{Charging=} E_{IN-} E_{C_{GG}-stored} = \frac{1}{2} C_{GGtot} {V_{IN}}^2 \tag{3.13}$$

$$P_{SW} = \frac{E_{total}}{T} = \frac{E_{C_{GG}-stored} + \mathrm{E_{Charging}}}{T} = f_{SW} C_{GGtot} {V_{IN}}^2 \tag{3.14}$$

The second loss is the parasitic bottom plate (P_{BOT}), which occurs due to driving the bottom plate capacitance (C_{BOT}) between the bottom plate of on-chip metal capacitors and the substrate [26], [64]. C_{BOT} value is a percentage (x) of C_{FLY} and can be as large as 10% of C_{FLY} [64], [73]. P_{BOT} is derived in a similar fashion to P_{SW} and the total parasitic loss is shown in (3.15). It can be seen that at higher f_{SW}, P_{PAR} is higher due to its direct proportionality to f_{SW}. Figure 3.6 is a plot of the defined losses, where P_{LOSS} is the total loss due to P_{ROUT} and P_{PAR}. It can be seen that P_{ROUT} is dominant at lower f_{SW}. At higher f_{SW}, P_{PAR} is dominant. Using these losses, PCE is calculated according to (3.16), where P_{OUT} is the output power.

$$P_{PAR} = P_{SW} + P_{BOT} = f_{SW}{V_{IN}}^2(C_{GGtot} + xC_{FLY}) \tag{3.15}$$

$$PCE = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + (P_{ROUT} + P_{PAR})} = \frac{P_{IN} - (P_{ROUT} + P_{PAR})}{P_{IN}} \tag{3.16}$$

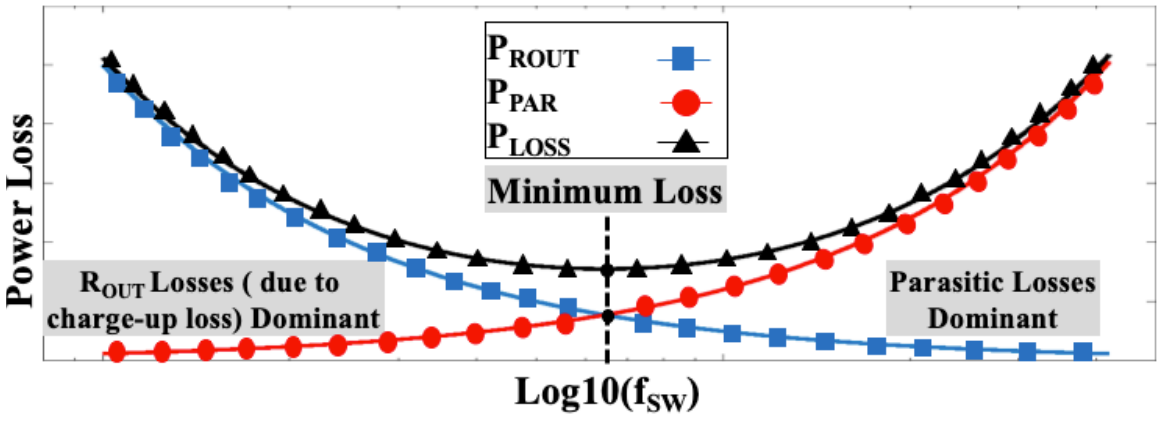

Figure 3.6 SC converter power losses

In order to facilitate the study of the proposed technique in Chapter 5, it is desired to find an expression for PCE as a function of the switching frequency. This can done be

by first multiplying V_{OUT} in (3.9) by $I_{OUT\text{-}avg}$ to find the output power as shown in (3.17). Following that, the power losses in (3.10) and (3.15) as well as P_{OUT} in (3.17) are substituted into the PCE equation in (3.16). The resulting PCE is shown in (3.18). Note that since R_{CHARGE} from (3.8) is one to two orders of magnitude larger than R_{COND} at the intended frequency range of operation in this design, R_{OUT} is approximated as equal to R_{CHARGE} to simplify the expression in (3.18). Moreover, all constants in (3.18) have been lumped into constants A_1 to A_4, as defined in Table 3.1, in order to clearly show that PCE is a function of f_{SW}.

$$P_{OUT} = V_{OUT} I_{OUT-avg} = \frac{(nV_{IN})^2}{R_L(1 + \frac{R_{OUT}}{R_L})^2} \tag{3.17}$$

$$PCE \approx \frac{A_1 f_{SW}}{A_2 {f_{SW}}^2 + A_3 f_{SW} + A_4} \tag{3.18}$$

Table 3.1 Constant values for power conversion efficiency in (3.18)

$A_1=n^2R_LC_{FLY}^2$	$A_3=[(n^2+2x)\ C_{FLY}^2+2C_{GGtot}C_{FLY}]R_L$
$A_2=R_L^2C_{FLY}^2C_{GGtot}+xR_L^2C_{FLY}^3$	$A_4=(n^2+x)\ C_{FLY} + C_{GGtot}$

Finally, the voltage conversion efficiency (VCE), shown in (3.19), measures how close the output voltage approaches the ideal value for the voltage doubler. The VCE measure is important because if the voltage doubler does not reasonably approach twice the input voltage, the circuit will not be useful in the desired applications, even if good PCE is achieved.

$$VCE = \frac{V_{OUT}}{nV_{IN}} \tag{3.19}$$

3.4 Challenges of WSN Energy Harvesting

Figure 3.7 shows a conceptual illustration of the PCE vs. P_{IN} for SC converters. At high P_{IN}, the converter requires increasing f_{SW} to match the available P_{IN} levels and deliver more power to the output [23], [74]. However, parasitic capacitances limit the PCE at these high P_{IN} levels. At lower P_{IN}, f_{SW} is decreased and PCE is limited by P_{ROUT}, leakage, and the clock generation overhead needed to operate the switches [23]. The range of P_{IN} during which the converter achieves above 30-50% PCE is referred to as the harvesting range for the rest of this dissertation, with the lower end referred to as the harvesting floor as shown in Figure 3.7 [23], [28]. Consequently, it is challenging to achieve good PCE across the large variation of available input power in energy-harvested IoT applications, particularly at ultra-low P_{IN} values.

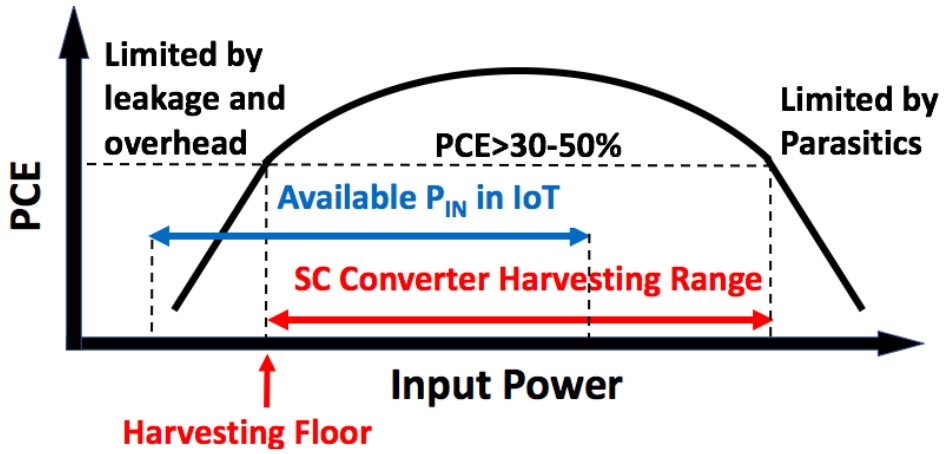

Figure 3.7 Switched-capacitor converter power conversion efficiency vs. P_{IN}

In summary, this chapter discussed the fundamental of switched-capacitor converters and the various power losses that limit efficient energy harvesting for WSNs The harvesting range limitations in SC converters cannot be overcome by optimizing the

sizing of circuit components [23]. Hence, several techniques have been presented in recent literature to extend the harvesting range of SC converters towards lower power levels, as discussed in the literature review in Chapter 4.

CHAPTER 4

REVIEW OF ENERGY HARVESTING AND MPPT TECHNIQUES IN IOT

In this chapter, a number of key papers related to this work in recent literature are briefly discussed. This chapter does not provide a comprehensive literature survey but rather highlights examples of various techniques in prior art that attempt to reduce power consumption and improve PCE and harvesting range. Additionally, examples of SC converters used in these low-power energy harvesting systems are shown. In this chapter, the author's analysis focuses on key innovative concepts in these papers. A performance comparison between previous works and the technique proposed in this dissertation are presented later in Chapter 10. Figures in this chapter are reused from their respective original publications.

4.1 Typical Switched-Capacitor Energy Harvesting

In [27], the energy harvesting system operates at higher power levels compares to state-of-the-art energy harvesters. However, it serves as an excellent resource for what a typical energy harvesting system incorporates.

Figure 4.1 shows the block diagram of this system. It consists of medium voltage and high voltage generators which are identical, except for boosting to different output voltages. The typical essential building blocks of an energy harvesting system can be seen in the medium voltage generator. First, an SC or CP-based up-converter is used to boost

the input voltage and store it on an output capacitor. The converter requires non-overlapping clocks to operate. Thus, a voltage-controlled-oscillator (VCO) and a four-phase clock generator are used. To minimize losses, an MPPT block adjusts the switching frequency of the VCO to achieve optimal output power. Additional blocks that may be needed include control, start-up, and voltage/current reference blocks.

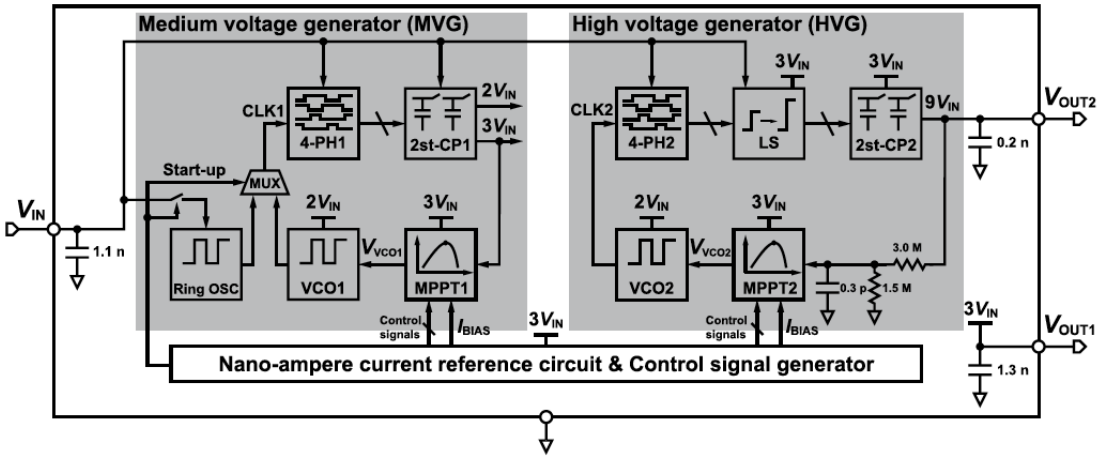

Figure 4.1 Block diagram of energy harvesting system in [27] © 2016 IEEE.

This system uses an MPPT scheme commonly used in energy harvesting systems, which is the hill-climbing algorithm shown in Figure 4.2. The system periodically samples the output voltage or power and the hill-climbing logic increases the VCO frequency as long as the new output value is larger than the previous. Once the new value drops below the previous, the system locks the switching frequency at this maximum power point. In this system, the VCO frequency is adjusted with the control voltage generator, which is a charge pump that charges/discharges the capacitor that holds the VCO control voltage. This system achieves 75.8% peak PCE at 396μW input power, which is much higher than the power levels recent low-power energy harvesting systems need to operate at.

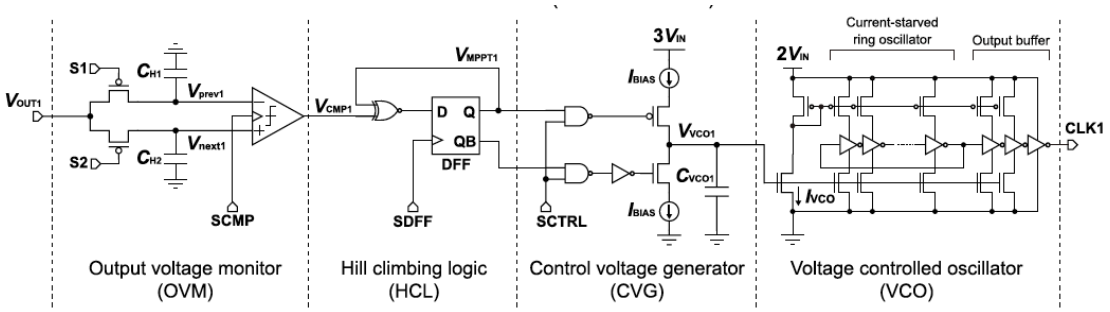

Figure 4.2 Schematic of MPPT and VCO circuits used in [27] © 2016 IEEE

In the following subsections, key previous works are discussed that deviate from the typical system in [27] with innovations in the MPPT scheme that reduce power consumption, improve the input power harvesting range and achieve high PCE at low input powers.

4.2 Examples of Power Loss Reduction Techniques

In [23], discontinuous harvesting technique is introduced where leakage is reduced to push the harvesting floor to lower P_{IN} levels. This work argues that when harvesting from a solar cell under very low power levels, the SC converter efficiency, dominated by leakage, is the main bottleneck of performance as opposed to the maximum power point operation of the system. Hence, the entire harvesting system is periodically shut down to minimize leakage.

A conceptual block diagram of this system is shown in Figure 4.3. An always-on mode controller is used to power gate the charge pump and its control circuitry. If available power is too low, the CP and its control are turned off to minimize leakage, and charge is accumulated on an external capacitor Cbuf. Once the voltage on Cbuf is high enough, the mode controller enables the CP and its control in order to transfer charge to the battery.

This trades off maximum power point operation for higher overall efficiency and an improved harvesting range.

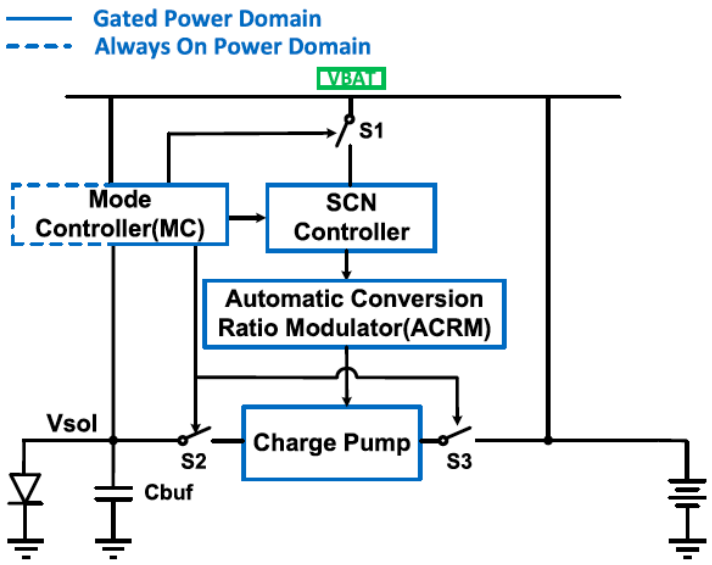

Figure 4.3 Block diagram of discontinuous harvester presented in [23] © 2017 IEEE

The concept of this technique is illustrated and compared to conventional operation in Figure 4.4. It can be seen that during the harvesting phase, leakage is low since most of the system is turned off. This lowers the harvesting floor due to lower losses, but the periodic start-up process results in larger energy losses every time the CP initializes the capacitors at the beginning of the transfer phase.

Additionally, this work also includes an SC converter with a variable conversion ratio to accommodate an input voltage range of 0.25-0.65V. The automatic conversion ratio modulator in Figure 4.3 senses the input voltage and adjusts the conversion ratio accordingly. The system achieves a peak efficiency of 50% at 8nW input power and can achieve over 40% PCE for an input power range of 113pW-1.5µW.

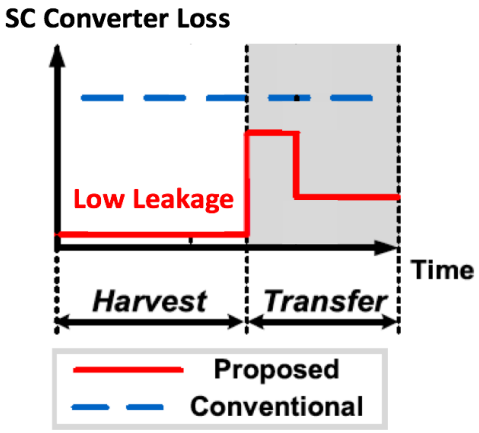

Figure 4.4 SC converter loss in [23] (Modified) © 2017 IEEE

In [47], MPPT techniques are not discussed. Instead, a charge recycling technique is introduced to reduce parasitic bottom plate power losses from (3.15), which improves PCE. Figure 4.5 shows the charge recycling concept proposed in this work. Figure 4.5 (a) shows the SC converter, where C_1 and C_2 are the flying capacitors and C_{BP1} and C_{BP2} are their respective parasitic bottom plate capacitors. For this analysis, capacitors C_{BP1} and C_{BP2} are assumed equal. Switch S_{qr} is added to connect the C_{BP1} and C_{BP2} to each other during non-overlap times as shown from the switch waveforms in Figure 4.5 (b). Figure 4.5 (c)-(e) show the operation during both phases, labeled period 1 and 3, as well as the non-overlap phases, labeled period 2 and 4. During the first period, C_{BP1} has no charge since both plates are grounded. C_{BP2} is charged to q_p, where q_p is equal to $VinC_{BP2}$. The charge waveforms for both capacitors are shown in Figure 4.5 (b). During the non-overlap period 2, C_{BP1} and C_{BP2} are connected in parallel. Due to the charge conservation law, each capacitor will carry half the charge, $q_b/2$. During the third period, both plates of C_{BP2} are grounded and its charge will be discharged. However, half of that charge has already been transferred to C_{BP1}. Hence, 50% of the charge is preserved and PCE is improved by 12.7%.

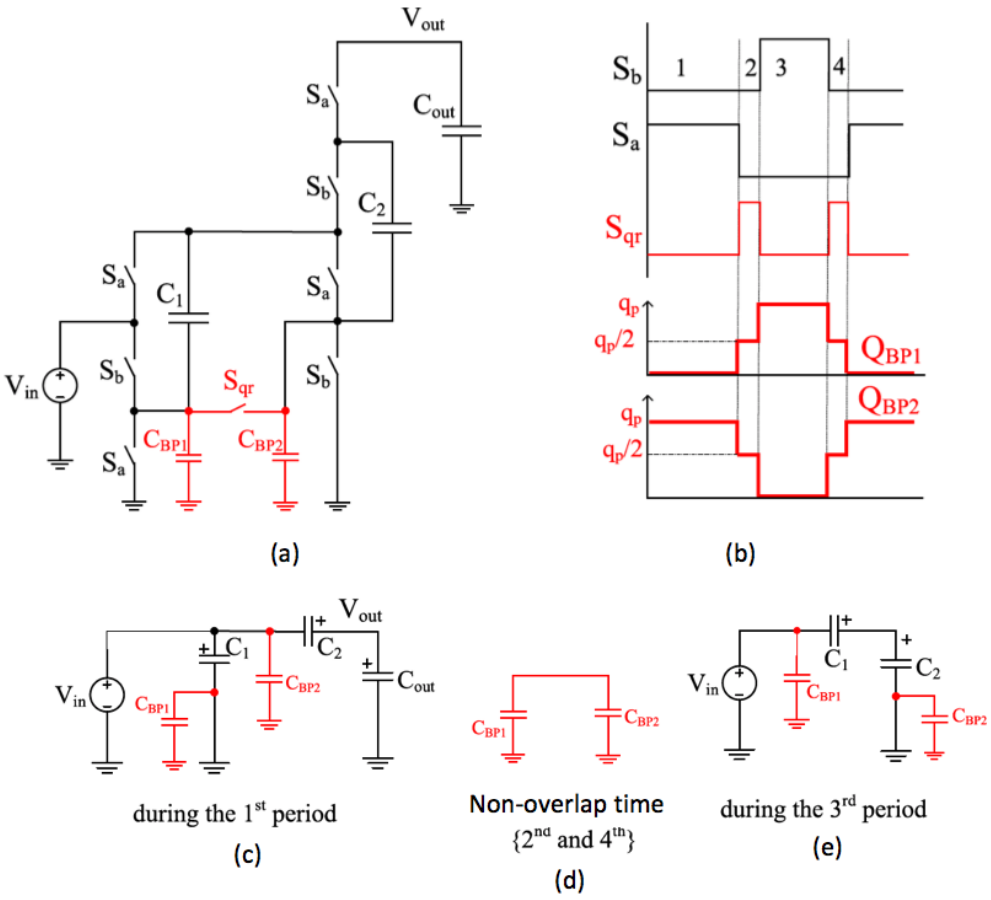

Figure 4.5 Charge recycling concept proposed in [47] (modified) © 2019 IEEE

4.3 Example of One-Dimensional MPPT Innovations

Most MPPT schemes for SC converters rely on tuning the switching frequency using a VCO to achieve the desired converter impedance and minimize losses by adjusting R_{CHARGE} in (3.1). However, R_{CHARGE} is also a function of the flying capacitors value. Hence, in [75], capacitor value modulation is proposed instead of the conventional frequency tuning. This is done to reduce MPPT power consumption because adjusting conventional VCOs requires analog blocks with quiescent current consumption such as the control voltage generator in Figure 4.2. However, capacitor value modulation can be implemented

digitally with a programmable capacitor bank and no additional static power consumption. A fixed-frequency ring oscillator is used since the frequency no longer needs to be adjusted.

The SC converter used in this work is shown in Figure 4.6 (a), where the operation in phase 1 and phase 2 are highlighted in Figure 4.6 (b). The structure consists of two nested voltage doublers to triple the input voltage. The first doubler consists of MOSFETS M_1 and M_2 and capacitors C_1 and C_2, along with their respective clock drivers. Similar to the ideal doubler in Figure 3.1, C_1 is charged to input voltage V_S in phase 1. During phase 2, its bottom plate connects to V_S pumping the top plate to $2V_S$. The same

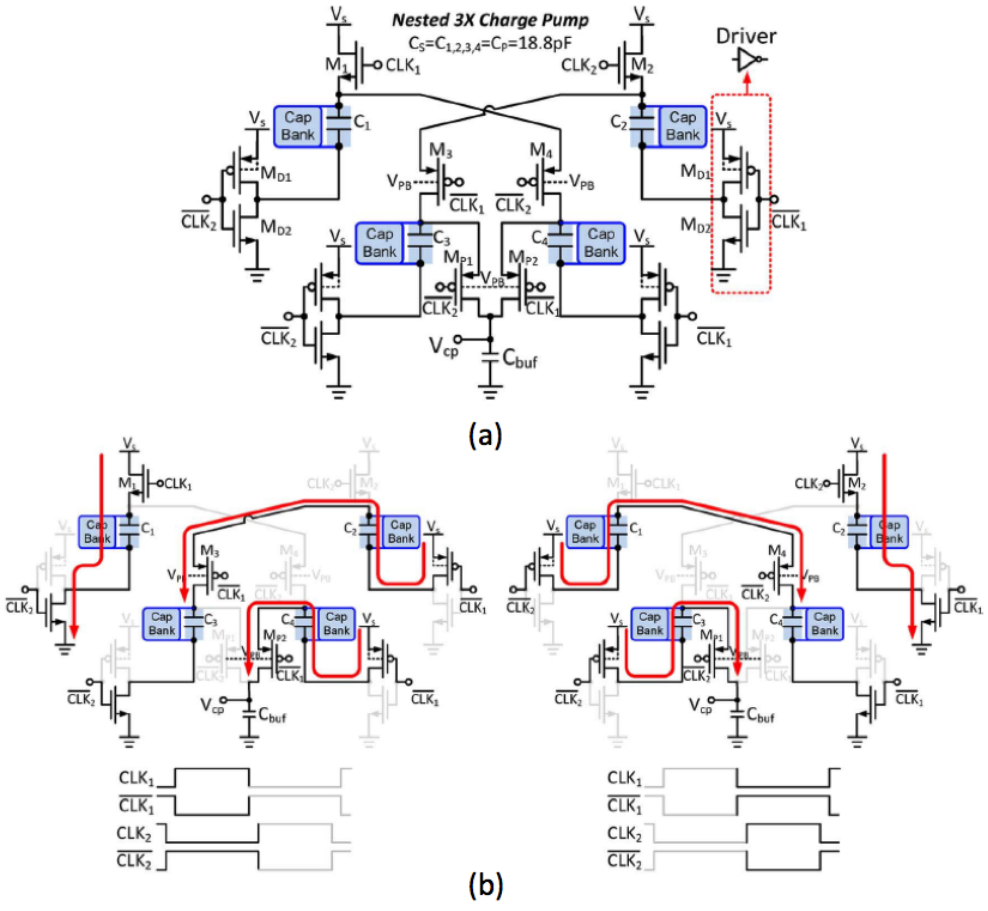

Figure 4.6 (a) Nested 3x charge pump used in [75] (b) its operation over both phases © 2015 IEEE

occurs to C_2 in the opposite phase. In the second voltage doubler, C_3 is charged to $2V_S$ during phase 1, allowing it to charge up to $3V_S$ during phase 2. The same occurs to C_4 during opposite phases. Each flying capacitor location in the circuit is connected to a programmable capacitor bank. The capacitor value modulation uses a hill-climbing algorithm to adjust the flying capacitor values by selecting capacitors from this programmable capacitor bank, shown in Figure 4.7. The hill-climbing locks when the highest output power is achieved.

This system achieves a peak PCE of 86.4% at 12µW of output power and achieves PCE above 40% for an input power range of 4.5-27µW.

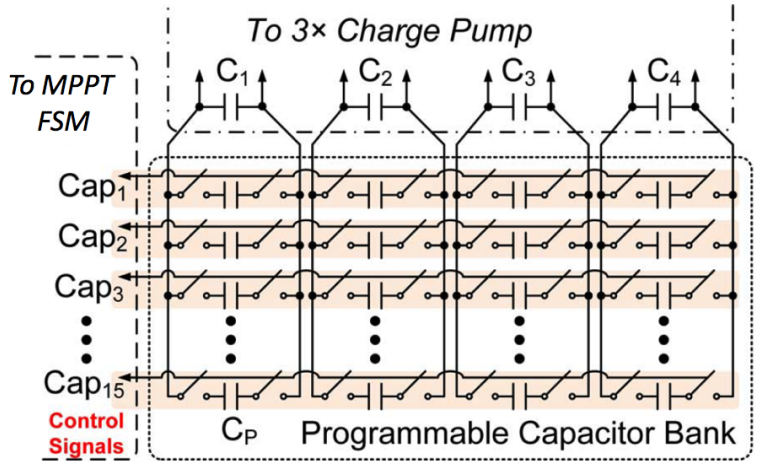

Figure 4.7 Programmable capacitor bank used in [75] © 2015 IEEE

4.4 Examples of Two-Dimensional MPPT Innovations

In [8], a 2D MPPT system is introduced that tunes the voltage conversion ratio of an SC converter in addition to the conventional switching frequency tuning. To enable that, a configurable CP architecture is used as shown in Figure 4.8 (a). Four stages of charge

pumps are used along with de-multiplexers to achieve various conversion ratios between 1.33x and 8x of the input voltage. Figure 4.8 (b) shows the circuit schematic of the 2x CP used in many stages, where two parallel charge pumps are used and operated in an interleaved fashion with local non-overlapping (LNO) clock and control signals. The operation is similar to the ideal model shown in Figure 3.1; capacitor C_1 is charged to a voltage V_S. After that, the bottom plate of C_1 is connected to V_S which pumps the top plate to twice V_S.

Following that, the 2D MPPT architecture in Figure 4.9 (a) is presented. A finite state machine (FSM) is used to first tune the conversion ratio based on the input voltage. After that, the switching frequency is tuned by controlling the VCO. The MPPT control circuit utilizes a hill-climbing algorithm as shown in Figure 4.9 (b). It consists of a sample and hold (S/H) circuit that compares the current value of V_{OUT} with a previous value every time the S_{MPPT} control signal enables. If the maximum power point is not achieved yet, the comparator output remains low. Once the maximum power point is achieved,

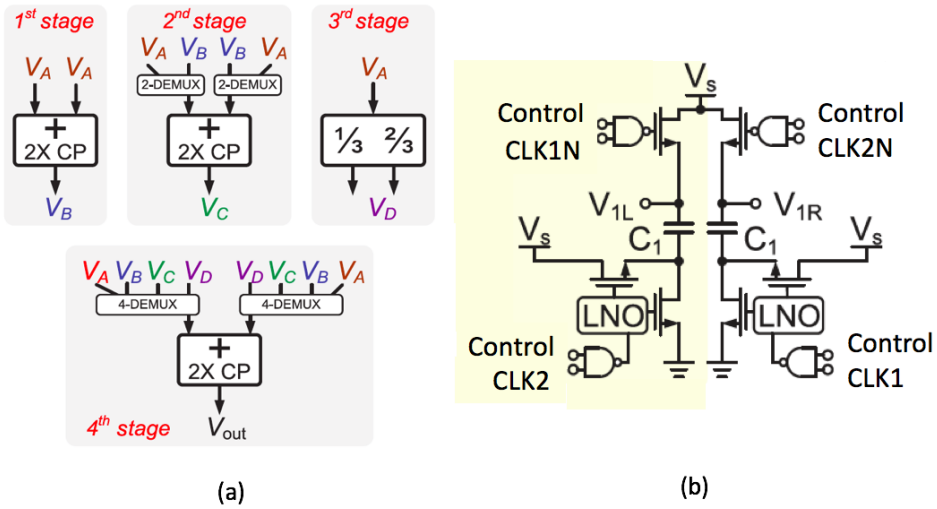

Figure 4.8 (a) Block diagram of configurable SC converter (b) Single stage voltage doubler used in [8] © 2016 IEEE

the comparator output, and consequently the output signal S_{ARB}, assert.

The conversion ratio and switching frequency control are achieved as shown in Figure 4.9 (c) and (d), respectively. In both cases, a 4-bit up/down counter is used where S_{MPPT} is used to clock the counter when S_{CR} or S_F control signals enable conversion ratio or f_{SW} tuning, respectively. The counters count up as long as S_{ARB} is low and the maximum power point is not achieved. Once S_{ARB} asserts, the counter counts one step down and locks at the maximum power point.

For f_{SW} tuning, the counter output, after a thermometer decoder, controls the oscillator. For conversion ratio tuning, the counter outputs are fed through combinational logic to generate the control signals S_{M1} through S_{M6}. This work enables good PCE operation at multiple input voltages. It achieves a peak PCE of 79% at P_{IN} above 35µW and can achieve over 40% PCE for an input power range of 2-50µW.

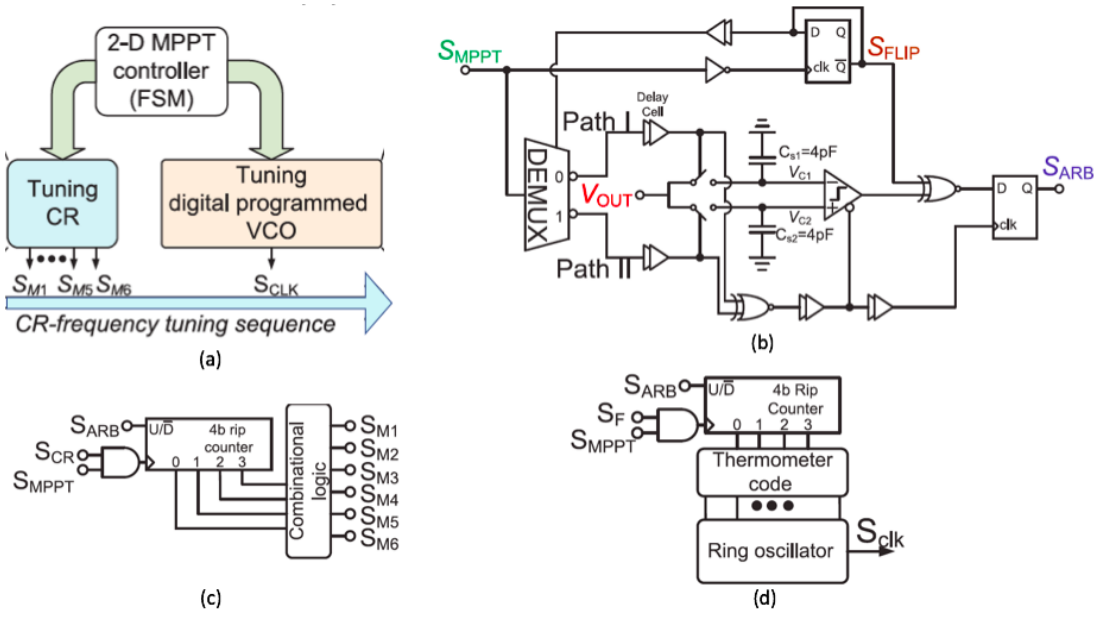

Figure 4.9 (a) 2D MPPT architecture in [8] (b) MPPT S/H and control (c) Conversion ratio control (d) Switching frequency control © 2016 IEEE

In [48], another 2D MPPT technique is presented. In addition to the standard switching frequency tuning, it adjusts the converter topology by adjusting the conversion ratio and flying capacitor values. However, this approach utilizes an open-loop look-up table. The MPPT architecture is shown in Figure 4.10. Four level detectors detect the voltage of the solar cell (V_{PD}) and adjust the oscillator frequency and the converter's conversion ratio and capacitance. This results in five working regions. The conversion ratio varies between 4x and 7x and the frequency varies between 100Hz and 150KHz. The different levels are selected during the design phase to cover the input voltage range of the solar cell and a look-up table approach is used to select the appropriate converter topology and oscillator frequency that would deliver the highest output current in every working region. The system is open-loop; it does not measure the output current and relies on the look-up table values assigned during the design and simulation phase. Nonetheless, this 2D approach enabled operation at ultra-low power levels, achieving an input power harvesting range of 0.5-10µW with PCE higher than 40%.

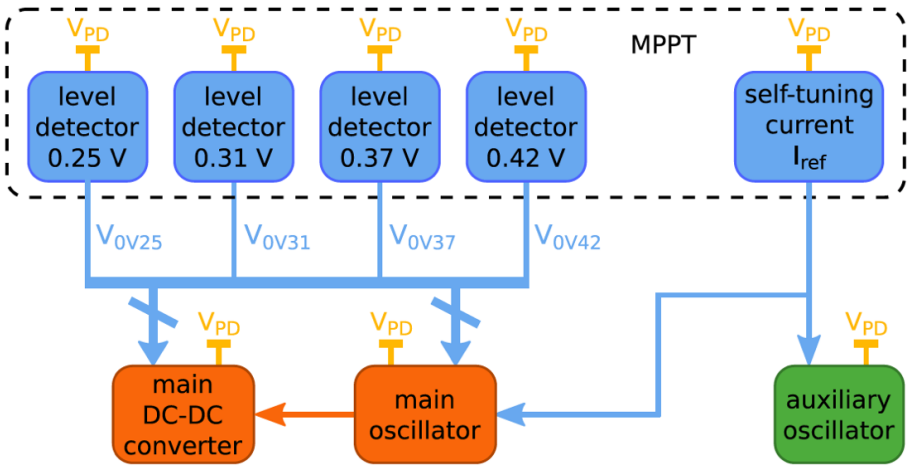

Figure 4.10 MPPT architecture presented in [48] © 2016 IEEE

In summary, this chapter presented key techniques in MPPT literature that enable SC energy harvesters to operate with higher PCE at lower power levels available in WSNs. In all the techniques discussed in this chapter, the reported peak PCE occurs at fixed, specific input and output power levels and the PCE continues to decrease elsewhere. Moreover, the performance is not optimized based on available input power, which varies significantly in WSN applications

CHAPTER 5

DISCONTINUOUS CHARGING TECHNIQUE

In this chapter, a discontinuous charging technique is proposed and a detailed theoretical analysis is presented to demonstrate how it achieves higher power conversion efficiency at lower input power levels.

5.1 Design Features

Typical SC converters continuously deliver current to the load or energy storage. This operation is referred to as conventional for the rest of this dissertation. In this work, a discontinuous charging technique is presented that enables operation at lower switching frequencies. In order to study the impact of this technique on power losses, the ideal voltage doubler in Figure 3.1 is modified as shown in Figure 5.1 (a) and discussed in detail.

Compared to conventional SC operation, this work proposes several design features. The first feature is a longer non-overlap time between the clock phases. In conventional operation, t_{NOL} is set as small as possible, such that the phases of operation do not overlap and the duty cycle of each phase is close to 50%. In discontinuous charging, d_{NOL} is defined as the ratio of t_{NOL} to the clock period as shown in (5.1), where T is the clock period. To allow utilizing this non-overlapping phase, d_{NOL} is increased to 10-20% of the period.

Second, the key feature of the proposed technique is to provide output current (I_{OUT}) only during t_{NOL}, as shown in Figure 5.1 (b). This is done by gating the clocks that control

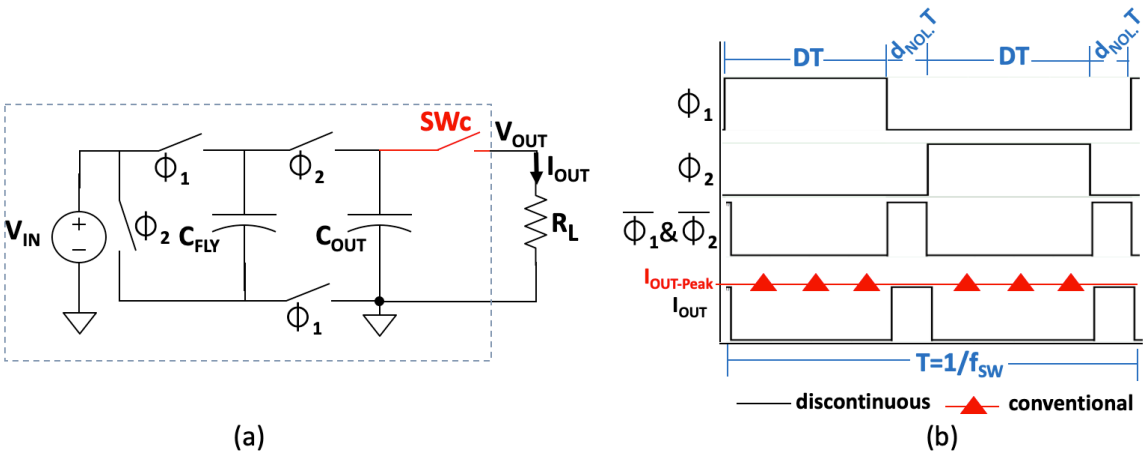

Figure 5.1 (a) Ideal SC voltage doubler with discontinuous output current. (b) Clocks and I_{OUT} waveforms for discontinuous SC voltage doubler

$$d_{NOL} = \frac{t_{NOL}}{T} \tag{5.1}$$

switch SW_C as shown in Figure 5.2. SW_C remains off during phases 1 and 2 and C_{OUT} is charged in a similar fashion to the conventional operation in Figure 3.2. However, the current is only transferred to the load or energy storage during the non-overlap phase in Figure 5.2. The purpose of these features is to control the average output current. In conventional operation, the average output is equal to the peak current ($I_{out\text{-}peak}$) and is determined by V_{OUT} and ES/load impedance. With discontinuous charging, since current

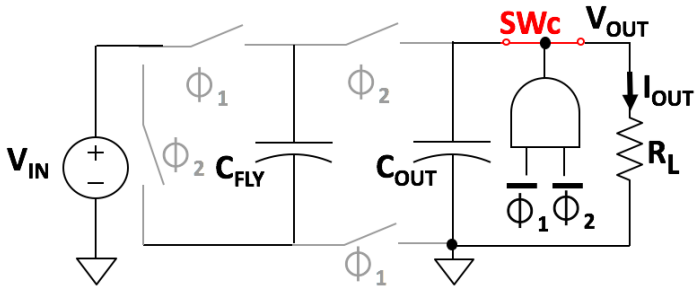

Figure 5.2 Operation during non-overlap time for ideal SC voltage doubler with discontinuous output current

is delivered only during t_{NOL}, the average output current becomes a function of d_{NOL} as shown in (5.2). This introduces d_{NOL} as a new control variable that will be utilized in this technique. The design features of the discontinuous charging technique discussed above are summarized and compared to the conventional continuous operation in Table 5.1

$$I_{OUT-avg} = 2d_{NOL}I_{OUT-peak} = 2d_{NOL}\frac{V_{OUT}}{R_L} \tag{5.2}$$

Table 5.1 Key features and parameters of the proposed design

Conventional(Continuous)	**Proposed (Discontinuous)**
d_{NOL} minimum (≈1%)	d_{NOL}=10-20%
Continuously provide output current	Provides output current only during t_{NOL}
$I_{OUT-avg} = I_{OUT-peak}$	$I_{OUT-avg} = 2d_{NOL}I_{OUT-peak}$

Since V_{OUT} and P_{ROUT} are functions of the average output current, V_{OUT} and P_{ROUT} are also now a function of d_{NOL} as shown in (5.3) and (5.4), respectively. In these equations, *n* is the voltage conversion ratio and is equal to 2 for a voltage doubler. Note that P_{ROUT} in (5.4) and P_{PAR} in (3.15) incorporate losses introduced by the additional switch SW_C.

$$V_{OUT} = \frac{nV_{IN}}{1 + 2d_{NOL}\frac{R_{OUT}}{R_L}} \tag{5.3}$$

$$P_{ROUT} = \frac{(2n.V_{IN}d_{NOL})^2\ R_{OUT}}{(R_L + 2d_{NOL}R_{OUT})^2} \tag{5.4}$$

5.2 Theoretical Analysis of Maximum Efficiency at Desired Input Power

This section discusses how controlling $I_{OUT-avg}$ minimizes power losses at a given input power. A mathematical analysis is detailed to provide the optimal PCE for a given

input power. For a fixed load resistance, the average output current in the discontinuous operation mode is smaller than its conventional counterpart due to supplying current only during t_{NOL}. If the input power drops, the system will reduce parasitic power losses in (3.15) to maintain the same PCE shown in (3.18). To accomplish that, f_{SW} is reduced. However, reducing f_{SW} increases R_{OUT} and would consequently increase P_{ROUT} and drop V_{OUT}. Therefore, reducing f_{SW} would not be possible in conventional operation.

To keep V_{OUT} in (5.3) constant and prevent P_{ROUT} in (5.4) from increasing, the additional control variable d_{NOL} is reduced to lower the average output current in (5.2). The lower losses result in achieving peak PCE at a lower P_{IN}. This effectively moves the entire efficiency curve towards a lower input power as shown in Figure 5.3 (a). If the input power increases, the opposite is done by increasing d_{NOL} in order to deliver more output power, as shown in Figure 5.3 (b). This process is summarized and presented graphically in Figure 5.4. The ability to move the peak PCE towards desired input power levels is especially advantageous in IoT applications that deploy WSNs in harsh environments, where ambient power levels vary considerably and can be very low.

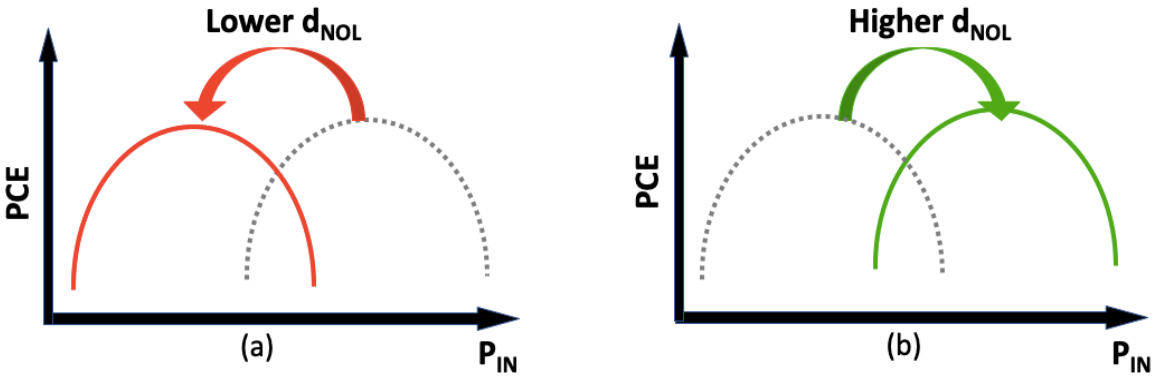

Figure 5.3 Shifting the PCE curve towards (a) lower P_{IN} (b) higher P_{IN}

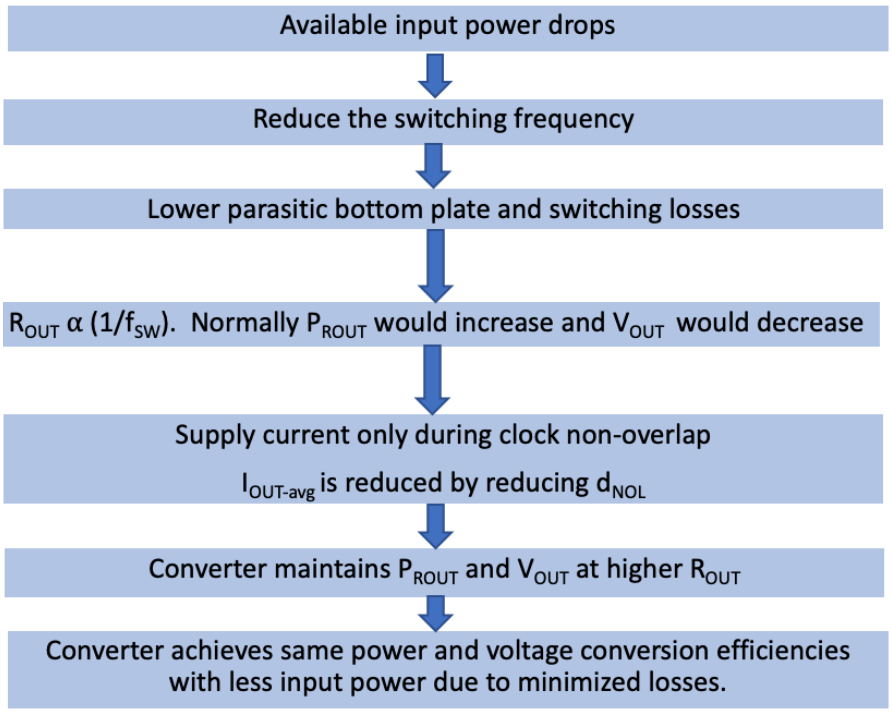

Figure 5.4 Process of achieving higher PCE and VCE at lower P_{IN}

This result can be shown mathematically by first multiplying $I_{OUT\text{-}avg}$ in (5.2) and V_{OUT} in (5.3) to find the output power as shown in (5.5).

$$P_{OUT} = V_{OUT} I_{OUT-avg} = \frac{2d_{NOL}(nV_{IN})^2}{R_L(1 + 2d_{NOL}\frac{R_{OUT}}{R_L})^2} \tag{5.5}$$

Following that, the power losses in (3.15) and (5.4), as well as P_{OUT} in (5.5), are substituted into the PCE equation in (3.18). The resulting PCE for discontinuous charging is shown in (5.6). Note that since R_{CHARGE} from (3.8) is one to two orders of magnitude larger than R_{COND} at the frequency range of operation in this design, R_{OUT} is approximated as equal to R_{CHARGE} to simplify the expression in (5.6). Moreover, all constants in (5.6) have been lumped into constants B_1 to B_4, as defined in Table 5.2, in order to clearly identify the two control variables for this scheme. It can be seen that PCE is now a function of the two

variables f_{SW} and d_{NOL} allowing for a second control knob, compared to conventional operation which is only controlled by f_{SW}.

$$PCE \approx \frac{B_1\, d_{NOL} f_{SW}}{B_2\, {d_{NOL}}^2 + B_3\, {f_{SW}}^2 + B_4\, f_{SW} d_{NOL}} \tag{5.6}$$

Table 5.2 Constant values for power conversion efficiency in (5.5)

$B_1=2n^2R_LC_{FLY}^2$	$B_3=C_{GGtot}(R_LC_{FLY})^2+xC_{FLY}^3R_L^2$
$B_2=(4n^2+4x)C_{FLY}+4C_{GGtot}$	$B_4=[4xC_{FLY}^2+(2n^2+4C_{GGtot})C_{FLY}]R_L$

Figure 5.5 represents the PCE in (5.6) as a Matlab contour plot commonly used to plot functions of two variables, where each line represents a constant PCE. It can be seen that for a constant PCE line, lower d_{NOL} enables operating at a lower switching frequency. Operating at lower switching frequency reduces parasitics power losses. Two lines exist for each efficiency value in the plot due to the PCE function's parabolic shape, as shown in Figure 3.7. This contour plot provides insight into the design methodology utilized in discontinuous charging. For lower available input power levels, lower d_{NOL} should be selected. Following that, the lowest switching frequency that achieves the desired PCE should be used. The contour plot is for a voltage doubler where R_L and C_{FLY} are 40KΩ and 160pF, respectively. Moreover, each MOSFET switch is modeled with 45Ω on-resistance and 70fF total gate capacitance.

To find the optimal frequency to operate the SC converter at, the PCE expression is differentiated with respect to f_{SW}. As shown in (5.7), the optimal switching frequency that yields the peak efficiency ($f_{SW\text{-}OPT}$) is linearly proportional to the non-overlapping time.

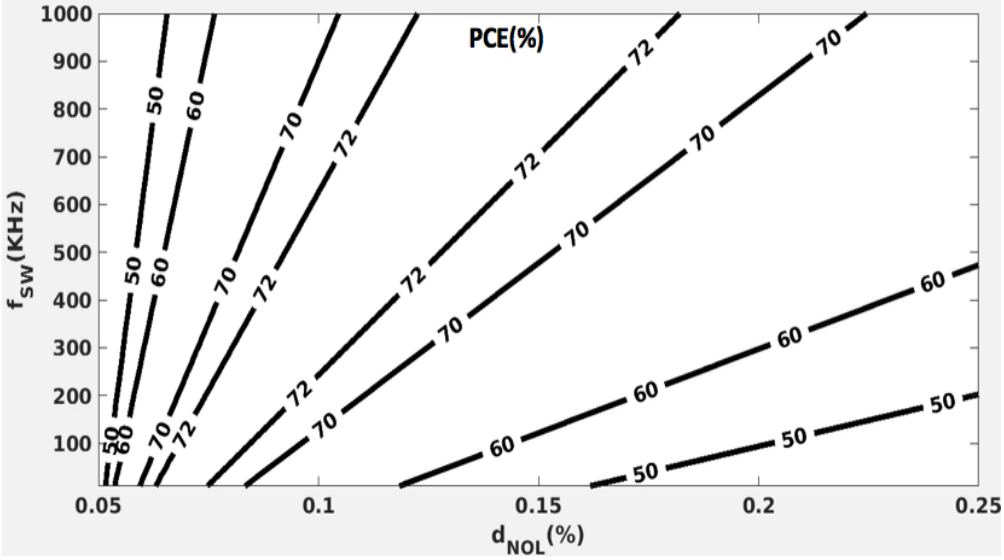

Figure 5.5 Contour plot of PCE as a function of d_{NOL} and f_{SW}

To find the input power at which this occurs ($P_{IN\text{-}OPT}$), $f_{SW\text{-}OPT}$ from (5.7) can be substituted into (3.15) and (5.4) to find P_{PAR} and P_{ROUT} at that frequency. Following that, $f_{sw\text{-}OPT}$ is also substituted in (5.5) to find P_{OUT} at this frequency. These output power and losses are then added together to find $P_{IN\text{-}OPT}$. As shown in (5.8), the optimal input power is also linearly proportional to d_{NOL}. Note that since C_{FLY} is at least two orders of magnitude larger than C_{GGtot}, C_{GGtot} is dropped when dominated by C_{FLY} to simplify the expressions in (5.7) and (5.8).

$$f_{SW-OPT} = \frac{dPCE}{df_{sw}} \approx \frac{2n}{\sqrt{x}C_{FLY}R_L} d_{NOL} \tag{5.7}$$

$$\begin{aligned} P_{IN-OPT} &= P_{OUT}(f_{SW-OPT}) + P_{ROUT}(f_{SW-OPT}) + P_{PAR}(f_{SW-OPT}) \\ &\approx \frac{2{V_{IN}}^2(n^2 + \sqrt{x}n)}{R_L} d_{NOL} \end{aligned} \tag{5.8}$$

The main result of the analysis in this chapter is that the proposed technique allows the peak power conversion efficiency to occur at lower switching frequency and consequently lower input power, by reducing the non-overlap time. This provides the theoretical basis for the optimization that is implemented in this work. The key result is that by controlling the average output current, the peak power conversion efficiency can track available harvested input power, as opposed to existing battery chargers which adjust current based exclusively on battery/load voltage [76]. The proposed discontinuous charging is only suitable for low input power levels. At higher power levels, d_{NOL} is increased further, which results in the PCE curve approaching conventional operation. At such levels, it is simpler to operate in continuous mode.

CHAPTER 6

CIRCUIT AND MATLAB MODELING OF DISCONTINUOUS CHARGING

In this chapter, in order to study and verify the proposed discontinuous charging operation, a circuit model that explicitly captures each of the power losses discussed in Section 3.3 and Chapter 5 is developed and compared to a Matlab model of the derived loss equations. As shown in Figure 6.1 (a), the model consists of two identical and parallel voltage doublers that are operated in an interleaved fashion with opposite phase clocks. They share the same input voltage source and output capacitor. This is commonly used in order to charge C_{OUT} with twice the effective frequency and reduce V_{OUT} droop [64], [77]. Switches N1 and N2 represent NMOS switches. NMOS switches are used here because the voltage they pass is low; i.e. equal to V_{IN}. Therefore, NMOS switches can pass this voltage successfully and require a smaller area to achieve the same on-resistance compared to PMOS switches due to the higher mobility of electrons compared to holes. Switches P1 through P3 represent PMOS switches, which are necessary since the voltage they pass is near $2V_{IN}$ and is therefore near logic high levels that are not possible for NMOS switches to pass fully [78].

The circuit is operated by 4-phase clocks as shown in Figure 6.1 (b). Since CLK_N and CLK_{NB} are used to drive NMOS switches N1 and N2, they must be non-overlapping

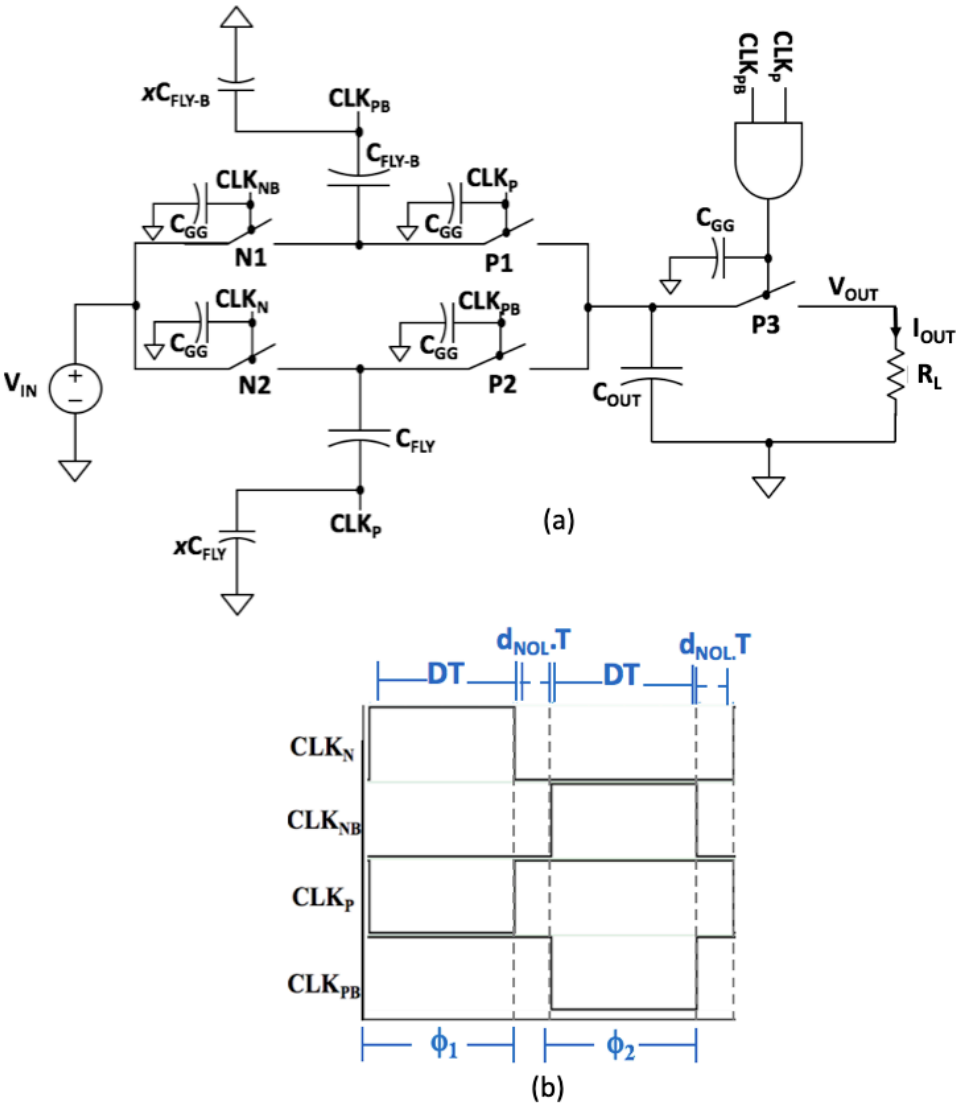

Figure 6.1 (a) Voltage doubler circuit model with discontinuous charging (b) Four-phase clock waveforms

to avoid lossy discharge of C_{FLY} and $C_{FLY\text{-}B}$. CLK_P and CLK_{PB} are used to drive PMOS switches P1 and P2 and therefore must be overlapping to avoid turning on simultaneously which causes lossy discharge of C_{OUT}. In this model, the switches have a finite resistance, R_{SW}, comparable to anticipated MOSFET on-resistance, and the power loss due to R_{OUT} in (5.4) is captured across the switches.

Following that, the parasitic switching power losses in (5.14) are modeled with capacitor C_{GG} placed where the clocks drive each of the switches. The total C_{GGtot} in (3.14) and (3.15) is the summation of all C_{GG} capacitors in the model. Similarly, the parasitic bottom plate power losses in (3.15) are modeled with parasitic capacitors placed at the bottom plates of C_{FLY} and C_{FLY-B} and are a percentage (x) of the flying capacitor values.

The interleaved operation of the two voltage doublers in phase (1) and phase (2) is shown in Figure 6.2 (a) and (b), respectively. Parasitic capacitors are removed from the

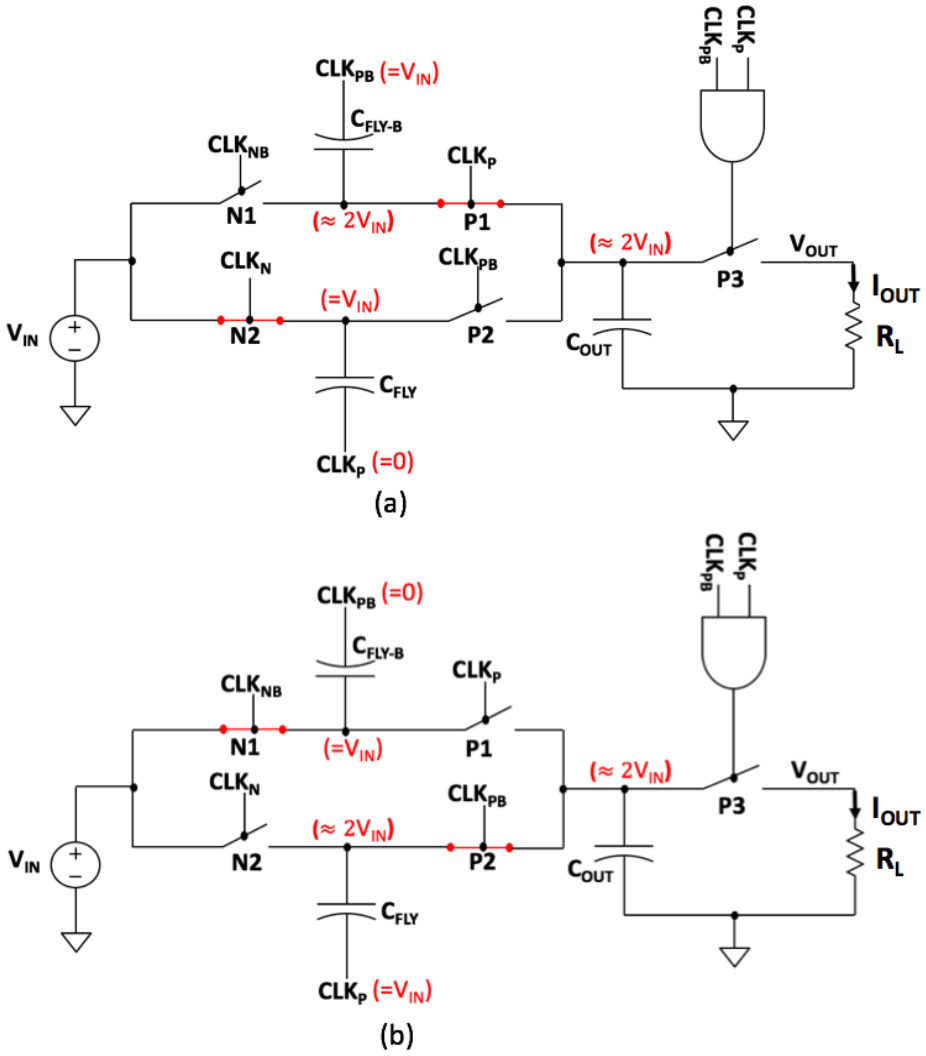

Figure 6.2 Circuit model operation during (a) Phase 1 (b) Phase 2

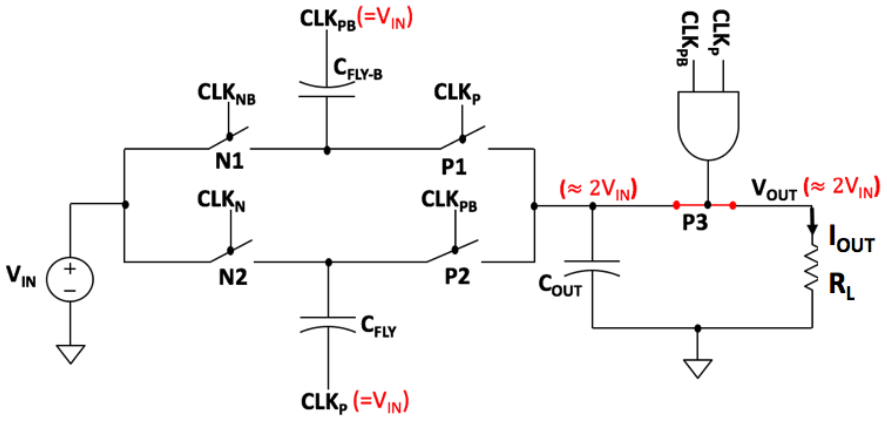

Figure 6.3 Circuit model operation during the clock non-overlap phase

figure to demonstrate the basic operation of the circuit. In phase (1), switch N2 is on to charge C_{FLY} to voltage V_{IN} whereas switch P1 is on in order to charge C_{OUT} to approximately twice V_{IN} through C_{FLY-B} which is previously charged up to $2V_{IN}$. In phase (2) switches N1 and P2 charge C_{FLY} and C_{OUT} to V_{IN} and $2V_{IN}$, respectively. In both phases, switch P3 remains off to disconnect the output capacitor which delivers the output current. During the clock non-overlap time, shown in Figure 6.3, only switch P3 is on in order to deliver output current from C_{OUT}.

The circuit model is simulated using HSPICE and the power losses and output power are measured and compared to a Matlab model which consists of the voltage and power equations from the mathematical derivation in Chapter 5. The Matlab model can be found in Appendix B. For both models, the input voltage is 0.6V and R_L and C_{FLY} are 40KΩ and 80pF, respectively. Moreover, each switch has approximately 45Ω on-resistance and 70fF C_{GG} and the bottom plate capacitance is 10% of C_{FLY} by setting x=0.1. As shown in Figure 6.4, P_{PAR} is linearly proportional to the switching frequency and the results of the circuit simulations and Matlab models are very similar.

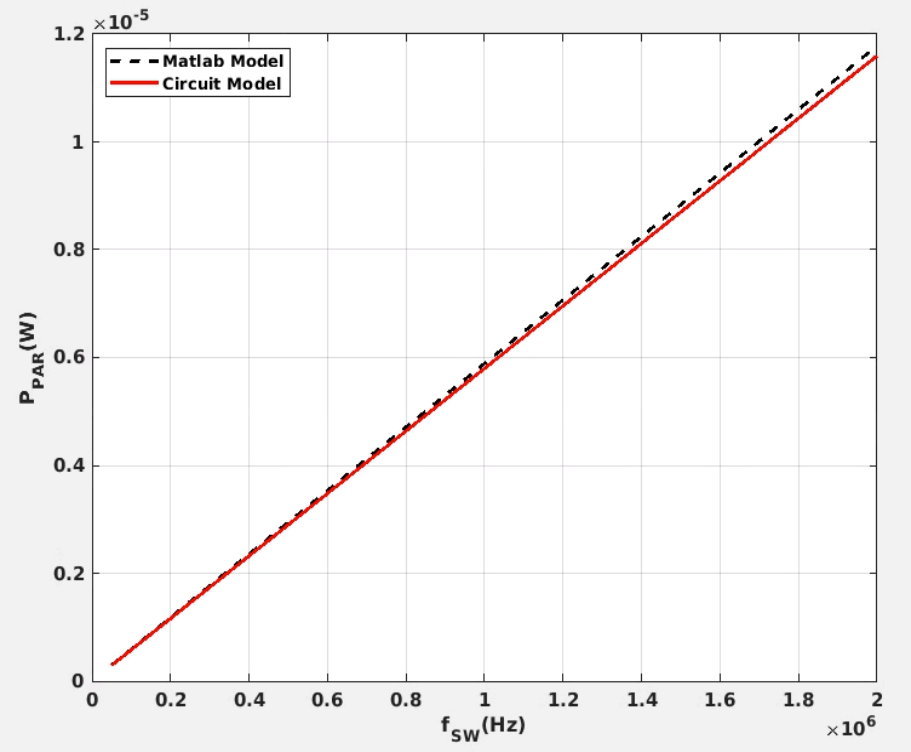

Figure 6.4 P_{par} for circuit model vs. Matlab equations model. V_{IN}=0.6V, n=2, d_{NOL}=5%, C_{FLY}=80pF, R_L=40kΩ

Furthermore, P_{ROUT} is shown in Figure 6.5. As expected, P_{ROUT} is inversely proportional to f_{SW} in both models. However, it can be seen that P_{ROUT} in the circuit model slightly deviated from its corresponding Matlab equation. This is because the circuit model captures the exact R_{OUT}, whereas the Matlab model uses the Euclidean norm approximation in (3.8). Finally, as shown in Figure 6.6, P_{OUT} is also inversely proportional to switching frequency. This is due to the output impedance which increases and results in a lower output voltage at slower switching frequencies.

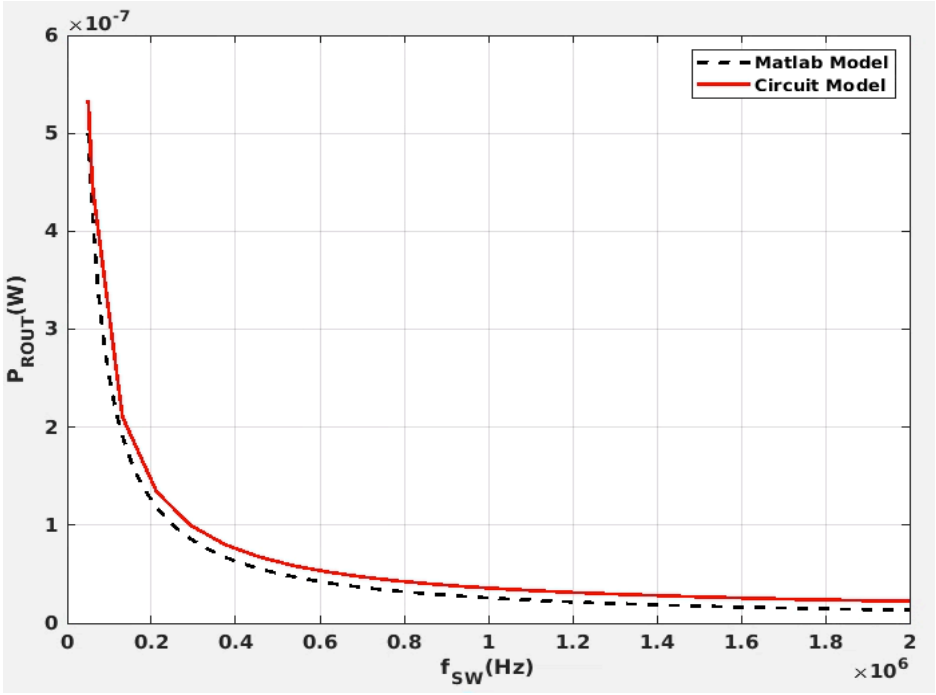

Figure 6.5 P_{ROUT} for circuit model vs. Matlab equations model. V_{IN}=0.6V, n=2, d_{NOL}=5%, C_{FLY}=80pF, R_L=40kΩ

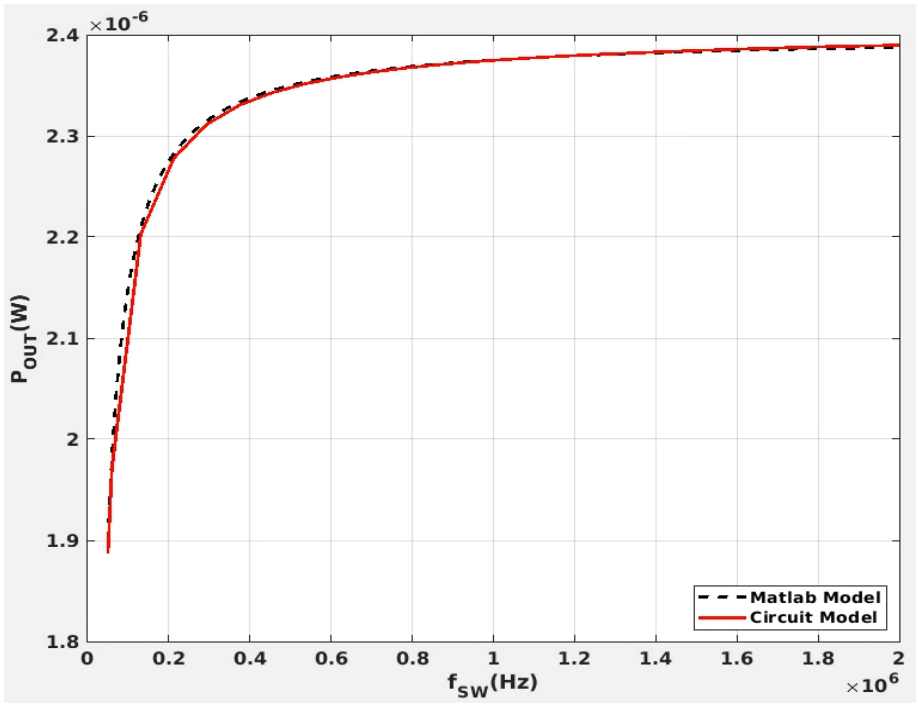

Figure 6.6 P_{OUT} for circuit model vs. Matlab equations model. V_{IN}=0.6V, n=2, d_{NOL}=5%, C_{FLY}=80pF, R_L=40kΩ

In Figure 6.7, PCE is plotted as a function of P_{IN} for the Matlab model vs. simulations of the circuit model. It can be seen that reducing d_{NOL} results in reducing $P_{IN\text{-}OPT}$. In the circuit model simulations, P_{IN_OPT} values for 10% and 15% d_{NOL} are 6.1µW and 8.4µW, respectively. Substituting in (5.8), the corresponding values for 10% and 15% d_{NOL} are 5.8µW and 8.7µW, respectively. The 0.3µW difference is due to the approximations discussed earlier in the derivation.

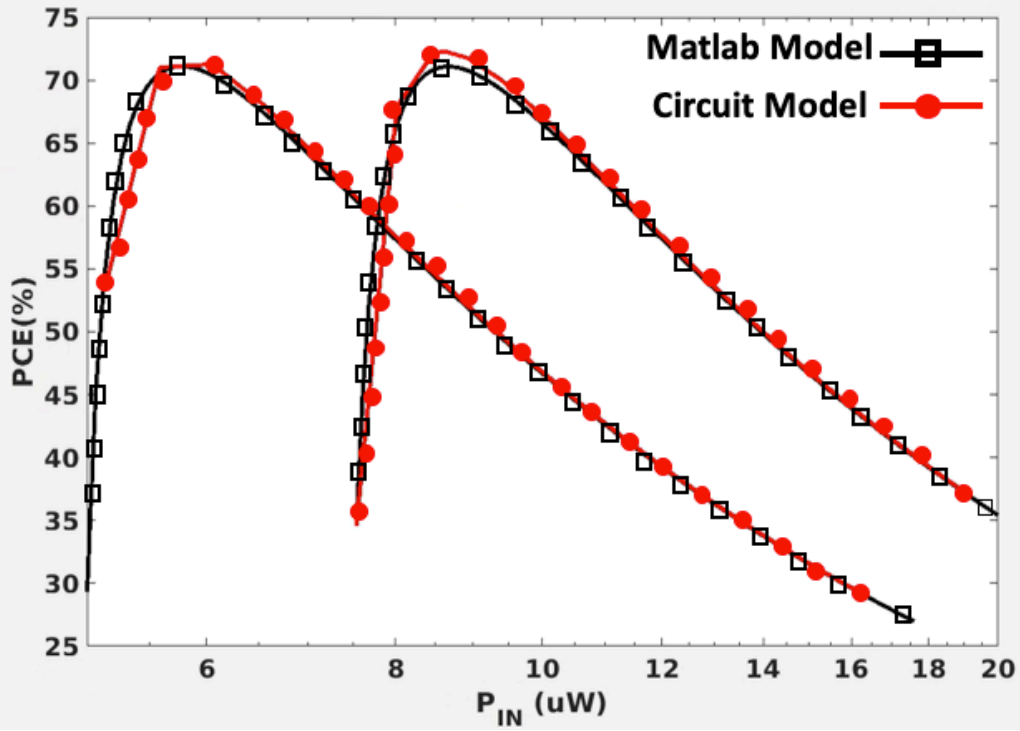

Figure 6.7 PCE vs. P_{IN} for circuit model vs. Matlab equations model d_{NOL}=10% (Left) and d_{NOL}=15% (Right). V_{IN}=0.6V, n=2, C_{FLY}=80pF, R_L=40kΩ.

Lastly, in Figure 6.8 the circuit model is used to plot PCE and VCE vs. P_{IN} for conventional continuous operation vs. the proposed discontinuous operation with d_{NOL} set to 5%,10%, and 15% of the period. It can be seen that the peak PCE occurs at 9.6-28.7% of the input power compared to the conventional circuit, depending on d_{NOL}. This allows

the proposed circuit to remain operational with high efficiency when the input power levels cause the conventional efficiency to drop significantly. Moreover, VCE is also higher at lower input power because the proposed discontinuous operation utilizes d_{NOL} to keep V_{OUT} constant when reducing the switching frequency, as discussed in Section 5.2.

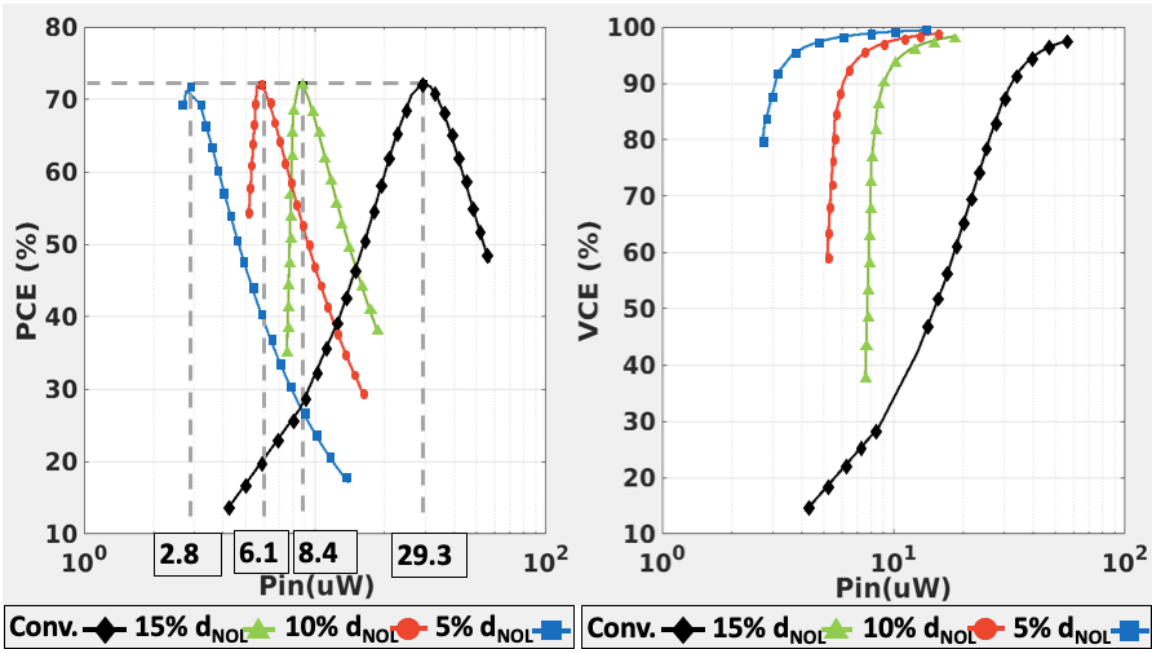

Figure 6.8 (a) PCE vs. P_{IN} for different non-overlap times vs. conventional (b) VCE vs. P_{IN} for different non-overlap times vs. conventional

In summary, this chapter presented a circuit model that explicitly captures each of the power losses discussed in Section 3.3 and Chapter 5. The circuit model results were compared to a Matlab model of the derived power equations and the results matched closely for the various power losses and PCE. Furthermore, in both models, it was shown that reducing d_{NOL} successfully shifts the PCE curve towards lower input power.

CHAPTER 7

MAXIMUM EFFICIENCY TRACKING TECHNIQUE

In this chapter, the proposed discontinuous charging is utilized to design a maximum efficiency tracking technique that provides two-dimensional optimization of power conversion efficiency. Furthermore, the circuit implementation of the system is detailed.

7.1 Two-Dimensional Maximum Efficiency Tracking

Conventional MPPT schemes only tune f_{SW} to adjust R_{OUT} in (3.8) with the goal of minimizing the power losses in (3.10) and (3.15), which results in a limited harvesting range. The proposed architecture utilizes the discontinuous charging technique discussed in Chapter 5 by adding clock non-overlap time tuning to adjust the average output current. This is combined with the conventional f_{SW} control to allow for a two-dimensional optimization of PCE. The additional control variable enables the system to extend the harvesting range towards lower power levels by dynamically shifting the entire PCE curve towards desired P_{IN} levels as shown in the conceptual illustration in Figure 7.1. Figure 7.2 presents a flowchart of the proposed technique. First, the input power provided by the energy source is sensed. Then, the clock control block selects the appropriate operation mode and d_{NOL}. Following that, the system sweeps the switching frequency and locks it at the optimal output current delivered to the energy storage.

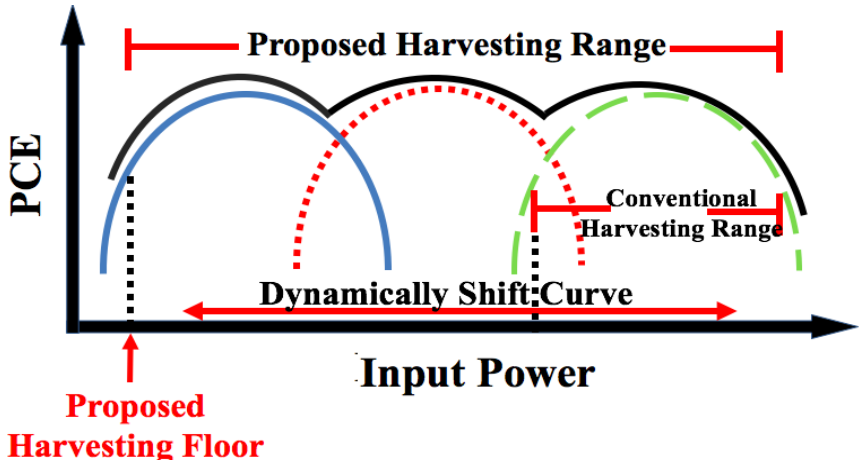

Figure 7.1 Conceptual efficiency illustration of the proposed technique

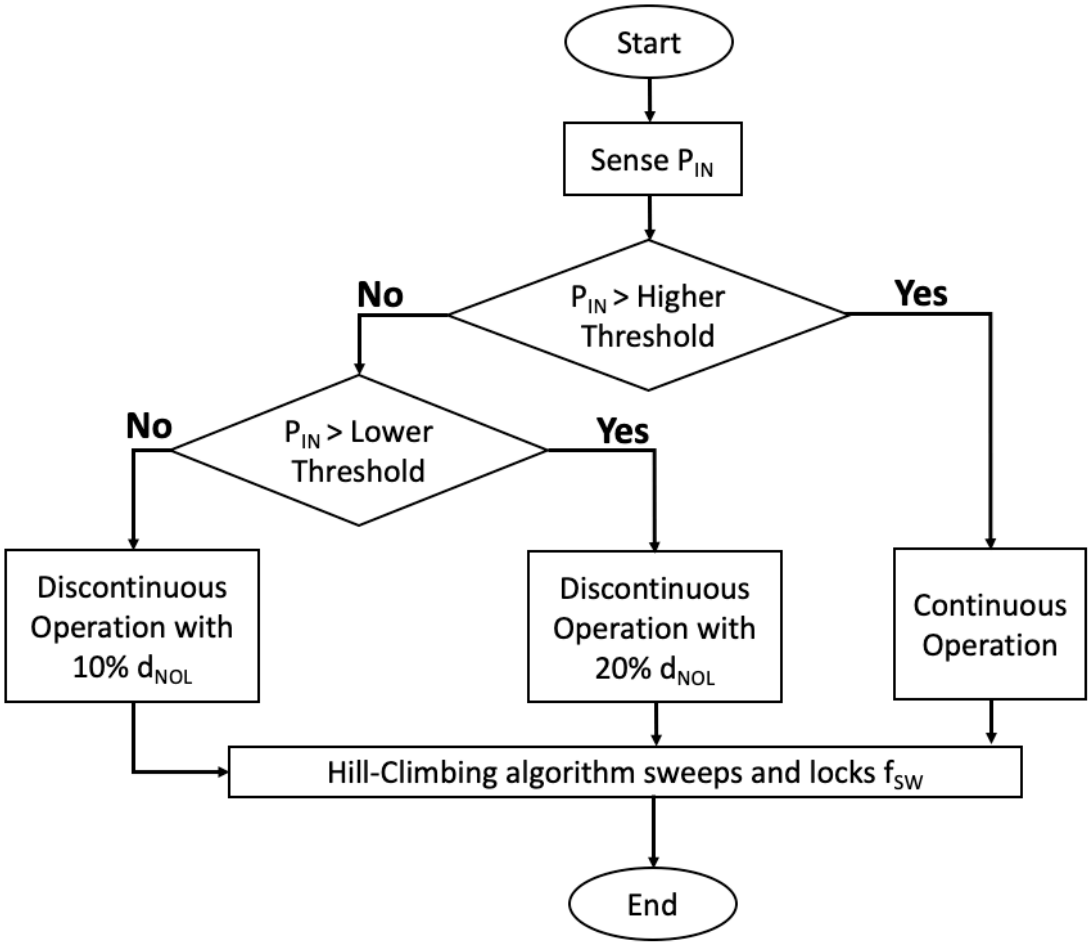

Figure 7.2 Proposed two-dimensional tracking technique flowchart

7.2 Circuit Implementation

This section discusses the circuits designed to implement the proposed technique. In Figure 7.3, a block diagram of the proposed two-dimensional efficiency tracking system is presented and will be referenced in the following subsections.

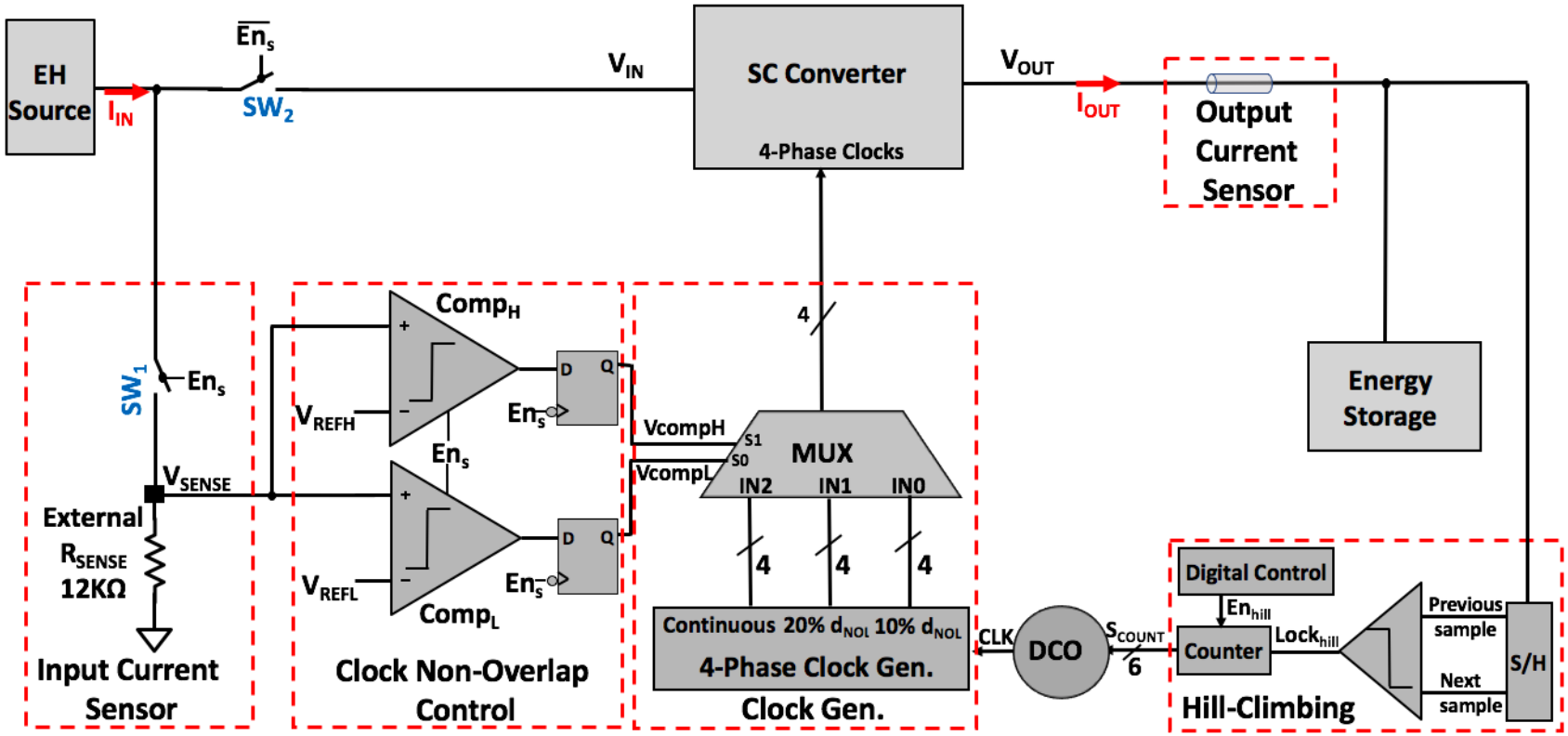

Figure 7.3 Block diagram of the proposed two-dimensional maximum efficiency tracking technique

7.2.1 Input Power Sensing and Clock Non-Overlap Control

When WSN nodes are placed in harsh environments, the available P_{IN} for harvesting can vary significantly. Hence, this work provides the advantage of shifting the peak PCE towards the suitable range of P_{IN} in order to deliver as much power as possible to energy storage. This is achieved by first sensing the input current supplied by the energy harvesting source (I_{IN}) shown in Figure 7.3. When signal EN_S enables the sensing process, the source is momentarily disconnected from the SC converter and I_{IN} flows through the external sensing resistor, R_{SENSE}. The resulting proportional voltage, V_{SENSE}, is compared to low and high reference voltages by comparators $Comp_L$ and $Comp_H$, respectively. At the end of the sensing period, the decisions are latched and the four-phase clock generator and MUX produce the appropriate operation mode and d_{NOL} value, as shown in Table 7.1. The clock control block selects continuous operation if P_{IN} is high enough to provide a larger constant output current efficiently. In this case, the system operates in a conventional manner. If P_{IN} is too low to sustain efficient continuous charging, the clock control block selects discontinuous operation with the appropriate d_{NOL}. This dynamically tunes the average output current and shifts the peak PCE to the appropriate P_{IN} levels as was shown in Figure 7.1.

Table 7.1 Clock operation mode control

V_{SENSE} Range	Operation Mode	d_{NOL}	$I_{OUT-avg}$
$V_{SENSE}<V_{REFL}$	Discontinuous	10%	$0.2I_{OUT-peak}$
$V_{REFL}<V_{SENSE}<V_{REFH}$	Discontinuous	20%	$0.4I_{OUT-peak}$
$V_{SENSE}>V_{REFH}$	Continuous	<1%	$I_{OUT-peak}$

In order to minimize power, the comparators are operated in the sub-threshold region and are only enabled when in use during the short time required for the comparators to resolve. For many IoT applications, it is not necessary to sense ambient power frequently. This is because many WSN nodes only turn on briefly to sense and transmit data and remain in standby for the rest of the time [79], [80]. Hence, average power losses due to the sensing operation are negligible, as seen in the simulation results in Section 8.6.

Finally, this sensing method requires that the input be disconnected from the converter during the time required to sense the current. However, this is not uncommon in MPPT techniques, such as the fractional open-circuit method shown in [81]. Moreover, the duty cycle at which the input power sensing occurs (d_{SENSE}) is very low, which minimizes the power losses.

7.2.2 Voltage Doubler with Mode Selection

The proposed system requires the SC converter to have the capability of switching between continuous and discontinuous charging. The cross-coupled CP voltage doubler in Figure 7.4 (a) is designed accordingly, and the clock waveforms are shown in Figure 7.4 (b). The circuit is similar to the circuit model shown in Figure 6.1 (a) and consists of two identical and parallel voltage doublers that are operated in an interleaved fashion with opposite clocks. This is used in order to charge C_{OUT} with twice the effective switching frequency, as one of the voltage doublers will always be connected to C_{OUT} at any given time. C_{OUT} is selected to be an order of magnitude larger than C_{FLY} to reduce output voltage ripple. The gates of switches N1 and N2 are cross-coupled through devices N3 and N4 resulting in a positive feedback mechanism that causes the gate of N1 or N2,

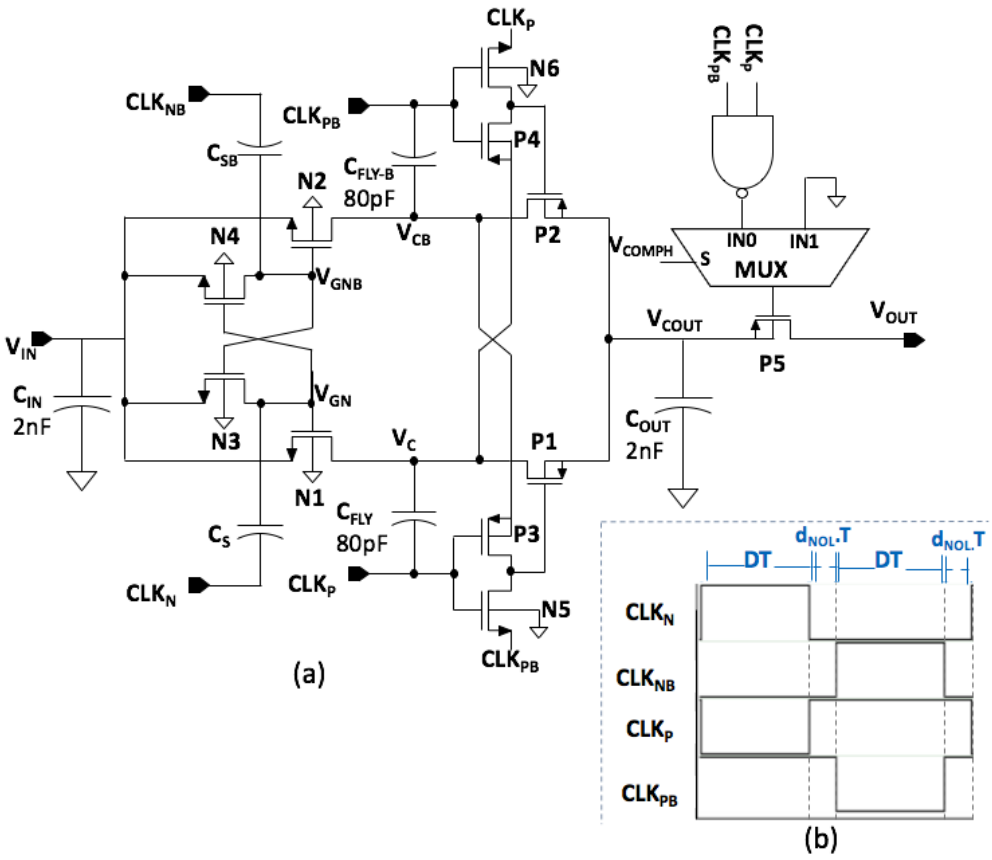

Figure 7.4 (a) Voltage doubler with mode selection (b) Clock Waveforms

depending on the phase of operation, to increase higher than V_{IN} and allow V_{GS} to be higher than the threshold (V_{th}) of N1 and N2.

The PMOS switch, P5, is added before the converter's output. P5 is controlled by a MUX that passes a logic zero to the switch if it is required to be always on for continuous operation. If discontinuous operation is selected, CLK_P and CLK_{PB} are gated and the MUX enables P5 only during clock non-overlap. The MUX is controlled by the V_{COMPH} signal in the clock control block of Figure 7.3. Moreover, care must be taken in MOSFET bulk connections to avoid any forward bias of undesired P-N junctions between the source/drain and the bulk of each device. For NMOS devices, this is easily achieved by connecting all bulks to ground. For PMOS devices, the bulk must connect to the highest possible voltage

across all phases of operations. For example, for P1 and P2, V_{COUT} is approximately $2V_{IN}$ in all phases of operation, whereas V_C and V_{CB} alternate between V_{IN} and approximately $2V_{IN}$. Hence, the bulks of P1 and P2 must connect to V_{COUT} to avoid forward bias the bulk to source/drain P-N junction.

Since this voltage doubler is intended for operation under very low power level conditions, the switching frequency can drop to less than a few hundred kHz to ensure that parasitic losses are not restrictively large. However, this can increase the R_{CHARGE} component of the output impedance. Under such conditions, R_{CHARGE} is significantly larger than R_{COND} for reasonably-sized switches, even if a large flying capacitor is used. Thus, the MOSFET switches must be sized to ensure that their total resistance is lower than R_{CHARGE}, but should not be increased beyond that to avoid increasing parasitic switching losses without noticeable improvement of the output impedance. The device sizes used in the voltage doubler are shown in Table 7.2.

Table 7.2 Voltage doubler device sizes

Device	W/L	Device Multiplier
N1, N2, P1, P2	3.8um/0.1um	4
N3, N4	0.23um/0.2um	2
N5, N6	2um/0.2um	1
P3, P4	4um/0.2um	1
P5	3.8um/0.1um	1

7.2.3 Switching Frequency Tuning

To find the optimal switching frequency, the system sweeps the switching frequency using a hill-climbing algorithm commonly used in MPPT schemes, as shown in

Figure 7.5. To reduce static power consumption, a digital hill-climbing similar to [8] is incorporated in this system. A power-efficient current sensor such as in [82] can be used to sense the output current and supply a proportional voltage V_{SENSE_OUT}. When the process begins, EN_{hill} control signal is set to logic high. When control signal S_{TUNE} is high, the S/H circuit samples V_{SENSE_OUT} on sampling capacitor C_{S1} or C_{S2}, depending on the polarity of S_{FLIP}. When S_{TUNE} is low, the comparator compares the new and previous values of V_{SENSE_OUT}. If the new value is larger than the previous, the comparator output, after polarity correction by an XOR gate, remains high. Therefore, the $Lock_{hill}$ signal remains high allowing the 6-bit up/down counter to increase the frequency of the digitally-controlled oscillator (DCO). When the new V_{SENSE_OUT} drops below its previous value, this indicates that the maximum efficiency is captured and $Lock_{hill}$ de-asserts. Consequently, the counter counts down one step and EN_{hill} disables the counter to lock the frequency at the maximum output power point.

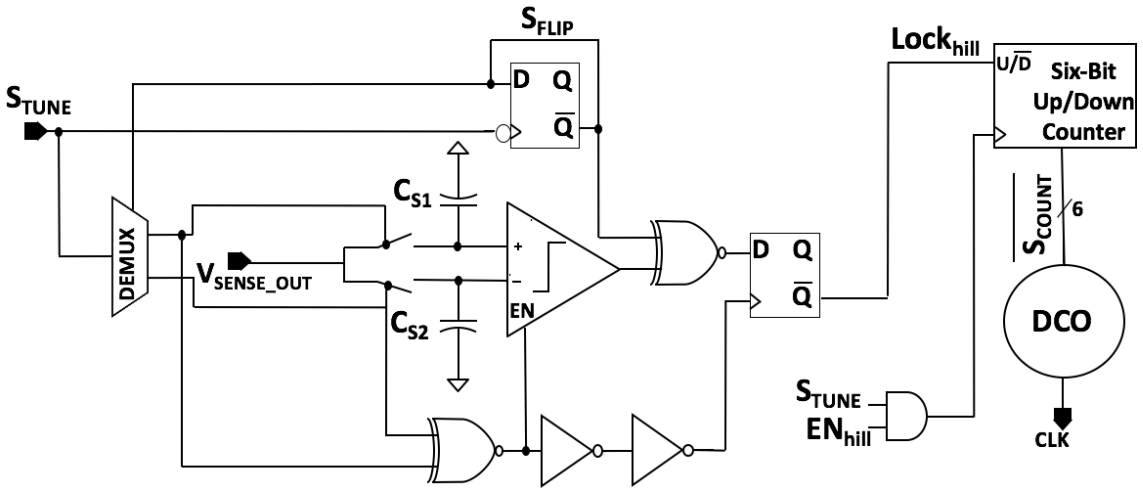

Figure 7.5 Switching frequency tuning through digital hill-climbing

7.2.4 Four-Phase Clock Generation

To generate the main clock while minimizing the power consumption, the DCO in Figure 7.6 is used. A 6-bit current digital to analog converter (DAC) controls the current available for a 5-stage ring oscillator. This controls how fast/slow the inverters can charge up to logic high and down to logic low. After the ring oscillator, the clock is buffered to isolate the ring oscillator from any loading that can impact the frequency. The buffered clock is then level shifted via inverters to the V_{IN} domain as needed by the voltage doubler. Since the inverters will be constantly switching, their supply voltage node, $I_{DCO,}$ will be noisy. Hence, capacitor C_{DCO} is placed on that node to reduce these ripples. To achieve the required frequency range with the current DAC alone, a wide range of currents would be needed, resulting in high power consumption at high frequencies. To avoid that, DCO power consumption is minimized by adding a 6-bit capacitor array to load each inverter stage in the ring oscillator. This provides further control of the frequency while limiting the required current range. The digital hill-climbing counter output S_{COUNT} programs both the current DAC and capacitor array simultaneously.

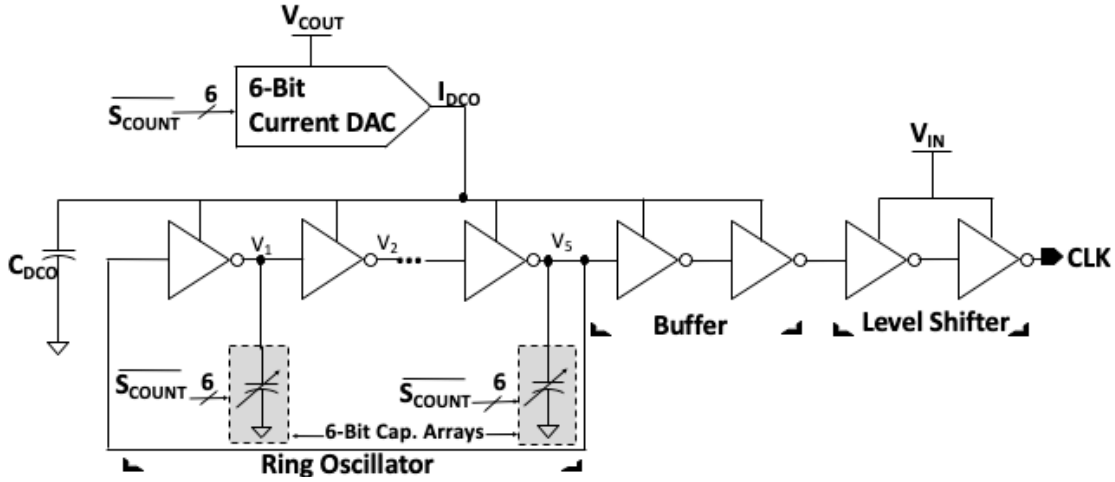

Figure 7.6 DCO circuit

The 6-bit current DAC is shown in Figure 7.7. Due to the strict power constraint in the target IoT applications, there is no bandgap voltage reference circuit to generate the reference current (I_{REF}). Instead, I_{REF} is generated with the V_{SG} voltage of PMOS P1 across a resistor R_{REF}. Unlike a bandgap reference voltage, V_{SG} will vary, for example with temperature and power supply variations. Additionally, on-chip resistors such as poly resistors can vary significantly. Therefore, to minimize variations to I_{REF}, an external reference resistor with ± 1% tolerance is needed. A commercially available 17.4MΩ resistor is selected for this design [83]. The reference current is then mirrored into binary-weighted, simple current mirrors and switches to select the desired current values. PMOS P8 is an always-on switch placed to minimize systematic offset between the reference current and other current branches. Finally, the capacitor C_{DAC} is placed to stabilize the bias voltage V_{BIAS} and improve power supply rejection ratio (PSRR). This keeps V_{SG} stable for the mirrors by coupling V_{BIAS} to the supply if high-frequency noise occurs on the power supply.

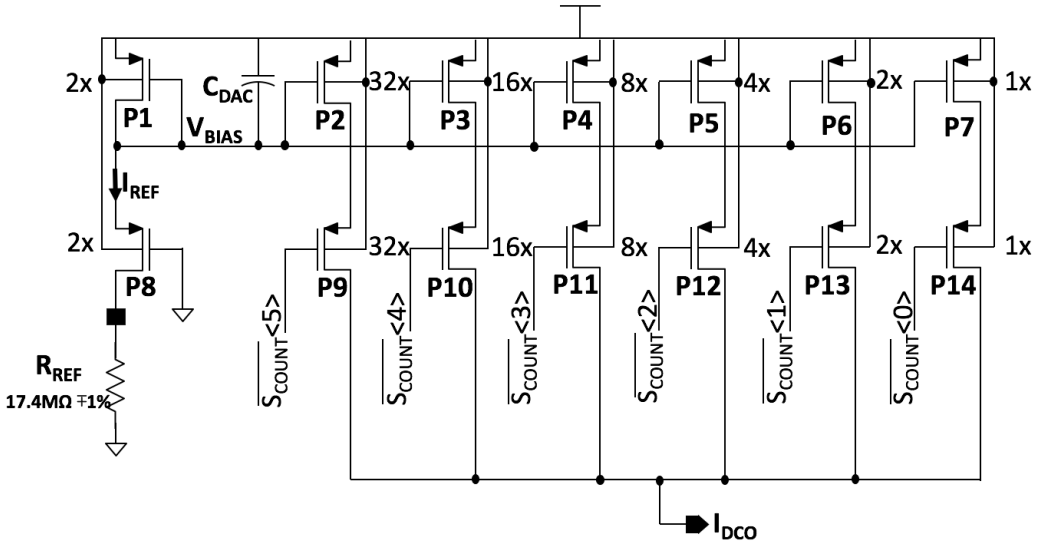

Figure 7.7 DCO 6-bit current DAC

The 6-bit capacitor array is shown in Figure 7.8. S_{COUNT} controls a binary-weighted MOS capacitor array where all branches turn on for the slowest frequency and branches are turned off in a binary fashion to reduce loading in the ring oscillator as frequency increases. The capacitors are implemented with MOS capacitors to achieve a smaller area. V_n denotes each of the V_0 through V_5 inverter outputs in the DCO.

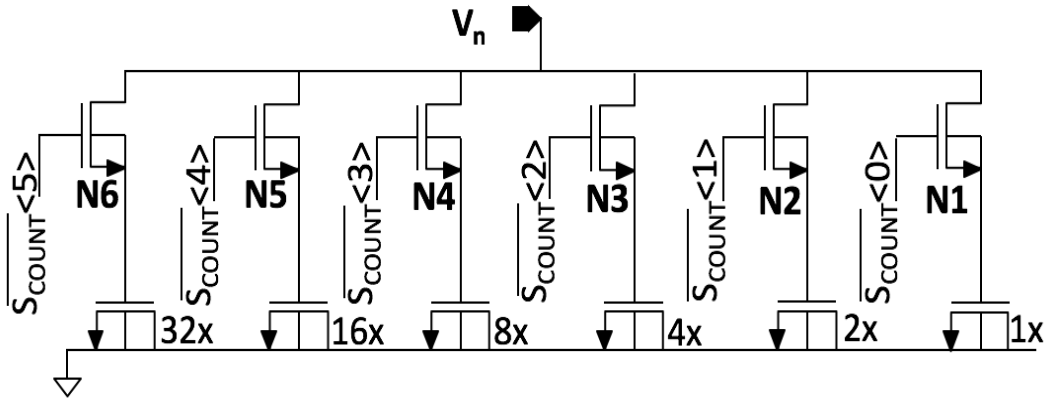

Figure 7.8 DCO 6-bit capacitor array.

The four-phase clock generator circuit is shown in Figure 7.9. For continuous operation, a conventional non-overlapping clock circuit is used [82]. For discontinuous operation, larger non-overlaps are required and cannot be provided using the same circuit. Thus, clocks are generated by utilizing the multiple phases of a ring oscillator-based DCO. Digital logic operations are performed on the DCO phases to achieve the desired d_{NOL}. For this implementation, 10% and 20% d_{NOL} are generated. Additional DCO phases and logic may be utilized to generate more non-overlap values. However, this also requires additional comparators for the clock non-overlap control in Figure 7.3, in order to set P_{IN} thresholds to control d_{NOL}. The trade-off with increased system complexity and power consumption may be counter-productive for small-sized, power-constrained WSN nodes. Finally, to

save power, unused circuits are disabled using the clock control signals V_{compH} and V_{compL} in Figure 7.3.

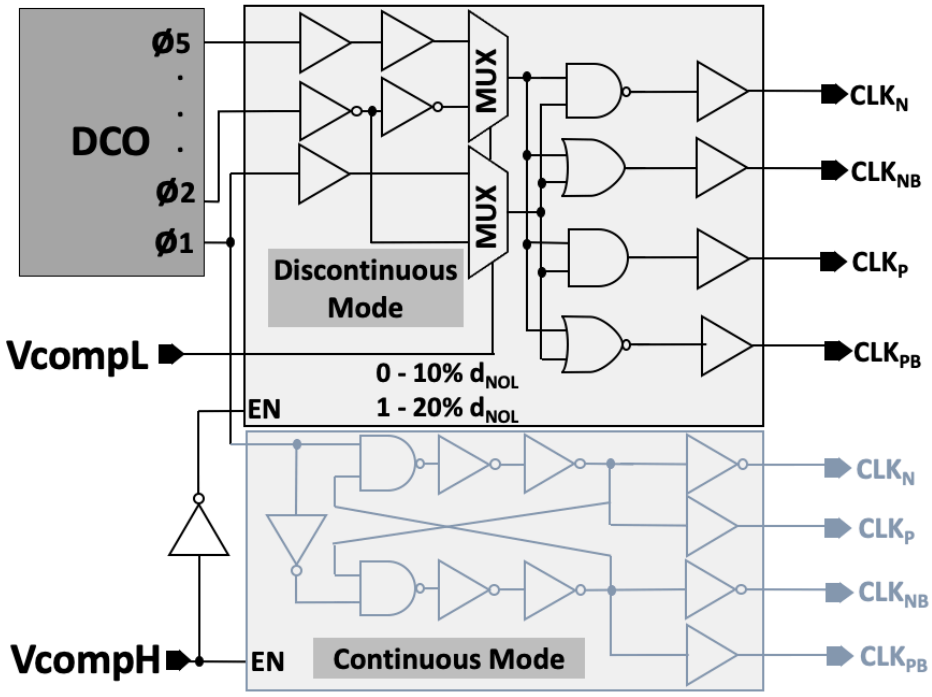

Figure 7.9 Four-phase clock generator

In this chapter, the circuit implementation of a two-dimensional tracking technique was discussed in detail to show how the system can adaptively optimize PCE based on sensed input power.

CHAPTER 8

SIMULATION RESULTS

In this chapter, the verification methodology and system specifications are discussed. Following that, simulation results are presented to demonstrate the system's functionality, test its robustness, and characterize its performance.

8.1 Verification Methodology

The discontinuous charging concept was first verified using Matlab equations and the circuit model in Chapter 5. Following that, industry-grade integrated circuit design tools have been used to build the transistor-level implementation of the system, as shown in the circuits of Section 7.2. Specifically, Synopsys Custom Compiler IC design tools have been used with a 90nm CMOS physical design kit (PDK) to build the schematics as well as the system layout. The layout is verified with the design rules checks (DRC) and the layout vs. schematic checks (LVS) provided with the PDK. Moreover, all functional and transient simulations were performed using Synopsys HSPICE with the device models provided with the PDK, which account for all MOSFET and passive device non-idealities.

To verify the design's robustness, simulations are performed over process, voltage, and temperature (PVT) variations. This accounts for variations in device parameters such as MOSFET threshold voltage, as well as variation in available input voltages. PVT simulations are required for analog circuitry to guarantee functional operation across PVT variations and increase confidence that simulation results will match measured silicon

results. Additionally, to characterize the system's efficiency, simulations are performed for various output currents and input voltages.

Finally, RC extraction is performed for the SC converter and post-layout simulations are performed to account for layout parasitic resistances and capacitances. Post-layout simulations are most critical for high-speed systems where metal parasitic capacitance and resistance can have major impacts on performance, or high-power designs where voltage drops can be large across metal parasitic resistances. The proposed technique is intended for low-power and low-speed applications where layout parasitics have minimal impact on performance. Nonetheless, the voltage doubler in Figure 7.4, which is the most important circuit for parasitics, has been RC-extracted for post-layout simulations.

To conclude, the verification methodology in this dissertation utilizes the same design kits, simulation tools, and methodologies adopted and standardized by the semiconductor industry and research.

8.2 System Specifications

The proposed system is designed and simulated in 90nm CMOS technology in order to demonstrate the PCE improvement that the discontinuous charging achieves. While this technique is applicable to any CMOS process, the 90nm process node is selected because it provides lower MOSFET V_{th} compared to larger nodes such as 0.18μm. Moreover, it allows for the higher voltages, lower leakage, and lower costs necessary for WSNs, as opposed to more recent nodes such as 28nm and FinFET technologies. The system is designed for an input voltage range from a DC energy harvester, such as mm-scale solar cells commonly used in WSNs. The output voltage of such solar cells is usually 0.2-0.65V depending on size and illuminance [2], [23], [84]. Therefore, this system is

specified for 0.5-0.7V. Lower voltages degrade performance as they approach V_{th} in this technology, while higher voltages cause device reliability concerns.

The system doubles the voltage and stores the energy to be used by a low-power WSN node. The flying capacitors are implemented with metal-insulator-metal (MIM) capacitors. The input/output capacitors are implemented with MOS capacitors to achieve a smaller area. This is because they are large storage capacitors and their variation across PVT corners is not critical for system performance. The DCO implemented in this system provides a 50KHz-3.5MHz frequency range in order to accommodate the slow frequencies needed for discontinuous operation and the fast frequencies needed for continuous operation. To facilitate simulation measurements of PCE and VCE, a 40kΩ load is connected for appropriate output current values.

8.3 Functional and Transient Simulations

In Figure 8.1, the operation of the current sensor and clock non-overlap control blocks is shown. The sensing operation is completed in 10μs as this time is sufficient for a reliable decision. As I_{IN} increases, V_{SENSE} increases and the comparators output the correct decision to adjust the average output current as shown. If I_{IN} is less than 15μA, 10% d_{NOL} is selected. If I_{IN} is between 15-30μA, the system switches to 20% d_{NOL}. Finally, if I_{IN} is larger than 30μA, the system switches to continuous operation. The sensing operation can be performed as often as needed for a specific application. In these simulations, the sensing is enabled once per minute which is sufficient to track variations in available power from DC energy harvesters. The circuits remain in standby otherwise in order to minimize power consumption.

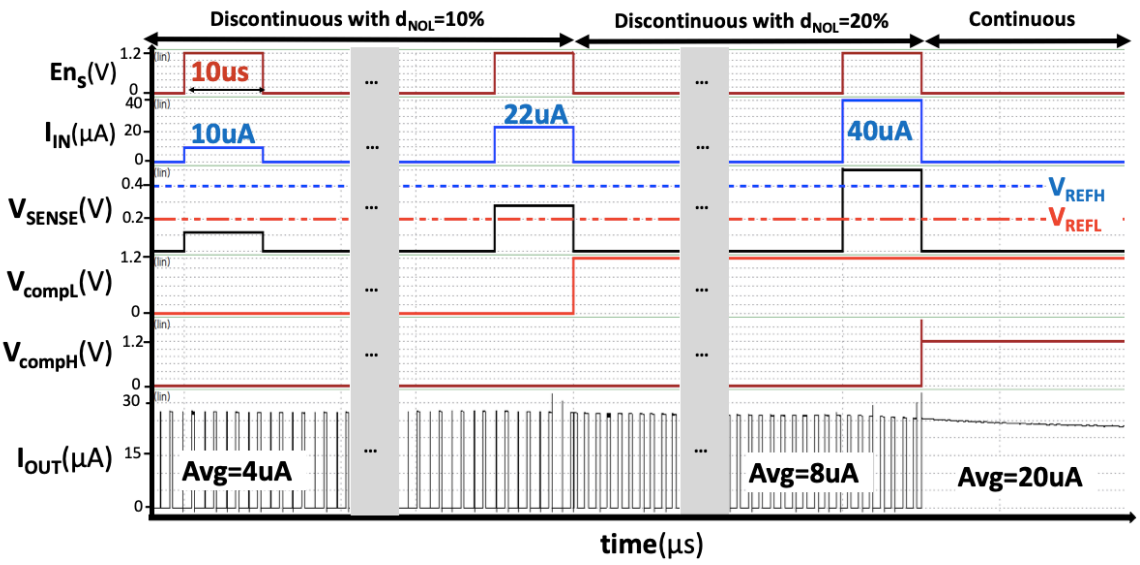

Figure 8.1 P_{IN} sensing and clock control tuning $I_{OUT\text{-}avg}$ at different P_{IN}

Figure 8.2 (a) shows how the hill-climbing logic sweeps f_{SW} and stops the counter controlling the DCO to lock f_{SW} at the highest PCE. The operation is performed in less than 1ms and is only enabled once a minute. Since the tuning operation is much slower than f_{SW}, a close-up of the operation at different frequencies is shown in Figure 8.2 (b).

Figure 8.3 and Figure 8.4 present transient simulations for the entire system in Figure 7.3 to show the 2D tracking. In Figure 8.3, a step change in the input voltage is applied to the settled system operating discontinuously with 10% d_{NOL}. In Figure 8.4 a step change in the output current is applied to the settled system operating in continuous mode, to demonstrate the system's response to a load transient. In both scenarios, P_{IN} is also changed and the step in V_{IN} or I_{OUT} is applied immediately as the P_{IN} sensing is enabled to demonstrate the 2D operation of the proposed system. The SC converter continues operation but is no longer providing the best V_{OUT} at optimal PCE. Once the P_{IN} sensing circuit is enabled via En_S, the comparators switch the system to the appropriate discontinuous operation. Next, hill-climbing logic sweeps f_{SW} to find the maximum output

power point. When the optimal point is captured, the $Lock_{hill}$ control signal de-asserts to count one step back to the optimal point and disable the counter controlling the DCO. This locks f_{SW} at the highest PCE as shown in the PCE measure in the figures. These simulations show how the system settles at optimal PCE with the new d_{NOL} and f_{SW} in less than 1.5ms.

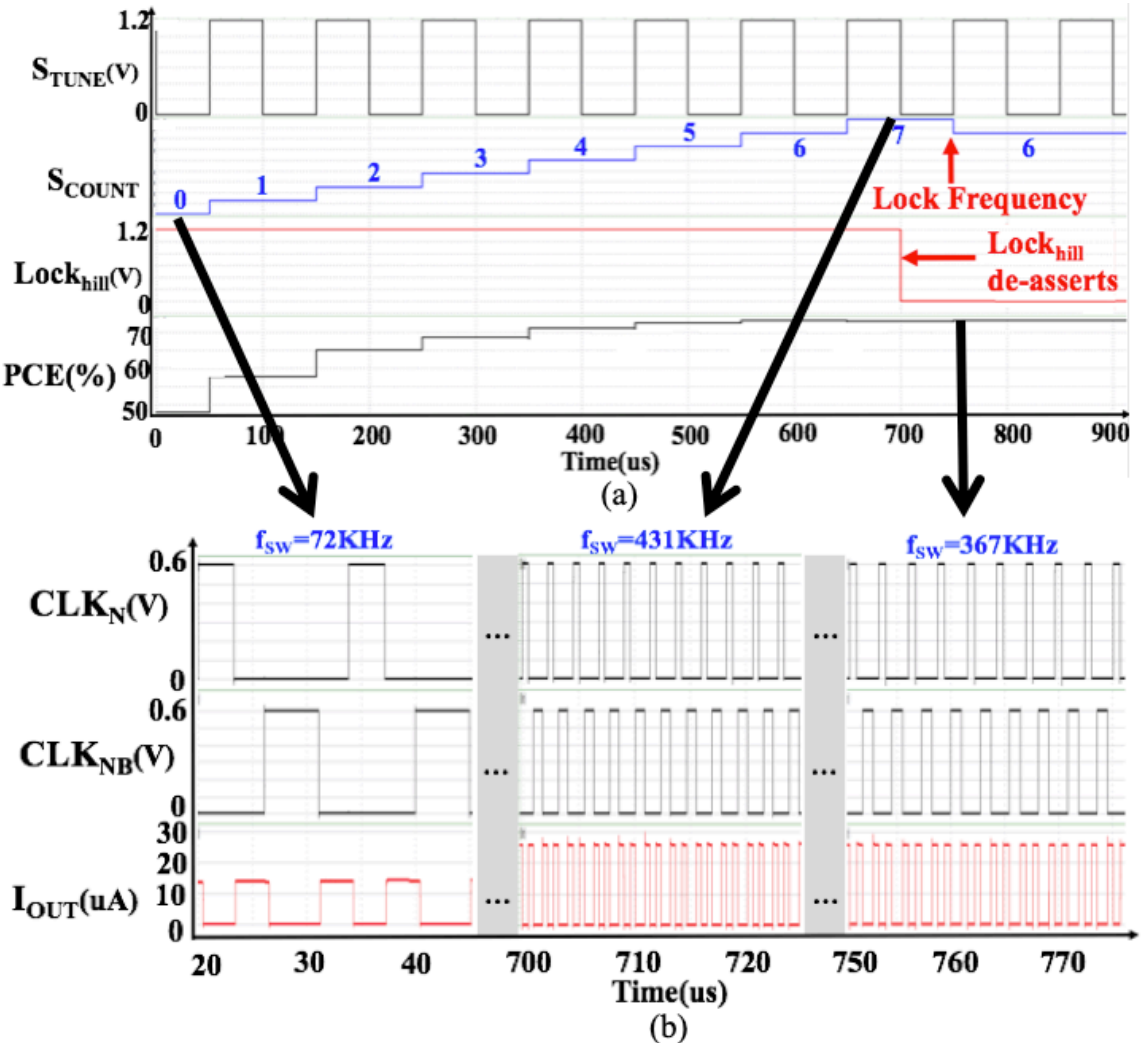

Figure 8.2 (a) Hill-climbing logic locking f_{SW} (b) Transient waveforms of clocks and output current at different f_{SW}

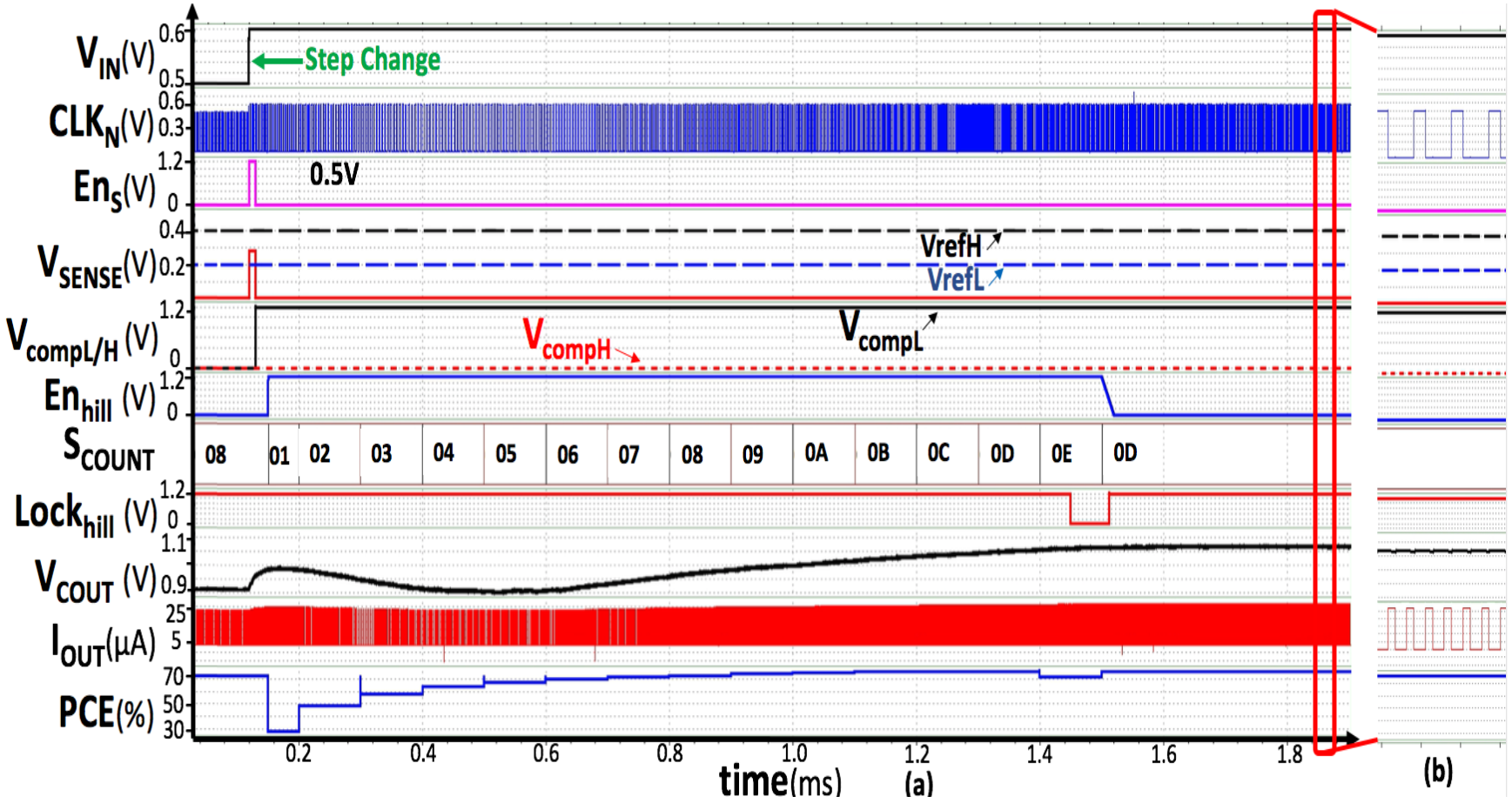

Figure 8.3 (a) Full system transient response to a step change in input voltage and power (b) Close-up on signals after system settles

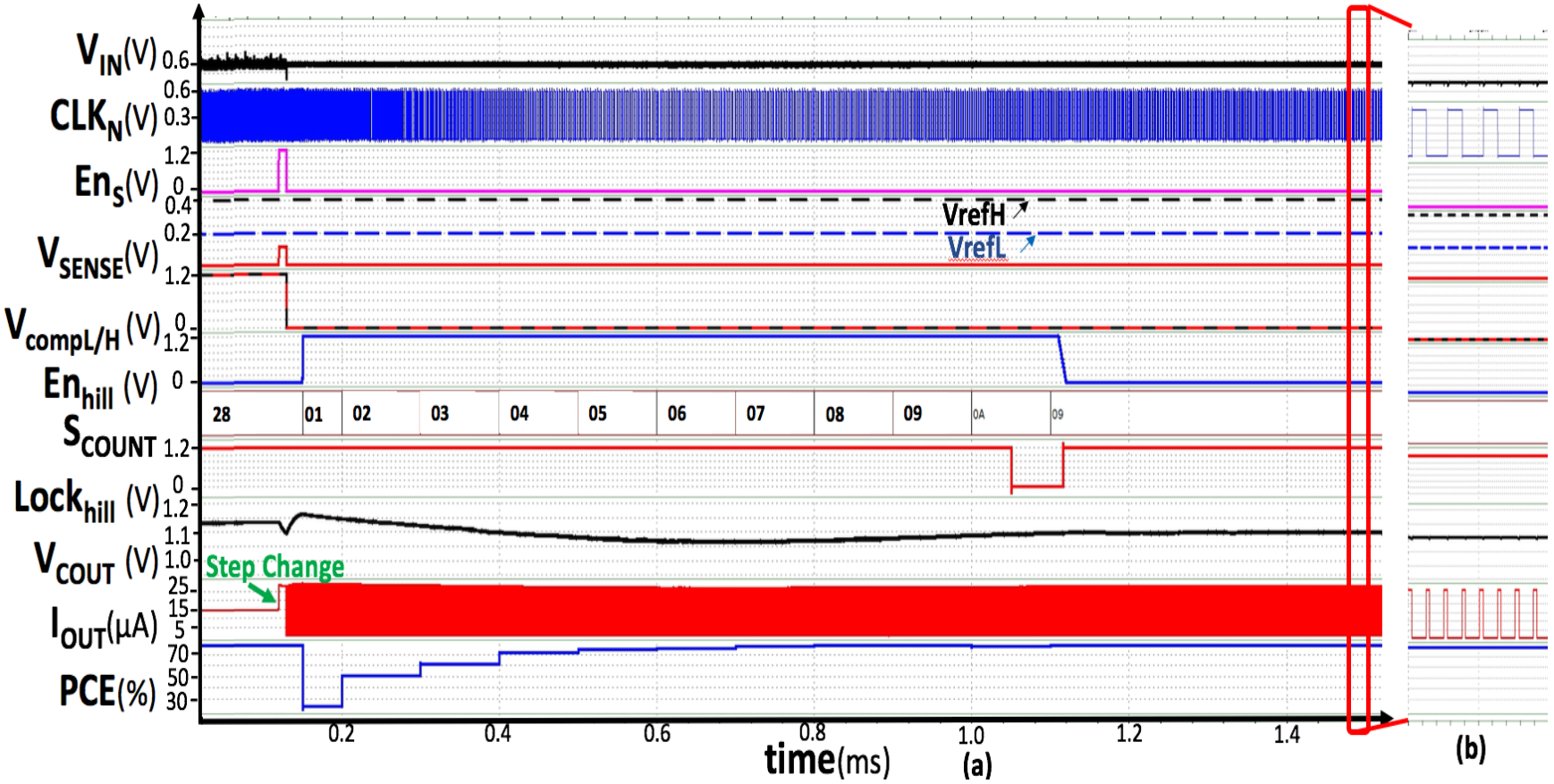

Figure 8.4 (a) Full system transient response to a step change in output current (b) Close-up on signals after system settles

8.4 System Layout and Post-Layout Simulation

Figure 8.5 (a) shows a floorplan of the system layout which occupies an area of 1.46mm^2, 91% of which is occupied by the flying capacitors and input/output capacitors. This area is suitable for WSN nodes and is comparable to other energy harvesters in recent literature, as will be shown in Chapter 10. A close-up of the voltage doubler circuit, excluding the flying and input/output capacitors, is shown in Figure 8.5 (b). The voltage doubler in Figure 7.4, which is the most important circuit for parasitic extraction, has been RC-extracted for post-layout simulations.

Figure 8.6 shows the pre-layout and post-layout PCE vs. the input power for the proposed system for 10% d_{NOL}. The peak efficiency is only reduced by 0.8% due to the additional parasitics, which would also affect the conventional continuous operation in the same fashion. Moreover, it can be seen that metal layout parasitics have no impact on the harvesting range that the discontinuous charging technique offers.

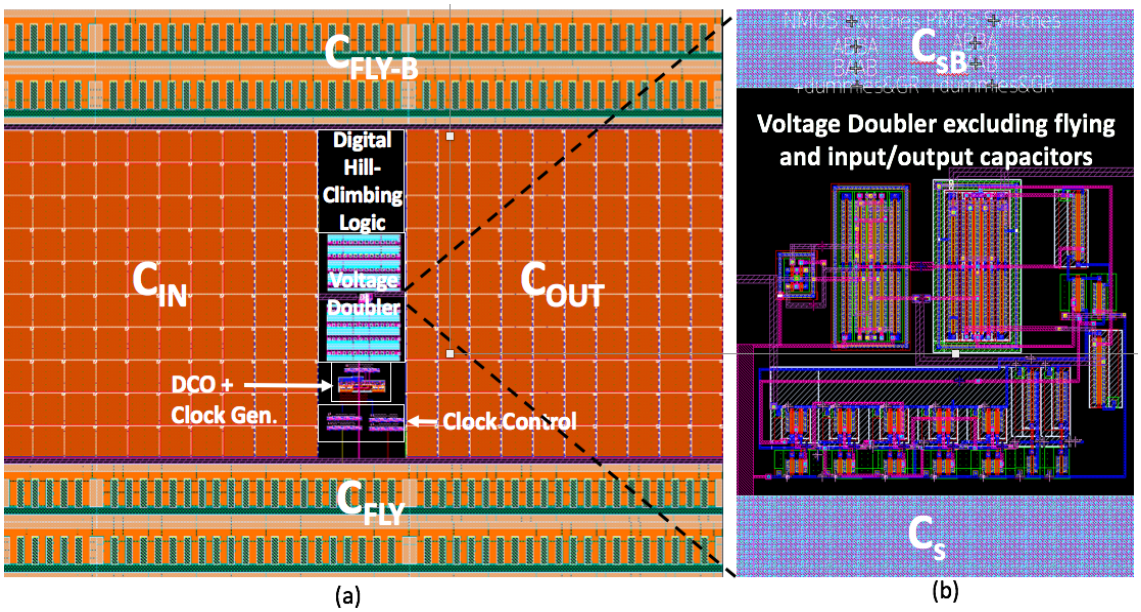

Figure 8.5 (a) System layout (b) Voltage doubler close-up excluding capacitors

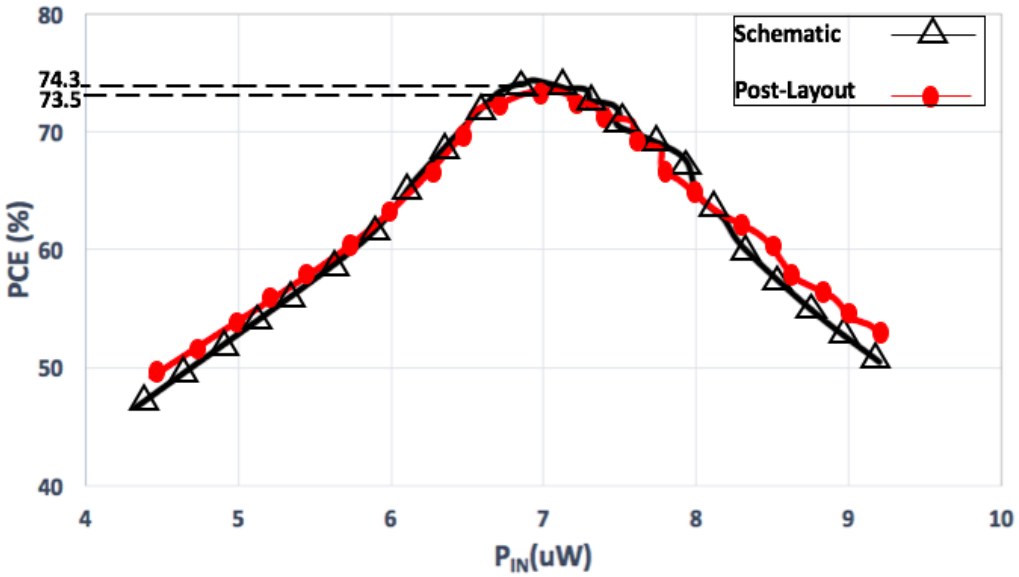

Figure 8.6 PCE vs. P_{IN} for pre-layout schematic and extracted post-layout voltage doubler when d_{NOL}=10%

8.5 Efficiency Characterization and PVT Simulations

Figure 8.7 plots the PCE vs. P_{IN} for the proposed system for a typical process at the nominal 0.6V input voltage and room temperature. In these simulations, the PCE plots are generated by measuring input power drawn from the source as the system sweeps through switching frequencies and non-overlap times. For the same load, it can be seen that the conventional operation, which is continuous, drops below 45% efficiency when P_{IN} is below 18.3µW. However, the proposed system switches to discontinuous operation for power levels lower than that and maintains efficiency above 45% for as low as 4µW. The switching points between different modes are calibrated by adjusting the comparator reference voltages, V_{REFH} and V_{REFL} in Figure 7.3 to maintain the efficiency above 45%. This extends the harvesting floor towards lower input power levels yielding a 1.5x harvesting range compared to conventional operation. This allows WSN nodes to operate in environments where lower power is available for harvesting. Peak efficiency of 73.3-

75.6% occurs at 7.3µW, 12.8µW, or 33.6µW depending on the operation mode. These values are suitable for the available P_{IN} from mm-scale solar cells commonly used in WSNs [2], [21], [85].

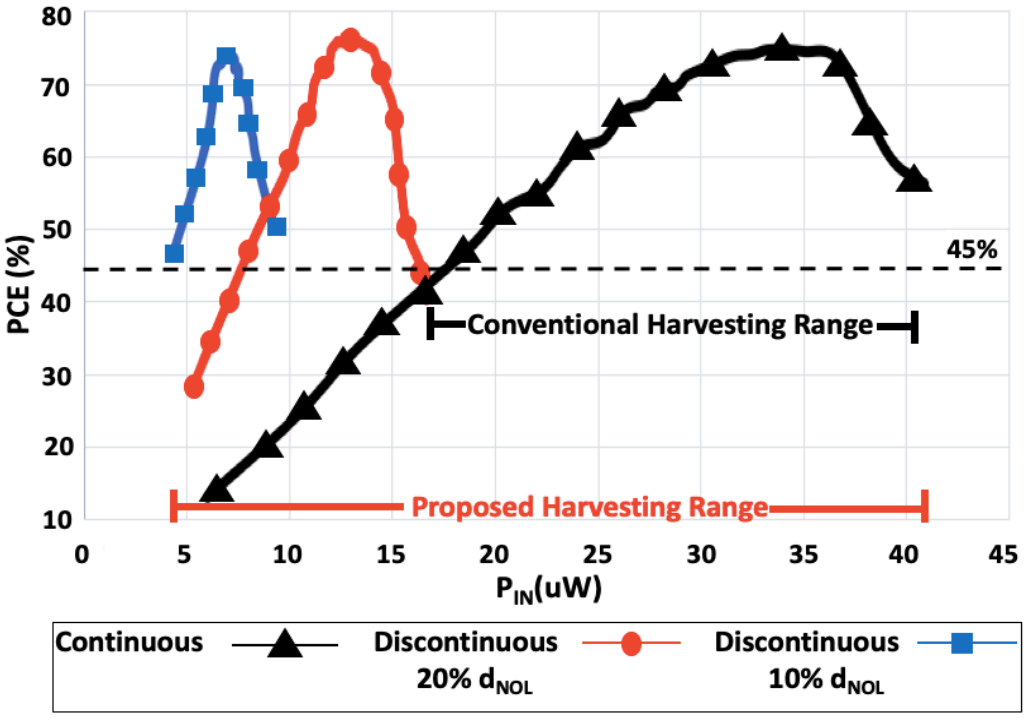

Figure 8.7 PCE vs. P_{IN} in typical corner (typical process, V_{IN}=0.6V,25°C)

Figure 8.8 and Figure 8.9 show PCE vs. P_{IN} for extreme PVT corners. The system temperature range in these simulations is intended for industrial applications because temperatures vary significantly and can reach extremes in IoT applications. As expected for these extreme PVT corners, the range of input power shifts due to variations in the devices. Moreover, for fast process and high temperatures, MOSFET threshold voltages are lower which results in higher current consumption and higher leakage. Hence, the worst-case peak PCE occurs at this corner and is 63%. Nonetheless, the harvesting range

is still extended by 1.4-1.5x compared to conventional operation. Table 8.1 summarizes the performance improvements this technique achieves across a number of extreme and skewed PVT corners.

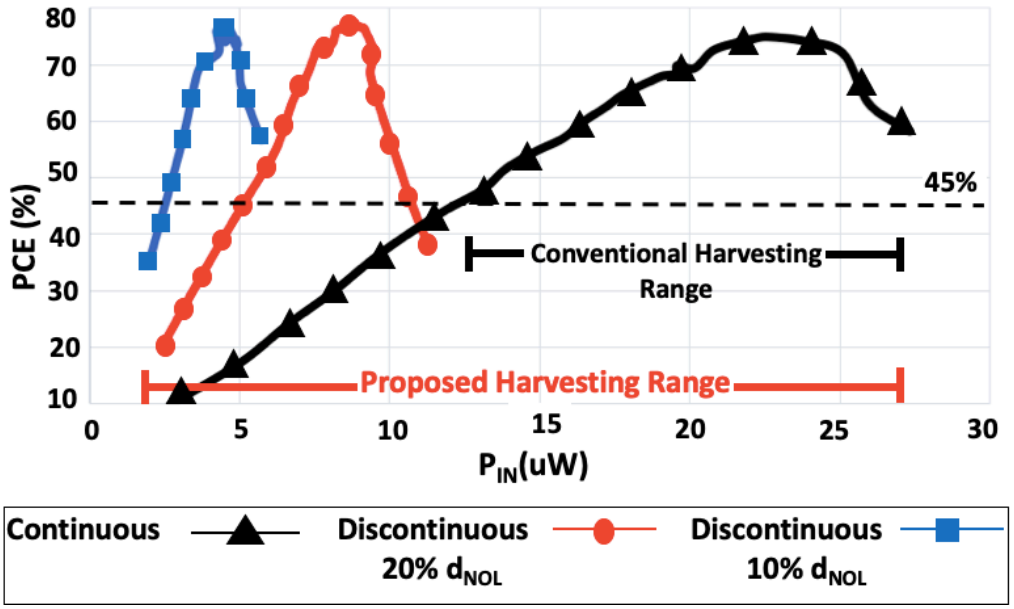

Figure 8.8 PCE vs. P_{IN} in slow NMOS and PMOS process (SS), V_{IN}=0.5V, -40°C

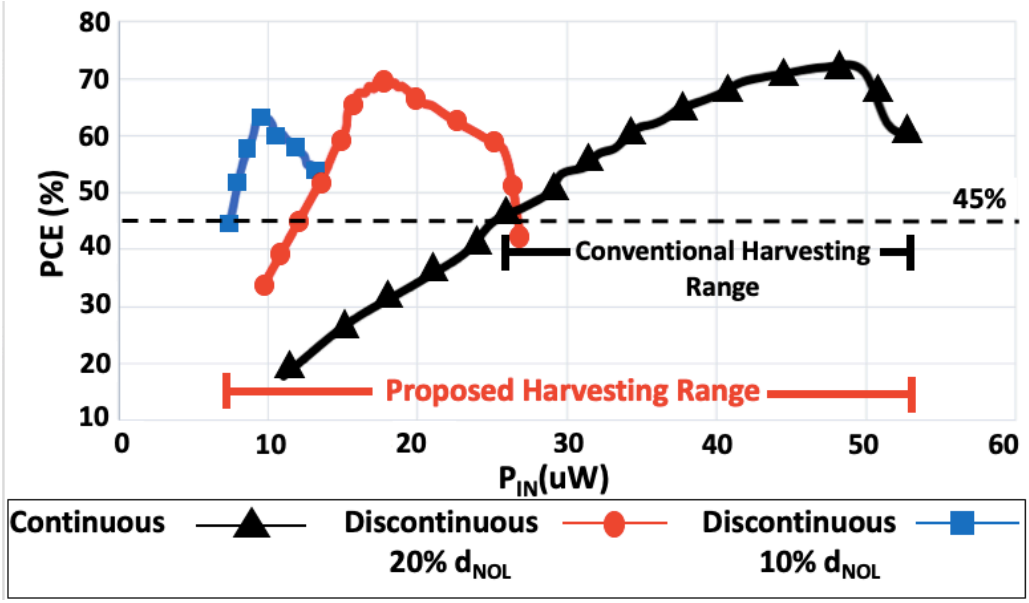

Figure 8.9 PCE vs. P_{IN} in fast NMOS and PMOS process (FF), V_{IN}=0.7V, 85°C.

Table 8.1 Performance summary across PVT corners

PVT Corner	Proposed Harvesting Floor (µW)	Conventional Harvesting Floor(µW)	Harvesting Range Improvement
TT, SS, FF, SF, FS. V_{IN}=0.5V. T= -40°C.	3-3.3	10.7-11.54	1.38x-1.45x
TT, SS, FF. V_{IN}=0.7V. T= -40°C.	8.21-9.38	22.1-26.8	1.25x-1.4x
TT, SS, FF. V_{IN}=0.5V. T= 85°C.	3.2-3.3,3.2	11.5-12.2	1.66x-1.79x
TT, SS, FF, SF, FS. V_{IN}=0.7V. T= 85°C.	7.6-8.6	23.1-25.3	1.5x-1.61x

To test the robustness of the system and characterize its efficiency, simulations are performed for various output currents and input voltages. Figure 8.10 shows the PCE vs. $I_{OUT\text{-}avg}$ provided to energy storage for different input voltages. For low output currents, PCE degrades due to the overhead from always-on circuits such as the DCO. For high output currents, P_{ROUT} and P_{PAR} losses, discussed in Section 3.3, increase and result in decreasing the PCE. The system achieves PCE above 45% for output currents as low as 1.5µA and as high as 80µA to 240µA depending on the input voltage.

Figure 8.11 shows the PCE vs. V_{IN} for different average output currents. For input voltages above 0.45V, the system is able to achieve above 70% efficiency. However, below 0.45V, the input voltage approaches the V_{th} of the MOSFET switches and the PCE begins to degrade.

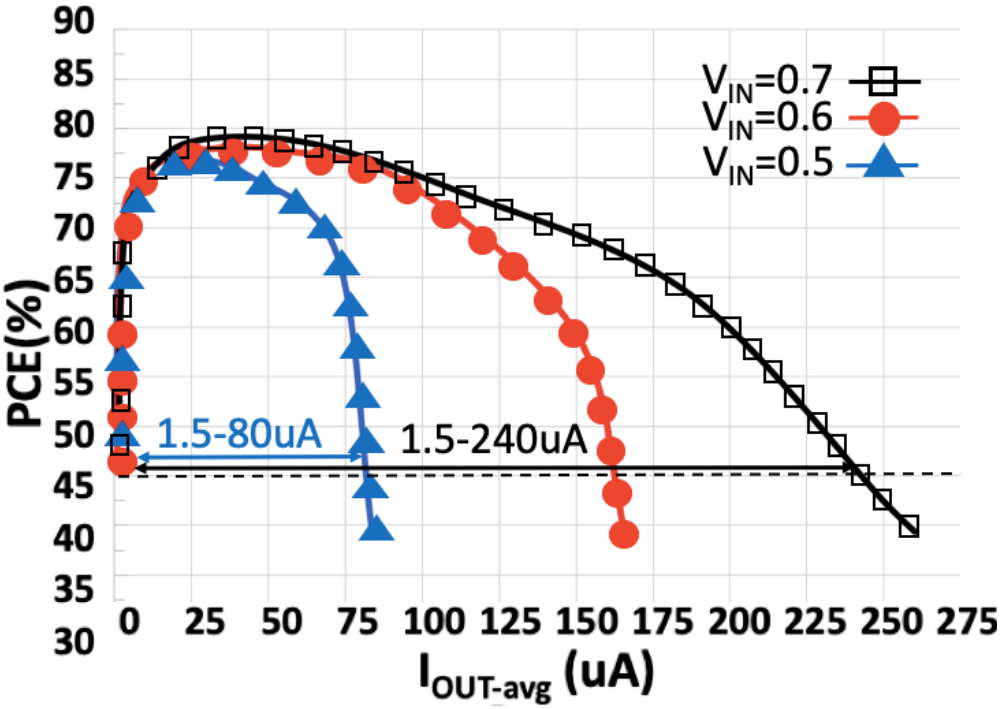

Figure 8.10 PCE vs. average output current for different input voltages

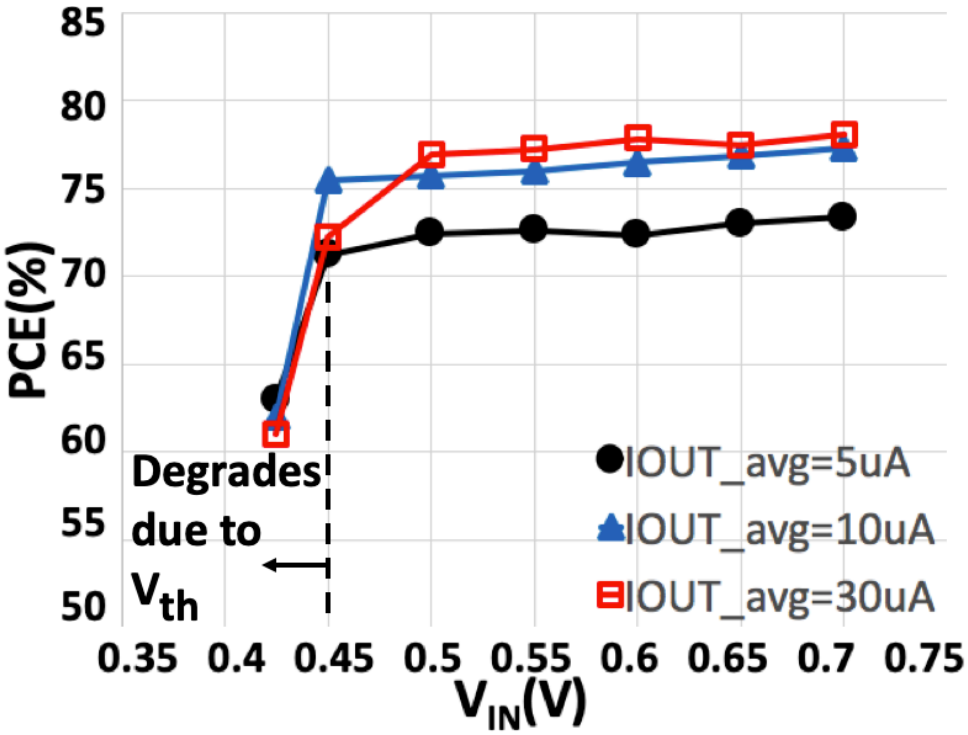

Figure 8.11 PCE vs. input voltage for different output currents

To verify the system's ability to double V_{IN} and deliver it to energy storage, simulations are performed to measure the VCE vs. V_{IN} for different average output currents, as shown in Figure 8.12. Similar to PCE, VCE also degrades below 0.45V due to V_{th}. Above 0.45V input voltage, the system achieves VCE above 85%. It can be seen that VCE can vary by a few percent when varying the input. This is because the DCO control has discrete values that approach the ideal frequency for some V_{IN}/I_{OUT} combinations but are slightly further away for other values. This VCE measurement is for the raw and unregulated V_{OUT} delivered to energy storage. After that, the output voltage of the energy storage must be regulated before powering a WSN node. The regulator is not included in this work as shown in Figure 1.2.

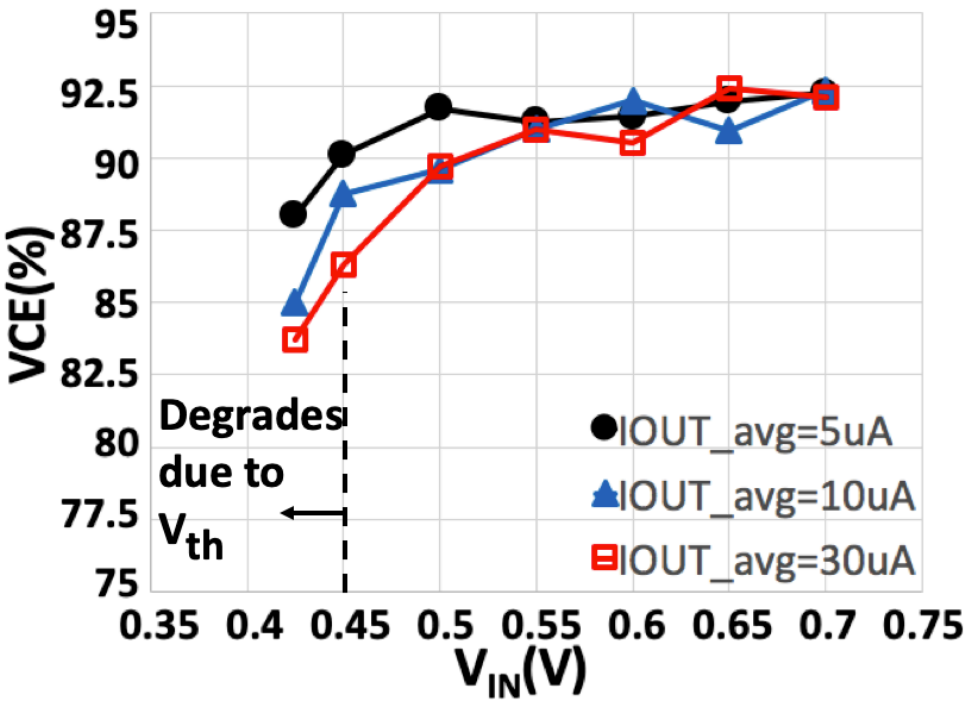

Figure 8.12 VCE vs. input voltage for different output currents

8.6 Block Power Consumption

Table 8.2 shows the power consumption by block when the system is locked at peak PCE with 10% d_{NOL}. The blocks are organized into always-on circuits and circuits that are only enabled periodically for sensing and remain in standby otherwise. The clock control block consumes 1.25µW when enabled and 15nW when in standby. This block is only enabled once every minute for 10us and remains in standby otherwise. Therefore, the average power loss of the input power sensing approaches the standby power. Compared to the PCE improvement these circuits provide, this power loss is negligible. The hill-climbing logic consumes 60µW average power when enabled due to the switching power of digital CMOS circuits and consumes 17nW in standby. Since the operation is performed in less than 1.5ms and is also only enabled once a minute, the average power loss approaches the standby power.

Table 8.2 Average power consumption by block for d_{NOL}=10% when locked at peak PCE of 74.3%. P_{IN}=7.3µW, P_{OUT}=5.45µW.

Always-on circuits		**Circuits only on during sensing**	
Voltage Doubler	0.96µW	Input Power Sensing and Clock d_{NOL} Control	15nW
DCO	0.71µW	Hill-Climbing f_{SW} control	17nW
Clock Generator	0.18µW		

In conclusion, the simulations demonstrate that the proposed technique functions as intended and improves the harvesting range by 1.25-1.79x across PVT corners. Moreover, the system is robust and can operate successfully with a range of input voltages and output currents. Finally, extracted post-layout simulations show minimal impact on peak PCE and harvesting range.

CHAPTER 9

APPLICATION ON WIRELESS SENSOR NETWORKS

Many WSNs define their communication protocol using the IEEE 802.15.4 standard for low data-rate, low-power, and low-complexity short-range radio frequency transmissions [36]. One example is the GreenNet protocol [21], [22]. In this chapter, the proposed technique is applied to the GreenNet-based WSN implementation described in [22] for industrial and wearable applications in dark indoor environments, to show how it enables energy autonomy in a scenario where that would not be possible otherwise.

As discussed in detail in Section 2.2, GreenNet utilizes the IEEE 802.15.4 energy-saving beacon mode, where nodes are synchronized with periodic beacons and can only wake up at specific instances to communicate [21]. The beacon mode settings are defined using the beacon order parameter (BO), which configures the interval between beacon transmissions (BI). The node remains in sleep mode between intervals. The BO and corresponding BI values are shown in detail in Table 2.3 and relevant examples are shown in Table 9.1. In Table 2.2, the power consumption of each operation, such as sensor data acquisition, was detailed. A full cycle requires 569.69μJ, where the highest current consumption is 11.56mA for radio transmission. During sleep, the node consumes 3.58μA. Thus, the average current required for each BO is shown in Table 9.1, where the higher the BO and BI values, the lower the power required by this GreenNet-based WSN.

Table 9.1 Current consumption for different BO parameter values of IEEE 802.15.4-compatible GreenNet WSN node [22]

BO	0	8	10	12	14
BI (s)	0.02	3.93	15.73	62.91	251.66
Average Current (μA)	12363.06	51.83	15.64	6.6	4.33

In harsh environments, the WSN would operate at the lowest power setting of BO=14 to save power. However, to meet the specifications at this setting, while also achieving energy autonomy, energy harvesting is essential to deliver a minimum current of 4.33μA to replenish energy storage. Assuming the input voltage from the solar cell is 0.6V, VCE is 91% at this current value as shown in Figure 8.12 (c). Hence, using (3.19), V_{OUT} is 1.1V. This corresponds to P_{OUT} of 4.76μW. Next, using (3.16) and Figure 8.7, the required P_{IN} for the proposed system is compared to conventional operation. A conventional system would require 13.5μW of P_{IN} harvested from the energy source in order to deliver 4.76μW to energy storage because its PCE is 33% at that power level. If P_{IN} is consistently below 13.5μW, it will not be possible to achieve energy-autonomous operation for this WSN and meet specifications because energy storage will eventually be depleted. However, for these power levels, the proposed system senses P_{IN} and switches to discontinuous operation mode with 10% d_{NOL}. As seen in Figure 8.7, this improves PCE to 70% requiring only 6.43μW of P_{IN} to be harvested from the energy source in order to deliver 4.76μW to energy storage. Therefore, the proposed technique allows this WSN node to meet the GreenNet protocol specifications and achieve energy autonomy when deployed in harsher environments where the available P_{IN} is up to 49% lower than what is required for conventional operation. Note that for applications where high P_{IN} is consistently available, the proposed technique performs similar to conventional operation.

Applying the proposed technique to the GreenNet-based node facilitates energy-autonomous operation for the low-power WSNs. Similar to what was demonstrated for the GreenNet protocol, this technique can be extended to WSNs based on other communications standards/protocols to facilitate energy autonomy in harsher environments.

CHAPTER 10

PERFORMANCE COMPARISON

In this chapter, the performance of the proposed technique is summarized and compared to other energy harvesting literature, as shown in Table 10.1.

In [20] and [80], a boost converter is used to achieve good efficiency for a low input voltage and a large range of P_{IN}. However, this topology relies on a large, off-chip inductor that significantly increases the system size and may not be suitable for many size-constrained WSNs. The remaining references represent key MPPT innovations for SC converters that focus on reducing power consumption and achieving high PCE at lower power levels appropriate for IoT energy harvesting applications. Hence, they serve as a benchmark to evaluate the performance of this technique. A major innovation in this work compared to these benchmark references is that P_{IN} is sensed and the PCE is adaptively optimized to achieve the best PCE performance at available power levels. This is key for WSN deployments in harsh environments where ambient power levels vary considerably.

In [47], a charge recycling technique is proposed to reduce parasitic bottom plate power losses by utilizing the clock non-overlap intervals to transfer and maintain charge between the different parasitic capacitors instead of discharging these capacitors. This reduces power losses by 27% and improves overall efficiency by 12.7%. However, no MPPT is implemented and the efficiency drops below 40% at higher input power levels that occur due to varying ambient power in IoT applications.

Reference [27] contains a cross-coupled CP converter similar to the converter utilized in this work, but operated in conventional continuous operation. The system is designed for low voltage energy harvesting, but the peak efficiencies occur at much higher input power levels that may not be available when WSN nodes are deployed in harsh environments. Reference [9] introduces an MPPT technique that relies on an inherent negative feedback loop between the CP and the oscillator to control f_{SW}. This reduces MPPT overhead power consumption by eliminating several MPPT sensors and circuit blocks. It contains CP-based converter and oscillator blocks similar to those utilized in this work. However, the MPPT technique is one dimensional and the converter is operated in conventional continuous operation. Therefore, the peak efficiencies occur at much higher input power levels that may not be available when WSN nodes are deployed in harsh environments.

In [75], MPPT power consumption is reduced by introducing capacitor value modulation instead of conventional frequency tuning. The hill-climbing MPPT adjusts the values of the converter's flying capacitors through a capacitor array to adjust the impedance and achieve the maximum power point. However, the input voltage ranges it is designed for is rather high compared to recent state-of-the-art input voltages. Moreover, the MPPT scheme is one dimensional and additional capacitance occupies more of the on-chip area. In [23], a discontinuous harvesting system is introduced that enables operation at ultra-low power levels by completely shutting the harvester down until enough energy is harvested, which reduces leakage and converter losses. This design achieves good efficiency at low power levels. However, operation at higher power levels, which may occur due to varying

ambient power, is not reported. Moreover, due to the recurring shutdowns, frequent start-up losses occur and are accounted for.

In [8], a 2D MPPT is introduced that sweeps f_{SW} and the conversion ratio of the converter to accommodate a large input voltage range. The peak efficiency occurs at P_{IN} larger than 35µW for comparable input voltages. However, PCE continues to decrease as P_{IN} drops to lower values and the system does not sense P_{IN} and adjust its PCE accordingly and continues to decrease as P_{IN} drops. In [48], a 2D MPPT scheme is proposed that modifies the charge pump topology and the f_{SW} to accommodate a wider harvesting range. The circuit starts up with as low as 2.38nW and achieves above 40% efficiency for input powers larger than 0.5µW as reported in Table 10.1. However, the MPPT scheme is open-loop and does not monitor the output power or voltage. Moreover, it monitors input voltage levels but does not directly monitor input current.

Finally, in all the systems in Table 10.1, the designs are not input-power aware and do not optimize their performance based on sensing the harvested input power levels. Additionally, the peak efficiencies occur at a fixed, specific input power and cannot be tuned as shown in the proposed technique. Hence, in this work, the peak PCE is reported at three possible P_{IN} values as opposed to one peak PCE in other works.

Table 10.1 Performance summary and comparison with recent literature

Paper/ Metric	Technology	Topology	MPPT	Peak Efficiency	Input Voltage Range	P_{IN} range with PCE>40%	Area	Output Regulation
IoTJ, 2018 [20]	0.18um	Boost Converter	No	76.4% @ 229µW	0.1V	5µW-1.33mW	Chip: 1.3mm^2 10uH ind. [a]: 6.2mmx6.2mm	Yes
TVLSI, 2019 [80]*	0.18um	Boost Converter	1D: Open-circuit voltage based	88.2% @ 1.8µW	70-525mV[b]	>300nW[c]	Chip: 0.18mm^2 820uH ind.[d]: 6mmx6mm	Yes, using buck converter
TVLSI, 2019 [47]*	0.5um	Switched Capacitor	No	47.5% @ 3.29µW[e]	0.3-0.6V	1.8-6.6µW[e]	4mm^2	Yes, using adaptive gain control
JSSC, 2016 [27]	0.18um	Switched Capacitor	1D: Sweeps f_{SW}	75.8% @ 396µW 49.1% @ 114µW	0.35-0.6V	Not reported	1.62mm x 1.08mm	No
IoTJ, 2017 [9] *	0.18um	Switched Capacitor	1D: Feedback loop for f_{SW}	70% @ 1.1mW[e]	0.3-0.7V	Not reported	0.658mm x 0.736mm	Yes, using Linear regulator
JSSC, 2015 [75]	0.18um	Switched Capacitor	1D: Cap. value modulation	86.4% @ 13.9µW[e]	1.1-1.5V	4.5-27µW[e,f]	1.5mm x 1.55mm	Yes, but 150mV ripple
JSSC, 2017 [23]	0.18um	Switched Capacitor	1D: Operates near MPP. Traded off to achieve higher PCE	50% @ 8nW	0.25-0.65V	113pW-1.5µW	1.7mm x 1.6mm	No

Paper/ Metric	Technology	Topology	MPPT	Peak Efficiency	Input Voltage Range	P_{IN} range with PCE>40%	Area	Output Regulation
JSSC, 2016 [8]	0.18um	Switched Capacitor	2D: Sweeps f_{SW} and conversion ratio	79% @P_{IN}>35µW [g]	0.45-3V	~2-50µW	2mmx2mm	Yes, but ripple > 100mV
TPE, 2019 [48]	0.18um	Switched Capacitor	2D: Sweeps f_{SW} and modifies charge pump topology	57% @ 3.63µW	0.17-0.5V	~0.5-10µW	0.575mm^2	No
This Work *	90nm	Switched Capacitor	P_{IN} sensing and 2D: Sweeps f_{SW} and clock non-overlap	73.5% @ 7.3µW or 75.6% @ 12.8µW or 73.3% @ 33.6µW	0.5-0.7V	4-41µW	1.05mm x 1.38mm	No

[a] Inductor area not reported. Typical 10uH surface mount Inductor size shown from reference [86].

[b] Maximum input voltage for the utilized PV cell. [c] PCE not reported for P_{IN} >10µW when source resistance is 10KΩ.

[d] Inductor area based on commercial inductor used in [80]. [e] Calculated from efficiency and P_{OUT} results.

[f] PCE not reported for P_{IN} >27µW. [g] For the 0.6V thermoelectric generator input case from Fig. 21-b in [8].

[*] Post-Layout Simulation Results

CHAPTER 11

CONCLUSIONS

This chapter concludes this work and summarizes the contributions it presents. Moreover, future research directions are discussed.

11.1 Conclusions

This dissertation introduces a two-dimensional maximum efficiency tracking technique for switched-capacitor energy harvesters. A discontinuous charging technique is proposed to supply current to energy storage only during clock non-overlap time. The clock non-overlap time is then utilized as a new control variable to minimize converter losses according to the sensed input power. For lower input power levels, clock non-overlap time is reduced in order to reduce the average output current and maintain high power conversion efficiency. The system also incorporates conventional switching frequency control. Unlike previous works, the proposed system is input power-aware and is capable of adaptively tuning the peak efficiency according to input power levels it senses at the input. As seen in Table 10.1, a peak power conversion efficiency of 73.3-75.6% can be tuned to occur at 7.3μW, 12.8μW, or 33.6μW input power for discontinuous charging with 10% d_{NOL}, 20% d_{NOL}, and continuous operation, respectively. Therefore, the proposed system achieves an input power harvesting range of 4-41μW with PCE of at least 45%. When compared to conventional, continuous charging with one-dimensional MPPT, the

harvesting floor is extended towards lower input power levels which extends the harvesting range by 1.25-1.79x across PVT corners.

The technique is applied to a WSN implementation utilizing the IEEE 802.15.4-compatible GreenNet communication protocol for industrial and wearable applications. This allows the WSN node to meet specifications and achieve energy autonomy when deployed in harsher environments where available P_{IN} levels are up to 49% lower than what is required for conventional operation.

11.2 Future Work

As IoT applications increase and more WSN nodes are placed in harsh environments with very low power available for harvesting, it continues to be critical to improve both the input voltage range and input power harvesting range with high PCE. One area of future work for this dissertation can be achieving a wider range of input voltage. This can be done by incorporating an SC converter with a variable conversion ratio that can be adjusted based on the input voltage to accommodate a wider range of input voltages. The conversion ratio was previously used as one dimension of MPPT control in [8]. Therefore, this work can be expanded into a three-dimensional tracking technique by adding conversion ratio control in addition to the clock non-overlap and switching frequency already presented in this work.

Another direction of future work that can be explored is further reducing the switching frequency in order to reduce parasitics power losses as well as DCO power consumption. This would result in increasing the harvesting range as efficient harvesting from lower input powers becomes possible. For example, this may be achievable by adopting capacitor value modulation similar to [75] instead of sweeping the switching

frequency. However, careful consideration is needed for the trade-off with the larger die area and parasitics due to the potentially larger capacitors needed for this modulation.

Finally, similar to the IEEE 802.15.4-compatible WSN application discussed in Chapter 10, the proposed technique can be applied to WSN nodes utilizing other communication standards and protocols such as BLE, which also enable lower power applications. This can facilitate energy autonomy by improving the power conversion efficiency when these WSN nodes are deployed in ultra-low power environments.

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APPENDIX A

CIRCUIT SCHEMATICS

This Appendix includes the transistor-level schematics for the circuits that were discussed in Chapter 7. The schematics are exported from Synopsys Custom Compiler and include all circuits and sub-circuits in this system as well as the full system testbench, which is used for full system transient simulations. Standard cells such as flip-flops and inverters are not included.

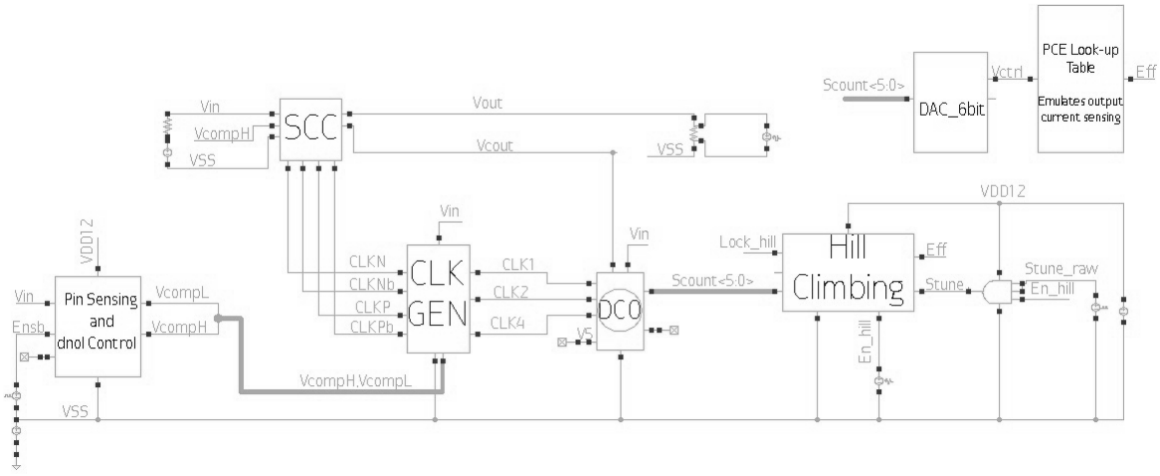

Figure A- 1 Full system testbench used for transient simulations

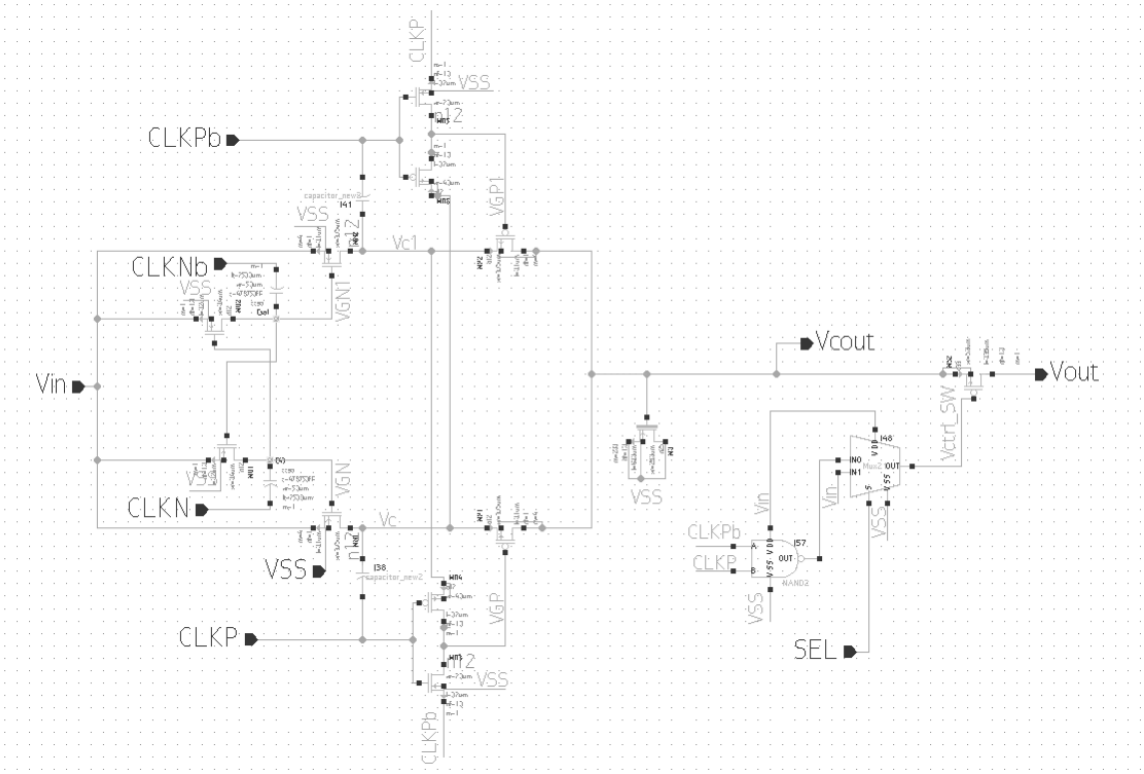

Figure A- 2 Schematic for voltage doubler with continuous/discontinuous mode selection

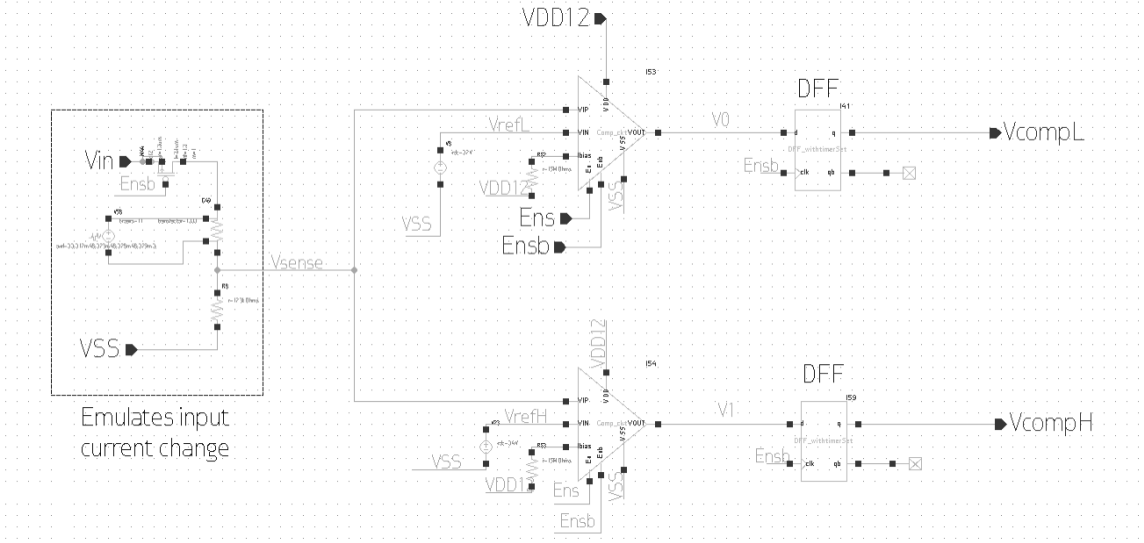

Figure A- 3 Schematic for input power sensing and clock non-overlap control

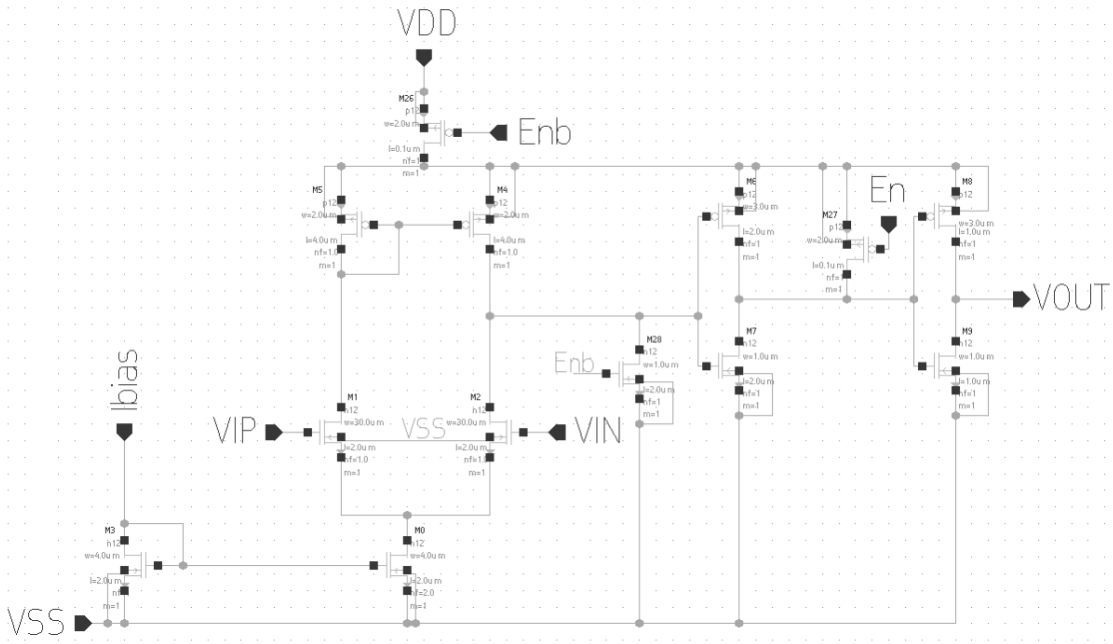

Figure A- 4 Schematic for input power sensing comparator

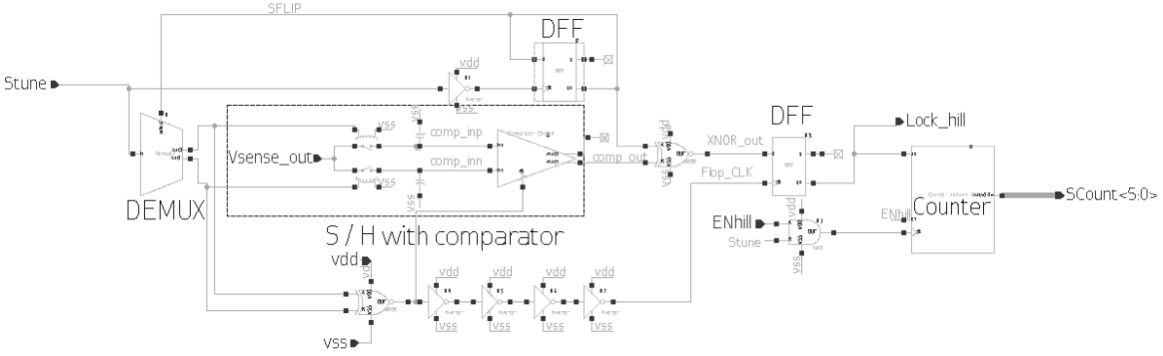

Figure A- 5 Schematic for digital hill-climbing used for switching frequency tuning

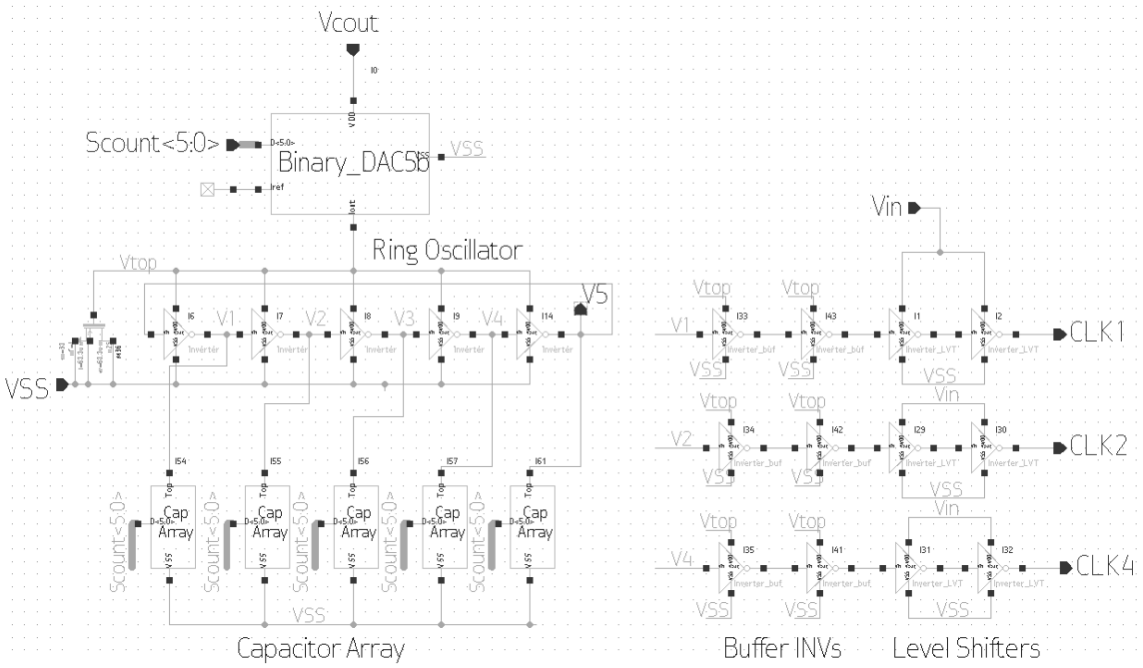

Figure A- 6 Schematic for digitally-controlled oscillator

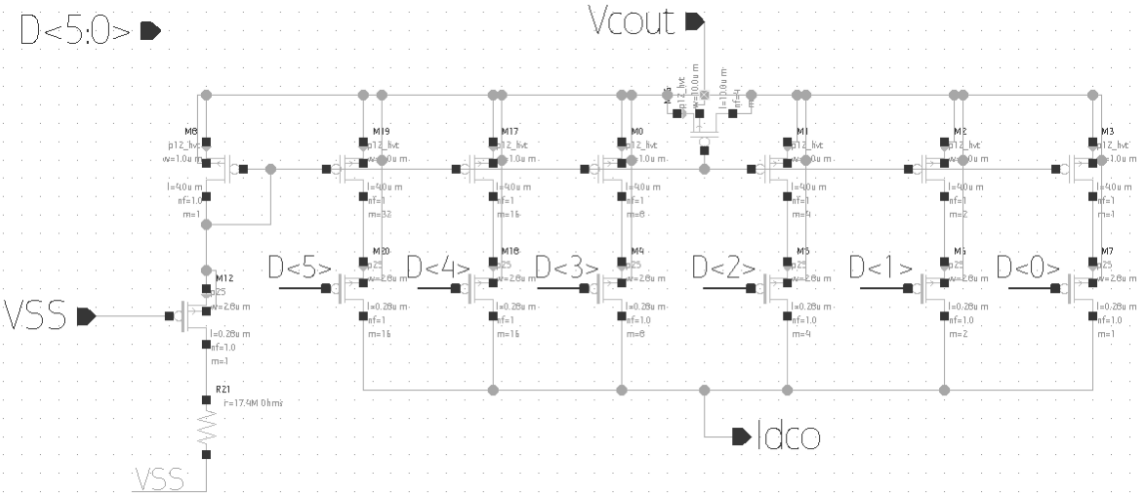

Figure A- 7 Schematic for 6-bit current digital-to-analog converter

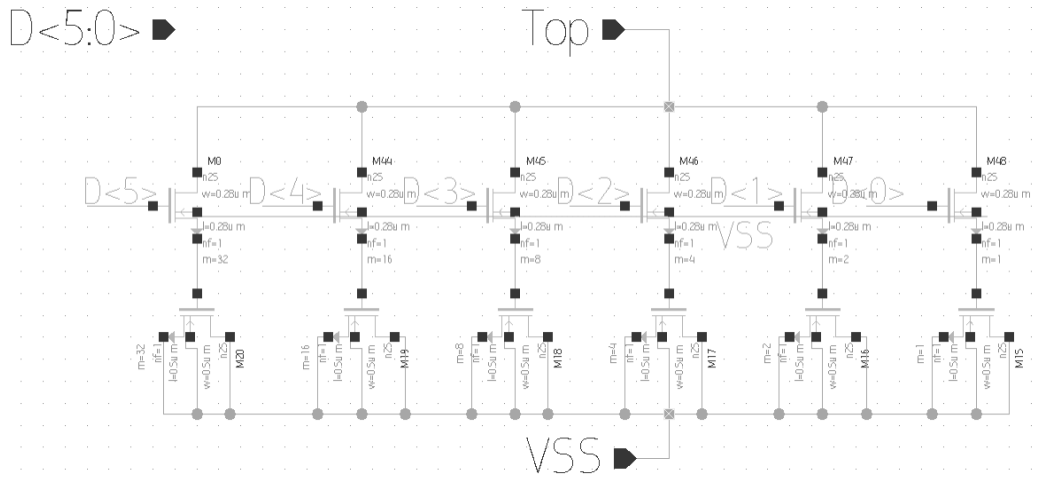

Figure A- 8 Schematic for 6-bit capacitor array

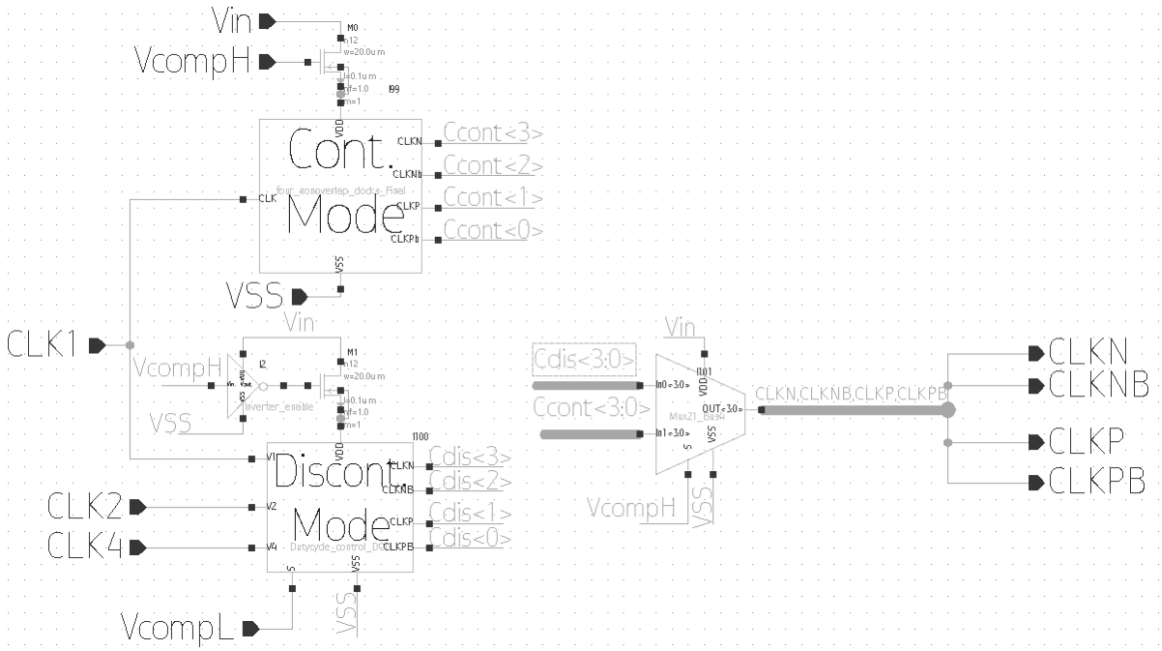

Figure A- 9 Top-Level schematic for 4-phase clock generator and MUX

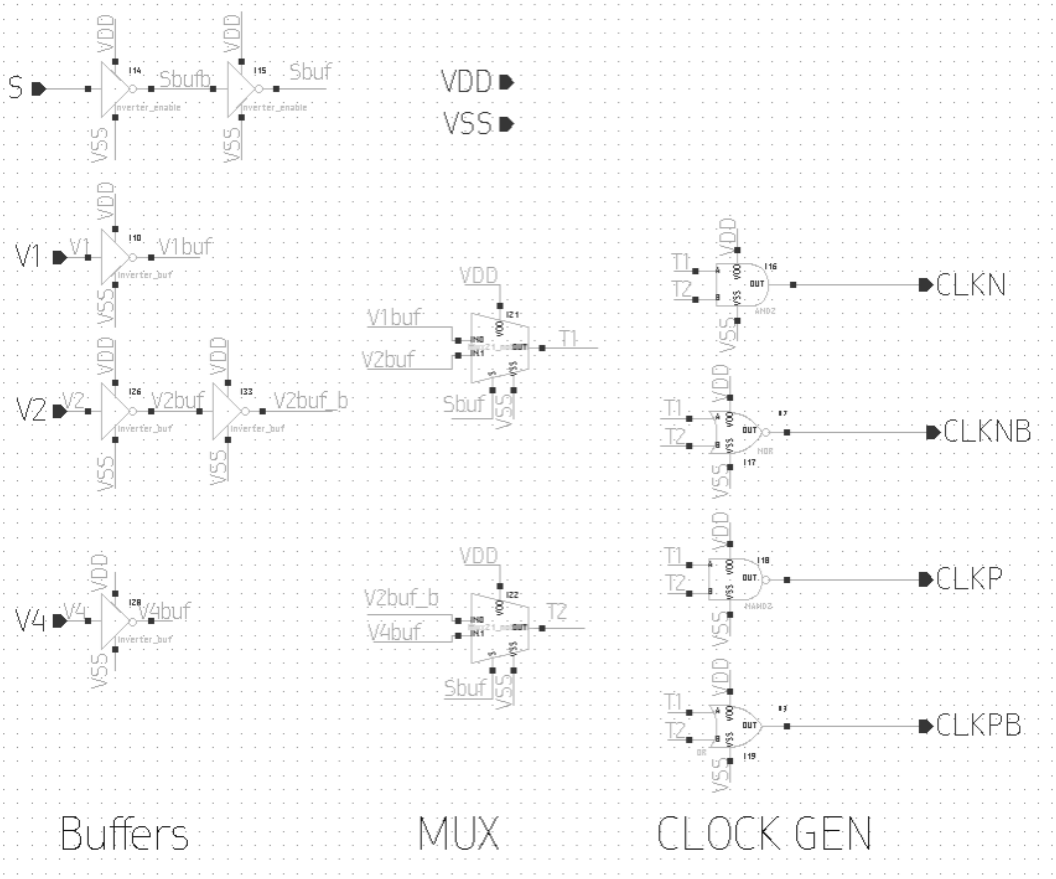

Figure A- 10 Schematic for 4-phase clock generation in discontinuous mode

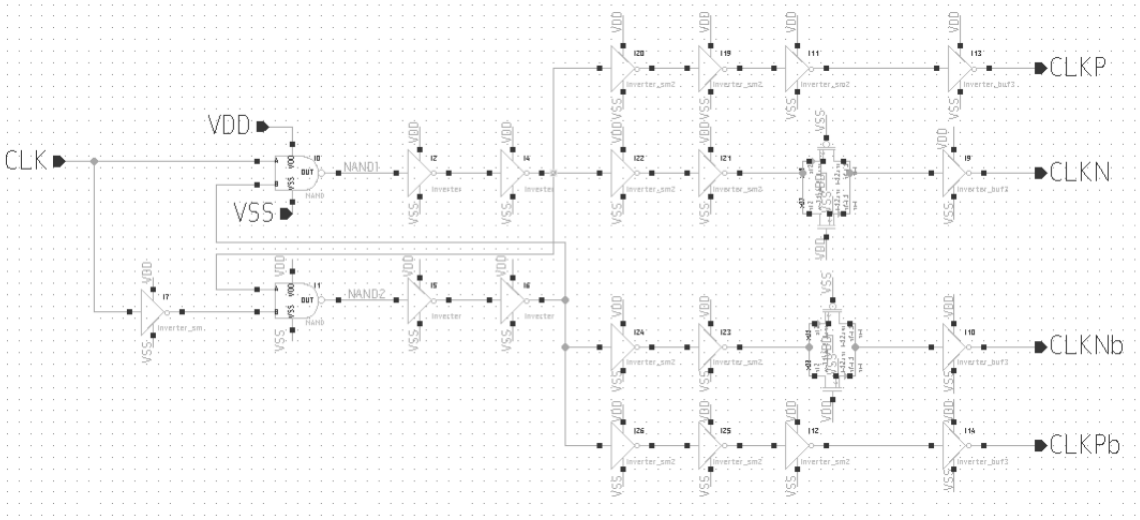

Figure A- 11 Schematic for 4-phase clock generation in continuous mode

APPENDIX B

MATLAB MODEL

This appendix includes the script used for the Matlab equations model and the comparison between circuit and Matlab models discussed in Chapter 6. Moreover, it includes the script used to generate the contour plot in Section 5.2.

B-1. Comparison Between Matlab and Circuit Models

```
%In this code the discontinuous charging technique is modeled in Matlab via equations. Matlab does the
%calculations and generates results for power losses and PCE. The results from circuit model simulations
%in Synopsys Custom Compiler (with HSPICE simulator) are imported as .cvs data. Following that, the
%results are compared between the two models.
```

Define Constants

```
Vin=0.6;          % Input Voltage
Rload=40e3;       % Load Resistance
k=0;              % counter
j=0;              % counter
Rsw=45;           % MOSFET switch Resistance (for each switch)
Cgg=360e-15;      % Total switch gate caps
Cfly=160e-12;     % Flying cap --> accounts for two 80pF caps
x=0.1;            % bottom plate cap percentage of Cfly
fignum=0;         % Figure counter
```

Define Variables

```
fsw=50e3:10e3:2e6;      % Switching frequency variable for discontinuous operation
dnol=0.05:0.05:0.15;    % Clock Non-Overlap time variable
```

Initialize Matrices

```
Vout=zeros(length(dnol),length(fsw));
Ipk=zeros(length(dnol),length(fsw));
Iout=zeros(length(dnol),length(fsw));
Pout=zeros(length(dnol),length(fsw));
Prout=zeros(length(dnol),length(fsw));
Ploss=zeros(length(dnol),length(fsw));
Pin=zeros(length(dnol),length(fsw));
PCE=zeros(length(dnol),length(fsw));
```

Import circuit/SPICE Simulation Data for discontinuous with 5% Non-overlap

```
[fsw_sim,Pout_sim1,Pin_sim1,PCE_sim1,VCE_sim1,Ploss_total_sim1,Psw_sim1,Pcbot_sim1,Prout_sim1]
= import_powerCSV...
   ('CP_discon_nocomparator_power_5percent.csv');      % Import function

% Convert the measured column vectors to single row vectors.
dim = size(fsw_sim);   rows = 1;     columns = dim(1,1);
fsw_sim = reshape(fsw_sim, rows, dim(1,1));
Prout_sim1   = reshape(Prout_sim1 , rows, dim(1,1));
Psw_sim1   = reshape(Psw_sim1 , rows, dim(1,1));
Pcbot_sim1   = reshape(Pcbot_sim1 , rows, dim(1,1));
Pout_sim1   = reshape(Pout_sim1 , rows, dim(1,1));
Ploss_total_sim1   = reshape(Ploss_total_sim1 , rows, dim(1,1));
Pin_sim1   = reshape(Pin_sim1 , rows, dim(1,1));
PCE_sim1   = reshape(PCE_sim1 , rows, dim(1,1));
VCE_sim1   = reshape(VCE_sim1 , rows, dim(1,1));
[PCE1_max,Fsim1]=max(PCE_sim1);
```

Import circuit/SPICE Simulation Data for discontinuous with 10% Non-overlap

```
[~,Pout_sim2,Pin_sim2,PCE_sim2,VCE_sim2,Ploss_total_sim2,Psw_sim2,Pcbot_sim2,Prout_sim2] =
import_powerCSV...
   ('CP_discon_nocomparator_power_10percent.csv');     %Import function

% Convert the measured column vectors to single row vectors.
Prout_sim2   = reshape(Prout_sim2 , rows, dim(1,1));
Psw_sim2   = reshape(Psw_sim2 , rows, dim(1,1));
Pcbot_sim2   = reshape(Pcbot_sim2 , rows, dim(1,1));
Pout_sim2   = reshape(Pout_sim2 , rows, dim(1,1));
Ploss_total_sim2   = reshape(Ploss_total_sim2 , rows, dim(1,1));
Pin_sim2   = reshape(Pin_sim2 , rows, dim(1,1));
PCE_sim2   = reshape(PCE_sim2 , rows, dim(1,1));
VCE_sim2   = reshape(VCE_sim2 , rows, dim(1,1));

[PCE2_max,Fsim2]=max(PCE_sim2);
```

Import circuit/SPICE Simulation Data for discontinuous with 15% Non-overlap

```
[~,Pout_sim3,Pin_sim3,PCE_sim3,VCE_sim3,Ploss_total_sim3,Psw_sim3,Pcbot_sim3,Prout_sim3] =
import_powerCSV...
   ('CP_discon_nocomparator_power_15percent.csv');

% Convert the measured column vectors to single row vectors.
Prout_sim3   = reshape(Prout_sim3 , rows, dim(1,1));
Psw_sim3   = reshape(Psw_sim3 , rows, dim(1,1));
Pcbot_sim3   = reshape(Pcbot_sim3 , rows, dim(1,1));
Pout_sim3   = reshape(Pout_sim3 , rows, dim(1,1));
Ploss_total_sim3   = reshape(Ploss_total_sim3 , rows, dim(1,1));
Pin_sim3   = reshape(Pin_sim3 , rows, dim(1,1));
PCE_sim3   = reshape(PCE_sim3 , rows, dim(1,1));
VCE_sim3   = reshape(VCE_sim3 , rows, dim(1,1));

[PCE3_max,Fsim3]=max(PCE_sim3);
```

Matlab Equations for Discontinuous Operation

```
%Equations pasted here from Matlab model for comparison with Circuit sims
```

```
Ppar=((Cgg+0.1*Cfly)*Vin^2).*fsw;      % Parasitic switching and bottom plate losses
a=Cgg+x*Cfly;                          % lump into single constant for use in equations
for k=1:length(dnol)
    for j=1:length(fsw)
      %Vout_dis(k,j)=2*Vin*Rload*Cfly*fsw(j)/(Rload*Cfly*fsw(j)+2*tnol(k));    %   Output Voltage
      %Ipk_dis(k,j)=Vout_dis(k,j)/Rload                                        % peak current
      Ipk(k,j)=20e-6;         % peak current, done to match circuit model which uses ideal current source.
      Iout(k,j)=2*dnol(k)*Ipk(k,j);                  % Average output current
      Vout(k,j)=2*Vin-Iout(k,j)/(Cfly*fsw(j));       % Output voltage
      Pout(k,j)=Vout(k,j)*Iout(k,j);                 % Output Power
      Prout(k,j)=(Iout(k,j)).^2/(fsw(j)*Cfly)+...
            (Iout(k,j)).^2*4*Rsw/(1-2*dnol(k));    % Power losses due to Rout
      Ploss(k,j)=Ppar(j)+Prout(k,j);                 % Total Power Losses
      Pin(k,j)=Ploss(k,j)+Pout(k,j);                 % Input Power
      PCE(k,j)=100*(Pout(k,j)./Pin(k,j));            % Power Conversion Efficiency

  end
end
```

Plots for Power Losses and PCE in Circuit/SPICE model vs. Matlab model

```
fignum=fignum+1;
figObj=figure(fignum);

% Prout plots for circuit model vs Matlab models
subplot(3,1,1)
Prout_plot=plot(fsw,Prout(1,:),fsw_sim,Prout_sim1);
title('Prout vs. f_S_W');
legend('Matlab Model', 'Circuit Model','Location', 'NorthEast');
grid on;

% Ppar plots for circuit model vs Matlab models
subplot(3,1,2)
Ppar_plot=plot(fsw,Ppar,fsw_sim,Pcbot_sim1+Psw_sim1);
title('Ppar vs. f_S_W');
legend('Matlab Model', 'Circuit Model','Location', 'NorthWest');
grid on;

% Pout plots for circuit model vs Matlab models
subplot(3,1,3)
Pout_plot=plot(fsw,Pout(1,:),fsw_sim,Pout_sim1);
title('Pout vs. f_S_W');
legend('Matlab Model', 'Circuit Model','Location', 'southEast');
grid on;

%Label all axes in subplots of Figure 1
% Y labels
Axes3=findobj(figure(fignum),'Type','Axes');
Ylabel3c=get(Axes3,'Ylabel');
Ylabel3=[Ylabel3c{:}];
set(Ylabel3,'string','Power(uW)');
% X labels
Xlabel3c=get(Axes3,'Xlabel');
Xlabel3=[Xlabel3c{:}];
set(Xlabel3,'string','f_S_W(Hz)');
% Figure title
```

```
suptitle(['Figure ',num2str(fignum,'%-2.u'),...
      ': Powers vs. f_S_W in Matlab vs. circuit models']);

fignum=fignum+1;
figObj=figure(fignum);

subplot(2,1,1)
PCE_plot5p=semilogx(Pin(1,:),PCE(1,:),Pin_sim1,PCE_sim1);      % Note: circuit model did not go low
enough in fsw for 5%
title('PCE vs. Pin ( d_N_O_L=5%)');
legend('Matlab Model', 'Circuit Model','Location', 'NorthEast');
grid on;

subplot(2,1,2)
PCEplot_comp=semilogx(Pin(2,:),PCE(2,:),Pin_sim2,PCE_sim2,Pin(3,:),PCE(3,:),Pin_sim3,PCE_sim3);
title('PCE vs. Pin ( d_N_O_L=10%,15%)');
legend('Matlab Model', 'Circuit Model','Location', 'NorthEast');
grid on;
%Label axes in subplots of Figure 2
% Y labels
Axes3=findobj(figure(fignum),'Type','Axes');
Ylabel3c=get(Axes3,'Ylabel');
Ylabel3=[Ylabel3c{:}];
set(Ylabel3,'string','PCE(%)');
% X labels
Xlabel3c=get(Axes3,'Xlabel');
Xlabel3=[Xlabel3c{:}];
set(Xlabel3,'string','P_I_N(uW)');
% Figure title
suptitle(['Figure ',num2str(fignum,'%-2.u'),...
      ': PCE for Matlab model vs. circuit model']);
```

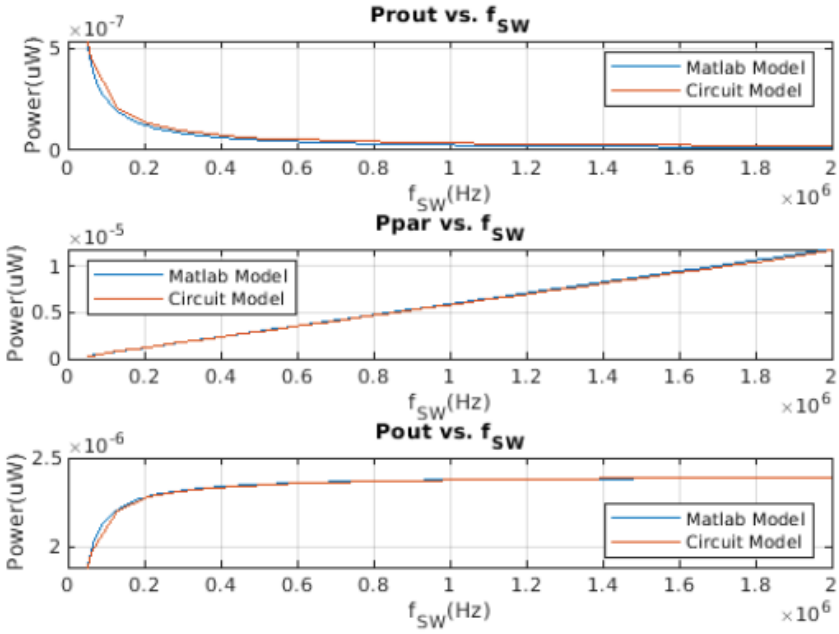

Figure B - 1 Power losses and P_{OUT} for Matlab vs. circuit model

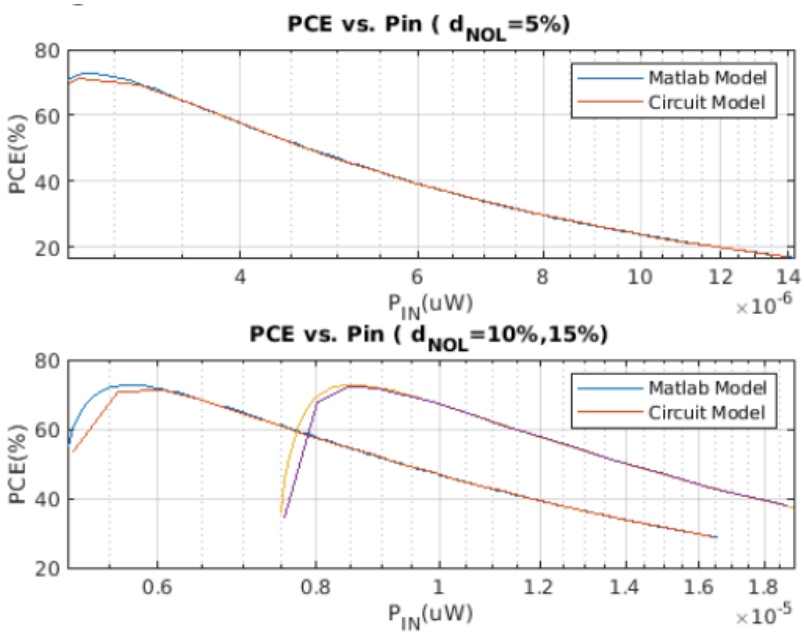

Figure B - 2 PCE vs. P_{IN} for Matlab vs. Circuit models

Import Circuit/SPICE Simulation Data Continuous Operation

```
[fsw_sim_cont,Pout_sim_cont,Pin_sim_cont,PCE_sim_cont,VCE_sim_cont,Ploss_total_sim_cont,Psw_si
m_cont,Pcbot_sim_cont,Prout_sim_cont,Iout_sim_cont] = import_powerCSV_res...
   ('CP_cont_resload_power.csv');

% Convert the measured column vectors to single row vectors.
dim = size(fsw_sim_cont);   rows = 1;     columns = dim(1,1);
fsw_sim_cont = reshape(fsw_sim_cont, rows, dim(1,1));
Prout_sim_cont   = reshape(Prout_sim_cont , rows, dim(1,1));
Psw_sim_cont   = reshape(Psw_sim_cont , rows, dim(1,1));
Pcbot_sim_cont   = reshape(Pcbot_sim_cont , rows, dim(1,1));
Pout_sim_cont   = reshape(Pout_sim_cont , rows, dim(1,1));
Ploss_total_sim_cont   = reshape(Ploss_total_sim_cont , rows, dim(1,1));
Pin_sim_cont   = reshape(Pin_sim_cont , rows, dim(1,1));
PCE_sim_cont   = reshape(PCE_sim_cont , rows, dim(1,1));
VCE_sim_cont   = reshape(VCE_sim_cont , rows, dim(1,1));
```

Circuit Model plots for PCE vs. Pin for Continuous vs. Discontinuous

```
fignum=fignum+1;
figObj=figure(fignum);

subplot(1,2,1)
PCEplot_comp=semilogx(Pin_sim1,PCE_sim1,Pin_sim2,PCE_sim2,Pin_sim3,PCE_sim3,Pin_sim_cont,P
CE_sim_cont);
ylabel('PCE(%)');
xlabel('P_I_N(uW)')
title('PCE vs. P_I_N');
legend('5% d_N_O_L', '10% d_N_O_L','15% d_N_O_L','Cont.','Location', 'SouthEast');
grid on;

subplot(1,2,2)
```

```
VCEplot_comp=semilogx(Pin_sim1,VCE_sim1,Pin_sim2,VCE_sim2,Pin_sim3,VCE_sim3,Pin_sim_cont,
VCE_sim_cont);
ylabel('VCE(%)');
xlabel('P_I_N(uW)')
title('VCE vs. P_I_N');
legend('5% d_N_O_L', '10% d_N_O_L','15% d_N_O_L','Cont.','Location', 'SouthEast');
grid on;
%Figure title
suptitle(['Figure ',num2str(fignum,'%-2.u'),...
    ': Discontinuous vs. Continuous operation in Circuit Model']);
```

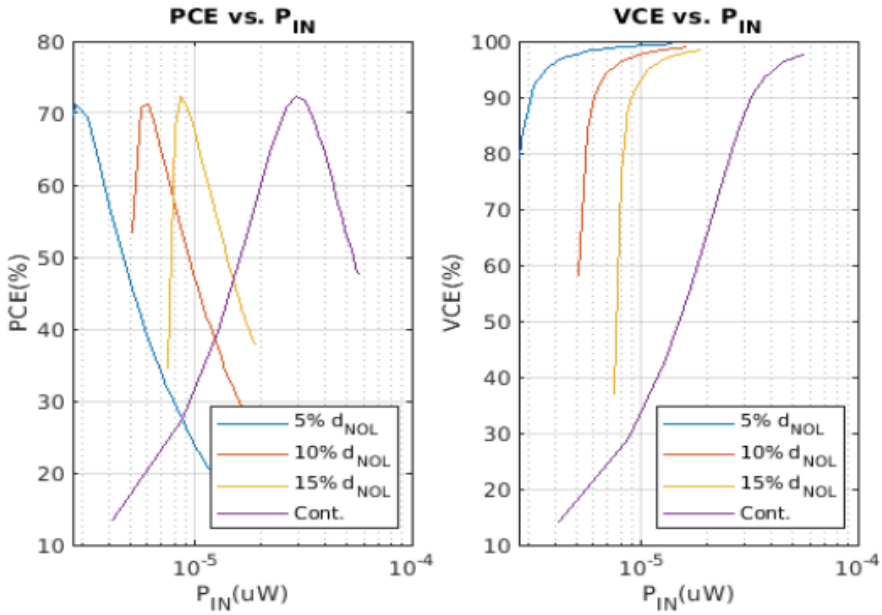

Figure B - 3 PCE and VCE vs. P_{IN} for discontinuous and continuous operation

B-2. Contour Plot of 2D Tracking Technique

Define Constants

```
Vin=0.6;          % Input Voltage
Rload=40e3;       % Load Resistance
k=0;              % counter
j=0;              % counter
Rsw=45;           % MOSFET switch Resistance (for each switch)
Cgg=360e-15;      % Total switch gate caps
Cfly=160e-12;     % Flying cap --> accounts for two 80pF caps
x=0.1;            % bottom plate cap percentage of Cfly
```

Define Variables

```
fsw=10e3:10e3:1e6;        % Switching frequency variable for discontinuous operation
dnol=0.05:0.2/99:0.25;    % Clock Non-Overlap time variable
```

Matlab Equations for Discontinuous Operation

```
% Pasted from Matlab model here. fsw and dnol vector sizes are different to enable contour plot ( dnol and
fsw must be same length)
```

```
Ppar=((Cgg+0.1*Cfly)*Vin^2).*fsw;                    % Parasitic switching and bottom plate losses
a=Cgg+x*Cfly;                                        % lump into single constant for use in equations
for k=1:length(dnol)
   for j=1:length(fsw)
      Vout_dis(k,j)=2*Vin*Rload*Cfly*fsw(j)/(Rload*Cfly*fsw(j)+2*dnol(k));    % Output Voltage
      Ipk_dis(k,j)=Vout_dis(k,j)/Rload;                                       % peak current
      %Ipk(k,j)=20e-6; % peak current, done to match circuit model which uses ideal current source.
      Iout(k,j)=2*dnol(k)*Ipk_dis(k,j);              % Average output current
      %Vout(k,j)=2*Vin-Iout(k,j)/(Cfly*fsw(j));      % Output voltage
      Pout(k,j)=Vout_dis(k,j)*Iout(k,j);             % Output Power
      Prout(k,j)=(Iout(k,j)).^2/(fsw(j)*Cfly)+...
            (Iout(k,j)).^2*4*Rsw/(1-2*dnol(k));      % Power losses due to Rout
      Ploss(k,j)=Ppar(j)+Prout(k,j);                 % Total Power Losses
      Pin(k,j)=Ploss(k,j)+Pout(k,j);                 % Input Power
      PCE(k,j)=100*(Pout(k,j)./Pin(k,j));            % Power Conversion Efficiency

   end
end
[TNOL,FSW]=meshgrid(dnol,fsw);                       % Generate meshgrid
[Con,h]=contour(TNOL,FSW./1000,PCE,[50:10:70,72]);   % Generate contour
clabel(Con,h,'FontSize',18,'FontWeight','bold');     % Labels for contour
xlabel('d_N_O_L');
ylabel('f_S_W');

%Figure title
title('Contour plot of PCE as a function of d_N_O_L and f_S_W');
```

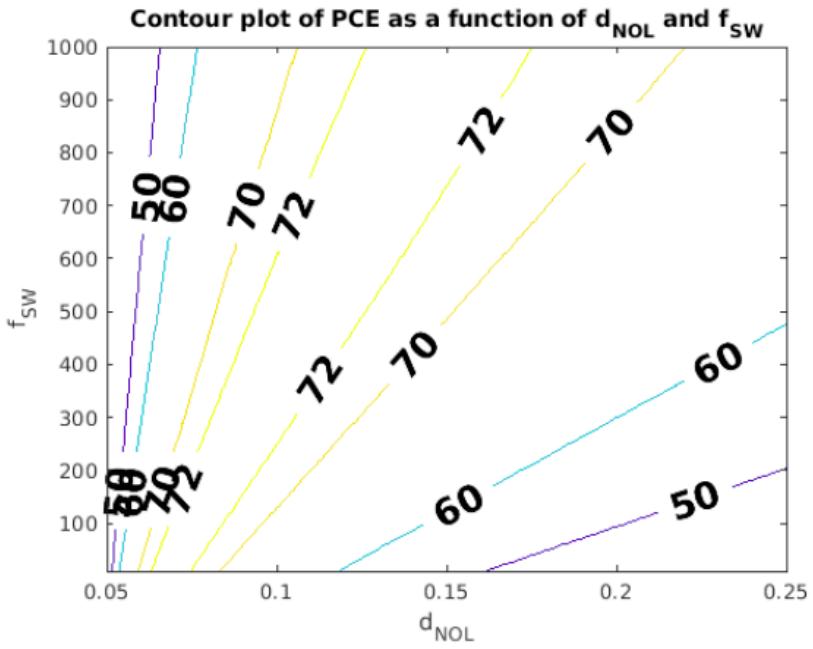

Figure B - 4 Contour plot of PCE as a function of d_{NOL} and f_{SW}