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Conducted EMI Mitigation in Power Converters using Active EMI Filters

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Conducted EMI Mitigation in Power Converters using Active EMI Filters

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy in Engineering with a concentration in Electrical Engineering

by

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Abstract

Wide bandgap devices enable high power density power converters. Despite the advantages of increased switching frequency, the passive components are still a major bottleneck towards enabling high power density. Among the passive components in the converter, the passive EMI filters are unavoidable to ensure compliance with conducted EMI standards. Active EMI filters help reduce the volume of the passive components and have been around for three decades now. Firstly, this work presents a summary of all the different active EMI filters based on the type of noise-sensing, noise-processing, the type of active circuits used and the type of control methods. This is followed by modeling, design and stability analysis of three different active EMI filters for DM noise attenuation. The first active EMI filter is a conventional active EMI filter. The key bottlenecks to improving performance of the conventional active EMI filter are identified while still achieving volume reduction of passive components. Following this two novel active EMI filters are presented that overcome the bottlenecks of conventional active EMI filter. The second active EMI filter is based on a analog twin-circuit. This novel filter uses a twin-circuit which enables the use of low-voltage surface-mount components for compensation. The third active EMI filter uses zero-phase filtering implemented in an FPGA. While all the filters are demonstrated for differential-mode noise, their use can be extended for common-mode noise attenuation.

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Dedication

Dedicated to my dad, mom and sister. Dad, I wish you were here to see me graduate.

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   doi: 10.1109/TEMC.2019.2953055.
   Chapter 2 is made up of this paper

2. B. Narayanasamy, F. Luo and Y. Chu, ”Modeling and Stability Analysis of Voltage Sensing based Differential Mode Active EMI Filters for AC-DC Power Converters,” *2018 IEEE Symposium on Electromagnetic Compatibility, Signal Integrity and Power Integrity (EMC, SI PI)*, Long Beach, CA, 2018, pp. 322-328. doi: 10.1109/EMCSI.2018.8495239
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3. B. Narayanasamy, H. Peng, Z. Yuan, A. I. Emon and F. Luo, ”Modeling and Analysis of a Differential Mode Active EMI Filter With an Analog Twin Circuit,” in *IEEE Transactions on Electromagnetic Compatibility*, doi: 10.1109/TEMC.2020.3006427.
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4. B. Narayanasamy, H. Peng, Z. Yuan and F. Luo, ”Zero-Phase-Filtering based Digital Active EMI Filter,” submitted for review *IEEE Transactions on Power Electronics*, **Under review.**
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1 Introduction

The world is progressing towards more and more electrification in many major sectors such as automotive, aerospace, automation in homes, commercial and industrial facilities. Further, the growth in the area of renewable energy is also accelerating at a rapid pace. And, the COVID-19 pandemic has, and will continue to change how people live, learn and work. With more and more work, education and services shifting remote or online, the cloud infrastructure will continue to see tremendous growth. Power electronics is at the heart of all these powering more devices than ever in our lifetime. And, all of these activities demand high-density and high-efficiency power conversion.

Wide bandgap semiconductors such as GaN and SiC devices are key enablers for a electrified future. These devices enable high switching speeds (few ns to 10s of ns) and high switching frequencies (100s of kHz to few MHz). In addition, the higher junction temperatures enable the reduction in cooling requirements. The combined effect of increased switching frequency and higher junction temperature enable high power density power converters. However, one of the major bottlenecks for high power density is the passive components in the converter. Passive components are part of power processing circuitry, output and input harmonics and electromagnetic interference (EMI) filters. Increasing switching frequency mostly guarantees reduction in passives used for power processing and harmonic filter. However, this is not true in case of EMI filters.

In order to understand this, it is essential to look at the factors affecting the generation and propagation of EMI. EMI in power electronic converters is a result of switching action of power semiconductor devices. The generation of EMI not only depends on the switching frequency, but

also on the switching speed and the parasitics of the semiconductor devices, passive components and layout that are part of the power electronic converter. The EMI could be classified into two types based on the propagation path as conducted and radiated emissions. Conducted emissions refers to the noise that propagates in the physical connections such as cables or PCB traces. And, Radiated emissions refers to the noise propagating through the medium enclosing the power converter (typically air). All power converters generate both forms of emissions. Depending on the area of application, the converter needs to comply with noise limits put out by organizations such as IEC, CISPR, FCC etc. For example, a desktop power adapter for domestic use is considered an Information Technology Equipment (ITE) and therefore needs to comply with either CISPR-22 Class B or FCC Class B standard. Most of the time, the converter by itself is not compliant with the standard limits. In such cases, PCB layout changes or additional components such as filters, shielding etc. are used to make the converter comply with the emissions part of the standard. Henceforth, the discussion will be limited to the filters used for mitigation of conducted emissions in a power converter. For nearly a century, the filters have been exclusively built using passive components. The parasitics of the passive components result in bulky passive EMI filters and reduced performance at high frequencies (above a few MHz). In a typical power converter, the passive EMI filter could occupy up to one-third of system volume and weight. Even in such power converters, the passive EMI filters form the bottleneck for major improvements in power density. This is because of two reasons. Firstly, advancements in passive components has not kept up with the pace of developments in the semiconductor industry. And, higher switching frequency and switching speeds may further increase the EMI filter requirements because the limits imposed by standards remain the same.

Therefore, it is necessary to develop high density EMI filter solutions that are more suit-

able for future power electronic converters. One such solution to reduce the volume of passive component in an EMI filter is active EMI filtering. In an active EMI filter, the noise in a circuit is sensed and injected into the circuit after flipping the phase by 180 degrees. Ideally, the injected noise would completely cancel the noise generated by the converter. But, the parasitics of the passive components in the noise-sensing and noise-cancellation stages, and the bandwidth of the active components, limits the maximum attenuation. Depending upon the propagation path, the conducted emissions could be further classified into common-mode (CM) and differential-mode (DM) noise. CM noise refers to noise that flows on both lines and returns through the ground and DM noise flows within the lines.

This work aims at overcoming the limitations of active EMI filters for DM noise mitigation and improving the maximum possible attenuation in ac-dc applications. This dissertation consists of 4 main parts. In Chapter 2, a review of all existing active EMI filters based on the type of converter, type of noise-sensing, noise-cancellation, noise-processing circuits among other factors such as power-loss, reliability and commercial products are summarized. In Chapter 3, design, modeling and stability analysis of a conventional analog active EMI filters for a desktop power adapter is presented. This exercise helps identify the limitations of conventional analog active EMI filters. To overcome these limitations, two novel active EMI filters are proposed. They are – analog twin based active EMI filter and zero-phase filtering based active EMI filter. The analog twin based active EMI filter is presented in Chapter 4 and zero-phase filtering based digital active EMI filter is presented in Chapter 5. Finally, the conclusion and future work are presented in Chapter 6.

2 A Survey of Active EMI Filters for Conducted EMI Noise Reduction in Power Electronic Converters

2.1 Abstract

Wide bandgap devices enable high power density power converters. Despite the advantages of increased switching frequency, the passive components are still a major bottleneck towards enabling high power density. Among the passive components in the converter, the passive EMI filters are unavoidable to ensure compliance with conducted EMI standards. Active EMI filters help reduce the volume of the passive components and have been around for three decades now. The design and implementation of the active EMI filters depend upon the type of noise (common-mode or differential-mode) and power converter (ac-dc, dc-dc or inverter). This paper presents a comprehensive survey of different active EMI filters and their implementations for different power converters presented in the literature. A comprehensive survey of noise-sensing, noise-processing, and noise-cancellation circuits is presented. Also, a comparison of attenuation provided by the active EMI filters for common-mode and differential-mode noise for different converters is carried out. Further, other facets of active EMI filters such as the auxiliary power supply, power loss and protection methods for the active EMI filter are also summarized. This paper is intended to be a useful reference for power converter designers in both industry and academia.

2.2 Introduction

Power converters generate conducted and radiated emissions due to the switching action of the power semiconductor devices. Conventionally, a second-order passive EMI filter is used to

mitigate the conducted EMI noise generated by the power converter. These passive filters tend to be bulky and could occupy up to 30% of the system volume. Therefore, minimizing the passive EMI filter volume has been a priority for power converter designers. By reducing the noise source, the passive filter volume could be minimized. A summary of reducing the noise at the source by employing different techniques such as circuit topologies (soft-switching), layout optimization and modulation have been summarized in [1, 2]. Besides these, different passive techniques could be employed to improve the attenuation provided by a given passive EMI filter. These techniques involve modifying the propagation path impedance using small passive components [3], proper design of the inductor to avoid saturation due to the common-mode (CM) volt-second and differential-mode (DM) currents [4–6], parasitic cancellation [7] and mutual coupling elimination [8].

Recently, emerging applications of Wide Bandgap (WBG) device based motor drives enable high efficiency and high power-density owing to superior switching speeds resulting in lower switching losses than their Si counterparts [9, 10]. WBG devices have been used to demonstrate high power density converters [11, 12]. But, passive filters are still one of the major bottlenecks to increasing power density due to other adverse effects of higher switching speeds [13]. Active EMI filters (AEF) show great promise in reducing the passive component volume in power converters. There have been numerous works in the area of applying AEF for power converters in the past three decades with volume reductions higher than 50% [14–16]. The fundamental building blocks of the AEF were identified and basic topology classification was carried out previously[17, 18]. In 2010, a summary of the classification of AEF was provided in [2]. The methodology of AEF topology selection for a given source and load impedance was presented in [16]. The generalization of the attenuation provided by the AEF and their corresponding impedance was studied in

[19]. Along with the AEF, another passive component could be used to improve the overall attenuation and bandwidth. These are referred to as hybrid EMI filters (HEF). The generalization and basic classification of HEF based on the equivalent circuits was presented in [20]. The generalization approach proposed in [20] was experimentally verified in [21, 22] for ac-dc converters. All these works discuss the generalized approach and classification of AEF and HEF. Besides these works, there are a few commercially available AEF and HEF. For input side EMI reduction, HEF for CM and DM noise mitigation (Picor® Quietpower® series) are available from Vicor Corp [23] and AEF for CM noise mitigation is available from Schaffner Inc [24] for dc-dc converters. A CM AEF is also available for ac-fed converters and inverters from EMcoretech Inc [74]. However, a comprehensive survey and comparison of different implementations of AEF/HEF for CM and DM noise mitigation in different power converters has not been performed yet.

Since the publication of [16, 19–21], there have been numerous other implementations involving different active techniques to achieve passive volume reduction. It is therefore important to revisit, compare and summarize these works in the literature to identify the best implementations. This work aims at summarizing the different implementations of these active techniques in different power converters (dc-dc, ac-dc and inverters) for CM, DM and line (positive/negative or line/neutral) noise. The passive volume reduction is proportional to the attenuation provided by the AEF. Therefore, different implementations of the AEF are compared in terms of the attenuation provided at frequencies of 150 kHz and 1 MHz for both CM and DM noise. Comparisons are made to identify the benefits and drawbacks of different implementations. Other aspects such as the types of noise-sensing networks, noise-cancellation networks, the implementation of the AEFs, the power source for the AEF, the power loss associated with AEF, and other considerations specific to different methodologies of implementation are also summarized.

The organization of the paper is as follows. Section II presents the various topologies of AEF and HEF. Section III presents the different implementations (noise-sensing, active circuits, and noise-cancellation methods) of the AEF for different power converters. Section IV presents the summary of different stability analysis and compensation techniques. Section V presents a comparison of the attenuation of AEF for different converters in literature. Section VI presents the summary of different implementations of the power source and power loss for the AEF. Section VII presents the different protection circuits for AEF. Section VIII presents the conclusion which identifies the prominent works of AEF and areas that require future research to enable widespread adoption of AEF.

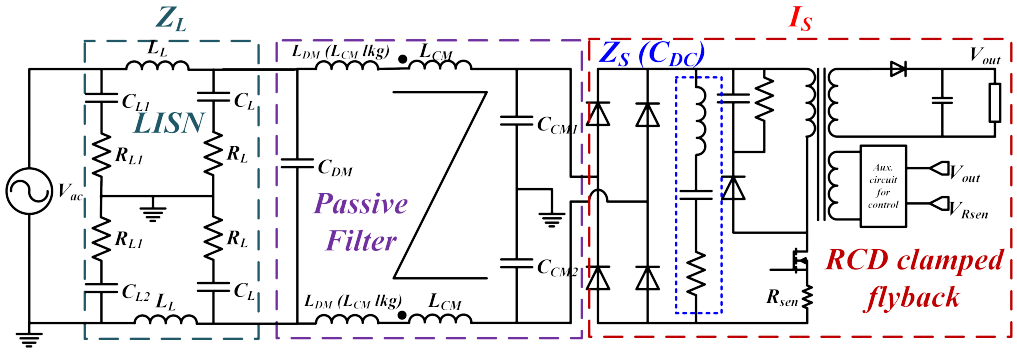

Fig. 2.1: Noise source (I_S), noise source impedance (Z_S) for DM noise, noise load impedance (Z_L) in an RCD (resistor capacitor diode) clamped flyback converter

2.3 Active EMI filter Topologies and Implementation

2.3.1 Introduction and Basic Classification of AEFs

A typical ac-dc converter is shown in Fig. 2.1. I_S denotes the noise source which is the converter, Z_S represents the noise source impedance and Z_L represents the load impedance which is the LISN. There are 3 main parts of an AEF circuit. They are: noise-sensing circuit, noise-processing active circuit and noise-injection circuit. Conventionally, the noise-processing active

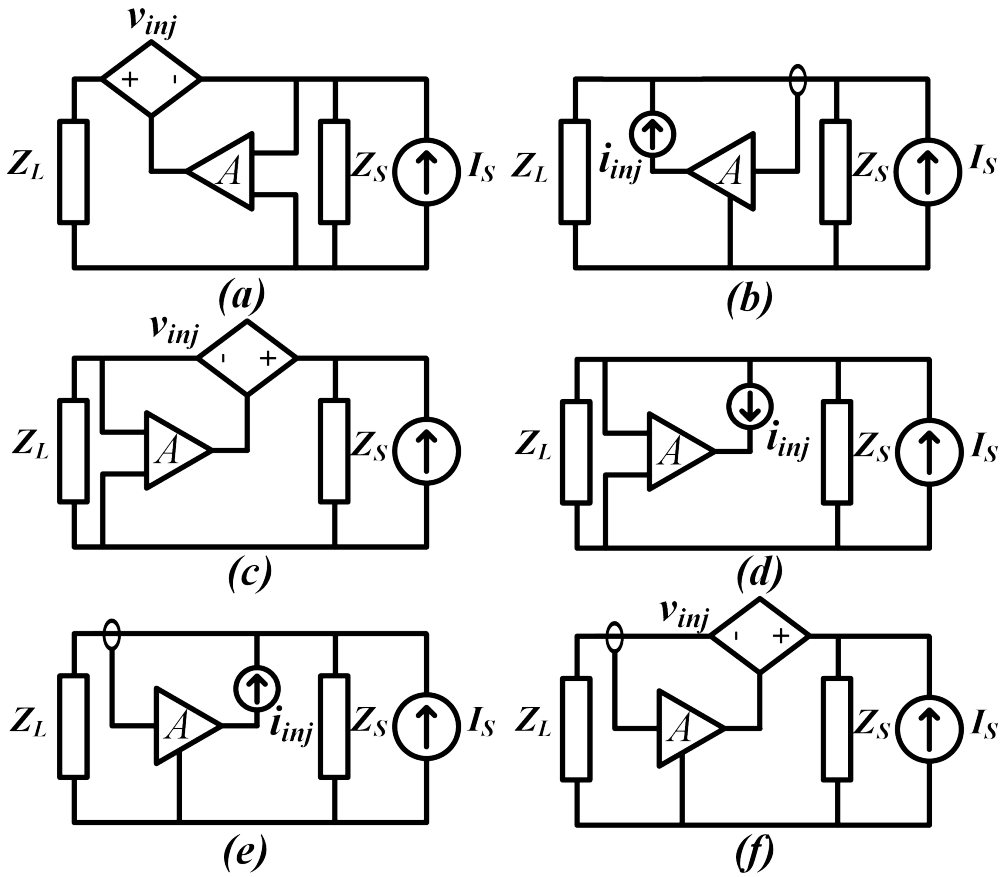

Fig. 2.2: Active EMI Filter Topologies (a) feedforward voltage-sense voltage-cancellation (b) feedforward current-sense current-cancellation (c) feedback voltage-sense voltage-cancellation (d) feedback voltage-sense current-cancellation (e) feedback current-sense current-cancellation (f) feedback current-sense voltage-cancellation. Z_S is the noise source impedance, Z_L is the load impedance. Different passive elements could be added in place of Z_S and Z_L to form different HEF (A - represents the gain of the active circuit)

circuit involves an amplifier stage that is capable of driving the injection stage. But, there have been other implementations of the AEF that use other components such as DSP (Digital Signal Processor) or an FPGA (Field Programmable Gate Array) in addition to the amplifier. Therefore, in this paper, this part of the circuit would be referred to as the noise-processing circuit. The AEF may either use noise-current or noise-voltage sensing or cancellation. The combination of different noise-sensing and noise-cancellation methodologies yields the conventional AEF as shown in Fig. 2.2. Further, depending upon whether the noise-sensing is done at the source or the load side, the

control scheme is either feedforward or feedback. The AEF by itself is a one-order filter. Owing to the bandwidth limitation of sensing, processing and cancellation stages, the AEF is intended to provide noise attenuation at frequencies from the start of EMI frequency range (150 kHz in case of the CISPR (International Special Committee on Radio Interference standard) up to a few MHz. In order to provide noise attenuation at higher frequency ranges, it is essential to have another passive element. This passive element in combination with the AEF forms the hybrid EMI filter (HEF). The higher the attenuation and bandwidth provided by the AEF, the smaller is the additional passive component required to form the HEF. The selection of a particular AEF topology depends upon the source and load impedance. The selection of the appropriate AEF and HEF topologies for CM and DM noise reduction was discussed in detail in [16, 19, 20].

2.3.2 Different noise sensing implementations for AEF

Depending on whether CM, DM or line/neutral noise is sensed, different implementations of noise-sensing have been demonstrated in the literature. Some of the most commonly used implementations are shown in Fig. 2.3.

Noise Current Sensing Implementations

In [68], a Rogowski coil was used to sense the DM noise current at the output of a dc-dc converter. In [53], a current transformer (CT) with high bandwidth was used for DM noise current sensing in a dc-dc converter. In ac-dc converters for noise sensing, the CT is part of a high pass filter to attenuate the fundamental frequency and its harmonics. In [54–58, 69], a CT is used as part of a second-order high pass filter for DM noise current sensing in ac-dc converters. No work has implemented current sensing using CT for DM noise reduction in inverters. The CM noise-

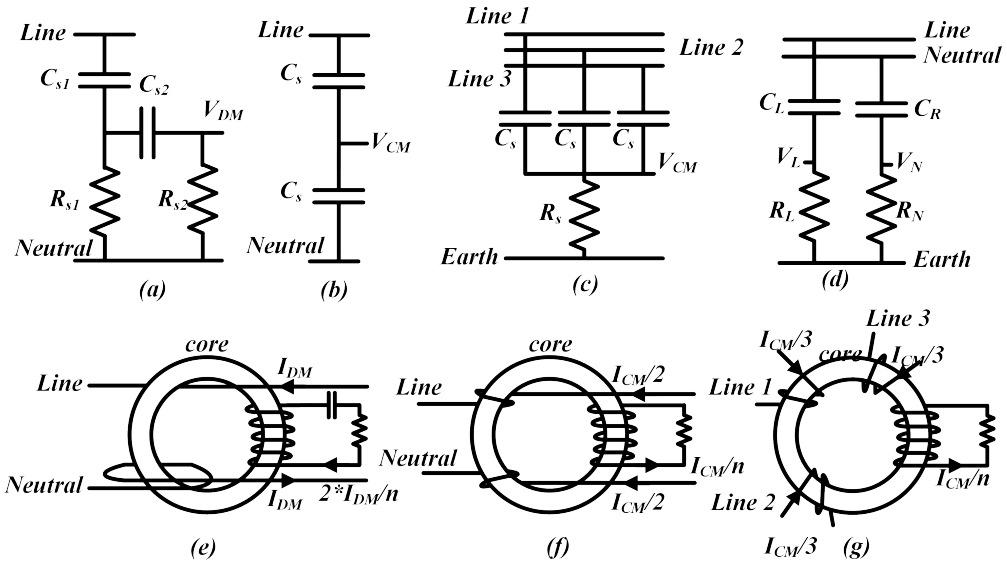

Fig. 2.3: Noise-sensing methodologies (a) second-order high pass filter for DM noise voltage sensing on single-phase ac lines [22, 25] . For dc systems just the capacitor or a single order high pass filter can be used [15, 17, 23, 26–32] (b) Y-capacitors on both lines for CM noise voltage sensing in single-phase ac and dc systems [14, 33–39] (c) Y-capacitors on all lines for CM noise voltage sensing in three-phase systems [16, 32, 40–48] (d) first order high pass filter for sensing on individual lines (line/neutral or Positive/Negative) for single-phase ac or dc systems [21, 31, 41, 49–52] (e) current transformer for DM noise current sensing in single-phase ac or dc systems [53–58] (f) current transformer for CM noise current sensing in single-phase ac or dc systems [20, 24, 53, 59–65] (g) current transformer for CM noise current sensing in three-phase systems [16, 19, 66, 67]

sensing CT could be directly connected to the active circuit and does not require any high/low pass filtering. However, there is one exception to this implementation. For output noise sensing in inverters, the CT has to be implemented alongside a high pass filter to prevent the AEF from compensating for low-frequency harmonics of fundamental frequency. In [20, 24, 53, 59–62], a CT was used for CM noise current sensing in a dc-dc converter. In [70–75], a CT was used for CM noise current sensing in an ac-dc converter. In [19, 66, 67], a CT was used to measure input CM noise in an ac fed motor drive. In [63, 64] a CT was used for measuring input CM noise in a full-bridge inverter. In [16], a CT was used for sensing output CM noise current in a dc fed motor drive. In [65], a CT was used for sensing CM noise in a single-phase grid-tied inverter.

Noise Voltage Sensing Implementations

DM noise voltage sensing requires only one capacitor that is rated for the operating voltage of the converter. In dc-dc converters, this capacitor could be directly connected to the active circuit. In ac-dc and dc-ac converters, the capacitor is part of a high pass filter network to attenuate the fundamental frequency and its harmonics and other low frequency that may be present in the source voltage. DM noise voltage sensing using capacitors was used in AEF for dc-dc converters in [15, 17, 23, 26–32]. Noise voltage sensing using capacitors as part of a high pass filter network is used in [22, 25]. For CM noise-sensing, capacitors are required on each of the lines with the other end of all the capacitors connected together. In [14, 33–37], capacitors were used on line and neutral for CM noise-sensing. In [38, 39], noise voltage sensing using capacitors was used for AEF in the input side of a three-phase sparse matrix converter. Noise voltage sensing was realized using a capacitor on all three-phase outputs in [40–45] for an ac-dc-ac converter (ac-fed motor drive) and in [16, 32, 46–48] for dc-ac converters (dc-fed motor drive). Besides CM and DM noise sensing, RC networks were used on each line to sense the individual line noise. This method was used in [21, 49, 50] for ac-dc converters, in [51] for a dc-dc converter, [52] for a grid-tied single-phase full-bridge inverter and [31] for a single-phase ac-dc-ac inverter (arc welding inverter). Another implementation used resistive voltage dividers along with high-voltage isolators to sense the CM noise voltage in a three-phase inverter [41].

2.3.3 Different Noise Processing Circuits for AEF

Active circuits process the noise from the sensing circuit and provide the cancellation voltage/current. Noise-processing involves multiple functions such as compensation for ensuring sta-

bility, amplification and others depending upon the control scheme. The active circuit should be capable of providing the necessary gain depending on the control scheme and should be capable of driving the noise injection stage without becoming unstable. In an AEF, instability may occur at frequencies lower or higher than the EMI frequency range. Typically, the active circuits have compensation networks to ensure stability. The different implementations of active circuits in literature are discussed based on the control scheme and the type of elements used in active circuits for CM, DM, and L/N noise-cancellation.

Different Control Scheme Implementations

Feedforward and feedback control are two basic control schemes of the AEF. The feedforward control requires unity gain throughout the desired frequency range. Because of parasitics of different elements in the circuit, the gain could easily overshoot or undershoot unity gain at different frequencies. While the feedforward control method could easily ensure stability, its performance is subjected to component tolerances. On the other hand, the feedback control requires a high-gain feedback loop. While the feedback control method is immune to component value variations, it could potentially become unstable at high or low frequencies. Therefore, it requires suitable compensation to ensure stable operation.

In [15, 32, 68], the AEF with feedforward control was used in for DM noise-cancellation in a dc-dc converter. In [34], AEF with feedforward control was used in AEF for CM noise-cancellation in an ac-dc converter. Feedback control was used for DM noise-cancellation in [23, 29, 30, 76] for dc-dc converters and [22, 25, 55, 58, 69] for ac-dc converters. Feedback control was used for CM noise-cancellation in [20, 59, 60, 62] for dc-dc converters and [14, 21, 24, 35–37, 61, 71, 73–75, 77] for ac-dc converters. In [16, 32, 40–42, 44, 47, 48, 78–80], feedforward

control is used for output CM noise-cancellation for inverters. In [19, 38, 39, 63, 64, 66, 67] and [44, 46, 65, 65], feedback control method was used for CM noise-cancellation on input and output of inverters respectively. A combination of feedforward and feedback control was used for DM noise-cancellation in [27, 28, 53, 81] for dc-dc converters and in [56] for ac-dc converters. In [57], a comparison of feedforward & feedback with series and parallel feedback structures was carried out.

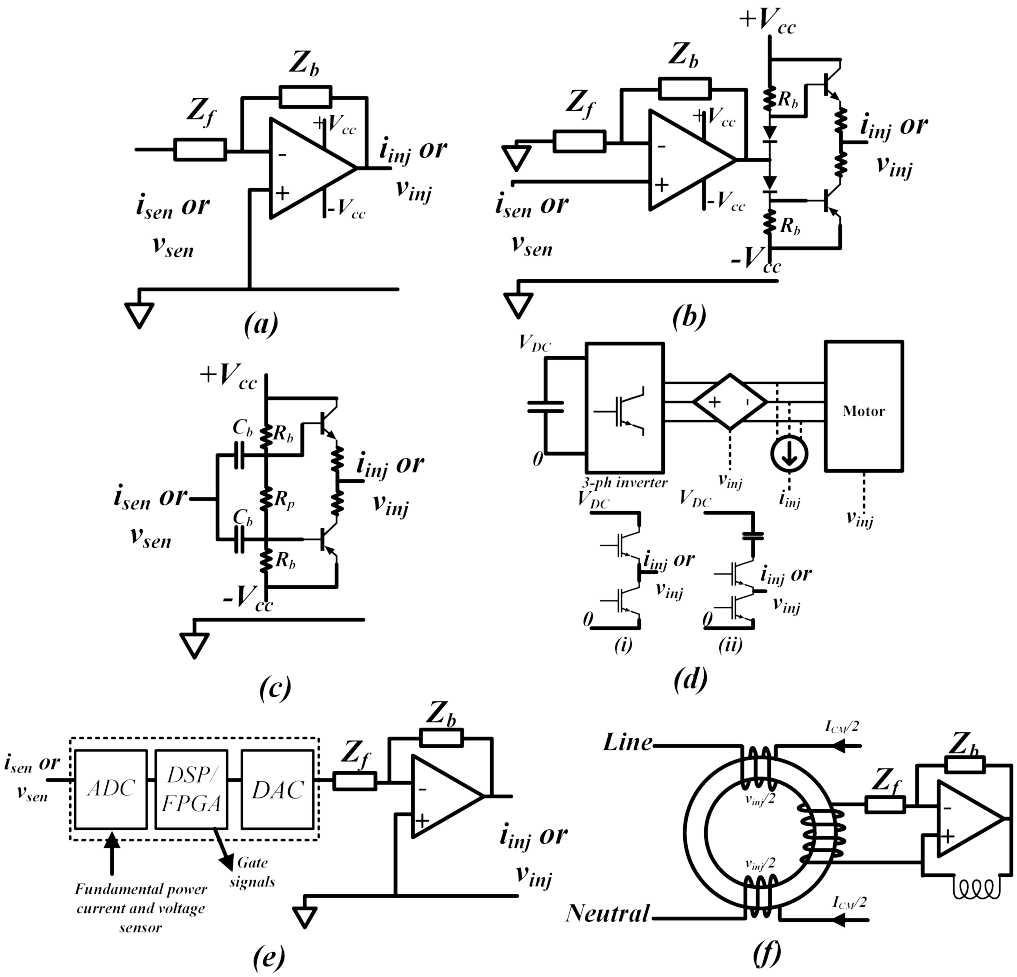

Fig. 2.4: Different active circuits (a) only op-amp [14–16, 20, 21, 23, 29–34, 44, 46, 47, 50–52, 54, 59–61, 65, 68, 70–72, 76, 80] (b) op-amp + discrete device based amplifier [27, 28, 36, 36, 38, 39, 53, 65, 74, 75, 81] (c) only discrete device based circuit [17, 26, 82] (d) For inverters (i) High-voltage BJTs based active circuit / 4^{th} leg [48, 66, 78, 79, 83] (ii) Low-voltage BJTs based active circuit [19, 40–43, 67**?**] (e) DSP/FPGA + op-amp active circuit where the converter control is implemented in the same DSP/FPGA [31, 32, 40–44, 51] (f) negative impedance converter based active circuit [77]

Different Active Circuit Implementations

A summary of different active circuits used in literature is shown in Fig. 2.4. The first implementation of AEF used only BJTs (bipolar junction transistors) as active circuits [17, 26, 82]. In most of the cases a single op-amp was used to drive the noise-injection stage or the active circuit to set the gain and as well as to drive the noise injection for CM and DM noise-cancellation in dc-dc, ac-dc and inverters [14–16, 20, 21, 23, 29–34, 44, 46, 47, 50–52, 54, 59–61, 65, 68, 70–72, 76, 80]. However, there are instances where it is economical to use discrete transistors only or along with a low power high gain op-amp to set the gain for the active circuit. Such implementations could be seen for DM noise-cancellation in [27, 28, 53, 81], for CM noise-cancellation [75] for dc-dc converters and for DM noise-cancellation in [55, 58, 69] and for CM noise-cancellation in [36, 36, 74] for ac-dc converters and for CM noise-cancellation in [38, 39, 65] for single-phase inverters.

For three-phase inverters, different active circuits have been implemented. First implementation used high-voltage BJTs fed from the dc-link for CM noise reduction [66, 78]. In [19, 67], the high-voltage BJTs were replaced with low-voltage BJTs. The transistors were connected to the dc-link via a dc blocking capacitor and were used to reduce output CM noise [40–44]. In [63, 64], used the CM noise current sensed to modulate the gate signals to achieve CM noise-cancellation. Another prominent method was using a 4^{th} leg in the three-phase inverter. This method was used in [79, 83] to reduce the CM noise in the circuit. Another implementation used BJTs rated for $V_{DC}/3$ for CM noise reduction [48].

In [73], multiple op-amps were cascaded to obtain higher gain for the feedback implementation. In [51], the use of DSP along with high-speed ADC/DAC (analog to digital converter/digital

to analog converter) was used as part of the active circuit. This is referred to as the digital AEF. The digital AEF was extended to a three-phase inverter in [50] and grid-tied inverter in [52]. In [84], the effect of delay between noise sensing and injection in a digital AEF was studied and methodology for decoupling the sensing and injection stages was presented and demonstrated in a single-phase arc welding inverter. In [31], an FPGA was used along with high-speed ADC/DAC to implement a filter that uses the noise sensed from the previous switching cycle to compensate for the current switching cycle. In [32], using noise from the previous cycle to inject into the current cycle using wavelet transforms was proposed and demonstrated in a dc-dc boost converter and dc fed z-source inverter.

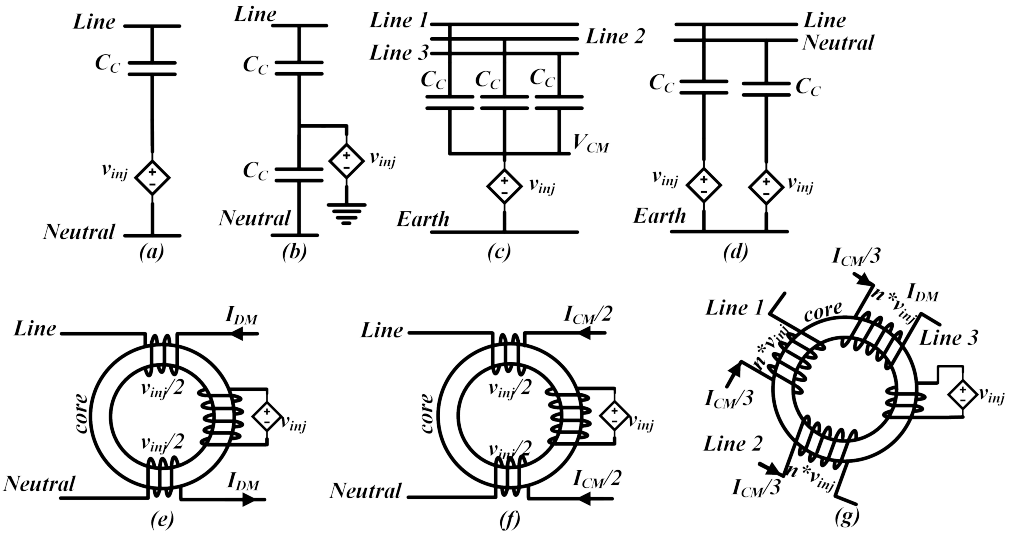

Fig. 2.5: Different noise-cancellation circuits (a) DM noise current cancellation in ac-dc and dc-dc converters [22, 25, 26, 29, 49, 53–58, 68, 70] (b) CM noise current cancellation in single-phase ac and dc lines [14, 21, 35, 37, 49, 54, 62, 72–75] (c) CM noise current cancellation in three-phase lines [16, 19, 38, 39, 48, 65–67, 85] (d) Line (/positive) and Neutral (/negative) noise current cancellation in single-phase ac (/dc) lines [50–52, 84] (e) DM noise voltage cancellation in ac-dc and dc-dc converters [27, 28, 76, 81] (f) CM noise voltage cancellation in single-phase ac lines [34, 36, 71] (g) CM noise voltage cancellation in three-phase ac lines [32, 40, 42–46, 78, 79]

2.3.4 Different noise-cancellation implementations

Noise-cancellation techniques involve noise current and noise voltage cancellation. Some of the cancellation techniques in the literature are shown in Fig. 2.5. In current cancellation, the active circuit drives a voltage across an injection capacitor resulting in cancellation current injected in the circuit. In voltage cancellation, the active circuit drives a voltage injection transformer that injects the cancellation voltage in the main circuit. The voltage cancellation is usually not preferred for DM noise, since the voltage injection transformer can be bulky. Since current cancellation requires only high-voltage capacitors, they are usually preferred. But, for CM noise-cancellation, the maximum value of capacitance is limited by the leakage current. Therefore, the maximum attenuation using current cancellation is limited. So, some implementations use noise voltage cancellation for CM noise. The connection of capacitors and voltage injection transformers for noise-cancellation is the same as that of noise current sensing. Another implementation of DM noise mitigation is to use a low-voltage MOSFET in series in the line. This was demonstrated in [23, 30] for dc-dc converters. The DM noise current cancellation using capacitors was demonstrated in [26, 29, 49, 53, 68] for dc-dc converters and in [22, 25, 54–58, 70] for ac-dc converters. The CM noise current cancellation using capacitors have been demonstrated for ac-dc converters in [14, 21, 35, 37, 49, 54, 62, 72–75]. For inverters, CM noise current cancellation using capacitors have been demonstrated for ac-dc-ac, dc-ac and other inverters in [16, 19, 38, 39, 48, 65–67, 85]. Capacitors have been used for line and neutral noise current cancellation in [50–52, 84].

The DM noise voltage cancellation using voltage injectors was performed in [27, 28, 76, 81] for dc-dc converters, for CM noise-cancellation in [34, 36, 71] for ac-dc converters. CM noise-cancellation using voltage injectors for CM noise-cancellation was demonstrated in [32, 40, 42–

46, 78, 79] for inverters. In [47], the voltage was injected into the chassis of the motor directly to reduce the CM noise.

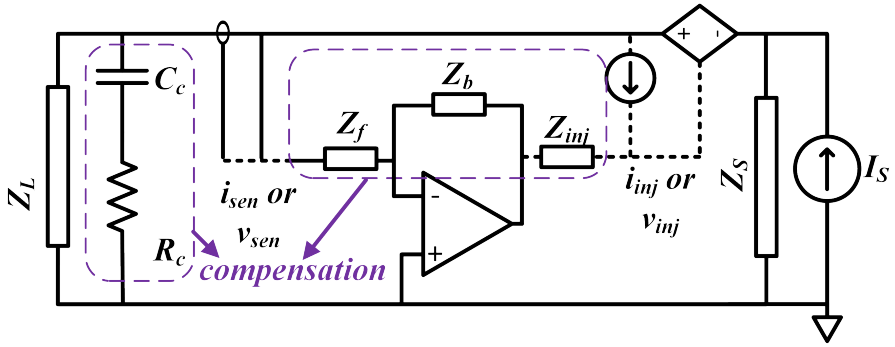

Fig. 2.6: Different compensation methods. The compensation circuit could be an RC network across the lines (R_c and C_c) or could be part of active circuit impedance (Z_f, Z_b) or could be part of the injection stage (Z_{inj}). Either one of these compensation methods could be used with noise current/voltage sensing or cancellation

2.4 Stability analysis and compensation of AEF

The AEF is expected to have a bandwidth of at least 1 MHz. This is to ensure a substantial reduction in the passive component volume. The AEF should be stable throughout the entire frequency range. Low-frequency instability could occur due to resonance between the AEF and the passive component that forms the hybrid filter [25, 34, 58]. In AEF that uses higher-order high pass filters for noise-sensing, the low frequency instability is exacerbated. For high gain AEF, even the first pole of the op-amp used in the active circuit could reduce the phase margin. High frequency instability could occur due to different parasitic components and a second pole of the op-amp present in the AEF [25, 58, 62]. Therefore, stability analysis is crucial for any AEF. Stability analysis is essential to develop the design procedure and come up with a suitable compensation technique for the AEF. Ideally, the compensation needs to be part of the active circuit. While some of the compensation could be added to the op-amp feedback loop, some AEF require additional

compensation that involves high-voltage or high-current elements. So, there is always a trade-off between the stability of the AEF and the possible passive component volume reduction. Because any new component introduced for compensation adds to the volume of the AEF. Various papers have studied the stability analysis of different topologies of AEF and their implementation. Some of the components used for compensation is shown in Fig. 2.6. All the components that are part of the active circuit (Z_f, Z_b *and* Z_{inj}) are low voltage components and do not add to the bulk of the volume. Any series injection impedance (Z_{inj}) used for stability improvement adversely affects the bandwidth and attenuation in case of current-cancellation and voltage-cancellation respectively. Some works use external RC network for stability improvement. While this method does not affect the performance or the bandwidth of the AEF, it adds to the overall passive volume because the C has to be rated for line voltage.

In [17, 82], the stability analysis for DM noise-cancellation using feedback voltage-sense current-cancellation topology for dc-dc converters was carried out. In [53], the stability analysis for DM noise-cancellation using feedback + feedforward current-sense current-cancellation topology for a dc-dc converter was performed. In [20, 59–62], stability analysis for CM noise-cancellation for feedback current-sense current-cancellation topology. Stability analysis was conducted for DM noise-cancellation in [54, 55, 58, 69, 70] for feedback, [56] for feedback + forward, feedforward + feedback and series feedback. In [38, 39], stability analysis for feedback voltage-sense current-cancellation topology for input side CM noise-cancellation in an ac fed three-phase inverter was performed. In [16], stability analysis for feedforward current-sense current-cancellation topology for output side CM noise-cancellation in a dc fed motor drive was carried out. The stability analysis for feedback voltage-sense voltage-cancellation topology for output side CM noise-cancellation in ac fed three-phase motor drive was presented in [44]. The stability analysis for the digital AEF

was presented in [50, 52]. The stability analysis for feedback current-sense current-cancellation topology is presented for CM noise-cancellation in a single-phase grid-tied inverter in [65].

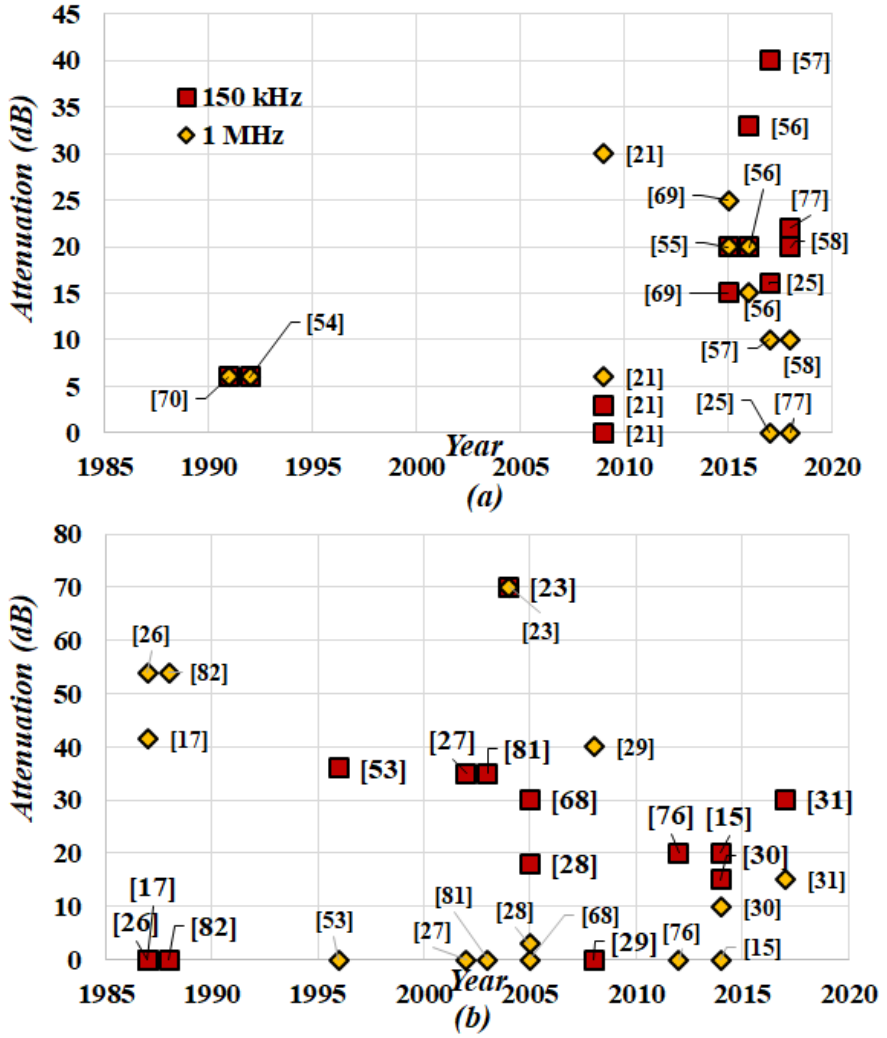

Fig. 2.7: DM noise attenuation provided by active EMI filters for (a) ac-dc converters and (b) dc-dc converters

2.5 AEF Attenuation Comparison of Different Implementations

Consider an LC passive filter whose corner frequency is decided by the noise at 150 kHz. The capacitor in the passive filter is now replaced by a feedback control based voltage-sense current-cancellation based AEF. The attenuation provided by the AEF depends on the gain of

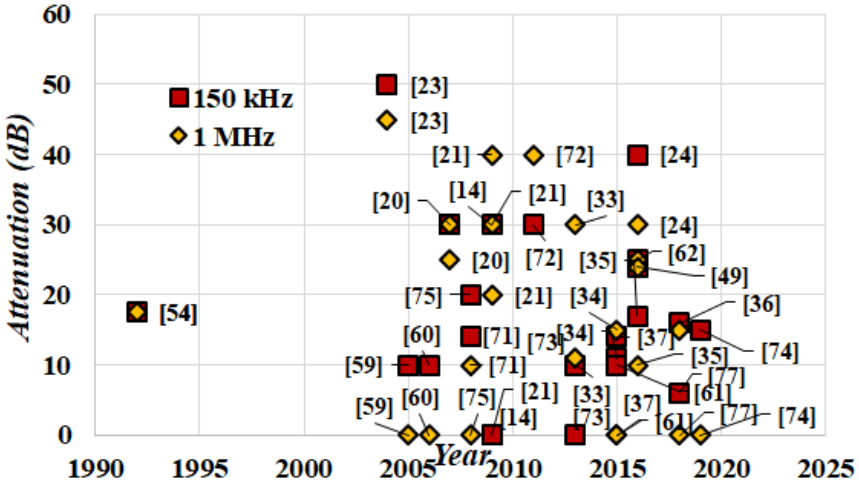

Fig. 2.8: CM noise attenuation provided by active EMI filter for dc-dc and ac-dc converters

the active circuit. If the active circuit is set to a gain of 20 dB at 150 kHz, then the value of the injection capacitor, C_{inj} can be reduced by 10 times while still providing the same attenuation as that of the original passive EMI filter at 150 kHz. Therefore, there is a direct relationship between the attenuation provided and the passive volume reduction. However, there is additional overhead from the components used for noise-sensing and active circuits. Most often, even with these additional components, the relationship between the attenuation and passive volume reduction remains the same.

Therefore, the effectiveness of the filter in minimizing the passive volume could be understood by comparing the attenuation provided by the active stage. Also, the same topology of the AEF performs differently in different converters and for CM and DM noise mitigation. Further, some topologies/implementations of AEF tend to fare well at frequencies lower than 100 kHz and some at frequencies around 1 MHz. For standardization of the comparison, the attenuation of different implementations are made at frequencies of 150 kHz and 1 MHz. And comparisons are made for DM AEF for dc-dc and ac-dc converters separately. This is because the high pass filter required in the sensing stage for ac-dc converters limits the possible attenuation. But, AEF implementations

for CM noise mitigation are similar for both ac-dc and dc-ac converters with the exception of different maximum values for Y-capacitance limited by the leakage current. For inverters (dc-ac and ac-dc-ac), almost all of the works deal with CM noise or line/neutral noise mitigation. Therefore, they are compared together to identify a methodology for maximum attenuation.

2.5.1 Attenuation comparison of AEF in dc-dc converters and ac-dc converters

The chart showing DM and CM noise attenuation for dc-dc and ac-dc converters across different literature is shown in Fig. 2.7 and Fig. 2.8 respectively. For DM noise attenuation in dc-dc converters, the highest attenuation reported in the literature is 70 dB at 150 kHz [23]. However, this implementation uses a series MOSFET to provide attenuation to DM noise and therefore suffers from 1% to up to 10% loss in efficiency depending on the input voltage levels of the converter. If there is no attenuation required at 150 kHz, attenuation of the order of 40 dB and above is possible [17, 26, 82] at 1 MHz. However, around 150 kHz, the highest attenuation reported is of the order of 35 dB [27, 53, 81] which used a combination of feedforward and feedback topologies to accomplish this. For ac-dc converters, the converters with and without PFC needs to be considered for comparison. This is because, for converters without PFC (power factor correction), the input current is spurious in nature and therefore requires special considerations [25]. For ac-dc converters with PFC, the highest attenuation reported is 40 dB around 150 kHz. This implementation uses a series of two feedback current-sense current-cancellation topology [57]. For converters without PFC, the highest attenuation around 150 kHz is 16 dB using a feedback voltage-sense current-cancellation topology [25]. Attenuation of about 30 dB reported in [21] is the highest attenuation at 1 MHz for ac-dc converters with PFC. For CM noise mitigation, the highest attenuation of about 50 dB around 150 kHz was reported [23]. However, it is not clear how much of the attenuation

is from the active stage itself. An attenuation of around 40 dB at 150 kHz was reported in [24] . However, only small-signal tests were performed in this case. In [20, 21], an attenuation of about 30 dB around 150 kHz was demonstrated for ac-dc converters. In [62], an attenuation of 24 dB around 150 kHz was demonstrated in a dc-dc converter using feedback current-sense current-cancellation topology. At 1 MHz, many works including [14, 21, 71] have reported an attenuation of around 30 dB for both ac-dc and dc-dc converters with different feedback topologies of AEF.

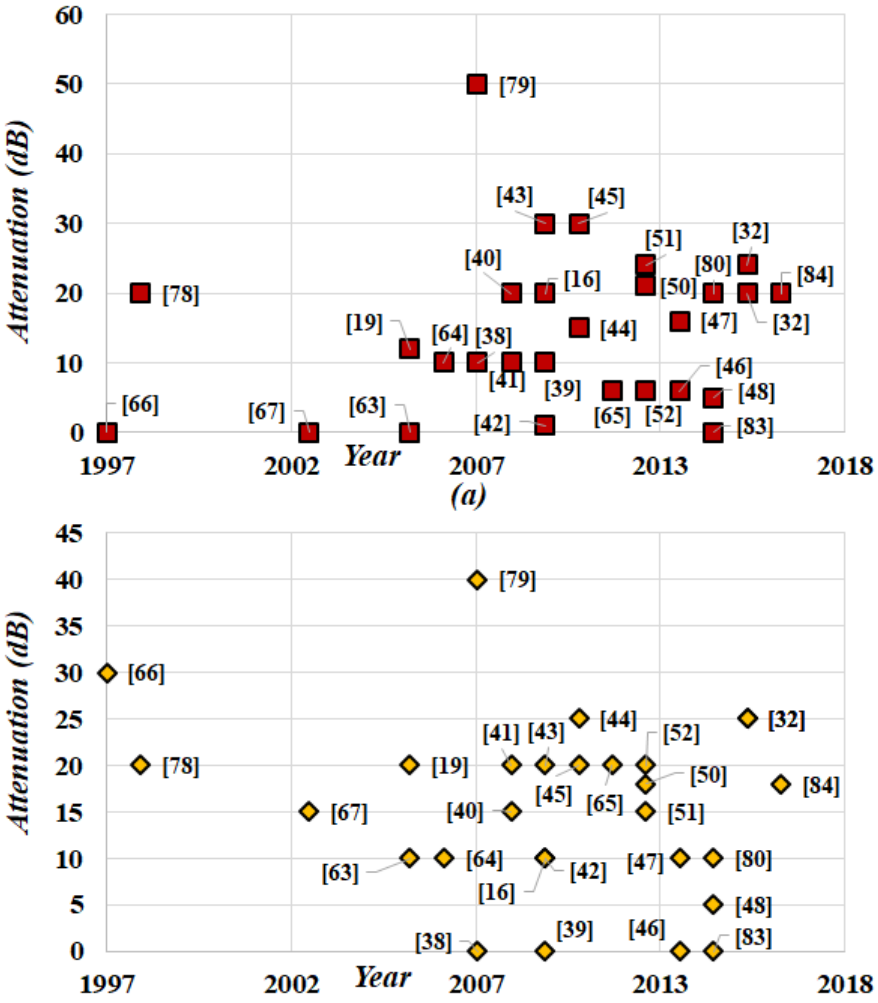

Fig. 2.9: CM/Line noise attenuation provided by active EMI filters at (a) 150 kHz and (b) 1 MHz for inverters

2.5.2 Attenuation comparison of AEF in Inverters

The chart showing attenuation for CM and line noise for inverters across different literature is shown in Fig. 2.9. For inverters, it was proposed to use an additional phase leg (referred to as 4^{th} leg) in an inverter for CM noise reduction in [79]. The work observed the CM voltage at the output of the inverter and reported a 40 dB reduction. But, there were no noise measurements that were made in the system to verify if this CM voltage reduction translates to actual noise reduction. Using low-voltage circuitry (capacitor to block the dc or fundamental frequency voltage), the highest attenuation for CM noise attenuation at the three-phase output is 30 dB around 150 kHz. This was demonstrated in [43, 45] using feedforward voltage-sense voltage-cancellation topologies. At 1 MHz, the highest reported attenuation is 30 dB [66] using feedback current-sense current-cancellation using high-voltage BJTs. Using low-voltage circuitry, [44] has demonstrated attenuation of the order of 25 dB using feedback voltage-sense voltage-cancellation topology.

2.6 Power loss in AEF

The power source and power loss associated with the active circuit are important. Because the additional components for the auxiliary power supply increases the associated power loss and the cost involved in the implementation of the AEF. The losses in the AEF consists of three parts. First is the constant power or standby power in the active circuit. Second is the power loss associated with driving (output) the cancellation current or voltage in the active circuit. Third is the power loss in the additional passive elements used for noise-sensing and compensation to improve stability. Usually, the loss involved in the driving stage dominates when compared to the standby power and passive losses. Further, higher the noise attenuation, the active circuit with higher driv-

ing capability is required and therefore incurs higher power loss.

In ac-dc converters and dc-dc converters, it was demonstrated that either the source voltage [53, 82] or output dc voltage [15] along with voltage regulators could be used for providing power to the active circuit. In inverters, the DC link [48, 66, 78, 79, 83] or capacitive voltage divider on the DC link [19, 67] could be used to power the active circuit. Besides these, most of the works demonstrated the AEF using auxiliary power supplies that were external to the system and do not quantify the power loss.

In [23], the AEF used a series MOSFET for DM noise attenuation. But, it suffered from a 1% to 10% loss in efficiency in dc-dc converters up to 600 W and the losses change with the input voltage. In [14], the AEF resulted in a 1.4% reduction in efficiency when used in a 600 W SMPS (switch mode power supply). In [43, 45] the power loss in AEF is studied in detail for application in a motor drive. At 1.52 kW, the AEF had a loss of about 1.9% which reduced to 0.5% at 20 kW. So, as the power level scaled up, the contribution of AEF towards the power losses reduces. In [58], the power loss from the auxiliary power supply, the AEF circuit and leakage current increase by the added capacitance were taken into account. It was found that the AEF saw a total power loss of about 2.3 W which resulted in a decrease in 0.66% lowering of efficiency at full load in a boost PFC at 350 W. At lower power levels the efficiency took a greater hit. In [36], a power loss of 288 mW was reported when AEF was used in a 2.2 kW current source inverter. This is negligible compared to the inverter power level. However, the attenuation provide by the AEF is only 6 dB around 150 kHz. In [74], a power loss of 310 mW was reported in a 200 W SMPS which is around 0.15% of the efficiency at full load for a 15 dB attenuation around 150 kHz.

2.7 Protection for AEF

Depending on the topology of the AEF, either the sensing or injection stage may be connected to the grid. The AEF should be resilient to the grid voltage transients or current transients due to the operation of the converter. Some literature has demonstrated techniques using galvanic isolation for both noise-sensing and cancellation. In a few other literature, additional components for protection are added when using AEF topologies without galvanic isolation. A CM AEF that has galvanic isolation from the grid using CT for current sensing and a transformer for voltage injection for use in an SMPS was presented in [71]. Also, [36] presented a CM AEF topology that does not use transformers for a resonance current inverter. This work uses capacitors for both sensing and noise-cancellation and uses a varistor on the noise-sensing side and TVS diodes on the noise injection side to implement the protection for the AEF. Another isolated topology that utilizes current-cancellation was proposed in [74]. This work uses a CT for noise current sensing and uses another transformer to inject voltage in the current injection branch. This way both the input and output of the active circuit have galvanic isolation from the mains voltage.

2.8 Conclusion

There are numerous AEF implementations for conducted EMI mitigation in power electronic converters. Different implementations of the AEF topologies have been summarized based on the noise-sensing, noise processing active circuits, the control methods, noise-injection and stability studies for dc-dc, ac-dc converters, and inverters (dc-ac and ac-dc-ac). Different sensing and cancellation methods have different advantages and disadvantages for implementation in terms of volume reduction. Careful attention must be paid to the stability, which depends on the

type of converter and the type of noise in order to select the appropriate AEF. Only then the attenuation and possible volume reduction with AEF could be maximized. The key points in terms of performance (attenuation), power loss and protection of AEF are as follows. Looking at the performance comparison, it is more challenging to achieve high attenuation at lower frequencies (around 150 kHz) using AEF than to design the filter for high attenuation at 1 MHz. For DM noise-cancellation in ac-dc converters without PFC, [25] reported highest attenuation of 16 dB around 150 kHz using feedback voltage-sense current-cancellation topology. For ac-dc converters with PFC, [57] achieves an attenuation of 40 dB around 150 kHz with multiple feedback current-sense current-cancellation topologies. For CM noise-cancellation, attenuation of around 24 dB was achieved using feedback current-sense current-cancellation topology for dc-dc converters. For output CM noise-cancellation in inverters, feedforward voltage-sense voltage-cancellation topologies to achieve an attenuation of about 30 dB around 150 kHz was demonstrated in [43, 45].

However, majority of these implementations uses additional high-voltage passive elements for compensation to ensure stability or rely on inductors either in the form of CTs for noise-sensing or voltage transformers for noise-cancellation. Novel methods that could further enhance the performance of the filter without the need for additional high-voltage capacitors for stability improvements or injection transformers on power lines are required. These new topologies could use all analog or hybrid analog and digital active circuits. Further, there only have been few works that studied the auxiliary power supply, power loss and protection for the AEF to enable widespread adoption. Further, a Figure of Merit (FoM) for implementation of AEF taking into account the volume reduction of passive components at different power levels and for different power converters is an important one that requires further research.

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3 Modeling and Design of Voltage Sensing based Differential Mode Active EMI Filters for ac-dc Power Converters without PFC

3.1 Abstract

Passive EMI filters are bulky and are a major bottleneck to achieve high power density particularly in the current Wide Bandgap devices era. Active EMI filters offer a solution to this problem and help reduce the volume of the passive elements in EMI filters. This paper presents the modeling and design of voltage sensing based active EMI filter for an ac-dc converter. The major bottleneck that limits the performance of the filter is identified as the phase shift introduced by the noise sensing stage which causes low-frequency instability. The trade-off between the low-frequency stability and the high-frequency attenuation are discussed. The design guidelines to choose the optimal gain of the active EMI filter and compensation to ensure the stability of the active EMI filter is presented. The limitation of using conventional compensation methods is identified and suitable compensation methods are selected. The model is verified by both small signal and in-circuit experimental results.

3.2 Introduction

Power converters generate conducted and radiated EMI due to the switching action of the power semiconductor devices. The passive EMI filter used to mitigate the noise is bulky and could occupy up to 30% total system volume. Active EMI filters and Hybrid EMI filters (active + passive) have been shown to reduce the volume of the filters by up to 75% [1]. Different active EMI filter topologies are possible based on noise sensing methods, noise cancellation methods and con-

trol schemes. Various previous works including [3-10] have studied the selection and suitability of active EMI filter topologies. Active EMI filters have been designed for separately for DM [9-15] and CM noise attenuation [3, 17-31] or together [1, 7-8] for both CM and DM noise attenuation. The factors for selection of a particular topology mainly depends on the noise source and load impedance and how the active EMI filter maximizes the impedance mismatch between them [3,5-7].

TABLE 3.1: Comparison of active EMI filters in this work and literature for DM noise attenuation (FF - Feedforward, FB - Feedback, V - Voltage, C - Current, eg. VSCC - Voltage Sense Current Cancellation, Multiple - combination of FF and FB

Reference	Converter	Topology	Noise Sensor	Noise Injection
[2]	30 W DC-DC	FB VSVC	Capacitors	Transformer
[8]	600 W AC-DC with PFC	Multiple	Capacitors & CT	Transformer & Capacitors
[11]	230 W DC-DC	FF CSCC	Rogowski coil	Capacitors
[12-14]	360 W AC-DC with PFC	Multiple	CT	Capacitors
[15]	Small signal only	FB CSCC	CT	Capacitors
[16]	230 W DC-DC	Multiple	Capacitor	Transformer
This work	30 W AC-DC w/o PFC	FB VSCC	Capacitor	Capacitor

After a particular topology is selected, the implementation could be carried out using different methods. Previously, noise current sensing was employed using Rogowski coil [11] and current transformers [3,7-8, 11-13,18,20]. Noise voltage sensing was carried out using capacitive voltage dividers by several authors [1-3, 13, 17, 21-23, 27-31]. Current-cancellation was implemented using capacitors in [1, 3,9-12,14-15,17,24-26,27-32] and voltage cancellation was carried out using voltage injecting transformers [2, 9, 15-16, 18-20]. Control schemes for the active EMI filters reported previously by different authors include feed-forward control scheme [3,11,24,27-30] and feedback control scheme [1-3, 9-10, 12, 14-16, 20, 25-26, 30-31]. A combination of both

feed-forward and feedback schemes in [13, 16-17]. Active EMI filters and hybrid EMI filters were applied to common mode and differential mode noise attenuation in dc-dc [2, 11, 17-18, 23-24] and ac-dc [1, 8-10, 12-15, 19-20] converters and dc-ac [3, 21-22, 25-32]. The main metric for application of active EMI filters is the passive volume reduction.

A summary of major works for DM noise attenuation in previous literature is presented in Tab. 3.1. All the previous works either involve dc-dc converters or ac-dc converters with PFC (power factor correction). Also, the original high voltage passive element (X-capacitor and inductor) would be replaced with multiple high voltage/high current components. These components are used for noise sensing, cancellation and compensation to improve stability. Nonetheless, overall volume reduction of up to 50% was achieved [14]. The most commonly used topology for DM noise cancellation is feedback control based current sense current cancellation [11-13] topology. In this topology, a second order high pass filter including a Current Transformer (CT) is used for noise current sensing. For a non-PFC converter, the CT required to sense the noise will be bulkier than for a converter with PFC stage. This is because of the spurious nature of the rectifier input current.

The contributions of this paper are as follows. Active EMI filter design methodology from literature cannot be applied to ac-dc converters without PFC due to the spurious nature of the input currents. Thus new design methodology for active EMI filter that uses less number of high voltage/high current components need to be developed for non-PFC ac-dc converters. Firstly, this paper presents the selection of the active EMI filter topology. Then, the individual sub-circuits are modeled in detail. Based on this modeling, design procedure is presented in the form of a flowchart. The design procedure involves deciding the loop gain and suitable compensation methods to optimize the volume reduction without the need for too many high voltage/high current

components. The model and design procedure are verified using small signal as well as experimental results in a power converter. The volume reduction of passive components using the active EMI filter is summarized.

The organization of the paper is as follows. Section II involves the DUT, suitability of selected topologies for DM noise attenuation and volume reduction is discussed. In section III the modeling and design of individual sub-systems is laid out and models are developed and small signal measurements of individual sub-circuits are carried out. In Section IV the modeling and stability analysis of the active EMI filter is carried out. Section V presents the small signal measurements of the insertion loss and the impedance with and without active EMI filter. Section VI presents the description of the noise measurement setup and the experimental results with and without the active EMI filter and provides comparison of the volume of active EMI filter components with that of the passive filter. Section VII presents the conclusion of this work.

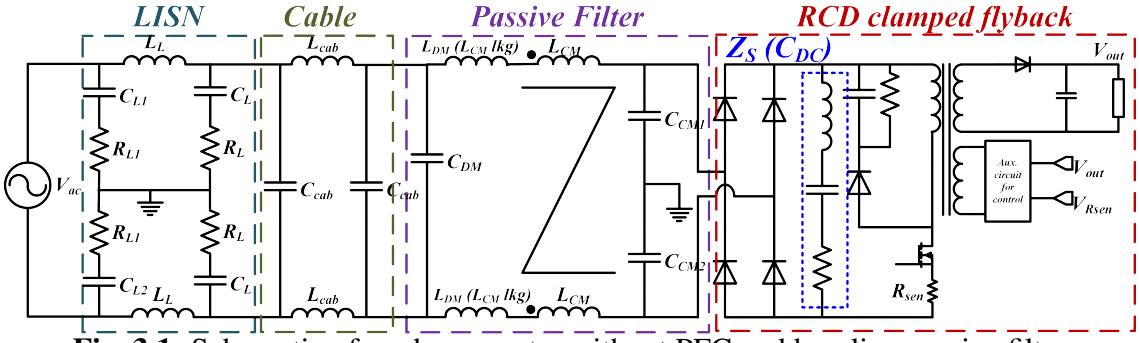

Fig. 3.1: Schematic of ac-dc converter without PFC and baseline passive filter

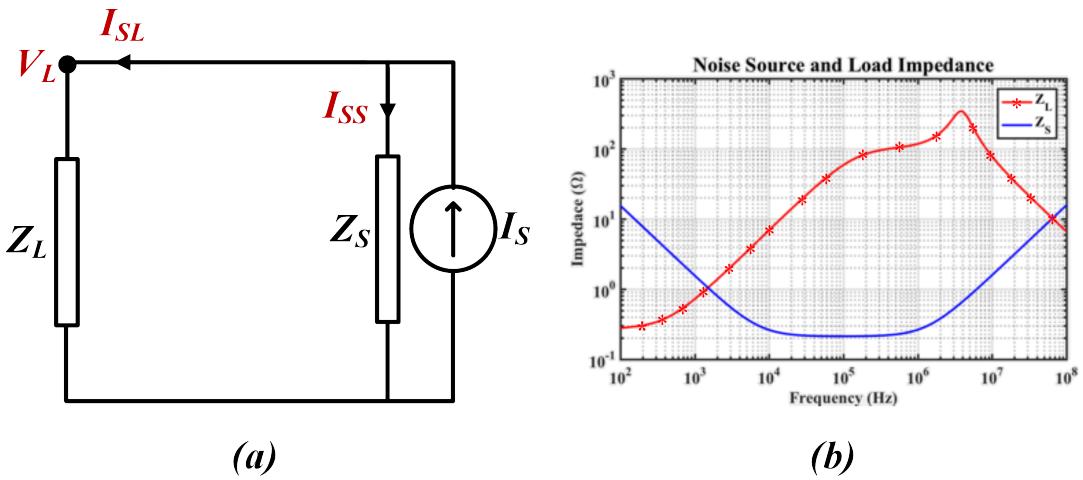

Fig. 3.2: (a) DM noise Norton equivalent circuit (b) Measured Z_S and Z_L impedance

3.3 DUT and Suitability of Active EMI Filter Topology

3.3.1 DUT and Baseline Passive EMI Filter

The schematic of a typical ac-dc converter without PFC (RCD clamped flyback converter) with passive EMI filter is shown in Fig. 3.1. The ripple voltage across the dc-link C_{DC} is the noise source voltage. The ripple voltage comprises of two components. The 120 Hz ripple (2 x f_o) and harmonics of the switching frequency, f_{sw}. This voltage divides between the cable connecting the power adapter and the LISN when the diode bridge is conducting. For demonstration of the active EMI filter, a 30 W commercial desktop power adapter from Meanwell [34] is chosen as the DUT. In the DUT, the DM filter consists of a 120 μH leakage inductance of the CM choke and an X-capacitor of 470 nF. The converter employs spread spectrum around 65 kHz of switching frequency. The passive filter provides an attenuation of about 32 dB around 200 kHz and it ensures the DM noise is below the standard throughout the entire frequency range. The active EMI filter should be able to provide the same attenuation for while having lower volume than the original passive components.

3.3.2 Active EMI filter Topology Selection for ac-dc converter DUT

The Norton equivalent circuit representing the noise source (the converter) and the LISN is shown in Fig. 3.2a. The current source represents the converter, and Z_S and Z_L denotes the noise source and load impedance respectively. Z_S represents the impedance of the DC link capacitor and Z_L represents combination of the load and input cable. These impedance are shown in the Fig. 3.2b. In [3, 5-6] the insertion losses with different topologies of filters based on the gain of the active stage, noise source and load impedance are identified. The active EMI filter could either enhance the inductor (voltage cancellation topology) or capacitor (current cancellation topology). Therefore, the possible topologies of hybrid EMI filters that can be used here are:

1. Feedforward voltage sense voltage cancellation (active L_{DM}) + C_{DM}
2. Feedback voltage sense voltage cancellation (active L_{DM}) + C_{DM}
3. Feedforward current sense current cancellation (active C_{DM}) + L_{DM}
4. Feedback current sense current cancellation (active C_{DM}) + L_{DM}

Feed-forward vs. Feedback

In order to implement feed-forward active filter, the amplifier stage should have unity gain for good noise attenuation. This is difficult to achieve especially because of the parasitics in the sensing and voltage injection components. The feedback active EMI filter implementations require high gain for better attenuation. While this poses risk for instability, compensation network using relatively small passive components can be implemented to ensure stability. Therefore, feedback topology is adopted here and options 1 and 3 are ruled out.

Voltage sensing vs. current sensing

In current sensing based topology, the current sensor has to be rated for carrying the rated current. In this case, the maximum value of input current is 1.8 A. The number of turns have to be 1 turn on each line to cancel out the CM current [5]. Therefore, the total AT for primary side of the CT is 3.6 AT. Also, the core should accommodate a single layer winding with suitable number of turns that form the secondary of the transformer. Single layer of winding is essential to reduce the parasitic capacitance and ensures high bandwidth of the active EMI filter. Considering a turns ratio of 1:10 for the CT, the core ZW41610TC can be chosen. The volume of this CT is approximately 2010 mm^3. This is comparable to that of the CM choke that is present in the power adapter. Therefore, current sensing based topology does not help reducing the volume of the EMI filter. Current-sensing based active EMI filter topologies are more suitable for PFC based ac-dc or dc-dc converters. An ac-dc converter with PFC and 1.8 A input current would be rated for approximately 150 W and therefore has large passive filters.

In comparison, voltage sensing requires only one high voltage safety rated capacitor (C_{s1}) connected across one of the lines to block the ac line voltage. This capacitor could be used along with low voltage components will be used to formulate the high pass filter for noise sensing. Therefore, voltage sensing based topology is adopted here and option 2 is ruled out.

Voltage cancellation vs. current-cancellation

Voltage cancellation requires a voltage injector (transformer). Similar to the current transformer, because of the nature of input current, voltage injectors will be bulky and will not result in overall volume reduction. Therefore, current-cancellation methodology which requires a high

voltage safety rated capacitor for current injection is adopted here. The schematic of the overall implementation of this filter is shown in Fig. 3.3. L_{DM} serves two purposes here, 1. It enhances the impedance mis-match resulting in improved filter performance and 2. It prevents the active circuit from being loaded by the dc link capacitor. Thus option 4, feedback control based voltage sense current cancellation topology is selected as the topology of active EMI filter.

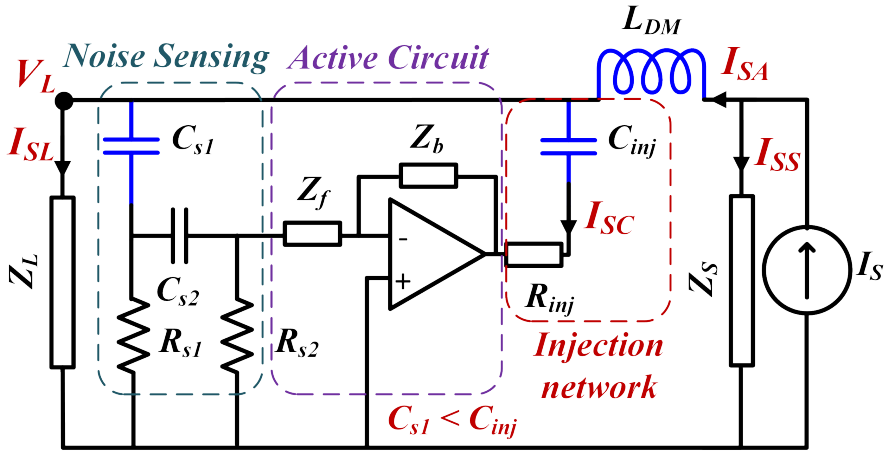

Fig. 3.3: Feedback control based voltage-sense current-cancellation active EMI filter topology

3.3.3 Insertion Loss of active EMI filter topology

For the case without filter, the transfer admittance is given by

$$G_{OL}(s) = \frac{I_S(s)}{I_L(s)} = \frac{Z_S}{Z_N + Z_S} \tag{3.1}$$

The closed loop transfer admittance is given by,

$$G_{CL}(s) = \frac{G_{OL}(s)}{1 + A(s)G_{OL}(s)}) \tag{3.2}$$

The insertion gain is given by the ratio of IL with and without filter is given by

$$IG(s) = \frac{1}{1+A(s)G_OL(s)} = \frac{1}{1+LG(s)} \tag{3.3}$$

$LG(s)$ should have sufficient gain and phase margin to maintain stability. As previously mentioned, Z_N is a DM inductance. At high frequencies, the $Z_N >> Z_S$. In this case,

$$G_{OL}(s) \approx 1 \implies LG(s) \approx A(s) \; and \; IG(s) = \frac{1}{1+A(s)} \tag{3.4}$$

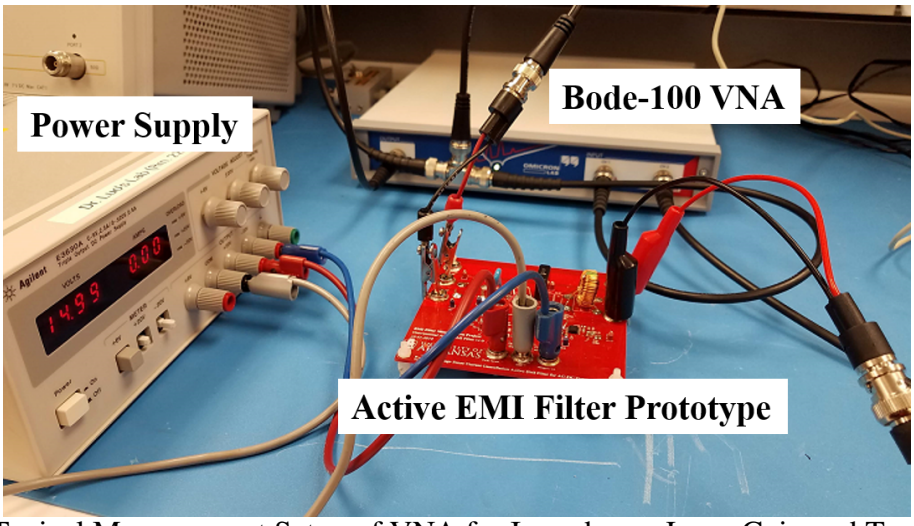

Fig. 3.4: Typical Measurement Setup of VNA for Impedance, Loop Gain and Transfer Gain

3.4 Modeling and Design of VSCC active EMI filter

The modeling of the individual sub-circuits and design guidelines are discussed in this section. This involves the selection of the values of C_{s1}, C_{s2}, R_{s1}, R_{s2}, C_{inj}, R_{inj}, op-amp, Z_f and Z_b such that the overall implementation is stable. The equations of the sub-circuit models are implemented in MATLAB and compared to the experimental measurements. The measurements

are carried out using Bode-100 Vector Network Analyzer. A typical measurement setup is shown in Fig. 3.4. The following are the steps taken to ensure the validity of the models.

1. The results from MATLAB are compared to the experimental measurements in order to verify the validity of the models of individual sub-systems, the loop gain of the filter and the small signal insertion loss (Section III and Section IV).

2. The active EMI filter is tested in the circuit and the resulting noise attenuation is obtained by comparing it to the noise without filter. The loop gain is obtained from the models is compared to the experimental results to further verify the validity of the model (Section V and VI).

3.4.1 Model of the LISN

For DM noise, the equivalent impedance of the LISN and the power cable form the load impedance. Since the power cable is less than 1 m long, its inductance and the stray capacitance introduced is much less than the 100 Ω equivalent impedance of the LISN up to a few MHz. Therefore for simplicity, the impedance of the cable is ignored. Since the active EMI filter is expected to operate at frequencies less than 1 MHz, ignoring the cable impedance does not affect the modeling. The equivalent impedance of the LISN is given by (3.5).

$$Z_L = \frac{s2 * L_L}{2 * R_L + 1/(sC_L/2)} \approx 100\ \Omega \tag{3.5}$$

3.4.2 Model of the Sensing Network

The converter is fed from an ac supply. Therefore, the noise sensing stage has to provide attenuation of the order 80 dB at 60 Hz so that the 60 Hz ac voltage its harmonics, and the high frequency currents due to rectifier are also sufficiently attenuated. Otherwise, any low frequency

harmonic can easily saturate the output of the active circuit. The output of the high pass filter should ideally be switching frequency and its harmonics in the desired EMI frequency range (150 kHz to few MHz). Therefore, the design of the sensing network requires careful consideration to ensure that it:

1. has the desired performance throughout the entire frequency range and
2. it does not add too much to the volume of the filter

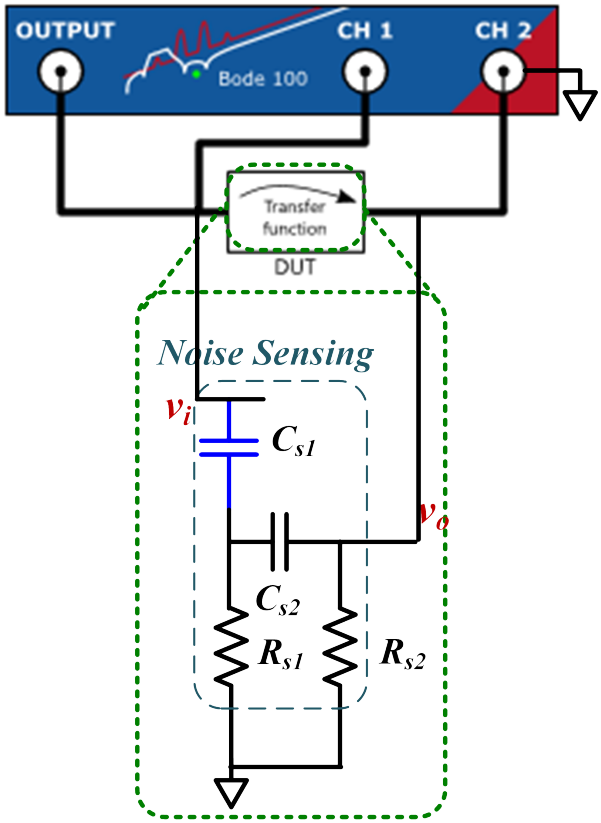

Fig. 3.5: Noise Sensing Network

It is not possible to get around 80 dB attenuation at 60 Hz with a 1^{st} order high pass filter. Therefore a 2^{nd} order high pass filter is used as the sensing network. The schematic of the high pass filter along with the measurement configuration is shown in Fig. 3.5. The capacitor C_{s1} needs to be rated for the input voltage and needs to be safety rated (X1Y1 rated). The other components C_{s2}, R_{s1} and R_{s2} are low voltage and low power components. The capacitor C_{s2} is a 50 V rated

X7R surface mount capacitor. The transfer function of the filter is given by the equation 3.6.

$$T_{HPF}(s) = \frac{s^2}{s^2 + s(1/(C_{s1}R_{s1}) + 1/C_{s1}R_{s2} + 1/(C_{s2}R_{s2})) + 1/(C_{s1}C_{s2}R_{s1}R_{s2})} \tag{3.6}$$

TABLE 3.2: Sensing Network Parameters

Noise Sensing	C_{s1} (pF)	C_{s2} (nF)	R_{s1} & R_{s2} $(k\Omega)$
HPF1	470	10	100
HPF2	4700	10	10
HPF3	4700	3.3	3.3

The design of the filter not only affects the volume but also the design of the active circuit. The same transfer function of the high pass filter can be implemented with different components. The value of the C_{s1} occupies the highest volume among the 4 components. Therefore, the sensing network design has to optimized to achieve lowest volume overall volume while maintaining the required frequency response. Three possible designs as shown in Tab. 3.2 are discussed here. While HPF1 with C_{s1} of 470 pF is desired, it requires 100 $k\Omega$ high frequency surface mount resistors with very low parallel capacitance. Any parallel capacitance from the resistor or the PCB will affect the frequency response of the filter and in turn affect the performance and stability of the filter. If R_{s1} and R_{s2} value and integration could be strictly controlled HPF1 becomes feasible. Even for HPF2 implementation, special 10 $k\Omega$ thin film high frequency resistors are used to ensure the frequency response. Finally, HPF3 is the filter of choice which uses 3.3 $k\Omega$ high frequency resistors. While HPF2 could be realized, HPF3 is more suitable. The reason behind this will discussed in the stability analysis section (Section IV). The frequency response of the model and the experimental measurement is shown in Fig. 3.6.

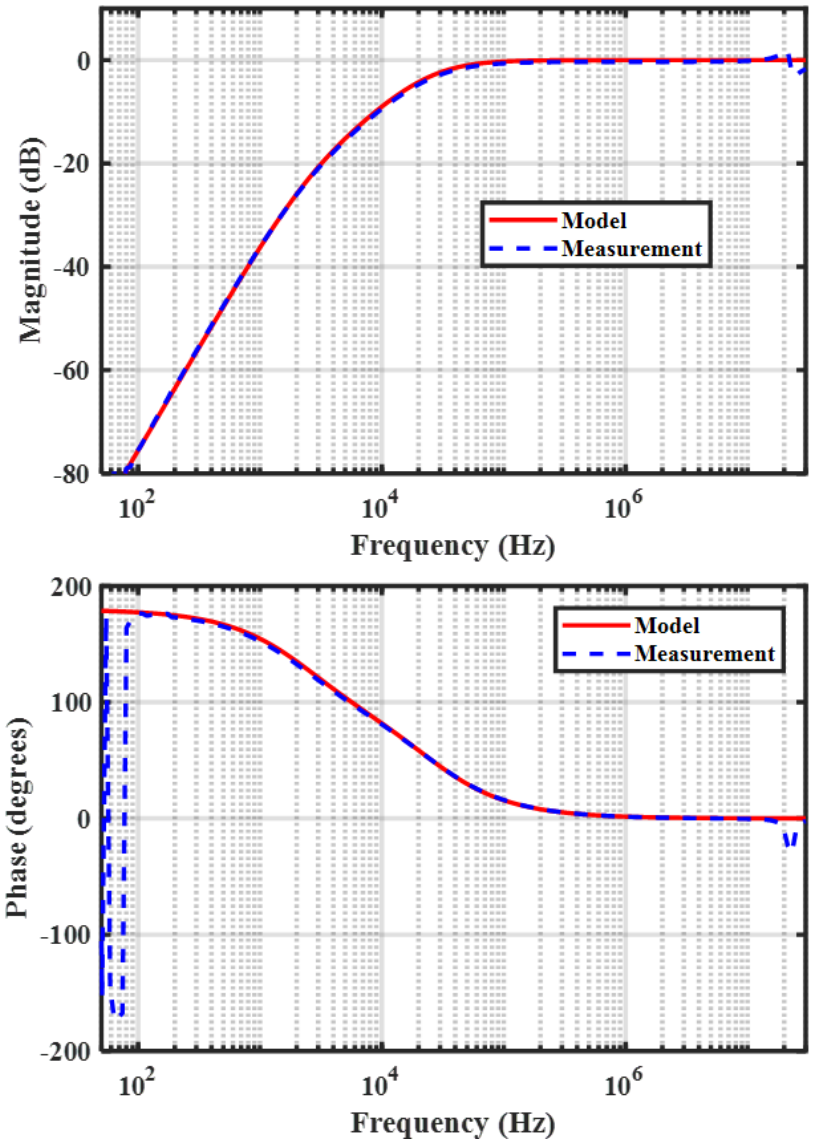

Fig. 3.6: Frequency response of the sensing network HPF3 model vs measurement

3.4.3 Operational Amplifier Circuit

The following are major considerations for the selection operational amplifier (op-amp) for the filter to be implemented in inverting configuration. The conventional considerations for the op-amp are should:

1. Have open loop gain equal to higher than the required gain of the active circuit in the operating frequency range

2. Have gain bandwidth (GBW) greater than the required bandwidth of the active EMI filter

3. Be unity gain stable to ensure high frequency stability

In many previous works that utilize current cancellation topology [11-13], the active circuit consists of two parts. The first part is a low power high bandwidth op-amp that is used to set the gain at different frequencies for the active EMI filter. The second part consists of an amplifier stage that is capable of supplying the high power current. This type of design is required in ac-dc converters at a higher power level where the bare noise level is also high (around 140 dB at 150 kHz). This makes the stability analysis more complex since the frequency response and thermal performance of both the stages need to be carefully designed in order to ensure stability. But, in this work, the DUT is at a power level of 30 W and therefore the noise level is also low (around 80 dB at 150 kHz). Therefore a single op-amp could be utilized for the active circuit. But, there are other special considerations that need to be taken into account because of the 2^{nd} order high pass filter.

The op-amp is configured in the inverting configuration with the output of the noise sensing network connected to the inverting input. Z_f and Z_b represent the two impedance in the inverting amplifier circuit. There are two ways of implementing the gain setting that is required for the ac-

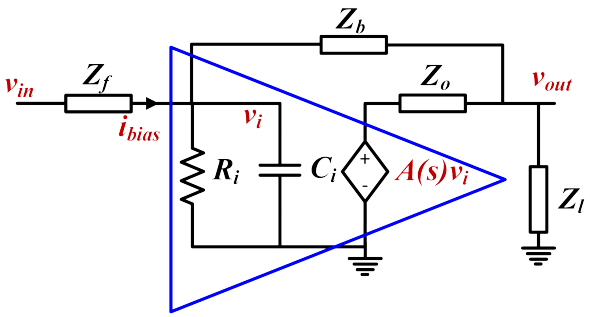

Fig. 3.7: Model of op-amp in the inverting configuration

tive circuit. Select $Z_f >> R_{s2}$ and select Z_b to set the required gain of the active circuit. In case of HPF1, where R_{s2} is of the order of 100 kΩ, Z_f should be at least 1 MΩ to effectively decouple the output impedance of the high pass filter network. This causes another problem. Any input bias current will flow through the Z_f and add to the input offset voltage. This input offset voltage would then be amplified at the output terminal of the op-amp. This reduces the effective output swing and therefore will impact the performance of the filter. And at high temperatures, the bias current combined with high Z_f can cause complete saturation of the op-amp rendering it completely useless. The solution to this problem is two fold. First, instead of decoupling the output impedance of the sensing network from the active circuit, set Z_f to zero. Now, Z_b could be set depending on the required gain of the active circuit. In order to ensure that the bias current does not cause any large voltage offset at the output, a FET input is required. Compared to BJT input op-amps which have bias current of the order of 10s of nA to 100s of nA, FET input op-amps have bias current of the order of 10s of pA throughout the entire operating temperature range. Therefore, in addition to conventional considerations, the op-amp for current cancellation in a ac-dc converter needs to meet the following considerations.

4. Be capable of supplying the required cancellation current and handle the leakage current from the 60 Hz line voltage

5. Low input bias current such that the op-amp does not saturate at high value of DC feedback resistor Z_b

The open loop gain and the output impedance of the op-amp are available in the datasheet [35]. The values from the datasheet are verified by measurements. The open-loop gain is measured based on [36] and the output impedance of the op-amp is measured by configuring it at a known value of closed loop gain [37]. The model of the op-amp could be derived based on the open-loop gain and its output impedance. Following the same procedure, the op-amp OPA828 is modeled. The open-loop gain is around 70 dB at 10 kHz and is capable of supplying up to 30 mA of current and therefore does not require a dedicated current-amplifier circuit. The input bias current is of the order of a 8 pA at room temperature and can be up to 400 pA at 85 ^oC. The active circuit is designed such that the increase in input offset voltage due to the bias current is only 1 μV even at 85 ^oC. This ensures that the the op-amp does not saturate. Also, because the op-amp of choice has FET input, the input resistance ($R_i = 10^{12}\ \Omega$) and capacitance ($C_i = 6pF$) could be ignored. In current-cancellation active EMI filter, the output impedance of is in series with C_{inj}. Therefore, it plays a significant role in the attenuation provided by the filter. It is represented by Z_o. The open-loop gain of the op-amp is represented in 4.13. The model vs. the measured open loop gain is shown in Fig. 3.8.

$$G_{op-amp}(s) = \frac{G_o}{(1+s/\omega_1)(1+s/\omega_2)} \tag{3.7}$$

where, G_o is the open-loop gain at DC and ω_1 and ω_2 represent the gain rollover frequencies. $G_o = 10^7; \omega_1 = 2*5.3\ rad/s; \omega_2 = 2*70\ Mrad/s$

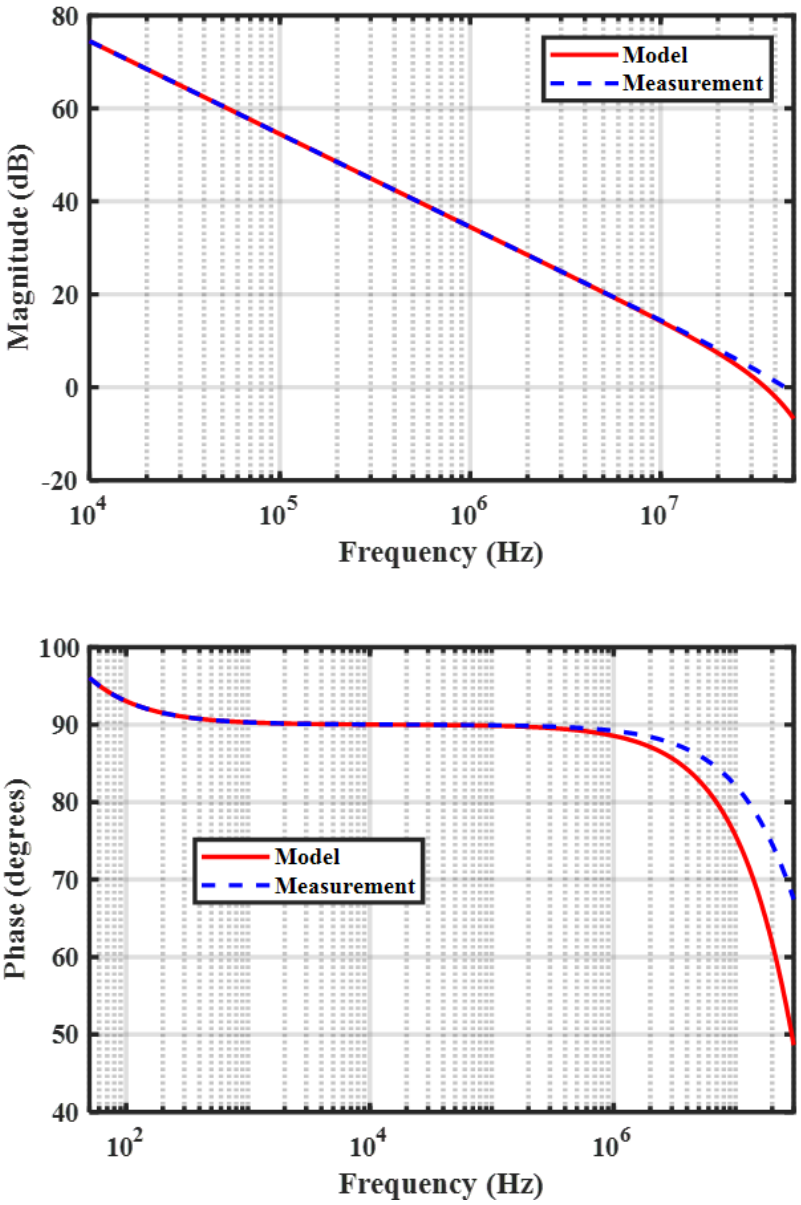

Fig. 3.8: Open loop gain of the op-amp measurement vs. model

The feedback factor of the op-amp in the inverting configuration with the high pass filter and the load is given by the following equation.

$$\beta = \left(\frac{Z_{ff}}{Z_{ff}+Z_b}\right)\left(\frac{Z_l//(Z_{ff}+Z_b)}{Z_l//(Z_{ff}+Z_b)+Z_o}\right) \tag{3.8}$$

$$where, Z_{ff} = Z_f// \left(R_{s2}// \left(\frac{1}{sC_{s2}}+\frac{1}{C_{s1}}//R_{s1}\right)\right) \tag{3.9}$$

The transfer function of the op-amp in the inverting configuration with the high pass filter and the load is therefore given by the following equation.

$$T_{op-amp}(s) = \frac{G_{op-amp}(s)(Z_b+(Z_o//Z_l))}{Z_{ff}+Z_b+(Z_o//Z_L)}\frac{1}{1+G_{op-amp}(s)\beta} \tag{3.10}$$

3.4.4 Model of the Injection Network

The injection network comprises of R_{inj} and C_{inj}. The original C_{DM} capacitor of the passive filter is 470 nF. When active EMI filter is employed, the value of the injection capacitance could be reduced. The transfer function of the injection network is given by 3.11. The selection R_{inj} will be discussed in the stability analysis section (Section IV).

$$Z_{inj}(s) = R_{inj} + \frac{1}{sC_{inj}} \tag{3.11}$$

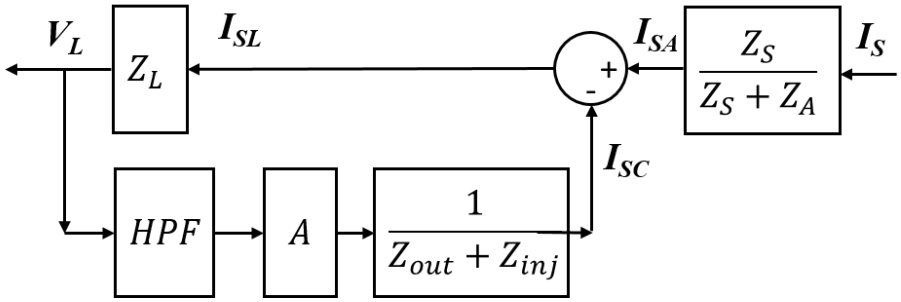

Fig. 3.9: Block diagram of feedback voltage sense current cancellation active EMI filter

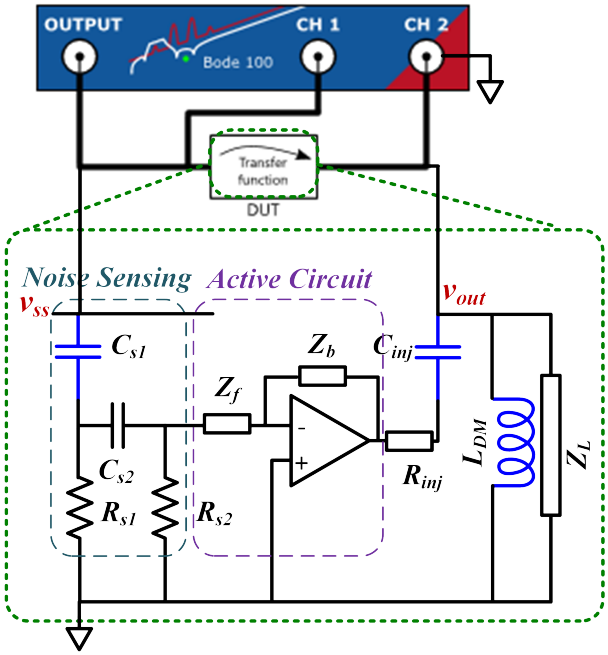

Fig. 3.10: Configuration for loop gain measurement

3.5 Modeling and Stability Analysis

The signal flow graph of the VSCC active EMI filter is given in Fig. 3.9. In order to carry out the stability analysis, the loop is disconnected at the sensing node and a small signal voltage v_{ss} is applied. The high pass filter is in parallel to the LISN impedance and therefore does not affect the loading of the op-amp even when disconnected for loop gain measurement. The voltage across the parallel combination of L_{DM} and Z_L denoted as v_{out} . The loop gain is the ratio of v_{out} to v_{ss}. This can be obtained by the product of transfer function of the sensing network, the inverting op-amp and the voltage divider at the output of the op-amp (Z_{inj} and $Z_L//Z_S$).

$$LG(s) = \frac{v_{out}(s)}{v_{ss}(s)} = \frac{V_{HPF}(s)}{V_{ss}(s)} \frac{V_{out}(s)}{V_{in}(s)} \frac{V_{LISN}(s)}{V_{out}(s)} \tag{3.12}$$

From (5),(9) and (10),

$$LG(s) = T_{HPF}(s)\ T_{op-amp}(s)\ \frac{Z_L//Z_S}{(Z_L//Z_S)+Z_{inj}} \tag{3.13}$$

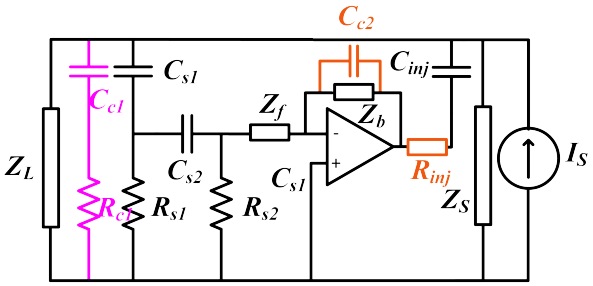

Fig. 3.11: Possible compensation techniques for stability improvements

3.5.1 Feasibility of Conventional Compensation Scheme

The gain of the op-amp is varied by changing Z_f and Z_b to see the condition that the active EMI filter will become stable. As specified earlier, Z_f is set to zero. Now, Z_b has to be adjusted in order to set the required gain. As mentioned in Section II, the gain of the active circuit is going to determine the insertion loss of the active EMI filter. Instability arises both at low and high frequency. Low frequency instability occurs due to the phase shift introduced by the noise sensing network and the due to the roll-off in the gain of the op-amp due to the first pole. High frequency instability occurs to due to other parasitics and 2nd pole in the open-loop gain of the op-amp. For this topology of the active EMI filter, it is impossible to ensure stable condition in low frequency ($<$ 100 kHz) even for very low gains of 6 dB without any compensation. The conventional compensation methods is to introduce a pole-zero pair at that frequency range to improve the phase margin. This could be implemented by using an RC network (R_{c1} *and* C_{c1}) in parallel to Z_s (connected across the line and neutral in the actual circuit) as shown in Fig. 3.11. This would require a safety rated capacitor of the order of 100 nF along with a resistor. Now, the original 470 nF C_{DM1} capacitor needs to be replaced with a C_{inj}, 4.7 nF C_{s1} and a 100 nF C_{C1}. Therefore, this method would not be viable as it would not help achieve volume reduction. Other method to use an LR network across the L_{DM}. This would also require another magnetic component and would also reduce the volumetric benefits of using the active EMI filter.

3.5.2 Compensation Scheme

The proposed compensation scheme realizes two functions:

1. Improves the low frequency stability and

2. Reduces the gain at high frequencies thereby improving the high frequency stability as well

In order to improve the low frequency stability, R_{inj} is used. The R_{inj} in combination of the C_{inj} helps improve phase margin at low frequency. But, using high value of R_{inj} reduces the attenuation of the active EMI filter. However, the noise at around 150 kHz decides the cut-off frequency and therefore the C_{DM} required. So, the gain of the active circuit is set such that the active EMI filter provides attenuation comparable to 470 nF from 150 kHz to a few 100 kHz. Above this, R_{inj} dominates and reduces the effective attenuation of the filter. With the high pass filter, there is nothing that limits the gain at frequencies above a few MHz. This will result in high frequency instability of the active circuit. This helps limiting the gain of the active circuit at high frequencies thus improving high frequency stability. In order to improve the high frequency stability, a gain compensation capacitor C_{c2} is used across the feedback resistance to reduce the gain of the active EMI filter at frequencies above 1 MHz. The flowchart for overall design of the active EMI filter is shown in Fig. 3.12.

TABLE 3.3: Component values in the passive filter and active EMI filter

Component	**Value**	**Ratings**
L_{DM}	120	Leakage of CM choke
C_{DM1}	470 nF	X2 and 275 V
C_{DM2}/C_{inj}	68 nF	X2 and 275 V
C_{s1}	4.7 nF	X1Y1 and 275 V
C_{s2}	10 nF	50 V SMD
$R_{s1}\&R_{s2}$	3.3 $k\Omega$	1/8 W SMD
Z_f	-	-
Z_b	$R_b \,\|\|^{el}\, C_{c2}$	-
R_b	100 $k\Omega$	1/8 W SMD
C_{c2}	470 pF	16 V SMD

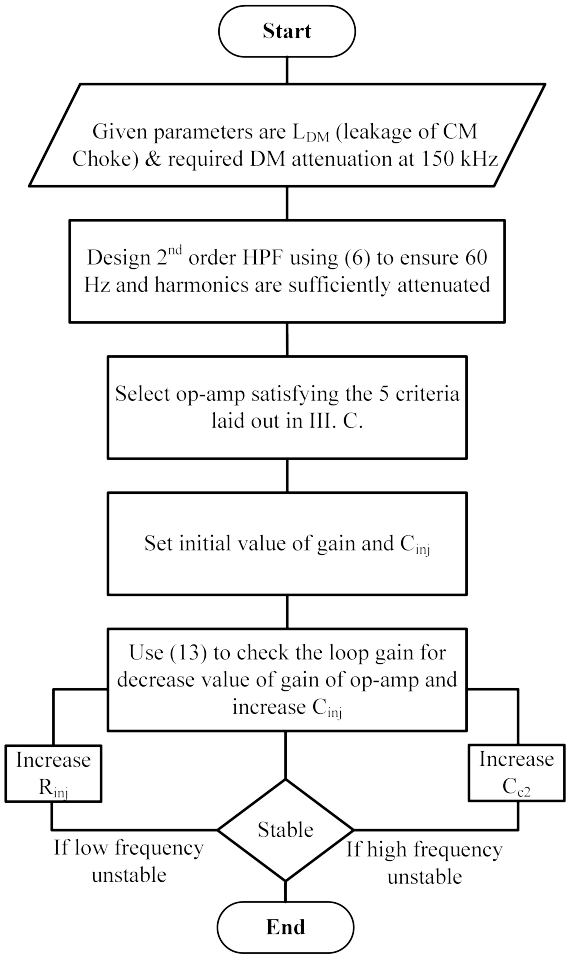

Fig. 3.12: Schematic for experimental testing

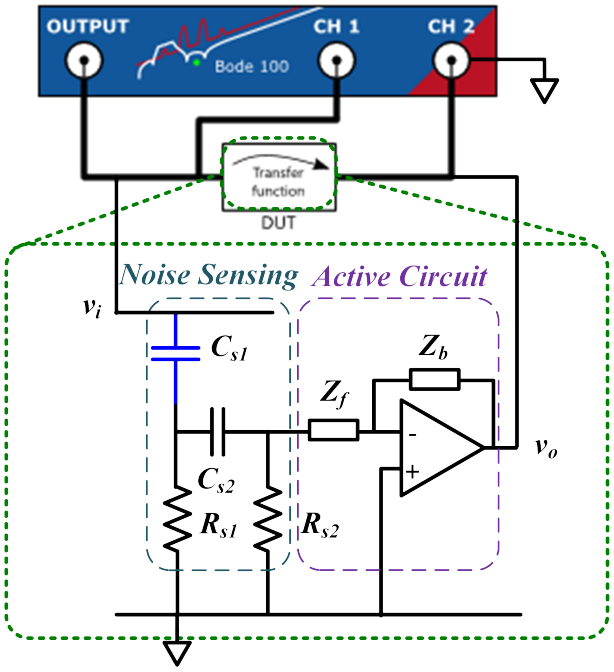

Fig. 3.13: Frequency Response of HPF and Active Circuit measurement configuration

3.6 Small Signal Measurements

The final component values used in the filter are listed in Table. 3.3. Firstly, the gain of the active stage along with the high pass filter is measured. The schematic of the measurement is shown in Fig. 3.13. The measurement result is shown in Fig. 3.14. The measurement and the model shows good agreement up to a few MHz. Next, the C_{inj} and R_{inj} are added to this circuit and the loop gain is measured by disconnecting the HPF at the sensing node. The measured loop gain is shown in Fig. **??**. From the figure, it can be seen that the active EMI filter has about 28 degrees phase margin around 40 kHz and around 80 kHz around 20 MHz. Thus both low frequency and high frequency stability are ensured. The output impedance of the actively enhanced 68 nF capacitor is measured using 1-port measurement of the VNA. This measurement vs. model is shown in Fig. 3.18. Then, the CM choke whose leakage inductance serves as the L_{DM} is connected and transfer gain of the filter is measured. This measurement vs. model shown in Fig. 3.20. From the impedance and the

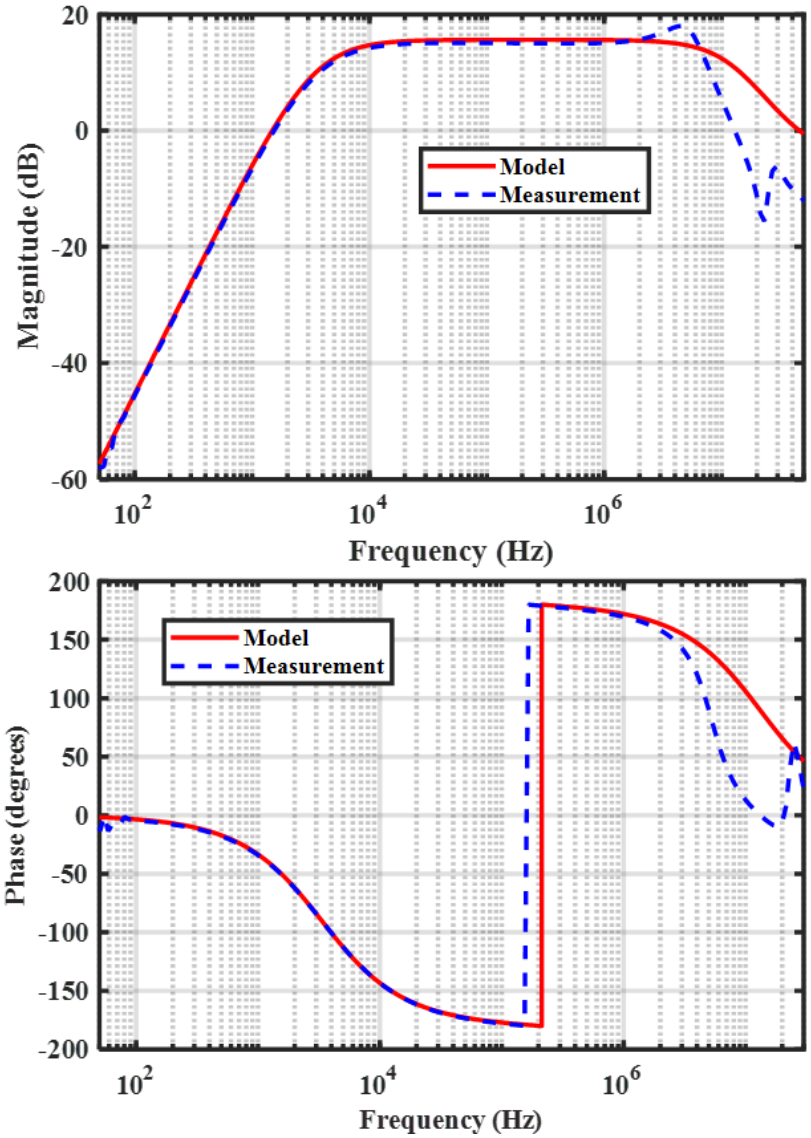

Fig. 3.14: Frequency Response of HPF and Active Circuit

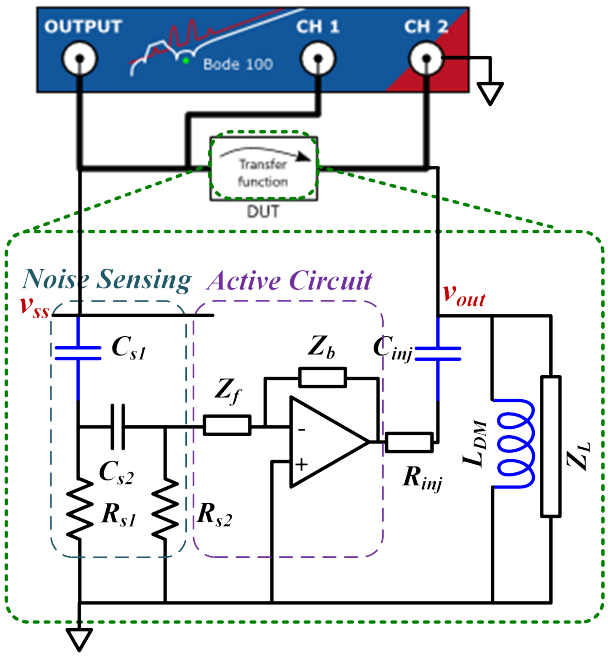

Fig. 3.15: Configuration for measuring loop gain

transfer gain it can be observed that the 68 nF capacitor's impedance is enhanced starting at 5 kHz. This ensures that low frequency harmonics of the ac line frequency and other harmonics from the operation of the rectifier do not saturate the active circuit. The impedance and the transfer gain with the actively enhanced 68 nF is comparable to that of the original 470 nF capacitor up to a few 100 kHz. Above this frequency range, the effectiveness of the active circuit reduces because of the reduction in gain due to the compensation capacitance C_{s2} and R_{inj}. Since the noise at frequency range around 150 kHz determines the values of the filter component required, this is sufficient to ensure that the noise level is below the standard. This will be shown in the next section.

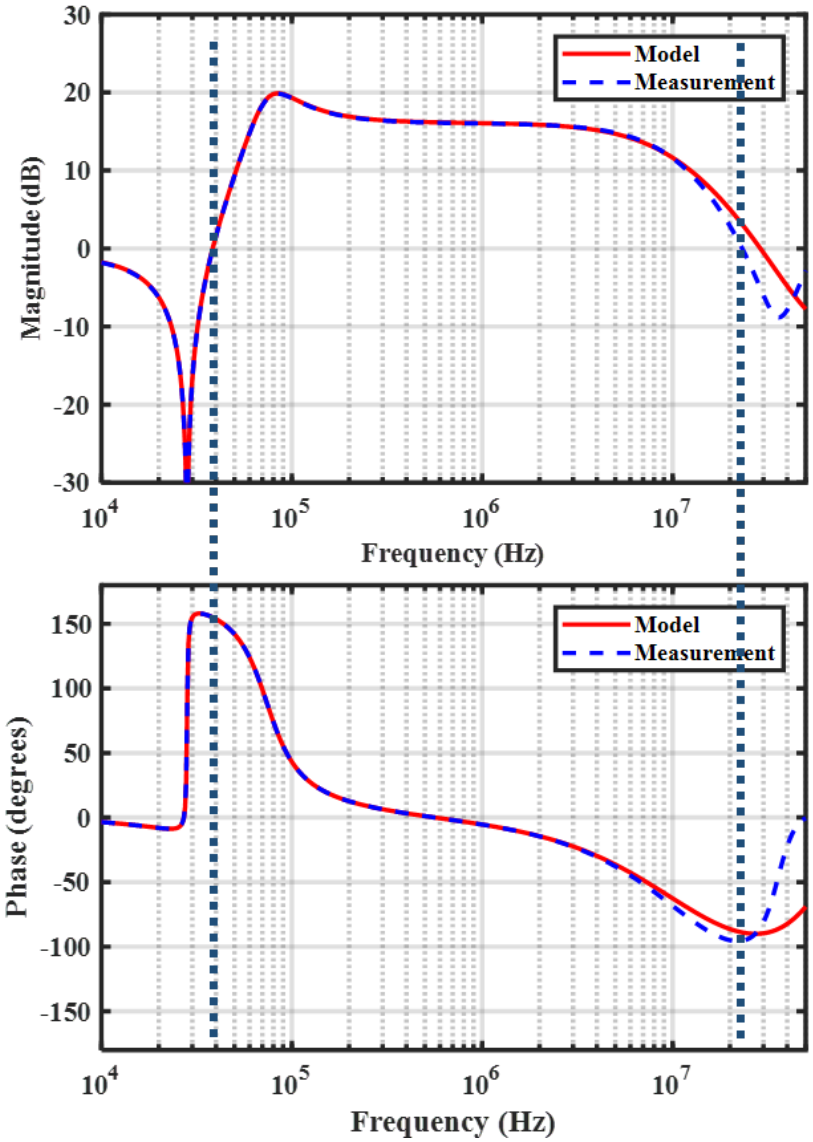

Fig. 3.16: Comparison of loop gain model vs. measurement

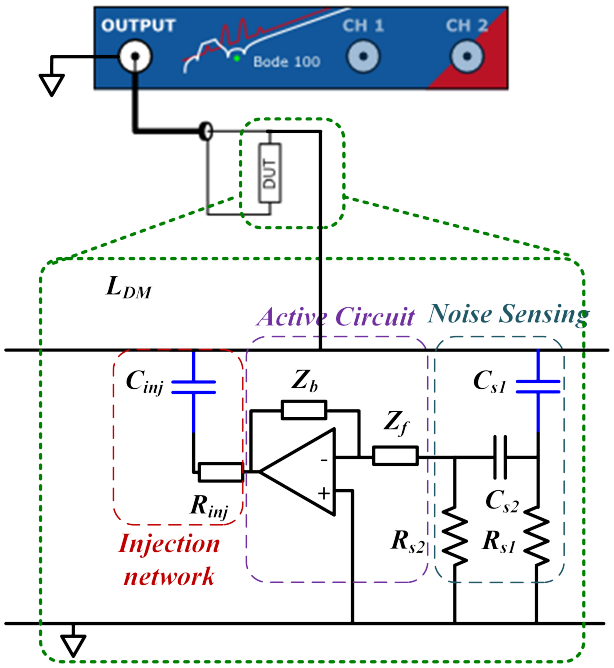

Fig. 3.17: Impedance measurement configuration of C_{DM1}, C_{DM2} and C_{inj} with active EMI filter

3.7 Experimental Setup and Results

3.7.1 Experimental Test Setup

The converter under consideration is a 30 W ac-dc converter. The test setup is done as described in CISPR-16 standard and is shown in Fig. 3.22. The Line Impedance Stabilization Network (LISN) pair used for EMI measurement is COM-Power LI-50A which is designed to carry out measurements for CISPR-22 standard. The differential mode measurements are made using power splitter ZSCJ-2-B+ from Mini-Circuits. The 3-dB bandwidth of the noise splitter covers the conducted emissions frequency range of CISPR-22 standard. The noise measurements are carried out using the Keysight N9038 MXE receiver. The resolution bandwidth, video bandwidth and the dwell times of the EMI receiver are setup as specified in the standard. The 110 V, 60 Hz single phase power supply from the wall outlet is fed to the power converter through the two LISNs. The neutral is tied to the ground at the wall outlet. An external isolated power supply is used to

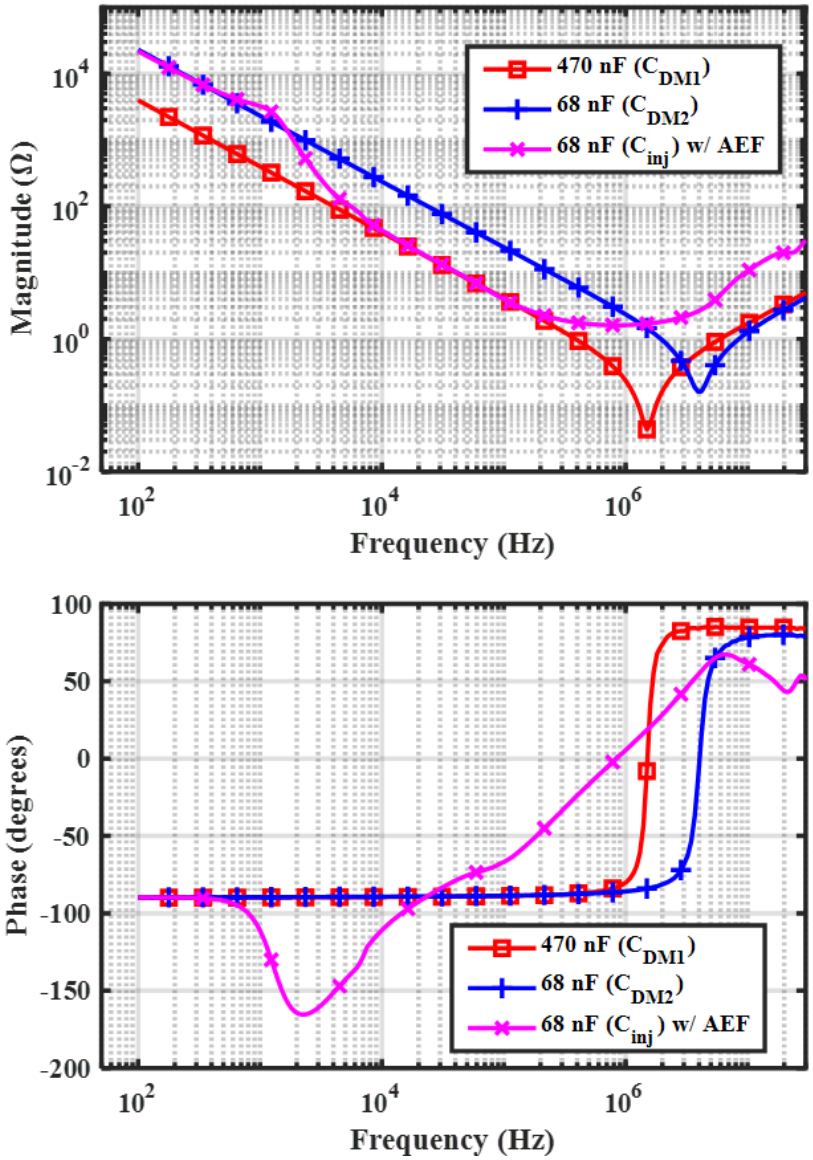

Fig. 3.18: Comparison of measured impedance of C_{DM1}, C_{DM2} and C_{inj} with active EMI filter

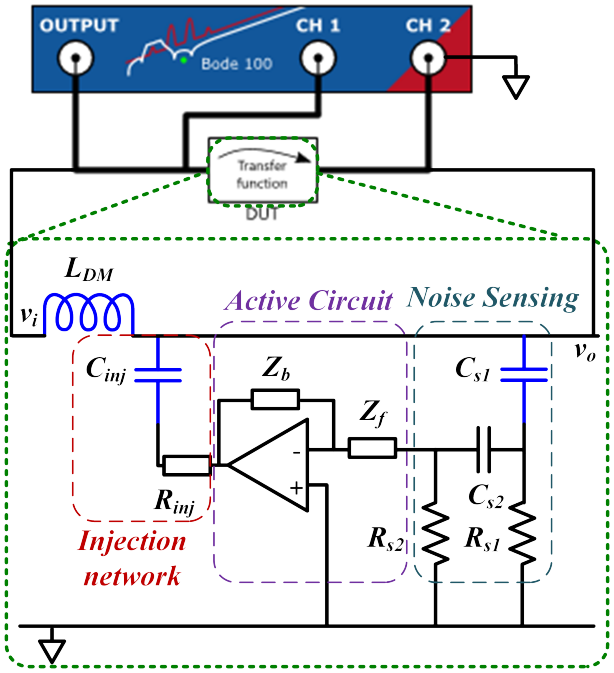

Fig. 3.19: Comparison of measured frequency response of filter with and without active EMI filter

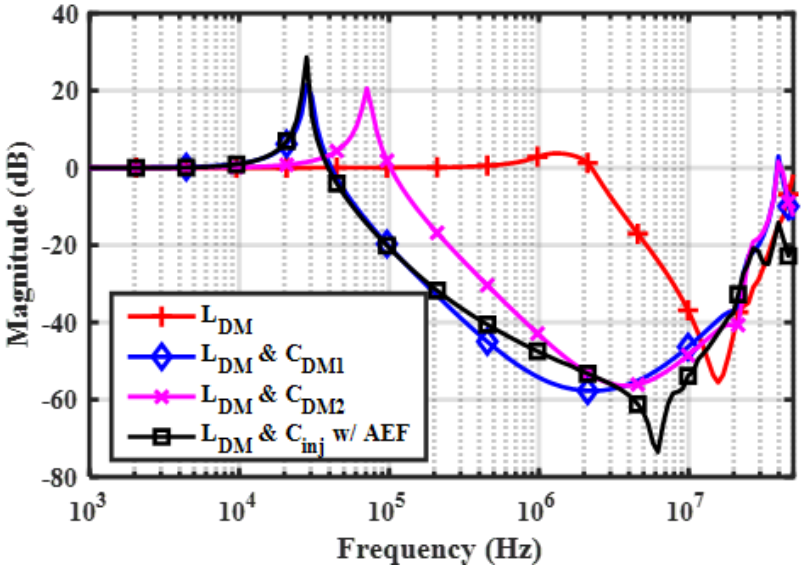

Fig. 3.20: Comparison of measured transfer gain of filter with L_{DM1}, C_{DM1}, C_{DM2} and C_{inj} with active EMI filter

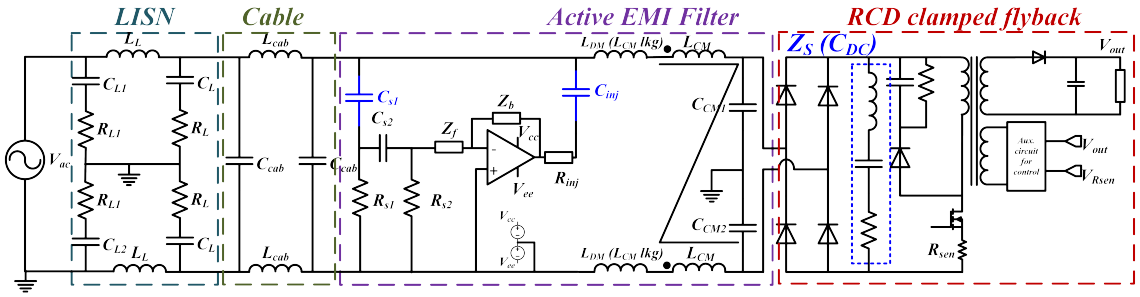

Fig. 3.21: Schematic for experimental testing

power up the active circuit. The active circuit uses the operational amplifier OPA828 from Texas Instruments.

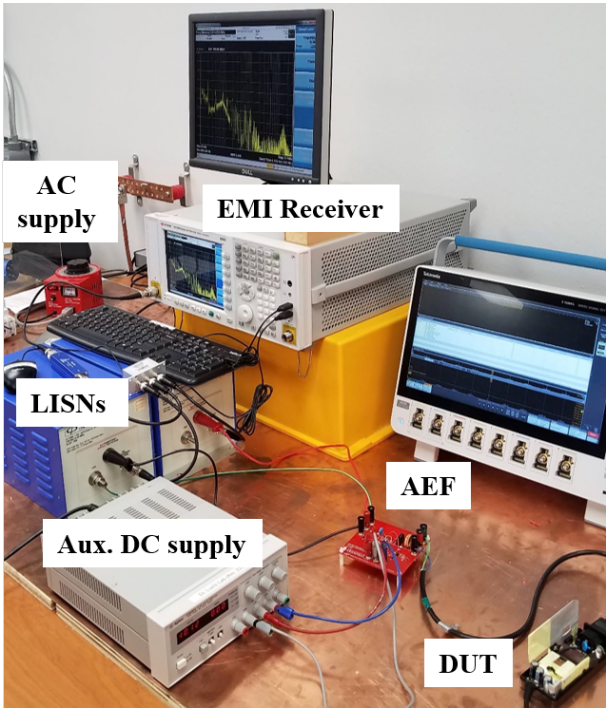

Fig. 3.22: Conducted Emissions Measurement Test Setup

3.7.2 Experimental Results

The noise measurements with the Quasi-peak detector are carried out and the results are shown in Fig. 3.23. From this it can be seen that with the active EMI filter, the attenuation is 16 dB using the same 68 nF capacitor around 150 kHz. Thus the performance of this filter is

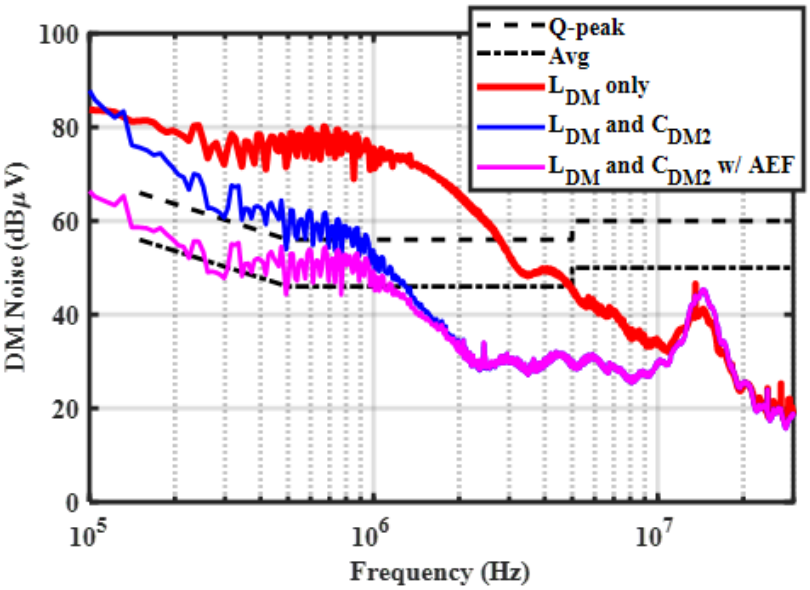

Fig. 3.23: Experimental results - Quasi peak detector

comparable to that of using 470 nF capacitor. The obtained attenuation from the filter is within the expected range. This validates the model obtained earlier. The filter prototype is shown in Fig. 3.24 and the volumetric comparison is summarized in Fig. 3.25. Thus, with a 68 nF capacitor, the equivalent attenuation would be approximately same as using a 470 nF capacitor. The volume of the 470 nF capacitor is 3901 cu. mm. The volume of the 68 nF C_{inj} capacitor 945 cu. mm. The volume of the 4.7 nF high voltage sensing capacitor (C_{s1}) is about 180 cu. mm. Thus, using this topology of active EMI filter, the volume of the X-capacitor has been reduced by about 67%. The filter prototype is shown in Fig. 3.24 and the volumetric comparison is summarized in Fig. 3.25. For low power ac-dc converters, the proposed work achieves two important things. It uses low voltage components for compensation and uses only one high voltage component for noise sensing. Even with one additional high voltage component, a volume reduction of 67% is achieved for the differential mode capacitor.

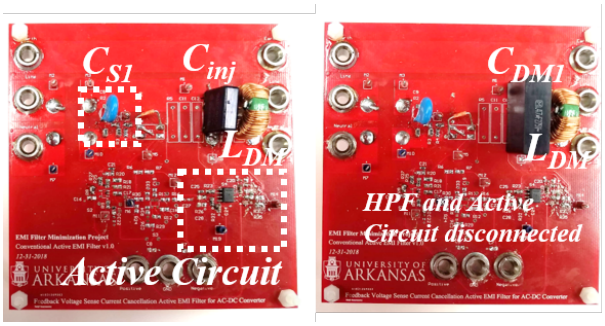

Fig. 3.24: Comparison of Passive Components with and without active EMI filter

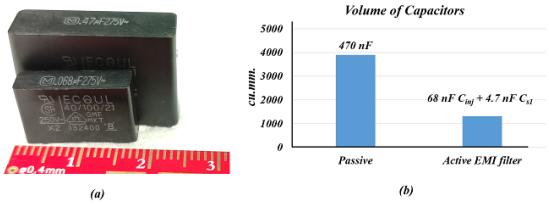

Fig. 3.25: Volumetric Comparison of the Capacitance with and without active EMI filter

3.8 Conclusion

The suitability of different active EMI filter topologies are discussed for the ac-dc converter without PFC is discussed. Because of the spurious nature of the input currents with higher peak values, current sensing or voltage cancellation topologies cannot be used for these converters. The feedback control based voltage sense current cancellation topology uses only high voltage capacitors for noise sensing and cancellation. The individual sub-circuits are modeled in detail. Based on this modeling, design procedure is presented in the form of a flowchart. The design procedure involves deciding the loop gain and suitable compensation methods to optimize the volume reduction without the need for too many high voltage/high current components. Feasibility of conventional compensation scheme was identified and a compensation scheme with better low and high frequency stability that uses only low voltage components is proposed. Small signal measurements are compared to the models in order to show the effectiveness of the models. The filter is tested with power adapter with and the results are consistent with the model and small

signal results.Active EMI filter helps reduce the value of the X-capacitor by about 10 times from 470 nF to 68 nF and the volume of the X-capacitor by 67%.

Acknowledgment

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4 Modeling and Analysis of a Differential-Mode Active EMI Filter with an Analog Twin-circuit

4.1 Abstract

Conventional passive EMI filters are bulky and occupy up to 30% of converter volume and weight. Active EMI filters are a key technology that enables the volume reduction of passive components in the EMI filter. The effectiveness of traditional active EMI filter for volume reduction is limited by the additional overhead from the passive components for noise-sensing and compensation to ensure stability. A novel active EMI filter is proposed and demonstrated for DM noise attenuation. The filter consists of a twin-circuit made up of low voltage/current components that mimic the high-power passive filter components in the main circuit. Unlike the conventional active EMI filter, the proposed filter uses compensation networks which consists of low-voltage surface-mount components only. The modeling of the entire circuit is carried out, and verified with small-signal measurements. The filter is then tested in a converter and the experimental results are shown to be consistent with the model and the small-signal measurements.

4.2 Introduction

Power converters generate conducted EMI noise due to the switching action of the power semiconductor devices. Conventionally, a second-order passive EMI filter is used for noise mitigation to ensure compliance with standards. With the advent of wide-bandgap devices such as SiC and GaN, the power density of the power stages is ever increasing, as demonstrated in the literature [1–3]. While the power density of the power stage increases, the high switching frequency and high

switching speeds of the wide-bandgap devices require careful design of EMI filters to ensure the high power density of the entire power converter. However, the passive components have not kept up with the developments in the power semiconductors area. Therefore, passive EMI filters are a significant bottleneck for power density and could occupy up to 30% of power converter volume and weight.

Active EMI filters are a key technology that will enable high-density passive solutions for the next generation of power converters. Typically, active EMI filters are implemented along with another passive component. This is essential because of the limitation of the bandwidth of the passive components and the active circuits used in the active EMI filter. Using active EMI filters along with a passive component is referred to as hybrid EMI filters. Active and hybrid EMI filters have been shown to reduce the volume of the passive components by over 50% [4–6]. The active EMI filters provide attenuation up to a few MHz, and a smaller passive filter is used to provide high-frequency attenuation. The active EMI filters can be classified based on the methodology of control, noise-sensing, and noise-cancellation mechanisms [7–9]. Previously, active EMI filters using feedforward[7], feedback[6, 10, 11] and a combination of both control techniques [12] have been demonstrated. Also, active EMI filters utilizing a combination of voltage or current sensing and cancellation have been demonstrated [4, 5, 13–15]. Active and hybrid EMI filters have been applied to common-mode (CM) and differential-mode (DM) noise attenuation in both dc-dc [5, 16], ac-dc [6, 10, 13] and dc-ac [7, 17] converters.

Among existing work, transformer-less current-cancellation topologies have been shown to offer higher volume reductions than voltage-cancellation topologies that use a voltage injector. Recently, a summary of different active EMI filters and their implementation of different power converters was presented in [18]. In [18], the need for novel analog or digital active EMI filters

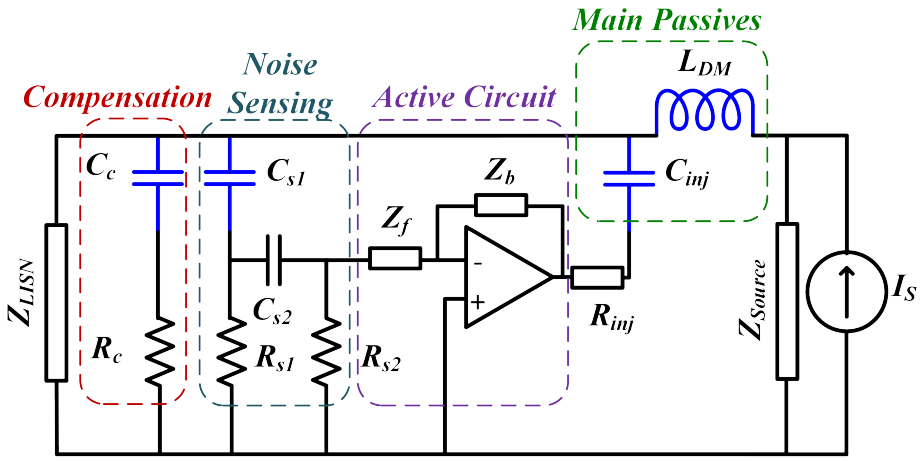

Fig. 4.1: Schematic of typical feedback control based voltage-sense current-cancellation active EMI filter

with improved performance (attenuation) while avoiding additional passive components for compensation was identified. In order to get good attenuation with the feedforward topology, tight control of tolerance of all the passive components is required. Moreover, for the most part, the feedforward topology remains stable.

While the feedback topology is resilient to component tolerances, it is subject to stability issues at low (<150 kHz) and high (>30 MHz) frequencies. Instability at low frequency occurs due to the phase shift introduced by the noise-sensing circuit. High-frequency instability stems from the gain roll-off of the op-amp circuit, and other parasitics in the circuit. In order to ensure stability, damping networks comprising of high-voltage/high-current components are added to the circuit. These components add to the bulk and reduce the benefits of using active EMI filters. The schematic of a typical feedback control based voltage-sense current-cancellation active EMI filter is shown in Fig. 4.1. There are four main parts of the active EMI filter. They are: the noise-sensing circuit, the active circuit (op-amp), the main passives and the compensation network. In [11], attenuation of up to 34 dB around 150 kHz in an ac-dc converter with PFC. using feedback current-sense current-cancellation topology active EMI filter was reported. However, in addition

to the CT (Current Transformer) for noise-sensing, additional high-voltage capacitor (C_C) and resistor (R_C) compensation network to ensure the stability of the active EMI filter. This additional high-voltage compensation network prevents maximizing the volumetric benefit of using an active EMI filter. It was shown in [10] that for an ac-dc converter without PFC, voltage-sense current-cancellation active EMI filter offers the most volume reduction. While this method avoided any current-transformers and additional high-voltage compensation network, an attenuation of only 12 dB was achieved around 150 kHz. The main bottleneck that limits the performance was identified as the phase shift introduced by the noise-sensing second-order high-pass filter.

This work proposes a novel active EMI filter with a twin-circuit. The proposed active EMI filter overcomes the stability issues facing a conventional feedback control based implementation. The proposed topology does not require any high voltage/current components for compensation, and instead only uses low-voltage surface mount components. Some of the preliminary results in this paper were previously presented by the authors in [19]. The organization of the work is as follows. Section II describes the proposed concept of the active EMI filter with a twin-circuit. Section III involves the modeling, design, and frequency domain measurements using the VNA to verify the modeling of individual sub-circuits and insertion loss of the entire filter as a whole. Section IV describes the experimental test setup, and discusses the small-signal and experimental results. Section V presents the conclusion.

4.3 Active EMI filter with twin circuit

4.3.1 Topology selection of active EMI filter

The active EMI filter could use either noise current or noise voltage-sensing and cancellation. Topologies that employ current-sensing and voltage-cancellation requires the use of CTs for current-sensing and voltage-injection transformers for voltage-injection, respectively. For DM noise, the CTs and voltage injection transformers can be bulky since they have to carry the line current without getting saturated. Therefore, using these topologies would affect volume reduction benefits that come with the use of the active EMI filter. Therefore, it is more desirable to use active EMI filter topologies that do not require the use of any additional magnetic components. The voltage-sense current-cancellation topology uses only high voltage capacitors in combination with low voltage active circuits for noise-sensing and cancellation. Therefore, using this topology will help maximize the volume reduction and therefore, is used in this paper. Previously, feedback control based voltage-sense current-cancellation topology was demonstrated in [10]. However, in order to avoid using additional high-voltage components for compensation for stability improvement, the attenuation of the active EMI filter was limited to 12 dB around 150 kHz. This work proposes a topology that only uses low-voltage components for compensation but still implements voltage-sense current-cancellation active EMI filter for DM noise cancellation while achieving 24 dB attenuation around 150 kHz.

4.3.2 Feedforward voltage-sense current-cancellation active EMI filter

The schematic of the overall implementation of the proposed active EMI filter for DM noise attenuation is shown in Fig. 4.2. The converter is represented by the current source, I_S, and the

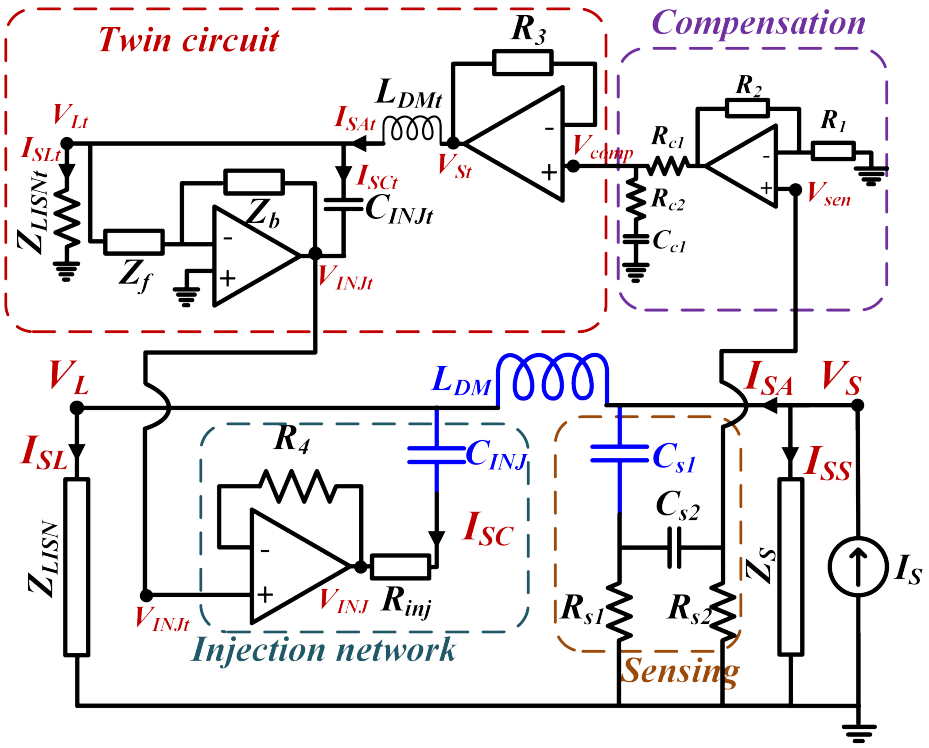

Fig. 4.2: Schematic of proposed feedforward control based voltage-sense current-cancellation active EMI filter with twin-circuit

noise source impedance Z_S represents the impedance of the dc-link capacitor. The load impedance Z_{LISN} represents the equivalent impedance of the LISN for DM noise. The original passive EMI filter consists of inductance, L_{DM}, and capacitor, C_{DM}. The proposed active EMI filter enhances the impedance of C_{DM}. And, in combination with L_{DM}, it forms the hybrid EMI filter. This L_{DM} could be a discrete inductor or leakage inductance of the CM choke. In the active EMI filter, the C_{DM} is referred to as the C_{INJ} since the noise current is injected through this capacitor. Noise-sensing is carried out at the converter end, making this implementation a feedforward topology.

There are four parts of the proposed active EMI filter circuit. The first stage involves the noise-sensing high pass filter. It consists of a second-order high pass filter that rejects any line frequency and other harmonics and senses only the switching frequency and its harmonics. The second stage is the compensation stage. The output of the high pass filter is buffered, and

the compensation network is used to improve the gain and phase around 150 kHz (start of EMI frequency range). The compensation network uses only low-voltage components and is key to enhance the attenuation of the active EMI filter. The next stage is the twin circuit. The output of the compensation network is fed to the twin circuit that comprises of the components that mirror the main filter components. That is, corresponding to L_{DM}, C_{INJ}, and Z_{LISN} in the main power circuit; there are L_{DMt}, C_{INJt}, and Z_{LISNt} in the twin circuit. The twin-circuit consists of a feedback control based voltage-sense current-cancellation topology active EMI filter. All the components in the twin circuit are low-voltage and low-power components. The final stage is the noise injection stage. This circuit buffers the injected noise in the twin circuit, V_{INJt}, and injects into the main circuit. Ideally, all the active circuitry and its components of the active circuit with the exception of L_{DMt} and C_{INJt} could be integrated into a single IC. Even then, since these components do not carry the line current or do not have to block the line voltage, they can be made from surface mount components or much smaller in volume relative to passive components in the power circuit for all cases. Moreover, the filter would be more beneficial at higher power levels. Further, in the entire active EMI filter, there are only two high-voltage components – C_{S1} and C_{INJ} capacitors avoiding the need for additional magnetic components or high-voltage capacitors.

4.4 Modeling of the active EMI filter and twin circuit

The block diagram of the entire active EMI filter circuit is shown in Fig. 4.3, and the equivalent circuit is shown in Fig. 4.4a. I_{SS} is the current through Z_S, and I_{SA} represents the current flowing through the filter. This cancellation current injected by the filter and the noise current through the LISN is represented by I_{SC} and I_{SL}, respectively. Alternatively, the DM noise source could be represented by the voltage source V_S given by (4.1) in series with an impedance,

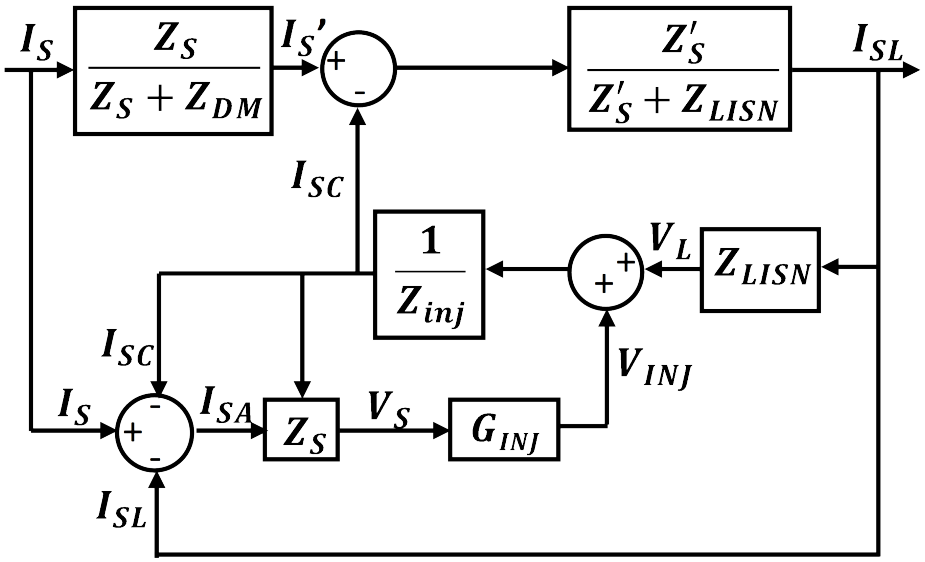

Fig. 4.3: Block diagram of proposed active EMI filter - twin circuit block diagram collapsed into G_{INJ}

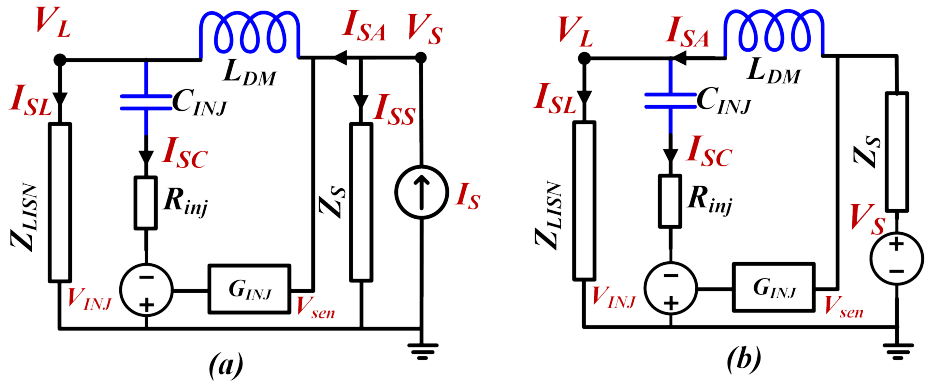

Fig. 4.4: (a) Equivalent circuit of proposed active EMI filter with noise source represented by current source (b) noise source represented by voltage source

as shown in Fig. 4.4b. Now, the sensed voltage, V_{SEN} is given by (4.2). Combining the impedance of L_{DM}, Z_{DM}, and noise-source impedance, Z_S, simplifies the derivation of the open-loop current gain. The new equivalent noise source (I_S') and noise source impedance (Z_S') is given by (4.3) and (4.4), respectively. Now, the open-loop current gain (G_{OL}) without the active EMI filter is given by (4.5).

$$V_S = I_S\, Z_S \tag{4.1}$$

$$V_{SEN} = V_S - I_{SA}Z_S = Z_S(I_S - I_{SA}) \tag{4.2}$$

$$I'_S = \frac{Z_S}{Z_S + Z_{DM}} I_S \tag{4.3}$$

$$Z'_S = Z_S + Z_{DM} \tag{4.4}$$

$$G_{OL} = \frac{I_{SL}}{I'_S} = \frac{Z'_S}{Z'_S + Z_L} = \frac{Z_S + Z_{DM}}{Z_S + Z_{DM} + Z_L} \tag{4.5}$$

The noise source voltage V_{SEN} is sensed by the active EMI filter using a high pass filter. The output of the high pass filter V_{HPF} is then inputted to the compensation stage. The output of the compensation stage is V_{COMP} is then used as the noise source V_{St} to the twin circuit. Let G_{INJ} be the ratio of the V_{INJ} to V_{SEN}. The injected cancellation current I_{SC} is given by (4.6). Substituting for V_{SEN} in (4.6), results in (4.7).

$$I_{SC} = \frac{I_{SL}Z_{LISN} + G_{INJ}V_{SEN}}{Z_{INJ}} \tag{4.6}$$

$$I_{SC} = \frac{I_{SL}Z_{LISN} + G_{INJ}(V_S - (I_{SL} + I_{SC})Z_S)}{Z_{INJ}} \tag{4.7}$$

.

The twin-circuit comprises of feedback control based voltage-sense current-cancellation active EMI filter circuit. The detailed derivation of the topology used in the twin circuit is presented

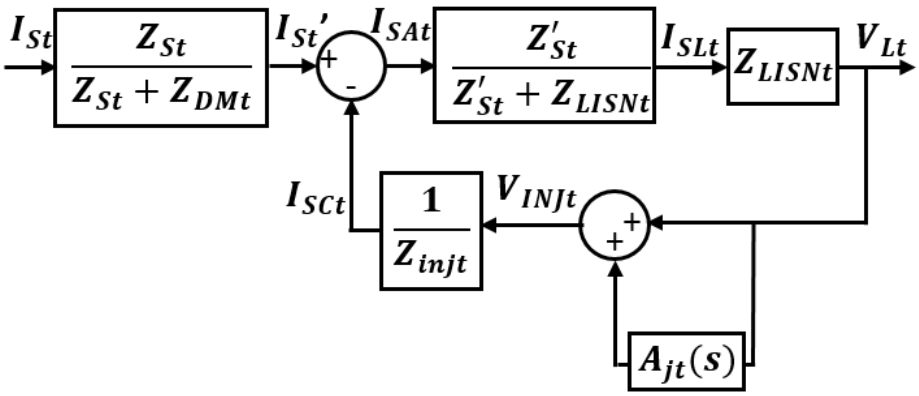

Fig. 4.5: Block diagram of twin circuit - feedback voltage-sense current-cancellation topology

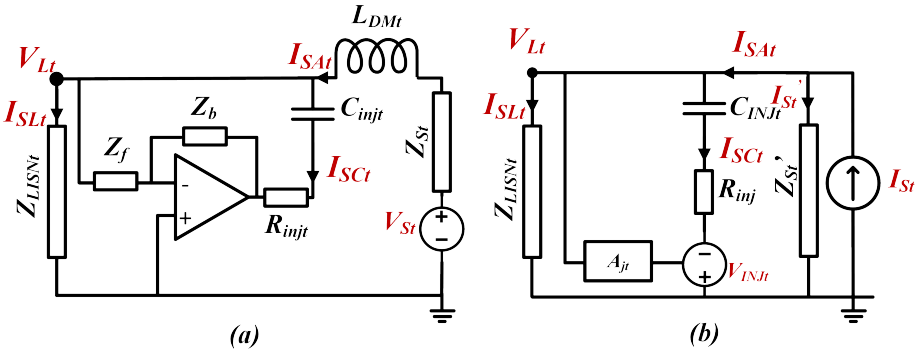

Fig. 4.6: Equivalent circuit of twin circuit with noise source represented by (a) voltage source and (b) current source

in [10] and general current-injection based active EMI filter topologies for DM noise are discussed in detail [6, 11, 12]. So, only final equations are given here for the sake of brevity. The block diagram of the twin-circuit is shown in Fig. 4.5. The circuit schematic and the equivalent circuit of the twin circuit are shown in Fig. 4.6a, and Fig. 4.6b respectively. The noise voltage source in the twin circuit is V_{St}. The current through L_{DMt} is I_{SLt}, and the cancellation current is I_{SCt} and the current through Z_{LISNt} is given by I_{SLt}. The feedback gain of the active circuit is represented by A_{jt}. The feedforward current gain and the loop gain of the feedback loop is given in (4.8) and (4.9) respectively.

$$\frac{I_{SLt}}{I'_{St}} = \frac{G_t}{1 + G_t \frac{Z_{LISNt}}{Z_{INJt}}(1 + A_{jt})} \tag{4.8}$$

$$where\ G_t = \frac{Z_{DMt}}{Z_{DMt} + Z_{LISNt}}$$

$$\frac{V_{INJt}}{V_{St}} = \frac{I_{SLt}}{I'_{St}} \frac{Z_{LISNt}}{Z_{DMt}} A_{jt} \tag{4.9}$$

Substituting (4.8) in (4.9), gives (4.10).

$$\frac{V_{INJt}}{V_{St}} = \frac{A_{jt}}{\frac{1}{G_t}\frac{Z_{INJt}}{Z_{LISNt}} + 1 + A_{jt}} \frac{Z_{INJt}}{Z_{DMt}} \tag{4.10}$$

The attenuation with the active EMI filter with the twin circuit is then given by (4.11).

$$G_{CL} = 1 - \frac{V_{INJt}}{V_{St}} \frac{Z_{DM}}{Z_{INJt}} T_{HPF} T_{COMP} \tag{4.11}$$

$$G_{CL} = 1 - \frac{A_{jt}}{\frac{1}{G_t}\frac{Z_{INJt}}{Z_{LISNt}} + 1 + A_{jt}} \frac{Z_{INJt}}{Z_{DMt}} \frac{Z_{DM}}{Z_{INJ}} T_{HPF} T_{COMP} \tag{4.12}$$

Substituting (4.10) in (4.11), yields (4.12). From (4.12), it can be seen that the attenuation of the proposed filter is highest when the second term is unity. For this to occur, the following conditions need to be satisfied:

1. The gain of the twin circuit which in turn determines the ratio of V_{INJt} to V_{St},

2. The degree to which there is a good match between Z_{INJ} and Z_{INJt}, Z_{DM} and Z_{DMt}, and

3. $T_{HPF}T_{COMP}$ should be unity in the EMI frequency range.

Further, the attenuation does not depend on the accurate match between Z_{LISN} and Z_{LISNt}, which makes the filter more robust to noise source impedance variations. The component selection, modeling, and design of each sub-circuit and overall circuit design to achieve maximum attenuation with the proposed active EMI filter are discussed next.

4.4.1 Operational Amplifier

The proposed active EMI filter uses op-amps in four parts of the circuit. Ideally, all four op-amps could be integrated into one single IC. The first three op-amps are all small signal circuits and do not need The open-loop gain and the output impedance of the op-amp are available in the datasheet [20]. The values from the datasheet are verified by measurements using the VNA. The open-loop gain is measured based on [21] and the output impedance of the op-amp is measured by configuring it at a known value of closed-loop gain [22]. The simplified model of the op-amp is shown in Fig. 4.7. The transfer function of the open-loop gain of the op-amp is given by 4.13. The open-loop gain is around 65 dB at 100 Hz and is capable of supplying up to 75 mA of current. This op-amp is over-designed to be used as the buffer for the noise-sensing and compensation stages. However, for the simplicity of modeling, the same op-amp is used in all three stages.

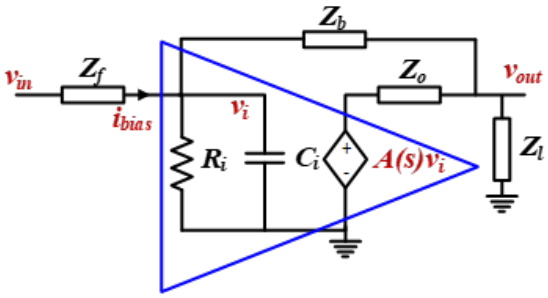

Fig. 4.7: Schematic of simplified model of op-amp

$$G_{amp} = \frac{G_o}{(1+s/\omega_1)(1+s/\omega_2)} \tag{4.13}$$

where, G_o is the open-loop gain at DC, and ω_1 and ω_2 represent the gain rollover frequencies. $G_o = 1780; \omega_1 = 2*180\ krad/s; \omega_2 = 2*350\ Mrad/s$

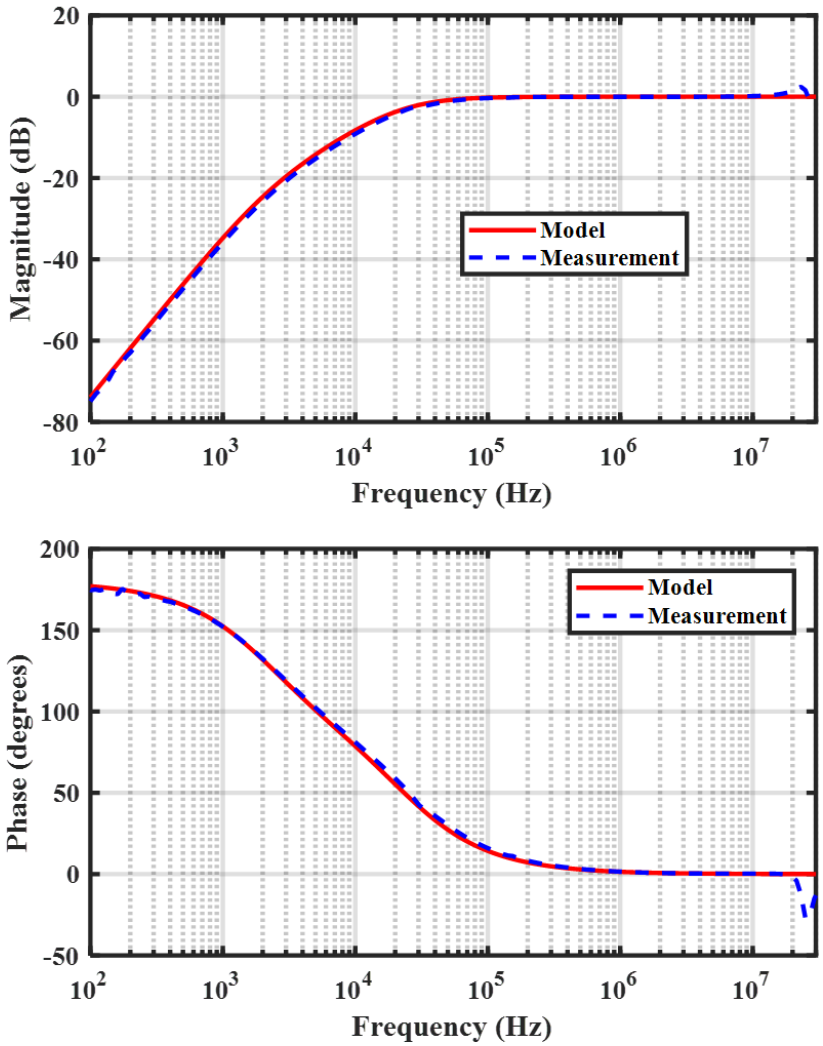

Fig. 4.8: Frequency response of high pass filter for noise-sensing - model vs. measurement

4.4.2 High Pass Filter

The converter that uses this filter could be fed from ac or dc supply. Either way, the noise-sensing stage has to sufficiently attenuate any 60 Hz ac voltage its harmonics, and the high-frequency currents due to rectifier operation or any other converters connected to the same node. Otherwise, any low frequency harmonics can easily saturate the output of the active circuits. Ideally, the output of the high pass filter should only include the switching frequency and its harmonics in the desired EMI frequency range (150 kHz to few MHz). The design of the sensing network requires careful consideration to ensure that it:

1. has the desired performance throughout the entire frequency range and
2. it does not add too much to the volume of the filter

It is not possible to get around 80 dB attenuation at 60 Hz with a 1^{st} order high pass filter. Therefore a 2^{nd} order high pass filter is used as the sensing network. The capacitor C_{s1} needs to be rated for the input voltage and needs to be safety rated (X1Y1 rated). The other components C_{s2}, R_{s1}, and R_{s2} are low voltage and low power components. The capacitor C_{s2} is a 50 V rated X7R surface mount capacitor. The transfer function of the filter is given by 4.14. The output of the high pass filter is buffered (op-amp configured as voltage-follower) and fed to the compensation stage. The selected op-amp is unity-gain stable with a gain-bandwidth of about 500 MHz. Therefore, the output of the buffer could be assumed to be the same as that of the high pass filter. The transfer function of the filter and the buffer is measured for $C_{s1} = 4.7\ nF$, $C_{s2} = 10\ nF$, $R_{s1} = 3.3\ k\Omega$ and $R_{s2} = 3.3\ k\Omega$ using the Bode-100 VNA. The comparison of model and measurement is shown in Fig. 4.8.

$$T_{HPF} = \frac{s^2}{s^2 + s(\frac{1}{C_{s1}R_{s1}} + \frac{1}{C_{s1}R_{s2}} + \frac{1}{C_{s2}R_{s2}}) + \frac{1}{C_{s1}C_{s2}R_{s1}R_{s2}}} \tag{4.14}$$

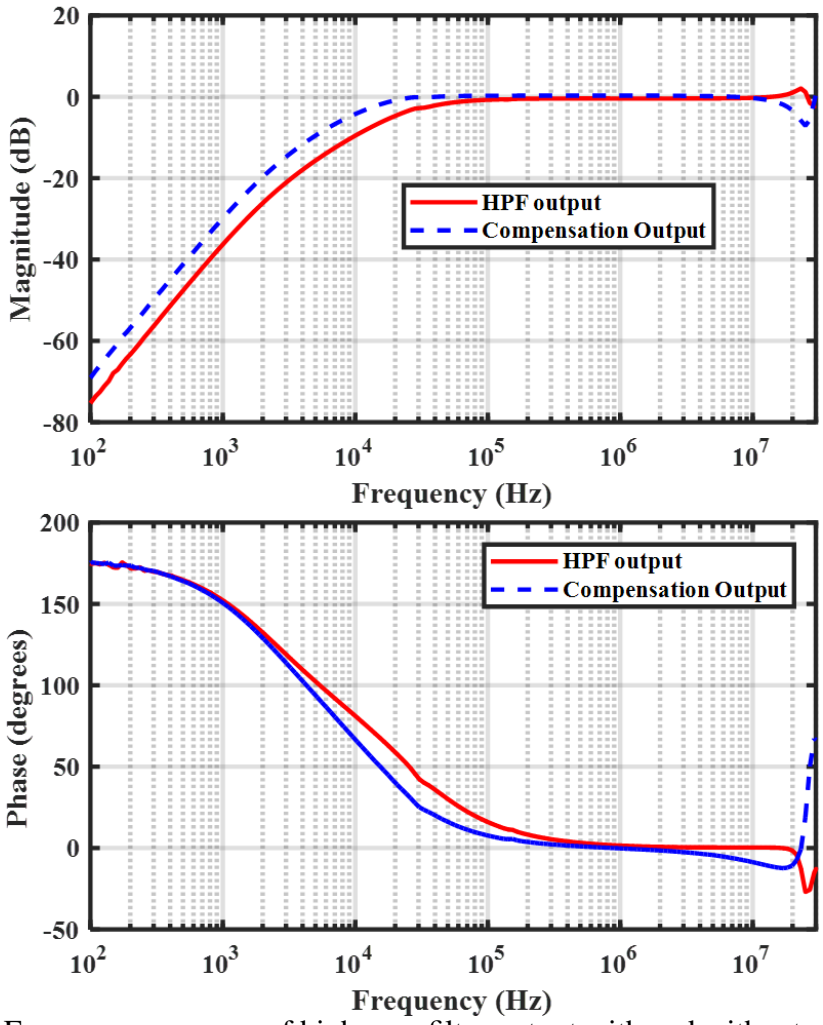

Fig. 4.9: Frequency response of high pass filter output with and without compensation

4.4.3 Compensation

The low-frequency compensation is a lead-lag compensator. As a whole, the proposed analog-twin based active EMI filter is a feedforward implementation. Therefore, the attenuation is maximum when the gain is unity with no phase shift. The high-pass filter that is used to sense the noise reduces the gain and introduces phase-shift up to a few 100 kHz. In order to reduce

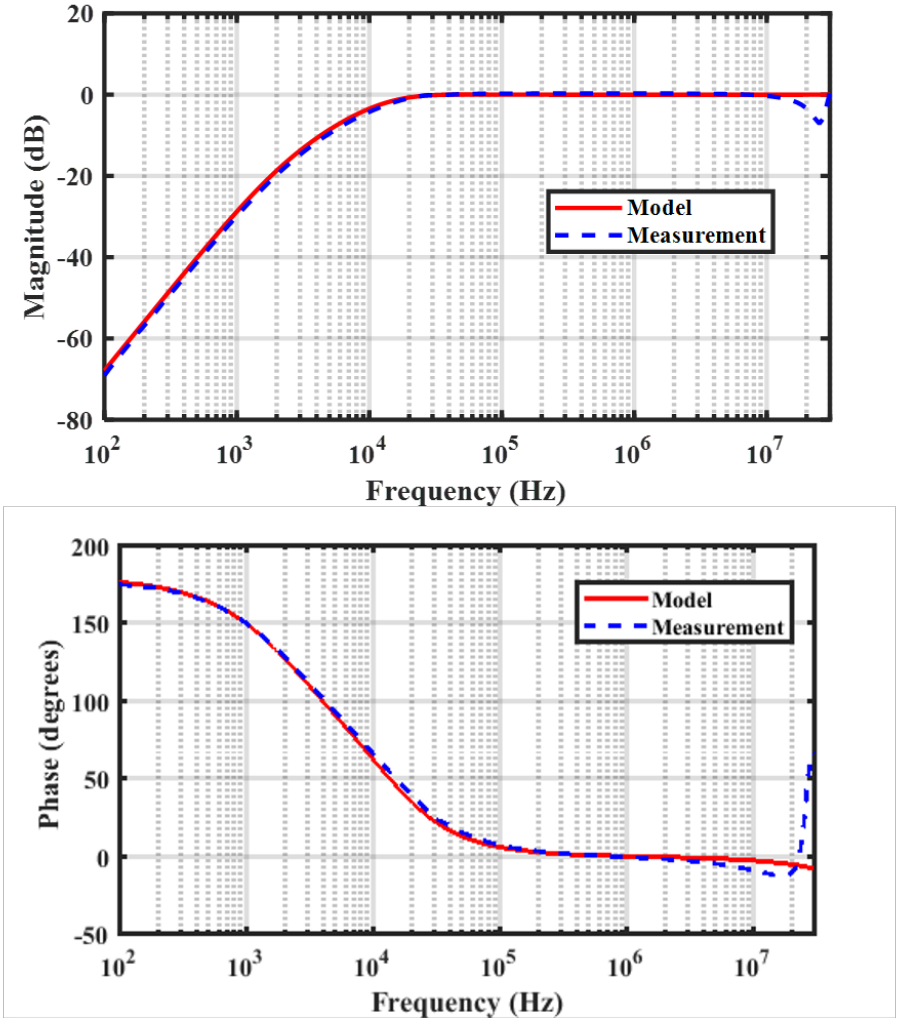

Fig. 4.10: Frequency response of compensation stage and high pass filter - model vs. measurement

this, a pole-zero pair (lead-lag compensator) is introduced after the high-pass filter. This transfer function of the sensed noised with and without compensation is illustrated in Fig. 9. The lead-lag compensator is chosen such to reduce the distortion in gain and phase in the EMI frequency range without overshooting the gain above unity. The compensation stage consists of a non-inverting amplifier with a gain of 2. Since the GBW of the op-amp is of the order of 500 MHz, the transfer function of the op-amp can be assumed to be approximately given by (4.15). The output of this circuit is fed to the compensation network. The compensation network consists of R_{c1}, R_{c2}, and C_{c1} and is used to introduce a pole-zero pair (lead-lag compensation) around 150 kHz to improve

the gain and the phase distortion introduced by the noise-sensing stage. The transfer function of the compensation stage is determined by the non-inverting amplifier and the passive network. The transfer function of the compensation network and the non-inverting amplifier is given by (4.16). The transfer function of the filter and the buffer is measured for $C_{c1} = 47\ nF$, $R_{c1} = 120\ \Omega$ and $R_{c2} = 120\ \Omega$ using the Bode-100 VNA. The comparison of model and measurement is shown in Fig. 4.8, and the comparison of the sensing stage with and without compensation is shown in Fig. 4.9.

$$T_A = \frac{1 + \frac{R_2}{R_1}}{1 + \frac{1+(R_2/R_1)}{G_{amp}}} \approx 2 \tag{4.15}$$

$$T_{COMP} = \frac{\frac{1}{sC_{c1}} + R_{c2}}{R_{c1} + \frac{1}{sC_{c1}} + R_{c2}} T_A \tag{4.16}$$

Besides this, all the op-amps require high-frequency compensation to avoid instability. This is ensured by conventional lag compensation by using a small capacitor across the feedback resistor to reduce the gain at frequencies higher than 30 MHz.

4.4.4 Twin Circuit

The twin-circuit comprises of feedback control based voltage-sense current-cancellation active EMI filter circuit. The detailed derivation of the topology used in the twin circuit is presented in [6, 10]. So, only final equations are given here for the sake of brevity. The block diagram of the twin-circuit is shown in Fig. 4.5. The circuit schematic and the equivalent circuit of the twin circuit are shown in Fig. 4.6a, and Fig. 4.6b respectively. The noise voltage source in the twin circuit is V_{St}. The current through L_{DMt} is I_{SLt}, and the cancellation current is I_{SCt} and the current

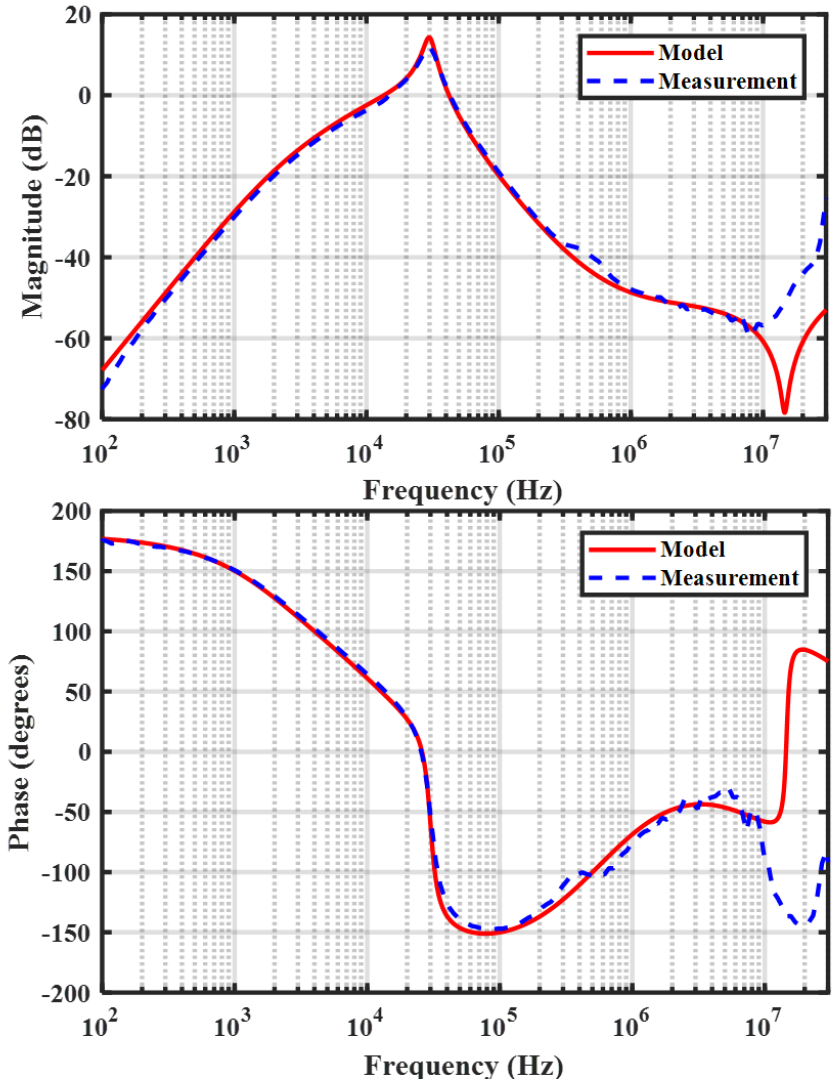

Fig. 4.11: Frequency domain measurement of V_{LISNt} - model vs. measurement

through Z_{LISNt} is given by I_{SLt}. The feedback gain of the active circuit is represented by A_{jt}. The feedforward current gain and the loop gain of the feedback loop is given in (4.8) and (4.9) respectively.

The twin circuit comprises of feedback voltage-sense current-cancellation topology which is designed based on [10] and only key details are provided here for the sake of brevity. The gain of the inverting amplifier is set using C_f, Z_f, and Z_b to 24 dB in the frequency range of 150 kHz to 1 MHz. The three main components of the twin circuit are L_{DMt}, C_{INJt}, and Z_{LISNt} which are

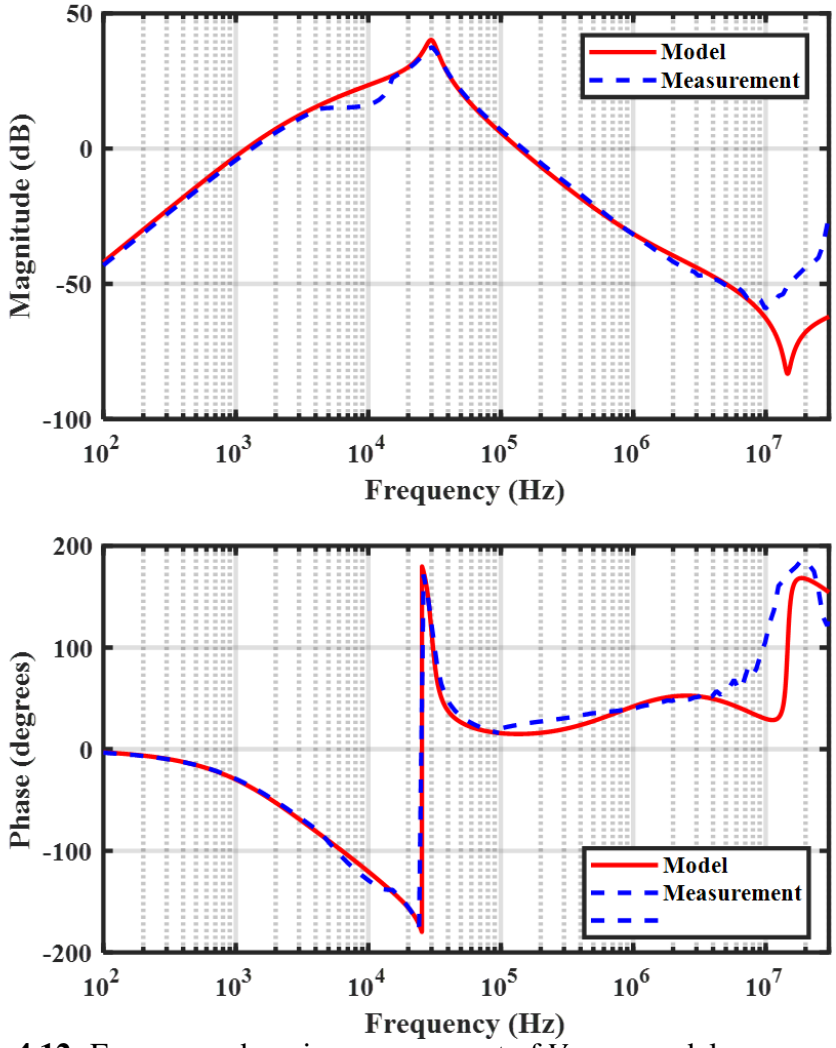

Fig. 4.12: Frequency domain measurement of V_{INJt} - model vs. measurement

identical to the components L_{DM}, C_{INJ}, and Z_{LISN} in the main power circuit. The twin circuit is configured in the feedback configuration. It operates to reduce the noise in Z_{LISNt}, which is a 100 Ω resistor. The gain of the amplifier circuit is directly related to the attenuation provided by the active EMI filter. The high-frequency stability of the twin circuit is ensured by using lead-compensation method (adding a capacitor across the feedback resistor) and using an injection resistor in series with C_{INJt}. The loop gain of the twin circuit is given by (4.17). The gain of the twin circuit is set to ensure that the twin circuit is stable and the output of the op-amp in the twin circuit is not saturated

by any low-frequency and its harmonics. The voltage V_INJt is then fed to a buffer in the injection stage. The output of this buffer is fed to C_{INJ} in the main circuit. The voltages V_{LISNt} and V_{INJt} are measured using the VNA for $L_{DMt} = 33\ \mu H$, $C_{INJt} = 47nF$, and $Z_{LISNt} = 100\Omega$. The comparison of model and measurement is shown in Fig. 4.11, and Fig. 4.12 and show good agreement.

$$A_{jt} = T_{IA}(s)\ \frac{Z_L//Z_S}{(Z_L//Z_S)+Z_{inj}} \tag{4.17}$$

where,

$$T_{IA} = \frac{G_{op-amp}(Z_b+(Z_o//Z_l))}{Z_{ff}+Z_b+(Z_o//Z_l)}\frac{1}{1+G_{op-amp}\beta}$$

$$\beta = \left(\frac{Z_{ff}}{Z_{ff}+Z_b}\right)\left(\frac{Z_l//(Z_{ff}+Z_b)}{Z_l//(Z_{ff}+Z_b)+Z_o}\right)$$

$$Z_l = Z_{INJt}+Z_{LISNt}//Z_{DMt}$$

4.4.5 Injection Network and Insertion Loss

The V_{INJt} voltage from the twin circuit is buffered and injected in the main circuit using C_{INJ}. A series resistor R_{INJ} is added to damp the resonance between L_{DM} and C_{DM}, similar to the twin-circuit. The model vs. measurement of insertion loss of the proposed analog-twin based active EMI filter is shown in Fig. 4.13. The measurement shows good agreement to the model up to a few MHz. The comparison of insertion loss with the inductor L_{DM} (33 μH) , passive components L_{DM} (33 μH) and C_{DM} (47 nF) only, the same passive components, L_{DM} (33 μH) and

C_{INJ} (47 nF), when used with the analog-twin based active EMI filter , is shown in fig. 4.14. In order to see the additional attenuation by the active EMI filter, the value of C_{DM} and C_{INJ} is kept the same. When compared to the passive components only, the active EMI filter provides 24 dB at 150 kHz with the bandwidth of 1 MHz. However, along with L_{DM}, the bandwith of the overall hybrid filter encompasses the entire conducted EMI frequency range of CISPR-22 standard (150 kHz to 30 MHz).

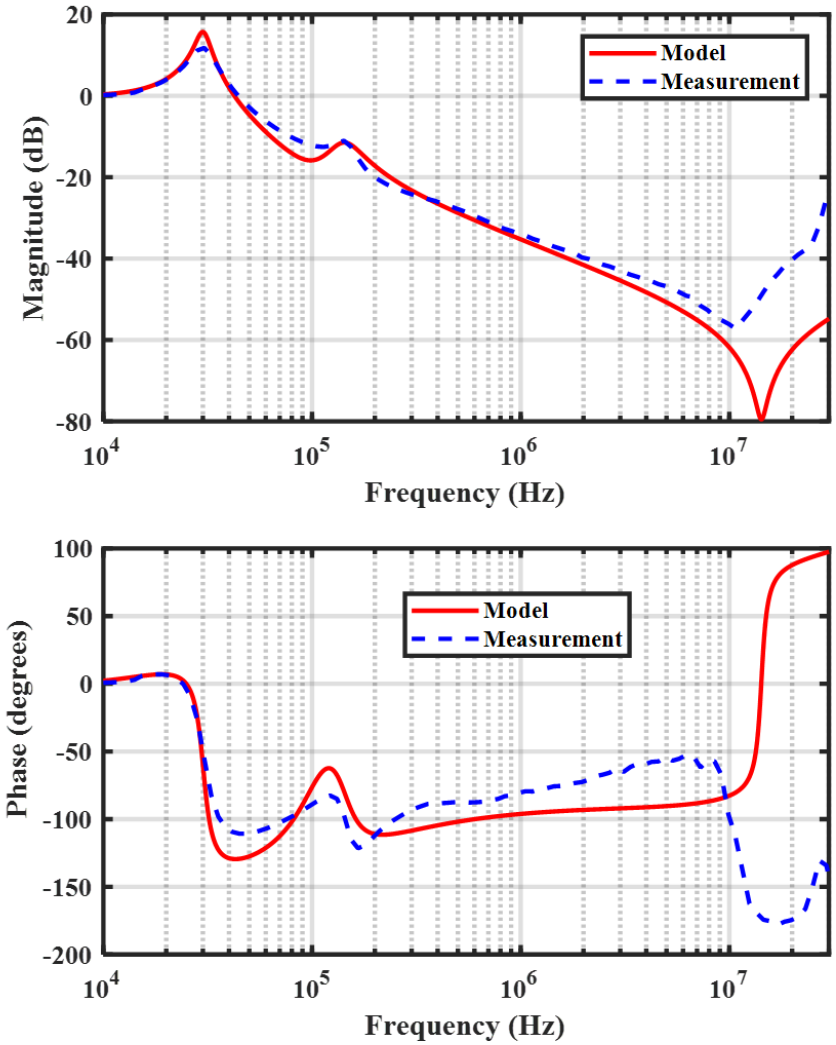

Fig. 4.13: Insertion loss of analog twin active EMI filter - model vs. measurement

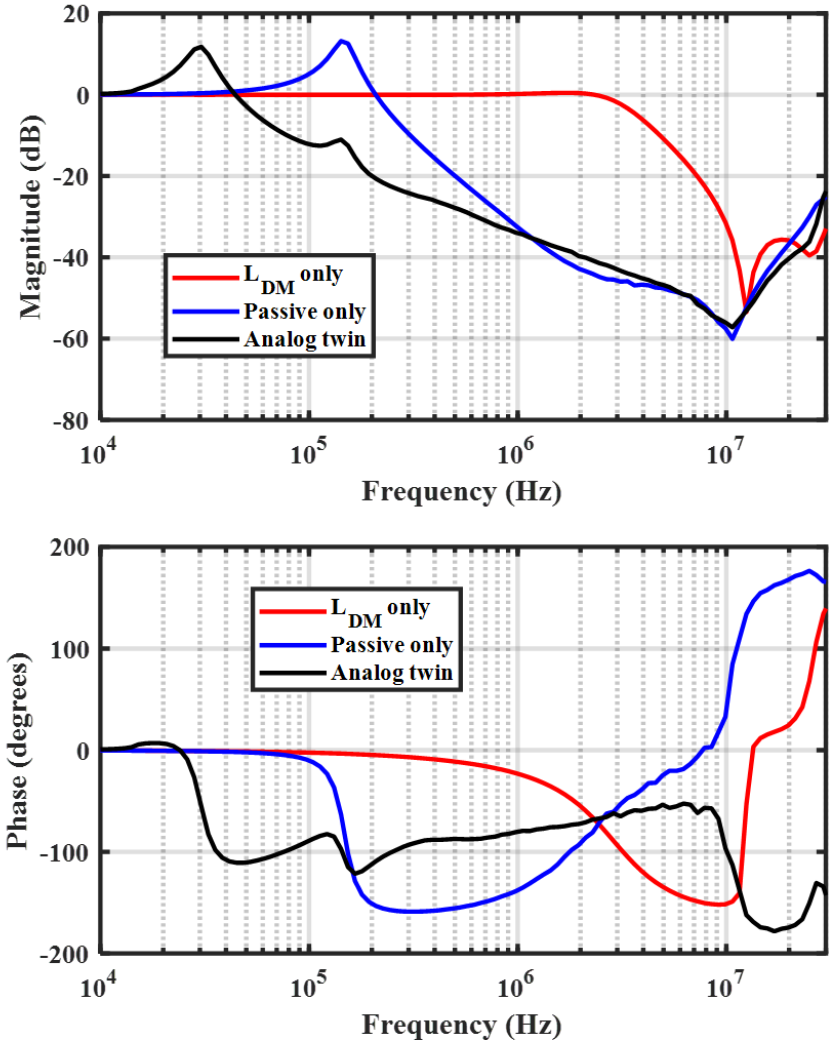

Fig. 4.14: Measured insertion loss of $L_{DM} = 33\ \mu H$ only, passive components ($L_{DM} = 33\ \mu H$ and $C_{DM} = 47\ nF$) only and with analog twin ($L_{DM} = 33\ \mu H$, $C_{INJ} = 47\ nF$ and active circuit)

4.5 Experimental Results

4.5.1 Small Signal Test Results

For carrying out the small-signal tests, the function generator is used as the noise source. Since the output of the function generator has a 50 Ω output impedance, the function generator is used with an op-amp configured as a voltage-follower. In addition, a 30 μF capacitor in series to the output of the voltage-follower to represent the capacitive noise source impedance in the actual

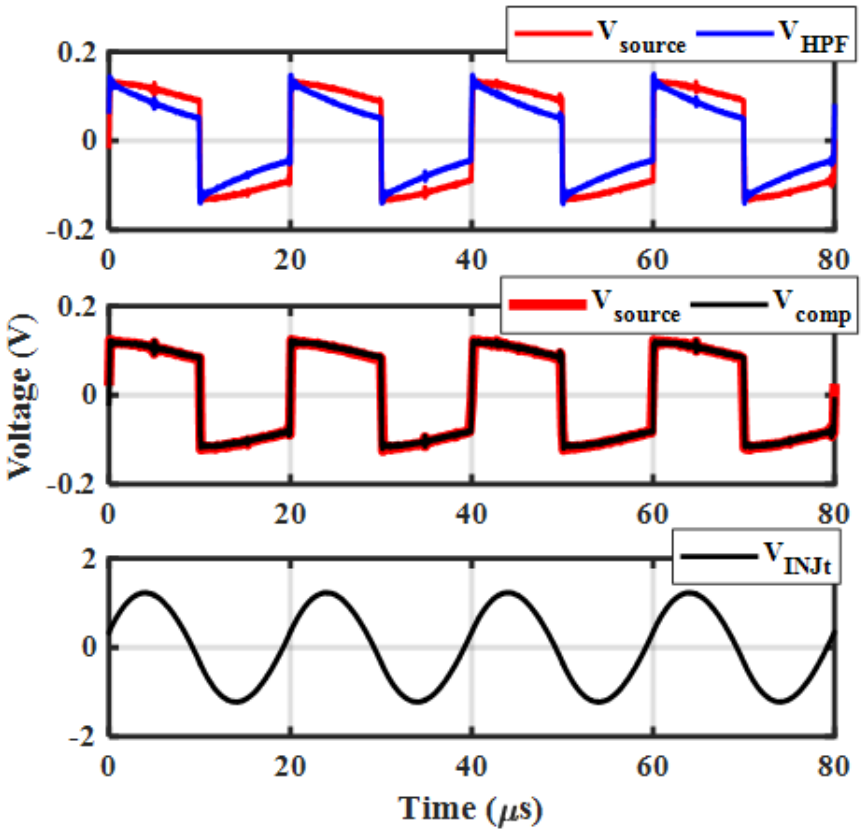

Fig. 4.15: Small-signal time-domain measurements

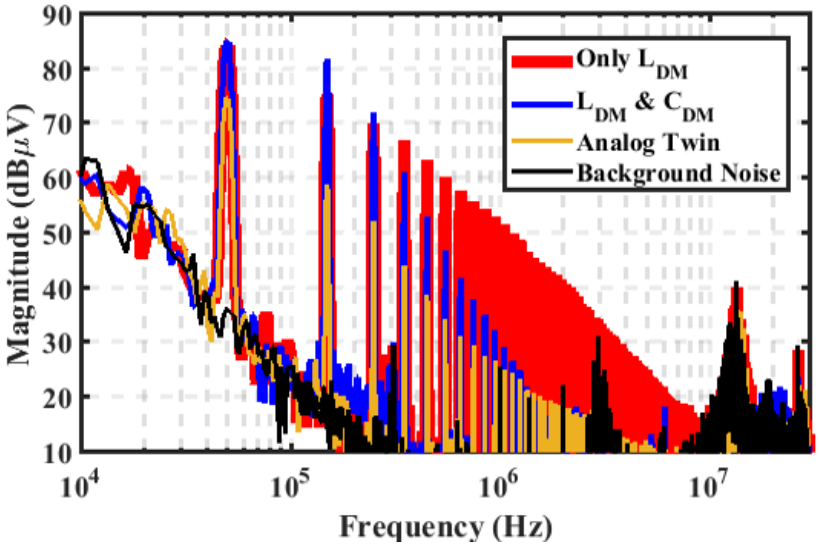

Fig. 4.16: Small-signal frequency-domain measurements with EMI receiver

converter. The output through the capacitor is then connected to the active EMI filter, and tests are carried out under two cases. One with the L_{DM} and C_{DM} and another with the L_{DM} and the proposed active EMI filter. The active EMI filter uses C_{INJ} same as that of C_{DM}. The noise is measured at the LISN with a DM noise splitter (Mini-circuits ZSCJ-2-2+). The output of the DM noise splitter is connected to the Keysight MXE EMI receiver. The time-domain waveforms at different stages of the proposed active EMI filter are measured using TPP1000 1 GHz passive probes and a Tektronix MSO-56 Oscilloscope and shown in Fig. 4.15. The noise voltage (V_{source}) is sensed using the high pass filter (V_{HPF}) is distorted due to the non-linear phase shift introduced by the high pass filter. The output of the compensation network has lower distortion and corresponds well to V_{source}. The injection signal(V_{INJ}) does not have any high frequency or low-frequency ringing confirming that the filter is stable. The frequency-domain measurements from the EMI receiver are shown in Fig. 4.16. With the proposed active EMI filter, there is about 24 dB attenuation around 150 kHz and the bandwidth of 1 MHz corresponds to the frequency domain measurements using the VNA.

4.5.2 Experimental results with converter

The measurement setup is the same as that of the small-signal test results. The filter is connected to a buck-converter with a switching frequency of 50 kHz and 75% duty cycle. The measurements are carried out under the same two cases, as previously mentioned in the small-signal tests. The time-domain measurements and are shown in Fig. 4.17 and the EMI receiver measurements are shown in Fig. 4.18, respectively. From Fig. 4.17 the distortion introduced by the high pass filter has been corrected by the compensation network. The injection stage has no high-frequency or low-frequency ringing, ensuring that the filter is stable. From Fig. 4.18, the attenuation at 150 kHz is around 24 dB, which is consistent with the small-signal results and

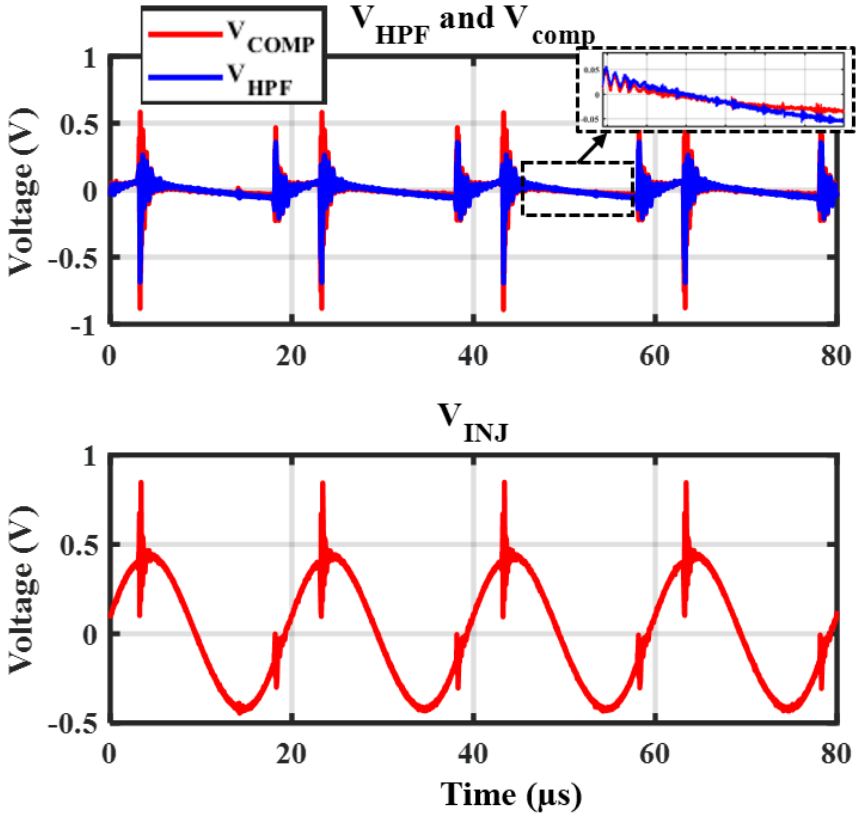

Fig. 4.17: Time-domain converter test results

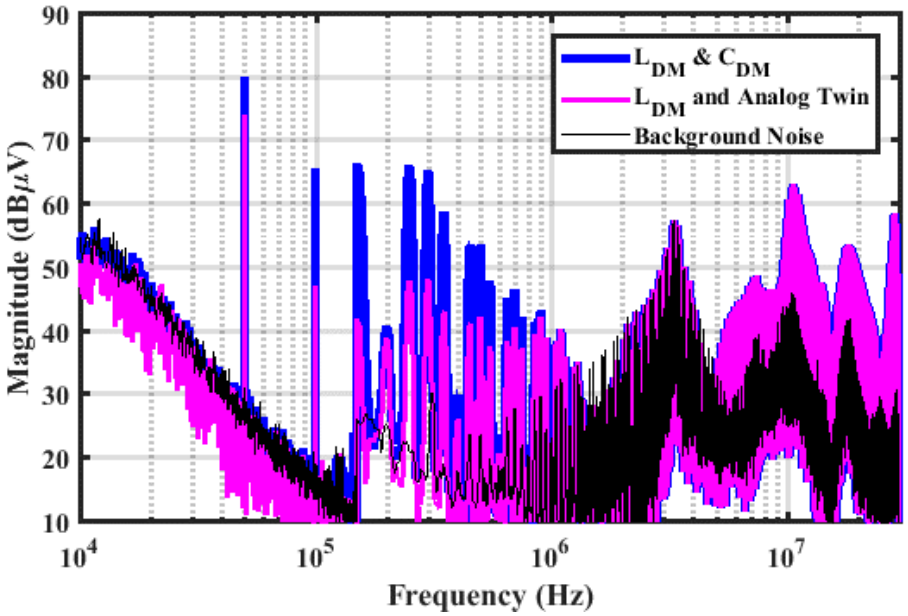

Fig. 4.18: Converter test frequency-domain measurements with EMI receiver

VNA measurement. There is some attenuation up to 1 MHz, which is also consistent with the measurements using the VNA.

4.5.3 Power Loss and Volume Reduction

The demonstration of the proposed filter includes three op-amps. For simplicity of modeling all the four op-amps were chosen to be same model. Also, as mentioned earlier, all of these op-amps could be integrated into a single op-amp. Therefore, the bias power of only one op-amp is considered for calculation of power loss. All the losses in the op-amp are calculated using 5 V bias power. The quiescent power loss in the op-amp is about 50 mW corresponding to quiescent current of about 10 mA. There are losses in the injection op-amp due to the leakage current in the injection capacitors. For dc systems, this loss is negligible. For ac 110 V 60 Hz supply, the leakage current is about 2 mA (for 47 nF C_{INJ}) which translates to about 10 mW in losses in the op-amp. Besides these losses, there is loss due to injected current. From Fig. 18, the majority of the injected noise current is only up to 500 kHz. So higher harmonics can be neglected. At 150 kHz, the noise reduces from 66 dBμV to 42 dBμV. These corresponds to 39.9 mA and 2.5 mA of current measured at the LISN at 150 kHz. Therefore, the losses in the injection op-amp is about 188 mW. Similarly, corresponding to noise injected up to harmonics of 500 kHz, the total power loss due to injection current is about 725 mW. Thus, the total power loss (quiescent + leakage current + injection current) is 785 mW. Majority of the losses comes from due to the noise cancellation current. At 30 W power level, the losses are about 2.5%. However, for the same attenuation, same amount of cancellation-current is injected in the circuit at any power level. For example, consider the case where the analog-twin based active EMI filter is used in 300 W converter. To arrive at worst case estimates, the bias voltage for the amplifiers is assumed to 15 V instead of 5 V. Then

the power losses in incurred in the injection circuit will be 2.175 W which corresponds to about 0.7%. Therefore, the percentage of losses incurred in the active EMI filter for the same attenuation reduces as the power level increases. Further, corresponding to a reduction of capacitance (X2, 275 Vac rated) from 470 nF (3790 cu. mm.) to 47 nF (1215 cu. mm.), the volume reduction of required capacitor is about 68%.

4.6 Conclusion and future work

A novel feedforward control based voltage-sense current-cancellation topology with a twin-circuit that uses only high-voltage capacitors for noise-sensing and cancellation is proposed. The topology uses only low-voltage surface mount components for compensation to improve attenuation and ensure the stability of the active EMI filter. The twin-circuit consists of components that are identical to that of the main circuit. The individual sub-circuits are modeled in detail to arrive at the overall system model and insertion loss. The small-signal measurements are carried out using the VNA at the sub-circuit level, and system level, and the insertion loss of the proposed filter is compared to the passive filter. The model is in good agreement with the measurement up to a few MHz. The small-signal test results and experimental test results show an attenuation of 24 dB at 150 kHz using a 47 nF capacitor, and a bandwidth of 1 MHz. This would enable replacing a 470 nF capacitor with a 47 nF one using the proposed active EMI filter resulting in a 68% smaller capacitor.

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Amp_Analysis/2018-01-18_Appnote_open_loop_gain_V1.1.pdf

5 Zero-Phase-Filtering based Digital Active EMI Filter

5.1 Abstract

Zero-phase filtering is a methodology of achieving filtering without any phase distortion. This methodology is applied to digital active EMI filters to enhance the attenuation at frequencies from 100 kHz to 1 MHz. The methodology for implementing this in an FPGA and the tuning procedure are presented. The novel filter is then demonstrated in a feed-forward voltage-sense voltage-cancellation active EMI filter for differential mode noise attenuation. Tests are carried out with small signal source and as well in a power converter. The test results show that the proposed filter can have up to 46 dB attenuation in the frequency range of 100 kHz to 500 kHz which is 22 dB higher compared to conventional digital active EMI filter.

5.2 Introduction

Power converters generate conducted EMI noise due to the switching action of the power semiconductor devices. Conventionally, a second order passive EMI filter is used to mitigate this noise. These passive filters tend be bulky and could occupy up to 30% of the system volume. Active EMI filters (AEF) could be used to reduce the volume of the passive components. The AEF provides attenuation up to a few MHz and a smaller passive filter is used to provide high frequency attenuation. The AEF along with the passive filters is referred to as hybrid EMI filters (HEFs). The HEFs have been shown to reduce the volume of the passive components by over 50% [1, 2]. The AEFs can be classified based on the methodology of control, the active circuits, noise sensing and noise cancellation mechanisms [3–5]. Previously, AEFs using feed-forward[5],

feedback[6–8] and a combination of both control techniques [8] have been demonstrated. Also, AEFs utilizing different voltage or current sensing and cancellation have been demonstrated [1, 2, 9–11]. All these implementations use analog ICs along with passive components for the active circuits. Recently, digital AEFs [12–15] that use DSP/FPGAs in addition to the analog circuitry have been demonstrated.

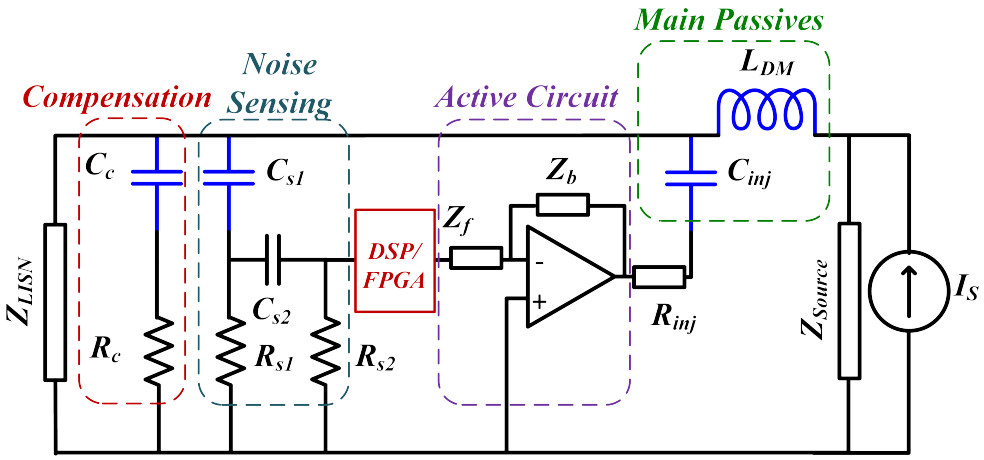


Fig. 5.1: A typical digital active EMI filter

A typical implementation of a digital active EMI filter is shown in Fig. 5.1. It comprises of the noise sensing high pass filter (HPF), the DSP/FPGA, the active circuit, the main passives and the compensation circuitry. The DSP/FPGA will not be present in an analog only implementation. The main limitations to the performance of any AEF is the stability. The stability is mainly influenced by the phase shift introduced by the noise sensing stage [7]. Particularly, in converters with ac voltage, a second order high pass filter is required to separate the sensed noise from the fundamental voltage or current signal. This results in reduced attenuation of the AEF and additional compensation network. Some compensation networks require high voltage capacitors thus reducing the volumetric benefits of using an active EMI filter. This limitation is applicable to both analog and digital AEF. In [16] showed how the processing delay in digital AEF affects the

attenuation. In [15], it was shown the noise from the previous switching cycle could be used to compensate noise in the next switching cycle to avoid the delay. However, an attenuation of only 24 dB could be achieved in the process.

A second order passive filter used for noise sensing introduces non-linear magnitude and phase distortion in the filtered signal. If the high pass filter could have linear phase response, then it could be compensated with ease in the DSP/FPGA thus resulting in zero-phase filter. This would boost the performance of the active EMI filter as well. However, this would require higher order passive filter with non-realizable passive component values. Other method is to use time reversed filtering [17, 18]. In this method, in addition to the passive filter, another set of digital filters are used in the DSP/FPGA to obtain linear phase filtering. But, this method introduces a minimum delay to carry out the time-reversed digital filtering in DSP/FPGA. Linear-phase filters for signal processing was first proposed in [17] for eliminating phase distortion in recursive filters. However, this method could be used offline and for signals of finite length only. This method was improved in [19] for offline filtering of infinitely long signals by considering one section of the signal at a time. This is referred to as block processing technique. Later, [18, 20] extended the block processing technique to carry out linear-phase filtering in real-time. Improvements to the method have been proposed to achieve reduced delay and distortion [21–23]. This methodology has been applied for applications ranging from robotics [24, 25] to motor-control [26].

For active EMI filters, by using the noise information from the previous cycles and synchronizing with the current cycle of data, zero-phase filtering could be obtained. This would boost the attenuation of the active EMI filter theoretically by up to 60 dB which is 35 dB higher than conventional digital active EMI filters. The contribution of this paper is as follows. This paper proposes a novel digital AEF that completely nullifies the phase shifts introduced at harmonics of

the sensed noise signal. This enables the digital AEF to have very high attenuation without the need for any additional compensation networks. The proposed AEF achieves an attenuation of 46 dB around 150 kHz which is 25 dB higher than conventional active EMI filter. This is the highest reported attenuation in the literature using a first order digital or analog AEF.

The organization of the paper is as follows. The concept of zero-phase filtering is discussed in Section II. Application of the zero-phase filtering to active EMI filters and its implementation in FPGA is discussed in Section III. The methodology of tuning the zero-phase filter and small signal tests are discussed in Section IV. The experimental test setup and results are discussed in Section V. The conclusion is presented in Section VI.

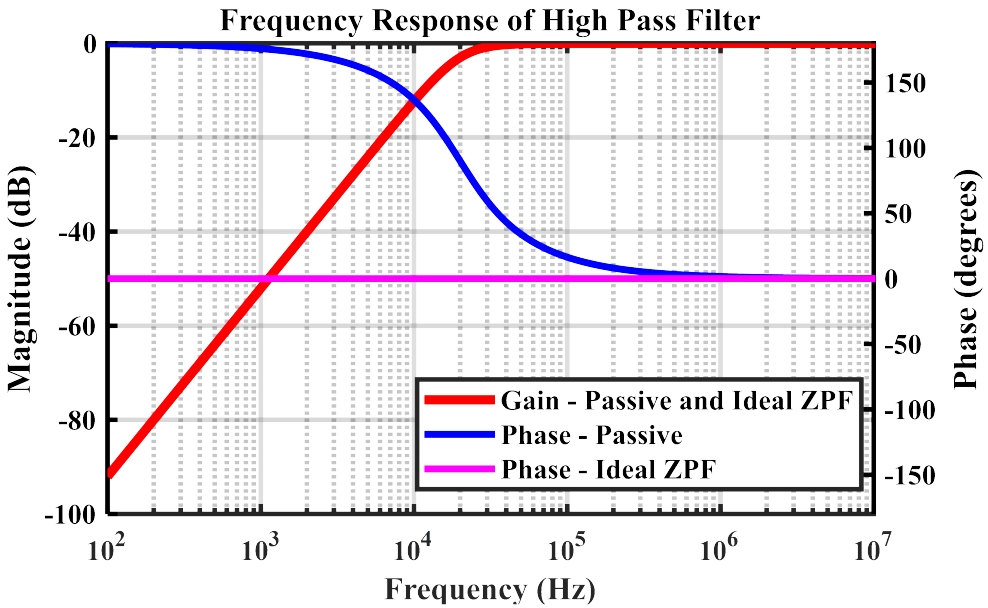


Fig. 5.2: A typical digital active EMI filter

5.3 Ideal Zero-phase Filtering based Digital Active EMI Filter

5.3.1 Ideal zero-phase filtering

Let $X(z)$, $Y_1(z)$ and $H(z)$ be the input, output and the filter transfer function respectively. The output, $Y(z)$ is given by (5.1). This is conventional filtering where $Y_1(z)$ has non-linear phase distortion introduced by the filtering action.

$$Y_1(z) = X(z)\,H(z) \tag{5.1}$$

If the filter is applied to $Y_1(z)$ in the opposite direction, the output $Y_2(z)$ is given by 5.2. Now, if $Y_2(z)$ is time-reversed again, the resulting output $Y(z)$ is given by (5.3).

$$Y_2(z) = Y_1(z^{-1})\,H(z) \tag{5.2}$$

$$Y(z) = Y_2(z^{-1}) \tag{5.3}$$

Substituting (5.1) and (5.2) in (5.3) gives (5.4). Substituting $z = e^{j\omega}$ in (5.4) gives (5.5).

$$Y(z) = Y_1(z)\,H(z^{-1}) = X(z)\,H(z)\,H(z^{-1}) \tag{5.4}$$

$$Y(e^{j\omega}) = X(e^{j\omega})\,|H(e^{j\omega})|^2 \tag{5.5}$$

The final output given in (5.5) is only affected by the magnitude of the filter applied but has no phase distortion. The gain-phase plot of a passive high pass filter and ideal zero-phase filtered HPF (ZPF HPF) is shown in Fig. 5.2. The conventional high pass filter has phase shift at frequen-

cies where it provides attenuation. But, the zero-phase filter completely nullifies the phase shift introduced by the high pass filter. If this technique could be used in a digital active EMI filter, there will be no-phase distortion introduced by the noise sensing stage resulting in a much higher attenuation than conventional analog or digital active EMI filter. One possible realization of the real-time implementation of zero-phase filtering is as follows.

5.3.2 Implementation Methodology

In this case, the noise sensed from one switching cycle is used to compensate the noise 2 cycles in the future. The flowchart of the implementation is shown in Fig. 5.5 and the corresponding time domain signals are shown in Fig. **??**. The implementation of the zero-phase filtering is as follows:

1. Save one switching cycle of noise sensed using the passive high pass filter.
2. The stored signal is time reversed.
3. The digital filter is then applied to the time-reversed signal.
4. Save the filtered signal.
5. Time reverse the save data and synchronize noise injection with the next switching cycle.

The flowchart of the zero-phase filter is shown in Fig. 5.6. The time domain waveforms shown in the Fig. 5.6 assume a delay of one cycle for processing which results in a two cycle delay from sensing to injection. This delay could vary depending on the hardware implementation.

The above implementation assumes that only the harmonics of the switching frequency are present in the source voltage. However, this is not true in many systems in which multiple converters operating at different switching frequencies may be connected to the same node in the system. In zero-phase filtering, digital filtering is carried out section by section of the sensed

noise signal. When filtering by sections, any transients are introduced. These transients result in distortion and reduce the attenuation of the filter. The methodology to avoid these transients and ensure high attenuation with the digital active EMI filter is discussed next.

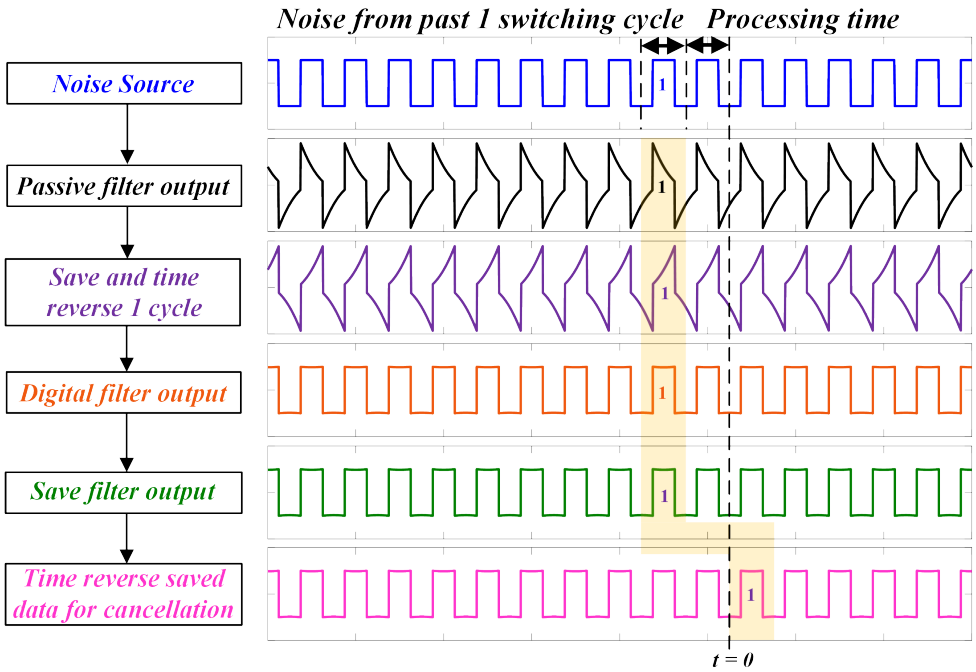


Fig. 5.3: Flowchart for cycle-by-cycle implementation

5.4 Real-time implementation of zero-phase filtering

The repetitive nature of the EMI noise is used for the real-time implementation of zero-phase filtering based digital active EMI filter. A passive high pass filter is firstly used to separate the harmonics of the switching frequency in the EMI frequency range from the line frequency and other low frequency harmonics. The sensed noise signal has non-linear phase distortion introduced by the high pass filter. Next, a section of this sensed noise is stored for time-reversal and digital filtering. Let L denote the length of the section of the stored signal for time reversal and digital filtering. And, f_{sw} denotes the switching frequency and T_p $(1/f_{sw})$ denotes the time period. Ideally,

L would be equal to T_p where noise from one switching cycle stored and used for zero-phase filtering. But, such an implementation is not possible because of the transients introduced by digital filtering. Therefore, L would have to be integer multiple of T_p. The effect of transients on the performance of zero-phase filtering and selection of an appropriate L is discussed as follows.

5.4.1 Transients due to digital filtering in sections

In zero-phase filtering, the sensed noise signal is divided into sections of length L and time reversed for digital filtering. When filtering is carried out in sections, transients occur during filtering of each section. These transients distort the filtered signal and affect the performance of the active EMI filter. Therefore this needs to be avoided. Previously, different overlap save and overlap add based techniques were introduced in [18, 23] for reducing the distortion of the zero-phase filtered signal. In this work, the overlap save technique is used to avoid transients. The overlap save technique uses section length that is long enough for the transients to die out. Ideally, infinite section length is required for the transient to die out. In order to realize the real-time implementation, the section length cannot be infinitely long. Also, the larger is the section length, larger is the delay introduced between the noise sensing and noise cancellation. Therefore, section length needs to be decided based on the trade-off between the distortion of the signal at the output of the digital filter and the delay. The effect of transients on signal distortion and the methodology for selecting the section length is discussed next.

The effects of transients is illustrated using an example. Consider two signals: signal-1 first a 40 kHz square wave signal with 50% duty cycle and signal-2 is made up of a 15 kHz sinusoidal signal and 40 kHz square wave signal with 50% duty cycle. The 15 kHz signal represents an external signal that could be present on the grid and the 40 kHz signal represents the EMI noise.

The choice of 15 kHz is arbitrary and used for illustration only. The high pass filter transfer function considered for illustration is given in5.6 with $\omega_1 = \omega_2 = 20\,kHz$. The filter is applied to both the signals under two different section lengths. The effects of transients on these signals under two different section lengths are considered for discussion below.

$$T_{HPF}(s) = \frac{s^2}{(s+\omega_1)(s+\omega_2)} \tag{5.6}$$

Case 1: $L = T_p$

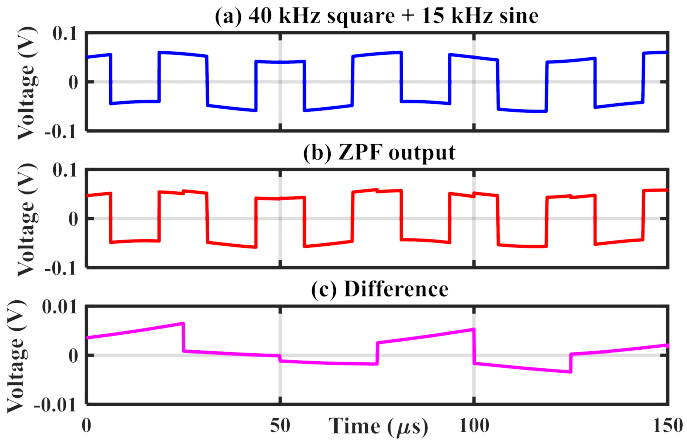
The signals are divided into sections of length equal to 25 μs which is one time period of 40 kHz signal. The time-domain waveforms and FFT of the filtered signal are shown in Fig. The FFT of filtered signal-1 is as expected while the FFT of filtered signal-2 contains even harmonics which are a result of the transients from filtering.

Case 2: $L = n * T_p$ When one time period of the 40 kHz.

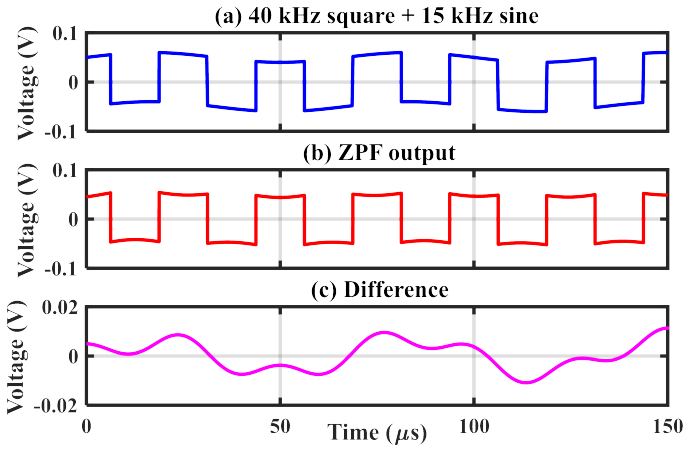
5.4.2 Application of zero-phase filtering to digital active EMI filter

The noise sensing comprises of a passive first order or second order high pass filter (HPF). This blocks the low frequency power and line transients on the main power line from saturating the following active circuit. But, the phase shift introduced by the HPF reduces the attenuation provided by the AEF.

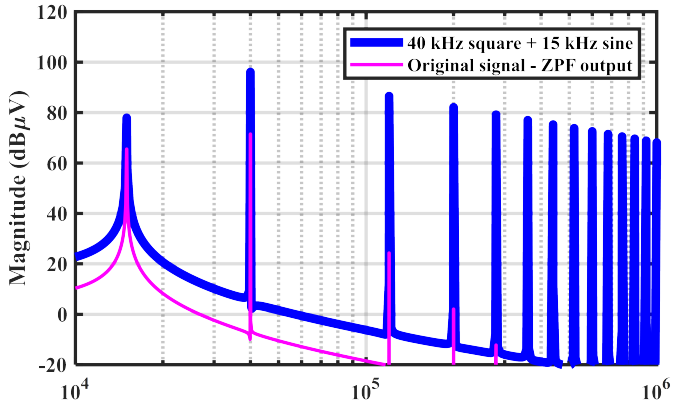
However, this methodology is suitable only when the power source is free from any other noise with the exception of switching frequency and its harmonics. Because, when one switching



(a) Cycle-by-cycle implementation



(b) Multiple-cycle implementation



(c) FFT comparison

Fig. 5.4: Simulation results

cycle of noise data is saved, a fraction of other frequency components (which are not harmonics of f_{sw}) are present. When digital filter is applied to this noise data, transients occur during each cycle. These transients results in undesired frequency components which affects the performance

of the filter. The frequency of these components depend upon the switching frequency f_{sw} and the frequency of the noise f_{noise} and occur at $m * f_{sw} \pm f_{noise}$ where $m = 1,\ 2,\ \ldots\ , n$. Therefore, the cycle-by-cycle implementation could be carried out only when the power source is free from other frequency components.

This phenomenon is illustrated using simulation in MATLAB. A signal of length 1 *ms* that consists of two components is considered here. This signal will be referred to as *original* signal. The two components of this signal are: a 40 kHz square pulse representing the noise source from a power converter and a 15 kHz sinusoidal component representing the noise on the grid. A second order high pass filter with transfer function shown in Fig. 5.2 is implemented using the $filter$ command in MATLAB. The high pass filter is applied to the full length of the original signal. This filtering corresponds to the passive high pass filter. This filtered signal is then split into sections corresponding to a length 25 μs (one period of 40 kHz). Then each section is time reversed and filtered individually using the same high pass filter. In real implementation, this sectioning and filtering would be carried out in the DSP or FPGA. The time reversed filtering will nullify the phase shift introduced by the first filtering action. Finally, each section of the signal is time reversed again to obtain the $ZPF\ output$ signal. The $ZPF\ output$ is subtracted from the *original* signal to get the $difference$ signal. The subtraction represents the filtering action and $difference$ signal represents the final filtered signal. The time domain waveforms of all the signals are shown in Fig. 5.4a. From the Fig. 5.4a, the discontinuities due to the transients could be observed in both the $ZPF\ output$ and the $difference$ signal. These transients cause the output of the ZPF to include undesired harmonics such as 25 kHz, 55 kHz, 65 kHz, 80 kHz etc which could be observed from the FFT in Fig. In real systems with either ac or dc source, the power supply will have other frequency components from other converters connected to the same source or from the

same converter itself. Therefore, the cycle-by-cycle implementation is not suitable for most of the systems.

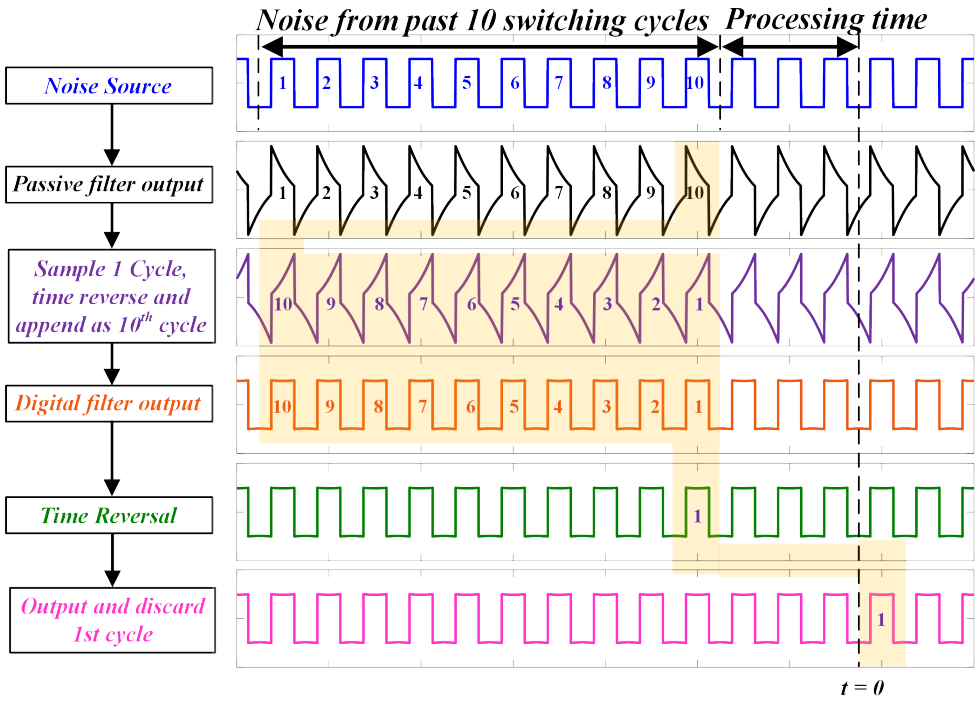


Fig. 5.5: Flowchart for multiple cycle implementation

Multiple cycle implementation

To ensure that the transients do not affect the performance of the filter, the length of the section of signal input to the digital filter should be longer than the impulse response of the digital filter [18, 23]. That is, the length of the signal for filtering should be longer than the length of the transients. This would result in impractical length of signals for real time filtering implementations. Previously, different implementations using overlap-add or overlap save methods [18] have been demonstrated to enable real time implementation of zero-phase filtering. In this work here, the overlap-save methods is used to implement the digital active EMI filter. Instead of sensing cycle-by-cycle, multiple-cycles are used. The implementation is as follows:

1. Save multiple switching cycle of noise data sensed using the passive high pass filter.

2. The stored signal is time reversed.

3. The digital filter is then applied to the time-reversed signal.

4. Save the last cycle of digital filtered data that is free from transients.

5. Time reverse the saved data and synchronize noise injection with the next switching cycle.

In multiple-cycle implementation, selecting the number of cycles is a crucial step. Firstly, the transients are characteristic of the digital filter. Ideally, signal of infinite length is required to negate the effect of the transients. But, depending upon the magnitude of the allowable distortion of the $ZPF\ output$, a finite section length is sufficient. The procedure to obtain the section length is as follows. A spectrum of the expected level of noise on the power supply is taken. For example, in an ac power source, the grid harmonics from the standard along with the conducted EMI levels from the CISPR-22 standard could be taken. These are plotted together in Fig.

5.5 FPGA implementation and Tuning of the ZPF AEF

5.5.1 FPGA implementation

The implementation of the zero-phase filtering is shown in Fig. 5.6. The high pass filter output is fed to the ADC. The time reversal is carried out using a last-in first-out (LIFO) register. One switching cycle of noise is stored and time reversed in the LIFO. The digital filter whose transfer function is same as that of the analog passive filter is implemented as transfer function in Verilog. Another LIFO is used for the time reversal that follows the digital filter. Finally, a first-in first-out (FIFO) register is used to implement the delay to synchronize the noise injection with that

of the next switching cycle. The process is continuously repeated. The P0035 AD/DA daughter card from Terasic that comprises of ADC AD9254 from Analog Devices and DAC DAC5672 from Texas Instruments. The sample rate of ADC and DAC are set at 100 MSPS. The Altera DE2-115 demo board with Cyclone IV EP4CE115 FPGA is used to implement the zero-phase filter. While the AD and DA operate at 100 MHz, the computation inside the FPGA is carried out only at 10 MHz to ensure that the multiple-cycle implementation with 10 cycles can be implemented. Therefore, at frequencies above 1 MHz, the sample sizes are insufficient to prevent aliasing which may in turn result in instability or signal distortion. In order to avoid these, a zero-phase low-pass filter with corner frequency of 2 MHz is added.

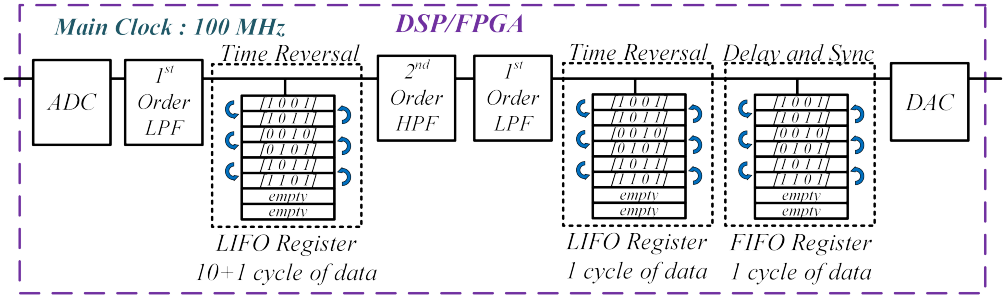


Fig. 5.6: Proposed zero-phase filtering implementation in DSP/FPGA for digital AEF

5.5.2 Tuning Procedure

The circuit used for tuning the digital AEF is shown in Fig. 5.7a and the methodology for tuning is shown in Fig. 5.7b. There are 3 parameters that needs to be tuned. They are the gain, the processing delay and the pole locations. The procedure for tuning is as follows:

Step 1: Disconnect the HPF from the circuit. Set the pole location of digital filter to 0 Hz. Apply a small signal ac source to ADC input and verify unity gain at the DAC output. Adjust gain if necessary. Step 2: With the pole location of digital filters at 0 Hz, apply small signal square wave source to ADC input. Measure ADC input and DAC output and calculate delay. This is the

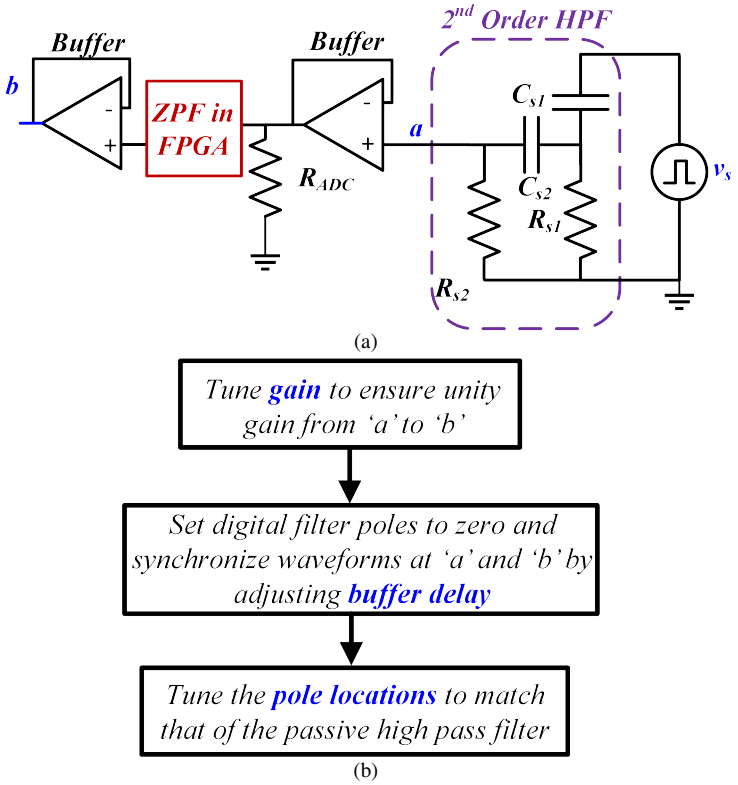


Fig. 5.7: (a)Test setup for tuning (b) Methodology for tuning

delay introduced due to the processing of the zero-phase implementation. Set this delay in FIFO to synchronize the input and the output. Step 3: Connect the high pass filter back in the circuit. Apply small signal square waveform to the input of the high pass filter. Tune the pole locations so that there is no distortion between the input and the output of the DAC.

5.6 Modeling and stability analysis

This section discusses the Modeling and Stability analysis of the proposed zero-phase filtering based digital active EMI filter with multiple-cycle implementation. The filter is implemented in a feedforward voltage-sense voltage-cancellation topology. While the feedforward implementation is inherently more stable, still the stability needs to be ensured in the entire frequency range. The schematic of the test setup is shown in Fig. 5.8 and the block diagram of the implementation

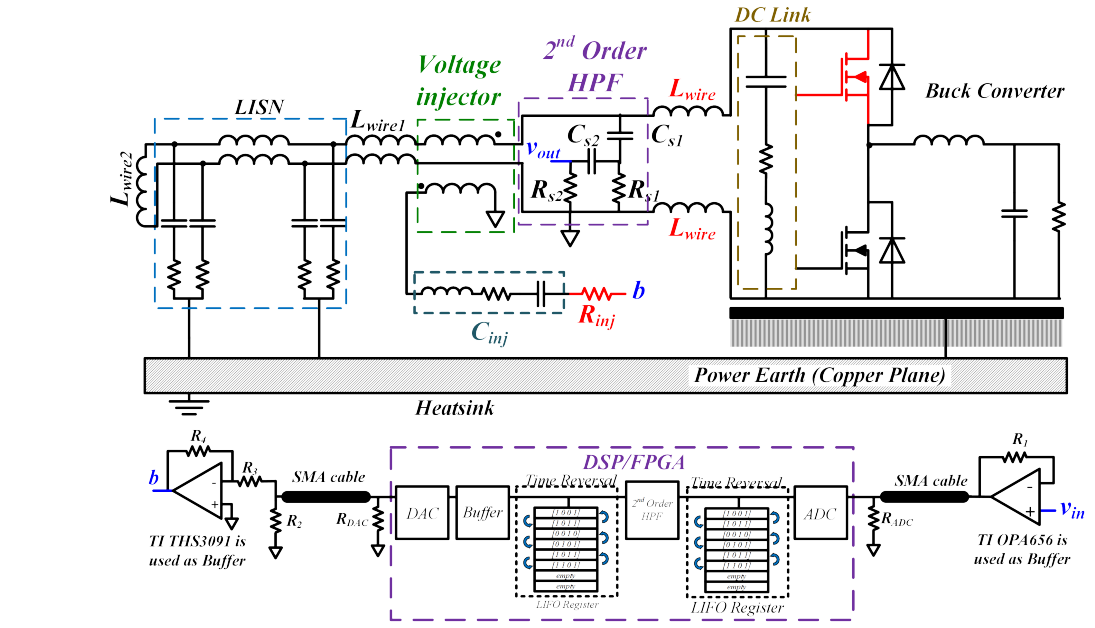


Fig. 5.8: Experimental results with converter

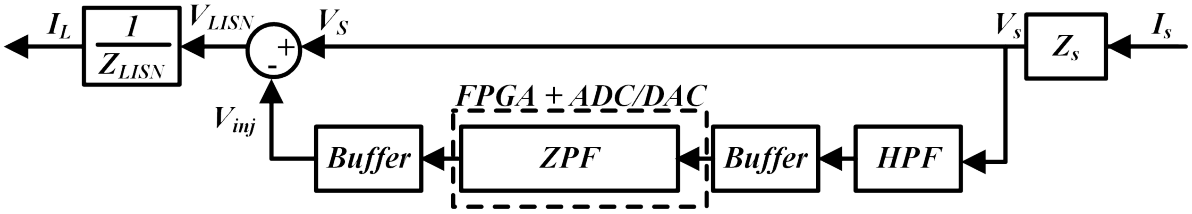


Fig. 5.9: Block diagram of Zero-phase filtering based digital Active EMI filter

is shown in Fig. 5.9. From Fig. 5.8, the voltage injector is implemented using a nano-crystalline core based inductor. The voltage injector consists of primary and secondary with 4 turns each implemented on VAC w453 core. Noise sensing is carried out using a second order high pass filter is fed to the AD/DA circuit. There are buffers present both at input and the output stages of the FPGA for impedance matching. Also, in order to prevent the voltage injector from saturating due to any dc offset voltages that might be present at the DA buffer, a series capacitance C_{inj} is added. In order to carry out the stability analysis, firstly the transfer gain of the zero-phase filtering implementation in the FPGA is measured. This is then followed by the loop-gain measurement and equivalent circuit development.

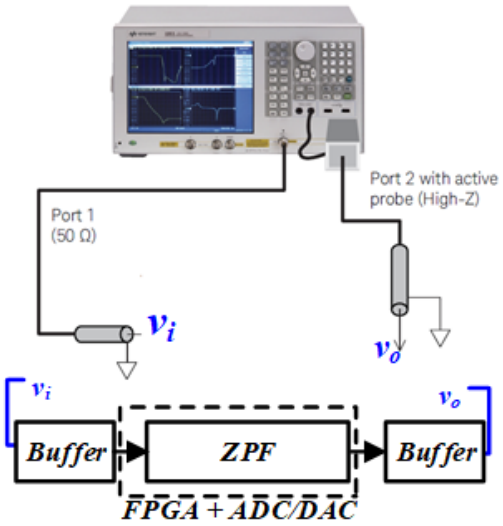


Fig. 5.10: Measurement setup for transfer gain of the FPGA

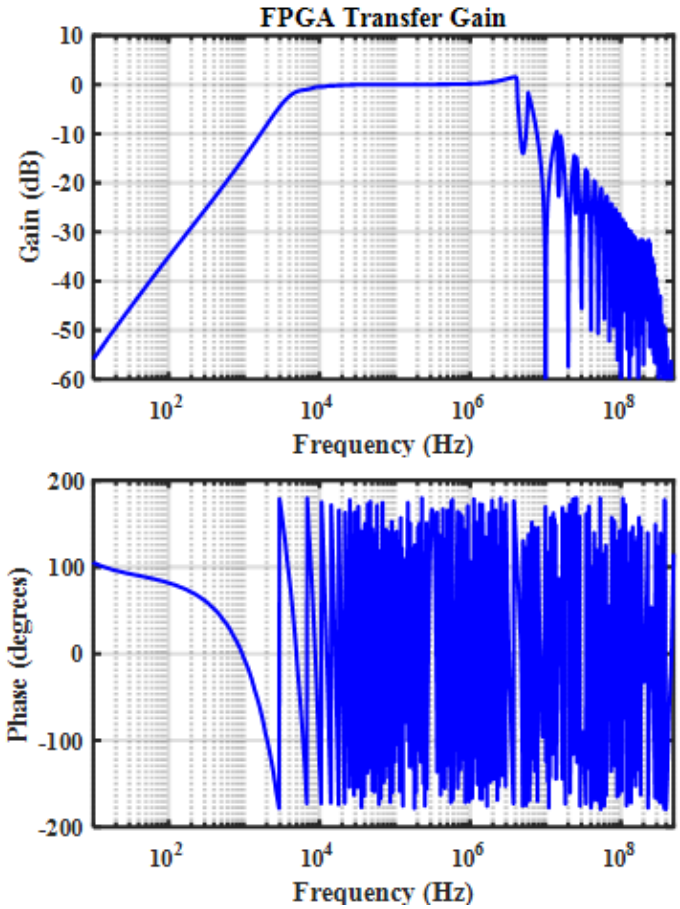


Fig. 5.11: Measured transfer gain of the FPGA implementation

5.6.1 Transfer Gain of FPGA implementation

The zero-phase filtering implementation in the FPGA is carried out as explained in section 5.5.1. This ensures that the sytem does not become unstable at high freqeuencies. Measurement of the transfer gain is carried out using the Keysight E5061B Vector Network Analyzer and Keysight 41800A 500 MHz probe. The measurement setup is shown in Fig. 5.10. The small-signal excitation from the VNA is applied to the input of the buffer which has a matching 50 Ω impedance. The response is measured at the output buffer is measured using the RF probe. This is done to avoid loading the output buffer which might affect the measurement. Further, the RF probe has very low capacitance (2 pF) and therefore ensures good high-frequency measurement. Also, the phase measurement is going to jump between -180 degrees and +180 degrees in the measurement due to the 10 cycle delay that is introduced in the FPGA. The mesurement is shown in Fig. 5.11. It can be seen that at low frequencies ($<$ 150 kHz), the transfer function is similar to that of the high pass filter and at high frequencies ($>$ 2 MHz), the gain reduces due to the low-pass filter. As mentioned previously, the computation in the FPGA is carried out at 10 MHz. This causes aliasing at 5 MHz and its multiples and is the reason there are resonances at 5 MHz and its harmonics.

5.6.2 Loop Gain of zero-phase filtering based digital active EMI filter

In order to measure the loop-gain of the filter, the loop is broken at a point such that the impedance seen by any part of the circuit is not affected. The loop is broken after the high pass filter at the input of the buffer. The high input impedance of the buffer ensures that the impedance seen by other parts of the circuit remain largely unchanged. The measurement setup is shown in Fig. 5.12 and uses the same equipment as the FPGA transfer gain measurement. The measured

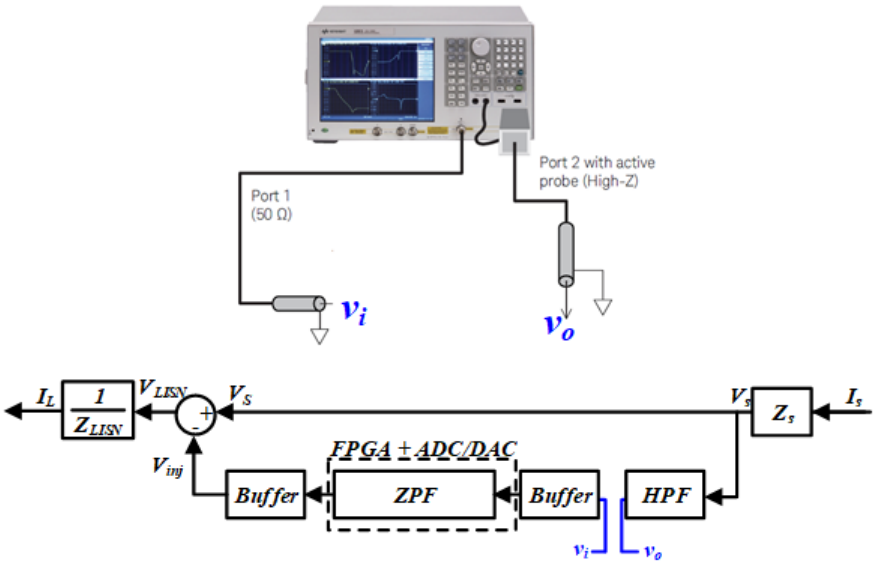


Fig. 5.12: Measurement configuration of loop gain of the zero-phase filtering based digital active EMI filter

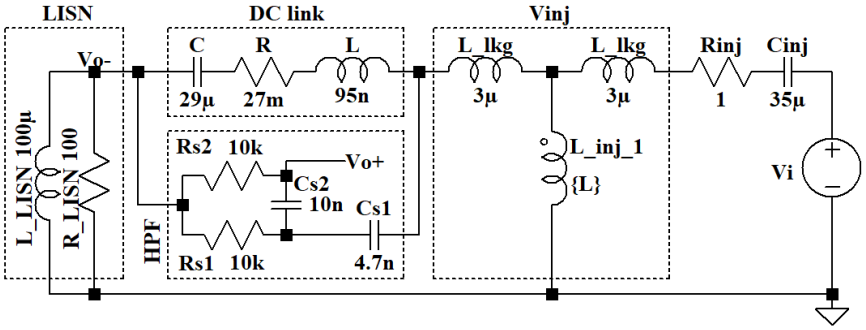


Fig. 5.13: Simulation model for loop gain estimation

loop-gain is the blue curve shown in Fig. 3.16. It can be seen that around 4 kHz, the gain margin is low. This is due to some resonance in the circuit. While this is occurring below the EMI frequency range ($<$ 150 kHz), it can still make the entire system unstable. In order to understand the source of the resonance, an equivalent circuit simulation representing the measurement configuration is setup in LTSpice. The simulation schematic is shown in Fig. 5.13. The simulation is mainly used to identify the source of resonance and not to accurately match the loop-gain from the experiment. Further, the voltage injector is modeled as T-network with a constant inductance value with the leakage inductance measured separately using the impedance analyzer. This is not accurate be-

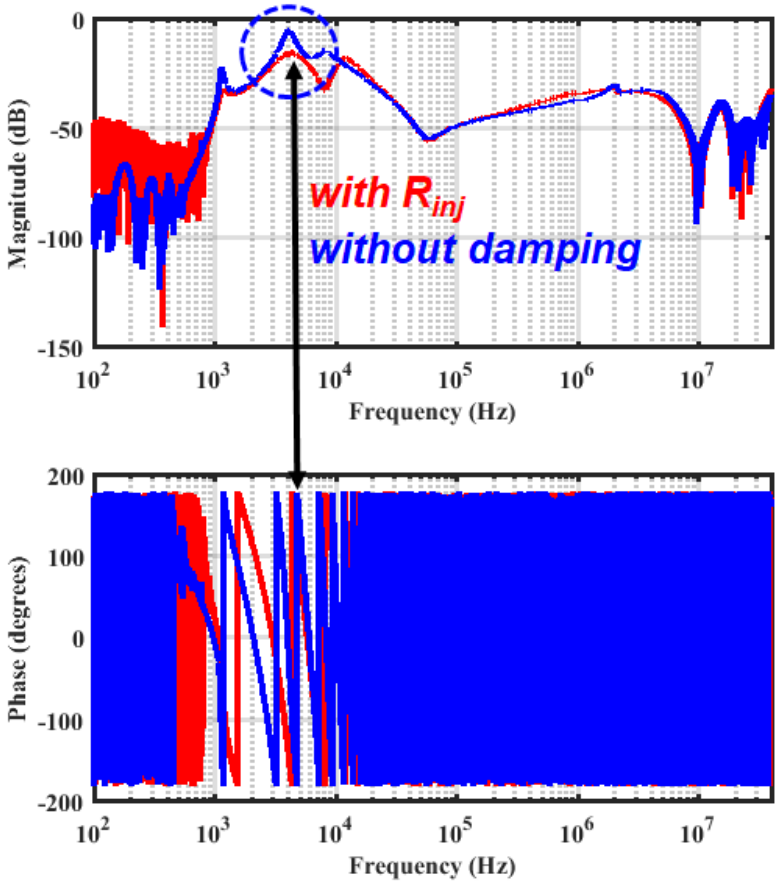


Fig. 5.14: Comparison of loop-gain with and without R_{inj}

cause the inductor uses a nano-crystalline core and whose permeability changes with frequency. But, since the resonance that needs to be identified is happening at a few kHz, the assumption for the simulation is valid one up to few 10s of kHz. All the other components are also modeled for simulation. It is seen that the resonance at 4 kHz is due to the resonance between the injection capacitor (C_{inj}), and combination of LISN inductance (L_{LISN}) and the voltage injector mutual inductance (L_{inj}). This can be resolved by using a injection resistor (R_{inj}) in series with the voltage injector and the injection capacitor. This helps reduce Q of the resonance and improves the gain margin by 16 dB. This ensures that the filter is stable through out the entire frequency range. The match between simulation and experimental measurement of the loop-gain after addition of R_{inj} is

shown in Fig. 5.15.

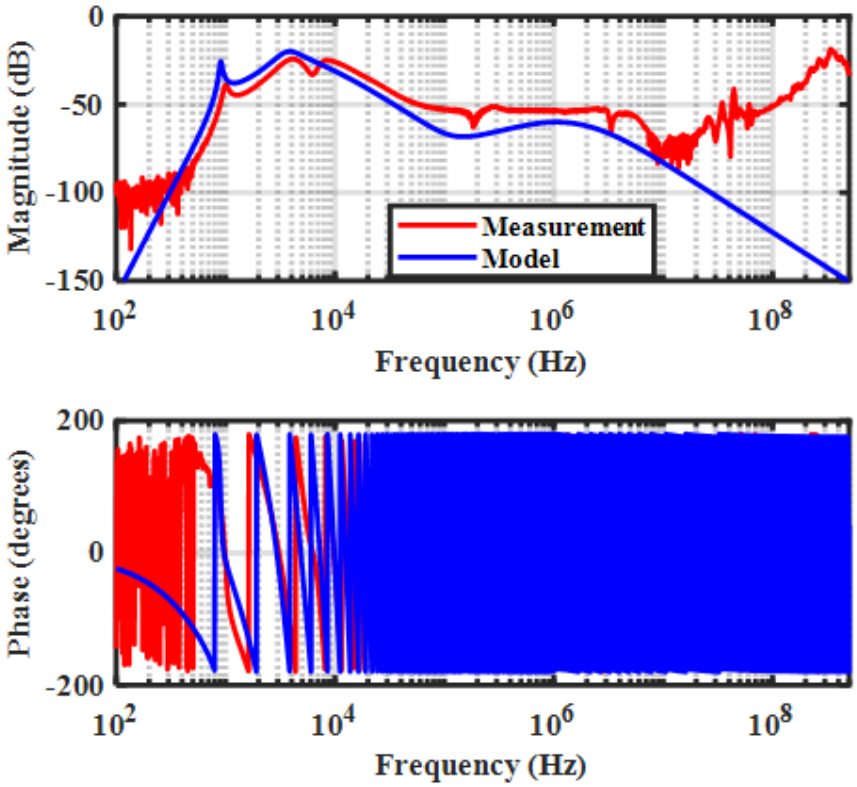


Fig. 5.15: Comparison of loop-gain from measurement and circuit simulation

While the

Previous discussion and the experimental measurement of loop gain dealt with frequencies only up to 30 MHz. While the FPGA has a low-pass filter with corner frequency at 2 MHz, the overall implementation of the filter could become unstable at frequencies above 30 MHz. Therefore, is essential to measure the loop gain at least till 500 MHz. While, the frequency of 500 MHz is limited by the active probe used for measurement, it still encompasses the bandwidth of the FPGA clock frequency (100 MHz), the bandwidth of the op-amps used in the buffer circuit (230 MHz). This way high-frequency instability due to any component could be identified. The measured loop-gain up to 500 MHz is plotted in red in Fig. 5.16. Throughout the entire frequency

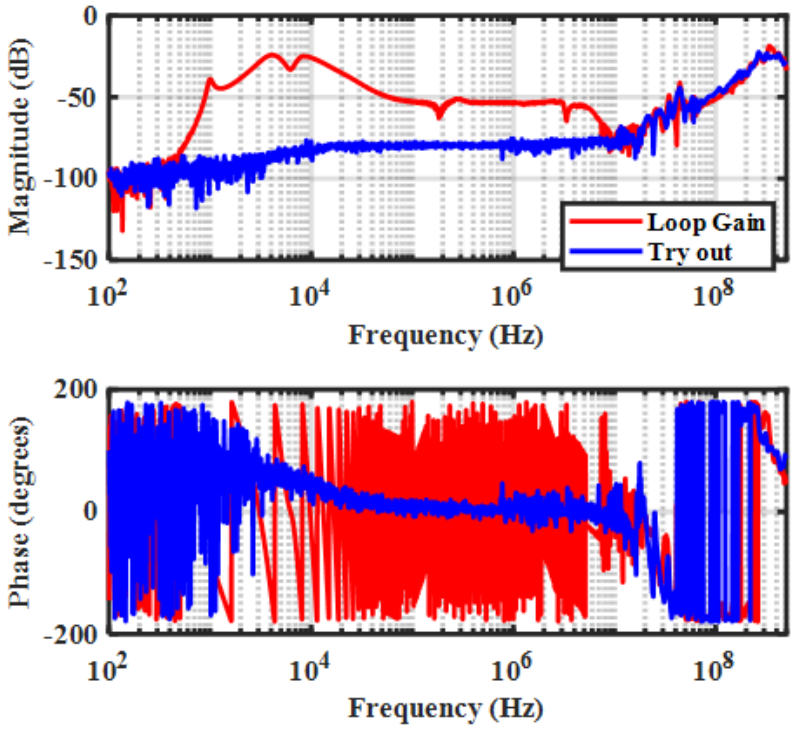


Fig. 5.16: Comparison of loop gain with the active circuit ON (Loop Gain) and OFF (Try out)

range, the filter seems to be stable. However, the gain margin at 400 MHz is only about 15 dB. This may cause the filter to become unstable when operating with the converter. Therefore, the source of this needs to be identified. The power to the FPGA and buffers is turned off, and the loop gain is measured. This is plotted in blue in Fig. 5.16. From the figure, the loop gains match each other above 10 MHz. This means some stray impedance that is not part of the converter nor the FPGA or buffer circuit is causing this.

In order to identify the reason behind this, an equivalent circuit schematic of the measurement setup with the power to the FPGA and the buffers turned-off is made in LTspice. The schematic is shown in Fig. 5.17. The excitation port of the VNA with the 50 Ω is modeled along with the impedance of the active probe connected to port 2 which measures the response. The high pass filter and the dc link capacitor are still present in the measurement, and therefore are included

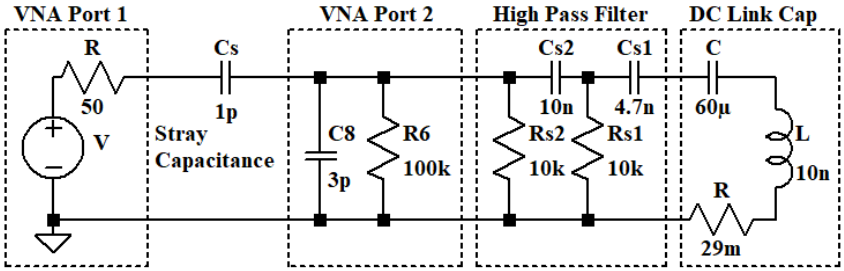


Fig. 5.17: Schematic of simulation to simulate the effect of the stray capacitance in the PCB on the loop gain measurement

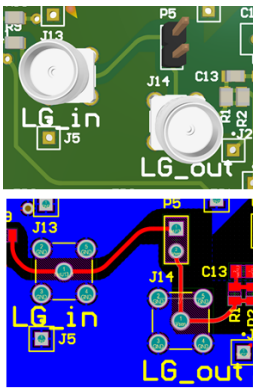


Fig. 5.18: PCB layout showing the SMA connector location for loop gain measurement on the board

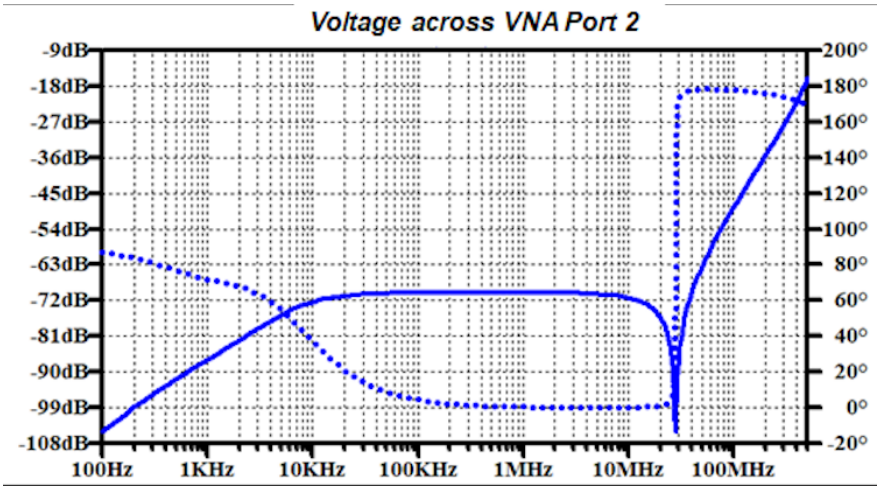


Fig. 5.19: Simulation of loop-gain to identify high-frequency effect

in the schematic. The snapshot of the PCB containing the two SMA ports used for loop-gain measurement are shown in Fig. 5.18. The header connecting the two ports is shorted during normal operation and is removed during loop-gain measurement. The stray capacitance between the two

SMA ports is assumed to be 1 pF. The simulated result is shown in Fig. 5.19. The simulation result is identical to the measurement in Fig. 5.17. Thus the high-frequency measurement is just due to the stray capacitance on the PCB between the measurement ports and does not affect the stability of the filter.

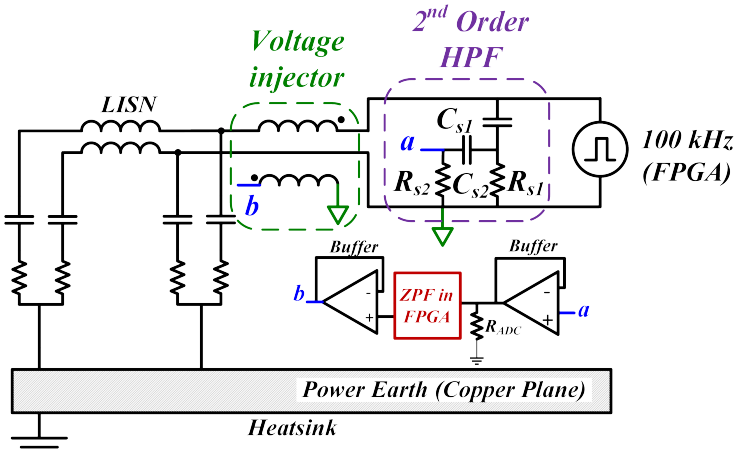


Fig. 5.20: Schematic of test setup for small-signal tests

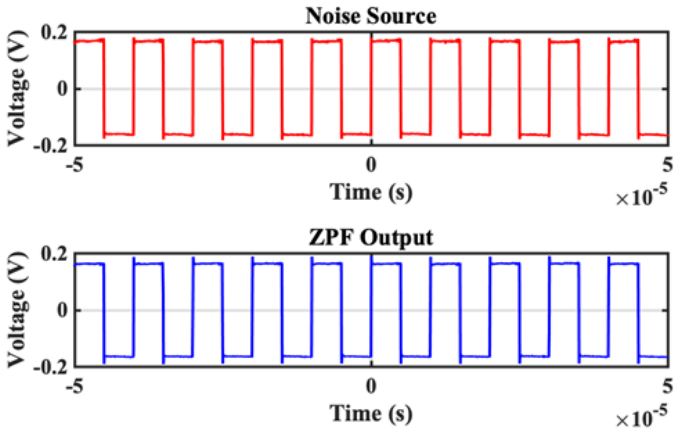


Fig. 5.21: Time-domain measurement results with signal-generator for multiple-cycle implementation

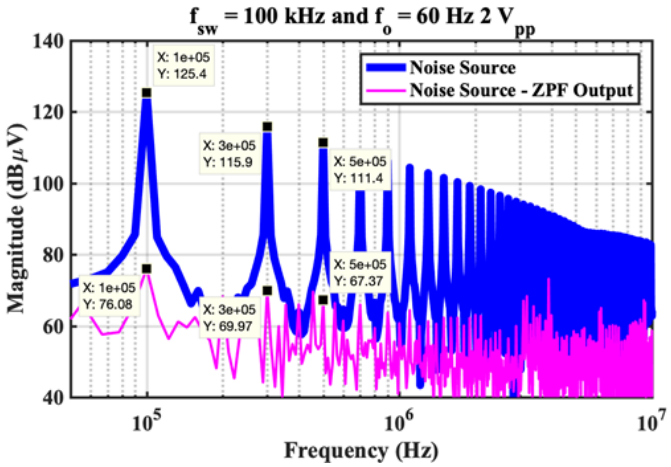


Fig. 5.22: Frequency-domain measurement results with signal-generator for multiple-cycle implementation

5.7 Small signal and converter experimental test setup and results

5.7.1 Small Signal Results

The ZPF AEF is demonstrated using a feed-forward voltage-sense voltage-cancellation topology for differential mode noise attenuation. A 100 kHz square wave signal is used as a noise source. The schemtaic of the test setup for small-signal tests is shown in Fig. 5.20. The tests are carried out under 2 conditions. First, the noise is measured without any filter. Then, the ZPF in FPGA is connected between the high pass filter and the voltage injector. The time-domain measurement is shown in Fig. 5.21. It can be seen that the output of the zero-phase filter has no distortions and closely follows the noise source. This reflects on the frequency domain noise measurements carried out in the EMI receiver. This is whon in Fig.5.22. With ZPF AEF, the attenuation is 49 dB, 46 dB and 44 dB at 100 kHz, 300 kHz and 500 kHz respectively.

The ZPF AEF is then tested in the converter. The schematic of the test setup is shown in Fig. 3.22 and the test setup is shown in Fig. 5.23 and 5.24. The power converter comprises of a CREE SiC half bridge configured as a buck converter switching at 40 kHz. The top device is

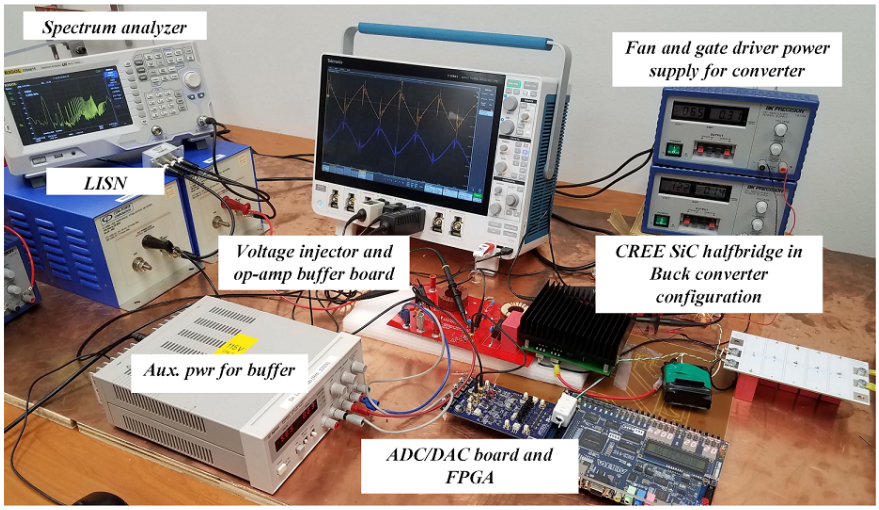


Fig. 5.23: Experimental test setup

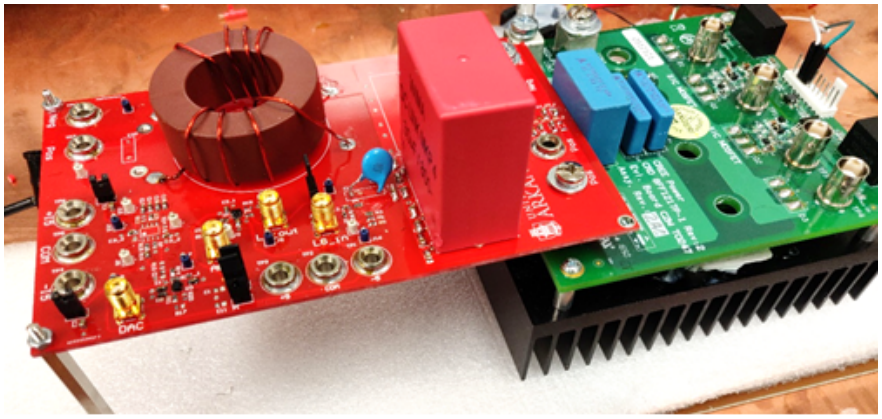


Fig. 5.24: CREE SiC half-bridge connected to PCB with V_{inj}, high pass filter and buffer circuitry with SMA connections to the ADC to DAC board

switched and the bottom device is kept off. The gate signal is fed from the same FPGA in which the ZPF AEF is implemented. This enables synchronizing the gate signal and the ADC/DAC board. The dc link for the converter, voltage injector, second order high pass filter and the buffers are implemented in a PCB and is connected to the SiC half bridge. Because the input of ADC and DAC are limited to 1.2 V, it is necessary to reduce any high frequency ringing that can have high magnitude. The noise measured with and without ZPF based AEF and is shown in Fig. 5.26. The attenuation at 120 kHz is 42 dB which is very close to attenuation from the small signal tests. The differential mode noise attenuation at 300 kHz and 500 kHz is 36 dB and 31 dB. This is limited by

the noise floor and the actual attenuation is higher.

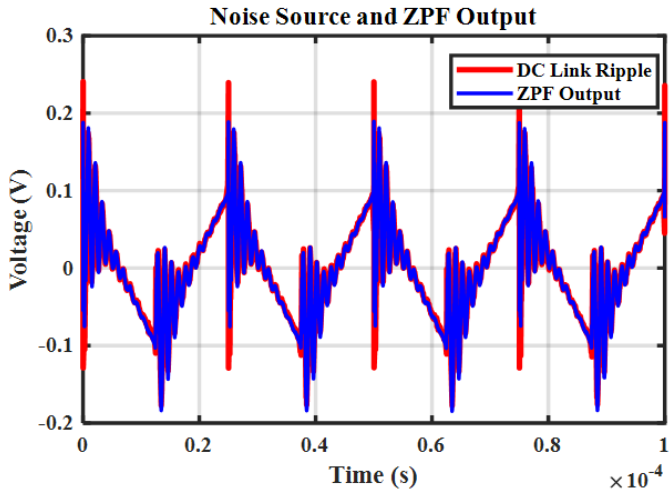


Fig. 5.25: Time-domain measurement results with converter for multiple-cycle implementation

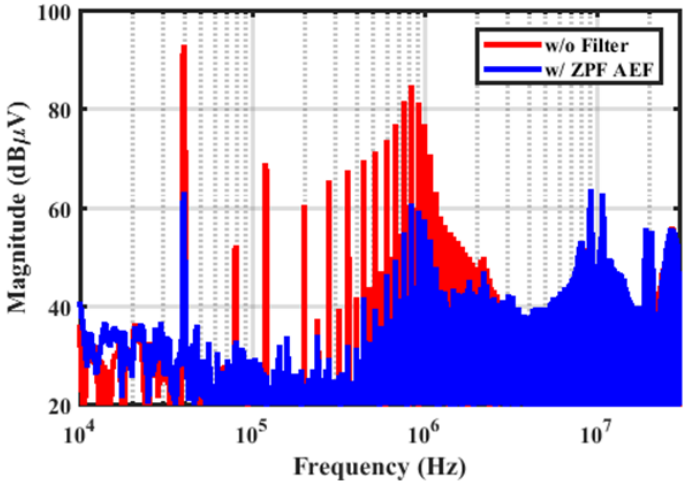


Fig. 5.26: Frequency-domain measurement results with converter for multiple-cycle implementation

5.8 Conclusion

Zero-phase filtering (ZPF) is a method to implement filtering without any phase distortion. This methodology was applied in a digital active EMI filter (AEF) to compensate the phase distortion introduced by the noise sensing passive high pass filter. The architecture for implementation

in the FPGA was presented. The modeling of the entire system with the filter is carried out and steps to improve the gain margin is presented. The ZPF based digital AEF is demonstrated using a simple feed-forward voltage-sense voltage-cancellation filter for differential mode noise attenuation. The small signal test results test results show up to 43 to 59 dB attenuation from 100 to 500 kHz. Converter test results show attenuation of 42 dB attenuation around 120 kHz. This is the highest attenuation reported with a single order filter around 150 kHz with analog or digital active EMI filters. This idea could be extended to any type of active EMI filter for both common mode and differential mode noise attenuation.

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6 Conclusion and Future Work

6.1 Conclusion

From the literature review in Chapter 2, there are numerous AEF implementations for conducted EMI mitigation in power electronic converters. Different implementations of the AEF topologies have been summarized based on the noise-sensing, noise processing active circuits, the control methods, noise-injection and stability studies for dc-dc, ac-dc converters, and inverters (dc-ac and ac-dc-ac). Different sensing and cancellation methods have different advantages and disadvantages for implementation in terms of volume reduction. Careful attention must be paid to the stability, which depends on the type of converter and the type of noise in order to select the appropriate AEF. Only then the attenuation and possible volume reduction with AEF could be maximized. The key points in terms of performance (attenuation), power loss and protection of AEF are as follows. Looking at the performance comparison, it is more challenging to achieve high attenuation at lower frequencies (around 150 kHz) using AEF than to design the filter for high attenuation at 1 MHz. Further, majority of these implementations uses additional high-voltage passive elements for compensation to ensure stability or rely on inductors either in the form of CTs for noise-sensing or voltage transformers for noise-cancellation. Novel methods that could further enhance the performance of the filter without the need for additional high-voltage capacitors for stability improvements or injection transformers on power lines are required. The state-of-art implementation of active EMI filter for DM noise implementation has an attenuation of 34 dB at 150 kHz using feedback current-sense current-cancellation active EMI filter. This additional overhead as a result of the current-transformer and additional high-voltage capacitor for stability improve-

ment reduces the volumetric benefits of using an active EMI filter. Three different approaches that do not use additional magnetics or high-voltage components is presented in Chapters 3 to 5 in this dissertation.

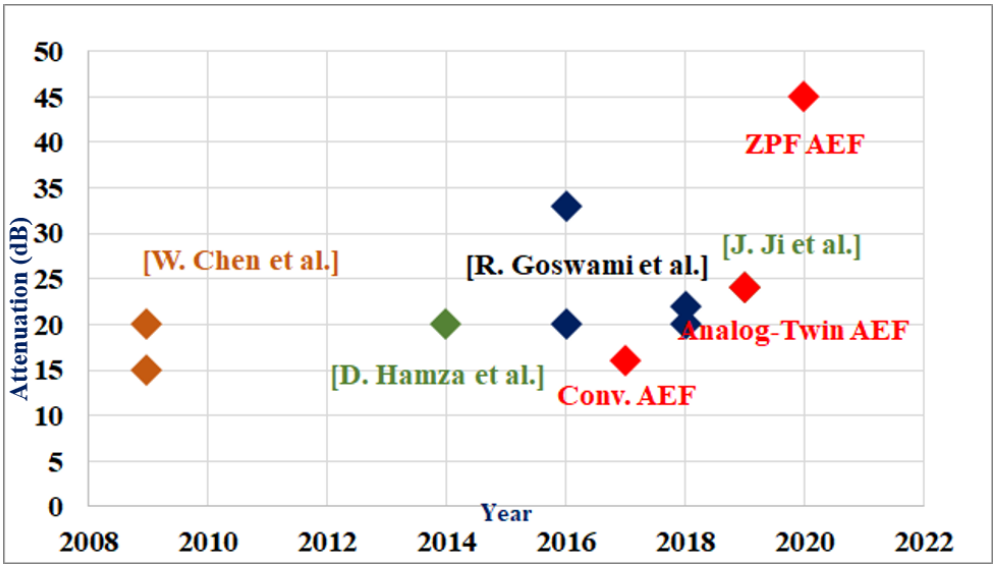

Fig. 6.1: Comparison of attenuation at 150 kHz of proposed active EMI filters against state-of-art analog and digital active EMI filters for ac-dc applications

In a conventional active EMI filter presented in Chapter 3, the non-linearity in the noise-sensing circuit and the active circuit introduce phase shift and result in instability. To ensure stability, either the gain of the active circuit has to be lowered or additional high-voltage components will have to be used. These additional passive components reduces the overall volumetric benefits of using an active EMI filter. A conventional active EMI filter is developed for an RCD clamped Flyback converter and could only achieve 16 dB attenuation around 150 kHz. Next, an analog-twin based active EMI filter which enables using low-voltage components for compensation is proposed and discussed in Chapter 4. This requires good matching between components in the high-voltage and low-voltage circuit for high attenuation. With this implementation, an attenuation of 22 dB was achieved around 150 kHz. While this is definitely an improvement over conventional active EMI filtering, it does not significantly improve the attenuation. Finally, a zero-phase filtering based

digital active EMI filter that overcomes the limitations of both conventional and analog-twin based active EMI filter is proposed. The proposed method completely nullifies the phase shift introduced by the sensing stage, and therefore enables attenuation of the order of 45 dB without the need for additional high-voltage components for compensation. This is the highest reported attenuation in the literature for any analog or digital active EMI filter. A comparison of attenuation of the proposed filters against the state-of-art is shown in Fig. 6.1. It can be seen that the digital active EMI filter with zero-phase filtering has 15 dB higher attenuation than any implementation without the need for any additional magnetics or high-voltage components. Further, modeling stability analysis, design example, and experimental verification is carried out for all three types of active EMI filters.

6.2 Future Work

Based on the literature review, the need for new topologies or implementations with high attenuation was identified and demonstrated. However, the experimental results were limited to a particular type of converter (constant duty cycle) or by the availability of the AD/DA and FPGA hardware. The following needs to be carried out as part of the future work to further research in this area:

1. Extend conventional active EMI filter to inverters. In particular, the motor drives for aerospace applications where cost premium is acceptable provided there is weight saving.

2. For analog twin based active EMI filter, extend to more converters and study the variability of attenuation with component tolerances, temperature, and grid-impedance variations.

3. For the digital active EMI filter, implement in current-cancellation topologies while using feedback control method. With the feedback control method, the filter could be easily adopted

to inverters with ease.

4. For all topologies of active EMI filter, the auxiliary power supply, power loss and protection need to be studied.

5. Further, a Figure of Merit (FoM) for implementation of active EMI filters taking into account the volume reduction of passive components at different power levels and for different power converters is an important one that requires further research.

A List of published and submitted work

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