7-2020

Converter- and Module-level Packaging for High Power Density and High Efficiency Power Conversion

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Converter- and Module-level Packaging for High Power Density and High Efficiency Power Conversion

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy in Engineering with a concentration in Electrical Engineering

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July 2020
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Abstract

Advancements in the converter- and module-level packaging will be the key for the development of the emerging high-power, high power-density, high-efficiency power conversion applications, such as traction, shipboards, more-electric-aircraft, and locomotive. Wide bandgap (WBG) devices such as silicon carbide (SiC) MOSFET attract much attention in these applications for their fast switching speeds, resulting in low loss and a consequent possibility for high switching frequency to increase the power density. However, for high-current, high power implementations, WBG devices are still available in small die sizes. Multiple SiC devices need to be connected in parallel to replace a large IGBT die. It is challenging to realize high-switching-frequency and low loss with a lot of parallel devices due to the inherent parameter differences, which lead to unbalanced dynamic current sharing resulting in unequal temperature distribution and overstress. Apart from the technical challenges, the price of SiC modules is another roadblock for its widespread application. The paralleling of a large number of SiC chips in the module to handle high current increases the module cost. Hence, this work proposes a Si-IGBT and SiC-MOSFET-based hybrid switch solution. For a converter-level packaging, the device technology, available device package, and orientation of the pins are the essential governing factors. This work addresses the converter-level packaging, which is referred to as a power electronics building block, of the proposed hybrid switch, combining discrete packages and frame-based modules for the devices and a single-phase three-level T-type topology. The primary optimization objective for converter-level packaging includes low inductance busbar design, high efficiency, and high specific and volumetric power density. Overall implementation is not trivial; however, this work achieves an optimum design compared to the state-of-the-art. The module-level packaging challenges

are dependent on the type of device technology and topology. Reducing the parasitic inductances, capacitances, and the junction to case thermal resistance are the optimization objectives in module packaging. Given the intended application of the module, achieving a high-reliability module is also essential. This work includes a hybrid switch-based power module addressing the challenges of WBG module-level packaging and challenges specific to the hybrid switch. The availability of engineering samples of SiC MOSFETs with voltage ratings above 10 kV and commercialization in the future drive the module-level packaging of high voltage devices. High voltage power modules will support the development of future solid-state circuit breakers, transformers, and power conversion applications in shipboards and rolling stocks. The availability of these modules can eliminate the necessity of multi-level topologies. This work investigates and demonstrates the module-level packaging of HV (10-15 kV) SiC MOSFETs.

Acknowledgements

I would like to convey my sincere gratitude and appreciation to my research advisor Dr. Fang Luo for his unconditional support and advice throughout my dissertation work. I wouldn't have completed the dissertation work without the support that Dr. Luo has provided me throughout the years of my degree.

I would also like to take this opportunity to thank Dr. Juan C. Balda, Dr. Yue Zhao, and Dr. David Huitink for their consent to serve as my committee members. I appreciate the time and support they have provided me.

I would like to thank the staff members of High-Density Electronics Center (HiDEC). Tom Cannon, Kaoru Uema Porter, Errol Porter, and Clint Hardee has always been extremely helpful. I have always received utmost cooperation and help from all of them when I needed it most. They have unconditionally contributed a lot of effort to make my research a success.

I would like to thank all my lab colleagues Balaji Narayanasamy, Zhao Yuan, Asif Imran, Hongwu Peng, and Riya Paul. I am also thankful to Si Huang, Andrea Wallace, Zeke Zumbro, Junji Ke, Ange Iradukunda, Hayden Carlton, Reece Whitt, Mahsa Montezari, Tristan Evans, Imam Al Razi, Shilpi Mukherjee, Quang Le, and Zhongjing Wang whom I have worked with during my time at University of Arkansas.

Lastly, I want to mention my parents, Rajendrakumar Deshpande and Uma Deshpande. They always encouraged and motivated me to pursue a Ph.D. degree. They have always been the greatest inspiration and support of my life. Whatever I am as a person today, it is due to their support and affection.

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2. A. Deshpande, Y. Chen, B. Narayanasamy, Z. Yuan, C. Chen, and F. Luo, "Design of a High-Efficiency, High Specific-Power Three-Level T-Type Power Electronics Building Block for Aircraft Electric-Propulsion Drives," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, pp. 407-416, 2020. [Published, Chapter 3 consists of this paper]

3. A. Deshpande, A. I. Emon, R. Paul, Z. Yuan, H. Peng, and F. Luo, "High Power Density 1700-V/ 300-A Si-IGBT and SiC-MOSFET Hybrid Switch-based Half-bridge Power Module," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, 2020. [Accepted and Submitted Final Paper Manuscript, Chapter 4 consists of this paper]

1 Introduction

1.1 Background and Motivation

High-power, high power-density, high-efficiency power conversion applications, such as traction, shipboards, more-electric-aircraft, and locomotive, pose increasing demand for high-current high-performance power modules and converters. High power-density is achievable using higher switching frequencies for the power semiconductor devices. Silicon (Si) IGBT is usually limited to a switching frequency of 20 kHz, considering the slow switching characteristics and high turn-off loss in the IGBT, due to the tail current. Wide bandgap (WBG) devices such as silicon carbide (SiC) MOSFET attract much attention in these applications because of their capability of fast switching speed, resulting in low loss and possibility for high switching frequency. However, SiC devices are still available in small die sizes. For example, the largest 1.7 kV SiC MOSFET bare die size is 7.35 mm x 4.08 mm with 72 A current rating. Whereas, the largest 1.7 kV Si IGBT bare die is 15.93 mm x 16.88 mm with 225 A current rating. Multiple SiC devices need to be connected in parallel to replace a large IGBT. However, it is challenging to realize high switching frequency and low loss with several paralleled dies. This challenge is due to the inherent parameter differences, which lead to unbalanced dynamic current sharing resulting in unequal temperature distribution and overstress. Apart from the technical difficulties, the price of SiC per ampere is another roadblock for its widespread application. The paralleling of a large number of SiC chips in the module to handle high current increases the module cost.

The module-level packaging challenges are dependent on the type of the device tech-

nology involved, i.e., Si IGBT or WBG such as SiC MOSFET or GaN HEMT. For example, the fast switching speed of WBG devices will generate high voltage overshoot if the parasitic inductances in the package are high. Also, the parasitic capacitances allow large common-mode currents to flow to the ground. The voltage overshoots stress the devices and reduce their lifetime, while the voltage oscillations and common-mode current cause electromagnetic interferences (EMI). Reducing the parasitic inductances and capacitances is a significant optimization objective in module packaging. However, high current-rated modules have their own set of challenges. Due to the demand for high power density modules, the devices have low spacing, which mandates a small thermal resistance layer stack between the junction and case. For a given application, achieving high-reliability is also essential. The module should utilize the full potential of WBG devices. However, the materials have primarily remained the same, which makes the module-level packaging challenging.

The converter-level packaging is dependent on the type of package and the available orientation of pin-outs. This type of packaging mandates an optimized module-level package. However, converter-level packaging is also reliant on the requirements of the topology and module availability. A combination of topology and module may render the converter-level packaging as non-trivial. The primary optimization objective for converter-level packaging includes low inductance busbar design and high specific and volumetric power density.

High voltage power modules are needed for solid-state circuit breakers, transformers, and power conversion applications such as shipboard and rolling stock. The availability of these modules can eliminate the necessity of multi-level topologies. The commercial availability of SiC MOSFETs with voltage ratings above 10 kV soon is the driving force behind the module-level packaging of these devices. The module-level packaging of HV

(10-15 kV) SiC MOSFETs has its own set of challenges.

1.2 Objectives of Dissertation

This dissertation aims to introduce a cost-effective and high-performance solution for a high-current power conversion application. This solution entails the demonstration of a Si-IGBT and SiC-MOSFET-based hybrid switch. Further, this dissertation intents to demonstrate the converter- and module-level packaging of a Si-IGBT and SiC-MOSFET-based hybrid switch for high-current high-power applications. Moreover, a demonstration of a module-level packaging of high-voltage (15-kV) SiC devices is also an essential aspect of the dissertation. For each element of the work, this dissertation describes the challenges and addresses them with innovative solutions. Design, simulation, and experiments are performed for each aspect. The proposed solutions ensure high compatibility with high-volume manufacturing processes used in the industry. This dissertation provides methods to integrate them into high-volume manufacturing.

1.3 Organization

The remainder of the dissertation is structured into four chapters. Chapter 2 introduces the concept and comprehensive analysis of the Si-IGBT and SiC-MOSFET-based hybrid switch. The study is based on the discrete version of the hybrid switch, where separate packages of Si-IGBT and SiC-MOSFET were utilized. Chapter 3 presents the design and validation of a hybrid switch-based converter-level packaging for a single-phase three-level T-type power electronic building block. This converter-level packaging of the building block is based on discrete packages of Si-IGBT and SiC-MOSFET. Chapter 4 makes a case for the

module-level packaging of the Si-IGBT and SiC-MOSFET-based co-packaged hybrid switch. The chapter includes, in detail, the design, analysis, assembly, and test of a half-bridge hybrid switch power module. Chapter 5 presents the design and prototype of module-level packaging of high voltage devices rated for 15 kV. Chapter 6 concludes the work in this dissertation. It further highlights the future work for continued research and development.

2 Practical Design Considerations for a Si IGBT + SiC MOSFET Hybrid Switch: Parasitic Interconnect Influences, Cost and Current Ratio Optimization

A. Deshpande and F. Luo

2.1 Introduction

The requirements of the future power electronics conversion systems, such as electric propulsion drive and battery chargers in more electric aircraft (MEA) and electric vehicles (EV), are high power-density and high efficiency. To achieve this, efforts to reduce the volume and weight of the passives and the thermal management system are needed. These components significantly contribute to power converter's volume and weight. Switching the power devices at high frequency reduces the weight and volume of passives. Moreover, operating the power devices at high junction temperatures reduces the weight and volume for the thermal management system. In a state-of-the-art silicon (Si) insulated gate bipolar transistor (IGBT) based converters, the IGBTs typically switch below or at the manufacturer recommended maximum switching frequency of 20 kHz [1]. This choice of switching frequency takes into consideration the slow switching characteristics of the IGBT, especially

the high turn-off loss resulting from the tail current, which result in high switching losses; its low junction temperature capabilities. On other hand, though the wide bandgap (WBG) device, silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs), attracts a lot of attention in high power-density applications because of their capability of high switching frequency and high junction temperature operation, they have their share of limitations at present; full replacement of Si IGBTs with SiC MOSFETs is difficult. The major roadblocks include, 1.) availability of SiC MOSFETs in only small current levels (die sizes), 2.) high cost/ampere ($/A), rendering a high-current multi-chip SiC module expensive and 3.) difficulty to parallel multiple dies in high-current power modules while maintaining superior switching characteristics. Hence, as an intermediate approach, hybrid switch (HyS) consisting of a Si IGBT in parallel with SiC MOSFET has been proposed in recent literatures.

2.1.1 Hybrid Switch Concept in Previous Literatures

In early literature, such as [2–6], researchers proposed discrete package based low voltage hybrid switch using Si IGBT and Si MOSFET. This facilitates the soft switching of the slow Si IGBT and enables the hybrid switch as a high frequency switch as mentioned in [7]. Recent literature such as [8–13], adapted this hybrid switch to utilize the benefits of presently available WBG devices. A preliminary analysis on Si IGBT and SiC MOSFET based hybrid switch was presented in literature [8–12]; Si IGBT and SiC JFET based hybrid switch in [8, 14]; Si IGBT and gallium nitride (GaN) high electron mobility transistor (HEMT) in [12, 13]. The parallel operation of these devices, compared to a standalone Si IGBT, should produce a better switching performance due to the presence of a WBG device.

Also, reduction in the cooling mass and volume can be achieved by allowing SiC device operation at higher junction temperature. Applications such as DC-DC converters where the switching frequency and size of passives are directly related [15], a HyS will yield high power-density. A SiC/Si current ratio of 1:1 was used in [16] and [9]. However, a possible cost economy of using a smaller SiC/Si current ratio was introduced in [16]. Independently, a SiC/Si current ratio of 1:4 and 1:5 was used in [8] and [12] respectively.

2.1.2 Contributions and Organization of this Paper

In this paper, a HyS with a large Si IGBT device and small SiC MOSFET device (low SiC/Si current ratio below unity) in parallel is proposed, as shown in Fig. 2.1 for high-current high-power converters. Also, the available Si+SiC gate sequence control options and their merits/demerits are highlighted. A systematic analysis on the influence of the parasitic interconnection inductance unbalance between Si and SiC within the HyS was not well studied. In this paper, using a parametric sweep, a systematic study on the influence of the parasitic interconnection inductance unbalance between Si and SiC device within the HyS is studied. A boundary-line of inductance unbalance is estimated, which helps to decide between available gate control options. Next, a comprehensive cost analysis was performed using commercial 1.2 kV devices. It was found that with a 1:4 and 1:6 SiC/Si current ratios, the cost for discrete device based HyS at currents above 50 A will be 50 to 75% lower compared to SiC device with identical current rating. Moreover, a maximum of 60% cost saving is achieved at 300 A, when comparing 1:6 current ratio module based HyS with an identical current rated SiC module. And, in the 300 A to 1200 A current range, the HyS will serve as a direct and the only replacement option for Si IGBT module. While the authors in

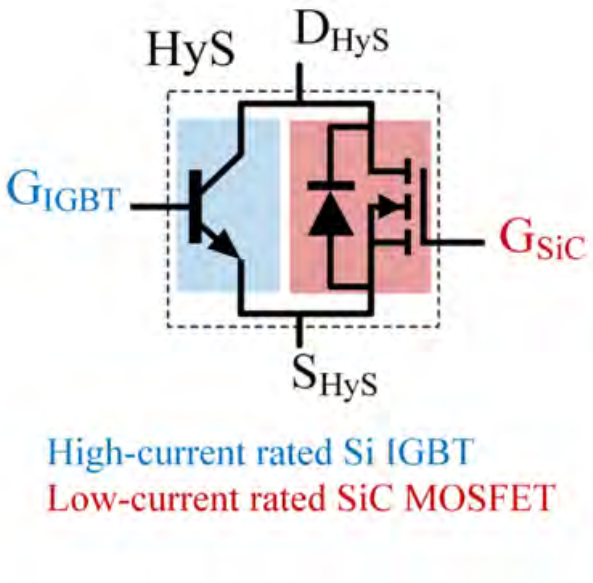

Figure 2.1: A Si IGBT + SiC MOSFET hybrid switch.

[8] and [12] use a 1:4 and 1:5 current ratio respectively, a justification of the particular sizing and its reliability were not reported. An algorithm using a dynamic junction temperature prediction is presented, to select an optimum SiC/Si current ratio, while ensuring a reliable HyS operation. Moreover, it is demonstrated with the aid of a design example that, 1:6 ratio HyS is possible, with the availability of an improved package, while using a lighter cooling system, enabling high specific-power density. From the experiment results, the savings in the switching loss by using the gate control option 3 are highlighted, which will allow the HyS based converter operation at high frequency to achieve high-power density. Finally, a 650 V Si IGBT and SiC MOSFET based HyS with a 1:5 SiC/Si current ratio was successfully demonstrated in a DC-DC boost converter. Also, EMI noise measurements and analysis is presented for the HyS based converter operation.

The organization of this paper is as follows: First, the principle of static current sharing in HyS is described in section II. Next, in section III, several available gate sequence

Table 2.1: 650 V devices used for simulation and experiment

Device	Purpose	Part#	Package	Manufacturer	Rating	$V_{CE(SAT)}$ $R_{DS(ON)}$
Si IGBT w/o Anti-parallel diode	Constitutes the HyS	IGW75N60T	TO-247	Infineon	600 V, 75 A	1.5 V
SiC MOSFET	Constitutes the HyS	SCT2120AF	TO-220	ROHM	650 V, 29 A	120 mΩ
SiC Schottky Barrier Diode	Top device in double pulse test	CVFD20065A	TO-220	CREE	650 V, 20 A	-

control options are summarized and the best control option for best switching performance for the HyS is highlighted. The systematic analysis of the effects of the parasitic interconnection inductance unbalance in the HyS, investigated using a parametric study in described in section IV. Further, based on the boundary-line inductance unbalance derived from the parametric study, suitable gate control options are recommended. Section V, presents the cost analysis. Further, an optimization algorithm derived for optimum SiC/Si current ratio sizing is presented in section VI. The experiment results are presented in section VII, which includes the EMI analysis of the HyS based converter.

$$I_{load} = I_{SiC} + I_{Si} = 2I_{sp} \tag{2.1}$$

$$\text{Light-load condition} \ : \ I'_{load} < 2I_{sp} \tag{2.2}$$

$$\text{Heavy-load condition} \ : \ I'_{load} > 2I_{sp} \tag{2.3}$$

2.2 Principle of Hybrid Switch: Static Current Sharing

The hybrid switch proposed in this paper consists of a large current rated Si IGBT and small current rated SiC MOSFET. The SiC MOSFET takes care of switching transitions

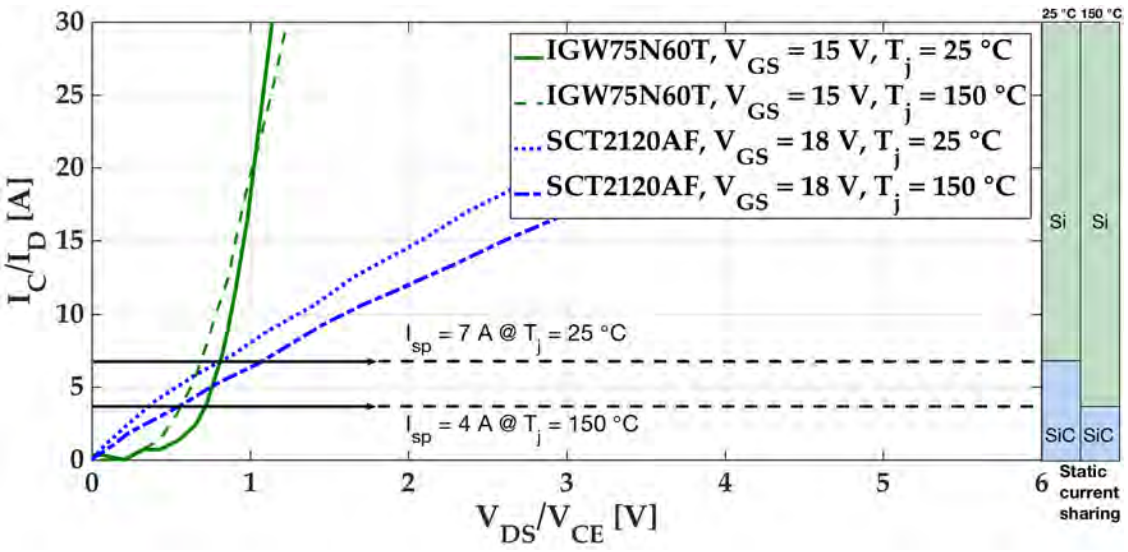

Figure 2.2: Static current sharing in a 650 V Si IGBT + SiC MOSFET HyS

while the Si IGBT takes care of static current conduction. This combination is expected to achieve low switching loss, consequently high switching frequency, at high current capacity. During steady conduction state, a Si IGBT has a low conduction power loss, at heavy-load conditions when compared to a SiC MOSFET. This is due to its fixed on-voltage ($V_{CE(SAT)}$) characteristics contrary to a fixed on-resistance ($R_{DS(ON)}$) in a SiC MOSFET. However, a 0.7 V forward PN junction barrier in Si IGBT, leads to a high conduction power loss, at light-load conditions for Si IGBT when compared to SiC MOSFET. Hence, a HyS, which includes a Si IGBT in parallel with a SiC MOSFET, should provide an inherent low conduction power loss for both light-load as well as heavy-load conditions. This is evident when the static I-V characteristics of both Si IGBT and SiC MOSFET devices (listed in Table 2.1) are superimposed as shown in Fig. 2.2. The Si IGBT in consideration is IGW75N60T (600 V/ 75 A) from Infineon and the SiC MOSFET is SCT2120AF (650 V/ 29 A) from ROHM. As shown in Fig. 2.2 and (2.1), the Si IGBT and SiC MOSFET share equal current, which is referred to as a sweet point (I_{sp}), while to load current (I_{load}) is twice of I_{sp} with an

$$E_{sw,IGBT-only} = \int_0^{t_{sw,on}} V_C I_C dt + \int_0^{t_{sw,off}} V_C I_C dt = E_{sw,ON,IGBT,HARD} + E_{sw,OFF,IGBT,HARD} \tag{2.4}$$

$$\begin{aligned} E_{sw,HyS,Op-3} = & \int_1^2 V_{HyS} I_D dt + \int_3^4 V_{HyS} I_C dt + \int_5^6 V_{HyS} I_C dt + \int_6^7 V_{HyS} I_D dt \\ & = E_{sw,ON,SiC,HARD} + E_{sw,ON,IGBT,SOFT} \\ & + E_{sw,OFF,IGBT,SOFT} + E_{sw,OFF,SiC,HARD} \end{aligned} \tag{2.5}$$

$$\begin{aligned} E_{sw,HyS,Op-4} = & \int_1^2 V_{HyS} I_C dt + \int_3^4 V_{HyS} I_D dt + \int_5^6 V_{HyS} I_C dt + \int_6^7 V_{HyS} I_D dt \\ & = E_{sw,ON,IGBT,HARD} + E_{sw,ON,SiC,SOFT} \\ & + E_{sw,OFF,IGBT,SOFT} + E_{sw,OFF,SiC,HARD} \end{aligned} \tag{2.6}$$

on-voltage V_{HyS} across the HyS. The I_{sp} for a junction temperature (T_j) condition of T_j = 25 °C is 7 A, therefore both IGBT and MOSFET carry 7 A each while the load current through the HyS is 14 A. Similarly, at T_j = 150 °C, I_{sp} is 4 A, which is lower than that at T_j = 25 °C. At light-load conditions (see (2.2)), the SiC MOSFET shares more current compared to Si IGBT in a HyS with a lower V_{HyS} compared to than across a standalone Si IGBT. Consequently, the HyS will have a low conduction power loss. Similarly, at heavy-load conditions (see (2.3)), the IGBT would share more current compared to MOSFET in a HyS with a lower on-voltage (V_{HyS}) across the HyS compared to a standalone SiC MOSFET. Hence, the conduction power loss of the HyS is low in the light-load and heavy-load region when compared to Si IGBT and SiC MOSFET respectively.

2.3 Si+SiC Gate Sequence Control Options for Hybrid Switch

There are four gate control options proposed for the HyS in different literature [3, 6, 12, 17]. These options differ from each other in the relative timing of Si and SiC device turn-on and turn-off within the HyS. These options are depicted in Fig. 2.3, where G_{IGBT} and

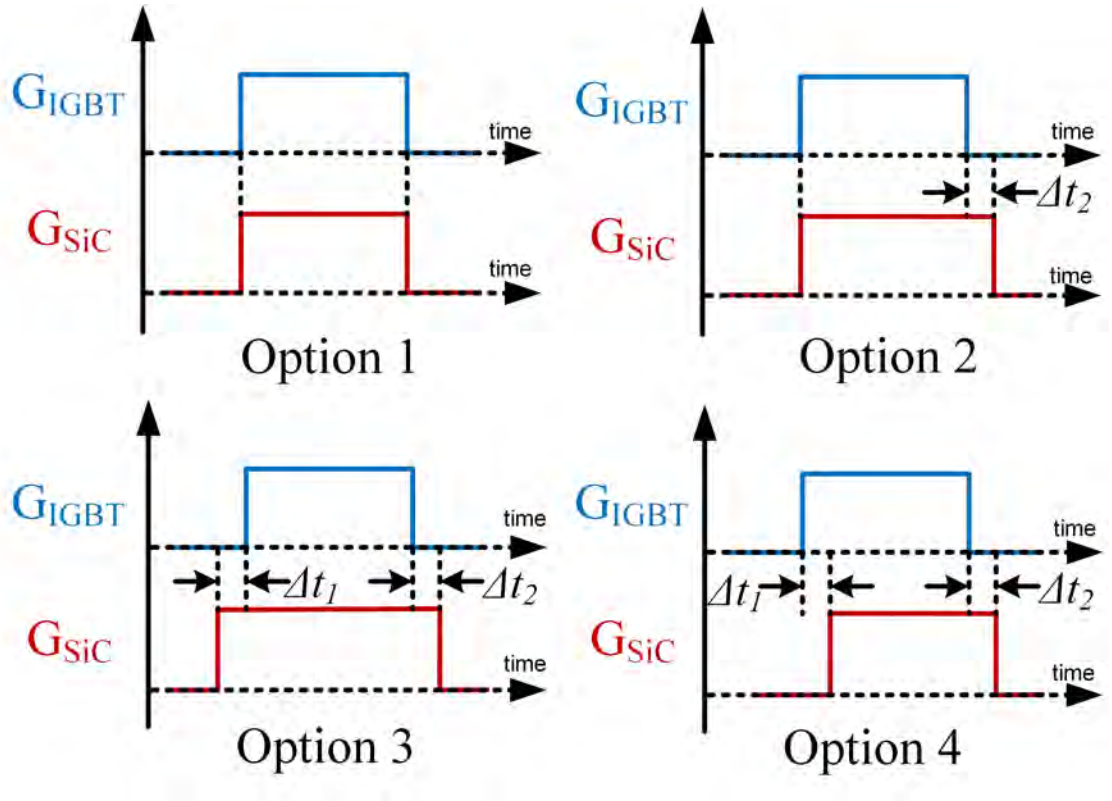

Figure 2.3: Si+SiC gate sequence control options for HyS

G_{SiC} represent the gate signal for Si and SiC device respectively within the HyS. Further, in this section, the performance of option 3 and 4 relative to the switching losses is discussed using simulation.

2.3.1 Option 1

In option 1, both devices receive the same gate signal using a single gate driver, in which the turn-on for each device triggers at the same instant. The same is true for turn-off of each device. As mentioned in the previous section, an inherent low conduction power loss of the HyS will be present. However, there will be no significant benefits in terms of switching performance when this option is used. During the turn-off, due to the tail current in the Si there is no reduction in turn-off switching energy compared to Si.

2.3.2 Option 2

In option 2, to eliminate the high turn-off loss in the Si resulting from its tail current, the SiC turn-off instant is delayed by time Δt_2 relative to SiC turn-off, which will cause the IGBT to turn-off while the MOSFET is still 'ON'. During this the voltage across the IGBT's collector and emitter terminal is approximately 0 V ($R_{DS(ON)}$ x I_D). This mimics a zero voltage switching (ZVS) during turn-off for the Si. Consequently, the turn-off switching energy in the IGBT is negligible. And, the turn-off switching energy of the HyS is equal to that of the SiC. The turn-on strategy is same as option 1.

2.3.3 Option 3

In option 3, the turn-off strategy is same as that in option 2. However, during the turn-on, Si turn-on instant is delayed by time Δt_1 relative to SiC turn-on instant, which will create a ZVS turn-on for Si and further reduce the turn-on switching energy compared to that in option 2. Moreover, switching losses in SiC are temperature independent. While in a Si IGBT they are heavily temperature dependent. Hence, by using option 3, a HyS yields a temperature independent behavior like a SiC device [18].

2.3.4 Option 4

In option 4, the turn-off control is same as option 2. However, during the turn-on, the SiC turn-on instant is delayed by time Δt_1 relative to Si turn-on instant. This is required in consideration of the parasitic interconnect inductance unbalance between the Si and the SiC cell within the HyS, as discussed in detail in section IV.

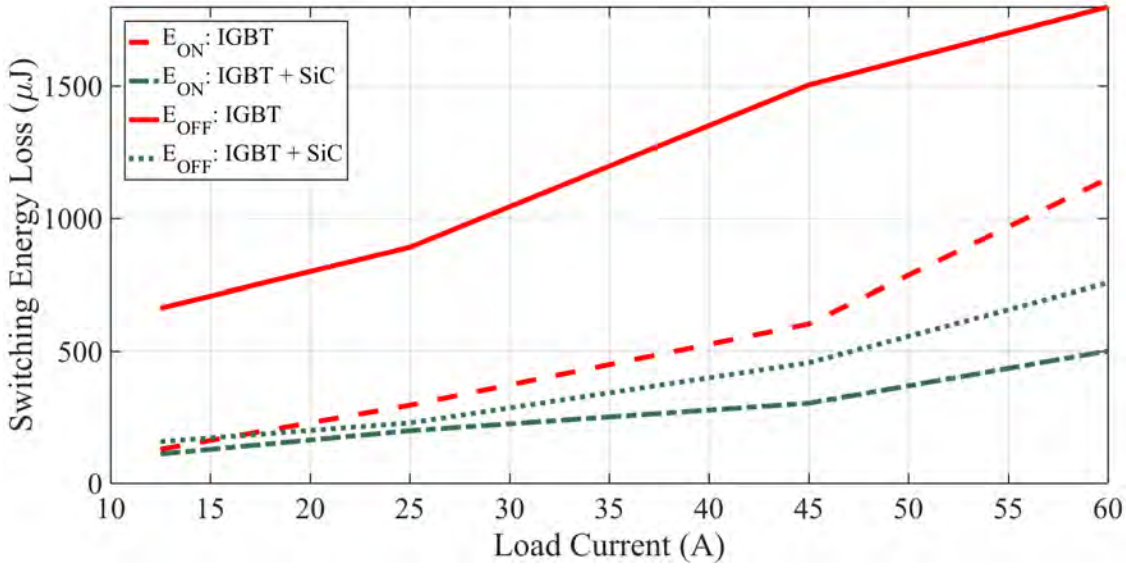

Figure 2.4: Comparison of switching energy with option 3 for HyS

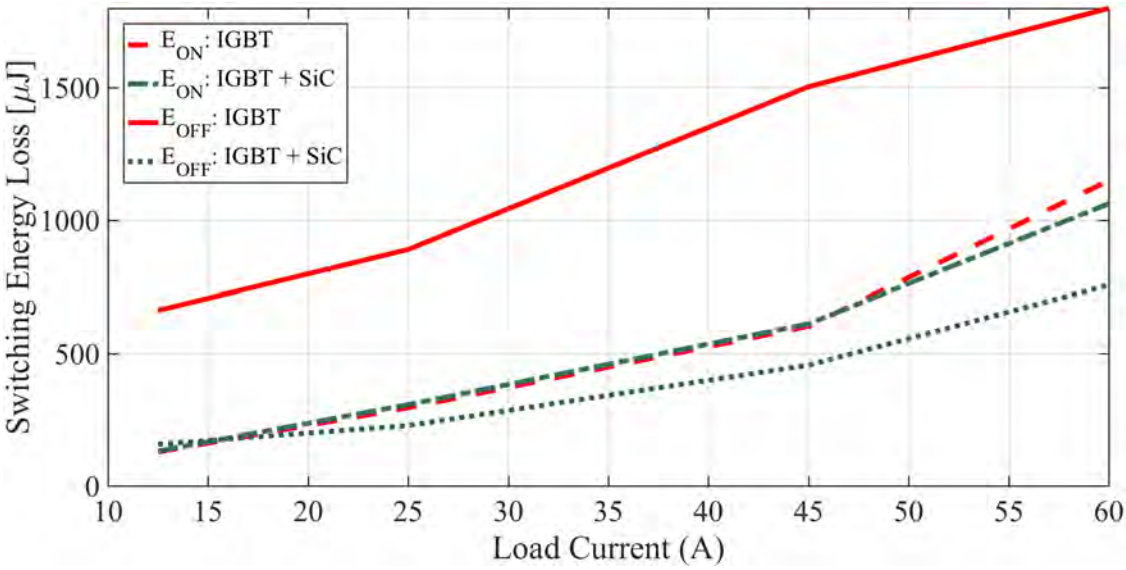

Figure 2.5: Comparison of switching energy with option 4 for HyS

2.3.5 Switching Performance

For options 3 and 4, the Δt_1 is generally greater than the turn-on time of the device turning 'ON' first. The Δt_2 is selected based on the carrier recombination time of the IGBT. The higher the Δt_2, the more carriers recombine within the IGBT during Si turn-off within

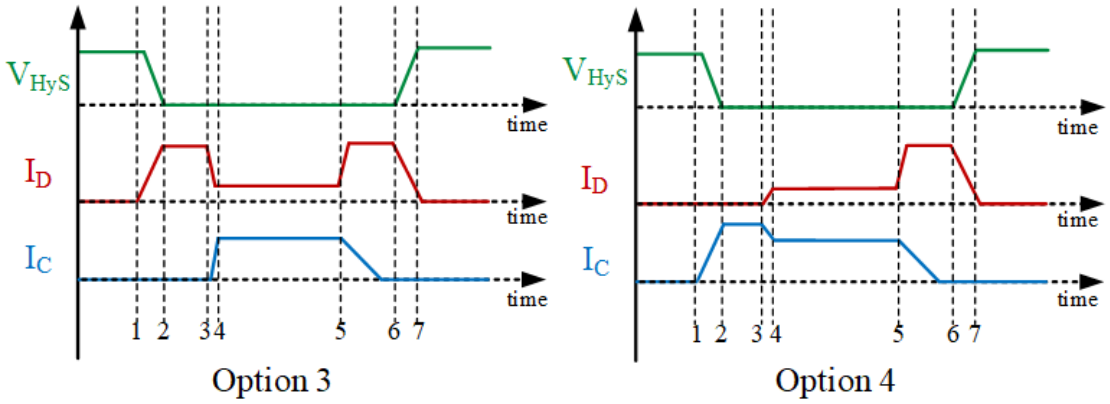

Figure 2.6: Timing diagram in the HyS for option 3 and 4 gate control

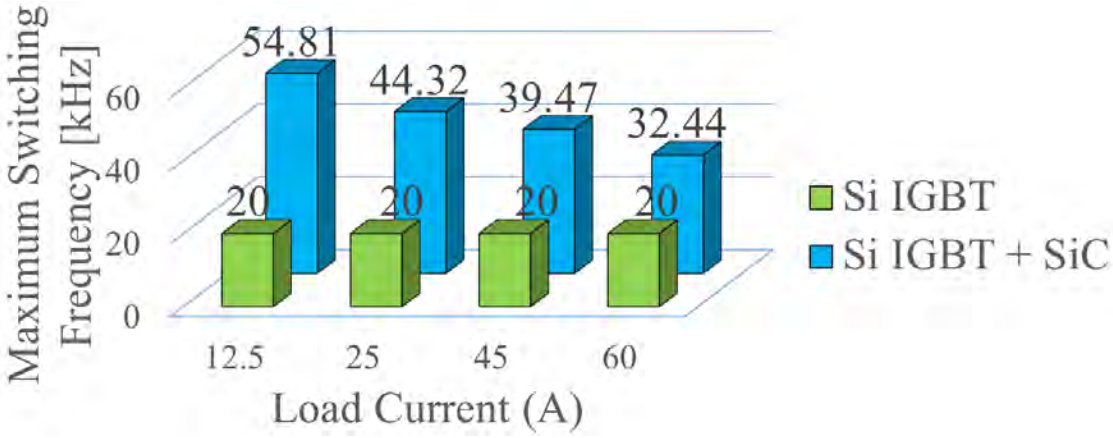

Figure 2.7: Relative maximum switching frequency possible for HyS.

HyS, and reduced current spike is observed in IGBT during SiC turn-off. Hence, the IGBT turn-off switching losses can be neglected. However, the Δt_1 (in option 3) and Δt_2 (in option 3 and 4) results in a high current transient across the SiC causing pulsed power loss which may risk the integrity of the die. Also, a very large Δt_2 may negatively impact the scope of increasing the switching frequency of the converter. Hence, there should be a trade-off between the IGBT turn-off loss, the pulsed power loss in SiC, and the switching frequency.

To demonstrate the switching performance of the HyS under gate control options 3 and 4, a double pulse test (DPT) simulation was performed on the device listed in Table 2.1.

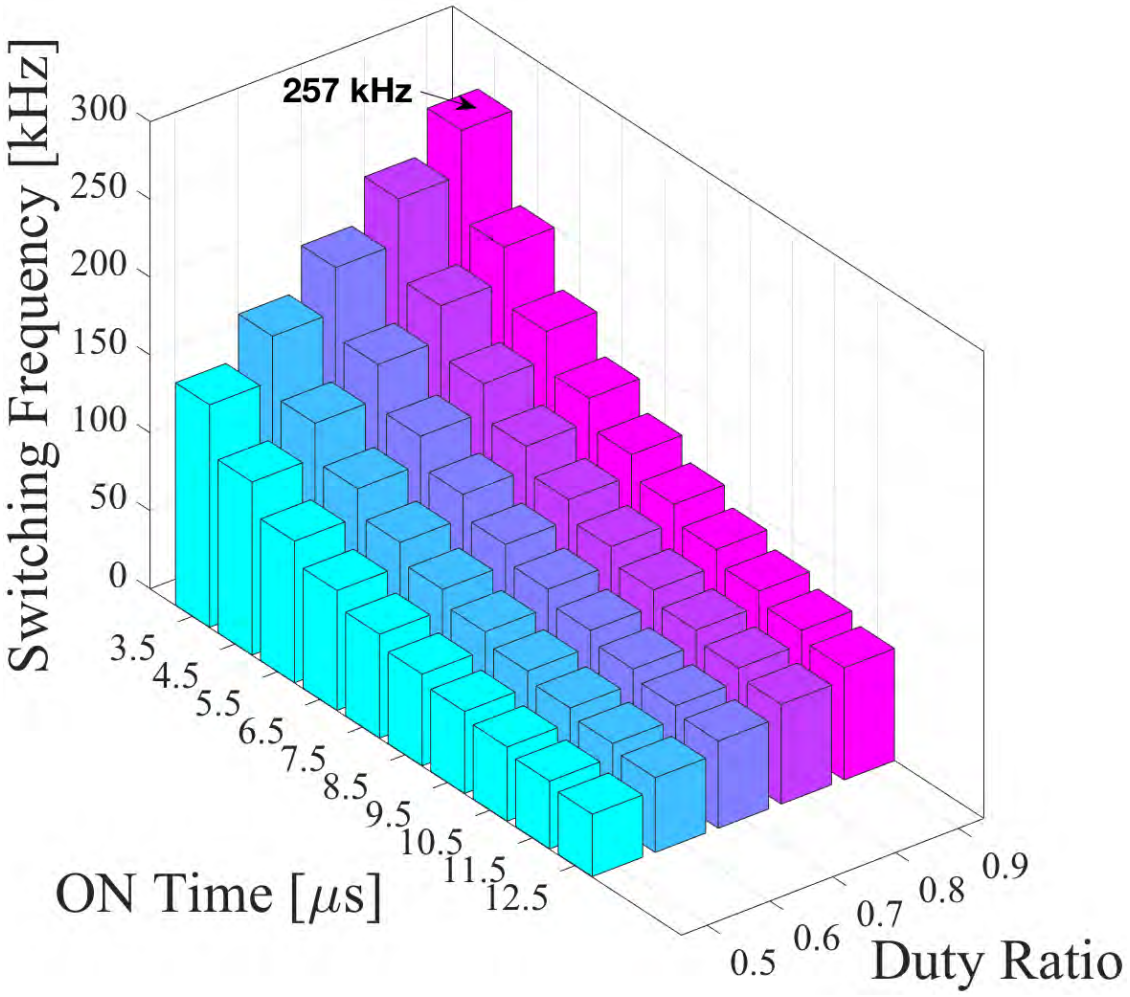

Figure 2.8: Maximum feasible switching frequency in a DC-DC converter

For each option, the delay times, $\Delta t_1 = 1$ μs and $\Delta t_2 = 1$ μs were used. As seen from the Fig. 2.4, the option 3 reduces both the turn-on and the turn-off switching energies for SiC based HyS compared to the IGBT. This is because the switching loss is contributed from the SiC hard switching, while the Si IGBT soft switching losses are assumed negligible (see (2.5)), when compared to Si hard switching for standalone IGBT (see (2.4)). Detailed power loss distribution in the HyS for option 3 is depicted in Fig. 2.16. In option 4 (see Fig. 2.5), savings in the turn-off switching energy due to SiC hard switching during turn-off is found similar to option 3. However, during turn-on, the switching loss is contributed from the

Si hard switching during turn-on. (2.6) indicates the devices contributing to the switching losses. (2.5) and (2.6) are relative to Fig. 2.6. Hence, option 3 yields the best switching performance for the HyS. Fig. 2.7 depicts the maximum switching frequency possible for the HyS based DC-DC converter at different load conditions. This is the frequency at which the HyS generates switching losses equal to the IGBT switching losses at 20 kHz. For example, a 62.2% increase in the switching frequency is possible at 80% of the full-load (133 A) using a HyS. The maximum switching frequency of a DC-DC converter will be restricted by the Δt_1 and Δt_2 times. The maximum switching frequency for a DC-DC converter, at various combinations of duty ratio and ON time of the switch, assuming $\Delta t_1 = 1$ μs and $\Delta t_2 = 1$ μs, is graphically represented in the Fig. 2.8. A consequent reduction in the size of passives, proportional to the increase in switching frequency is assured. This is true especially within a DC-DC converter as compared to that in a DC-AC converter [15].

2.4 Influence of Parasitic Interconnect Inductance on Dynamic Current Sharing

Although gate control options 3 has a good switching performance, the use of option 3 would be restricted in certain cases. The unbalance of the parasitic inductance in the Si device and the SiC device, and consequent slow dynamic current transfer from SiC to Si device can limit the use of option 3. In such a case, option 4 will be a better choice. However, the suitable range and limitations of the gating options 3 and 4 remains unclear. In this section, a systematic study on the influence of packaging parasitics is presented. Furthermore, a gating option selection based on the parasitic inductance unbalance within the HyS is presented. The proposed HyS concept is not restricted to bare dies, but can also be realized using off-the-shelf discrete devices as well as power modules. The parallel

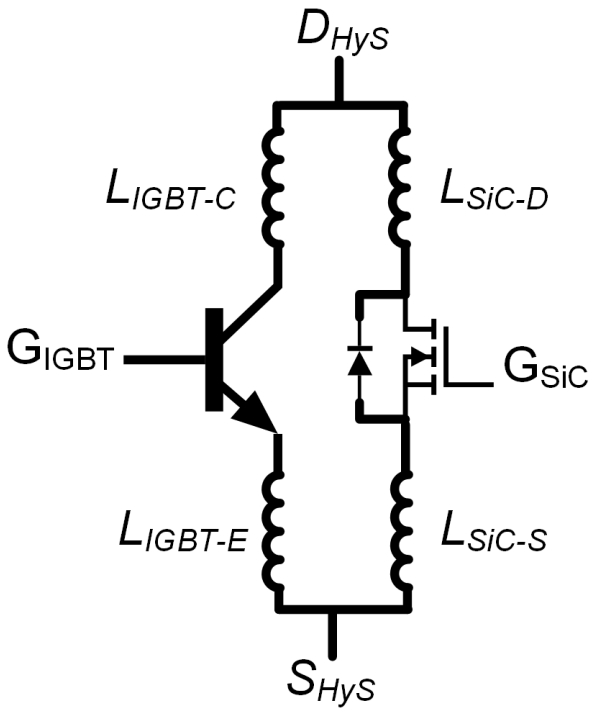

Figure 2.9: Parasitic interconnect inductances in HyS

interconnection of the Si and SiC may be done using either wire-bonds or planar techniques for bare dies in a custom module, or copper traces in a PCB for discrete devices, or bus bars for power modules. The layout in either of the interconnection options, may introduce series parasitic inductances for each of the device as shown in Fig. 2.9. The distribution of the parasitic inductances may be symmetrical or asymmetrical, while asymmetrical inductances will cause slow dynamic current transfer from one device to another. In case of multiple parallel devices, with each device represented as a commutation cell, a series inductance in the commutation cell will affect the time constant (L/R) of the respective cell [19]. This indicates that the time constant unbalance between Si and SiC cells will cause slow dynamic current transfer during the switching period 3-4 from Fig. 2.6. During this period, in the option 3 gate control, the current transfers from SiC to Si, however due to a larger time

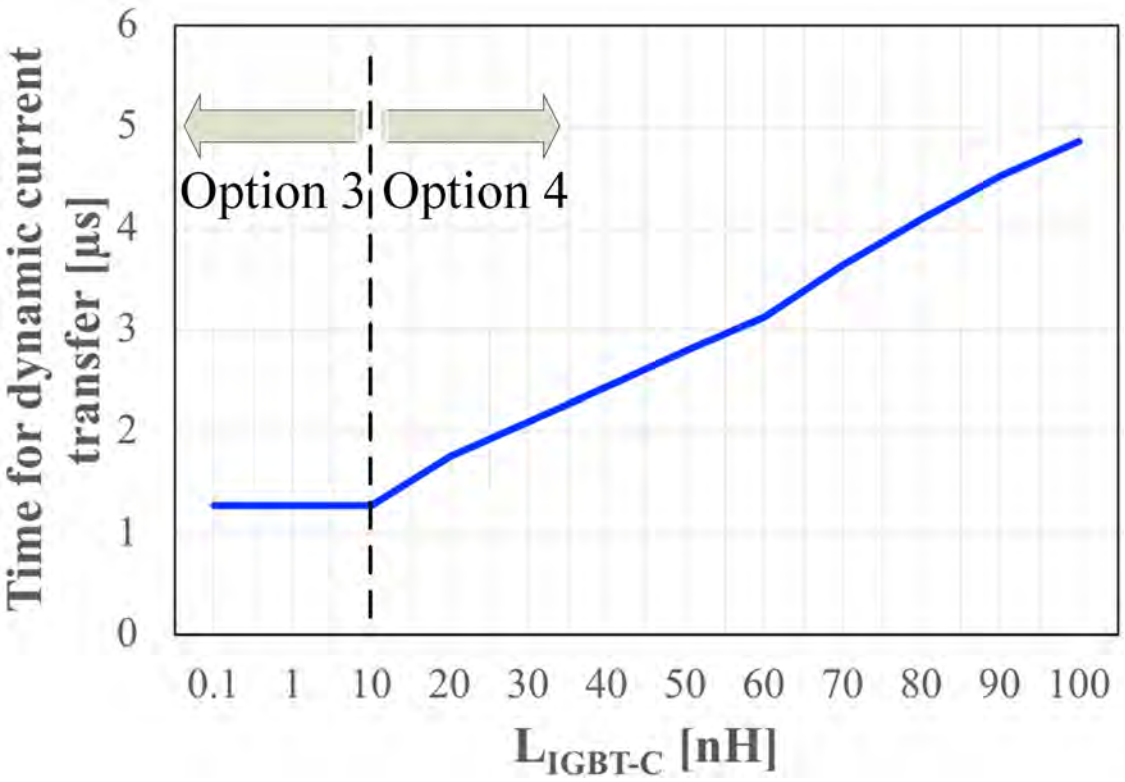

Figure 2.10: Parametric sweep of the interconnect inductance in IGBT

constant unbalance, the dynamic current transfer from SiC to Si will be slow. Consequently, the SiC will experience more conduction loss in period 3-4 from Fig. 2.6. This will decrease the reliability of the SiC device, especially when the proposed low SiC/Si current ratio is used. To avoid this option 4 [6] may be used. In option 4, the current transfers from Si to SiC in the period 3-4. However, with Si device sufficiently large, the additional conduction power loss will not affect Si device reliability. Hence, in case of high inductance unbalance option 4 gate sequence control should be used in place of option 3. Hence, a systematic study to understand the effect of unbalance on losses, and to determine a boundary line between the region for using option 3 and 4 is warranted.

For the following systematic analysis to determine a boundary-line of parasitic inductance unbalance, the HyS can be considered to have two commutation cells, one with

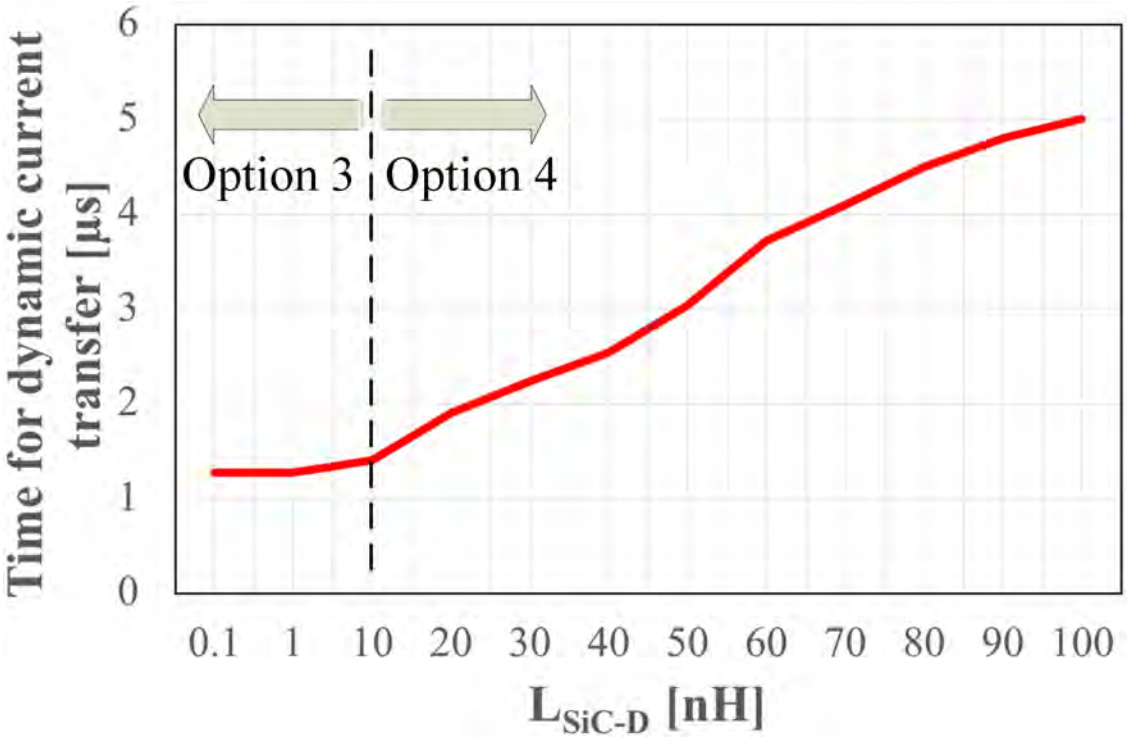

Figure 2.11: Parametric sweep of the interconnect inductance in SiC

the IGBT and the other with the SiC device. As shown in the Fig. 2.9, the interconnect parasitic inductance in IGBT cell is L_{IGBT-C} and L_{IGBT-E}, and in the SiC cell is L_{SiC-D} and L_{SiC-S}. In the first case, as shown in Fig. 2.10 the L_{IGBT-C} is parametrically swept from 0.1 nH to 100 nH with the inductances L_{SiC-D}, L_{IGBT-E} and L_{SiC-S} each set fixed at 0.1 nH. Similarly, in the second case, as shown in Fig. 2.11 the L_{SiC-D} is parametrically swept from 0.1 nH to 100 nH with the inductances L_{IGBT-C}, L_{IGBT-E} and L_{SiC-S} each set fixed at 0.1 nH. The sweep in each case will generate an unbalance of 0 nH to 99.9 nH.

Fig. 2.10 and Fig. 2.11 indicate the time taken for dynamic current transfer from SiC cell to IGBT cell due to an inductance unbalance between the Si and SiC cell. With an unbalance of less than 10 nH, the static current sharing can be reached in slightly higher than 1 μs. However, the dynamic current transfer is affected above 10 nH. It takes 4.86 μs for the

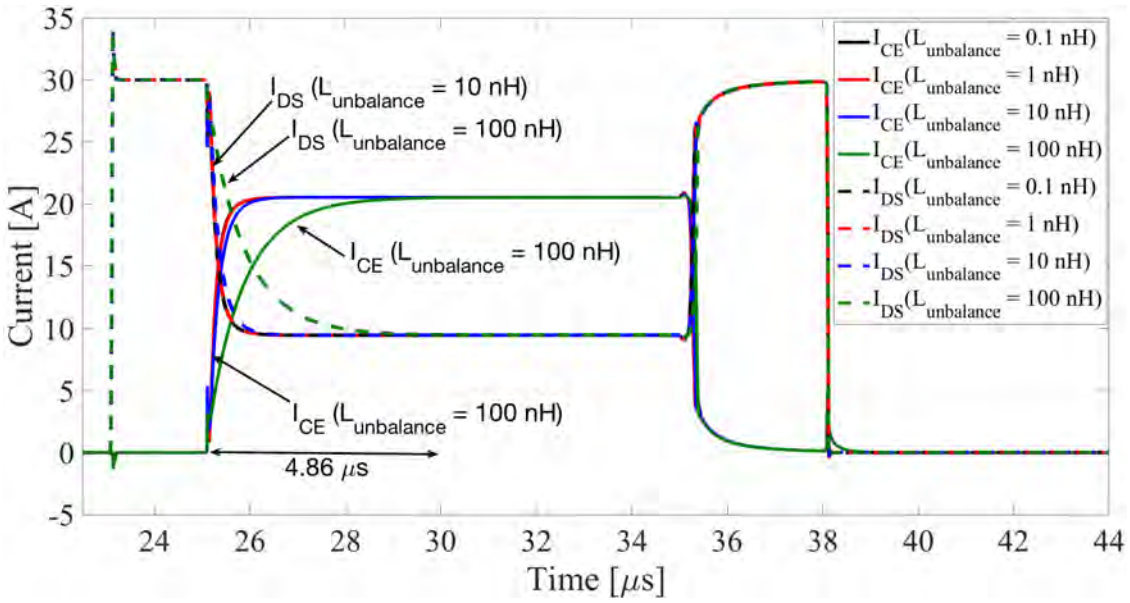

Figure 2.12: Dynamic current transfer from SiC to Si device in option 3 gate sequence control with parasitic inductance unbalance

transfer at a 99.9 nH unbalance as shown in Fig. 2.12. During that transfer the SiC device experiences a 34.5 % increase in conduction losses. This is not advisable as the junction temperature fo the small current rated SiC may overshoot the maximum permissible limits. Hence, it is recommended to restrict the parasitic inductance unbalance in the HyS under the boundary-line of 10 nH. However, if it cannot be restricted to 10 nH, the use of option 4 gate control is recommended. Since, the large IGBT device is rated for higher current will not get as heated as the SiC.

2.5 Cost Analysis

The available SiC devices have a high cost/ampere ($/A) rating compared to the Si IGBT devices [20]. Hence, a small current rating SiC in HyS will keep the cost low. Moreover, the main purpose to parallel a SiC device with Si device was to enable the switching action through the fast switching SiC device. Hence, there is no need for a full load current

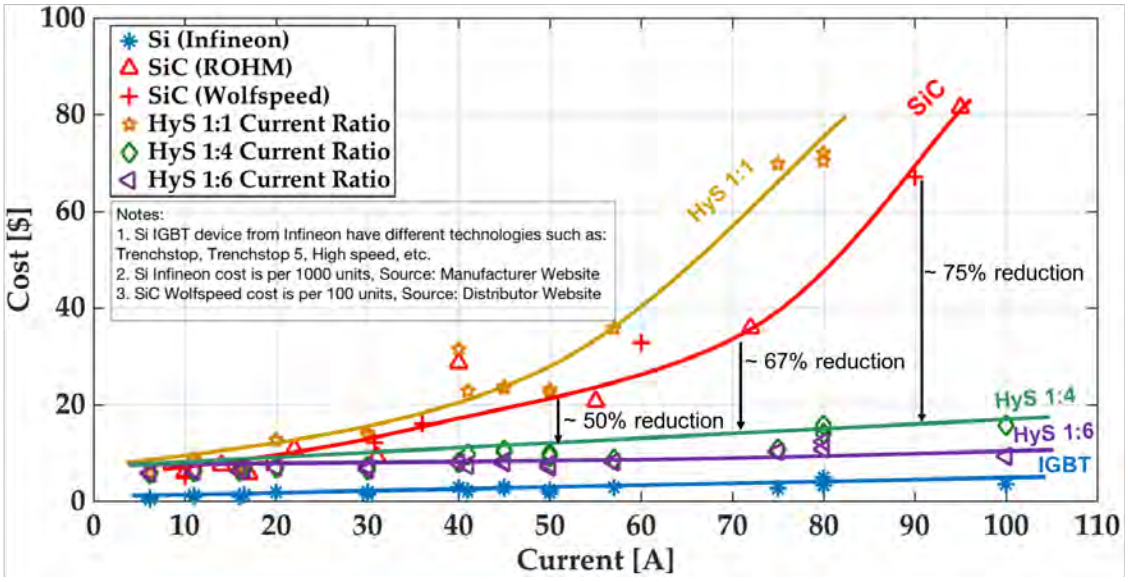

Figure 2.13: Cost comparison of 1.2 kV discrete devices

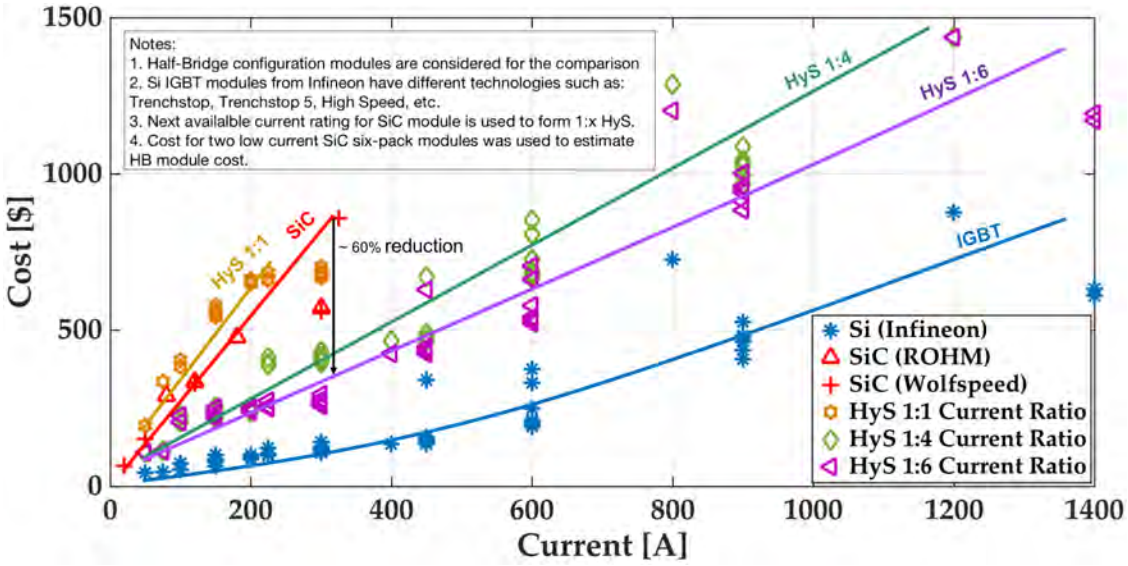

Figure 2.14: Cost comparison of 1.2 kV modules

rated SiC in the HyS. Consequently, using a SiC/Si current ratio less than unity will ensure a lower cost for the HyS. To compare the cost of the HyS solution with the all-SiC approach for replacing Si IGBT, for high-current, high-power converter applications, a cost analysis is presented. In this analysis, a HyS with 1:1, 1:4 and 1:6 SiC/Si current ratio are considered. In this analysis, state-of-the-art, 1.2 kV commercial off-the-shelf Si and SiC discrete

devices, and power modules are used. Si devices are from the catalogue of the major IGBT manufacturer Infineon, with the per-unit cost information true for >1000 units bulk order from the manufacturer. SiC MOSFETs are from two major manufacturers Wolfspeed and ROHM, with the per-unit cost information true for >100 units bulk order from Digikey. In the Fig. 2.13, each marker represents a discrete device, plotted against its current rating (x-axis) and per-unit cost (y-axis). Similarly, the Fig. 2.14 is for half-bridge power modules. Fig. 2.13 and Fig. 2.14 serve as a cost model for designers to select the HyS according to their cost targets. Also, this model can be replicated for other voltage class of devices.

The interpretations of the 1.2 kV voltage class cost models are as follows: As shown in Fig. 2.13, in the discrete device category, the cost of a 1:1 HyS is higher than a SiC device, because the HyS has an additional cost of Si IGBT above the SiC MOSFET. However, with a 1:4 and 1:6 current SiC/Si ratios, the cost for the HyS at currents above 50 A will be 50 to 75% lower, when it is compared with an identical current rated SiC device, with the 1:6 HyS being relatively more cost-effective than 1:4 HyS. Hence, a SiC/Si current ratio below unity, at a ratio 1:4 or lower is recommended for low device cost.

Similar trends are also observed for the power module category as seen from Fig. 2.14. A maximum of 60% cost saving is achieved at 300 A, when comparing 1:6 HyS module with an identical current rated SiC module. Moreover, it should be noted that no 1.2 kV SiC module is available above 300 A current rating. Whereas, 1:6 HyS module with current rating ranging from 300 A to above 1200 A can be achieved. In the 300 A to 1200 A current range, the HyS will serve as a direct and the only replacement option for Si IGBT module. SiC modules can be paralleled, however, they will be expensive looking at the linearly increasing cost trends. Moreover, due to several challenges, a maximum of only 2

Table 2.2: Cost comparison of 1.2 kV discrete devices for direct replacement of a Si IGBT

Device technology	Part number	Current [A]	Cost [$]	Remarks
Si IGBT	IGW60T120	60	6.29	
SiC MOSFET	C2M0160120D	12.5	8.33	Used in HyS
SiC MOSFET	C2M0025120D	60	69.8	Direct replacement of Si IGBT
Si IGBT + SiC MOSFET	IGW60T120 + 5 x C2M160120D	60	47.94	1:1 SiC/Si current ratio
Si IGBT + SiC MOSFET	IGW60T120 + C2M0025120D	60	76.09	1:1 SiC/Si current ratio
Si IGBT + SiC MOSFET	IGW60T120 + C2M160120D	60	14.62	1:5 SiC/Si current ratio

SiC modules in parallel has been demonstrated [21].

A small set of devices as listed in the Table 2.2 in discrete device category are used to further illustrate the cost difference. The cost of a Si IGBT is compared with a direct SiC MOSFET replacement, and a HyS based on 1:1 and 1:5 SiC/Si current ratio. As observed from the costs listed in Table 2.2, a direct replacement of IGW60T120 with C2M0025120D will cost 11 times more. A 1:1 HyS, will be 7.6 times expensive, however, this solution requires paralleling 5 SiC MOSFET. Whereas, a 1:5 HyS, using only one SiC device will be only 2.3 times the Si IGBT cost.

Apart from the $/A comparison, $/kW comparison of device technology is generally well accepted [22]. Hence, a $/kW comparison of the HyS, all-Si and all-SiC technology is presented as well. For this comparison, a 800 V, 200 kW DC-AC three-phase inverter application is used. f_{sw} is assumed to be 20 kHz for all the device options. A 1200 V/600 A Si IGBT half-bridge module ($230) for each phase is used for an all-Si drive. Two 1200 V/ 300 A SiC half-bridge modules ($600 each) are used for each phase in an all-SiC drive. A 1:6 HyS, with a 1200 V/600 A Si IGBT ($230) and 1200 V/ 100 A SiC module ($200) connected in parallel, is considered for a HyS-drive. With this information, the active device cost for a Si drive, SiC drive, and HyS based drive is 3.45 $/kW, 18 $/kW, and $6.45/kW respectively. This estimation further demonstrate the cost viability of HyS solution for end-applications.

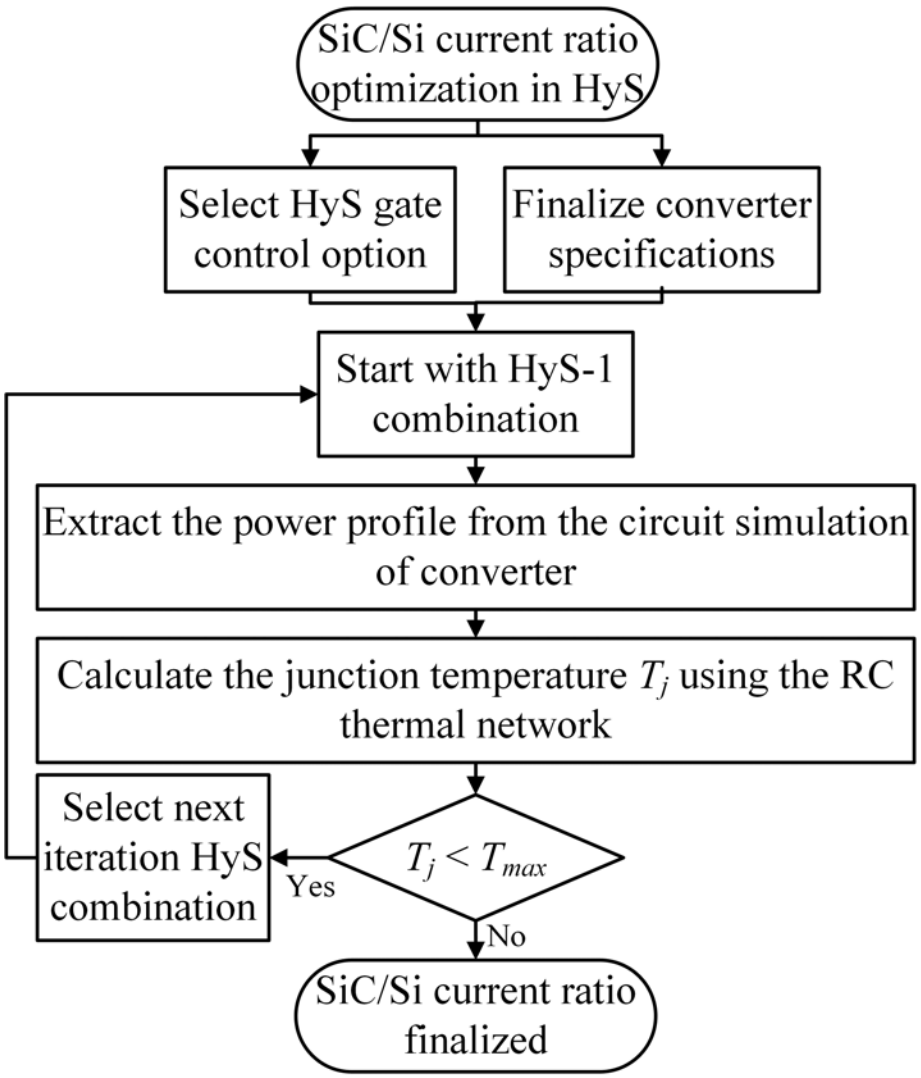

Figure 2.15: Flowchart for the current ratio optimization

2.6 SiC/Si Current Ratio Optimization

2.6.1 Optimization Problem

In the previous section, it was concluded that using a SiC current rating over Si current rating (SiC/Si current ratio) less than unity will make the HyS a cost effective solution. Moreover, the main purpose to parallel a SiC device with Si device was to enable the switching action through the fast switching SiC device. However, by employing the option

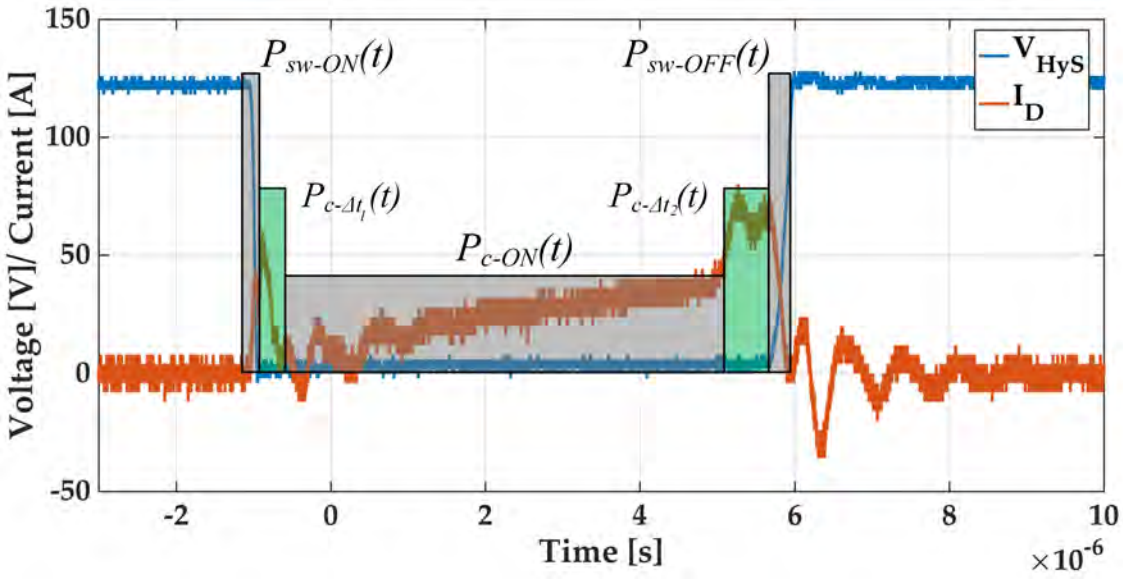

Figure 2.16: Power profile of SiC in HyS during option 3 gate control

3 gate control for the HyS, the entire load current is conducted through the SiC device during the Δt_1 and Δt_2 delay times. Consequently, the SiC device will be stressed periodically with pulsed currents having a peak value of SiC current rating over the SiC/Si current ratio. Hence, a SiC/Si smaller than unity, results in pulsed power losses, generating high heat flux during a continuous converter operation. With a decreasing SiC/Si current ratio, which reduces the SiC die area, the thermal resistance and the heat capacity of the SiC device increases and decreases respectively within the HyS. This will result in transient junction temperature peaks, which could exceed the maximum permissible temperature for the device. This indicates that there is a SiC/Si current ratio boundary point, below which the SiC will be damaged. Further, the SiC failure will cause a consequent failure of the Si device from its excessive switching power loss at high switching frequency. This warrants the selection of an optimal SiC/Si current ratio that keeps the transient peak junction temperature of the SiC device just below the maximum value, for attaining a trade-off between safe operation

and low cost. Generally, a SiC device can sustain 175 °C to 200 °C; whereas, a Si device can sustain only 150 °C. Hence, there is relatively more peak junction temperature tolerance on the SiC device, providing a scope of analysis to find a SiC/Si current ratio below unity.

$$P_{loss}(t) = P_c(t) + P_{sw}(t) \tag{2.7}$$

$$P_c(t) = P_{c-\Delta t_1}(t) + P_{c-ON}(t) + P_{c-\Delta t_2}(t) \tag{2.8}$$

$$P_c(A,i,t)|_{Bare-die} = \frac{R_{ON,sp}(i) \times i^2(t)}{A_{die}} \tag{2.9}$$

$$P_c(i,t)|_{Packaged-device} = R_{DS,ON}(i) \times i^2(t) \tag{2.10}$$

$$P_{sw}(A,v,i,t)|_{Bare-die} = (m \times A_{die} + n_1) \times i(t) \times v(t) \tag{2.11}$$

$$P_{sw}(v,i,t)|_{Packaged-device} = n_2 \times i(t) \times v(t) \tag{2.12}$$

$$T_j = P_{loss}(t) \times Z_{th}(j-c) + T_c \tag{2.13}$$

2.6.2 Current ratio optimization algorithm

In this paper, an algorithm using a dynamic junction temperature prediction is presented (see Fig. 2.15), to select an optimum SiC current rating for the HyS. This was derived from a previous work on die optimization [23]. The dynamic junction temperature predic-

tion is obtained by transient thermal simulation, using the thermal equivalent network of the SiC device package. This current ratio optimization algorithm can be used for devices of any voltage and current rating as long as the thermal equivalent network is available, or is extracted for the package in consideration for the HyS. To begin with, a set of HyS combinations with a descending order of SiC device current rating against a fixed current rated Si IGBT is selected. Next, a HyS gate control option and converter specifications are selected. The first iteration starts with the HyS-1 in the set. An instantaneous power loss profile for the SiC device is extracted from the converter simulation at the selected operating conditions. This is represented by the analytical model in (2.7)-(2.12), where, $R_{ON,sp}$ is the specific on-resistance of the die, A_{die} is the area of the die, $R_{DS,ON}$ is the on-resistance of the packaged device, m is the linear scaling factor for die area; n_1 and n_2 are the linear scaling factor for the die and packaged device current respectively. An example of a rectangular approximation instantaneous power profile for option 3 is shown in Fig. 2.16. Further, the power profile is fed to the thermal equivalent network (in the form of RC cauer network, where R is the thermal resistance and C is the heat capacity) for running transient thermal simulations and extracting the transient peak junction temperature of the SiC device. This is represented by the analytical model in equation (2.13). In the thermal equivalent network, each RC branch represents a layer in the thermal stack for SiC device. With respect to a TO-247 package, there are three RC network branch. The first RC (R_1/C_1) represents the thermal resistance and heat capacity of the SiC die. Successive RC elements, R_2/C_2 and R_3/C_3 represent the die attach material and the die tab or substrate (on which the die it attached) respectively. Further in the algorithm, if the extracted transient peak junction temperature is below the maximum permissible junction temperature limit of the SiC de-

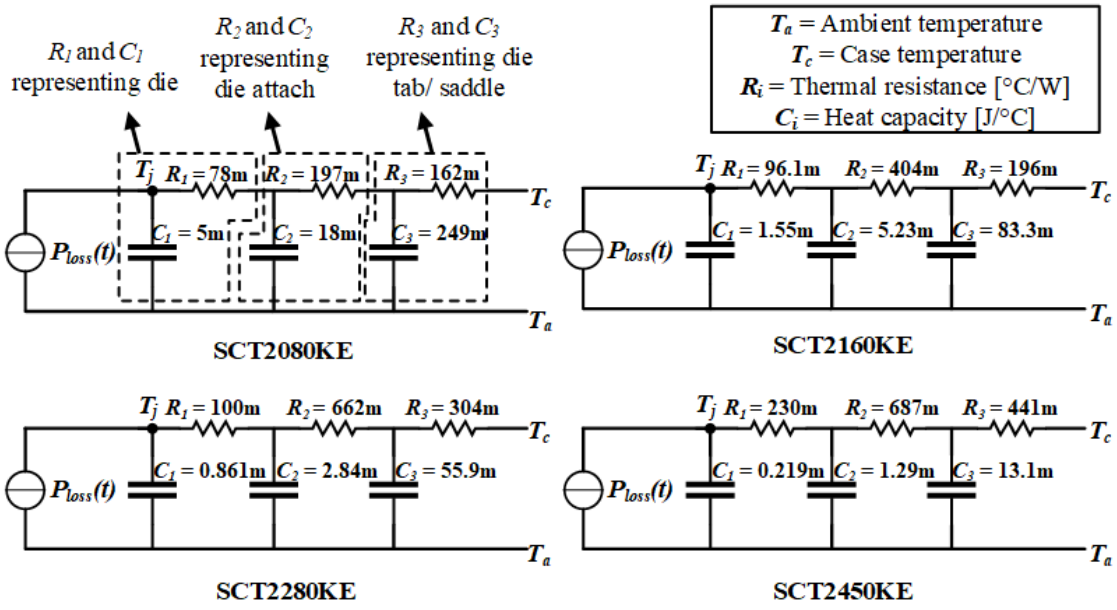

Figure 2.17: Thermal equivalent RC cauer network of each SiC MOSFET in respective HyS combination in their TO-247 commercial package

vice, same procedure until this point is repeated for a second iteration with HyS-2 from the set. Successive iterations will continue until the peak junction temperature crosses the set threshold for n^{th} HyS-n. The main idea here is to operate the SiC device at the maximum temperature it can sustain (which is 175 or 200 °C). The $n-1^{th}$ HyS-(n-1) in the preceding iteration is the HyS with optimum SiC/Si current ratio for the selected converter operating conditions and gate control option.

2.6.3 Optimization design example and results

To demonstrate the current ratio optimization using the algorithm, a design example is presented with a set of 4 HyS, formulated using a Infineon Si device and second generation SiC devices from ROHM. This set is shown in the Table 2.3. Option 3 gate control was used, which is the worst case scenario due to the presence of two pulsed currents in one cycle. A DC-DC buck converter operation is considered, with operating conditions as listed

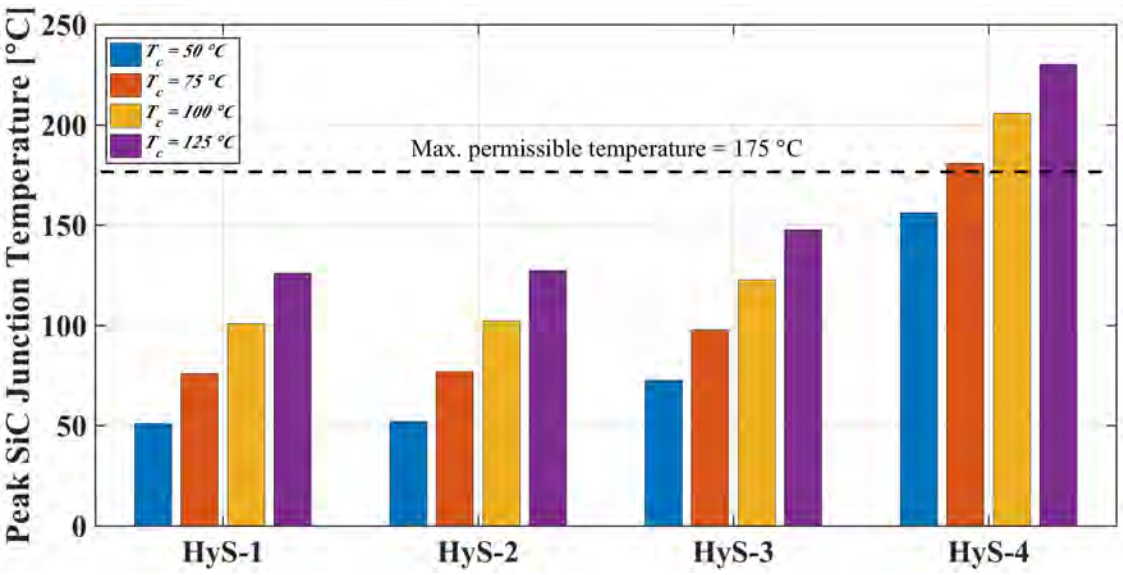

Figure 2.18: Peak junction temperature of SiC in HyS with a standard package

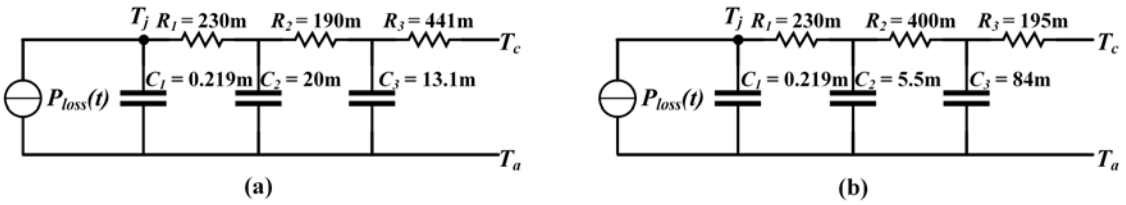

Figure 2.19: Thermal equivalent RC cauer network of the SiC MOSFET in an improved package (a) a low thermal resistance and high heat capacity die attach material (b) thermal via cooling

in the Table 2.4. The peak load current was selected such as to stress the SiC device with the Si device current rating during the pulsed current. The instantaneous power dissipation across SiC device was extracted; fed to the thermal equivalent network of the SiC to run transient thermal simulations. The RC networks used for each SiC (in their commercial TO-247 package) in the respective HyS are shown in the Fig. 2.17. For transient thermal simulations, the ambient temperature (T_a) was assumed to be 50 °C. The peak SiC junction temperature was extracted at 4 different case temperature (T_c) = {50, 75, 100, 125} °C. Each T_c demonstrates different level of cooling system, with T_c = 50 °C representative of a

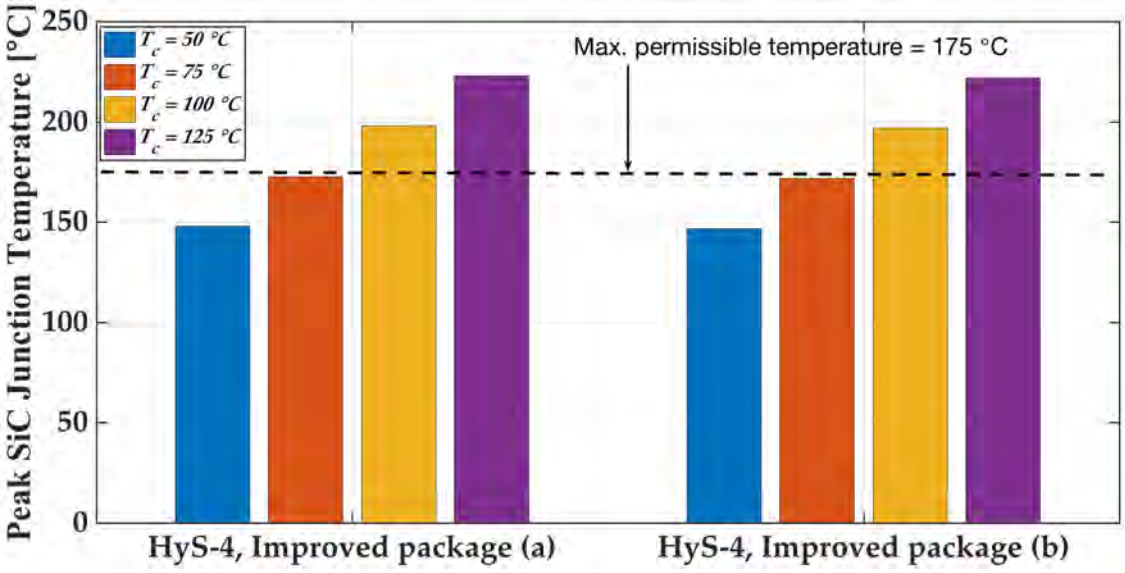

Figure 2.20: Peak junction temperature of SiC in HyS with improved packages as shown in Fig. 2.19 (a) and (b)

bulky cooling system, considering the fact that it needs to maintain the case temperature at 50 °C; T_c = 125 °C representative of a lighter cooling system. The extracted peak junction temperatures of each SiC device in the respective HyS combination are presented in Fig. 2.18. With reducing SiC current rating, the SiC die area decreases, consequently the thermal resistance and heat capacity increase and decrease respectively. Hence, a monotonic increase in the peak junction temperature of the SiC devices from HyS-1 to HyS-4 can be observed from Fig. 2.18. The peak junction temperature of the SiC device SCT2450KE in TO-247 package within HyS-4 under the operating conditions listed in Table 2.4, will exceed the maximum permissible junction temperature of 175 °C at T_c = 75 °C and T_a = 50 °C. The conclusion is that the designer will have to use the HyS-4 combination (1:6 ratio) with bulky cooling system (T_c = 50 °C), or use HyS-3 (1:4 ratio) with lighter cooling system (T_c = 125 °C). This may be important while considering the specific power density of the converter in an aerospace applications with restricted weight allowance.

The use of HyS-4 combination in the design example was restricted at $Tc = 50$ °C (heavy cooling system) condition. This was due to the peak junction temperature of the SiC within overshooting the 175 °C maximum limit. In order the use HyS-4 at $Tc = 75$ °C (lighter cooling system) condition, an improved package (lower thermal resistance and high heat capacity) for the SiC device in the HyS is needed. Hence, the effect of an improved package using advanced packaging materials and designs on the peak transient junction temperatures and consequently to the cooling system is demonstrated. The RC network of SCT2450KE within HyS-4 is modified; Fig. 2.19 illustrates the two variation of improved thermal equivalent network of SCT2450KE. For comparison, the thermal equivalent network of SCT2450KE in its original TO-247 package is illustrated in Fig. 2.17. In TO-247 package, the die attach is generally a solder material and the tab is aluminum or copper. In the first possible improvement, for package (a) in Fig. 2.19, the R_2/C_2 elements now represents a low thermal resistance and a high heat capacity material. When comparing R_2/C_2 from Fig. 2.19 with Fig. 2.17, R_2 is lower than that in Fig. 2.17, whereas, C_2 is more than that in Fig. 2.17. This could be achieved using an advanced die attach material such as nano-silver paste [24]. In the improved package (b) in Fig. 2.19, the R_2/C_2 as well as R_3/C_3 elements now represent low thermal resistance and a high heat capacity materials, This could be achieved using an advanced package feature, thermal via cooling [25]. The peak junction temperature for SCT2450KE for each improved package is presented in Fig. 2.20. Now, HyS-4 (1:6 current ratio) with an improved package can be used with lighter cooling system ($T_c = 75$ °C), compared to the commercial TO-247. Hence, it is demonstrated that an improved package will help to reduce the dynamic temperature rise in SiC, to further enable lower SiC/Si current ratio below unity, consequently achieving cost reduction as demonstrated in

Table 2.3: Set of HyS used for the optimization design example

HyS#	Si IGBT	Si current rating [A] @ T_c = 100 °C	SiC MOSFET	SiC current rating [A] @ T_c = 100 °C	SiC/Si Current Ratio
HyS-1	IKW40N120T2	40	SCT2080KE	28	1:1.43
HyS-2	IKW40N120T2	40	SCT2160KE	16	1:2.5
HyS-3	IKW40N120T2	40	SCT2280KE	10	1:4
HyS-4	IKW40N120T2	40	SCT2450KE	7	1:5.7

Table 2.4: Converter operating conditions for the optimization design example

Parameter	Value
Peak device current [A]	40
Input/ Output voltage, V_{in}/ V_{out} [V]	300/ 150
Duty ratio, D	0.5
Switching frequency, f_{sw} [kHz]	20
Power rating [kW]	12

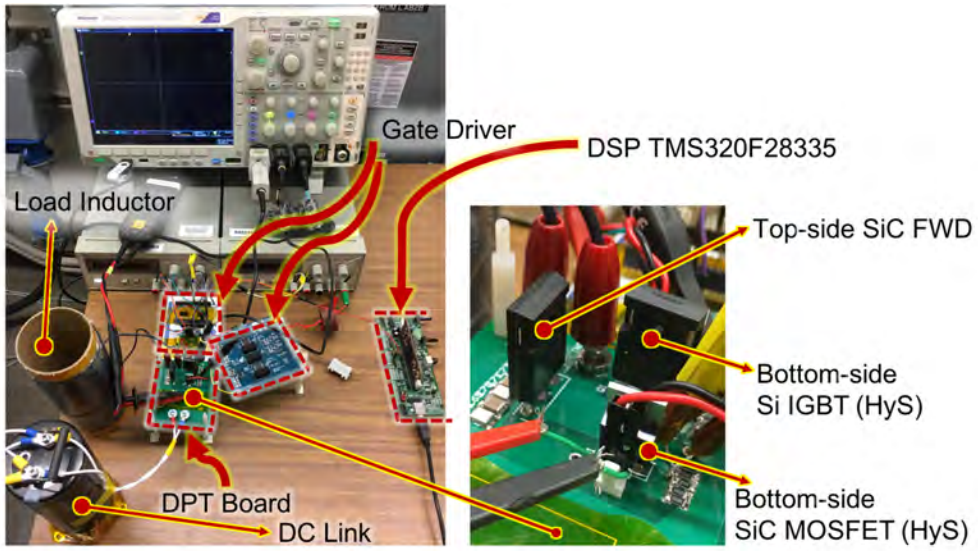

Figure 2.21: Experiment setup. [Source: Photo by Author.]

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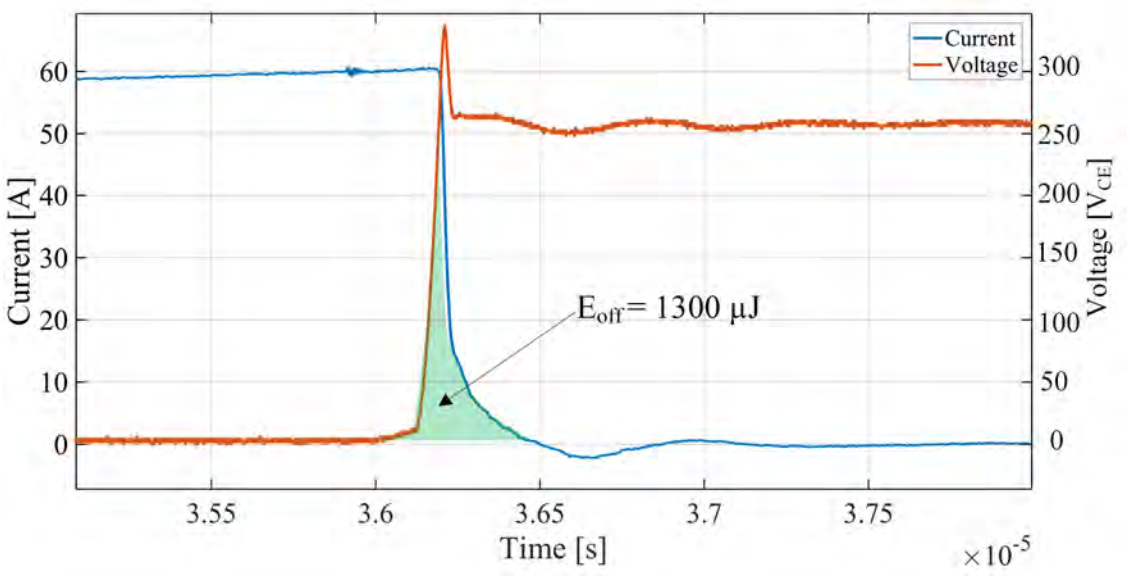

Figure 2.22: Turn-off switching transient for IGBT

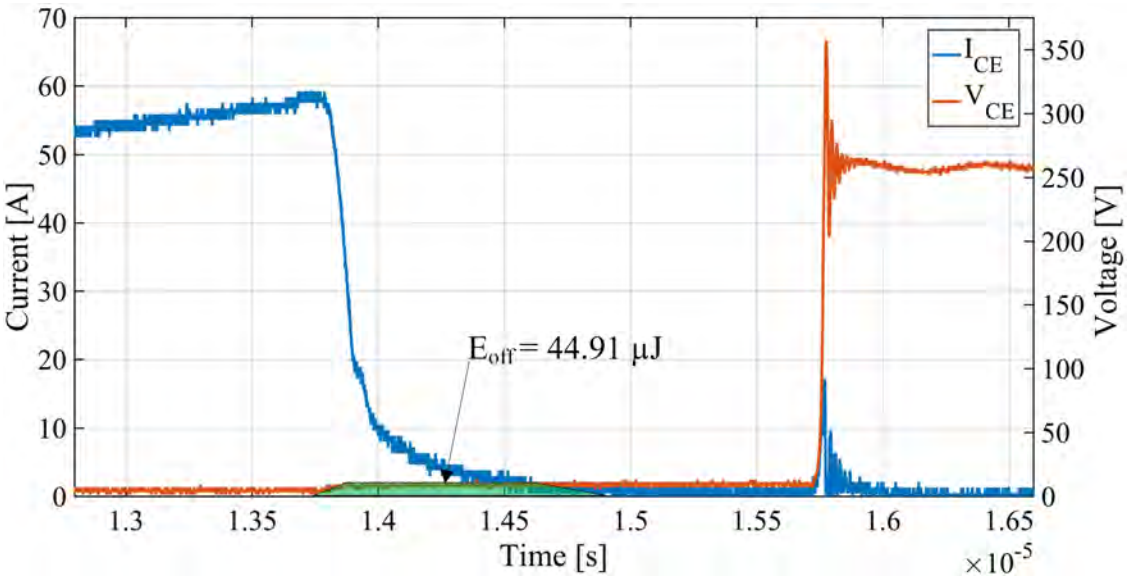

Figure 2.23: Turn-off switching transient for IGBT in HyS

2.7 Experiment Results

2.7.1 Double Pulse Tests: Switching Characterization

To characterize the switching performance of the HyS, a double pulse test (DPT) in an inductive clamped circuit was performed for the evaluation of the switching performance

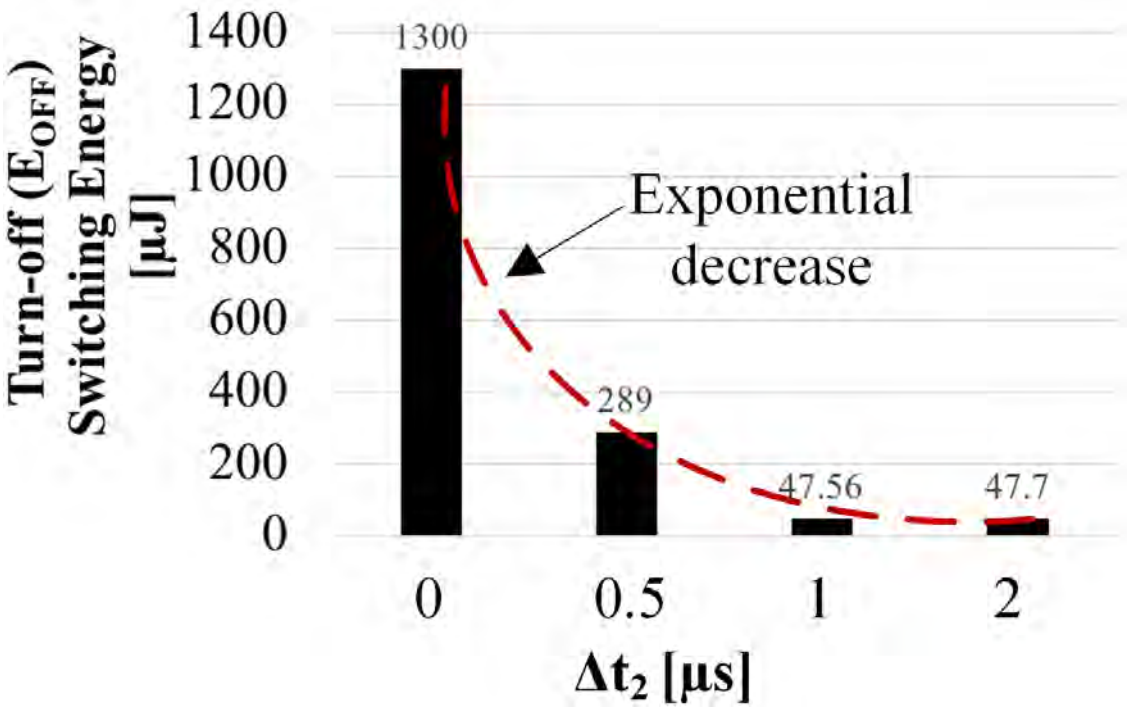

Figure 2.24: Parametric sweep of the turn-off delay

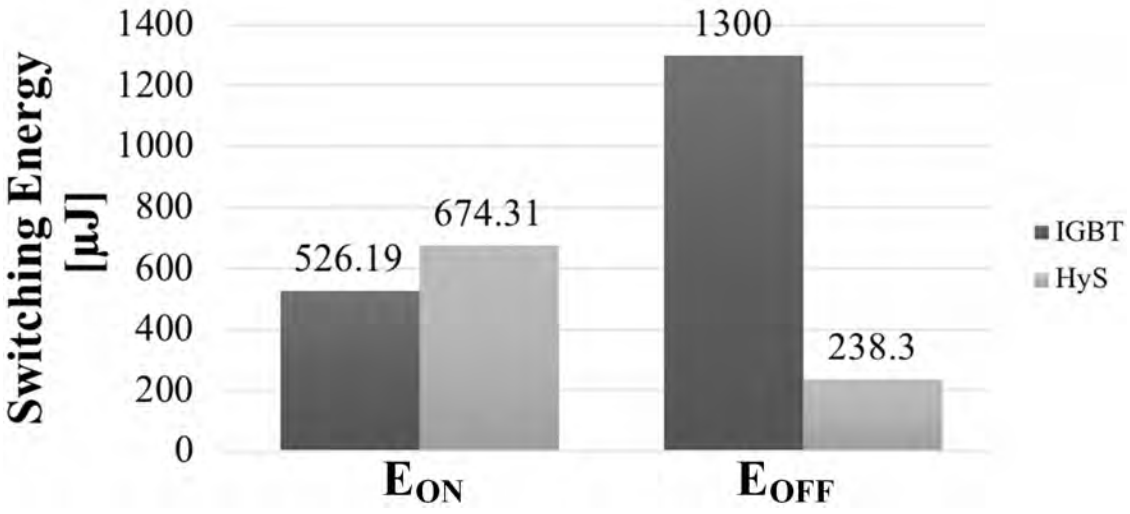

Figure 2.25: Experiment based switching loss comparison

of the HyS. Devices used for the evaluation are listed in the Table 2.1. The DPT was performed at 250 V, 60 A with a 131 μH load inductor. First, both Si IGBT and SiC MOSFET were tested individually in the test setup to calculate the turn-on and the turn-off switching energies. Later, the HyS was evaluated at same conditions. The double pulse gate

signals for individual device testings as well as option 3 gate control in the HyS testing were generated using a DSP TMS320F28335. A commercially available gate driver board (CRD-001) from CREE was used for each device. The V_{GS} for the Si IGBT and SiC MOSFET was +15 V/ -5 V and +18 V/ -5 V respectively. The turn-on and turn-off switching energies were calculated by integrating the recorded current and the voltage waveforms from the experiment using MATLAB. Under the option 3 gate control, the turn-off delay (Δt_2) was swept from 0 μs to 2 μs for determining the ideal delay time while the turn-on delay (Δt_1) was fixed at 1 μs.

The turn-off switching transient of a standalone IGBT and a HyS is shown in Fig. 2.22 and Fig. 2.23 respectively. It is observed from the Fig. 2.22 that the lifetime of the carriers in the IGBT during turn-off is approximately 1.5 to 2 μs. Fig. 2.24 shows that the turn-off loss in a HyS decreases exponentially as Δt_2 increases, hence the selected Δt_2 = 2 μs. Fig. 2.25 shows a comparison of the turn-on and turn-off switching energies for the IGBT and the HyS. A reduction in the turn-off switching loss by 81%, whereas an increase in the turn-on switching loss by 30% is observed for the HyS as compared to a standalone Si IGBT. The reduction in the turn-off loss is due to the elimination of the Si IGBT's tail current during turn-off. During the turn-on mechanism, the switching loss is induced by diode reverse recovery process; the energy stored in the output capacitance C_{DS} of the switching device. Hence, the increase in turn-on loss is attributed to the effective higher capacitance $C_{DS,HyS}$ (= C_{DS} + C_{CE}) during SiC MOSFET turn-on instant in the HyS. The C_{DS} is 77 pF while the C_{CE} is 151 pF. The effective $C_{DS,HyS}$ is 228 pF, which is 51% higher compared to a standalone Si IGBT C_{CE}. However, an overall 50% reduction in the switching loss is observed for a HyS compared to a standalone IGBT. The gate resistor for the SiC

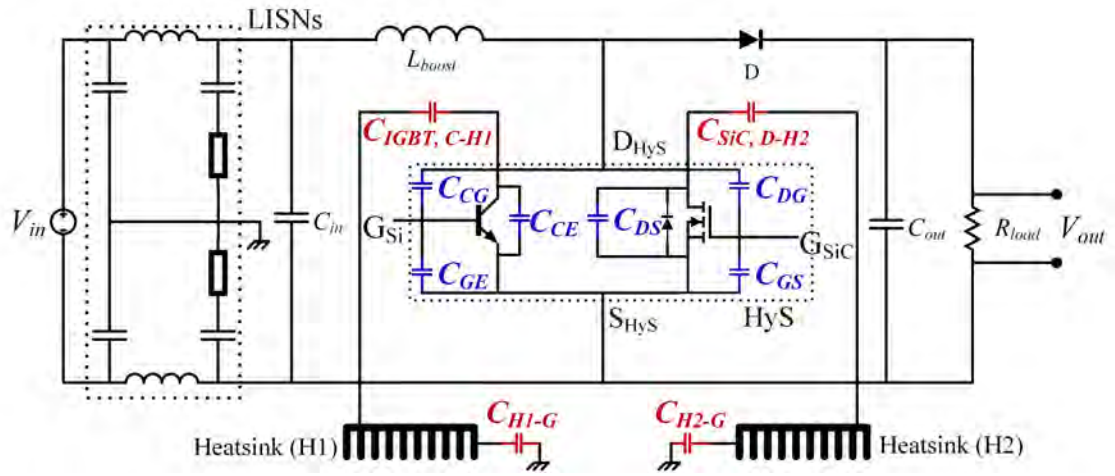

Figure 2.26: HyS based DC-DC boost converter test schematic with common-mode capacitances (red) and switching device stray capacitances (blue)

MOSFET was 6.67 Ω for all the test results and that the savings in switching losses can further increase if a smaller gate resistance value is used.

2.7.2 Comparison of Electromagnetic Interference in a HyS, all-Si and all-SiC based converter

Introduction

HyS demonstrates static and dynamic performance benefits compared Si IGBT and low cost compared to SiC MOSFET. However, the electromagnetic interference (EMI) emissions of the HyS could be higher than SiC. Hence, comparison of EMI in a HyS, all-Si and all-SiC based converter is presented. The main source of EMI noise in a power converter is the switching device. Its switching speed will characterize the high-frequency conducted noise emissions. However, the parasitic common-mode capacitances, especially the capacitance between the switching node (drain terminal of the switching device) and the ground (usually a grounded heatsink) provides path for the high frequency noise propagation and

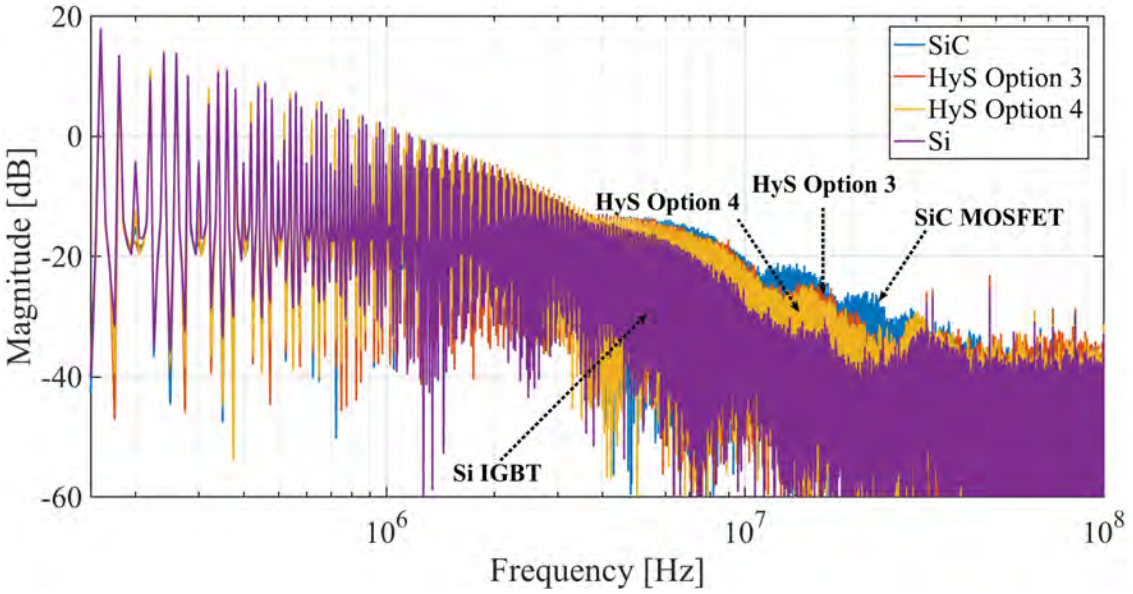

Figure 2.27: Magnitude spectra of V_{DS}, V_{HyS} and V_{CE} trapezoidal switching waveform measured from the tests

also characterize the high-frequency emissions. It has been demonstrated in literature [26], that when comparing a SiC MOSFET and Si IGBT with identical voltage and current ratings, both packaged individually in a TO-247 package, and utilized in same converter setup, the SiC MOSFET exhibits higher conducted emissions in high-frequency range compared to Si MOSFET. This is attributed completely to the fast switching speed of SiC, as in this case both the packages have equal area and thus equal common-mode capacitance. While designing a package for SiC devices, efforts are made to reduce the package area to restrict the common-mode capacitance and hence the EMI. However, in a HyS power package, when using a large Si IGBT die and a smaller SiC MOSFET die, the effective area of the HyS package will be significantly larger than a standalone SiC MOSFET and a standalone Si IGBT package. This is under the assumption that the Si and SiC dies, within the module, are placed far apart to avoid any thermal coupling (i.e. complete thermal isolation). Depending on the relative difference in the package area and the switching speeds, the HyS

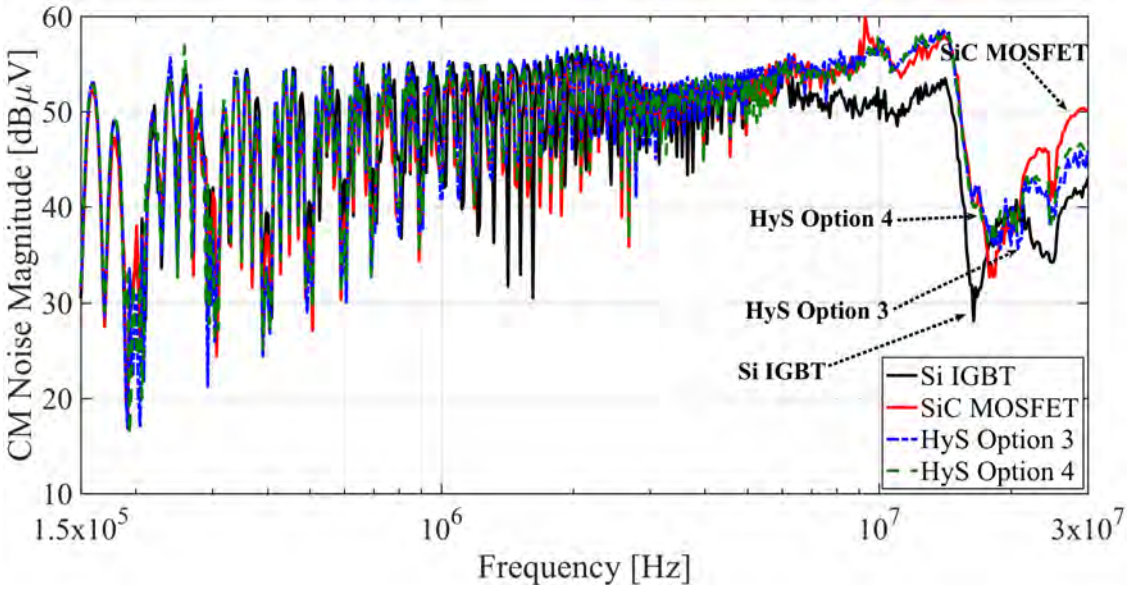

Figure 2.28: Comparison of CM noise emission

EMI emissions could be more than SiC.

In the following subsection, noise emission comparisons are made between HyS, Si and SiC based converter. The measurements are analyzed for drawing conclusions towards the EMI in a HyS based converter. Firstly, the magnitude spectra of the trapezoidal voltage switching waveform across the devices is used for comparative EMI analysis [27]. Further, a preliminary correlation between the results from the spectra and the conducted emissions measured is presented.

Noise Measurements and Analysis

Using the commercial devices listed in Table 2.1, conducted EMI noise emissions are measured in a DC-DC boost converter (Fig. 2.26) without EMI filters. Successive measurements were made on the converter with a standalone Si IGBT, a standalone SiC MOSFET, and a Si IGBT + SiC MOSFET HyS acting as the switch. Further, the HyS was operated

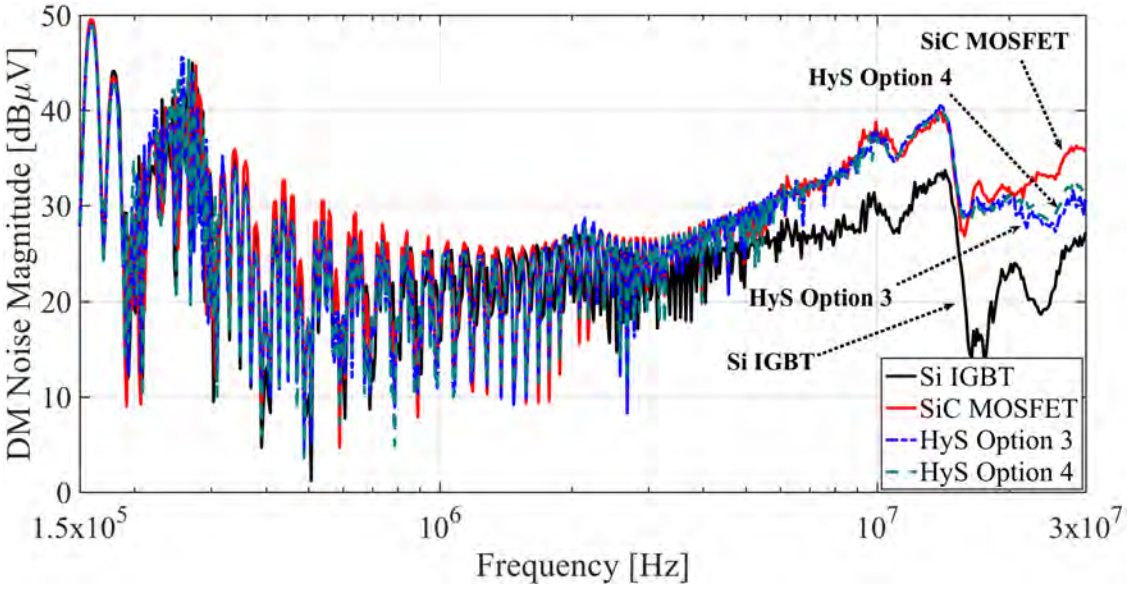

Figure 2.29: Comparison of DM noise emission

with gate control options 3 and 4. The noise emissions were recorded in the frequency range of 150 kHz to 30 MHz, which is consistent with the EMC testing standard, CISPR-22. Line-impedance stabilization networks (LISNs) are inserted between the DC source and DC-DC boost converter for EMI measurement. Using RF power splitters at the output of LISNs, the common-mode (CM) and differential-mode (DM) noise emissions were measured separately. The operating conditions of the converter at the instant of measurement are listed in Table 2.6. The common-mode (CM) and differential-mode (DM) noise emission spectra comparisons are shown in Fig. 2.28 and Fig. 2.29 respectively.

As a first step, the comparison between HyS, all-Si and all-SiC technology is made based on the spectra of switching voltage across the device. The dv/dt of the SiC MOSFET is inversely proportional to the C_{DG} of the device as shown in (2.14). Consequently, the rise and fall times relative to the V_{DS} are directly proportional to the C_{DG}. However, in (2.14), the effect of C_{DS} is not modeled [28]. C_{DS} charges and discharges along with C_{DG}

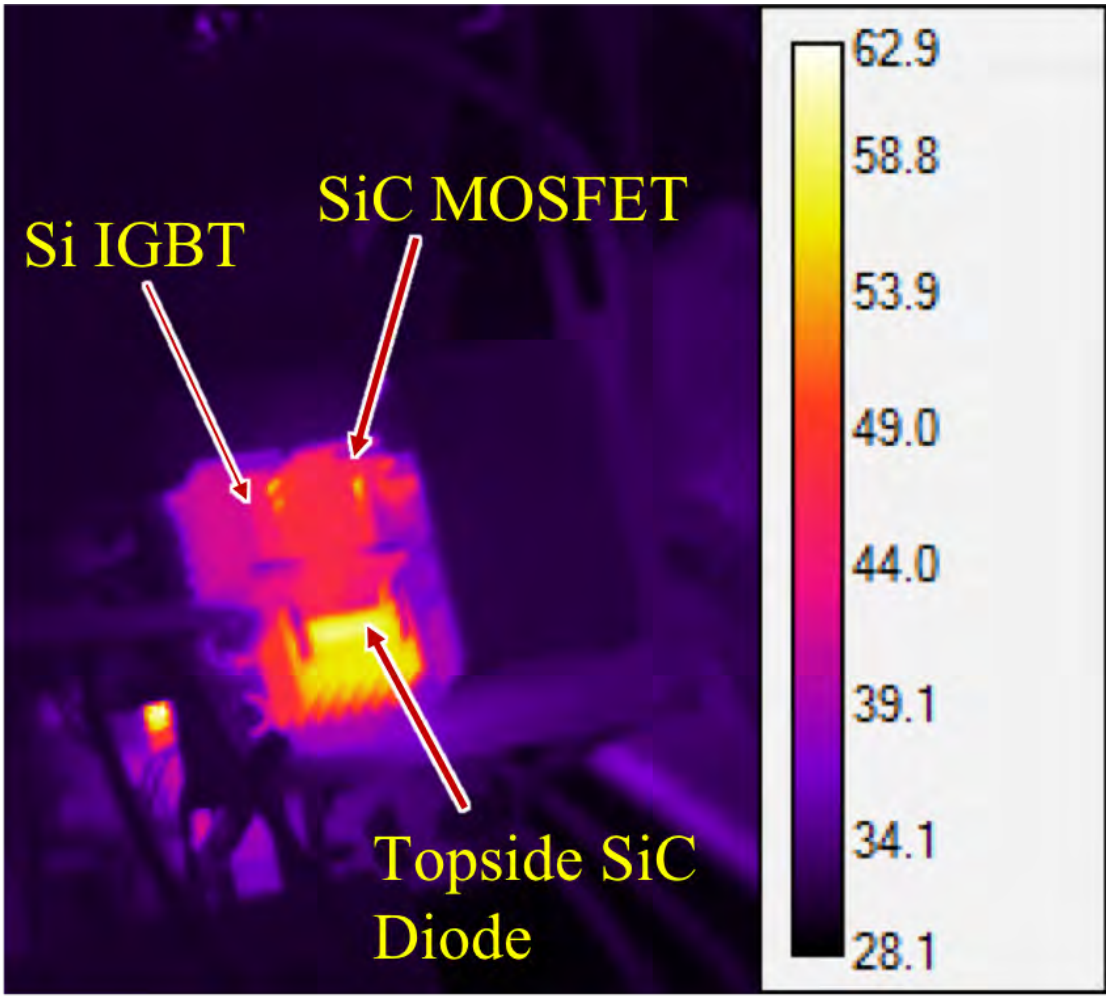

Figure 2.30: IR thermal image recorded during boost converter operation

during the device turn-off and turn-on respectively. Hence, C_{DS} also affect the rise and fall times of the voltage. The C_{CE} capacitance of Si (which is approximately 2 times the C_{DS}), is in parallel with the C_{DS} capacitance of SiC as shown in Fig. 2.26, which increases the effective capacitance across the drain and source of the HyS. Under the influence of this effective capacitance, the voltage rise and fall times will increase during the HyS switching compared to a standalone SiC. The switching speeds associated with voltages of each device are measured from experiments and documented in the Table 2.5. The switching speed of the HyS is slower than a standalone SiC device but faster than standalone Si IGBT. Consequent

effect can be observed in the magnitude spectra for each device presented in Fig. 2.27. In 10-30 MHz frequency region, the SiC spectral magnitude is 0 to 10 dB higher than of the HyS option 3 and option 4. Whereas, the HyS spectral magnitude is 5 to 15 dB higher than that of the Si device.

The Si device in a TO-247 package and the SiC device in a TO-220 package are placed on separate heatsinks, to achieve thermal isolation. $C_{IGBT,C-H1}$ and $C_{SiC,D-H2}$ are the parasitic CM capacitance (C_{CM}) between the collector/drain of Si IGBT/ SiC MOSFET and the heatsink. Since, during the experiment the heatsinks were isolated from ground, C_{H1-G} and C_{H2-G} are the parasitic CM capacitance between respective heatsinks and ground. Moreover, in this setup (as shown in Fig. 2.26), with the common mode capacitance between each device tab and heatsink in parallel, the HyS had a higher effective CM capacitance. The CM capacitance of the HyS is given by (2.15). The dv/dt under the presence of CM capacitance, depicted in Fig. 2.26, will result in CM noise emissions. It will be important to understand EMI emission level for the HyS in comparison to a standalone Si and SiC device under the influence of both the common-mode capacitance and switching speeds as documented in the Table 2.5, which will be captured in the CM noise measurements through LISNs.

In addition to the dv/dt, the common-mode capacitance calculated for each device will further affect the emissions in all the device. The effect of common-mode capacitance along with the dv/dt can be seen in the CM and DM noise emissions recorded separately from the LISNs. The fall and rise times for a standalone SiC switching are 10 and 20 ns respectively. Correspondingly, they have bandwidths of 17 and 32 MHz. In the Fig. 2.28, the CM noise emissions for SiC are 10-15 dB higher than Si in the frequency range of 17 MHz to 32 MHz. The HyS Options 3 and 4, have fall and rise times of 30 ns and hence a

corresponding 39 dB peak around 10 MHz is observed. Si device has a fall time of 30 ns as well and hence it also has a 31 dB peak at around 10 MHz, 8 dB lower than the peaks for SiC and HyS. Similar differences were found in the DM noise emissions measured. Overall, both CM and DM noise emissions measurement indicate that, the SiC and HyS options 3 and 4 have equal emission level upto 20 MHz. Above 20 MHz, the SiC emission levels are 5-10 dB higher compared to HyS options 3 and 4. The difference of about 5 dB between SiC and HyS magnitude spectra in the 10 - 20 MHz region (as seen in Fig. 2.27), has reduced to almost zero, when comparing the CM and DM noise emissions (as seen from Fig. 2.28 and Fig. 2.29). This change is attributed to the high C_{CM} for the HyS. Hence, highlighting the importance of achieving a low C_{CM} package.

$$\frac{dV_{DS}}{dt} = \frac{V_{plateau}}{R_g C_{DG}} \tag{2.14}$$

$$\begin{aligned} C_{CM}|_{HyS} &= (C_{IGBT,C-H1} || C_{H1-G}) \\ &\quad + (C_{SiC,D-H2} || C_{H2-G}) \end{aligned} \tag{2.15}$$

A further detailed explanation of the EMI behavior is possible if more frequency dependent characteristics of the parasitic coupling paths within the converter are modeled. However, such a modeling is outside the scope of this work and will be a valuable area of future work.

Table 2.5: Measured voltage rise and fall times, Device output capacitances and common-mode capacitances

Device	t_{vf} [ns]	t_{vr} [ns]	C_{CE}/ C_{DS}/ $C_{DS,HyS}$ [pF]	C_{CM} [pF]
Si IGBT	30	85.6	151	0.47
SiC MOSFET	10	20	77	0.37
HyS Option 3	30	30	228	0.83
HyS Option 4	30	30	228	0.83

Table 2.6: DC-DC boost converter specifications and operating conditions

Parameter	Value
V_{in}/ V_{out}	44 V/ 220 V
D	0.8
f_{sw}	20 kHz
L_{boost}	91 μH
C_{in}/ C_{out}	385 μF/ 40 μF
R_{load}	89 Ω

2.7.3 Thermal

To verify the findings of the peak junction temperature and the SiC package, as presented in section VI, steady state temperature measurements were made during the converter operation (see Table 2.6). The operating point of the boost converter was at $V_{in} = 30$ V, $V_{out} = 60$ V, $D = 0.5$ and $f_{sw} = 20$ kHz under forced convection for the heatsinks. The measured case temperature from the IR camera for the SiC and the Si device in the HyS was 56 °C and 47 °C respectively. The thermal image from IR camera is shown in the Fig. 2.30. Also, it is important to note that both devices used separate heatsinks, hence negligible thermal interaction or coupling can be assumed. In this 1:5 HyS, the small SiC device has a high thermal resistance and low thermal capacity, hence resulting in a peak junction temperature, and a

higher average case temperature, about 9 °C higher than Si device case temperature. This test was performed using a standard silicone based thermal interface material pad as well as a phase change material (high thermal capacity) based thermal interface pad. However, they both yielded the same steady state temperatures. In agreement with the findings on peak junction temperatures and different packages in section VI, the high junction temperature of the SiC in a HyS is attributed to the small die size (high thermal resistance and low heat capacity) and the TO-220 package used for the SiC device. An improved package for the SiC here would have resulted in low peak junction temperature. Hence, innovative packaging of the SiC die in the HyS for better thermal management and low C_{CM} (as per the findings in subsection B of section VII) will be a valuable area of future work.

2.8 Conclusion

In this paper, a HyS consisting of a large Si IGBT and small SiC MOSFET device (low SiC/Si current ratio below unity) in parallel is proposed for high-current, high-power power conversion systems. The major contributions of this paper are as follows: 1). Using a systematic analysis involving parametric sweep, the influence of the parasitic interconnection inductance unbalance between Si and SiC device within the HyS is studied. A boundary-line of inductance unbalance is estimate to be 10 nH, which helps to decide between gate control option 3 and 4. 2). A comprehensive cost analysis was performed using commercial 1.2 kV devices. It was found that with a 1:4 and 1:6 SiC/Si current ratios, the cost for HyS at currents above 50 A will be 50 to 75% lower for discrete devices. Moreover, a maximum of 60% cost saving is achieved at 300 A, when comparing 1:6 HyS module with an identical current rated SiC module. And, in the 300 A to 1200 A current range, the HyS will serve as

a direct and the only replacement option for all-Si IGBT module. 3). An algorithm using a dynamic junction temperature prediction is presented, to select an optimum SiC/Si current ratio, which ensures a reliable HyS operation. Moreover, it is demonstrated with the aid of a design example that 1:6 ratio HyS is possible, with the availability of an improved package, while using a lighter cooling system, enabling high specific-power density. 4). From the experiment results, the savings in the switching loss by using the gate control option 3 are highlighted, which will allow the HyS based converter operation at high frequency to achieve high-power density. Finally, a 650 V Si IGBT and SiC MOSFET based HyS with a 1:5 SiC/Si current ratio was successfully demonstrated in a DC-DC boost converter. Also, EMI noise measurements and analysis is presented for the HyS based converter operation. This analysis in conjunction with the insights on thermal management requirements will help to shape the future work of a co-packaged HyS module.

Acknowledgment

The authors would like to thank Mr. Balaji Narayanasamy for his guidance and inputs on the EMI testing and analysis.

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3 Design of a High Efficiency, High Specific-Power Three-level T-type Power Electronics Building Block for Aircraft Electric-Propulsion Drives

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3.1 Abstract

The electric propulsion drives for the more-electric aircraft need lightweight and high-efficiency power converters. Moreover, a modular approach to the construction of the drive ensures reduced costs, reliability, and ease of maintenance. In this paper, the design and fabrication procedure of a modular dc-ac three-level t-type single phase-leg power electronics building block (PEBB) rated for 100-kW, 1-kV dc-link is reported for the first time. A hybrid switch consisting of a silicon IGBT and silicon carbide MOSFET was used as an active device to enable high switching frequencies at high-power. The topology and semiconductor selection were based on a model-based design tool for achieving high conversion efficiency and lightweight. Due to the unavailability of commercial three-level t-type power modules, a PCB- and off-the-shelf discrete semiconductor-based high-power switch was designed for the neutral point clamping. Also, a non-trivial aluminum-based multilayer laminated busbar was designed to facilitate the low-inductance interconnection of the selected active devices

and the capacitor bank. The measured inductance indicated symmetry of both current commutation loops in the busbar and value in the range of 28 - 29 nH. The specific-power and volumetric power density of the block were estimated to be 27.7 kW/kg and 308.61 W/in3, respectively. The continuous operation of the block was demonstrated at 48 kVA. The efficiency of the block was measured to be 98.2%.

3.2 Introduction

The aerospace industry is continuing with its plans to make the aircraft more-electric for increasing fuel efficiency, reliability, and reducing the audible noise [1]. Electric systems have replaced mechanical hydraulic and pneumatic systems in the state-of-the-art commercial aircraft like Boeing 787 and Airbus A380 [1]. In the future, the more-electric aircraft will incorporate a hybrid turbo-electric propulsion system [2]. The dc-ac power converters used for the turbo-electric propulsion system must achieve a specific-power greater than 20 kW/kg [2]. Additionally, the dc-ac power converters must have efficiencies greater than 99.5% [2]. The low-weight and high electrical efficiency of the power converters result in increased fuel efficiency [3]. The operation of these power converters at switching frequencies well above 20 kHz reduces the audible noise for humans. Also, power converters built in a modular approach lends the much-desired reliability and ease of maintenance of the aircraft.

A power electronics building block (PEBB), introduced by Ericsen et al. [4], integrates power devices, gate drives, DC-link capacitors, and accessible interface for power and control [4–7]. The building block facilitates a modular converter implementation that reduces engineering efforts, testing times, costs, and weight [4–8]. The modular implementation also allows for increased reliability [9]. A multi-layer laminated busbar serves as an integral part

of the PEBB. The busbar enables the interconnection of power device packages and the capacitors. The block may have provision for adding more components in the future. The design and fabrication of PEBBs reported in the literature includes the conventional two-level phase-leg [10–13], two-level three-phase [14], h-bridge [15], [16], and three-level neutral point clamped circuit topology [12], [17–21].

In this paper, we report on the design and fabrication of a PEBB with a three-level t-type single-phase circuit topology for the first time. A three-level t-type topology for dc-ac power conversion is reported to have better efficiency compared to the conventional two-level topology [22]. Moreover, the decision to use a three-level t-type topology was made using a model-based multi-objective optimization for the required specifications of the PEBB. A hybrid switch consisting of a silicon and silicon carbide transistor was used as an active device. Due to the unavailability of Si-IGBT and SiC-MOSFET based three-level t-type standard modules, the busbar design is not trivial. Hence, a novel design of a low-weight multi-layer laminated busbar to achieve symmetrical and low-inductance current commutation loops is discussed. The inductance of the fabricated busbar was measured to verify the design. Further, the design of a PCB-based switch, which is one of the switches in the common-source clamping leg of the three-level t-type topology, is discussed. The approach to the design of the thermal management system is outlined. The specific-power and the volumetric power density of the fabricated PEBB were estimated. Finally, the continuous operation of the PEBB was demonstrated with an inductive load at 48 kVA.

3.3 Design Procedure of a Three-level T-type PEBB

3.3.1 Topology selection

The selection of the topology for a high-efficiency, high specific-power PEBB was aided by a model-based multi-objective optimization [23], based on semi-physical mathematical models. It includes weight and cost models apart from the loss model. For the listed required specifications of the PEBB in Table 3.1, three different converter topologies were considered: two-level converter (2LC), three-level neutral point clamped converter (3L-NPC2), three-level T-type neutral point clamped converter (3L-T2NPC2). Moreover, three active device technologies for each topology were considered: all-Si-IGBT, all-SiC-MOSFET, and Si-IGBT + SiC-MOSFET based Hybrid Switch (HyS) [24]. HyS is a parallel combination of a silicon (Si) insulated-gate bipolar junction transistor (IGBT) and silicon carbide (SiC) metal-oxide semiconductor field-effect transistor (MOSFET) as shown in Fig. 3.1a. It combines the benefits of the high-current carrying capability of the Si-IGBT and the fast switching capability of the SiC-MOSFET for high efficiency or high switching frequency operation [24]. The switching sequence of the Si-IGBT and SiC-MOSFET within the HyS is shown in Fig. 3.1b. This switching sequence allows for a zero-voltage switching (ZVS) turn-on and turn-off of the slower Si-IGBT resulting in lower switching energy. Moreover, it yields a low-cost solution compared to an all-SiC-MOSFET based implementation [24]. The radar charts in Fig. 3.2 map the efficiency (based on active device loss), active device weight, and active device cost at a fixed switching frequency resulting from the optimization for the topologies under consideration.

Fig. 3.2 indicates that all-Si-IGBT based topologies have the worst efficiency across

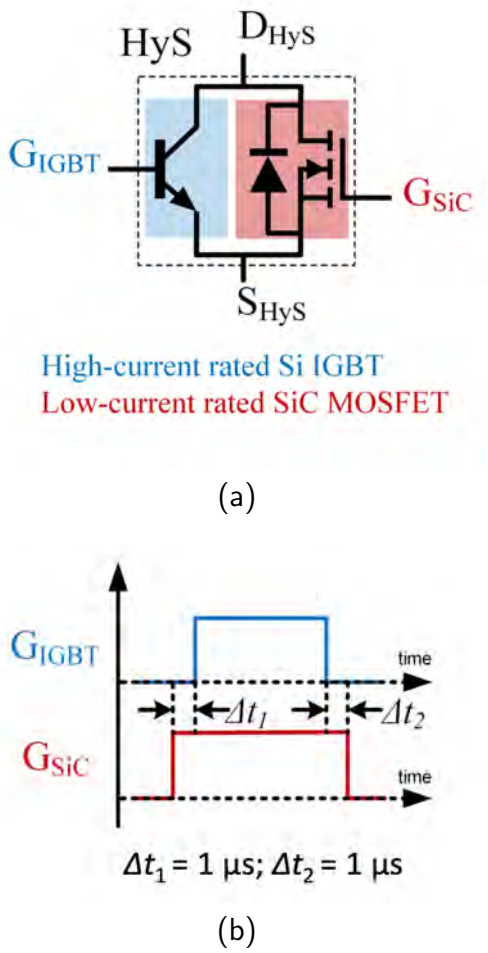


Figure 3.1: (a) The schematic of a hybrid switch with Si-IGBT and SiC-MOSFET connected in parallel. (b) The turn-on and turn-off sequence of the Si-IGBT and SiC-MOSFET in the hybrid switch.

the board. Hence, all-Si-IGBT technology was excluded from further consideration. HyS provides the highest efficiency for all topologies with a maximum for 3L-T2NPC2 (see Fig. 3.2d). Moreover, HyS-based 3L-T2NPC2 led to lower weight compared to the next best efficient 3L-NPC2, which has a relatively higher part count. Hence, a HyS-based 3L-T2NPC2 topology was determined for the implementation of the PEBB. The choice of a HyS-based 3L-T2NPC2 for the PEBB is further strengthened due to a low requirement on the dc-link capacitance compared to 2LC and consequent reduction in the weight from the dc-link

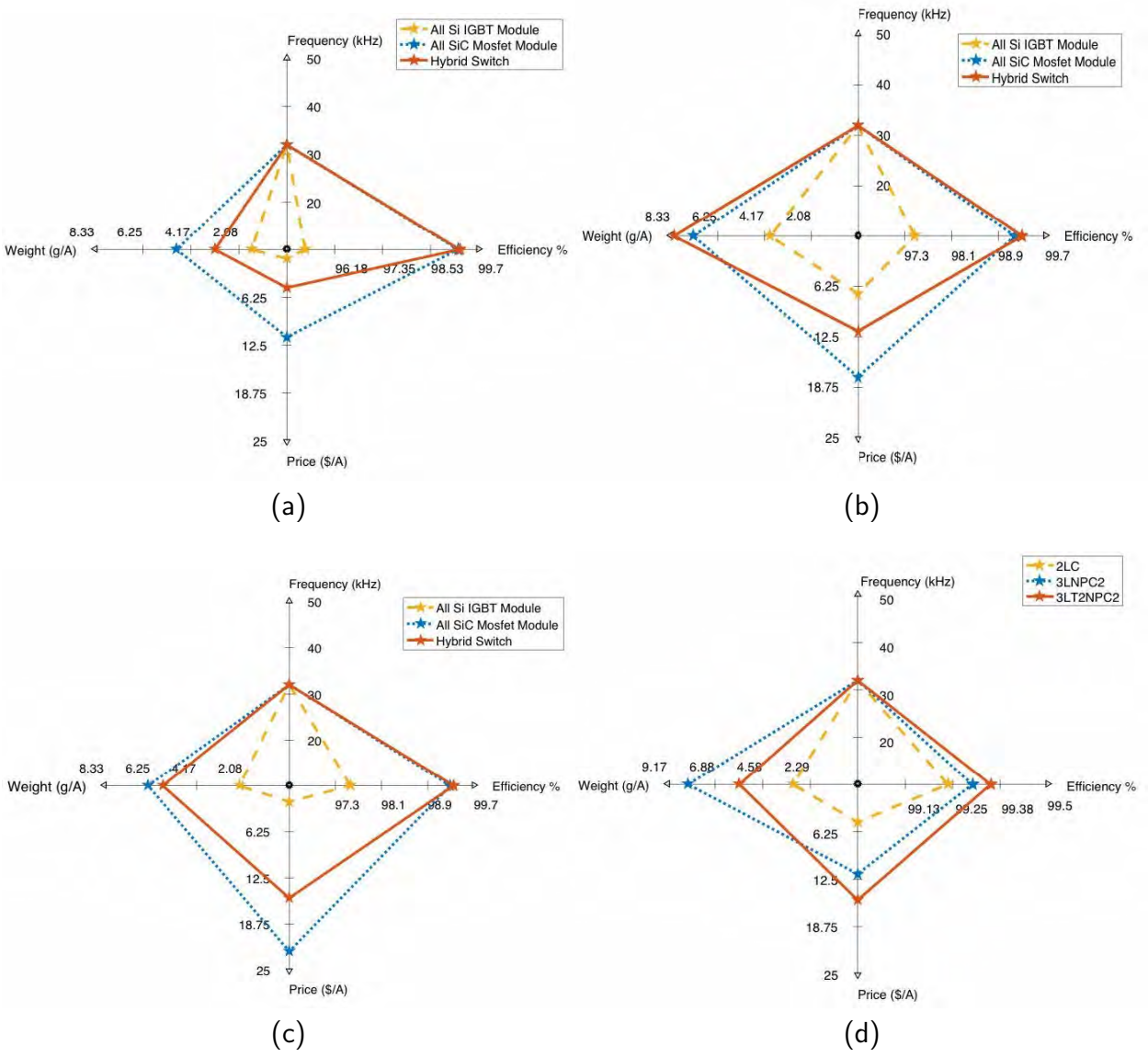


Figure 3.2: Radar charts comparing the efficiency (%), switching frequency (kHz), weight (kg), and price ($/A) for the following topologies: (a) 2LC (b) 3L-NPC2 (c) 3L-T2NPC2. (d) Radar chart comparing the efficiency (%), switching frequency (kHz), weight (kg) and price ($/A) for all HyS-based topologies.

capacitors [22]. Also, a neutral point balancing algorithm integrated into the PWM strategy would further aid the dc-link capacitance size reduction. Additionally, 3L-T2NPC2 has better output power quality [22], leading to a reduced weight from the EMI filters.

3.3.2 Device selection

Fig. 3.3 illustrates the circuit topology of a single-phase three-level t-type topology used for the PEBB. The circuit topology has four active device positions, two each for the vertical and horizontal branch referred to as the half-bridge and the clamping-leg, respectively. The SiC MOSFET M1 and Si IGBT Q1 form the hybrid switch for the high-side active device position in the HB. The diodes D1M and D1Q are the free-wheeling diodes within the M1 and Q1 transistor package, respectively. The devices in the HB, M1, Q2, M4, Q4, D1M, D1Q, D2M, and D2Q are rated to block the full dc-link voltage. The 1.7 kV Si-IGBT and 1.7 kV SiC-MOSFET HB modules from Infineon and ROHM, respectively, were connected in parallel to form respective HyS with Si/SiC current ratio of 4:1. The devices in the horizontal branch, M2, Q2, M3, Q3, D2Q, and D3Q are rated to block half of the dc-link voltage and connected in the common-source (CS) configuration. Due to the unavailability of an off-the-shelf Si- and SiC-based CS power module, PCB based switches, M2/Q2/D2Q and M3/Q3/D3Q, were prepared using discrete Si-IGBT and SiC-MOSFET devices. Each PCB included 8 units of 1.2 kV rated Si-IGBT devices from Infineon and 2 units of 1.2 kV rated SiC devices from Wolfspeed. The selected devices lend the PEBB capability of handling an active power of 100 kW. The gate drivers for the devices were configured to allow a maximum switching frequency of 28 kHz.

3.3.3 Low-inductance 3D Laminated Busbar Design

The busbar was designed for fabrication with aluminum, contrary to the conventional choice of copper, to reduce the weight and consequently meet the high specific power density

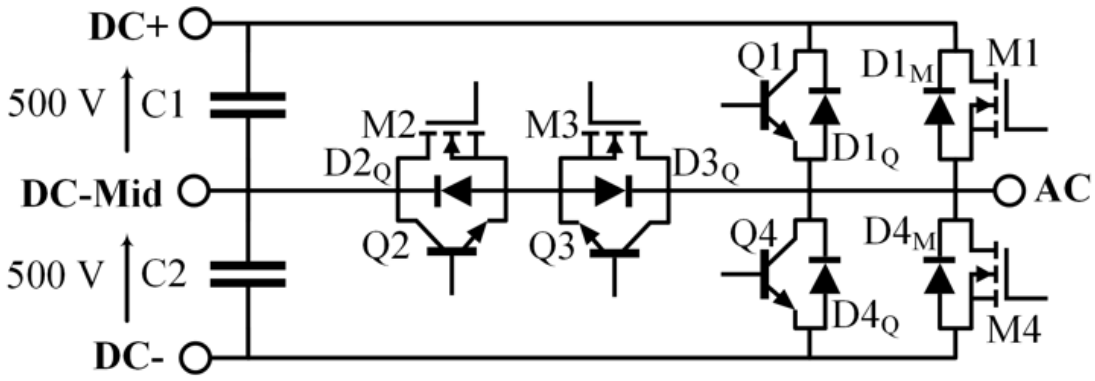


Figure 3.3: The circuit schematic of a three-level t-type topology used that consists of a hybrid switch as an active device.

Table 3.1: The electrical specifications of the designed PEBB using the three-level t-type topology shown in Fig. 3.1a

Parameter	Symbol	Unit	Value
Nominal output power	P_{out}	kW	100
Nominal DC-link voltage	V_{DC}	kV	1
DC-link capacitance	C	μF	60
Maximum switching frequency	f_{sw}	kHz	28
Nominal output phase voltage	V_o	V_{rms}	474
Nominal output phase current	I_o	A_{rms}	211

requirements. As shown in (1), a multiplier factor of 1.67 was used to incorporate a proportional lower amperage of aluminum relative to copper in the conventional equation for sizing the busbar. The sizing of a busbar determines the required cross-section area, Ac, for a rated current, I. The thickness of the busbar, Tc is decided using (2) with minimum width, Pterminal, usually the power terminals. The inductance in the current commutation loops (CCLs) of the topology comprises of the stray inductances from the dc-link capacitors, device packages, and interconnection busbar. Since a system designer has the most control over the busbar stray inductance, the busbar design is a crucial aspect of the PEBB design. To ensure a low voltage stress on each device within the PEBB, the busbar design was optimized for minimum inductance in the CCLs of the 3L-T2NPC2 topology. One of the operating areas

of the 3L-T2NPC2 where the output voltage is positive and the current is positive at the AC node, is shown in Fig. 3.4a and Fig. 3.4b. In Fig. 3.4a, devices Q1/M1 are in ON state, resulting in an output voltage of DC+ and a positive current. In Fig. 3.4b, devices Q2/M2 are in the ON state, resulting in an output voltage of DC+/2 and a positive current flowing through Q2/M2 and D3 from N to AC. The current commutation from Q1/M1 to Q2/M2 results in the current commutation loop CCL1, as highlighted in Fig. 3.4c. Similarly, the current commutation loop CCL2, shown in Fig. 3.4d, is a result of commutation between Q4/M4 and Q3/M3. Additionally, to ensure equal voltage stress, it was ensured that the inductance in both CCLs is symmetrical. The isometric views of the optimized busbar 3D rendering are shown in Fig. 5 3.5a and 3.5b, while its cross-section shown in Fig. 3.6a. The current flux in the busbar during CCL1 and CCL2 are highlighted in Fig. 3.6b and 3.6c, respectively. The current flux directions in the plates of the busbar during each CCL allows for a negative mutual coupling effect. The negative mutual coupling amongst the plates in the horizontal section of the busbar are MN, DC+ and MN, DC-. While, in the vertical section MAC, CS and MN, CS are the negative mutual couplings. These mutual couplings are highlighted in Fig. 3.6a. As shown in (3) and (4), the negative mutual coupling ensures a low stray inductance in the respective loop by reducing the self-inductance effect of each plate. The inductance of the fabricated busbar was measured using a Keysight 4294A precision impedance analyzer for validating the design. Both current commutated loops within the busbar were measured. Busbar terminals were shorted appropriately to create the presence of an on-state active device in the current commutation loop. The impedance was measured over a frequency range of 40 Hz – 110 MHz. The frequency of interest was 1 – 10 MHz that corresponds to the bandwidth of an active device switching speed.

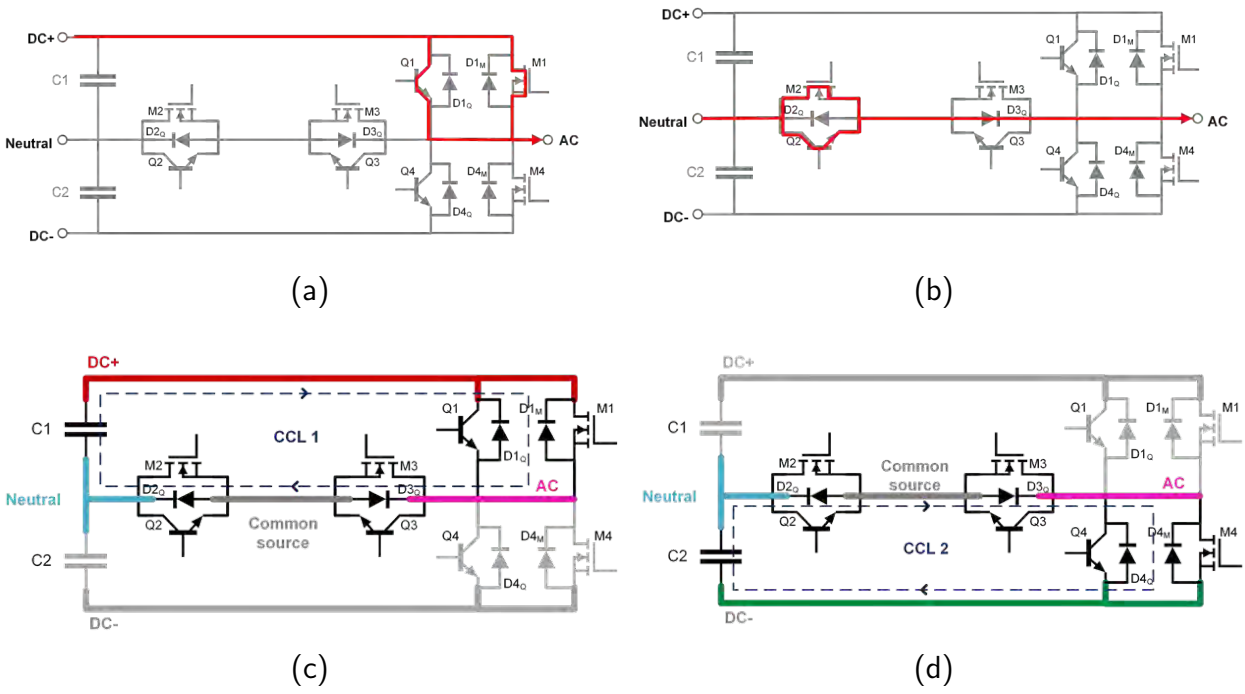


Figure 3.4: (a) The output voltage is DC+; output current is positive. (b) The output voltage is N; output current is positive. (c) The current commutation loop (CCL) #1 formed by the transition from (a) to (b). (d) The current commutation loop #2.

The measured impedance magnitude and phase plot for the fabricated busbar in one of the current commutation loops is presented in Fig. 3.7. The inductance of the busbar is extracted from the measured impedance value at 1 MHz, the approximate bandwidth corresponding to the turn-on and turn-off switching speed of the active SiC MOSFET. The inductance was calculated to be 28.01 nH at 1 MHz.

$$A_c = I \times 400 \times 0.785 \times 1.67 \times 10^{-6} \tag{3.1}$$

$$T_c = A_c / P_{terminal} \tag{3.2}$$

$$\begin{aligned} L_{CCL1} &= L_{AC} + L_{CS} + L_N + L_{DC+} \\ &+ 2M_{AC,CS} + 2M_{AC,N} + 2M_{N,CS} + 2M_{N,DC+} \end{aligned} \tag{3.3}$$

$$\begin{aligned} L_{CCL2} &= L_{AC} + L_{CS} + L_N + L_{DC-} \\ &+ 2M_{AC,CS} + 2M_{AC,N} + 2M_{N,CS} + 2M_{N,DC-} \end{aligned} \tag{3.4}$$

After including the stray inductance from modules and discrete transistors, the inductance of current commutation loop 1 and loop 2 is 40.69 nH and 41.12 nH, respectively. The virtually equal inductance for both loops verifies that the busbar design yields symmetrical loops. A comparison of the extracted inductance with a few state-of-the-art busbar designs is presented in Table 3.2. The busbar design for a Si IGBT based three-phase three-level t-type 3-phase inverter by Wang, et al. [25] achieved 17 nH loop inductance due to the possibility of simple bussing resulting from a module with a three-level t-type configuration. However, the module had significant parasitic inductance resulting in a higher total commutation loop inductance of 50 nH. Another busbar design for a three-level NPC topology-based converter by Wang, et al. [26], yielded asymmetrical commutation loops with an inductance of 73 nH and 192 nH, respectively. A state-of-the-art H-bridge busbar design for a PEBB by Mehrabadi, et al. [27] achieved a symmetrical total commutation loop of 35 nH. Again, the availability of half-bridge modules allows for a more straightforward design of the busbar in H-Bridge

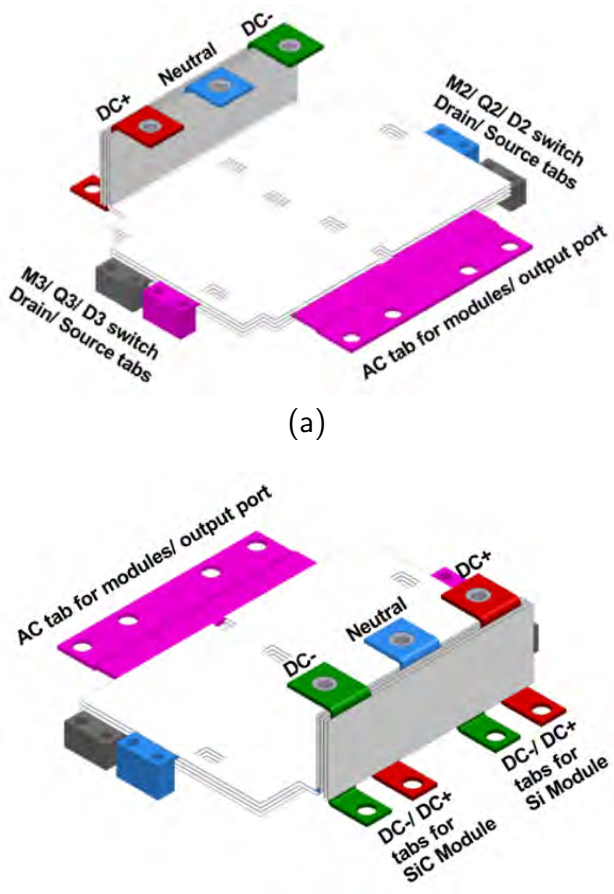


Figure 3.5: (a) Color coded CAD isometric view #1 of the designed busbar (b) Color coded CAD isometric view #2 of the designed busbar.

PEBB. Hence, in comparison to the state-of-the-art designs, the non-trivial busbar design for a three-level t-type single-phase PEBB presented, offers low inductance and symmetrical current commutation loops.

3.3.4 Clamping-leg design and PEBB Assembly

Fig. 3.13 is a picture of the fabricated PEBB. It highlights the assembly of major components within the PEBB. Due to the unavailability of an off-the-shelf Si- and SiC-based CS power module, a PCB based switch was prepared using discrete Si-IGBT and SiC-MOSFET devices. Each PCB includes eight 1.2 kV rated Si-IGBT devices from Infineon and

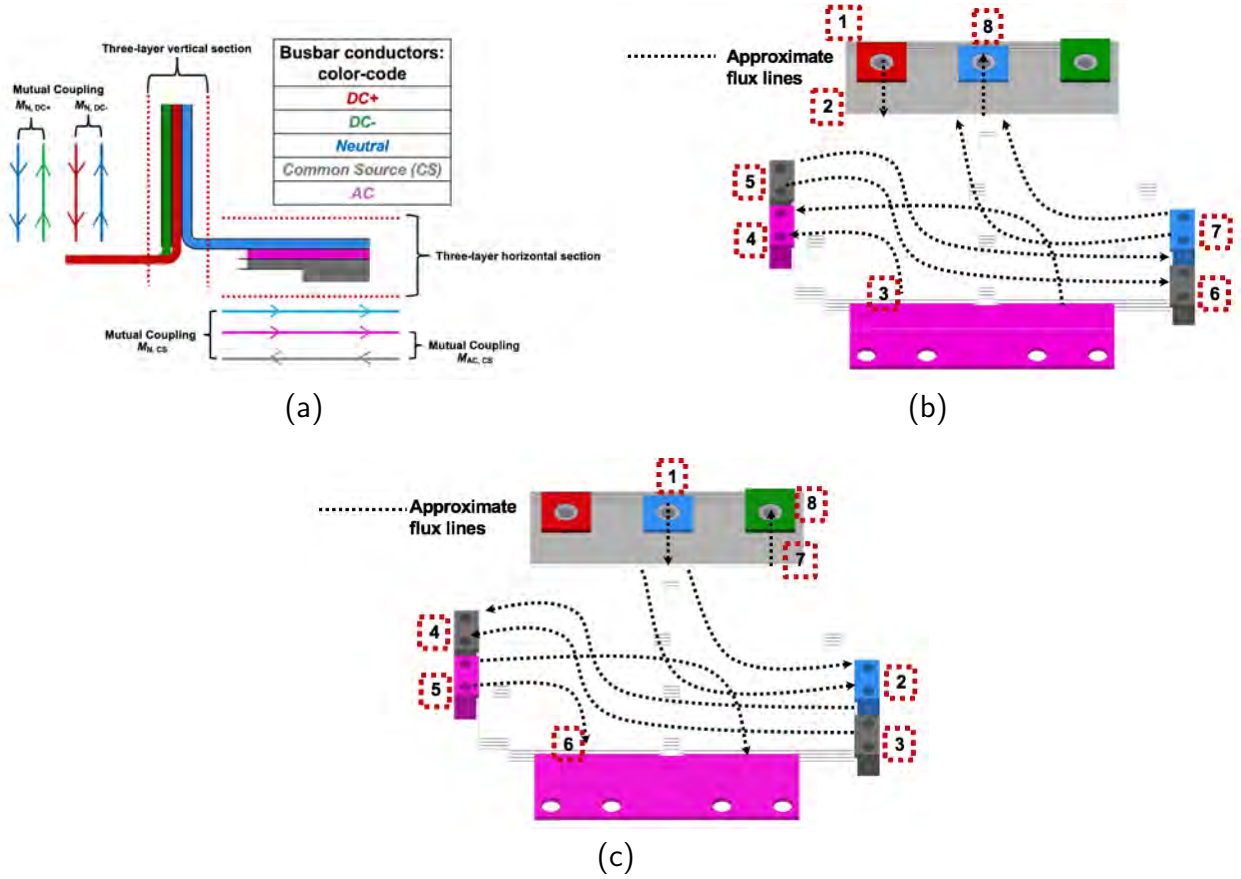


Figure 3.6: (a) The cross-section of the designed busbar highlighting the vertical and horizontal sections and the mutual coupling of current in each. (b) The current flow path in the designed busbar in the current commutation loop 1. (c) The current flow path in the designed busbar in the current commutation loop 2.

two 1.2 kV rated SiC devices from Wolfspeed connected in parallel, as shown in Fig. 3.8. The parallel combination yields a 4/1 Si/SiC current ratio. The discrete-transistor-based PCB placed on either side of the busbar allows interconnection in a common-source configuration through the busbar. They form a HyS-based clamping-leg of the 3L-T2NPC2 topology. The described spatial arrangement of both the discrete-transistor-based PCB around the busbar enables symmetrical current commutation loops, as mentioned in the previous section. A dedicated gate driver board drives each PCB in the clamping leg. The gate driver board consists of 5 isolated gate driver cells driving with each cell driving two of the discrete devices

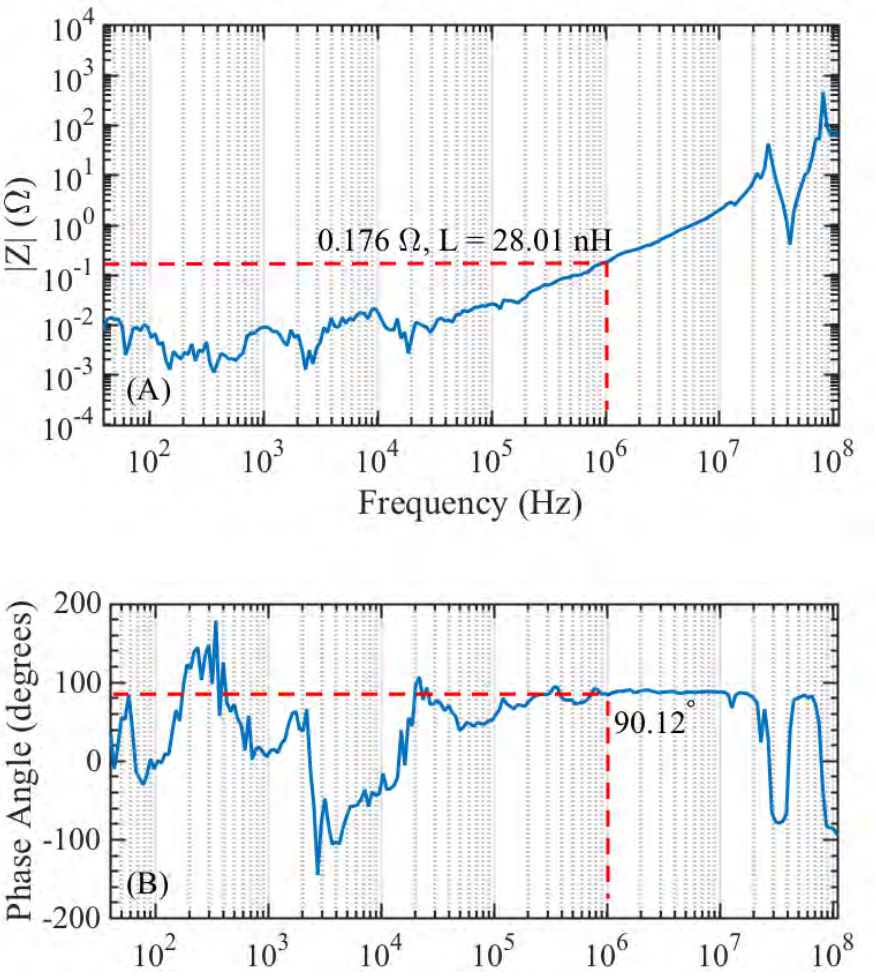


Figure 3.7: The impedance magnitude and phase angle of the fabricated busbar in the current commutated loop - 1 is measured versus frequency.

on the PCB. The routing from the signal input port on the gate driver board to each input of an isolated gate driver cell results in a signal propagation delay. The propagation delay per unit length of the microstrip is given by (5). A mismatch in the delay amongst the cells causes current sharing issues within the parallel connected devices. An interactive length tuning feature of the PCB design software was used to achieve equal lengths and consequent propagation delays and impedances for each cell. This can be seen in Fig. 3.9. The dynamic current sharing during turn-on and turn-off of the device is verified using a double-pulse test on the clamping leg switch. The test was performed at 600 V and 320 A. The measured

Table 3.2: Comparison with state-of-the-art busbars.

	DUT	Reference #1 [25]	Reference #2 [26]	Reference #3 [27]
Topology	Three-level T-Type phase-leg PEBB	Three-level T-Type, three-phase inverter	Three-level, Neutral Point Clamped, three-phase inverter	H-Bridge PEBB
Power Rating	100 kW	10 kVA	750 kVA	-
CCL 1	29.04 + 11.65 = 40.69 nH	16.711 + 33 = 49.71 nH	38.7 + 35.1 = 73.8 nH	19.77 + 15 = 34.77 nH
CCL 2	29.47 + 11.65 = 41.12 nH	17.718 + 33 = 50.71 nH	117.2 + 75 = 192.2 nH	18.9 + 15 = 33.9 nH

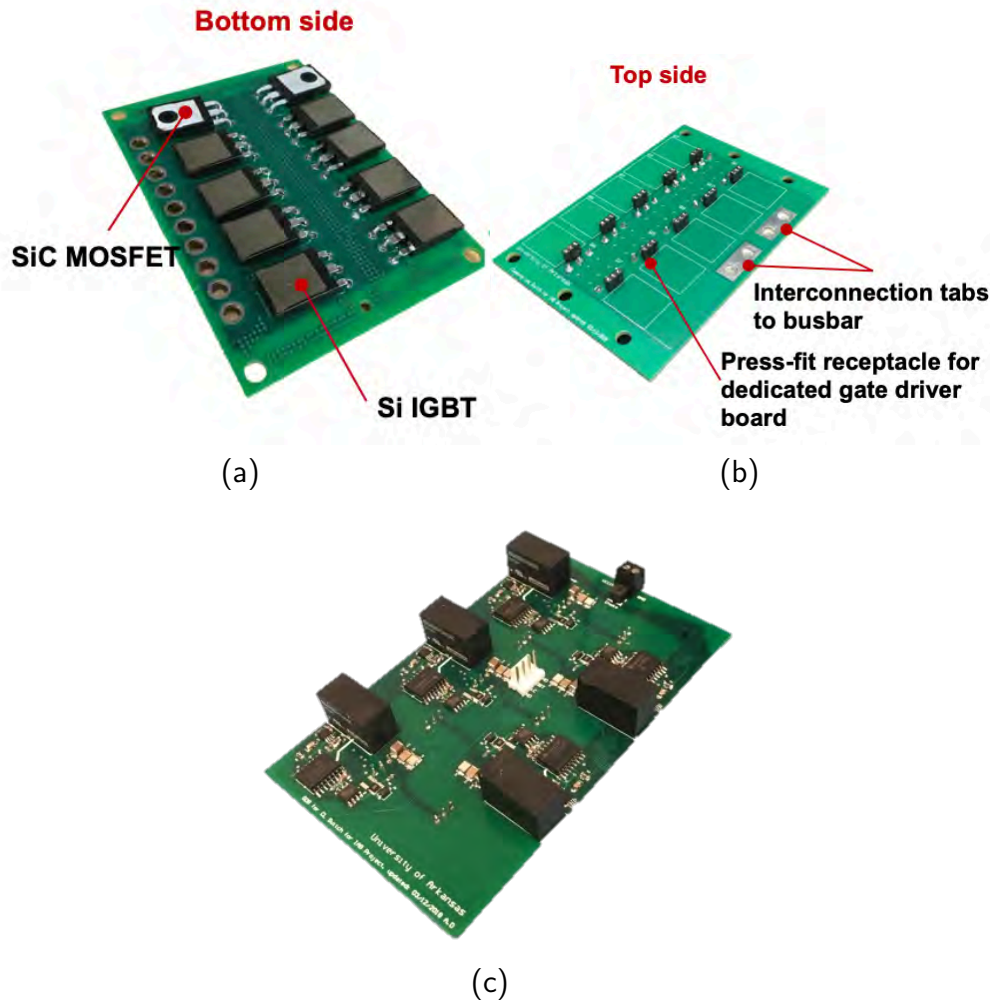


Figure 3.8: The discrete-device-based PCB for the clamping-leg: (a) Bottom-view (b) Top-view (c) Dedicated gate driver board. [Source: Photo by Author.]

currents using Rogowski coils in each of the eight Si-IGBTs of the clamping leg are shown in Fig. 3.10.

$$t_{pd-effective} = 3.34 \times 10^{-9} \times \sqrt{0.475\varepsilon_r + 0.67} \text{ s/m} \tag{3.5}$$

The laminated busbar facilitates the interconnection of the dc-link capacitor bank, HB power modules, and discrete-transistors-based printed circuit boards (PCB) for the clamping leg of the 3L-T2NPC2 topology. A 60-µF distributed PCB-based dc-link capacitor bank was designed with a series-parallel connection of 8 pieces of 30-µF film capacitors. The use of multiple small film capacitors in the design allows reducing the weight of the capacitor bank relative to a single large capacitor. The capacitor bank is connected to the vertical section of the busbar with a footprint matching the HB modules. The busbar lays on top of the Si and SiC HB modules. The height of the vertical section of the busbar is set to accommodate the HB gate driver PCB on top of each HB module. The gate driver PCBs are also mounted on top of their respective discrete-transistor-based PCBs. The HB modules and the discrete-transistor-based PCBs are installed on a heat-sink to dissipate the heat from power loss.

3.3.5 Thermal Design

The design of the thermal management system uses ParaPower, a tool co-developed by the United States Army Research Laboratory (ARL) and the United States Naval Academy [28]. The tool enables quick analysis of the design using a 3D thermal resistance network model and aids in the selection of an appropriate thermal management solution. In the tool, a rectilinear approximation of the 3D structure of the PEBB and the heatsink is constructed [29], while distributed heat power loads are assigned to each discrete device and the power

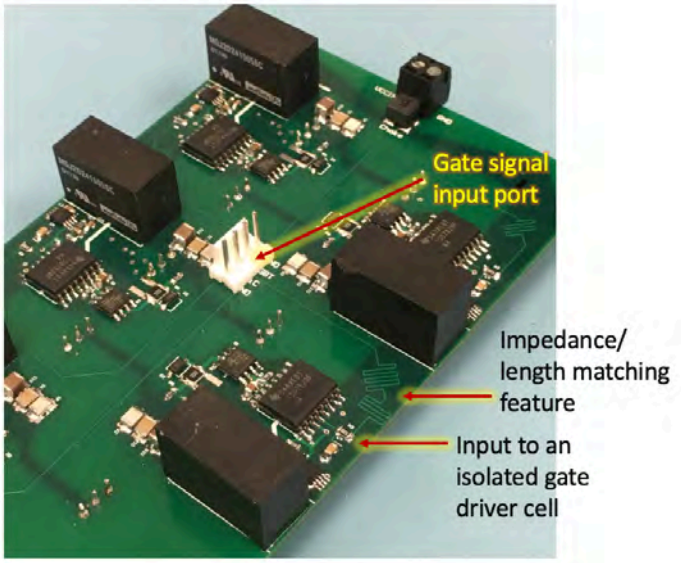


Figure 3.9: Close-up view of the gate driver board highlighting the impedance matched trace routing feature. [Source: Photo by Author.]

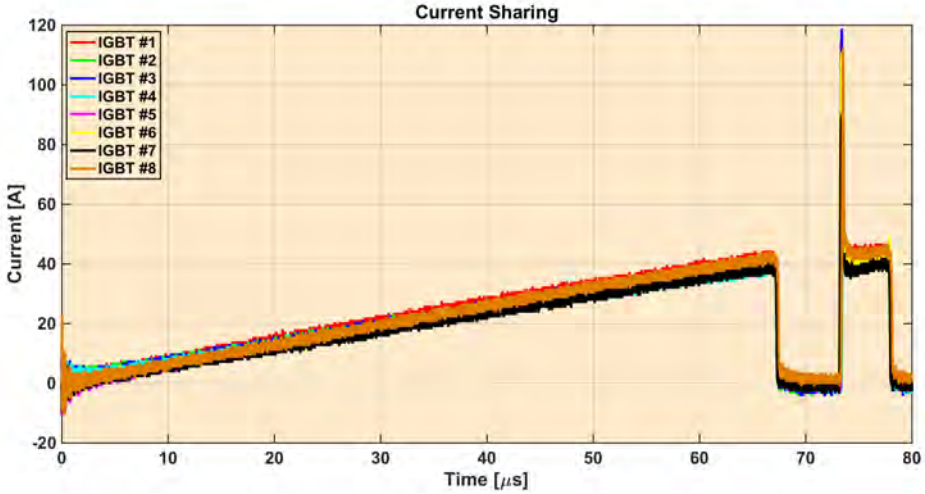
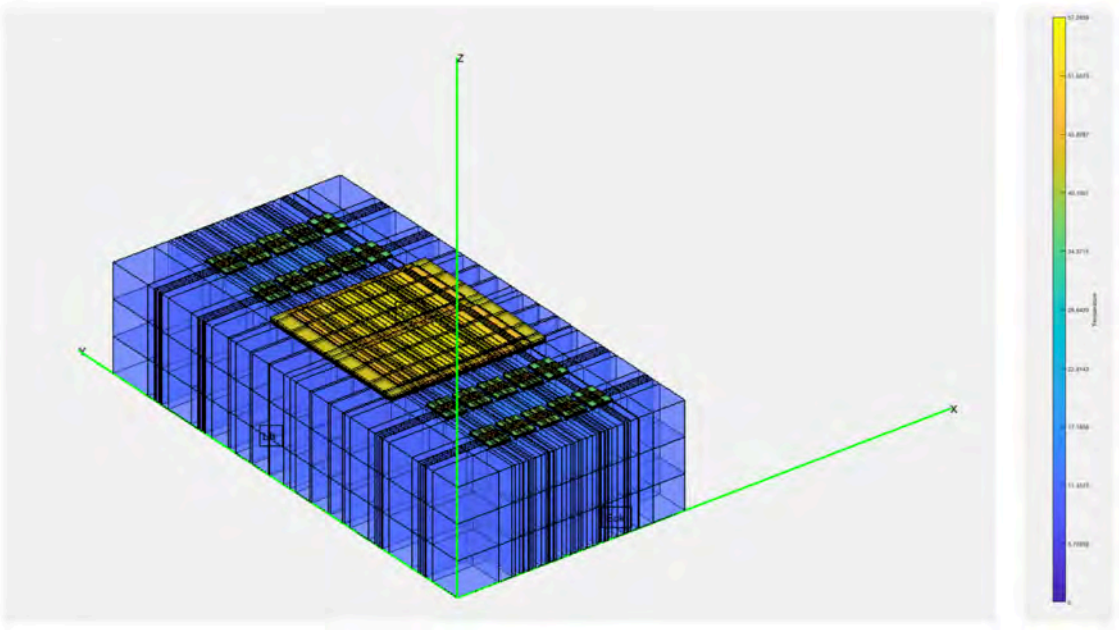
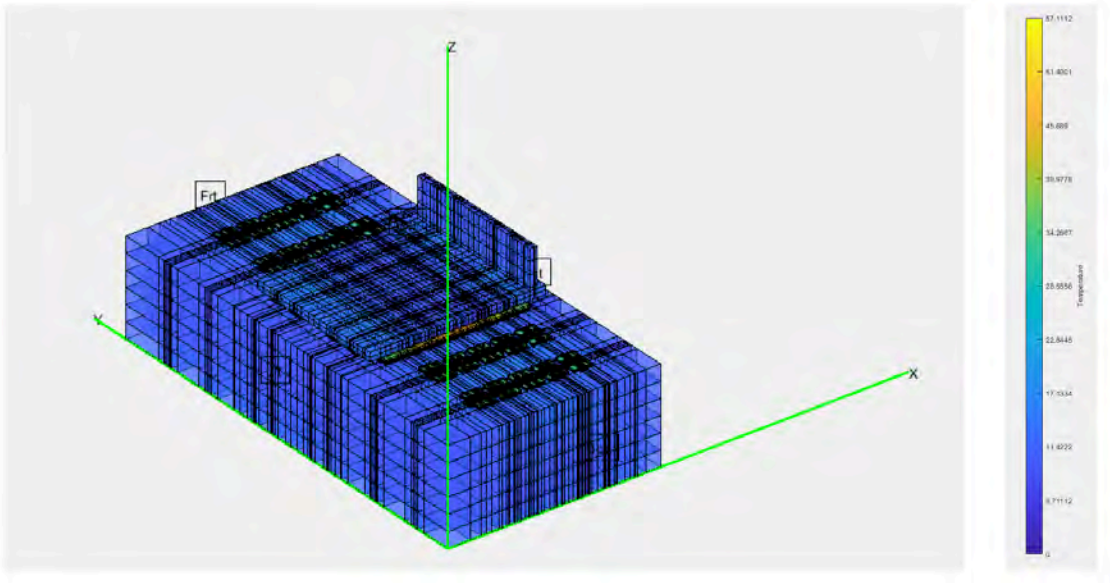


Figure 3.10: Current sharing among the eight parallel connected Si-IGBTs in the clamping leg PCB as measured when subjected to a double-pulse test.

module in the PEBB. An ambient temperature of 25 ℃ is assumed for the simulation. Fig. 3.11a and 3.11b show the 3D structure of the PEBB without and with the busbar, respectively. The peak temperature in the first case was 57.28 ℃, whereas in the second case, the temperature was found to be 57.11 ℃. The difference in the peak temperature



(a)



(b)

Figure 3.11: The steady-state thermal simulation of the PEBB design. (A) without the busbar (B) with approximate busbar.

between the two cases is less than 0.2 ℃. This indicates that the busbar does not play an integral role in the removal of heat from the design PEBB.

In the 3D model approximation, the busbar was attached directly to the module's

Table 3.3: Experiment operating conditions.

Parameter	Value
DC input voltage, V_{DC}	800 V
Load inductance, L	400 μH
Switching frequency, f_{sw}	28 kHz
HyS turn-on delay, Δt_1	1 μs
HyS turn-off delay, Δt_2	1 μs
Fundamental output frequency, f_o	666.667 Hz
Carrier ratio, f_{sw}/fo	42
Output voltage, V_{out}	313 V_{rms}
Output current, I_{out}	154 A_{rms}
Apparent output power, S_o	48 kVA

power terminals, which are laying on the top copper of the DBC. Also, the wire-bonds in the module were not modeled. The terminals do not offer a low thermal resistance path for the heat to flow to the busbars. Also, it needs to be considered that the power terminals are not attached directly to the substrate within the selected HB power modules, as seen from the internal module structure in Fig. 3.12. Also, wire-bonds are used to make electrical connections from the power terminals embedded in the power module housing to the DBC substrate. These wire-bonds contribute to high thermal resistance, and hence the busbar cannot be used for heat extraction. This explanation is valid for the discrete devices as well, where wire-bonds provide the interconnection between the die and the TO-247 package leads. However, the busbars could play a critical role in the heat extraction for modules employing large area power terminals attached to the DBC substrate directly and close to the dies. An example of such a module is CAS325M12HM2, a 62-mm high-performance, SiC MOSFET HB power module manufactured by Wolfspeed.

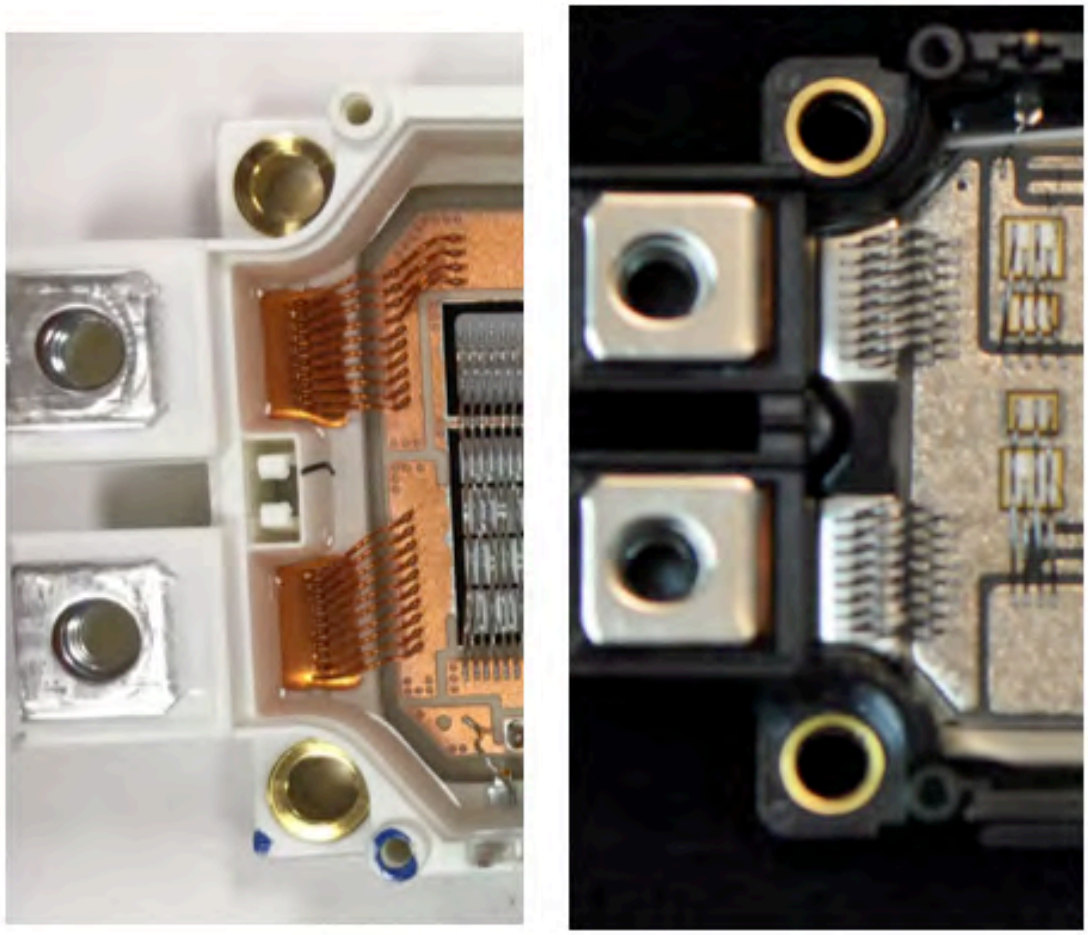


Figure 3.12: The power terminal connection inside the (A) Si-IGBT HB power module and the (B) SiC-MOSFET HB power module. [Source: Photo by Author.]

3.3.6 Experiment Results and Discussion

The assembled PEBB was tested in a single-phase inverter mode using an inductive load and the operating conditions as listed in Table 3.3. The block diagram of the single-phase system using the designed PEBB is shown in Fig. 3.14. An external DC power supply with a 1-mF bulk capacitor was connected at the DC-link power interface of the PEBB. A programmed FPGA demo-board was used to provide sine-triangle pulse width modulated (SPWM) gate signals for all the hybrid switches along with necessary dead-time

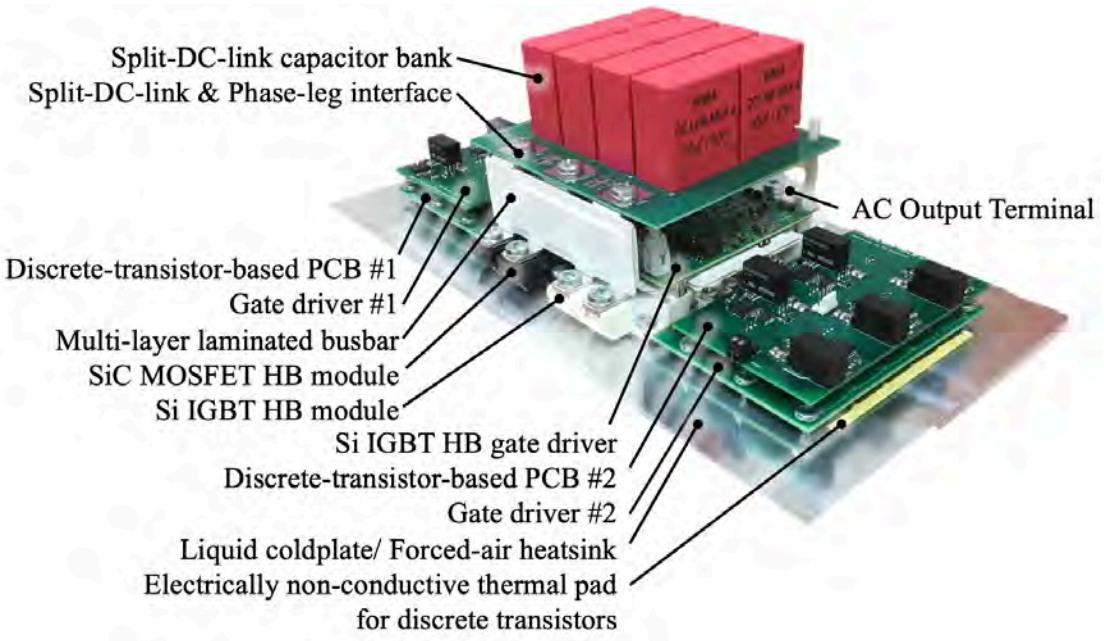


Figure 3.13: Photograph of the power electronics building block after fabrication. [Source: Photo by Author.]

at the signal interface of the PEBB. 24-V and 15-V auxiliary power supplies were used for the gate driving power supplies in the PEBB. The PEBB was assembled with a forced air-cooled heatsink. The output voltage and current were measured using a Tektronix MSO58 mixed signal oscilloscope. An active differential probe and a Rogowski coil were used for probing the output voltage and current, respectively. A block diagram for three-phase system implementation in future is shown Fig. 3.15.

The switching frequency, fsw, of the devices during the continuous operation tests of the PEBB was increased progressively from 10 kHz to the targeted 28 kHz, for safety. The measured waveforms for different switching frequency cases are shown in Fig. 3.16a through 3.16d. The effect of increasing the switching frequency at fixed output fundamental frequency, fo, is an increase in the carrier ratio, fsw/fo. The increased carrier ratio results in the reduction of the current total harmonic distortion (THD), as seen from the measured

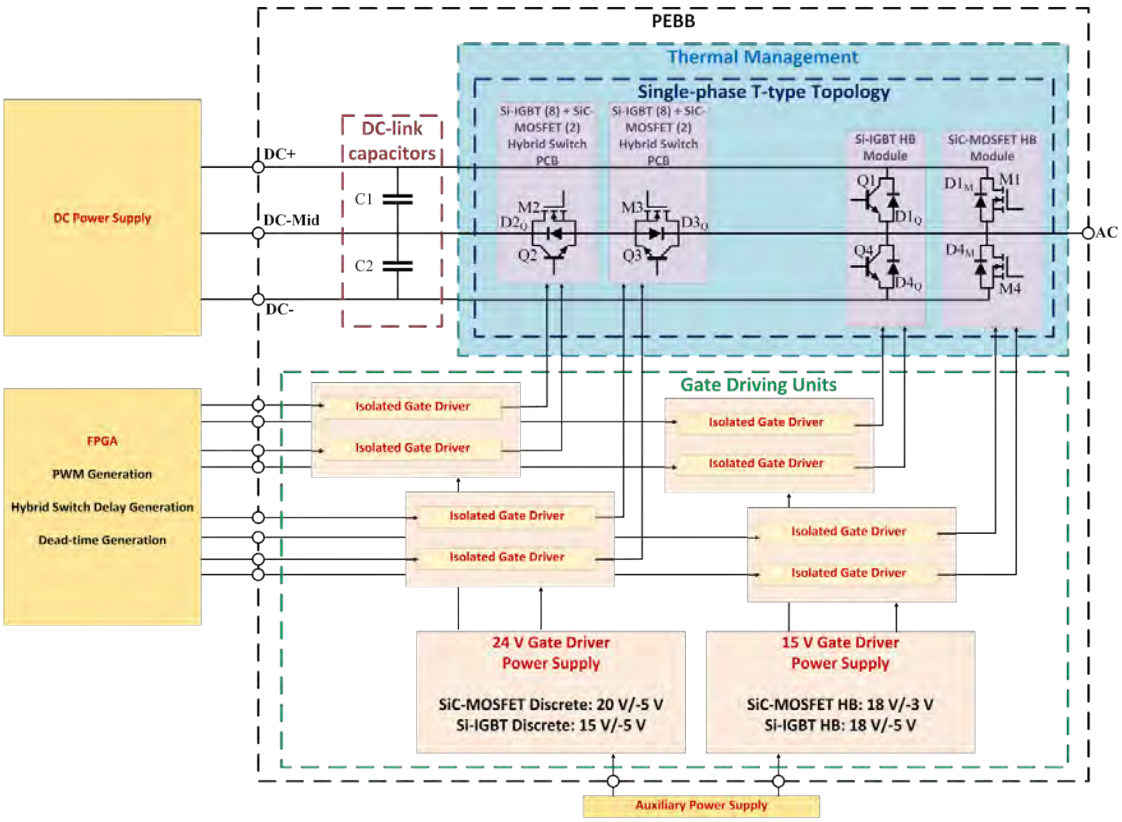


Figure 3.14: Block Diagram of the single-phase T-type inverter using the designed PEBB.

current waveforms in Fig. 3.16. Consequently, the harmonic losses in the motor will be reduced. The measured THD for the maximum carrier ratio of 42 was 6.59%, as opposed to a THD of 18.08% for a minimum carrier ratio of 15. The PEBB was finally tested at the operating conditions listed in Table 3.3. During the tests, thermocouples were employed near the HB power module baseplates and a discrete device from each PCB based switch to ensure that the temperatures did not increase above 58 ℃. The measured output voltage and current are shown in Fig. 3.17. Also, the efficiency was measured to be 98.2%.

The fabricated PEBB achieved a specific-power and volumetric power density of 27.7 kW/kg and 308.61 W/in3, respectively. The distribution of the weight amongst different components in the designed PEBB is provided in Fig. 3.18. The specific-power estimations

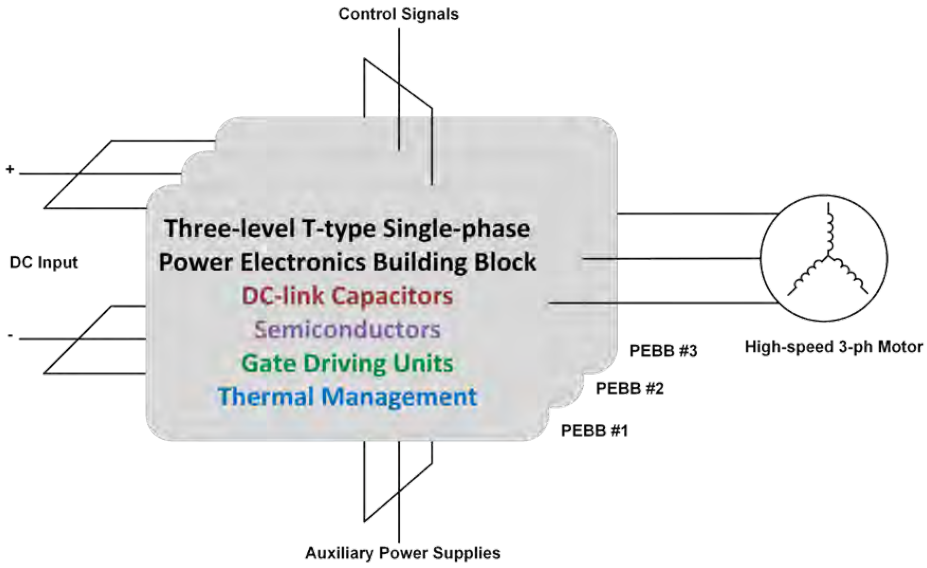


Figure 3.15: Block diagram implementation of three PEBBs for driving a 3-phase motor.

did not include the weight from EMI filters since they were not integrated into the fabricated PEBB. However, presuming the weight of conventional I/O EMI filters at 30% of the active component weight in the PEBB, an estimation of total weight was made. With the inclusion of the weight from EMI filters, a 24.5 kW/kg power density (4.08 kg/PEBB and 12.44 kg/three-phase inverter) will be assured. As a reference, in comparison to a Toyota Camry 2013 drive [30], which has a power density of 17.2 kW/kg, the designed PEBB with EMI filter integration will achieve 40% more specific-power density. However, as a part of the future work, hybrid active EMI filters will be utilized for further weight reduction of I/O EMI filters. The volumetric power density estimations did not include the existing air-cooled heatsink/coldplate integrated into the PEBB. A low profile commercial coldplate will make sure the volumetric power density is not too low compared to the estimated value of 308.61 W/in3, which does not include the heatsink. Also, a non-metallic coldplate that significantly reduces the weight of the system is being developed as part of future work to achieve higher

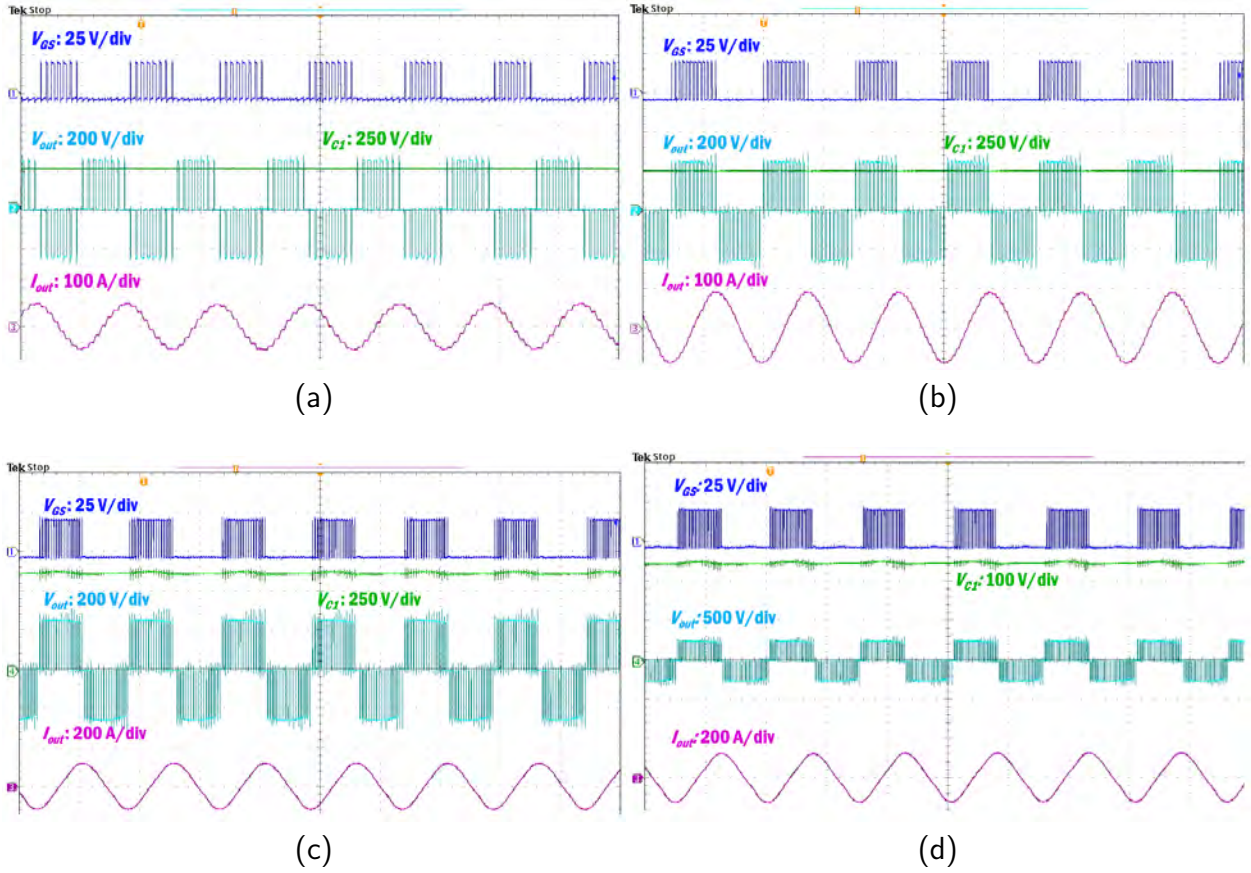


Figure 3.16: Measured output phase voltage and current at fo = 666.667 Hz and switching frequencies: (a) fsw = 10 kHz, Carrier ratio = 15 (b) fsw = 15 kHz, Carrier ratio = 22.5 (c) fsw = 24 kHz, Carrier ratio = 36 (d) fsw = 28 kHz, Carrier ratio = 42.

specific-power density.

3.4 Conclusion

A design methodology for a three-level t-type power electronics building block using a Si-IGBT plus SiC-MOSFET-based hybrid switch was developed. A phase-leg power module with an inherent three-level t-type topology was unavailable, resulting in the use of multiple modules for the PEBB implementation. Moreover, the requirement to use a hybrid switch further exacerbated the implementation. Consequently, the busbar design

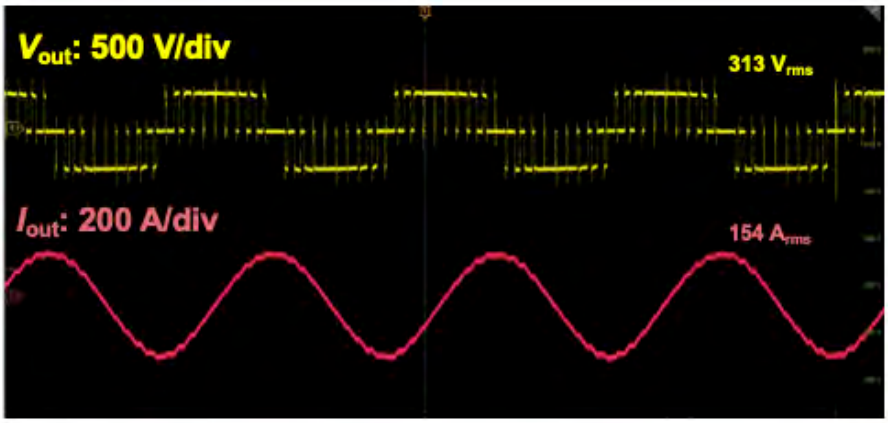


Figure 3.17: Measured output phase voltage and current at the operating conditions in Table III.

for low-inductance and symmetrical commutation loops was not trivial. A low inductance multi-layer laminated busbar was designed with symmetrical current commutation loop inductances. The aluminum busbars and semiconductor and dc-link capacitor selections led to a lightweight PEBB implementation, with a specific-power density of 27.7 kW/kg. Also, the designed PEBB achieved a volumetric power density of 308.61 W/in3. The operation of the PEBB was demonstrated at the 48 kVA. The future work includes testing three PEBBs in a three-phase system implementation with a motor load. Additionally, I/O EMI filters will also be integrated into the PEBB.

3.5 Acknowledgement

This work was supported by the National Science Foundation Engineering Research Center for Power Optimization of Electro-Thermal Systems (POETS) with cooperative agreements EEC-1449548. The authors would like to thank Dr. Lauren Boteler from the United States Army Research Laboratory, Adelphi, MD, for allowing the use of the ARL

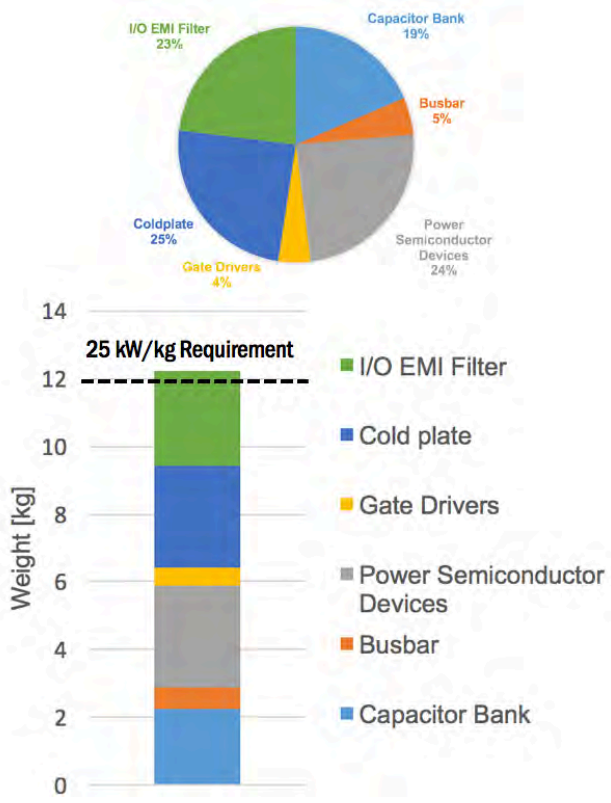


Figure 3.18: The weight distribution within a PEBB and estimated three-phase inverter total weight.

ParaPower program for the analysis. ARL ParaPower can be found at `https://github.com/USArmyResearchLab/ParaPower`

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4 A 1700-V/ 300-A Si-IGBT and SiC-MOSFET Hybrid Switch-based Half-bridge Power Module

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This paper has been accepted and submitted as final paper for IEEE ECCE 2020 conference to be held on October 11-15 in Detroit, MI.

4.1 Introduction

The next generation of high-power, high power-density, high-efficiency power conversion applications, such as traction, shipboards, more-electric aircraft, and locomotive, demands high-current and high-efficiency power modules. High power-density is achievable using higher switching frequencies. On the one hand, silicon (Si) IGBT is usually limited to a switching frequency of 20 kHz, considering the slow switching speed of the IGBT, especially during the turn-off due to the tail current. On the other hand, wide bandgap (WBG) devices such as silicon carbide (SiC) MOSFET attract much attention in these applications because of their capability of fast switching speed, resulting in low loss and possibility for high switching frequencies well above 20 kHz. Presently, the WBG devices are only available in small die sizes. For example, the largest 1.7 kV SiC MOSFET bare die size is 7.35 mm x 4.08 mm with 48 A current rating. Whereas, the largest 1.7 kV Si IGBT bare die is 15.93 mm x 16.88 mm with 225 A current rating. Although multiple SiC devices in parallel can replace a large IGBT, it is still challenging to implement a multichip all-SiC power module. Significant roadblocks to achieving high switching-frequency in all-SiC modules include

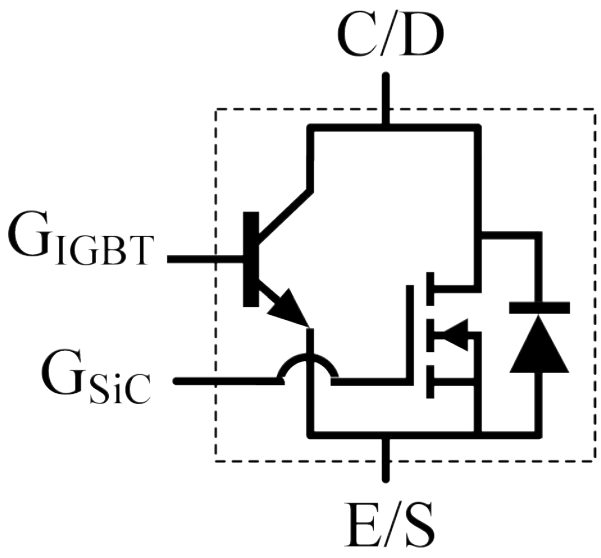

Figure 4.1: A Si-IGBT and SiC-MOSFET hybrid switch.

dynamic current sharing due to inherent differences in the electrical parameters and consequent unequal temperature distribution. Apart from the technical challenges, the cost of SiC modules is another issue for its application. Paralleling a large amount of SiC chips in the module to handle high current will increase the module cost.

A hybrid switch consisting of a large-current rated Si-IGBT in parallel with a small-current rated SiC-MOSFET combines both devices' benefits. The hybrid switch provides excellent light and heavy load conduction performance, lower switching energy compared to IGBT, both at low cost provided the current ratio of Si over SiC is high. In Section 4.2, the concept of hybrid switch is presented. In Section 4.3, the design of the hybrid switch-based power module is described in detail. The fabrication process of the power module is presented in Section 4.4. A prototype is fabricated and the test results are discussed in Section 4.5.

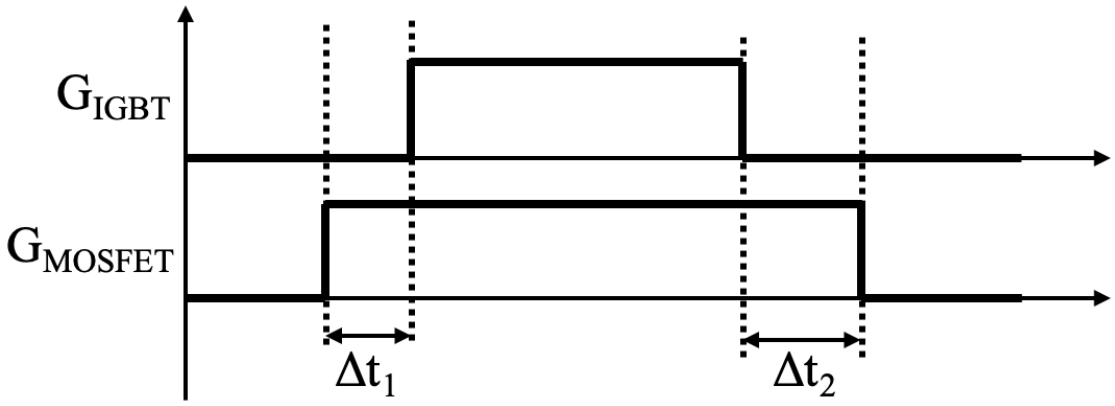

Figure 4.2: The staggered gate signals for the constituent Si-IGBT and the SiC-MOSFET of the hybrid switch.

Table 4.1: Devices used in the proposed half-bridge power module.

Device	PN#	MFG.	Voltage (V)	DC Current (A) @ 100 °C	$V_{CE(sat)}$ (V) $R_{DS(ON)}$ (Ω) V_F (V)	$T_{j(max)}$ (°C)	Qty/ switch-cell (Qty/module)
Si-IGBT	5SMY 86M1730	ABB	1700	150	2.75 V	150	2 (4)
SiC-MOSFET	CPM2-1700-0045B	CREE	1700	48	45 mΩ	175	1 (2)
SiC-SBD	CPW5-1700-Z050B	CREE	1700	50	2.8 V	175	6 (12)

4.2 Si-igbt and SiC-mosfet hybrid switch

The concept and comprehensive evaluation of a Si-IGBT and SiC-MOSFET-based hybrid switch was demonstrated in an earlier study by the authors [1]. The hybrid switch solution combines the operational benefits from both Si-IGBT and SiC-MOSFET [2–4]. The schematic of a hybrid switch is shown in Fig. 4.1. The Si-IGBT lends high-current handling capabilities, while the SiC MOSFET allows for light-load efficiency improvements, fast switching speeds, and high operating junction temperature. The improved switching performance is possible with optimized staggered gate signal pulses to the respective devices in the hybrid switch [1], as shown in Fig. 4.2. In addition to the electrical performance, the hybrid switch is a cost-effective solution. A cost analysis performed on the commercial 1.2 kV Si-IGBT and SiC-MOSFET packages, indicated up to 75% reduction in cost can

be achieved using the hybrid switch with 4-over-1 or 6-over-1 Si-over-SiC current ratio [1]. The hybrid switch-based converter implementations demonstrated using discrete commercial off-the-shelf (COTS) Si and SiC packages have some limitations to fully realize the potential of the hybrid switch [5]. The dynamic current sharing due the parasitic interconnection inductance imbalance, resulting from the external interconnection PCB traces or busbars and the internal package inductance of discrete Si and SiC packages, increases the losses [1]. Moreover, the thermal impedance of the material stack-up in COTS SiC discrete packages is not enough to dissipate the heat power loss profile of SiC when used in hybrid switch and keep the junction temperature under 175 °C. Hence, a co-packaged hybrid switch to mitigate these issues is needed and the design and fabrication of such a module is the key contribution of this paper.

4.3 Power module design

This section discusses the proposed design of the power module with each subsection detailing various elements of the design. A constraint was placed on the module design to ensure enabling of the use of standard power module manufacturing processes used in high volume manufacturing. However, there was a flexibility to use novel materials whenever possible.

4.3.1 Die Selections

A 1.7-kV and 300-A rated Si-IGBT and SiC-MOSFET-based half-bridge power module is proposed. The half-bridge circuit topology consists of two switch positions as highlighted in Fig. 4.3. A 1.7-kV and 150-A Si-IGBT die, the highest current rated die available

for purchase at the time from ABB was selected. Hence, two Si-IGBT dies were paralleled for each switch position. For the parallel connected SiC-MOSFET, one 1.7-kV and 48-A die from CREE was selected for each switch position. Consequently, a Si over SiC current ratio of six was achieved. The SiC-MOSFET die would be insufficient to handle a reverse current conduction of 300 A, hence, six 50-A SiC Schottky barrier diodes (SBD) from CREE were selected per switch position. Table 4.1 summarizes the above die selections for the module with important parameters/specifications. It is important to note that the current rating in the die datasheet is a maximum DC current rating assuming a junction to case thermal resistance of less than or equal to 0.4 K/W as per IEC 60747. The CAD rendering of the module is shown in Fig. 2.

4.3.2 Layout

A direct bonded copper (DBC) or active metal brazed (AMB) ceramic substrate is proposed for the module. The top copper of the substrate is patterned to make islands representing the DC+, DC-, and AC node of the half bridge topology. The dies are placed on the substrate in the power module, based on the switching cell concept [6]. Each half of the module was dedicated for one switching cell to optimize the switching power loop for low inductance. The left and right half of the module in Fig. 4.4 represents the P- and N-cell, respectively. This layout yielded symmetrical P- and N- cells with a power loop inductance of 12.38 nH. Moreover, the design offers excellent dynamic current sharing among the dies. That was possible due to an interconnect inductance of less than 0.34 nH. The dies were densely populated, edge-to-edge spacing of, on the DBC substrate to reduce the area of the metallization pattern on the DBC for minimizing the common-mode capacitance to ground

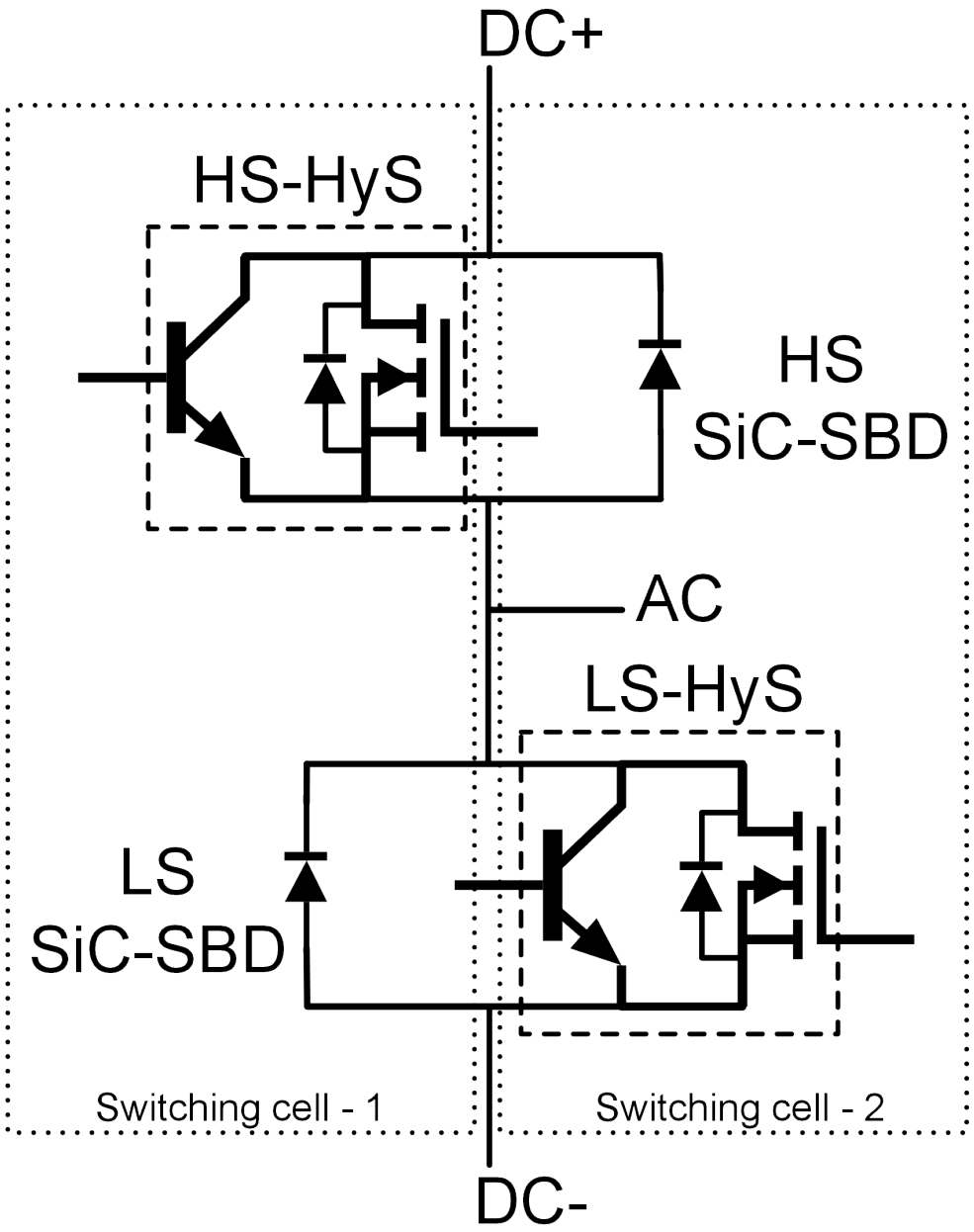

Figure 4.3: The half-bridge topology.

and enable good EMI performance. The extracted parasitic loop inductance and capacitance from ANSYS Electronics Desktop Q3D at 1 MHz (see Fig. 4.5) are listed in Table 4.2 and 4.3, respectively.

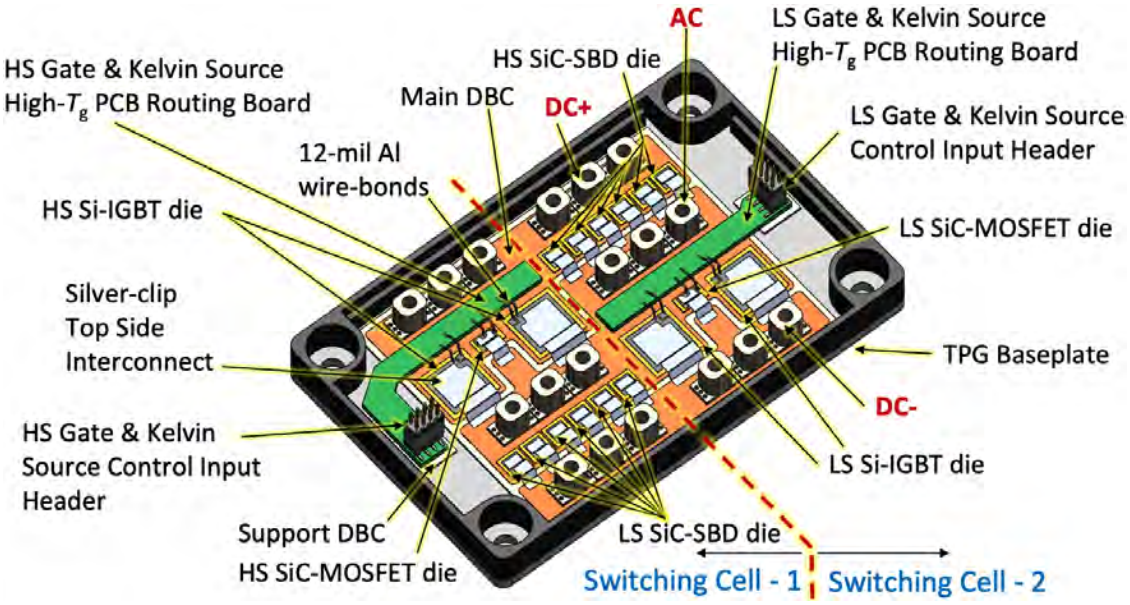

Figure 4.4: The CAD render of the proposed Si-IGBT and SiC-MOSFET-based hybrid switch power module.

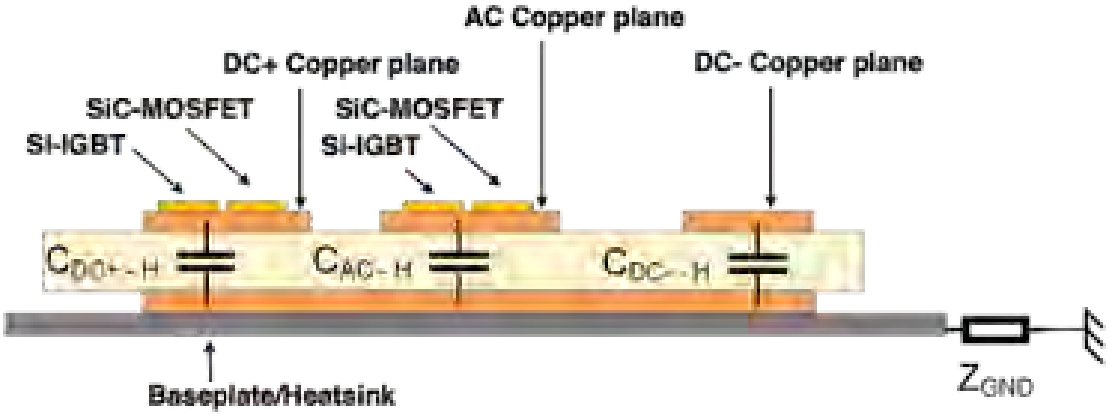

Figure 4.5: Parasitic capacitances in the power module.

4.3.3 Internal Gate and Kelvin Source Routing

The module provides Kelvin connection for the emitter and source of dies. This eliminates the negative/positive feedback effects of the common-source inductance. Two internal gate and Kelvin source routing printed circuit boards, one each for the high side and the low side were placed next to the dies as shown in Fig. 4.4. The placement of the PCBs relative

Table 4.2: Extracted stray inductance of the commutation power loops

Stray Inductance	Value at 1 MHz (nH)
L_{sc1}	12.34
L_{sc2}	12.30

Table 4.3: Extracted parasitic capacitance

Capacitive coupling	Value at 1 MHz (pF)
C_{DC+}	262.5
C_{AC}	305.75
C_{DC-}	139.6

to the dies provided a low-inductance gate-source signal loop. The PCBs are placed on the top copper without breaking the commutation power loop for switching cells. The power loop inductance increases due to this design choice, however, the trade-off is acceptable. The PCBs were fabricated from an FR-4 material with a high glass transition temperature (T_g), 180 °C, to sustain the high processing and operating temperatures. Moreover, the pads on PCBs had an electroless nickel/immersion gold (ENIG) surface finish to enable gate and KS wire bonding. The use of these PCB-based gate routing boards enables the layout to achieve the previously mentioned excellent dynamic current sharing.

4.3.4 Power Terminals

The power terminals are designed like terminal blocks, as shown in Fig. 4.6 and are soldered on the DBC substrate. The holes at the feet of the terminal block serve as a solder catch during the solder liquefaction stage. The solder will climb up inside them and work as rivets to provide strong mechanical contact. This is especially useful as the surface area is small and the terminals can snap off during external termination. The terminals are milled out of copper to provide the required high ampacity of the module.

Figure 4.6: The picture of a terminal block. [Source: Photo by Author]

4.3.5 Topside Interconnects

Wire bonds are conventionally used in power electronics module for top side interconnect. This is because of the maturity of the technology for a high volume processing. However, there is a limit to the number of wire bonds on a die, particularly SiC die, which is smaller is size. With increasing current density the wire bonds became the bottle neck for high current density. Moreover, they are the first element of the package to fail in the reliability testing [7]. Wire bondless approaches from academia tend to take a drastic change in the module architecture deeming it far fetched for module makers. The proposed module incorporates novel, wire bond-less, low-parasitic, and high-reliability topside power interconnects. They are ideal for high current applications since they offer low resistance and inductance compared to the conventional aluminum wire bonds [8]. They are beneficial for Si-IGBT dies as the on voltage of the devices may reduce by 4.8% [9]. They have shown a reduction in the thermal impedance by 22-25% for the die and a consequent reduction in the junction temperature by 27% and a uniform temperature distribution on the chip [10]. They also have high short-circuit withstand capability. Most importantly, they have proven

improvement in the power cycling reliability leading to higher life cycle by a factor of 2 [10] to 7 [9]. The ideal thickness of the silver clips is 0.1-0.6 mm. The module employs three unique designs for the silver clip each corresponding to the Si-IGBT, SiC-MOSFET, and SiC-SBD as shown in Fig. 4.7. Each clip has a thickness of 0.7 mm. This thickness is more than the ideal choice of thickness, however, this is the minimum thickness as per manufacturabilty guidelines from the supplier. Silver is a better electrical and thermal conductor compared to copper. Silver has a higher CTE, 19 ppm/K, compared to that of copper, 16 ppm/K, however, it has a better match with the topside metallization of aluminum or silver. The clip should be attached to the device top side with a high thermal conductivity silver sintering paste.

The metallization on topside pads of the dies is aluminum for enabling wire bonding, a matured topside interconnection process for IGBT power semiconductor packaging. However, aluminum neither solderable nor sinterable. Hence, for attaching silver clip to topside, the source pads should have a Ni/Ag metallization similar to the backside of the dies. Since module manufacturer do not have the access to such dies, a re-metallization to Ni/Ag, Ni, or Au is required for long-term reliability. There are literature which describe and demonstrate the procedure for re-metallizing a SiC die in depth [11]. Major reliability concerns include poor adhesion of silver paste on an aluminum surface and the galvanic corrosion due to the contact of dissimilar metals in the presence of electrolyte. In this case, the aluminum on the topside of the die and the silver from the clip and attachment paste will lead to galvanic corrosion. The aluminum surface, which is more anodic compared to silver, will corrode. The re-metallization will significantly reduce the issue of galvanic corrosion. However, in the development of prototype, the dies were not re-metallized and silver epoxy was used for the

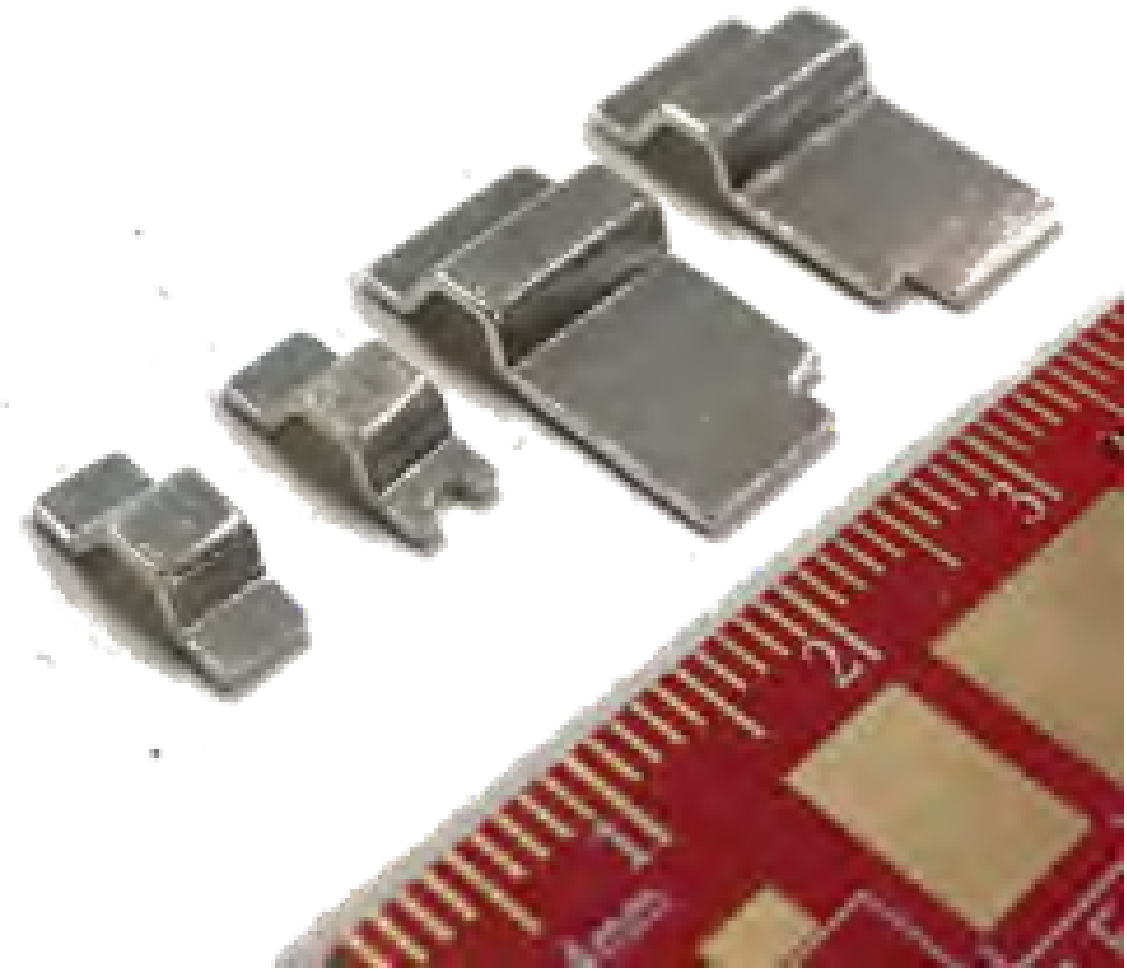

Figure 4.7: The pictures of the molded silver clip interconnects. [Source: Photo by Author]

attachment. The use of silver epoxy allowed for the simplicity needed to demonstrate the proof-of-concept.

The use of silver clips for gate (G) and Kelvin source (KS) interconnection from the die topside to the pads on the internal G/KS routing board is possible yet unnecessary. Hence, 12-mil wire bonds are used for the purpose of these control interconnects.

4.3.6 Materials and Heat Transfer

A 6-over-1 ratio of Si-over-SiC can be achieved with a low thermal impedance and near isolated thermal path to avoid thermal coupling between the hotter SiC-MOSFET and relatively cooler Si-IGBT in the hybrid switch dies [1]. Also, as mentioned previously, the goal was to develop a module with standard packaging techniques. A high thermal conductivity aluminum nitride (AlN) ceramic-based metallized substrate, DBC or AMB, was proposed. It consists of 0.3-mm thick copper on either side of a 0.64-mm thick AlN. The metal was plated with silver (Ag) for compatibility and high-strength bond line while using silver containing pastes for all attachments. For die, terminal and substrate attachment, a high thermal conductivity silver sintering paste is proposed. The bond line thickness (BLT) for the die-attach, substrate-attach, and terminal-attach was set to be 75 μm each, considering the in-house processing capabilities.

Traditionally, a nickel-plated baseplate was used for commercial power module. Copper offers exceptional heat spreading due to its thermal conductivity. On the other hand, the industry is transitioning to a nickel-plated metal matrix composite, aluminum silicon carbide (AlSiC), for baseplate material. AlSiC has a better CTE match with the substrate. The reduced CTE mismatch induces lower thermo-mechanical stress. AlSiC, as compared to copper, is lighter, about one-third of copper, leading to a lightweight module. Moreover, AlSiC is a cast material, thus, allowing to build in a domed shape to counteract the concave deformation after the high-temperature attachment processes in the fabrication process. These benefits of AiSiC are trade-off for its limited thermal conductivity with a maximum reported value of 200 W/mK, about 50% that of copper. Overall, AlSiC provides high re-

Table 4.4: Thermal Conductivity of constituent elements in the TPG-encapsulated metal baseplate.

Element	k_x (W/mK)	k_y (W/mK)	k_z (W/mK)
Copper base	400	400	400
TPG tile	10	1500	1500
Copper lid	400	400	400

liability and low-weight module with increased thermal resistance. The thermal spreading, however, causes thermal coupling and increases the temperature of a particular die in a multi-chip power module. The die with highest temperature is usually the one that has dies on either sides. The use of a thermal pyrolytic graphite (TPG)-encapsulated metal baseplate, as shown in Fig. 4.9, is proposed over a conventional copper material.

The orthotropic thermal properties of the TPG tile that is embedded inside the metal baseplate nearly eliminates the thermal coupling between adjacent dies [12]. For reference, the thermal conductivities of copper, which is isotropic, and TPG are listed in Table 4.4. AlSiC would be an ideal choice for the reasons mentioned previously. However, WCu and MoCu would also be good alternatives. Due to costs and demonstration of the key idea of using TPG for restricted heat spreading, Cu was chosen for the metal. The proposed TPG-embedded Cu base plate has a thickness of 3.17 mm. The base plate consists of three parts, the base, TPG inserts, and lids. The base, which has pockets for two TPG inserts, is made of copper. TPG inserts, one for each switching cell, were positioned underneath them. Copper lids then encapsulate the TPG inserts in the Cu base. The weight of the metal-encapsulated TPG baseplate for the module design is 169 grams, 28% less than that of a copper baseplate (233 grams). The baseplate was manufactured by Momentive, who specializes in TPG based products. The manufacturing process is proprietary and its description beyond the scope of this work.

A steady-state heat tranfer finite element analysis (FEA) was performed on the proposed stack-up (see Fig. 4.8) for determining the maximum junction temperature in the module. SOLIDWORKS Simulation was used to perform finite element method (FEM) simulations. The BLTs were not modelled in the CAD, hence, a consequent virtual distributed thermal resistance was used at interfaces in the FEM simulation. A convective boundary condition was used at the backside of the base plate, where the effect of liquid-cooling and the thermal interface material between the base plate and cold plate was emulated with an effective convective heat transfer coefficient of 6000 W/m^2K. All other open surfaces were assumed to be adiabatic, as the heat transfer from them negligible. For calculating power losses, two-level converter operation was considered with a DC-link voltage of 1000 V, load current of 300 A, output power factor of 0.8, fundamental output frequency of 50 Hz, and a switching frequency of 20 kHz. The results from FEM at the operating conditions when using a copper baseplate with wire bond top side interconnect, TPG baseplate with wire bond top side interconnect, and TPG baseplate with silver clip interconnects is shown in Fig. 4.11, Fig. 4.12, and Fig. 4.13, respectively. The junction temperature for SiC-MOSFET was reduces by restricted under 175 °C. There is a reduction of more than 16% in the maximum junction temperature of the SiC die in the module when using a TPG-embedded base plate with silver clips when compared with the conventional wire bonded module with copper baseplate.

4.4 Fabrication Process

This section discusses the fabrication process of the power module with pictures during each process step illustrated in Fig. 4.14. As highlighted in section 4.3, the main

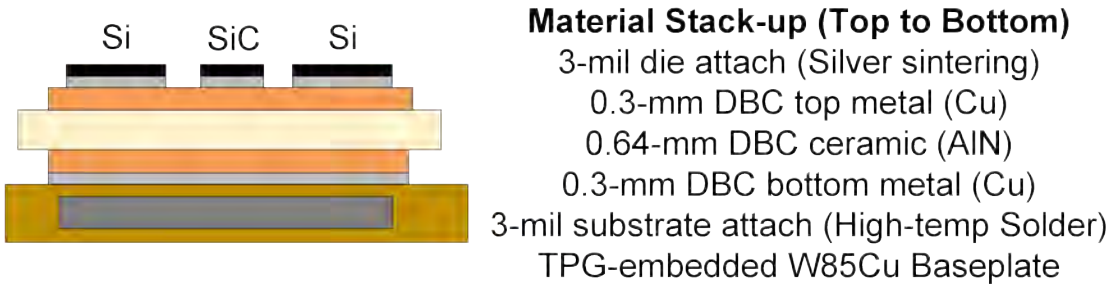

Figure 4.8: The heat transfer stack within the power module.

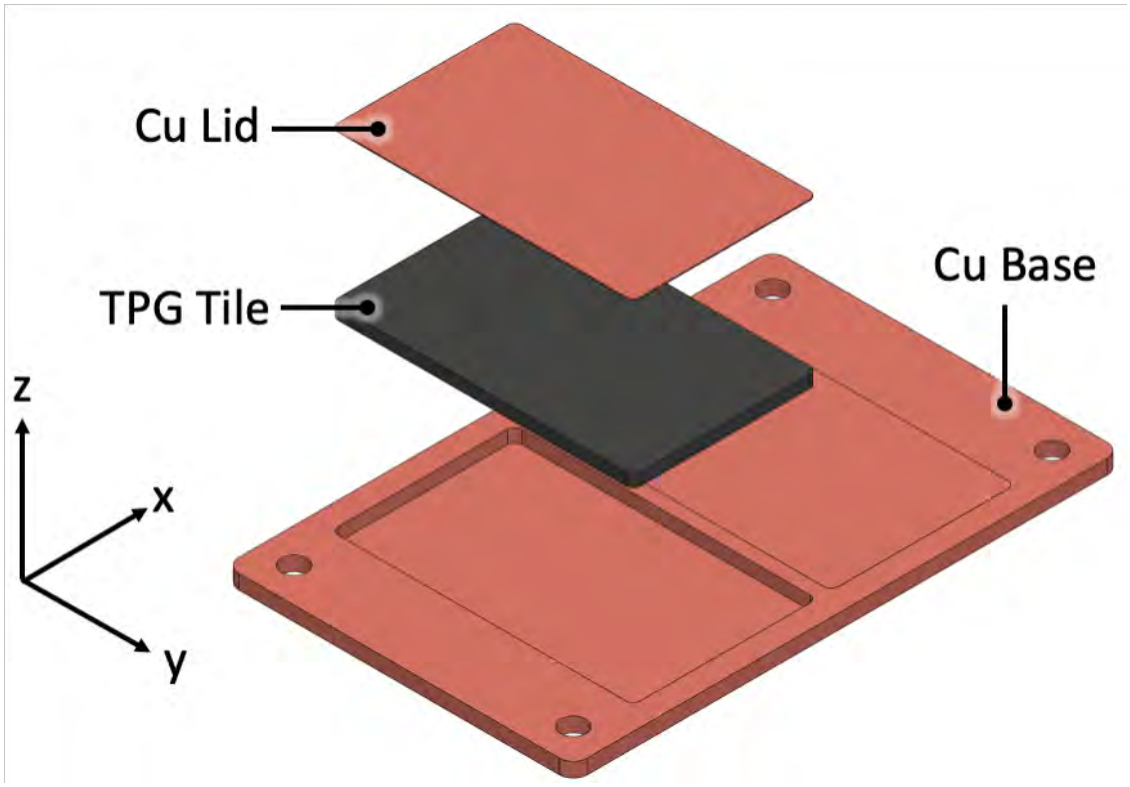

Figure 4.9: An exploded view of the TPG-encapsulated metal baseplate

goal was to use standard power module manufacturing processes to enable high volume manufacturing. The description of each step is as follows:

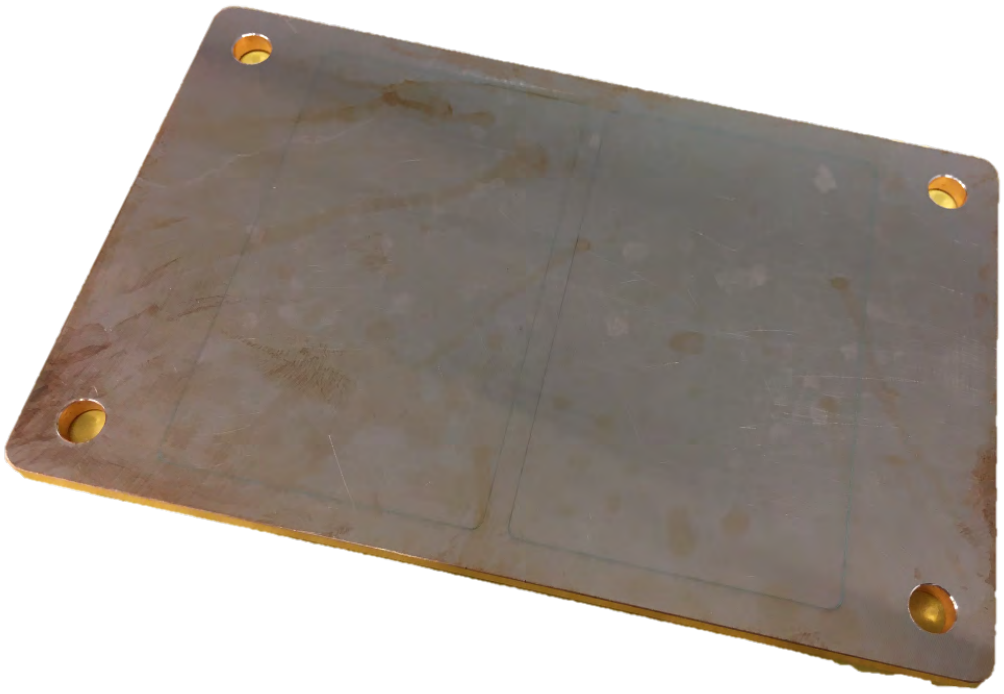

Figure 4.10: A picture of the TPG-encapsulated metal baseplate. [Source: Photo by Author.]

4.4.1 Step-1, -2, and -3:

A fixture milled out of graphite is placed bottom-up with pockets for the main substrate and baseplate accessible. The main substrate is placed first in the fixture's lower pocket as seen in Fig. 4.14. Solder/ epoxy is dispensed/ stencil-printed on the substrate's back copper. This solder/ epoxy is meant for substrate to baseplate attachment. Next, the baseplate is placed in the fixture's upper pocket as seen in Fig. 4.14.

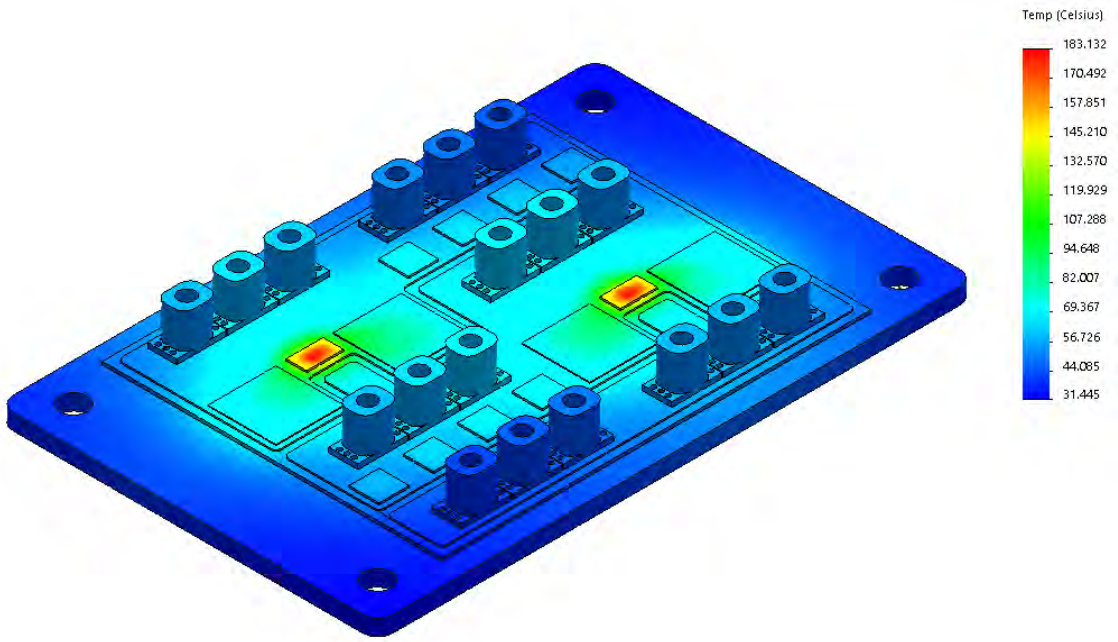

Figure 4.11: Surface temperature plot from the steady-state heat transfer finite element method simulation for the case using wire bond interconnects and copper baseplate.

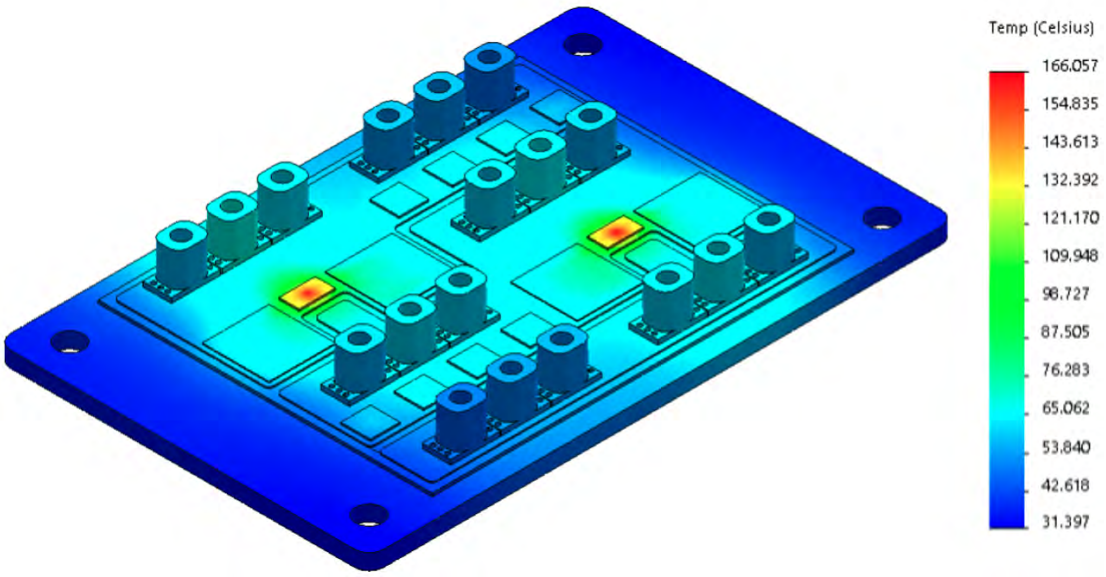

Figure 4.12: Surface temperature plot from the steady-state heat transfer finite element method simulation for the case using TPG-encapsulated metal baseplate.

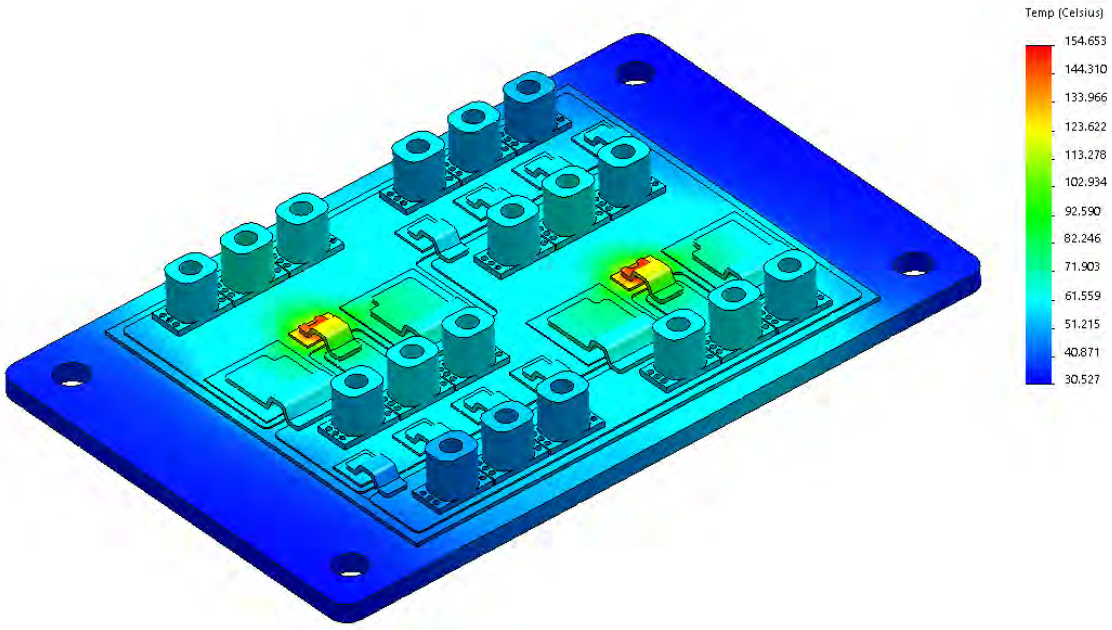

Figure 4.13: Surface temperature plot from the steady-state heat transfer finite element method simulation for the case using TPG-encapsulated metal baseplate and silver clips for top side interconnection.

4.4.2 Step-4, -5, and -6

The assembly consisting of the fixture, main substrate, and the baseplate are flipped up side down. The pockets in the fixture designed for dies and G/KS boards are now accessible. Solder/ epoxy is dispensed on the main substrate's top copper and baseplate through the fixture's pockets for all dies and support substrates. This solder/ epoxy is meant for the die attach and support substrate attach. Next, support substrates and dies are hand placed in the respective fixture pockets using a vacuum pick-up. The solder/ epoxy is further dispensed on the top copper of support substrates and the main substrate. G/KS PCBs are placed in the respective fixture pocket as seen in Fig. 4.14. The assembly consisting of the graphite fixture, baseplate, main substrate, support substrates, dies, and G/ KS PCBs are placed in a vacuum oven for the reflow/ curing of the solder/ epoxy.

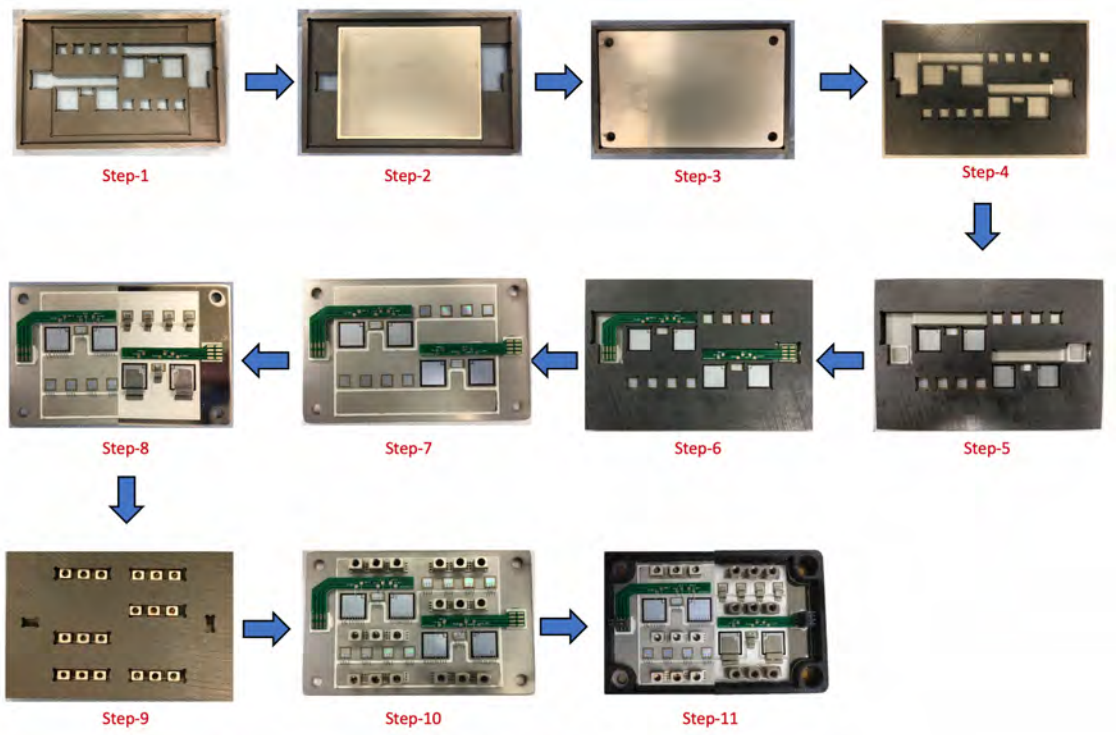

Figure 4.14: The fabrication process for the proposed module. [Source: Photo by Author]

4.4.3 Step-7 and -8

The fixture is then removed from the assembly and the remaining is ready for the next step of top side interconnection. In this step, the top side interconnection is made from source/ anode pads of IGBT/ MOSFET dies and SBD dies, respectively. Either wirebonds or silver clip can be used at this point. 12-mil wire bonds were used in an earlier version. For silver clip attachment, the silver paste is printed on the silver clips in the area that makes contact with the die. The silver clips are then placed on top of the dies using a vacuum pickup. The module is then placed in the oven for curing the silver paste. Next, the G/ KS wire bonds are made from the IGBT/ MOSFET dies to the G/ KS PCBs.

4.4.4 Step-9:

A separate fixture milled from graphite is used for the attachment of the power terminals to the main substrate. First, the fixture is placed on the assembly from step-9 and solder/ epoxy is dispensed through the fixture's pockets designed for power terminals. Next, the power terminals are hand-placed in the fixture pockets using tweezers. The entire assembly is then placed in the vacuum oven for second round of reflow/ curing to complete the power terminal to substrate attachment. This step could be performed during step-6 along with the dies and G/ KS PCBs to reduce the total steps in the assembly. However, the available manual wire bonder, which is used in step-8 for G and KS connections, has its bonder head held with a protruding arm that would interfere with the power terminals had they been attached earlier. Of course, this will not be the case for latest wire bonders used by module manufacturers.

4.4.5 Step-10 and -11

The fixture is removed from the assembly and the remaining is ready for the next step. In this step, first, G/ KS control headers are soldered on G/ KS PCBs. Next, the housing sidewall is attached to the baseplate using a silicone RTV sealant adhesive. ABS material was used to 3D-print using stereo lithography and a 15 um resolution. The material has enough heat deflection temperature and glass transition temperature to sustain the curing of adhesive and the following encapsulant curing. After curing the adhesive, the encapsulant in poured in the housing. For encapsulant, Wacker Semicosil 915HT, a high dielectric strength and low viscosity silicone gel, was used. The silicone gel is a two-part material with a 10:1 mix

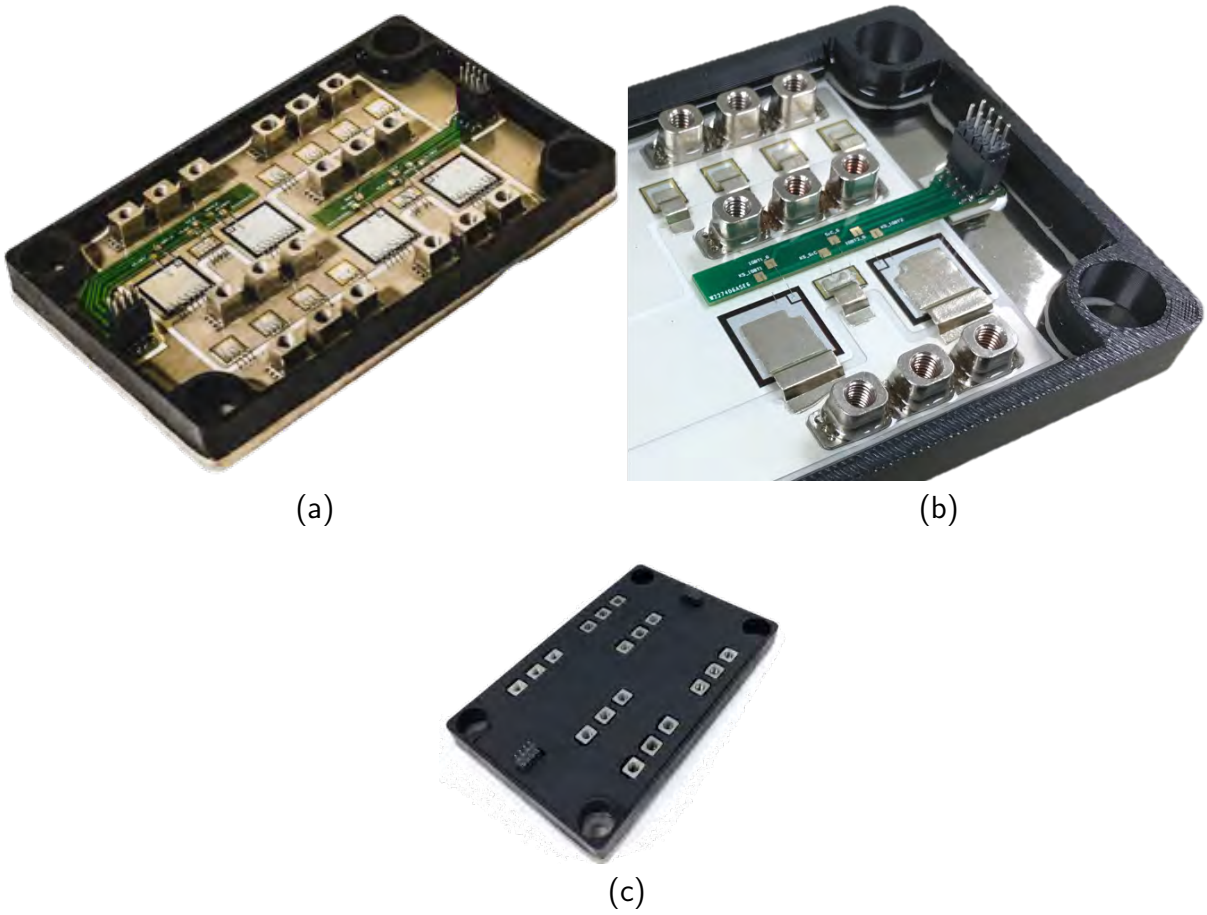

Figure 4.15: (a) The fabricated power module with wire bond implementation and without the lid. (b) The fabricated power module with the silver clip implementation and without lid. (c) The fabricated power module with the lid. [Source: Photo by Author]

ratio by volume. SEMICOSIL 915HT and ELASTOSIL CAT PT, a catalyst, were mixed in an automated stirrer prior to dispensing in the housing. After dispensing, the assembly was placed in a vacuum oven and 25 in. Hg vacuum was used to pull the bubbles out from the gel. Nitrogen was purged to break the remaining bubbles on the top surface. Three rounds of vacuum and purging nitrogen were carried out. After the fourth round of vacuum, the gel was cured at 100 °C for 30 minutes. At this point, the housing lid is placed on the sidewall to complete the module assembly.

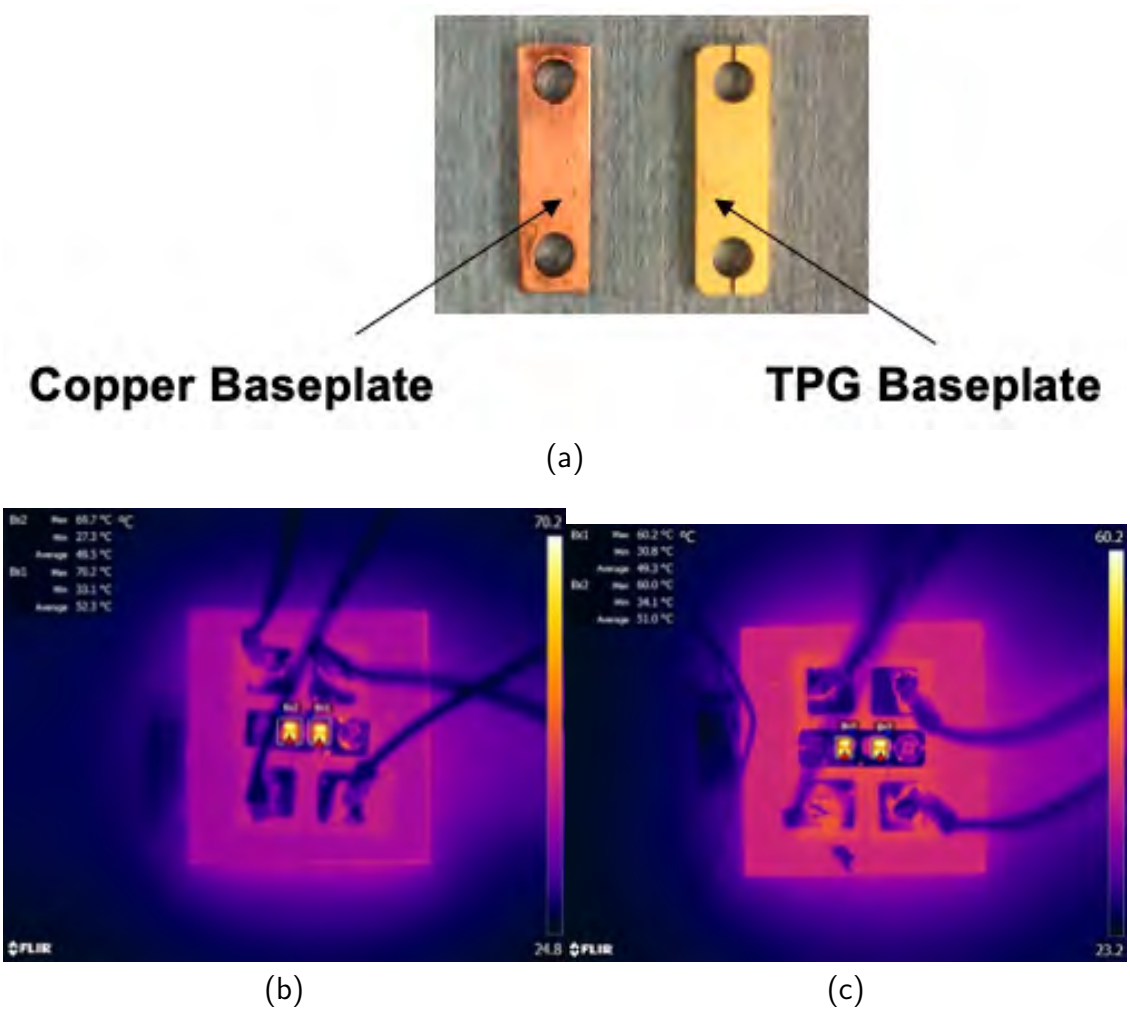

Figure 4.16: (a) The copper and metal encapsulated TPG baseplate sample used for evaluation. (b) Thermal image for DUT with copper baseplate. (c) Thermal image for DUT with TPG baseplate. [Source: Photo by Author]

4.5 Results

The benefit of TPG baseplate was evaluated using a small-scale sample while the original sample was in manufacturing. As shown in Fig. 4.16a, a TPG baseplate with one TPG tile and a copper baseplate of similar dimension were used. Two resistor dies were attached on both samples with a 1.5 mm minimum spacing. The samples were attached on heatsinks. With equal power dissipation in both dies the junction temperature was recorded

for each die across in both samples for the same cooling conditions in both simulation and experiment. The peak junction temperature in the sample with TPG baseplate reduced by 9.5 °C compared to its counterpart, in line with the 9 °C drop observed in simulation. The difference in the simulation and experiment result is derived from the slight inaccuracy in achieving 1.5 mm spacing and the calculations of effective heat transfer coefficient for simulation.

The fabricated module included alumina DBC, Cu baseplate and wire-bonded power interconnects is shown in Fig. 4.15a and 4.15c. Moreover, only 4 diodes per switch position were utilized to save cost and circumvent the lack of tight tolerances on the soldering fixtures available at the time. Double pulse test (DPT) was performed on the power module in a clamped inductive load (CIL) setup. The SiC device was switched with a gate to Kelvin source voltage, V_{gs}, of +20 V/ -5 V while the Si-IGBT was switched with 15/ -9 V. The module was tested up to 1000 V and 300 A. A Tektronix MSO58 was used for recording the switching waveforms. A 1 GHz passive probe and 200 MHz differential probe, was used to record the V_{gs} and V_{ds}, respectively. The adaptor board connected to the module consists of the current viewing resistors which come in series with the bottom dies. A 1 GHz passive probe was used to record the voltage across the current viewing resistors and was converted to current using on-scope processing. The load current was recorded using a 30 MHz Rogowski coil. The switching waveforms from the DPT are shown in Fig. 4.17. The overshoot voltage at the power terminals is approximately less than 100 V.

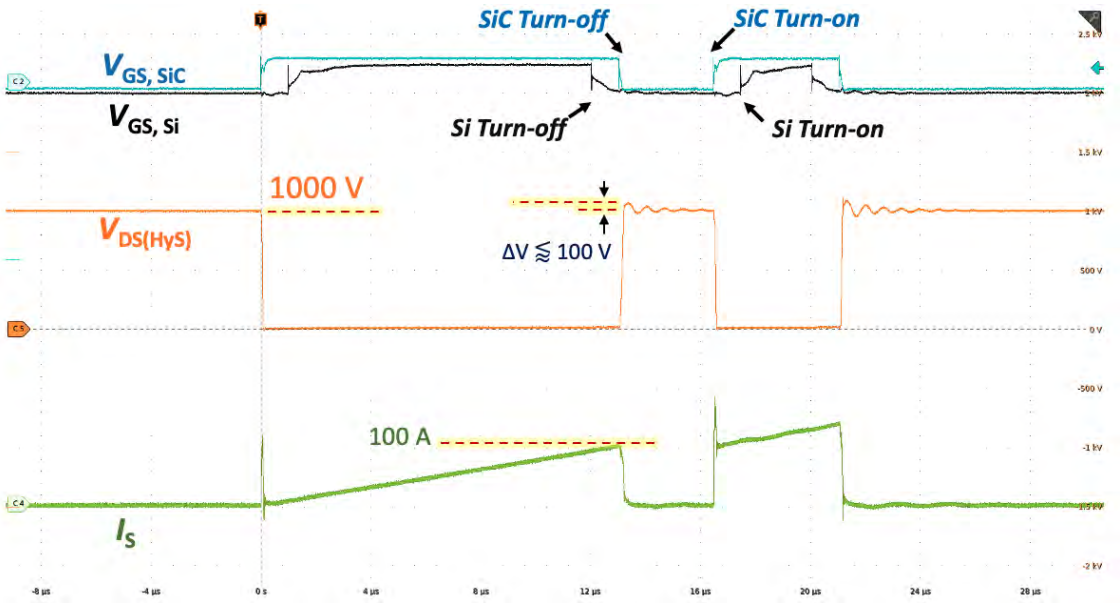

Figure 4.17: The switching waveforms for the clamped inductive load testing.

4.6 Conclusion

A high power-density 1700-V and 300-A Si-IGBT and SiC-MOSFET hybrid switch-based half-bridge power module is presented. The module offered a 6-over-1 Si over SiC current ratio in a low inductance (12.34 nH) layout. The use of a custom-designed metal-encapsulated TPG baseplate and silver clips top-side interconnects in the module offered low thermal impedance and near isolated thermal path for the SiC MOSFET to operate at higher temperature compared to the Si-IGBT. The module operation was demonstrated in a clamped inductive load testing.

Acknowledgment

This work was supported by the National Science Foundation Engineering Research Center for Power Optimization of Electro-Thermal Systems (POETS) with cooperative

agreements EEC-1449548. The authors would like to acknowledge use of the University of Arkansas High Density Electronics Center (HiDEC) in the completion of the work presented herein. The authors would also like to acknowledge the assistance of Mr. Tom Cannon, Ms. Kaoru Porter, Mr. Errol Porter, and Late. Mr. Clint Hardee at HiDEC in the completion of the work presented herein.

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5 15 kV Power Module Packaging

5.1 Introduction

The silicon-carbide (SiC) semiconductor technology enables power switching devices with high blocking-voltage, potentially above 15 kV, with a 10-kV SiC MOSFET already reported [1]. Conventional low-voltage power module DBC substrates are scalable for high-voltage applications. A 1-mm aluminum nitride ceramic (17 kV/mm breakdown strength), which is the thickest commercially available substrate, is in use for 6.5 kV power module designs [2]. At further higher voltages, however, the issue of e-field concentration at the triple-points (DBC metallization, encapsulant and DBC ceramic) leads to partial discharge and consequent breakdown. The investigation of partial discharge phenomenon in a high-voltage IGBT module is reported in literature [3–5]. Some solutions to these problems include electric-field redistribution using field grading materials [4, 6–11], protruding ceramics [12], field plates of top of a DBC [13], and stacking DBCs [14]. Also, these triple points can be removed altogether by eliminating the conventional DBC substrate as demonstrated in [15], however, it comes with challenges for high-volume manufacturing. Among all solutions, stacking substrate provides maximum scalability with the voltage rating and can be used for >15 kV devices. Moreover, the stacked substrate allows the use of legacy power module fabrication processes such as wire-bonding, encapsulation, and die and substrate attach.

In this work, a stacked DBC cavitied substrate, as shown in Fig. 5.2, which consists of a stack of multiple DBCs with the top-surface metallization pattern replicated on each inter-layer and the bottom-surface metallization. This creates a series-connected multi-

layer capacitor under the DC+, DC-, and AC top-surface metallization. The name, stacked DBC cavitied substrate, is derived from the cavities within the stacked substrate. These cavities are a consequence of the proposed approach. The can be used for integrated cooling as discussed in a further section. Most importantly, the multi-layer capacitors, with the DBC ceramic acts as a dielectric, equally distribute the high-voltage of the top-surface metallization across each ceramic under it. The voltage distribution enables field grading and consequent minimization of the electric fields at the critical triple-point and within the bulk of ceramic.

The considerations for HV SiC packaging include the following:

- High voltage isolation to ground: The datasheet breakdown strength of standard ceramics available in DBC are 20 kV/mm. However, with operating voltages approaching 15 kV the maximum off-the-shelf thickness of 1 mm may not be sufficient. Moreover, the substrates need to undergo isolation tests as per IEC standard, where the test voltage is more than the operating voltage.

- Electric field (E-field) mitigation at triple points: The electric field intensification at the triple points lead to partial discharge, which over time will lead to a complete breakdown of the insulation material in the module. The partial discharge test profile is shown in Fig. 5.1b.

- Creepage and clearance distances: These distances specified in standards must be ensured for reliable operation of the power module.

- Low parasitic inductances (power-loop and gate-loop): Similar to a low voltage module, the fast switching speeds will result in the voltage overshoot during the turn-off

transition stress the device. Hence, the parasitic inductance needs to be kept low.

- Low CM parasitic capacitance: The parasitic CM capacitances in the module provide paths for common-mode currents to flow to ground, increasing the EMI issues. The fast switching high voltage SiC devices, generate high dv/dt. This further exacerbates the displacement current, Cdv/dt, in the modules in comparison to the fast switching low-voltage SiC modules.

- High heat flux removal: The reduction of module footprint or power density is the obvious first step module designers take in order to achieve lower parasitic inductances and CM capacitances. The higher power density design puts stringent requirement on the heat flux removal. Moreover, the approach proposed in this work will degrade the junction-to-case thermal resistance compared to a standard power module, unless steps are taken to offset them.

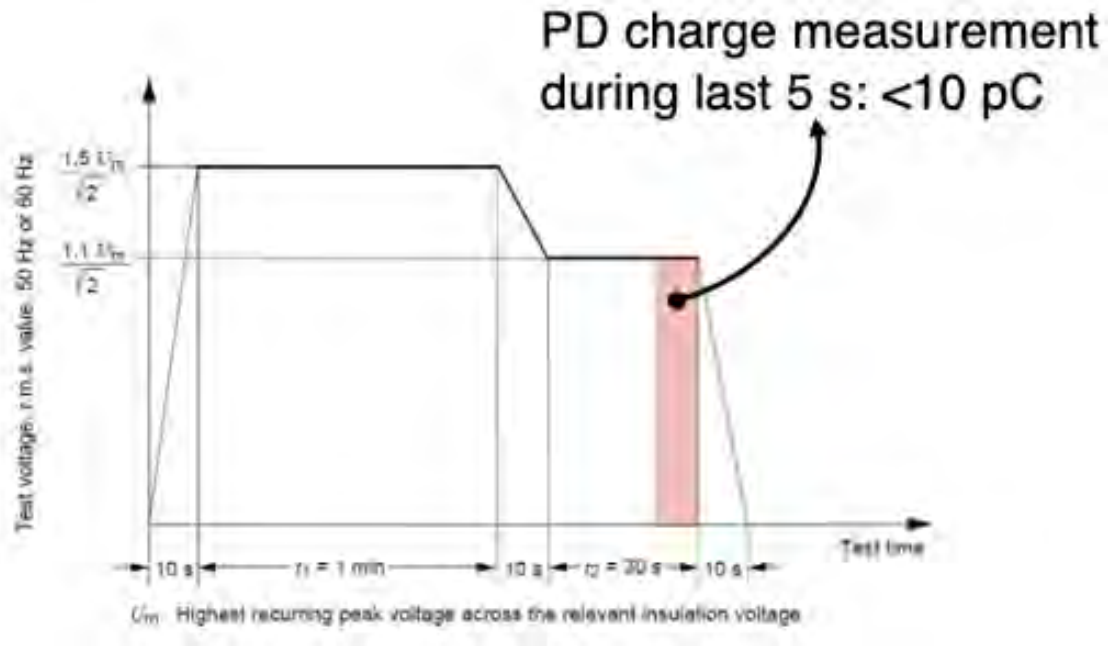
- Minimize thermo-mechanical stresses: Long term operation of the high voltage power modules is critical considering the intended applications.

- Design for manufacturability (DfM): Use of standard power module manufacturing process allows for shortening the time-to-market.

5.2 Proposed Stacked DBC Cavitied Substrate

The mitigatation of E-field at the critical triple points using stacked substrates was introduced by [14]. However, the stacking in [14] was proposed for a single-switch module. The internal metal layer in a two-layer stacked DBC used for a half-bridge power module,

(a)



(b)

Figure 5.1: (a) The test schematic for insulation and partial discharge testing of the designed module. (b) The test waveform for partial discharge testing of the power module as per IEC 61287 standard.

spreads under the top surface patterns as shown in Fig. 5.3b. This leads to an electric potential less than $V_{DC}/2$ on the middle metal layer when left floating. Hence, an increase in the e-field in the bulk of the lower ceramic was observed and the floating layer was clamped to a $V_{DC}/2$ potential from the mid-point of two series-connected MLCC decoupling capacitors [16] to mitigate the E-field intensification in the bulk of ceramic, as shown in Fig. 5.3c. This required the use of interconnection vias within the DBC, increasing the complexity

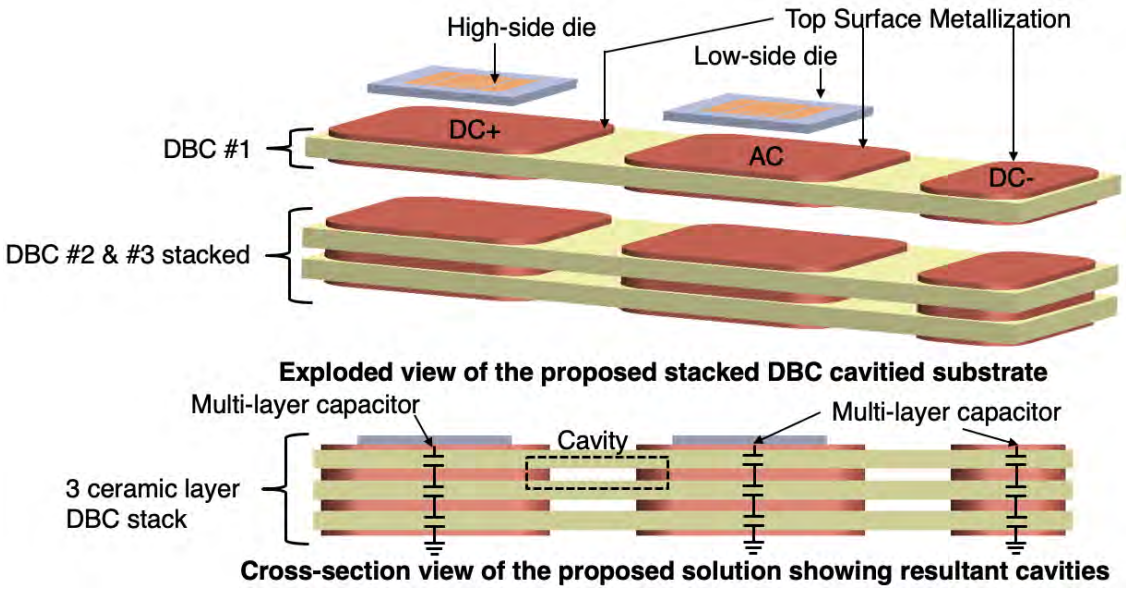


Figure 5.2: Exploded and cross-sectional views illustrating the proposed stacked DBC cavitied substrate.

and cost of DBC fabrication. With the availability of further high-voltage rated devices, there might be a need to stack more than two DBCs to reduce the e-field intensification. However, the approach of clamping internal metal layers to an electric potential fails when stacking more than two layers, especially when stacking odd number of DBC layers such as 3 and 5. For example, if there are n DBCs in the stack, during a high-voltage (DC+) state on the top-side AC metallization, the voltage gradient across each ceramic would be V_{DC}/n. However, during the low-voltage (0 V) state the voltage gradient across the top ceramic would be $(n-1)V_{DC}/n$ i.e. $n-1$ times higher compared to that during the complementary state. With more DBCs in the stack, this voltage gradient across the top ceramic will be exacerbated. Hence, a more scalable solution was pursued. The proposed stacked DBC cavitied substrate is illustrated in Fig. 5.3d. The stacked DBC cavitied substrate consists of a stack of multiple DBCs with the top-surface metallization pattern replicated on each inter-layer and the bottom-surface metallization. This creates a series-connected multi-layer

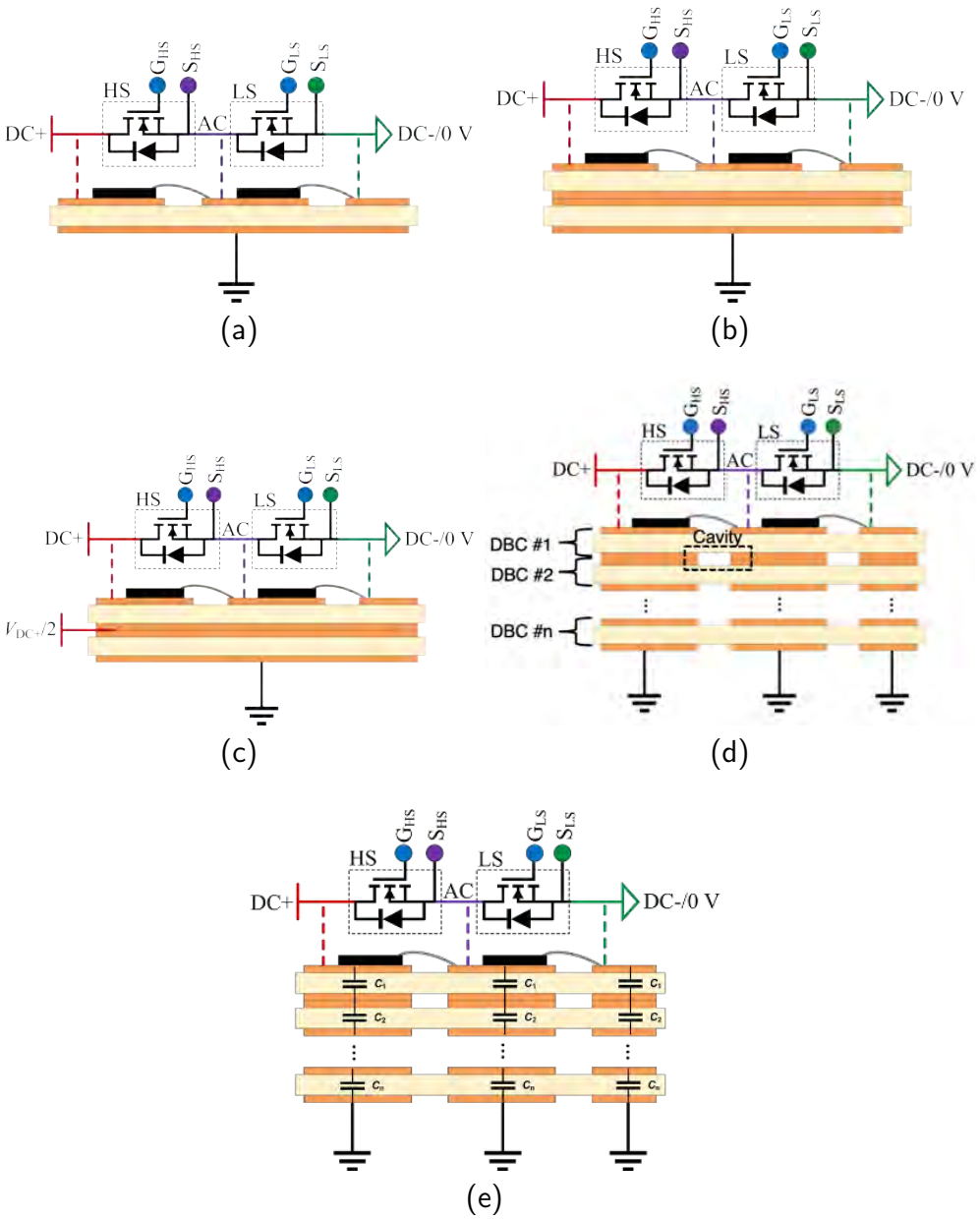
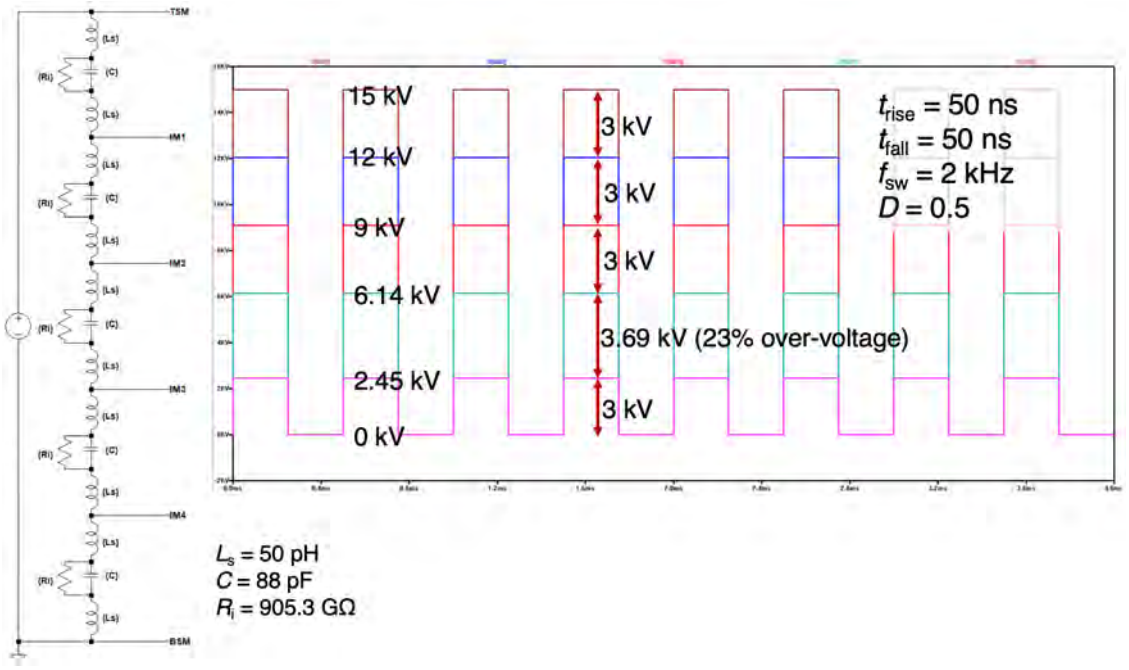


Figure 5.3: (a) Cross-sectional view of a conventional DBC substrate for a low-voltage and high-voltage half-bridge power modules. (b) Cross-sectional view of a stacked DBC substrate as proposed by Hohlfeld, *et al.* [14] when used for a high-voltage half-bridge power modules. (c) Cross-sectional view of a stacked DBC substrate with voltage-clamped mid-layer for high-voltage half-bridge power modules as proposed by DiMarino, *et al.* [16]. (d) Cross-sectional view of the proposed stacked DBC cavitied substrate. (e) The capacitance network in the stacked DBC cavitied substrate.

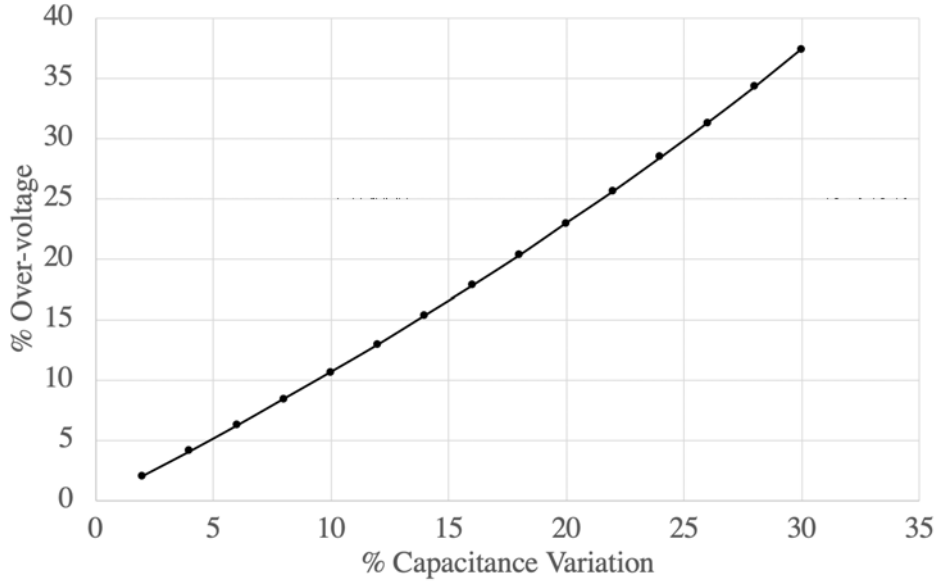
capacitor under the DC+, DC-, and AC top-surface metallization. The name, stacked DBC cavitied substrate, is derived from the cavities within the stacked substrate. These cavities are a consequence of the proposed approach. The can be used for integrated cooling as discussed in a further section. Most importantly, the multi-layer capacitors (see Fig. 5.3e), with the DBC ceramic acts as a dielectric, equally distribute the high-voltage of the top-surface metallization across each ceramic under it, i.e., the voltage gradient across ceramics in the stack is V_{DC}/n under DC+ and AC pads, including when the potential on top-side AC pattern switches from high to low state. The voltage distribution enables field grading and consequent minimization of the electric fields at the critical triple-point and within the bulk of ceramic.

5.3 Dynamic Voltage Distribution

Variation on the capacitance of each ceramic in the stacked DBC cavitied substrate could result in unequal voltage distribution. The DBC samples were characterized to study the effect of percentage variation of capacitance of DBC layers in the stack on the voltage stress across the ceramics. Figure. 5.4a illustrates the equivalent parasitic circuit between the top-side AC metallization and the corresponding bottom-side metallization in the stacked 5-DBCs cavitied substrate. The network includes the parasitic capacitance, and the parallel insulation resistance resulting from each ceramic in the stack. Also, the series inductance resulting from the Cu-to-Cu interconnection while stacking DBCs is included. DBC manufacturers do not provide the tolerance on the capacitance resulting due to the ceramic in the DBC. Hence, as shown in Fig. 5.4a, the 4th and 5th capacitor are assigned a tolerance of -20% and +20%, respectively. The equivalent circuit is excited with a trapezoidal waveform

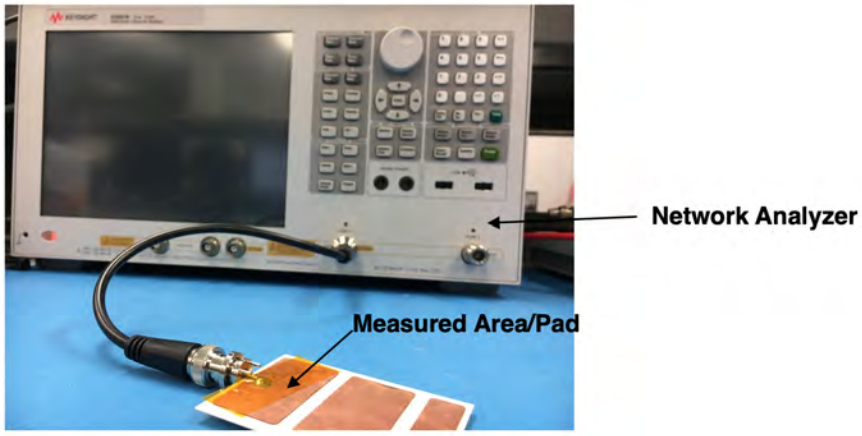


(a)



(b)

Figure 5.4: (a) The extracted parasitic capacitance of the stacked DBC (left). Voltage distribution across the stacked DBC upon trapezoidal excitation (right). (b) The maximum temperature and stress map from the parametric analysis for the stacked DBC cavitied substrate.



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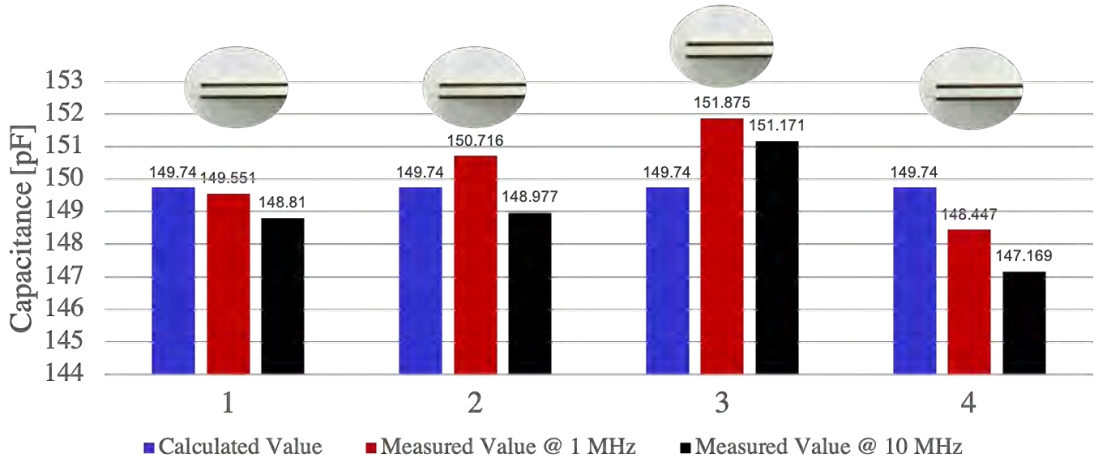

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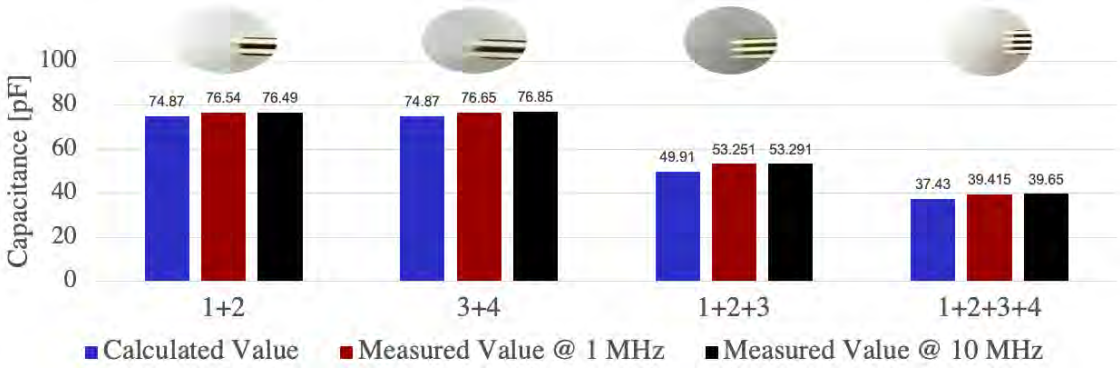
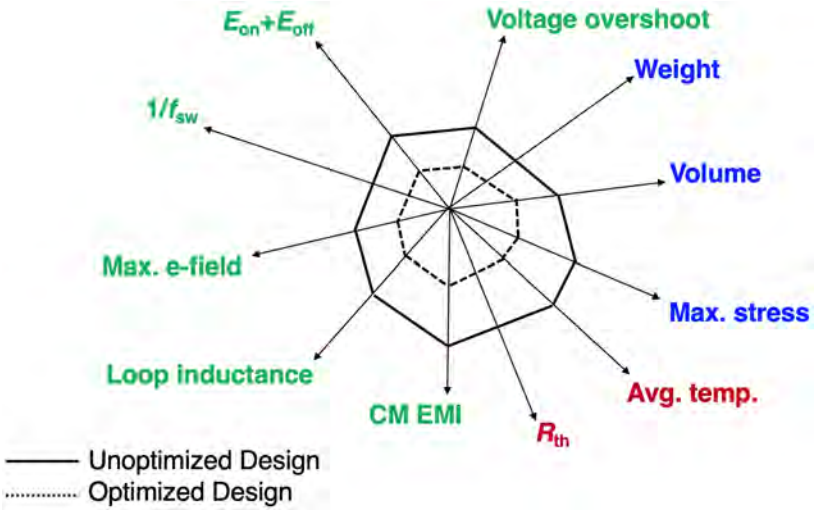


(c)

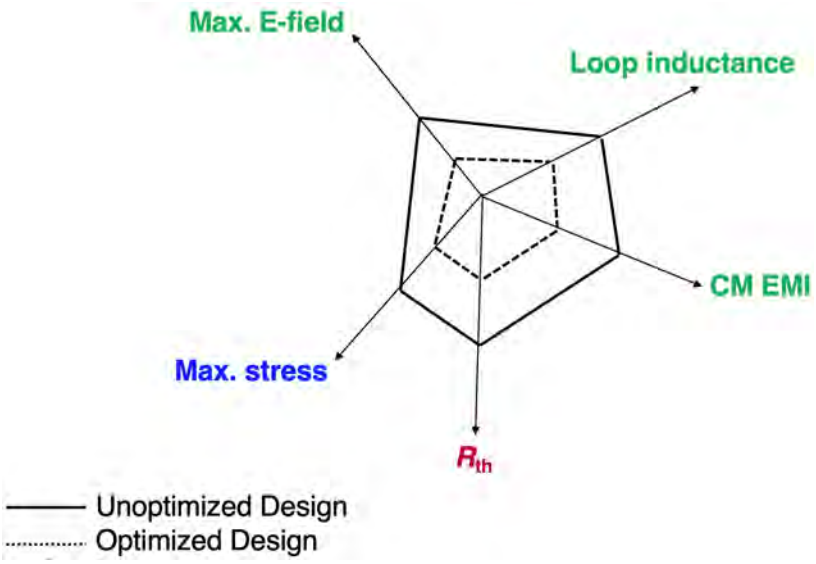
Figure 5.5: (a) Capacitance measurement setup. (b) Single DBCs. (c) Measured capacitance between the top-side and bottom-side AC pattern. [Source: Photo by author.]

resembling the voltage at the AC terminal during half-bridge operation with a rise and fall time of 50 ns and a switching frequency was 20 kHz, to test the dynamic voltage distribution. This results in an unequal voltage distribution across the capacitors. The 4th capacitor is stressed to a voltage that is 23% above the intended value. This over-voltage translates to an equivalent e-field intensification in the 4th ceramic in the stack. A sweep of capacitance variation from 2% to 30% was performed to estimate the over-voltage across the 4th ceramic. This is shown in Fig. 5.4b.

For experimental characterization, a 0.3-mm Cu/ 0.62-mm Al_2O_3/ 0.3-mm Cu DBC master card was etched out and singulated to form 4 DBC layers. The capacitance resulting from the DBC alumina ceramic between the AC/DC top surface metallization and corresponding bottom surface metallization is measured for each DBC. A Keysight E5061B network analyzer was used to measure the capacitance. A photograph of the test setup is shown in Fig. 5.5a. The measured capacitance value for each of the DBC as compared to the calculated value based on the 47 x 23.5 mm AC/DC pad area is shown in Fig. 5.5b. The percentage variation in the capacitance value was found to be less than 2% over the four samples. It can be inferred that the worst-case percentage over-voltage across the ceramics when DBCs are stacked will be less than 2%. Further, the etched DBC samples were stacked and the capacitance for these stacked DBCs were measured and compared to the estimated values as shown in Fig. 5.5c. These measurements indicate that the voltage distribution within the stack will be self-sustaining.



(a)



(b)

Figure 5.6: (a) Radar chart for comparison of designs using electrical, thermal, and mechanical co-design. (b) Radar chart with a subset of optimization objectives for evaluating the stacked DBC substrate architecture for 15 kV power electronics module.

5.4 Optimization Objectives and Parametric Analysis for Substrate Design

The radar chart in Fig. 5.6a could be used to evaluate the design space for a given architecture for a 15-kV power module. Each axis on the radar chart is an optimization objective. Several combinations of variables will generate different designs in the design

space. Moreover, the radar chart can also be used to evaluate the best designs from each different architecture. One of the design architectures presently under consideration is the stacked DBC cavitied substrate (SDCS) module. Fig. 5.6b shows a radar chart with limited design optimization objectives.

A parametric analysis was performed to evaluate the design space and find an optimal design for the optimization objective. The ceramic material sweep includes alumina, aluminum nitride, and silicon nitride. Further, the variable-sweep includes ceramic thickness (10, 15, 25, 40 mil), copper thickness (5, 8, 12 mil), number of DBC layers (1, 2, 3, 4, 5), and the heat transfer coefficient (1000 – 20,000 W/m^2K). While performing the parametric analysis, certain variables were fixed and predetermined using common design equations. These fixed variables include the copper-to-copper spacing, based on the enacapsulant's breakdown voltage, the required lateral isolation, and a safety factor. The conventional thermal spreading 45-degree angle theory determines the die-to-die spacing. The number of dies per switch position and the die-to-die spacing determined drives the copper area.

5.4.1 Parametric Isolation Voltage Map

One of the optimization objectives is to achieve an isolation voltage more than the mandated test voltage for 60 s insulation withstand test. The ceramic of the power module's substrate is subjected to the blocking voltage of the device it packages. For safety, IEC 61287-1 recommends a test voltage higher than the blocking voltage of the devices. The module must withstand that test voltage for 60 seconds. The test voltage for a 15-kV power module is 22.2 kV. A parametric isolation voltage map (see Fig. 5.7) is generated for the stack-ups generated by parametric sweeps. The dielectric strength of Al_2O_3, AlN, Si_3N_4 ceramic as per

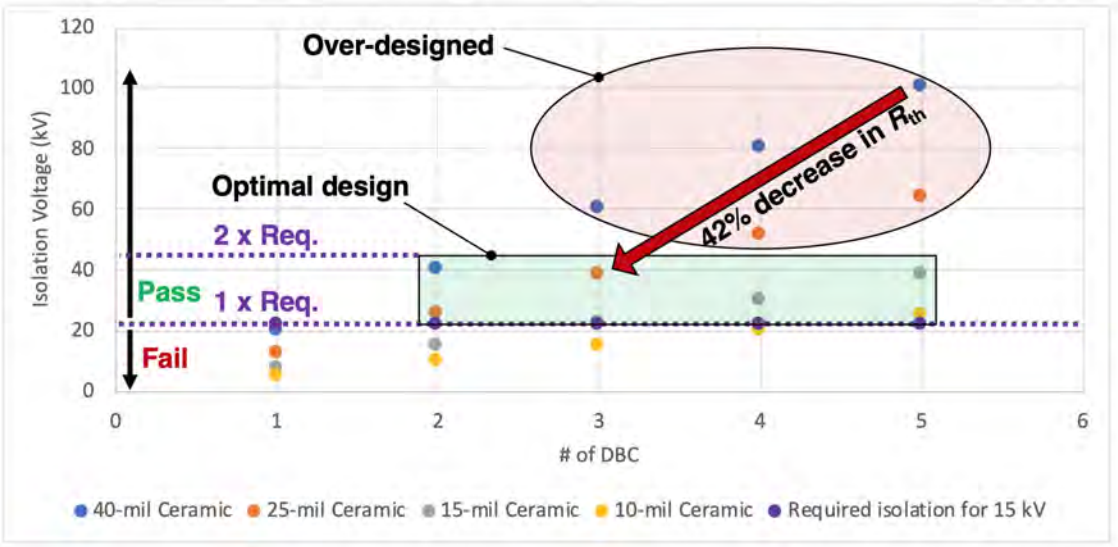


Figure 5.7: Parametric Isolation Voltage Map

Table 5.1: The set of possible stacked DBC cavitied substrates using commercial off-the-shelf single layer DBC with 1-mm thick ceramic.

		No. of ceramic layers				
		1	2	3	4	5
Total ceramic thickness (mm)	1	✓	✓	✓	✓	✓
	2		✓	✓	✓	✓
	3			✓	✓	✓
	4				✓	✓
	5					✓

manufacturer datasheet is 20 kV/mm. A 'pass' or 'fail' criteria is set at 22.2 kV. The region between this pass/fail criteria and twice the test voltage is described as optimal design. The stack-ups with an isolation voltage above twice the test voltage are considered over-designed as they significantly increase the junction to case thermal resistance. Table 5.1 presents the matrix of generated stack-ups for the parametric study.

5.4.2 Parametric E-field Map

The cross-sectional model used for the e-field analysis is presented in Fig. 5.9. The E-field was measured at a point, in the vicinity of the critical triple point in the stack,

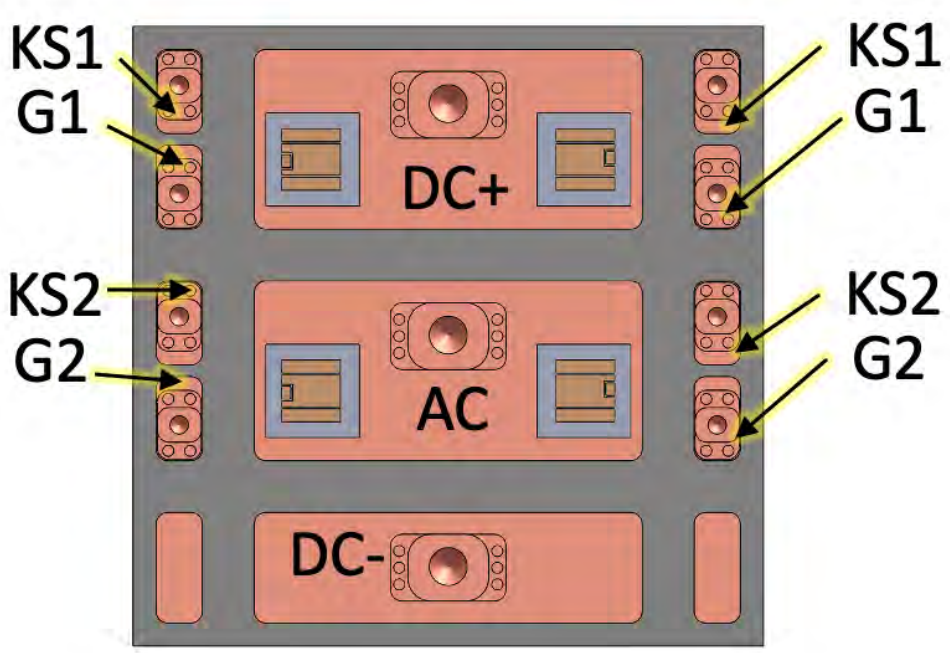


Figure 5.8: Layout of the designed substrate for the HV module.

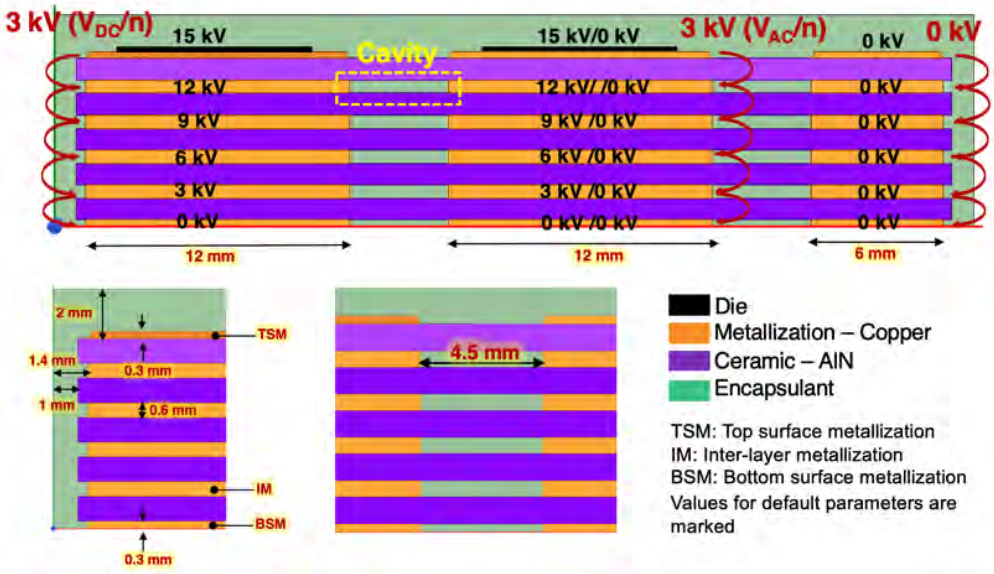


Figure 5.9: 2D model of the stacked DBC cavitied substrate for electrostatic simulations.

to mitigate the mesh dependency of the extracted value [17]. Two variants of the E-field parametric map were generated. The plot lines in Fig. 5.10 represent stack-ups with the same ceramic thickness. Also, the copper thickness for all plot lines is fixed at 0.3 mm.

Whereas, the Fig. 5.11 shows the sweep for combinations of different ceramic thickness and copper thickness used in the stack. They both indicate that the stacking of DBCs resulted in E-field reduction. A maximum of 60% E-field reduction was observed for the 5-layer ceramic stack (5-mm total ceramic thickness) when compared to a conventional DBC (1-mm ceramic thickness) and conventional silicone encapsulant. Also, it was observed that an encapsulant with a high dielectric constant further reduced the peak e-field. There is a diminishing return on the e-field reduction with stacking over 3 DBCs. Further, increasing the number of layers will increase the thermal resistance. Also, thick copper layers are better compared to thin copper layers in the stack. The differences in the electric field values are insignificant with the ceramic material. Hence, a 3-layer stack with 2-mm total ceramic thickness is one of the recommended solution. Other recommended solutions include the 4-layer stack with 2-mm total ceramic thickness and 5-layer stack with 2-mm total ceramic thickness. Additionally, the recommended stack-ups may reduce the parasitic common-mode capacitance, consequently reducing the common-mode noise current.

5.4.3 Parametric Thermal Map

The same parametric set in Table 5.1 was used to determine maximum stress and temperature map using ParaPower [18], a tool co-developed by US Army Research Laboratory and Naval Academy. Figure 5.12 and Fig. 5.13 present the extracted peak temperature and von Mises stress maps, respectively.

With the thermal maps the goal is to select the stack-ups that restrict the peak temperature under the maximum permissible device junction temperature, 175 °C, for given power loss and effective heat transfer coefficient at the module backside. The target is to

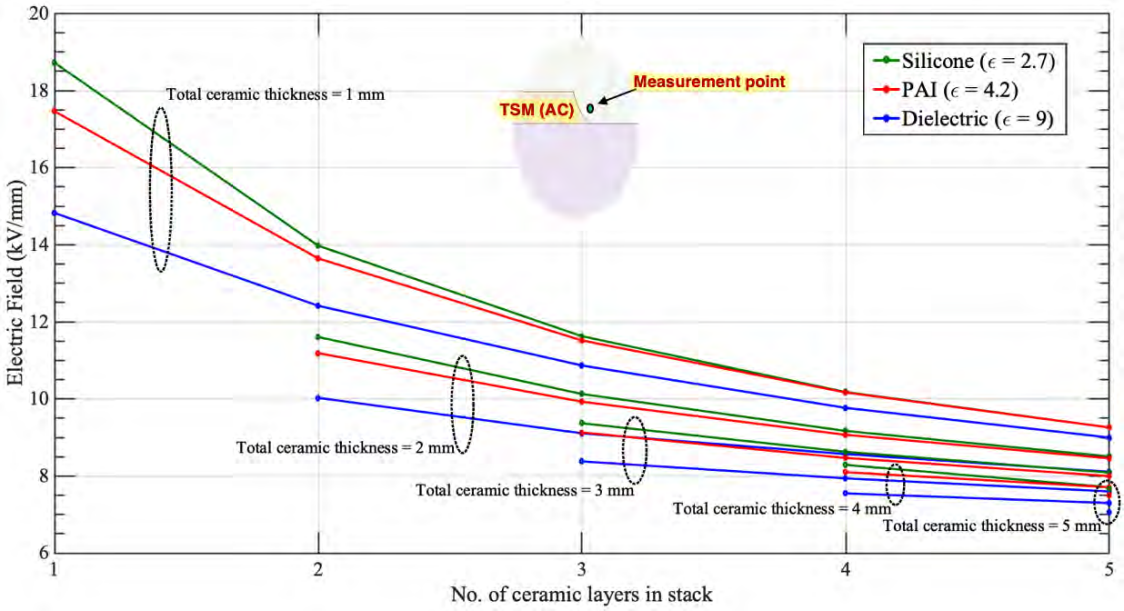


Figure 5.10: The electric field map from parametric analysis using a measurement point (inset), to eliminate singularity/ mesh dependency of the electric field extracted from the electrostatic simulation.

have a junction to case thermal resistance of less than 0.1 K/W per switch position. This number is derived from the datasheet of a 10-kV die. AlN ceramic is highly recommended for it high thermal conductivity. Silicon nitride is the next best choice. However, it is advisable to use AlN in recommended stacks with thickness above 0.64-mm and SiN in stacks with ceramic thickness less than 0.64-mm because of the material strength. Also, thicker copper in the stack provides better thermal spreading; hence, recommended.

5.4.4 Parametric Stress Map

The stress limits are based on the flexural strength of AlN (300-350 MPa), Alumina (300-400 MPa), and silicon nitride (500-800 MPa) ceramic. Silicon nitride being the material with highest strength is preferred for the stacking. However, other materials are possible if a specific stack up pass the stress limit in the stress map. However, the translation of the

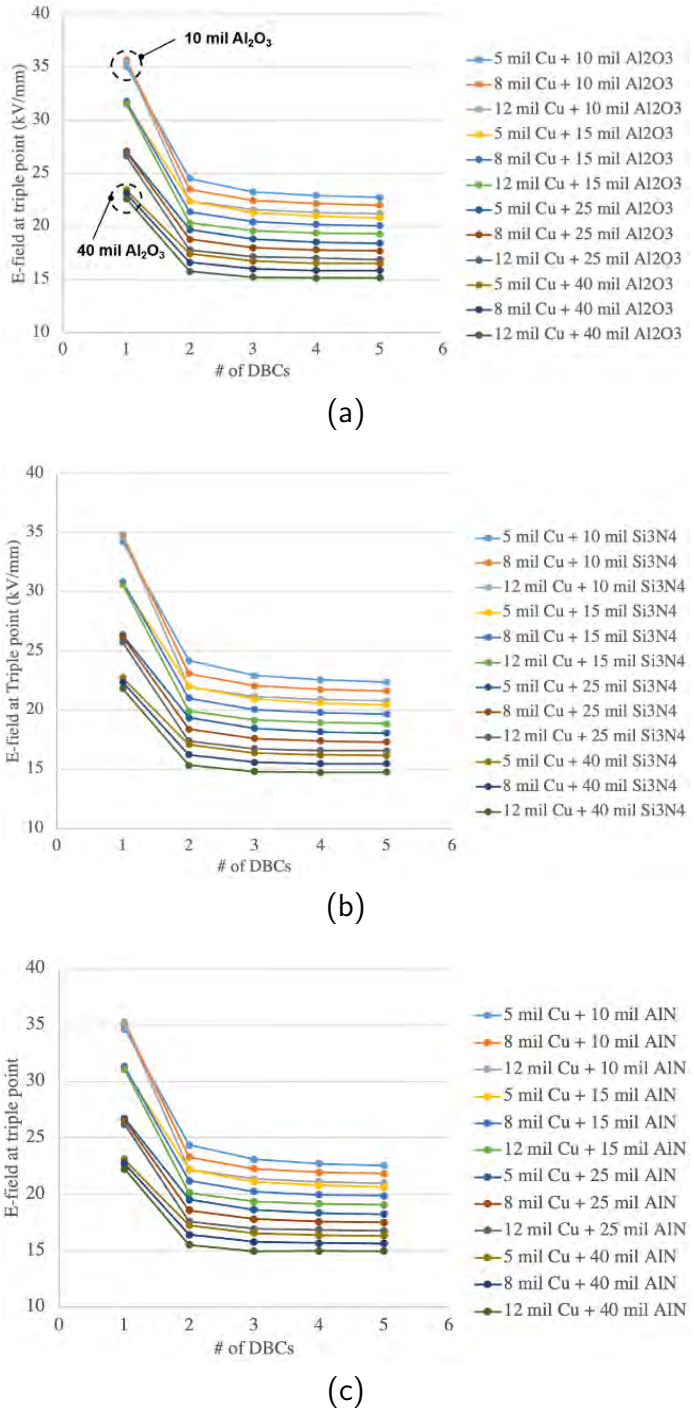
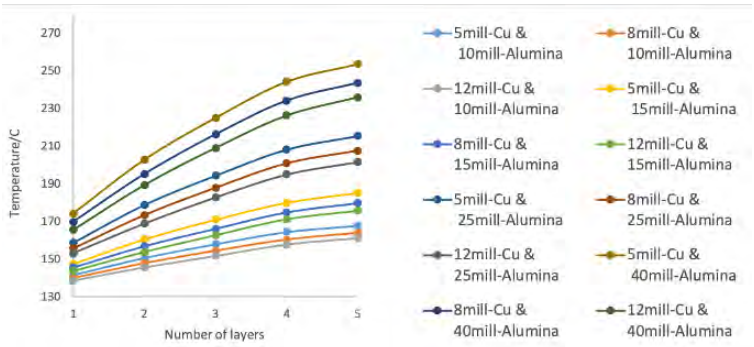


Figure 5.11: E-field maps. (a) Alumina ceramic based substrate (b) Silicon nitride ceramic based substrate. (c) Aluminum nitride ceramic based substrate.

stress to reliability needs further investigation.



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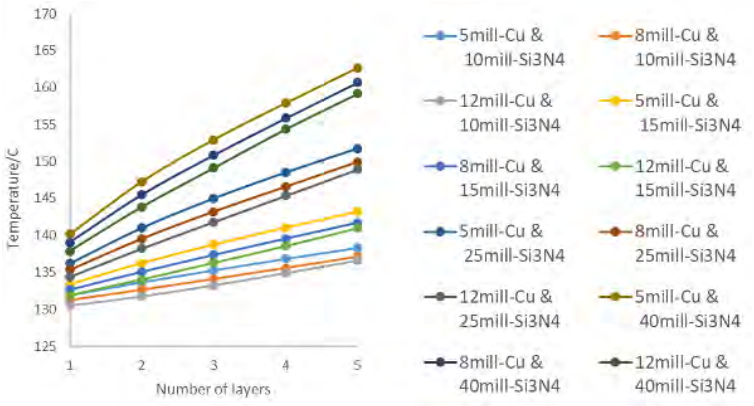

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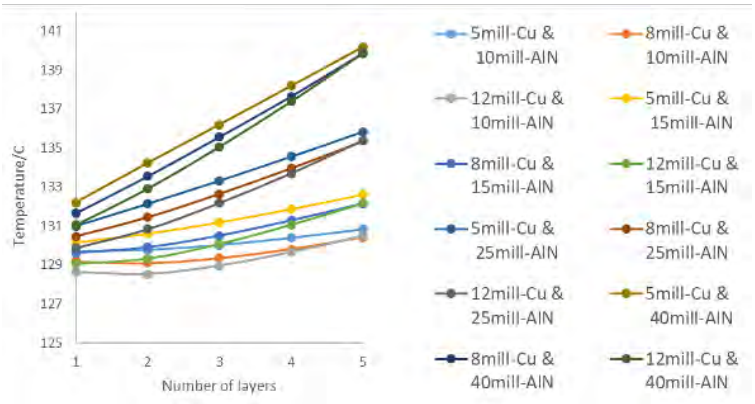
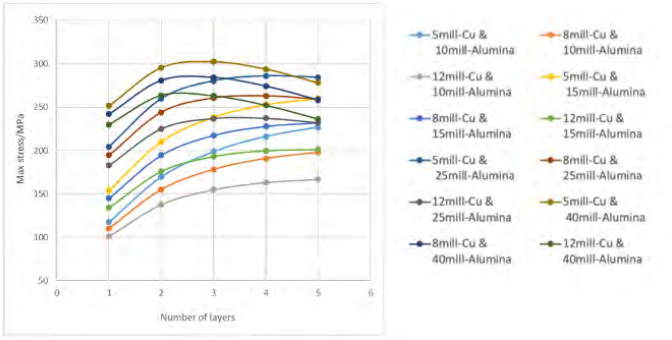
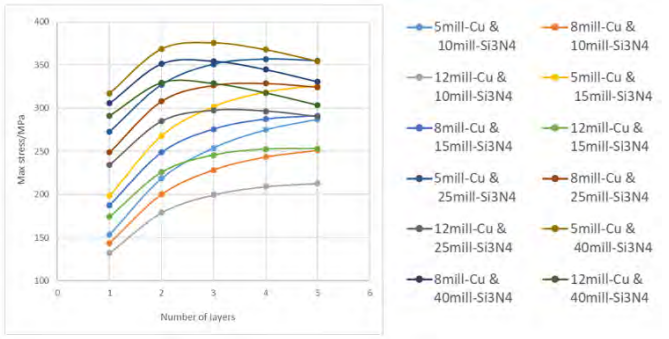


(c)

Figure 5.12: Thermal maps. (a) Alumina ceramic based substrate (b) Silicon nitride ceramic based substrate. (c) Aluminum nitride ceramic based substrate.



(a)



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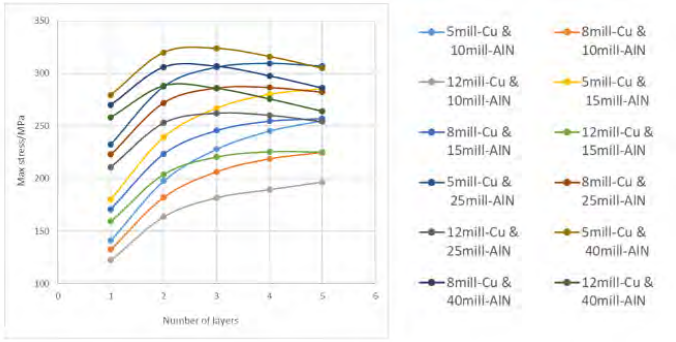


(c)

Figure 5.13: Stress maps. (a) Alumina ceramic based substrate (b) Silicon nitride ceramic based substrate. (c) Aluminum nitride ceramic based substrate.

5.4.5 Design Space Minimization

The design space consists of 60 options resulting from the parametric sweep. However, the design space is minimized using the flowchart in Fig. 5.14. As an example, the critical values for voltage rating, breakdown field strength, thermal resistance, and flexural strength

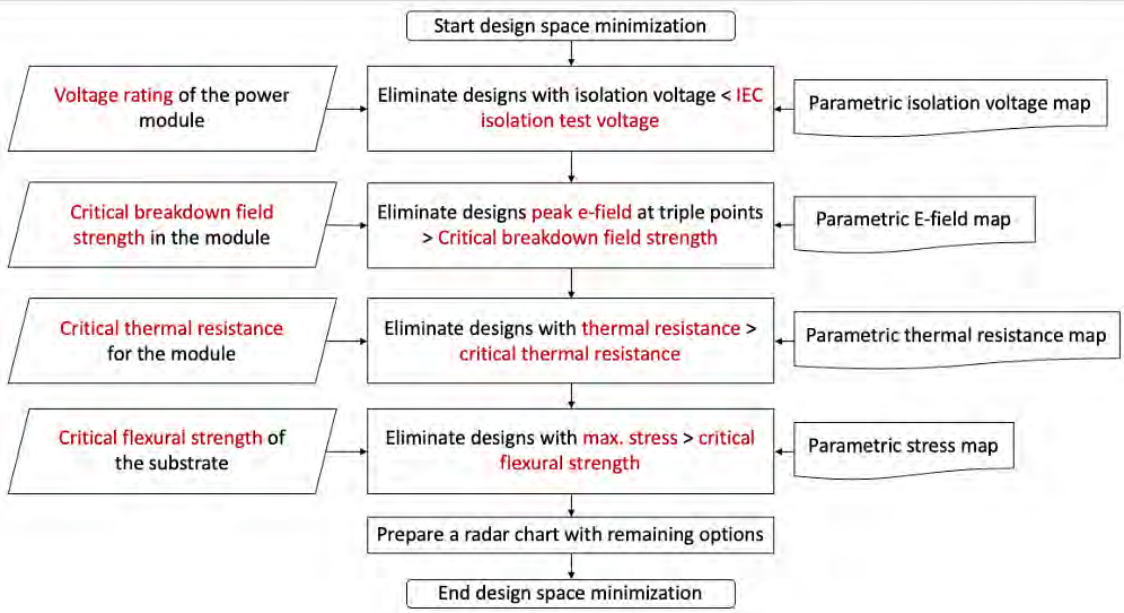


Figure 5.14: The flowchart for design space minimization.

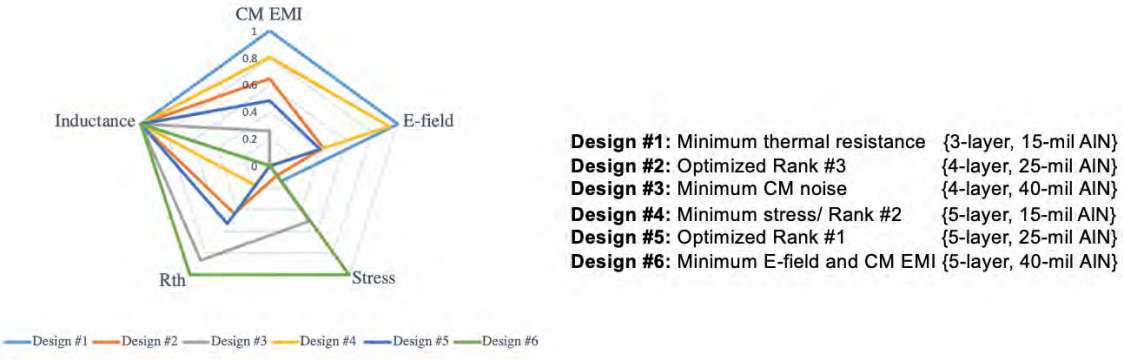
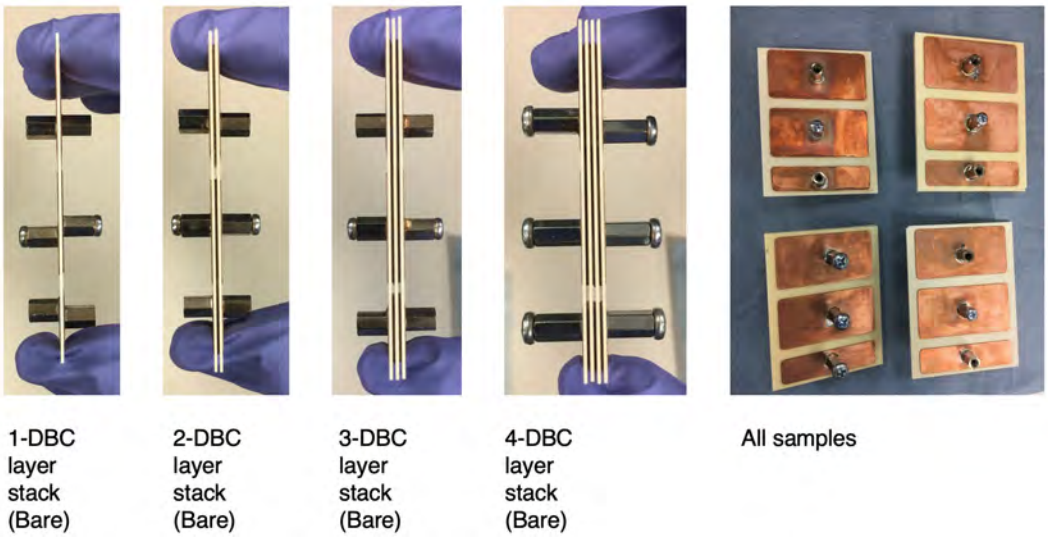
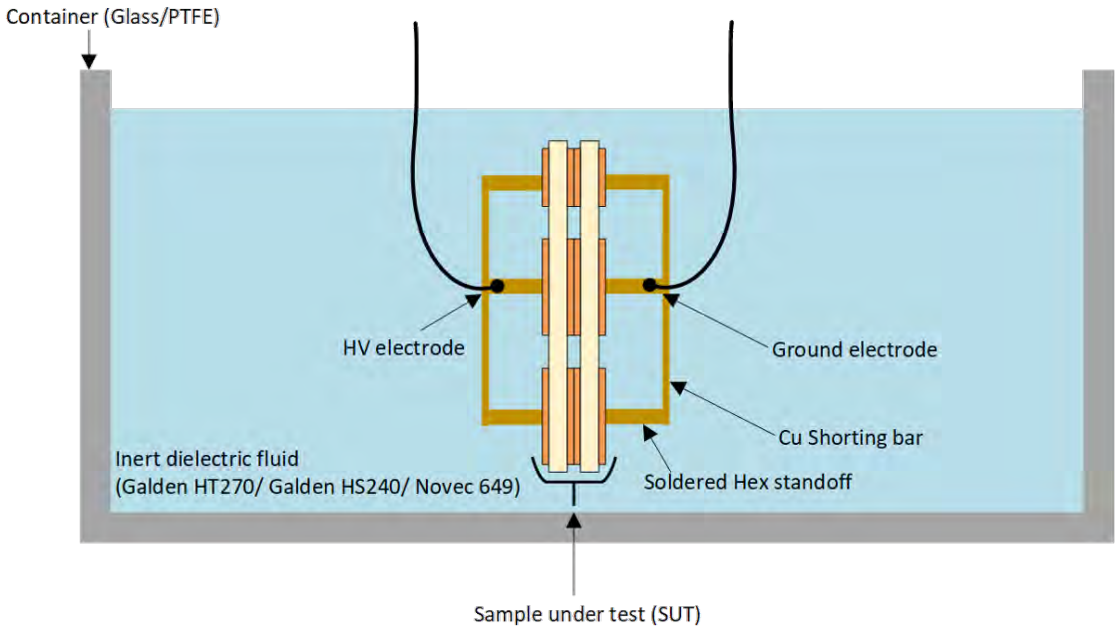


Figure 5.15: Radar chart comparing the downselected designs in the design space.

were set to 15 kV, 20 kV/mm, 0.07 K/W, and 300 (Alumina), 500 (Silicon nitride), 300 (Aluminum nitride), respectively. At each step the design not meeting the critical values were eliminated. Only 14 design options were left at the end of design space minimization. A few downselected options are illustrated on a radar chart in Fig. 5.15.



(a)



(b)

Figure 5.16: (a) Samples prepared for the DC testing (b) Test setup for the DC testing of the samples. [Source: Photo by author.]

5.5 DC Isolation Testing

1-, 2-, 3- and 4-layer stacks were tested for DC isolation and leakage current test. The samples are shown in Fig. 5.16a. These samples were tested using a Spellman MP30

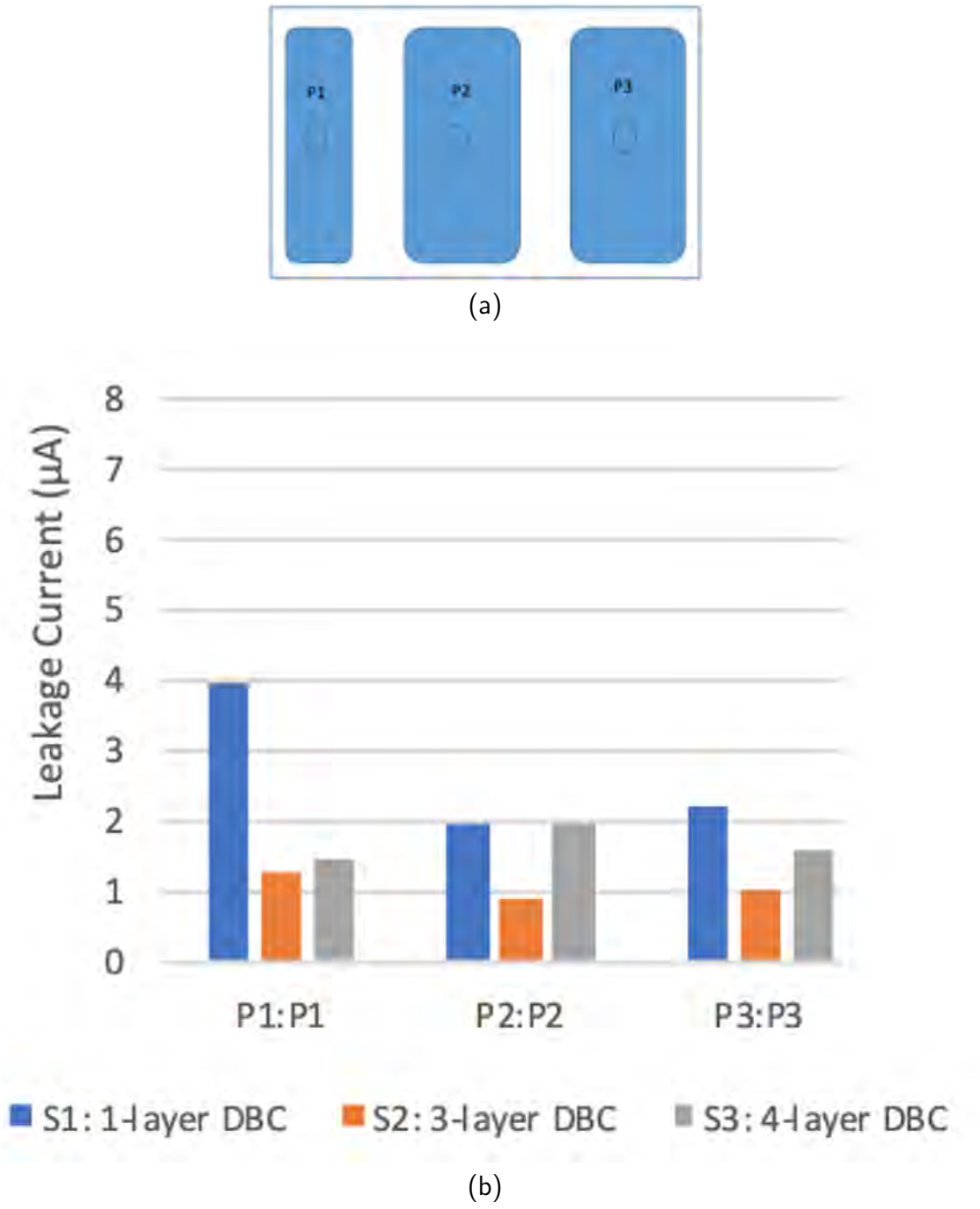
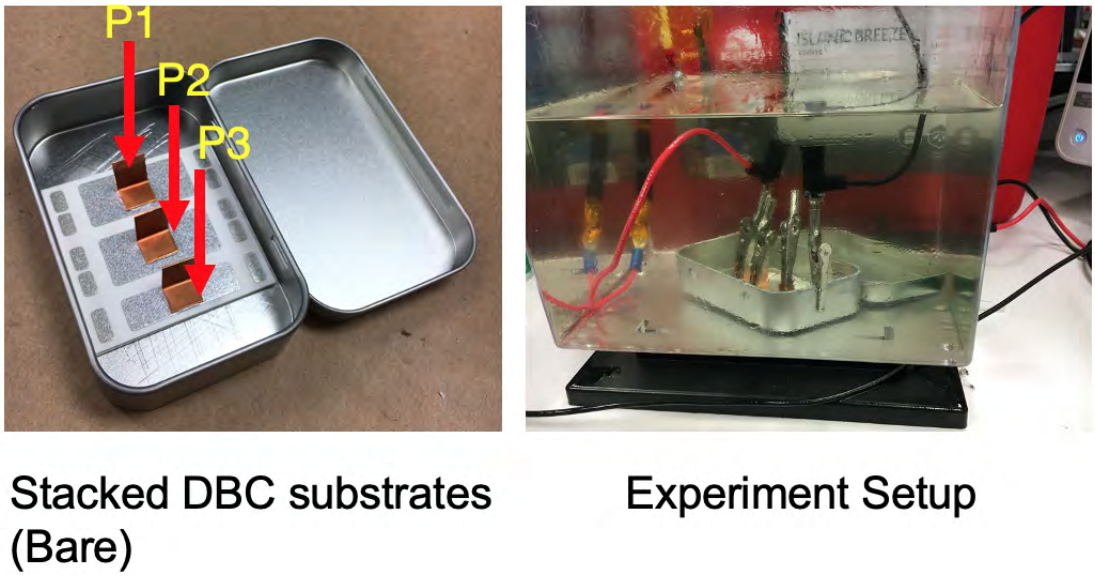
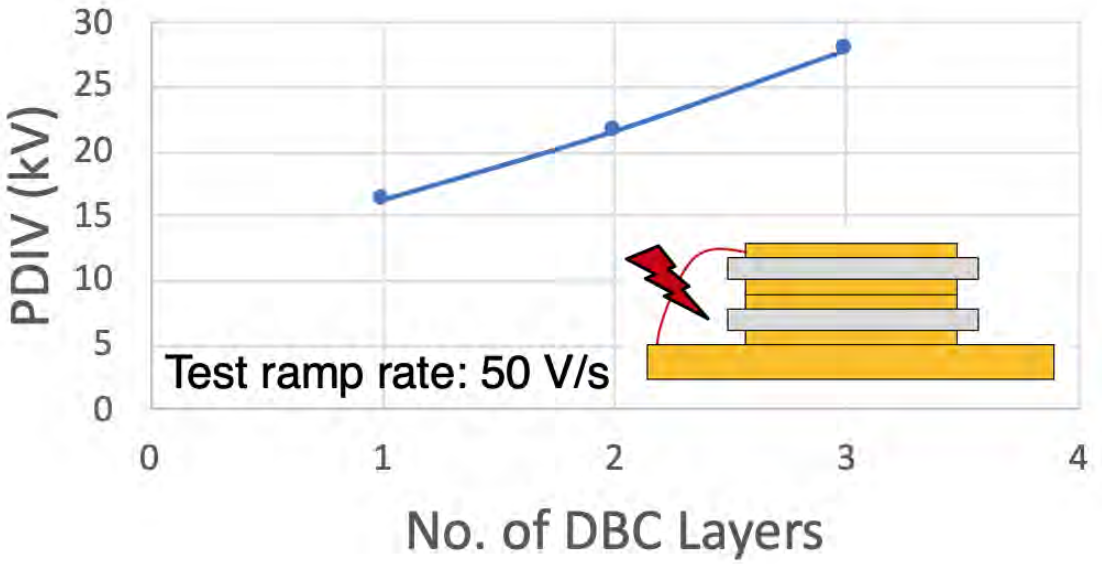


Figure 5.17: (a) The top view of the substrate with annotations highlighting the probe point. (b) Leakage current measurement during DC testing.

HV 30-kV, 10 W programmable power supply at the Army Research Laboratory, Adelphi, MD. The leakage current measurements are shown in Fig. 5.17b. The test voltage points are illustrated in Fig. 5.17a. P1:P1 refers to the application of test voltage across the top



(a)



(b)

Figure 5.18: (a) The samples and the test setup used for in-house DC testing. (b) The PDIV results from in-house testing. [Source: Photo by author.]

and bottom point P1. Results indicate that the leakage current reduced with a stacked substrate. Results exclude data for the 2-layer sample due to reduced surface cleanliness of the samples during fabrication and shipping, which led to the failure of the sample in

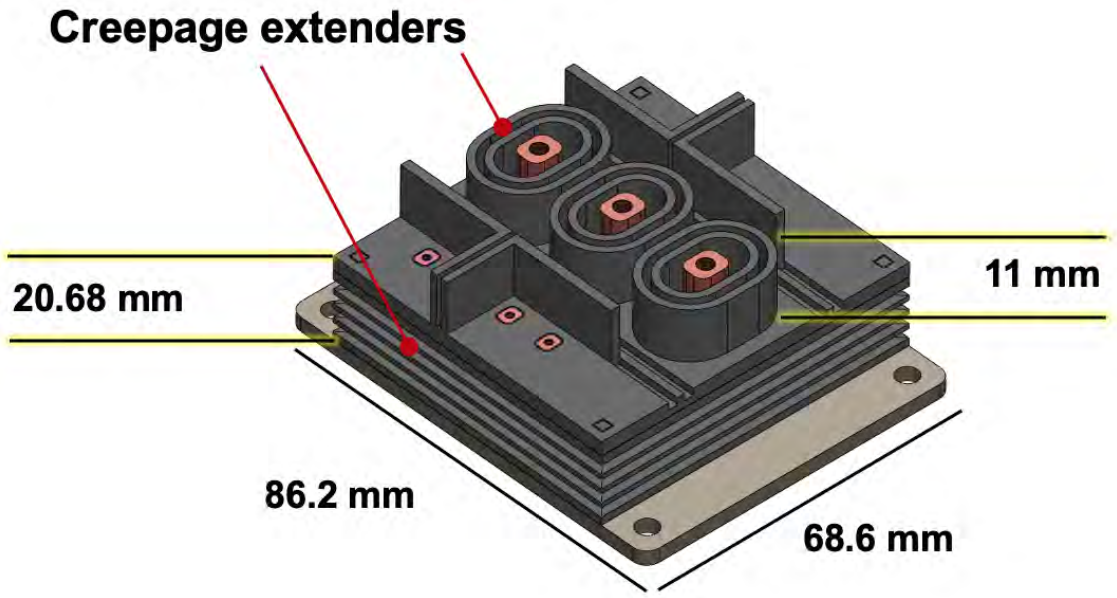


Figure 5.19: CAD model of the HV module.

testing. This issue also explains the higher leakage current for a 4-layer sample compared to its 3-layer counterpart.

Similar samples are made and attached in a steel can to emulate the effect of the module's baseplate on the breakdown voltage. Photos in Fig. 5.18a show such a sample and the experiment setup. The results in Fig. 5.18b highlight that the partial discharge inception voltage increases with the stacking of substrates. Further, from observation during the test, the breakdown occurred in the dielectric fluid between the top copper edge and the baseplate.

5.6 Housing Design

The module housing was designed to meet the requirements of creepage and clearance distances. The requirements for creepage and clearance distances are specified by the UL 840 standard. Since these values are specified for lower operating voltages, a linear interpolation

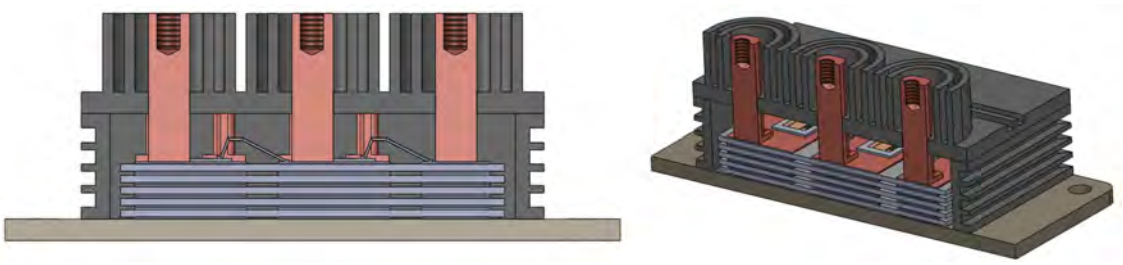
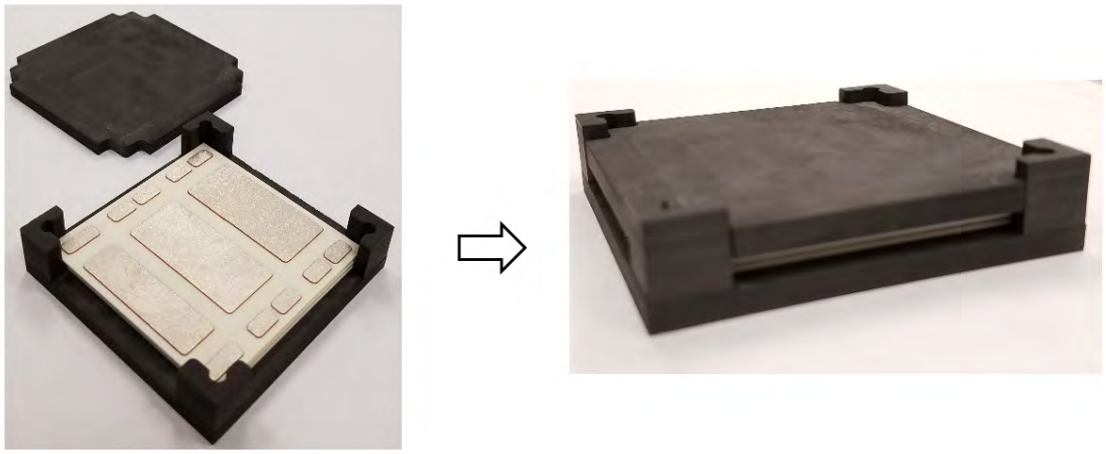


Figure 5.20: Cross sectional view of the HV module.

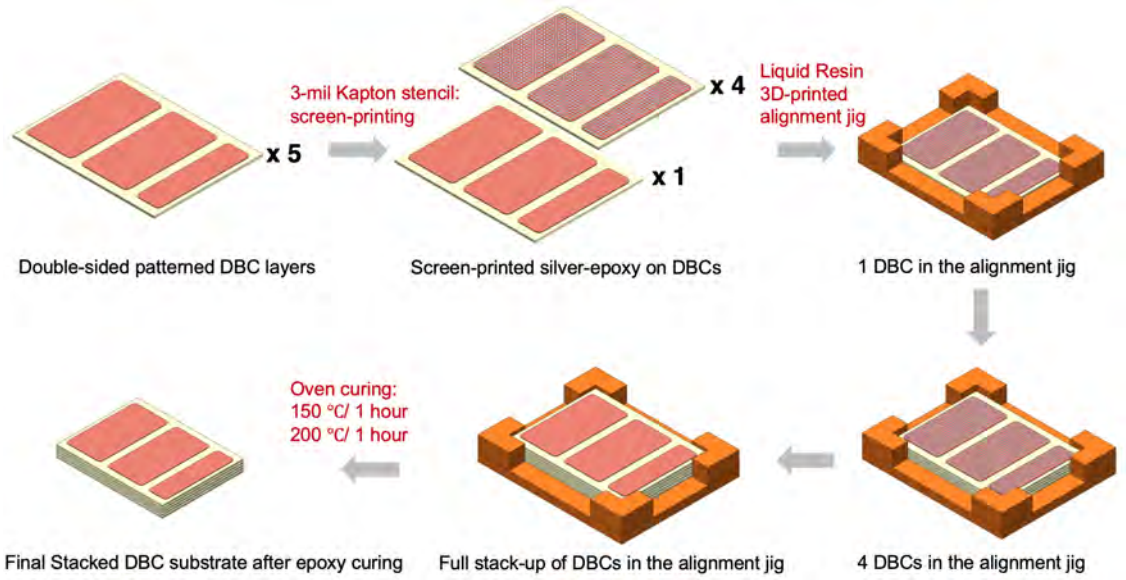
was used to determine the requirements at a 15-kV operating voltage of the designed power module. The creepage and clearance required were determined to be 75 mm and 45 mm, respectively. The required creepage and clearance distances determined are based on the assumption that the housing material is made of a material with a comparative tracking index (CTI) of 600 or more. A commonly used material for power modules with a CTI of 600 and more is polytetrafluoroethylene (PTFE). Fig. 5.19 shows the isometric and cross-sectional CAD renders of the designed power module to illustrate the housing design.

5.7 Assembly Process and Prototyping

The process for assembling a stacked DBC cavitied substrate mainly involves 1. Preparation of multiple DBCs, depending on the number of DBCs in the stack, with the same top-side and back-side patterns (see Fig. 5.22a). 2. DBC-to-DBC attachment using a thermally conductive silver epoxy, EK1000 from Epoxy Technology, which is stencil-printed on the DBC's top-side copper (see Fig. 5.22b and 5.22c). A negative stencil aligns the substrate on the printing base. A positive stencil aids the printing of the attachment paste on the top copper of the substrate. 3. An alignment jig milled from a graphite block (see Fig. 5.21a) ensures alignment and better handling during the assembly. The illustration in Fig. 5.21b describes the overall assembly process for stacking the substrates.



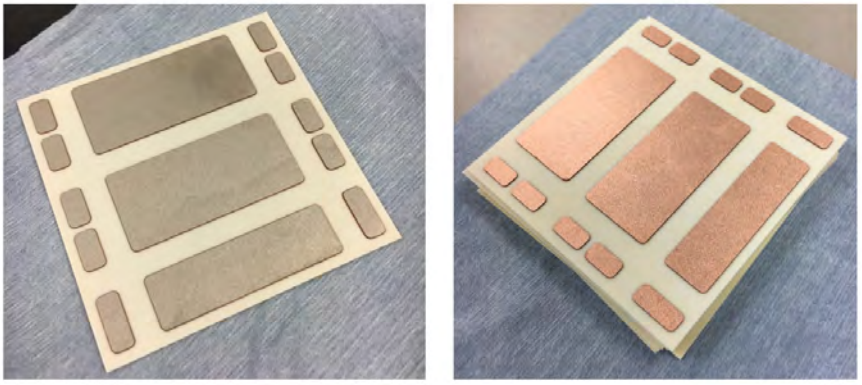
(a)



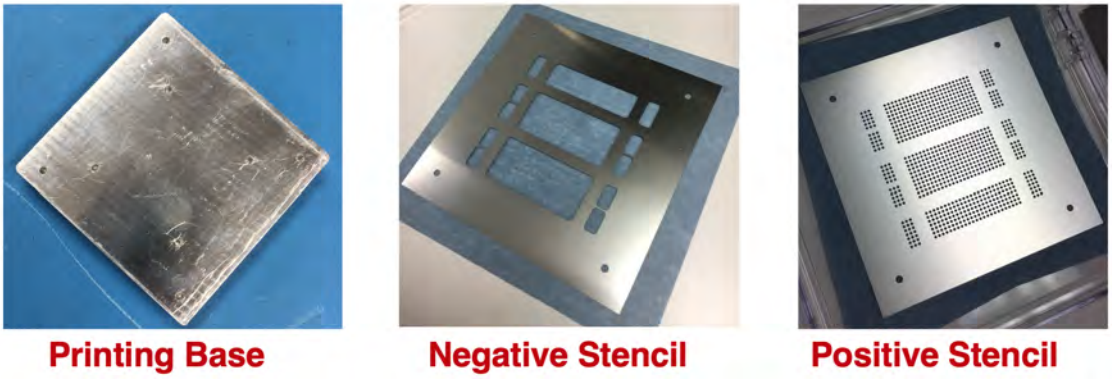
(b)

Figure 5.21: (a) Stacking substrate in a graphite alignment jig. (b) Detailed process for stacked DBC cavitied substrate. [Source: Photo by author.]

Next, the stacked substrate is attached to the baseplate (see Fig. 5.23). For this step, the silver paste is printed on the baseplate before placing the stacked substrate. The next step involves the attachment of the dies to the substrate, again printing the silver paste on the top copper using a stencil. Wire bonding is performed next for the power and signal bonds. Terminal attachment follows next. The housing, as shown in Fig. 5.24, is attached



(a)



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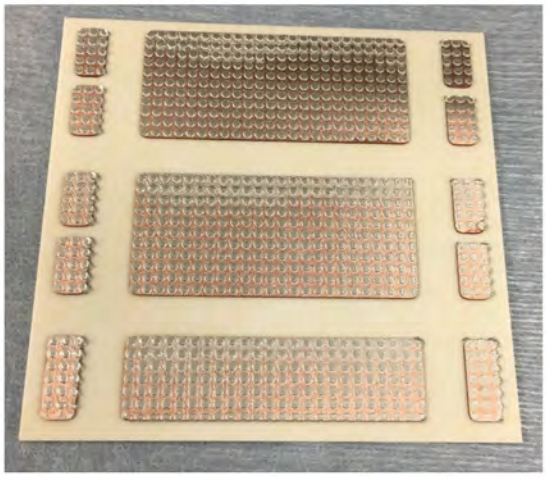


(c)

Figure 5.22: (a) Unit substrate for the HV module (b) Various stencils used for screen-printing. (c) Screenprinting attachment paste using stencils. [Source: Photo by author.]

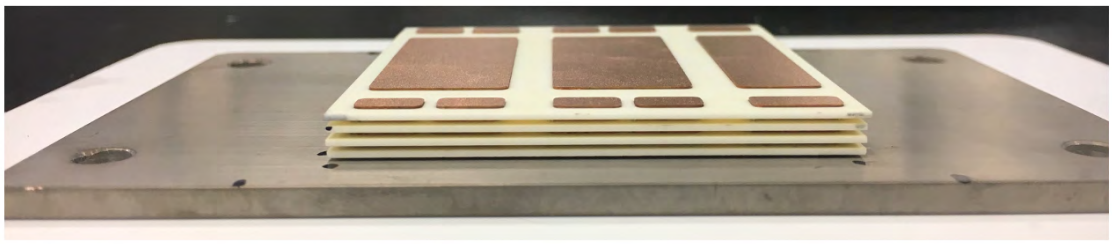
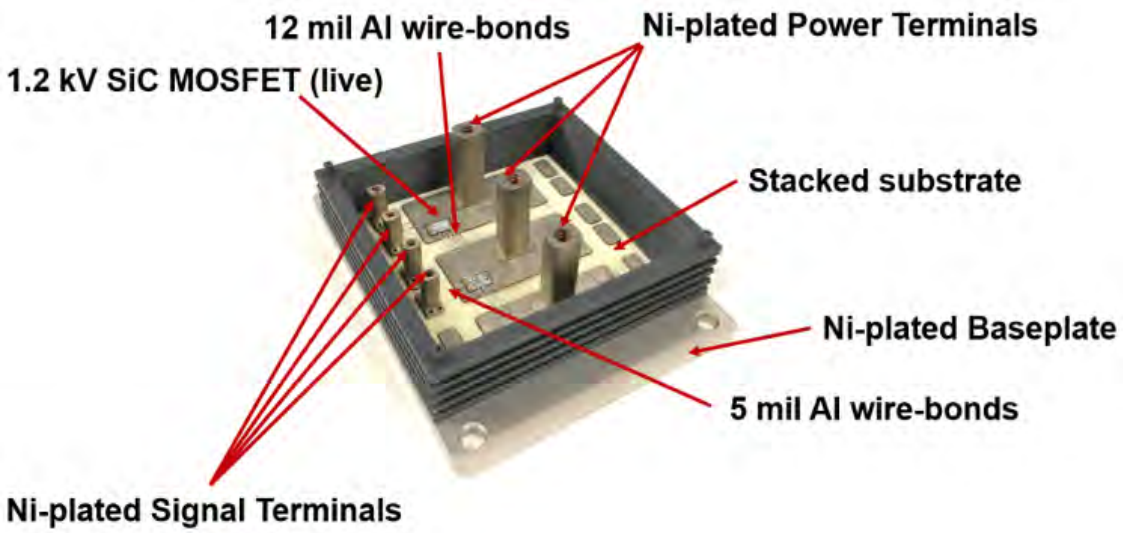


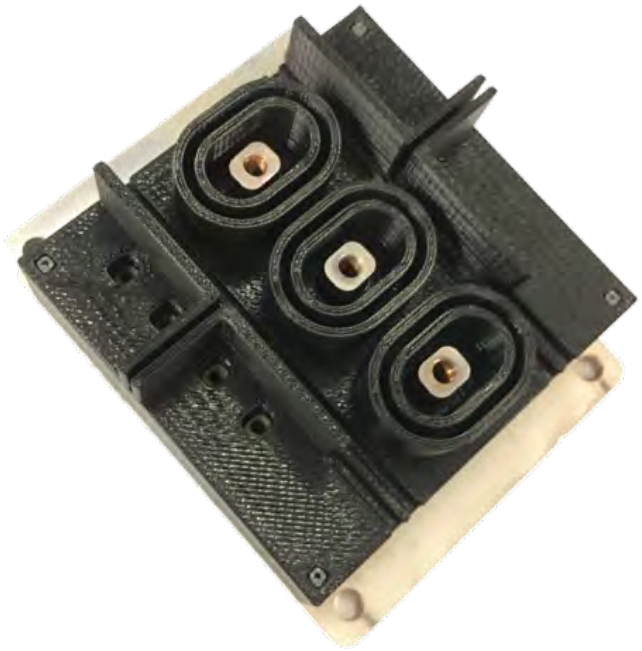
Figure 5.23: Substrate to baseplate attach. [Source: Photo by author.]

Figure 5.24: Photograph of the 3D printed housing and lid for the module. [Source: Photo by author.]

using a silicone RTV adhesive gel to prepare for the following encapsulation of the module with a high dielectric strength silicone gel. The final prototype after this step is shown in Fig. 5.25a and 5.25b.



(a)



(b)

Figure 5.25: (a) Photograph of the HV module prototype built using one die per switch position. (b) Photograph of the HV module prototype. [Source: Photo by author.]

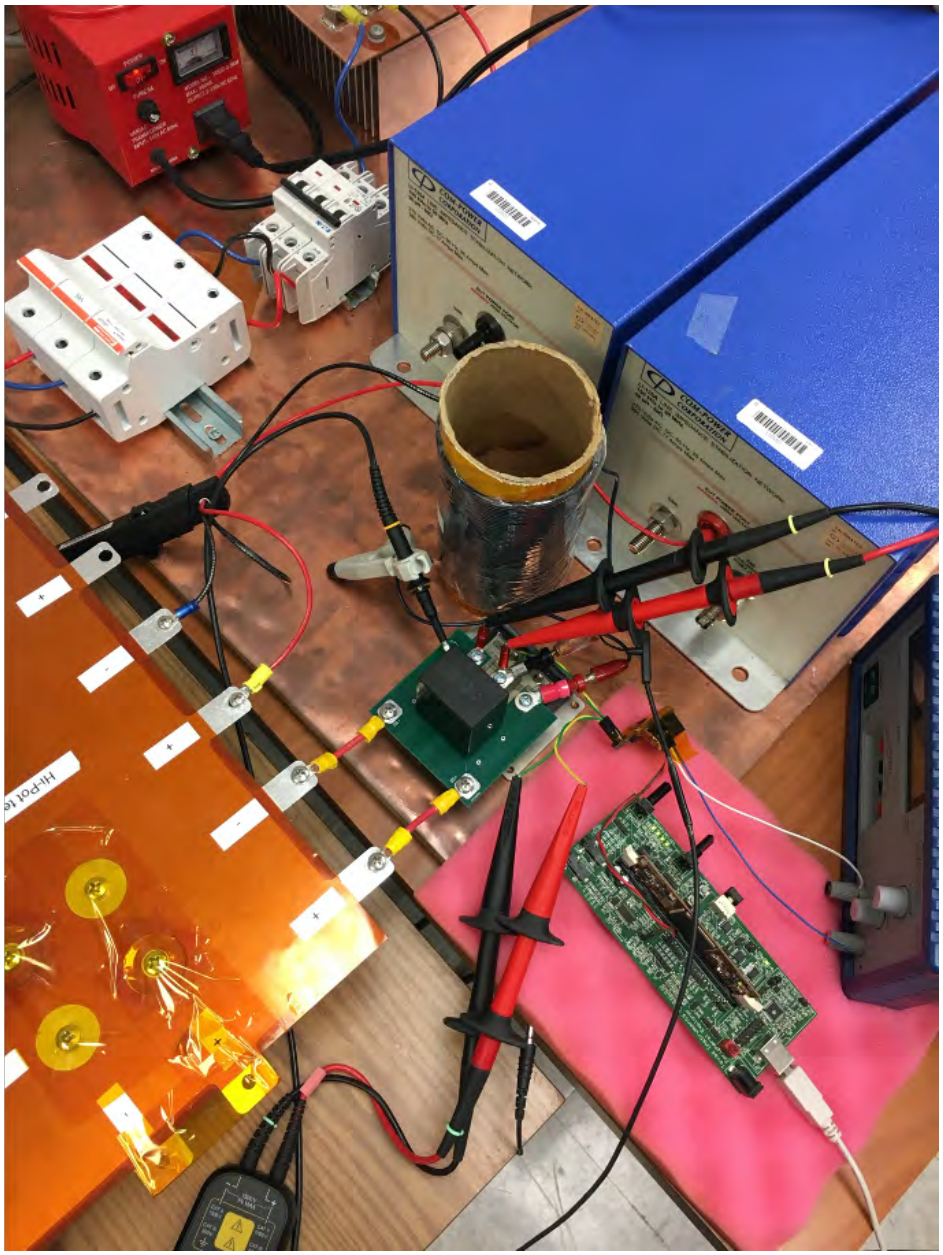


Figure 5.26: Test setup for double pulse testing and EMI characterization of the HV module prototype. [Source: Photo by author.]

5.8 Switching Tests and EMI characterization

The fabricated stacked DBC cavitied substrate prototype in Fig. 5.25b includes 3-layers of DBC with 0.64-mm thick Al_2O_3 ceramic for each DBC. Alumina ceramic DBCs

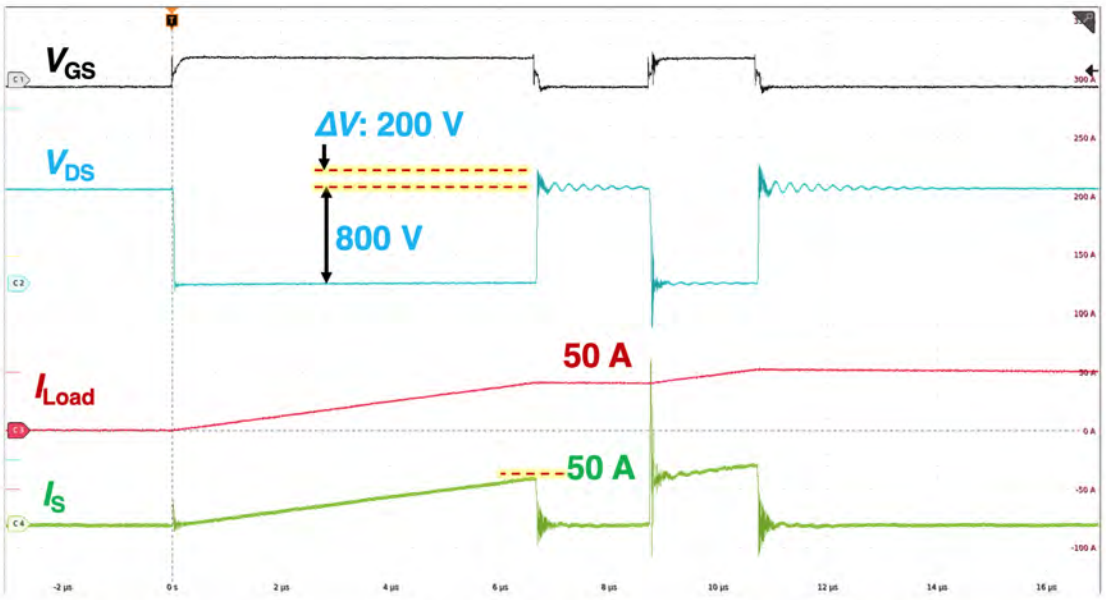


Figure 5.27: Waveforms from the double pulse testing of the HV module prototype.

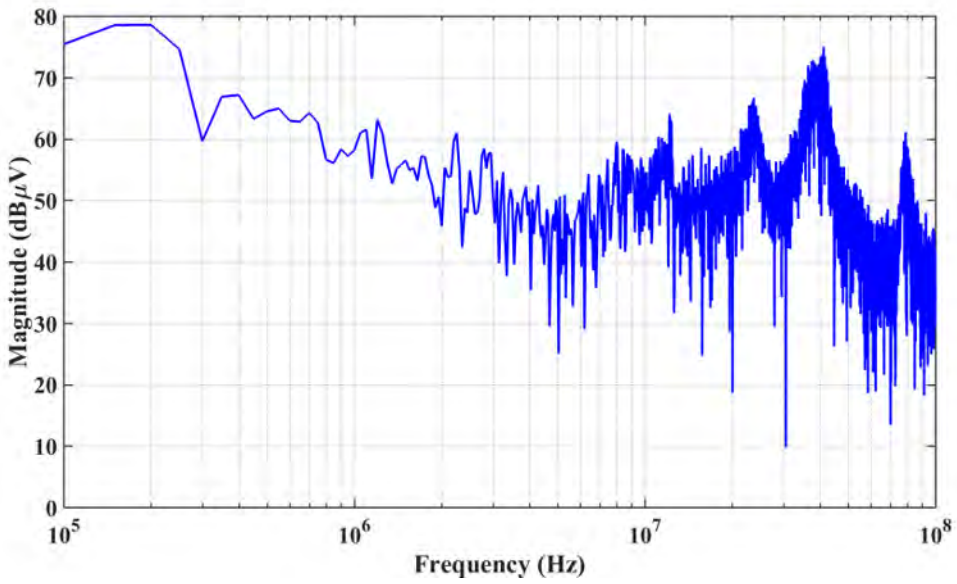


Figure 5.28: CM EMI noise emission from the power module prototype.

were used due to the availability and lower cost compared to aluminum nitride and silicon nitride. Each switch position is occupied by a 1.2 kV SiC MOSFET die from CREE. A low-voltage die was selected as the high-voltage die (10 kV) had a long lead-time. Double

pulse testing was performed on the power module at DC voltage of 800 V and a load current of 50 A. A decoupling capacitor board was used at the power module terminal to restrict the overall inductance in the power loop to that solely in the power module. The external turn-on and turn-off gate resistances were 10 and 5 Ohm, respectively. The waveforms from the testing (see Fig. 5.26) are shown in Fig. 5.27. Moreover, the CM noise emission of the power module was also measured. The measured noise from the line impedance stabilization network (LISN) is shown in Fig. 5.28.

5.9 Associated Work Done by Other Group

The proposed substrate would enable an integrated active-passive cooling solution. A phase-change material (PCM) integrated within the cavities of the proposed substrate would mitigate transient thermal loads by passive means. Thermal analyses with ANSYS and ParaPower were performed to investigate the effectiveness of PCM integration within the cavities of the stacked DBC. The performance was benchmarked against cases including a traditional encapsulant and no filling. The electrical characteristics of the sugar alcohol PCMs were explored and for integrating into the cavities of the proposed substrate. For validation and determination of dielectric strength was carried out using a specially designed test apparatus. The test setup also features a ceramic hotplate to enable the evaluation of temperature-dependent breakdown voltage [19]. There is also a possibility of integrated liquid cooling, which is being explored presently for improvements in the thermal performance.

5.10 Conclusion

A stacked DBC cavitied substrate-based high voltage power module is proposed for 15-kV SiC MOSFET. The stacked DBC cavitied substrate allows to reduce the electric-field concentration at the critical triple-points on the top-side. Moreover, it allows to independently distribute the high-voltage at each top-side pad equally across the ceramic stackup under them, which leads to equal bulk e-field in the ceramics. The feasibility of the proposed approach of stacking is validated using the capacitance measurements on DBCs for the substrate. An electrical, thermal and mechanical co-design approach with optimization objectives demonstrates the down-selection of best stack-up for the desired module operating voltage. The DC isolation and leakage current tests also suggest that the stacking approach presented is suitable for increasing the voltage rating of the module. The module was loaded with low-voltage devices (1.2 kV) and subjected to switching tests and EMI characterization.

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6 Conclusion

This chapter highlights the critical contributions and significance of the work performed in this dissertation. Moreover, it recommends several possible items for further improvements in the future. Although the work performed as part of this dissertation research focuses on the Si-IGBT and SiC-MOSFET-based hybrid switch, the ideas and findings are applicable to further the state-of-the-art in the converter- and module-level packaging of WBG devices as well.

6.1 Dissertation Contribution

This dissertation demonstrates a converter- and module-level packaging of a Si-IGBT and SiC-MOSFET-based hybrid switch. Also included is the work related to the packaging of 15-kV SiC devices in this dissertation. The contributions and conclusions from each chapter in this dissertation are as follows.

Chapter 2 presents a HyS consisting of a large Si IGBT and small SiC MOSFET in parallel for high-current, high-power power conversion systems. The influence of the parasitic interconnection inductance unbalance between Si and SiC devices within the HyS is studied using a systematic analysis. A boundary-line inductance unbalance value is estimated to be 10 nH, which helps decide between gate control options. A comprehensive cost analysis is performed using commercial 1.2 kV devices. The analysis indicates that with a 1:4 or 1:6 SiC/Si current ratio, the cost for HyS at currents above 50 A will be 50 to 75% lower for discrete devices. Moreover, a maximum of 60% cost saving is achievable at 300 A, when comparing 1:6 HyS module with an identical current rated SiC module. The

presented algorithm, which uses a dynamic junction temperature prediction, helps select an optimum SiC/Si current ratio to ensure a reliable HyS operation. Also, a design example suggested that 1:6 ratio HyS is possible, with the availability of an improved package, while using a lighter cooling system, enabling high specific-power density. The experiment results suggested approximately 50% savings in the switching loss using the proposed gate control option. A 650 V HyS with a 1:5 SiC/Si current ratio in a DC-DC boost converter operation was demonstrated. Also, analysis based on the EMI noise and thermal image was presented.

A design methodology for a three-level t-type power electronics building block using a hybrid switch was presented in chapter 3. It emphasized the development of a converter-level package using discrete packages for Si and SiC devices. The primary focus was the non-trivial busbar design with low inductance and symmetrical commutation loops. The use of aluminum for busbars, selection of discrete semiconductor package, and distributed dc-link capacitor bank led to a lightweight PEBB implementation, with a specific-power density of 27.7 kW/kg. Also, the PEBB had a volumetric power density of 308.61 W/in3. The PEBB was operated in a continuous test at 48 kVA to an efficiency of 98.2%.

In chapter 4, a high power-density, 1700-V, and 300-A Si-IGBT plus SiC-MOSFET hybrid switch-based, half-bridge power module is presented. The module offered a 6-over-1 Si over SiC current ratio with a low power loop inductance of about 12.3 nH. Heterogeneous integration of a custom-designed metal-encapsulated TPG baseplate and silver clips top-side interconnects is presented in the module. The integration of these two technologies offered low thermal impedance and near isolated thermal path for the SiC MOSFET to operate at a higher temperature than the Si-IGBT. The module operation was demonstrated in a clamped inductive load testing.

A stacked DBC cavitied substrate-based power module is proposed for 15-kV SiC MOSFET in chapter 5. The stacked DBC cavitied substrate allows reducing the electric-field concentration at the critical triple-points on the top-side of the substrate. Moreover, the stacking with cavities allows independent distribution of the high-voltage at each top-side pad equally across the ceramic stack up under them, which leads to equal bulk e-field in the ceramics. The feasibility of the proposed approach of stacking is validated using the capacitance measurements on DBCs for the substrate. An electrical, thermal, and mechanical co-design approach with optimization objectives demonstrates the down-selection of best stack-up for the desired module operating voltage. The DC isolation and leakage current tests suggest that the stacking approach presented is suitable for increasing the module's voltage rating. The module was loaded with low-voltage devices (1.2 kV) and subjected to switching tests and EMI characterization.

6.2 Future Work

As with all research and development work, there is scope for further development using the work demonstrated in this dissertation. The hybrid switch-based converter-level packaging has already served as a ground work for a full-SiC-based converter-level packaging and demonstrated in literature. The future work includes development and testing of three PEBBs in a three-phase system with a motor load and closed-loop control.

The developed hybrid switch-based power module can further integrate gate drivers inside the module on the gate routing PCB. Moreover, the PCB can be integrated in the housing's sidewalls to reduce the process step of attaching the PCB on the DBC substrate. Improvements in the assembly fixtures may allow for attaching the terminals along with the

dies to further reduce a process step. Moreover, the DBC substrate can be divided into two halves (one for each cell) for better thermal cycling performance leading to a better DBC-to-baseplate attachment.

Next steps for the high-voltage power module development involves the validation of the stacked substrates using AC testing at 50/60 Hz. Further, the proposed stacked substrate should also be tested under a high frequency square waveform with fast switching transients. There is also a possibility of integrated liquid cooling, which is being explored presently for improvements in the thermal performance.