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Synthesis and Application of Ceramic Paste for High-Temperature Electronic Packaging

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Synthesis and Application of Ceramic Paste for High-Temperature Electronic Packaging

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by

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ABSTRACT

This dissertation research focused on the synthesis and application of ceramic paste for high-temperature applications. An alumina paste material comprising aluminum dihydric phosphate and alumina powder was developed for high-temperature electronic packaging. Nano aluminum nitride and nano-silica powders were embedded to promote the paste curing process, limit the grain growth, and increase its bond shear strength. The chip-to-substrate bond strength was enhanced and met the MIL-STD requirements for die-attach assembly. Its encapsulation property was improved with fewer cracks compared to similar commercial ceramic encapsulants. The die-attach material and encapsulation properties tested at 500°C showed no defect or additional cracks. Thermal aging and thermal cycling were carried out on the synthesized paste. XPS analysis revealed a higher oxygen bonding percentage for the 10% nanosilica ceramic sample than other samples. XRD peak broadening is largest for the 10% nano-silica ceramic which indicated smaller crystallite sizes. The smaller crystallite size for the 10% nanosilica sample introduces a larger microstrain to the alumina crystal structure. FTIR revealed the presence of alumina-silicate bonds on these samples with the largest amount present in the 10% nanosilica samples. SEM and EDX results showed a uniform bond line for the 10% sample and uniform material distribution.

An electronic packaging technology that survives the Venusian condition was developed. Alumina ceramic substrates and gold conductors on alumina were evaluated for electrical and mechanical performance. The most promising die-attach materials were found to be thick-film gold and alumina-based ceramic pastes. Alumina, sapphire, silicon, and silicon carbide dice were attached to the alumina substrates using these die-attach materials and exposed to the Venusian condition for 244 hours. The devices on the packaging substrates were encapsulated by a ceramic

encapsulant with no significant increase in cracks and voids after the Venusian simulator test. Wire pull strength tests were conducted on the gold bond wire to evaluate mechanical durability before and after the Venusian simulator exposure test with about 30.8% decrease which satisfied the minimum requirement for the MIL-STD-885 method. The overall wire-bond daisy-chain resistance change was 0.47% after the Venus simulator test, indicating a promising wire bond integrity. A titanium package was fabricated to house the ceramic packaging substrate and a two-level metalized feedthrough was fabricated to provide electrical interfaces to the package.

A double-layer ceramic electronic packaging technology that survives the Venusian surface condition was developed using a ceramic interlayer dielectric with gold conductors. A 60-μm ceramic interlayer dielectric served as the insulator between the top and bottom gold conductors on high-purity ceramic substrates. Test devices with AuPtPd metallization were attached to the top gold pads using a thick-film gold paste. Thermal aging for 115 hours at 500°C and thermal cycling from room temperature to 450°C were performed. Dielectric leakage tests of the interlayer ceramic layer between the top and bottom gold conductors revealed a leakage current density of less than 50×10^{-7} A/cm^2 at 600V after thermal cycling. The die shear test showed a 33% decrease in die shear strength after thermal tests but still satisfies the MIL-STD method.

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Chapter 2: Ardalan Nasiri, Simon S.Ang, 2020 "Application of Alumina-Based Ceramic Paste for High-Temperature Electronics Packaging" Journal of Electronic Packaging, The American Society of Mechanical Engineers (ASME), accepted on June 4, 2020.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF PUBLISHED PAPERS

Chapters 2, 3, and 4 were published/accepted in scientific journals that are listed below with minor modifications.

Chapter 2: Ardalan Nasiri, Simon S.Ang, 2020 "Application of Alumina-Based Ceramic Paste for High-Temperature Electronics Packaging" Journal of Electronic Packaging, The American Society of Mechanical Engineers (ASME), accepted on June 4, 2020. (in press).

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CHAPTER 1

Introduction

1.1 Introduction

Any human-constructed mission to hot planets is limited by the electronics and materials which are used in the equipment that collect, process, and deliver valuable scientific data. Advanced missions depend on remote monitoring techniques to study hot planets especially Venus exploration [1-1]. Yet, the flight through Venus's atmosphere is expected to last about an hour. This offers a tremendous challenge to the electronics due to its extreme temperature, pressure, and corrosive environment [1-2]. The Venus atmosphere consists of sulfuric acid clouds and carbon dioxide, which keep the heat from the sun and results in high surface temperature (~ 470°C) [1-3].

To implement long-term in-situ probes on Venus or other similar hot planets, a robust data processing, navigation, and communication system is required which can withstand 500°C as well as the corrosive environment. To achieve operation within this harsh environment, bulky cooling radiation shielding and systems utilized to prevent degradation during operation is required. Unfortunately, this increases the payload and consequently, the cost. Ultimately, a higher operating temperature impacts mission duration and design [1-4].

To solve and improve this technology gap, high-temperature electronics packaging must be developed. Wide bandgap semiconductor materials including gallium nitride (GaN) and silicon carbide (SiC) have been shown to operate well in high-temperature environments. However, current packaging technology fails below 500°C and cannot survive the chemical attack due to a harsh environment (e.g., sulfuric acid haze and clouds) [1-5]. A new thermally-stable material platform comprising a weather-resistant packaging architecture must be developed for extended operation in an extremely harsh environment. In addition to electronics, the package housing,

interconnects, substrate, and passivation material should survive the chemical attack from the harsh weather conditions. This will solve a host of terrestrial problems, in addition to hot planet exploration. The high-temperature packaging technology can be utilized in numerous industries such as geothermal energy production, oil and gas exploration, and nuclear energy [1-6].

Additionally, the modern increase in demands on the electronic power supply, i.e., higher power density resulting from smaller integrated circuit size, power electronics systems need promising, high-reliable, and thermally conductive components. For future power electronic systems, high-temperature operation, enhanced lifetime, thermal dissipation, and reliability aspects are the major challenges. Researchers and industries who are dealing with increasingly harsher environments are struggling with reliability and durability issues within high-temperature and corrosive environments. The industries that are involved with the high-temperature capable technology could be aerospace, oil and gas industries, geological surveys, military installations. With a general focus on space vehicles, especially for Venus exploration, the package operating temperature needs to be 500ºC with continuous operation for 500-1000 hours [1-7].

Different reliability tests are used to evaluate package sustainability. Thermal and mechanical tests can be performed such as thermal aging, thermal shock, thermal cycling, die shear, wire pull strength, etc. The bonding strength of the chip and substrate is evaluated by the Military Standard Product Testing Services (MIL-STD) method (MIL-STD-883 method was used for die shear evaluation). This metric, which is so crucial in electronics packaging, changes after multiple thermal and mechanical cycles. This is generally understood to be due to grain boundaries evolution during the thermal reliability tests [1-8].

1.2 Ceramic materials

Ceramics can be synthesized or fabricated by different methods, the initial material could be in either the solid, gas or liquid phases. The relevant chemical reactions involved in their synthesis are divided into three categories. The first category is gas-phase reactions, which include chemical vapor deposition, conducted metal oxidation, and reaction bonding. The second category is the liquid precursor method, which includes the sol-gel and polymer pyrolysis processes. The third category is a fabrication from powders including melt casting and pressed powder firing, which is utilized to fabricate glasses and polycrystalline ceramics. In this dissertation, the focus will be on the firing of the compacted powders. In this method, powders are compacted to create a porous cast, which is then post-fired to create a dense material [1-9].

Ceramics cover a vast range of materials, that generally can be divided into two categories, advanced and conventional ceramics. Historically, conventional ceramics are connected with those materials which developed with beginning of the civilization such as pottery and clay-based refractories. This now includes cement, concretes, glasses, and compromise most of the ceramic industry. Recently, advanced ceramics became more relevant. The advanced ceramics include those with applications in electronics, optics, magnetics, and structures (elevated temperatures) and are often referred to as functional ceramics. These are nonmetallic inorganic materials. Common examples of ceramic materials are the silicate compounds such as Mullite ($Al_6Si_2O_{13}$), Kaolinite [$Al_2Si_2O_5$ $(OH)_4$], in addition to simple oxides including zirconia (ZrO_2), alumina (Al_2O_3), etc. Other, more complex oxides are considered ceramics, such as barium titanate ($BaTiO_3$) and an example of superconducting materials could be $YBa_2Cu_3O_{6+\delta}$. Additionally, there are non-oxide ceramics including silicon nitride (Si_3N_4) and boron nitride (BN), as well as carbides such as boron carbide (B_4C) and silicon carbide (SiC) [1-10].

All solids can be commonly classified as either crystalline or amorphous, which is often pointed out to as the glassy phase. The crystalline ceramics are made up of many small grains of single crystals, which are isolated from each other along their grain boundaries. Here, two distinct length scales govern material properties. These are the atomic lengths and the microstructure lengths or grain sizes. Atomic-scale refers to the bonding category and amorphous or crystal structure for glassy or crystalline structures while in microstructure which is a larger scale, it refers to nature, distribution quantity of the structural elements, and phases in the ceramic. The intrinsic property of the material that is associated with the microstructure is a separate topic to discuss [1-11].

The intrinsic or inherent properties can be determined by structure of atomic scale of the material. The inherent properties cannot be changed easily by microstructural modifications. These properties are such as elastic modulus, coefficient of thermal expansion, melting point, and other intrinsic properties such as brittleness, ferroelectricity, and magnetism. On the other hand, many properties depend on microstructure, which varies by external engineering application of the material such as dielectric constant, mechanical strength, and electrical resistivity. Inherently, ceramic materials have relatively high melting points, which is why they are known as refractory materials.

The ceramic materials have high stiffness, are chemically inert, and generally brittle. At the same time, their electric, dielectric, and magnetic properties vary over very wide ranges. For instance, their conductivity can range from insulating to highly conductive. The crucial relation between atomic structure, ceramic fabrication, polycrystalline ceramics characteristics, and microstructure is shown in Figure 1.1. For example, the ferroelectric property of the $BaTiO_3$

originated from a perovskite crystal structure, i.e., chemical composition. The inherent properties of the ceramic materials should be considered in the material selection stage [1-12].

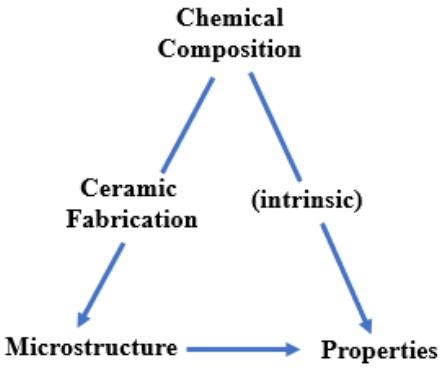

Figure 1.1. Crucial relation in ceramic fabrication.

1.2.1 Polycrystalline ceramics synthesis from powders

The fabrication of ceramics is divided into processes before the firing and processes during the firing. The chart shown in Figure 1.2 describes this synthesis process for polycrystalline ceramics. The powder mixing could be with a binder or additives, then the consolidation process is carried out by different methods such as molding, casting, and pressing processes. The characteristics or properties of the powder depends on its synthesizing method. The major powder characteristics are size, shape, degree of agglomeration, size distribution, purity, and chemical composition [1-13].

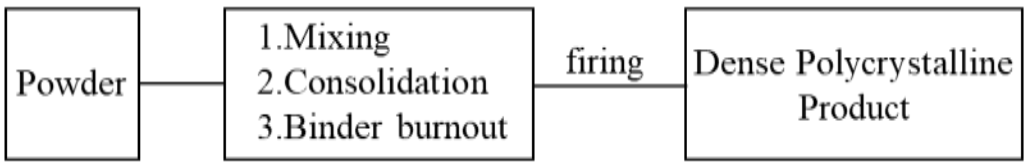

Figure 1.2. Flow chart of ceramic polycrystalline synthesis from consolidated powder by the firing process

1.2.2 Inorganic ceramic paste synthesis

There are different types of ceramic pastes with different synthesis methods. The initial material can be gas-, liquid-, or solid-phase. The ceramic paste constituents are base material, filler, and curing agents. Different oxide materials are added to the curing agent to optimize the curing rate and temperature. The typical oxides such as MgO, ZnO, SiO_2 can be added to the paste but each of those has its pros and cons which effect the paste characterizations such as curing temperature, mechanical strength, and agglomeration of the particles.

Different types of high-temperature pastes are available such as Polysilazane (PSNB), alumina paste, etc. The PSNB is a high-temperature capable paste that can be synthesized by thermal decomposition of polymeric precursors or a pyrolysis (fire separation) process which requires temperatures around 1400°C, while the final ceramic (inorganic) paste cures at a lower temperature. The alumina-based ceramic paste consists of nano-AlN, nanosilica, and aluminum dihydric phosphate materials. Each constituent material has a different role in the paste synthesis process. For instance, nano-AlN has high thermal stability which can promote the phosphate reactions and it creates many NH_3 groups from which an excessive amount can result in higher paste porosity and lower mechanical strength [1-14].

1.2.3 Ceramic Drying Process

Drying is a complicated process in which three different factors are involved including solvent evaporation, shrinkage after curing, and pores change due to fluid flowing. There are two major steps in the drying process, a constant rate period (CRP) and the falling rate period (FRP). In the CRP the evaporation rate is close to a constant value while in the FRP, the evaporation rate reduces with time. For some materials, the FRP is divided into two parts, FRP1 and FRP2. In FRP1, the evaporation rate reduces linearly but in the FRP2 the rate decreases nonlinearly. Cracks

often result from an excessively high drying rate or cross-sections of the deposited material which are too thick. Cracks normally are observed at the critical point when the shrinkage rate reduces, and the liquid diffuses into the material. Cracking is generally the result of stresses introduced by a pressure difference in the paste materials [1-15].

The drying process is shown in figure 1.3. In the CRP, the liquid-vapor boundary's edge stays at the surface of the liquid. Evaporation happens at a rate equivalent to that of an open container of that liquid. The stages of drying are shown in Figure 1.3. Figure 1.3. (a) shows the initial stage. In figure 1.3. (b), which is CRP, the capillary tension expands in the liquid (paste's slurry). When it extends to decrease the solid phase exposure, the structure is pulled back to the paste's slurry. The structure at the beginning needs a little stress to keep it submerged. Figure 1.3. (c), shows the FRP of the material, where the liquid-vapor boundary diffuses toward the center creating empty pores [1-16].

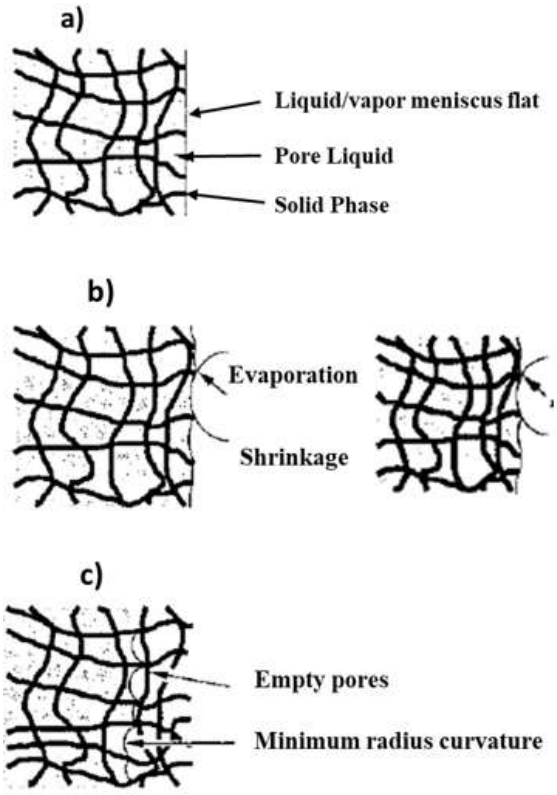

Figure 1.3. Different stages of ceramic drying a) Initial condition before evaporation, the meniscus (boundary's edge) becomes flat at this stage b) Constant rate period, capillary tension occurs in the paste's slurry c) During the FRP, liquid diffuses toward the center [1-16].

1.3 Electronic packaging

The purpose of electronic packaging is to create microsystems including optoelectronics, microelectronics, energy systems, and sensors. The electronic packaging connects devices (chips) and other components into the package or microsystem. The electronic packages usually operate at temperatures between 150°C-1000°C for different applications such as automotive and thermionic integrated circuits, for low and high-temperature applications, respectively. The main consideration for high-temperature electronic packaging is minimizing the mechanical stress which is generated by the Coefficient of Thermal Expansion (CTE) mismatches. With this in mind, a proper heat sink and heat dissipation system must be considered, which can match with the proper material. Finally, proper environmental protection (encapsulant) must be provided to the system [1-17].

The recent generation of the power electronic devices are made from wide-bandgap semiconductors, which allow for use in harsh environments and high-temperature applications of devices such as photovoltaics, sensing components, and automotive electronic systems. This is due to their wide-bandgap energy, outstanding thermochemical stability, and high dielectric strength. Using the high-temperature capable semiconductor devices requires less expensive and smaller cooling systems with higher reliability. A different part of the package must be evaluated for harsh environment exposure such as die-attach bonding strength, wire bonding, package housing, and encapsulation material reliability [1-18].

1.3.1 Die attach evaluation

The die shear test is one of the methods to evaluate the bond line mechanical strength which determines the integrity of die-attach materials. The die shear test measures the applied force to the die, versus the distance in which force was applied until failure occurs. Figure 1.4 shows how the shear tool approaches the die.

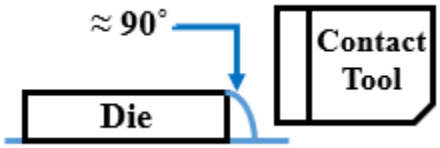

Figure 1.4. The shear tool should place across the side of the die and make a 90° angle with the substrate.

A shear strength test based on the MIL-STD-883 2019.9 method applies to the bond line interface, and it is corresponded to the measurement of applied force to the bond-line interface to evaluate the resulted failure modes. Referring to the MIL-STD-883 2019.9 method which is shown in Figure 1.5, all dice with areas larger than 63×10^{-4} IN^2 (4.13 mm^2) shall withstand at least a force of 2.5 kg. The die shear strength can be categorized into 3 levels according to MIL-STD-883 2019.9: poor (below the 1X line or 2.5 Kg-F) bond strength region, medium (between 1X (2.5 Kg-F) and 2X (5 Kg-F) lines) bond strength region, and excellent (more than 2X line or 5 kg-F) bond strength region. In this study the 2.6 mm × 2.6 mm die size was utilized which is 0.0676 mm^2 or 105×10^{-4} (IN^2) [1-19].

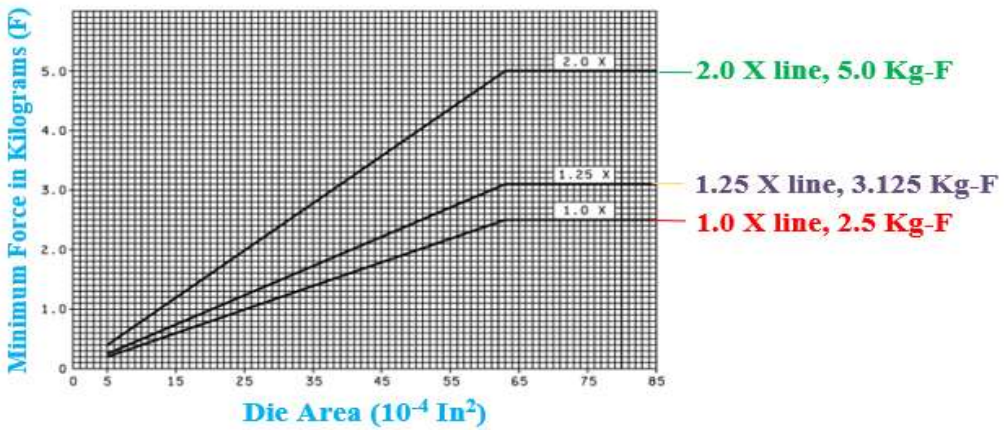

Figure 1. 5. Die shear strength diagram

1.3.2 Wire bonding mechanism

Wire bonding was introduced by Bell Telephone laboratories (in 1957) with well-known techniques of capillary- and wedge- based ball bonding. The physical attachment of the wire to the wire bond pads is called the joining process. The required energy is provided by a combination of force, temperature, and ultrasound. Combinations of these are now commonly called: Ultrasonic (US), Thermocompression (TC), and Thermosonic (TS). US bonding was initiated in 1960 and is a room temperature (RT) process utilizing both force and ultrasonic energy. In general thicker wire should be used (up to 500 µm) for high power density devices [1-20].

TC bonding was introduced in 1957 and requires a temperature around 300°C along with a mechanical force during the bonding process. The thermo-compression wire bonding is widely utilized for Au bonding and wedge-wedge bonding. The surface contamination highly impacts the bonding process. The TC bonding process needs high temperature and long process time to operate in comparison to other conventional methods. For example, when a gold wire with a diameter between 5 to 250 µm bonds to the pads using the TC bonding method, the bonding process take from seconds to minutes. A successful bond requires a substrate temperature between 200-300°C with a pressure between 35-70 MPa [1-21].

TS bonding was invented in 1970 and is a mixture of Thermocompression and Ultrasonic bonding. The TS bonding method is usually utilized for ball-stitch bonding of gold wires to various metallic pads. A combination of force, heat, and ultrasound introduces the required input energy level. The Thermosonic bonding of thin wires with a diameter between 18 to 50 μm is one of the commonly used and promising techniques in the Integrated Circuit (IC) industry [1-22]. To evaluate the wire bond strength, a wire pull test set up should be utilized. The MIL-STD method is used to evaluate the wire bond pull strength and the value is variable based on the wire bond material and size [1-23].

1.3.3 Encapsulation

The encapsulation process is a final step to protect the package from the outside environment. The encapsulation material should completely seal the electronic package to prevent the electronic components from interacting directly with the outside environment. Wire bonds, devices, and interconnects must be entirely contained within the encapsulation material. The encapsulation cover must be chemically and mechanically compatible with the chip and substrate. Figure 1.6 shows a schematic of encapsulated devices with chips on the substrate. Generally, the encapsulation is evaluated by examining flaws and cracks in the final encapsulation, which usually appear during the drying process [1-24].

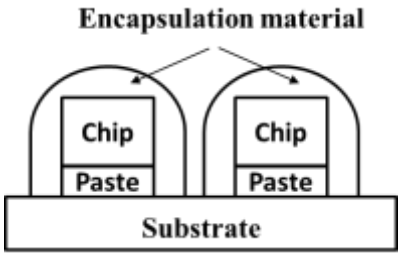

Figure 1.6. Illustration of the encapsulated component.

1.4 Dissertation Motivation

With the development of wide bandgap power semiconductors, the demand for high-temperature electronic packages has been increasing relentlessly. The current electronic packaging technology, just able to withstand up to 300°C, is not sufficient to operate in high-temperature applications such as Venus exploration at temperatures potentially reaching ~650°C, for example. Commonly used die-attach materials, such as nanosilver paste, are conductive and commonly have problems with thermo- and electro-migration resulting in the shear strength degrading after thermal aging at 500°C for 1000 hours [1-25]. Similarly, commonly used encapsulation materials, such as epoxy (polymer), can only withstand up to 300°C because of their organic bonding decomposition [1-26]. A significant goal of this research was to investigate the use of ceramic-based materials for both die-attachment and encapsulation to facilitate a high-temperature functioning electronics package.

Ceramic materials generally withstand higher temperatures, however, their effectiveness in die-attachment and encapsulation must be determined. Depending on the die and the substrate materials, the mechanical strength will different. Mechanical shear strength is evaluated by the MIL-STD standard test and the minimum shear strength value shall not be lower than 2.5Kg-F [1-9]. As a ceramic base for the tested materials, alumina ceramic paste has been synthesized. The novel idea was to add the nanosilica into the paste to improve the mechanical performance of the

die-attach significantly while improving encapsulation behavior by introducing fewer cracks and pores by optimization of the curing profile.

1.5 Dissertation Objectives

The overall objectives of this research were to develop the materials, processes, and integration technologies for high-temperature (>300^{o}C) electronic packaging for gallium nitride (GaN) and silicon carbide (SiC) devices. As such, several commercially available ceramic pastes were investigated to serve as the die-attach and encapsulation materials capable of high-temperature (>300^{o}C) operation. A custom ceramic paste was also synthesized, and its die-attach and encapsulation properties were compared to those of the commercial ceramic pastes. Finally, the integration of various packaging components such as substrate types, die-attachment materials, wire bonding materials and processes, and encapsulation materials and processes into electronic packages are investigated. Various criteria were used to evaluate the suitability of these packaging substrates, die-attach process, wire bonds, and encapsulations at high temperatures. Finally, as a practical application of the above results, a double-layer ceramic substrate was developed and tested.

1.6 Dissertation Organization

This dissertation is organized into five chapters. Chapter 1 introduces the motivations and objectives, background, and review of relevant literature for this dissertation research. Chapter 2 presents the journal manuscript for the application of alumina-based ceramic paste for high-temperature electronics packaging. Chapter 3 presents the journal manuscript for high-temperature electronics packaging for simulated Venus conditions. Chapter 4 presents the journal manuscript

for a high-temperature double-layered ceramic substrate for high-temperature packaging. Finally, chapter 5 summarizes the dissertation research and presents the research contributions.

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CHAPTER 2

Application of Alumina-based Ceramic Paste for High-Temperature Electronics Packaging

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2.1 Introduction

High-temperature packaging at or above 300^{o}C requires high-temperature capable die attach and encapsulation materials. One of the candidates for die-attach material is an alumina-based ceramic paste which is high-temperature capable (1300℃-1700°C), lead-free, inorganic, and electrically insulating. The inorganic alumina pastes have a high melting point, excellent bonding strength, and due to their non-toxic and nonpolluting characteristics, they are utilized for bonding ceramics, metals, and glass [2-1 - 2-3]. The alumina paste can be cured at room temperature, but the post-curing process increases the bonding strength and reduces the number of voids and cracks [2-4].

The corresponding curing temperature varies depending upon the molar ratio of aluminum dihydric phosphate /alumina (P/Al). The minimum curing temperature occurs with a P/Al ratio of 2.49 but by increasing the phosphate content, its porosity increases. Another type of room temperature cured paste contains a low melting point glass or glass powder [2-5] with an inorganic filler such as boron carbide (B_4C) [2-6]. Silicon Carbide (SiC) whisker (about 1 wt. %) with Aluminum Nitride (AlN) can be utilized to enhance the mechanical performance of the paste. An alumina paste was synthesized for ceramic-to-ceramic bonding using phosphoric acid (H_3PO_4) and aluminum hydroxide ($Al(OH)_3$) as the matrix and B_4C and silicon (Si) as the non-organic fillers. Yet, the shear strength was not high due to the room temperature curing [2-7].

There are different types of curing agents that can be added to the formulation, such as magnesium oxide (MgO), zinc oxide (ZnO), and cupric oxide (CuO). The MgO, when added as

a curing agent, improves the curing rate but the density of crosslink decreases which leads to the shear strength degradation [2-8]. The ZnO increases the shear strength but it increases the curing temperature [2-9] while nano-AlN (n-AlN) is alkaline which can promote the phosphate reactions and has strong thermal stability [2-10]. To increase the bonding shear strength, nano-silica can be added to reduce the curing tension and increase shear strength [2-11]. The n-AlN is a high thermally-stable material and is categorized as an alkaline material that can promote chemical reactions of phosphate material. The n-AlN can reduce the curing temperature, and that is because the aluminum dihydric phosphate ($Al(H_2PO_4)_3$) is acidic and the basicity of n-AlN can cause an acid-base reaction and can promote the reaction for phosphate formation. By increasing the n-AlN, the amount of Al^{3+} would increase in the paste material [2-12]. The n-AlN can be hydrolyzed easily and by increasing the Al^{3+}, the shear strength will be increased. On the other hand, by adding an excess amount of the n-AlN, many NH_3 groups will be formed which can cause a higher porosity rate and lower shear strength [2-4].

In this work, a ceramic paste material comprising of aluminum dihydric phosphate (binder) and alumina powder (filler) for high-temperature (300^oC – 500^oC) electronic packaging is synthesized and investigated as a die attach and encapsulation material. Nano aluminum nitride and nano-silica powders were embedded to promote its curing process, reduce its curing tension, and increase the bonding shear strength. Scanning electron micrographs show how these curing promoters affect the bond line and reduce voids and defects. The encapsulation process was investigated by optimizing the curing rate, time, and temperature which resulted in reducing the number of cracks and voids.

2.2 Materials and Methods

2.2.1 Materials Overview

The aluminum dihydric phosphate, aluminum oxide, nano-aluminum nitride, and nano-silica were purchased in powder form. Aluminum dihydric phosphate, $Al(H_2PO_4)_3$, was utilized as a binder material. The aluminum oxide powder (300 nm) was mixed with the $Al(H_2PO_4)_3$ as a binder. The alumina (Al_2O_3) powder and curing promoters (n-AlN and nano-silica) were mixed with solvent thoroughly in a high-speed disperser, then the binder was added, and the mixing process continued for at least 20 minutes. The slurry was heated for 40 minutes at 200°C. The ceramic synthesis process is demonstrated in Figure 2.1. Different percentages of nano-silica (5%, 10%, and 15 %) were added to the paste as a curing promoter to evaluate the bonding strength and encapsulation properties.

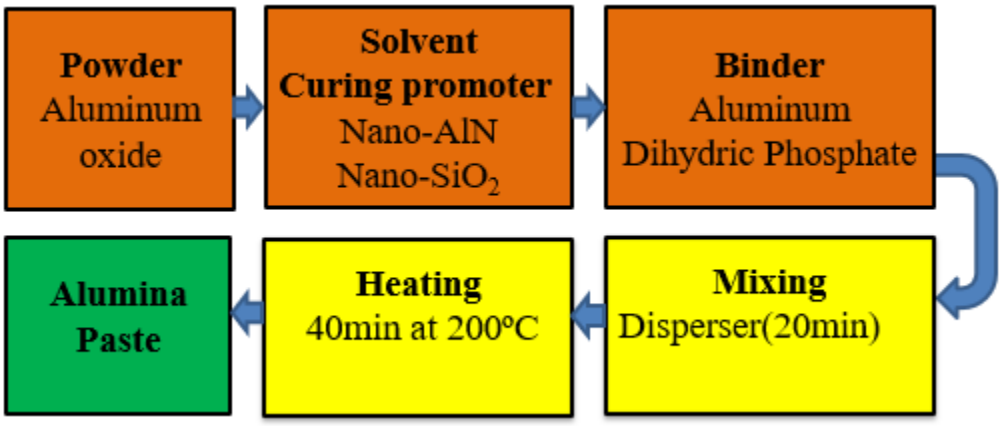

Figure 2.1. Ceramic synthesis process flow chart for synthesizing the alumina paste.

2.2.2 Experimental Procedure

The alumina powder and n-AlN (10 wt. %) were mixed with water as the solvent for 20 minutes. The mixing process is performed in a digital homogenizer and dispersing tool (IKA T-25 digital homogenizer) which operates at variable speeds in the range of 1000-20000 rpm. The

nanopowders must be mixed thoroughly to ensure that there are no agglomerated particles in the slurry to yield a homogenized and consistent paste. Different weight percentages (5%, 10%, and 15%) of nano-silica were added to the paste. Finally, nano aluminum dihydric phosphate powder (P/Al molar ratio of 1) which served as the binder material was added. The mixing process was continued for 30 minutes, then the slurry was transferred onto a hotplate and heated at 200°C for 40 minutes to yield a consistent alumina ceramic paste. Silicon (Si), silicon carbide (SiC), alumina, and gallium nitride deposited on sapphire (GaN/sapphire) dummy dice were attached to alumina packaging substrates. A dicing saw was used to dice the Si, SiC, and GaN wafers into dummy dice of 2.6 mm by 2.6 mm. After die and substrate preparation, the synthesized ceramic paste was screen printed using a metal squeegee onto the ceramic substrate through a mask.

2.2.2.1 Curing Profile

The ceramic paste curing temperature and rate affect its die attach bond strength as well as crack and voids formation in the encapsulation layer. A faster curing rate was found to introduce more voids and cracks. Different curing profiles have been evaluated with curing rates between 2°C/minute to 10°C/minute and curing temperatures of 200°C to 580°C.

2.2.2.2 Die Shear Test

The die shear test was carried out using a Dage 4000 shear and pull bond tester. This tester applies a horizontal force to the die under test until the bond fails to yield a peak force in Newton versus a horizontal distance plot.

2.2.2.3 Material Characterization

XRD analysis used to determine crystalline structures of the material while XPS was utilized to analyze the binding energy for each existing element. By XRD analysis and subsequent calculations, the crystallite size, lattice spacing, and lattice micro-strain are found. FTIR plots determined the infrared (IR) absorptions for each specific bonding at a certain wavenumber. The scanning electron microscope was used to observe the micro-topography and bond line quality of the material between the die and substrate. EDX mapping and diagrams can demonstrate the material distribution and percentage of each material in a specific area in the bond line.

2.3 RESULTS AND DISCUSSION

2.3.1 Effects of Curing Promoter on Bonding Strength

Ceramic pastes with 10% n-AlN and different percentages of nanosilica curing promoter were synthesized using 5 wt. %, 10 wt. %, and 15 wt. % of nanosilica. These synthesized pastes were screen printed onto alumina substrates using both the alumina and GaN/sapphire dice. The samples were sintered at three temperature stages: a binder burnout (110°C), a low-temperature soak (260°C), and isothermal sintering (372°C) and cooling. Figure 2.2 shows the curing profile for the synthesized paste.

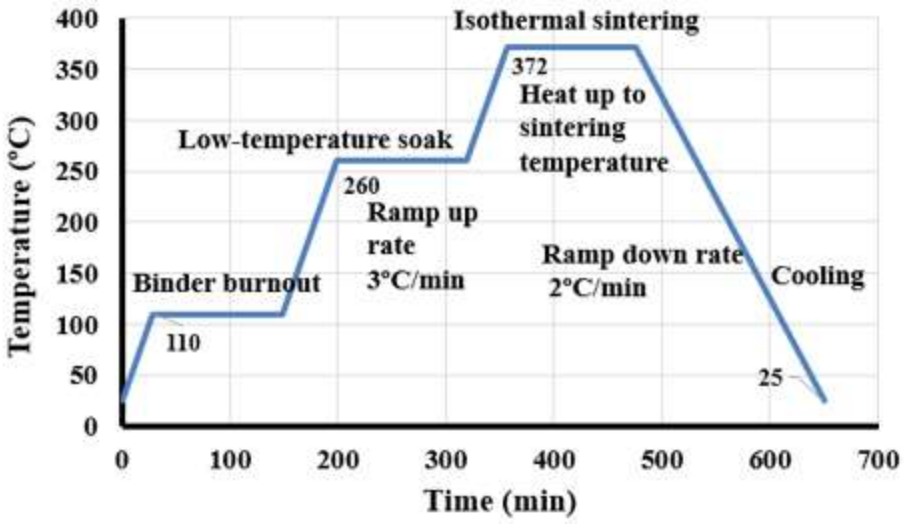

Figure 2. 2. The curing profile shows 2 hours soak at each temperature (110°C, 260°C and 372°C).

Since there is no high-temperature shear strength test standard, a shear strength test method based on the MIL-STD-883 2019.9 method was carried out on the bond line interface to determine the integrity of these die-attach bonds. This test is based on the measurement of applied force to the bond-line interface and evaluates the resulted failure modes. Based on the MIL-STD-883 2019.9 method, all dice with areas larger than 4.13 mm^2 should withstand a minimum force of 2.5 kg. The die shear strength can be categorized into 3 levels according to MIL-STD-883 2019.9: poor (<2.5 kg-F) bond strength region, medium (between 2.5 kg-F and 5 kg-F) bond strength region, and excellent (>5 kg-F) bond strength region. The die size used was 2.6 mm by 2.6 mm (or 6.76 mm^2), as such, all bonds that survived higher than a force of 2.5 kg satisfied the MIL-STD-883 2019.9 method.

Die shear tests were performed on the die attach samples using a ceramic paste with 0%, 5%, 10%, and 15% nano-silica added to the alumina paste. The average die shear strengths for this die attach samples are shown in Figure 2.3. The shear strength values of alumina dice (Figure 2.3(b)) were more than GaN/sapphire dice, this is due to higher CTE compatibility of alumina

dice with alumina-based ceramic paste and alumina substrate (96% purity) than GaN/sapphire dice. For both the alumina and GaN/sapphire dice, the 10% nanosilica addition to the ceramic paste yielded the highest shear strength which exceeded the MIL-STD-883 2019.9 requirements. As such, the 10% nano-silica ceramic paste has been chosen and additional experiments were conducted. The lowest standard deviation value represents more consistency in its corresponded data set.

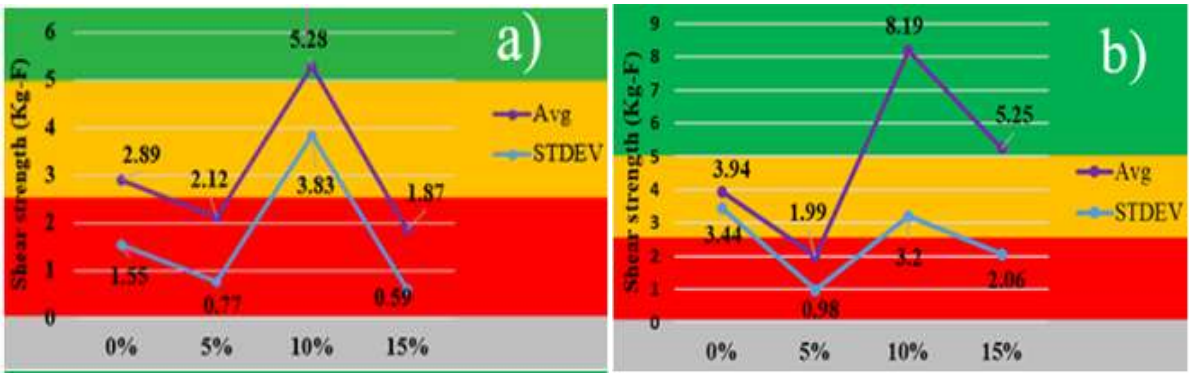

Figure 2. 3. Die shear strengths versus different weight percentages of nanosilica to the ceramic pastes (a) GaN/sapphire dice on a ceramic substrate and (b) alumina dice on the ceramic substrate.

2.3.2 Thermal Cycling

A 20-cycle thermal cycling test between room temperature and 500^{o}C was performed on the 10% nanosilica ceramic samples. After applying the thermal cycling, the shear strength test was performed on the samples. The shear strength values for the alumina and sapphire samples before and after thermal cycling showed a 22.2% and 62% decrease, respectively. For both the alumina and sapphire samples, the shear strength values were decreased after thermal cycling. However, the shear strength decrease in the sapphire samples was more significant than that of the alumina samples. The die shear strength decrease is due to the pile-up of creeping dislocations to form microcavities at the grain boundaries of the ceramic paste [2-13]. The microstructure and grain size of the alumina paste impacts the mechanical and dielectric properties. A smaller grain

size improves the mechanical properties including strength [2-14] wear resistance [2-15], hardness, and toughness [2-16]. The material's strength can be improved by controlling the grain size and limiting the movement of the dislocations. By giving enough thermal energy, dislocations move easily through the grain boundaries. In other words, grain boundaries stop dislocations from moving further. The smaller grain sizes yield a higher surface area over the volume ratios that demonstrate a higher ratio of grain boundary to imperfections. A higher number of grain boundaries result in higher shear strength. So, by having a larger grain size, dislocations have more freedom to move and this causes the shear strength degradation [2-17]. The grain growth depends on the temperature and annealing time. By increasing the annealing time and temperature, the grain size increases based on the Grain Growth Law as is shown in Equation (2.1) [2-18].

$$D^n - D_0^n = K_0 t\, e^{\frac{-Q}{RT}} \qquad (2.1)$$

Where D is the mean grain size, D_0 is the average size of the grain before heat treatment, n is the grain growth exponent, K_0 is Kinetic coefficient, t is the time, Q is the activation energy, R is gas constant, and T is the absolute temperature. The grain growth exponent was calculated to be about 2 [2-20]. By considering $\Delta D = D^n - D_0^n$ for the grain size change, and plug the values ($R=8.314$ J mol^{-1}, n=2, Q= 440 Kj/mol) into the Equation (2-1), the grain size change ratio for 100 hours thermal aging at 500°C (t=100 hrs., T=773K), over the grain size change with no thermal aging (t=100 hour, T=300K), yields a 10% increase in grain size. At the elevated temperature (500 °C), grain fusion yields lower surface energies and increasing the grain size.

The maximum diameter of the grain size (D_{max}) which is blocked by a spherical particle with a radius of r, is calculated by Zener-Smith equation (Equation (2.2)) where f is the volume percentage of each constituent in the paste mixture.

$$D_{max} = \frac{4r}{3f} \quad (2.2)$$

For alumina particles with a radius (r) of 150 nm and a volume fraction of 23.14%, the maximum grain size diameter was calculated to be 869.57 nm.

2.3.3 Thermal Aging

The alumina and sapphire samples were stored at 500ºC for 100 hours to evaluate their shear strength changes after thermal aging. Thermal aging was found to reduce their shear strengths but a smaller decrease in shear strength was found in the alumina samples than in that of the sapphire samples which could be due to the fact alumina die and the substrate has a perfect coefficient of thermal expansion (CTE) match. Generally, the thermal aging process affects the bond shear strength which could be due to increased grain size resulting in bond strength reduction. The shear strength value for the alumina and sapphire samples had 17.40% and 47% decrease, respectively, for the alumina and sapphire samples after thermal aging. The final bond shear strength of the alumina sample is higher than that of the sapphire sample after the thermal aging process.

The shear strength, degradation delamination, forming the crack and voids, could be linked to the imperfection of the ceramic materials. The SEM image (Figure 2.4) shows a synthesized alumina ceramic interface after 100 hours of thermal aging and 20 temperature cycles (a few examples of micro-crack are shown by red circles). A large number of micro-cracks have depleted the local regions and results in a failure mode in the bonding interface and encapsulated surface. There is a higher rate of microcrack in the center of the die-attach interface that is due to the paste in the center is heavily constrained by the top die and bottom substrate components. These aspects appear to be the major reason for shear strength degradation and

micro-crack formation. Also, another reason is the organic binder was trapped in ceramic paste during the curing process, and that may have increased the pore creation rate [2-20].

When ceramic die-attach is subjected to thermal cycling, by the interconnection of cracks and porosities the crack growth will be faster, and pores coalesce and grow to form microcracks. These cracks and porosities can cause shear strength degradation or delamination on the bonding interface. With higher pores and crack concentration at the bonding interface of the joint, the CTE mismatch can cause shear strength degradation. In addition to that, during thermal cycling, the material with different CTE expands differently than adjacent materials. In thermal cycling hold time (90 seconds at each temperature peak) the ceramic paste is constrained under the top die, while during the cooling-down or heating-up steps, high strain and constraint happen due to the CTE mismatch. The predicted CTE for the synthesized alumina paste is about 8.08×10^{-6} °C^{-1}) while the CTE value for alumina and sapphire are 7.9×10^{-6} °C^{-1}and 7.6×10^{-6} °C^{-1} respectively [2-21, 2-22]. All the aforementioned factors can degrade the shear strength and interface quality after thermal reliability tests.

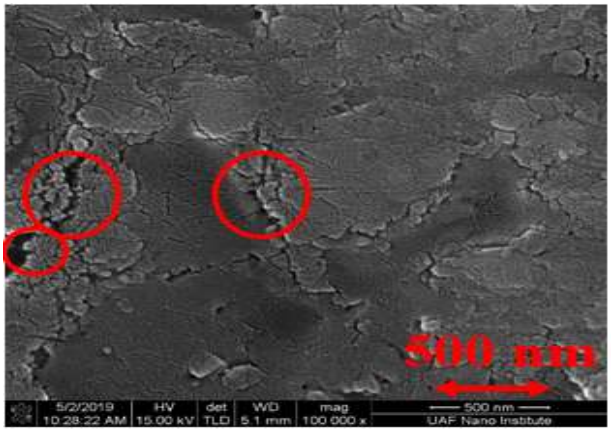

Figure 2. 4. SEM image from the ceramic interface after 100 hours of thermal aging at 500°C and 20 temperature cycles.

2.3.4 Structural Properties

2.3.4.1 XPS Analysis

X-ray photoelectron spectroscopy (XPS) test was carried out on fired alumina paste samples. Figure 2.5(a) shows the intensity versus binding energy (eV) for the ceramic sample without nanosilica and a 10% nanosilica ceramic sample. As can be seen, the 10% nanosilica fired ceramic paste has a higher oxygen count than the sample without nanosilica. Figure 2.5(b) shows the overall percentage of each element for the ceramic samples without and 10% nano-silica. The oxygen percentage for the 10% nanosilica ceramic sample is 75% versus 65% for the ceramic sample without nano-silica. It was found that the binding energies for oxygen closely matched those for the hydroxide bonding and while the binding energies for aluminum closely matched those for AlOOH (boehmite) and Al_2SiO_5 (sillimanite) which indicates the presence of the alumina-silica bonding [2-23].

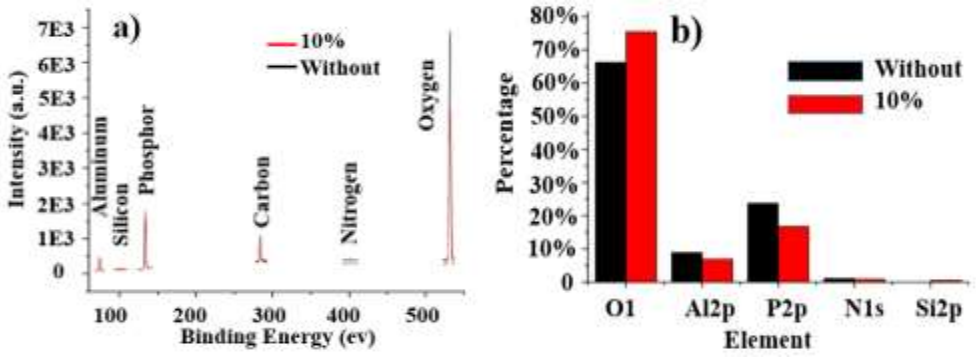

Figure 2. 5. (a) Intensity versus binding energy (eV) for the ceramic sample without nanosilica and a 10% nanosilica ceramic sample, (b) Overall percentage of each element for the ceramic samples without and 10% nano-silica.

2.3.4.2 XRD Analysis

X-ray diffraction is to investigate a change in structural properties caused by embedding nanosilica into the alumina paste. A Miniflex diffractometer with Cu K_α X-ray source (λ=1.5406Å) was used. Figure 2.6 shows the XRD plots for several ceramic samples with and without

nanosilica. Nano-silica and alumina peaks are used to calculate the crystallite size, lattice spacing, and crystal microstrain. The corresponding lattice orientations (Miller indices) for nanosilica and alumina are 23.02° and 58.10º for (001) and (116) planes, respectively [2-24,2-25]. The peak positions shift along with broadening with the addition of the nanosilica. The peak broadening for the 10% nanosilica ceramic sample is larger than those for other samples which means that a smaller crystallite size is present in the 10% nanosilica sample. The smaller grain boundaries limit the dislocation (imperfections) movement and have a higher surface area to the volume ratio which yields a higher ratio of grain boundary to imperfections. As such, a smaller grain (crystallite) size yielded a higher mechanical strength [2-26]. Figure 2.6 shows the XRD peak broadening of alumina powder due to adding the nanosilica. The full-width half- maximum (FWHM) was calculated by using Origin© graphing and analysis software. It was found that the peak broadening (FWHM) of 10% nanosilica is higher than those of other samples**.**

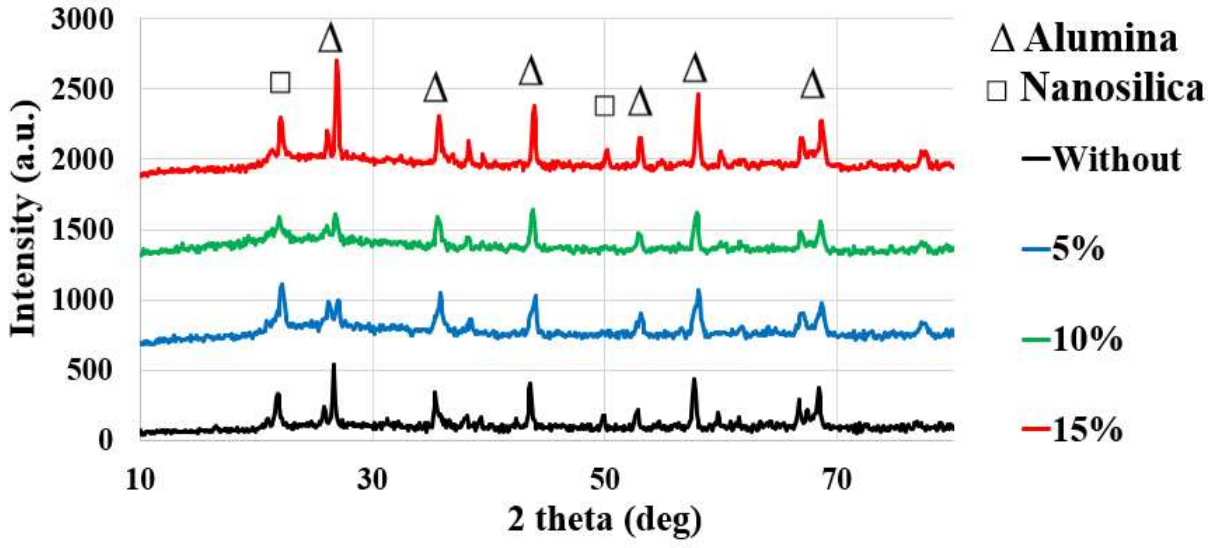

Figure 2. 6. XRD plots for different nano-silica percentage samples.

2.3.4.3 Crystallite Size

By adding nanosilica to the ceramic paste, the crystallite size becomes larger. However, the crystallite size for the 10% nanosilica ceramic paste remains smaller. The smaller crystallite size or grain size may make a higher bonding strength with adjacent crystals [2-26]. The crystallite size changes as nanosilica are added to the alumina paste. Figure 2.7 shows the nano-silica and alumina crystallite size had a minimum value for the 10% nanosilica samples. The crystallite size can be calculated from Equation (2.3) using the Scherer equation [2-27].

$$\tau = K\lambda / B(2\Theta)\cos\Theta \qquad (2.3)$$

where $B(2\Theta)$ is FWHM of the peak at the Bragg angle Θ, and λ is the wavelength of x-ray which was CuKα radiation and the wavelength value is 1.5406 Å for this specific source. τ is the crystal size in nanometer and K is a shape factor with a value of 0.94. The maximum peak position for the nano-silica and alumina powders are 2Θ=22.8596 and 2Θ=58.0994, respectively, with different FWHM values for each sample.

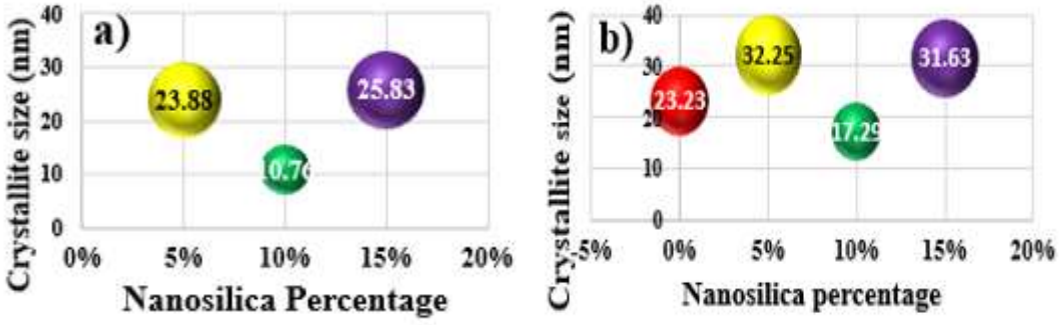

Figure 2. 7. (a) nanosilica crystallite sizes versus nanosilica percentages, (b) alumina crystallite sizes versus nanosilica percentages.

Adding highly stable additives such as oxide, carbide, and nitride can be an effective method to reinforce the chemical reactions in nanostructured materials and act as an effective barrier for dislocations and grain boundaries from additional movement. Intrinsic stability of the nanoscale grain size of the material is due to some structural factors such as low energy of grain

boundaries, the physical structure of grain boundaries, porosity, and so on [2-28]. Nano-structured materials have a large grain boundary area that results in large stored energy. This tends to make the material unstable during grain growth under high-temperature thermal testing. The suppression of grain growth and the densification of the film can be achieved by kinetics changes between grain boundary migration and diffusion. Different factors affect the grain growth rate, such as grain boundary energy, instantaneous grain size, thermal stability, the activation energy of the grain growth, annealing temperature, the driving force (a pressure difference created by curved grain boundaries to yield a free energy difference), etc. [2-29]. The grain growth is driven by the excess stored energy in the grain boundaries that provide the driving force for the grain growth (ΔG) based on Equation (2.4) [2-30]

$$\Delta G = \frac{3.3\gamma}{D} \tag{2.4}$$

Where γ is the specific grain boundary energy and D is the grain diameter. The thermal stability of nanostructured materials is divided into two approaches, thermodynamic and kinetic approaches. In the thermodynamic approach, by reducing the grain boundaries energy, the driving force of grain growth is lowered according to Equation (2.4). In the kinetic approach, a drag force applied by additives (nanosilica in this case) to migrating grain boundaries and limit their movements [2-31]. The improvement in thermal stability is accomplished by adding additives that hinder grain growth and recrystallization of nanomaterials at elevated temperatures [2-32]. The crystallite or grain size at the 10% nanosilica sample is minimized than other nanosilica percentages. This can be explained by the grain boundary energy which is minimized at 10% nanosilica samples to result in a lower grain growth rate. Also, the nanosilica additives exert a driving force to the grain boundaries to constrain grain growth [2-33].

2.3.4.4 Lattice Microstrain

The crystallite size change introduces micro-strain to its crystal structure. Micro-strain is the lattice strain caused by a displacement of the unit cell from their original positions. The 10% nanosilica sample has a maximum micro-strain due to the crystallite size change. Generally, the micro-strain broadening is produced by dislocations, surfaces, and domain boundaries. The micro-strain or internal strain is common in nano-crystalline materials and can be calculated from Equation (2.5) [2-34]:

$$B(2\Theta) = 4\varepsilon \frac{\sin\theta}{\cos\theta} \quad (2.5)$$

where B is FWHM (deg) and Ɛ is the micro-strain at a specific Bragg's angle, Ɵ. The calculated micro-strain for alumina and nanosilica materials is shown in Figure 2.8, the micro-strains in the 10% nanosilica samples for both nanosilica and alumina crystallites are maximum compared to those samples with 5% and 15% nano-silica. This can of the 10% nanosilica samples.

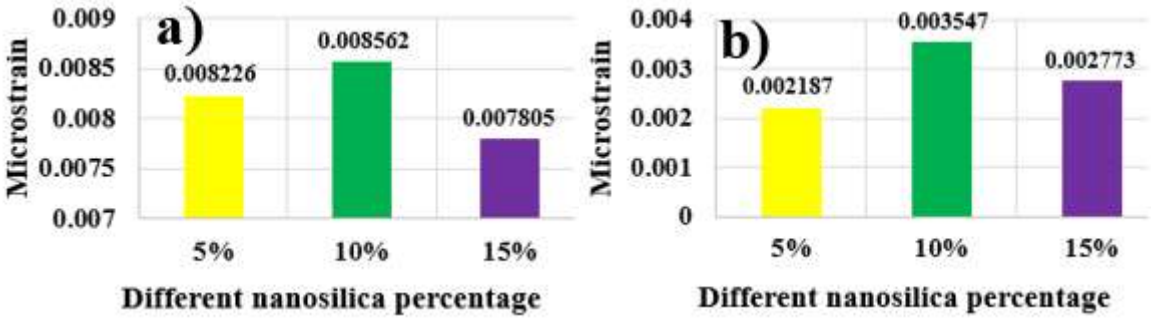

Figure 2. 8. (a) Microstrain in the nanosilica crystallites versus nanosilica percentages, (b) microstrain in the alumina crystallites versus nanosilica percentages.

2.3.4.5 Lattice Spacing

The diffraction peak position is due to interplanar spacing, and the lattice spacing varies because of the defect concentration changes. The lattice spacing can be calculated from Equation (2.6) using Bragg's law [2-35]:

$$\lambda = 2d_{hkl} \sin \Theta \quad (2.6)$$

The Miller indices (hkl) for nano-silica and alumina powders for 23.02° and 58.10º are (001) and (116), respectively. The lattice spacing (d_{hkl}) is calculated for each sample and the results are shown in Figure 2.9. The lattice spacing is maximum for the 10% nanosilica samples due to the peak shifts at Θ position.

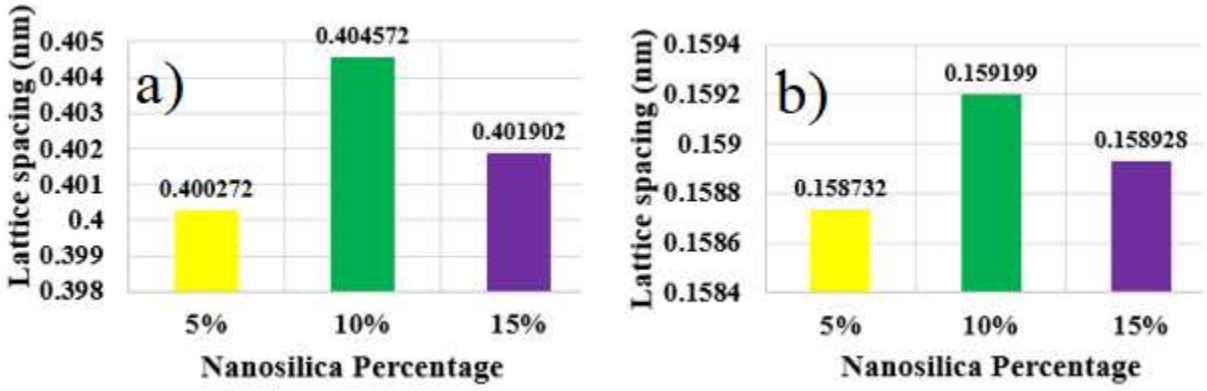

Figure 2. 9. (a) Lattice spacing for nanosilica versus nanosilica percentages, (b) Lattice spacing for alumina versus nanosilica percentages.

2.3.4.6 FTIR Analysis

The transmittance FTIR spectra of different synthesized samples are presented in Figure 2.10. The region from 400-1200 cm^{-1} corresponds to the asymmetric stretching of Si-O-Si or Si-O-. As shown in Figure 2.10, the associated peak intensity of the IR absorption is highest for the 10% nano-silica ceramic sample. The absorption peak observed at 472 cm^{-1} is associated with the deformation mode of Si-O-Si [2-36]**.** The band at 470 cm^{-1} is the characteristics of the Si-O bonds of amorphous silica [2-37]. The stretching and bending modes of the Al-O are supposed to be in the region of 500-750 cm^{-1} and 330-450 cm^{-1} [2-38], consequently. Meanwhile, the absorption peak at 618 cm^{-1} corresponds to Al-O (e.g., AlO_6) while the band around 731 cm^{-1} could be due to

AlO_4 [2-39]. A shoulder is observed in the 870-890 cm^{-1} wavenumber which is due to the bending vibration of the Si-OH groups [2-40]. A shoulder at 1170 cm^{-1} indicates that the alumina-silicate bonding has been formed due to ($3Al_2O_3$-$2SiO_2$) or ($2Al_2O_3$-SiO_2) compositions [2-41].

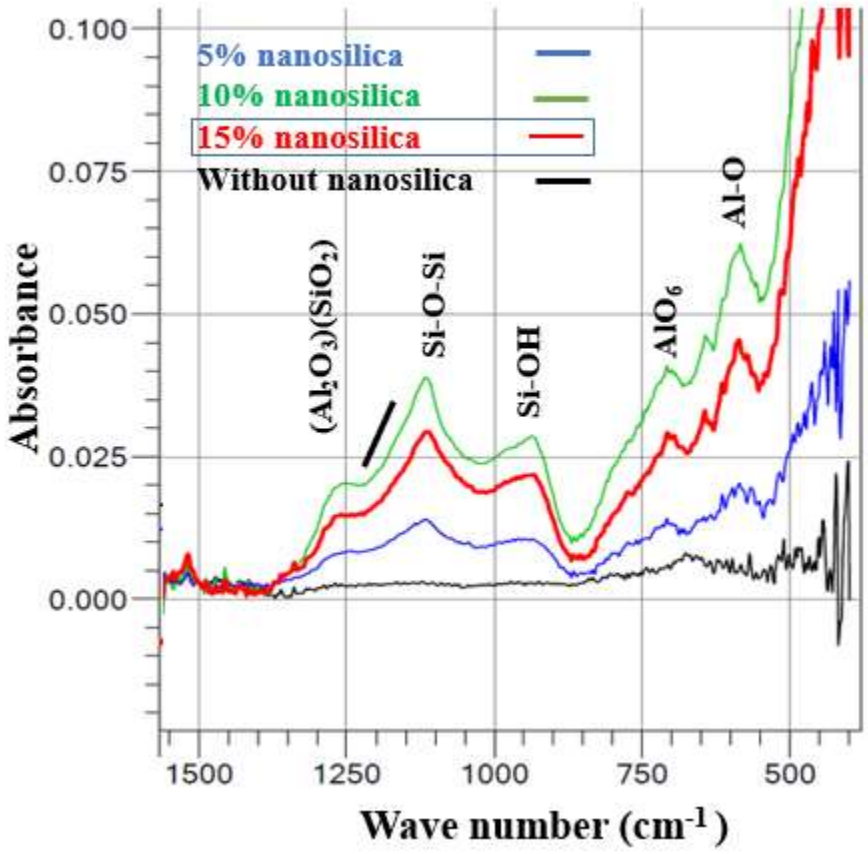

Figure 2. 10. FTIR absorption spectra of samples without, 5%, 10%, and 15% nano-silica.

2.3.4.7 Encapsulation Properties

Properties of encapsulant in packaged electronic devices are critical for environmental protection during their operating life. Ceramic materials are good candidates for encapsulation for high-temperature applications. Several commercial ceramic paste materials are available, but they suffer from cracking during curing. There are several potting compounds (encapsulation materials) that can be used as an encapsulation material but there were several issues after the curing process, while each one has its drawbacks after the curing process. Some of these encapsulation materials

pulverized after physical scrubbing while others introduce uneven surface after curing. Some of them introduce surface voids with visible cracks. The reason for crack formation could be CTE mismatches, especially with a thicker encapsulation layer. The curing rate also has a crucial role in the cracks and voids formation. By reducing the curing rate, the number of cracks was found to reduce.

Alumina pastes with different nano-silica percentages were synthesized and dispensed onto the alumina and gold-alumina substrates as an encapsulation layer. A larger encapsulation surface area is expected to introduce more cracks to the paste after curing. Figure 2.12(a) shows crack formation after the curing process when a commercial ceramic paste was used as the encapsulation material on an alumina substrate. Figure 2.12(d) shows the encapsulation with the 10% nanosilica ceramic paste on the gold-coated alumina package with KOVAR leads. As can be seen, a uniform encapsulation surface with no significant defects was observed on the 10% nanosilica encapsulated package.

2.4.8 Micromorphology, SEM and EDX Analysis

The bond lines between the die-attach and substrate as well as between the die and die-attach were observed by the Scanning electron microscope. For non-conductive samples, a metal, usually, gold or titanium, is sputtered to enable electron conduction at surfaces. The die-attach samples are embedded into a white clear resin and cured at 50ºC for 8 hours. Then they are cut using a low-speed saw right at the edge of the die/substrate bond line. The cut cross-sectional areas are then polished using diamond polishing powders of diameters 45µm, 9 µm, 6 µm, 3 µm, and 1 µm size in suspension at different polishing speeds. The cross-sectional images were taken from the bond lines to show the bond line uniformity and thickness. Surface voids were visible on the cross-section but microscopic voids can only be visible after finer polishing. The bond line

thicknesses are in the range of 20 µm to 50 µm. Figure 2.11 shows the bond-line thickness and uniformity for one of these die-attached samples.

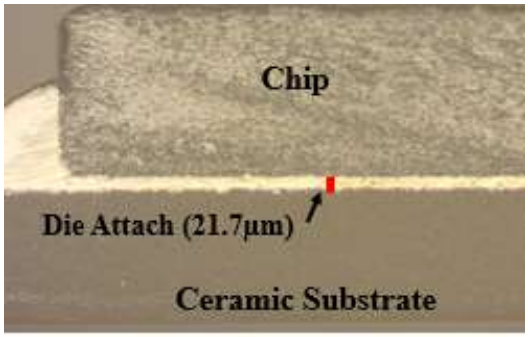

Figure 2. 11. Bond line thickness and uniformity.

After the 1 µm grade polishing step, a 4 nm platinum was sputtered onto the samples. Different nano-silica weight percentage samples were prepared, and SEM pictures were taken at their cross-sectional areas. Figures 2.12(b) and 2.12(c) show the SEM micrographs for the sample without nano-silica. Voids and defects can be seen within the ceramic die-attach (the voids are shown by the arrows).

The 10% wt. nano-silica die-attach with alumina die had a more uniform bond line with fewer voids and defects. Figure 2.12(e) shows the die attach with lesser voids and cracks and Figure 2.12(f) shows the bond line image and its uniformity. A color change is observed in the bond line and it can be explained by polymer resin residue shown in the bond line. The shiny edge of the bond line can be explained by surface transfer reflection because all surfaces might not be leveled, and it shows as white lines in SEM images. When 10% nano-silica was added as a curing promoter to the ceramic paste, the curing tension reduces which results in fewer voids and cracks in the die attach [2-42].

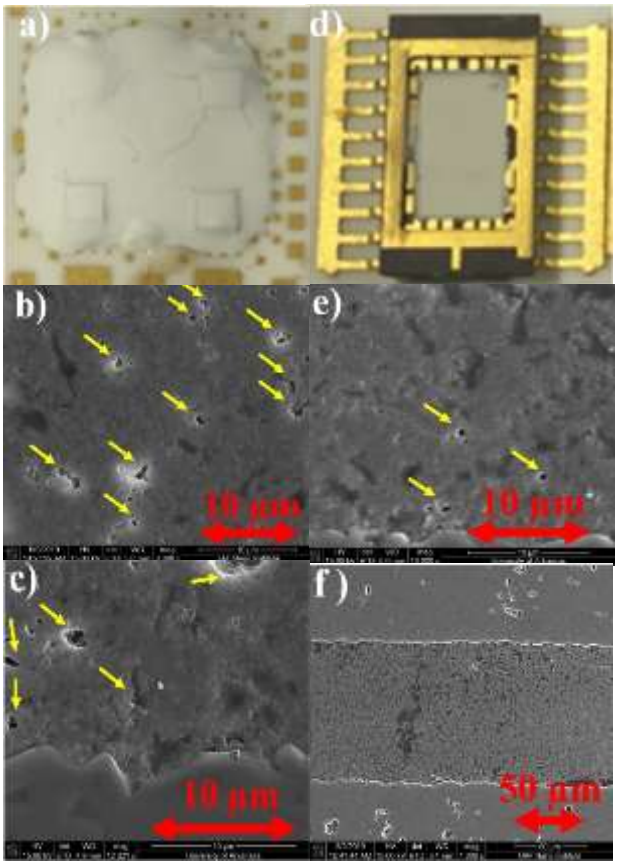

Figure 2. 12. (a) Ceramic encapsulation with a commercial ceramic paste on the alumina substrate, (b) and (c) SEM micrographs of the sample without nanosilica, (d) Ceramic encapsulation with a gold alumina package encapsulated with the 10% nanosilica ceramic paste, (e) Die-attach material with lesser voids and cracks for 10% nanosilica sample, (f) Bond line image and its uniformity for 10% nanosilica sample.

2.3.4.9 EDX Analysis

EDX point mapping results show the amount of material in bond line cross-section. The highest percentage compositions are attributed to aluminum, and oxygen, after carbon which normally exists in the material when exposing to a high-temperature. The EDX mapping shows the distribution of materials in the 10% nano-silica samples. The amount of silicon is not significant compared to other elements due to the low weight percentage of nanosilica than the other elements. Figure 2.13 shows the EDX mapping of each element and intensity diagram. The EDX map shows a uniform distribution of Al, Si, and oxygen in the bond-line area.

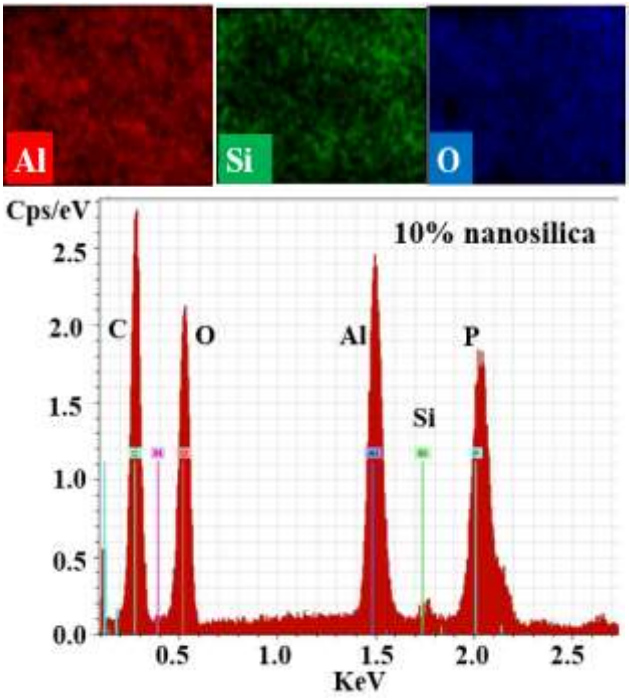

Figure 2. 13. EDX test summarized the material percentage on the bond line for 10% nanosilica sample.

2.4 CONCLUSIONS

This work addressed the high-temperature ceramic paste for high-temperature (300-500ºC) electronic packaging applications. Die-attach and encapsulation materials have been synthesized using alumina powder, n-AlN (10%), and aluminum dihydric phosphate with various curing promoter percentages (0, 5, 10, and 15% wt.) of nanosilica. The samples which contain 10% nanosilica exhibited a higher bonding strength and bonding quality than other percentages. Sintering or curing profile, heating, and sintering temperature, and curing rate have important roles in the die-attach bonding and encapsulation quality. A lower curing rate (2-3ºC/min) has been shown to yield better bonding quality and fewer voids/microcracks when applied as an encapsulant to electronic packages. Thermal cycle tests were performed from room temperature to 500ºC for 20 consequent cycles and thermal aging was performed at 500ºC for 100 hours on the alumina and sapphire die samples. Both samples exhibited a decrease in their die shear strengths after thermal

cycling (22% and 62% decrease for alumina and sapphire dice) and thermal aging (17.40% and 47% decrease for alumina and sapphire dice).

The 10% nanosilica-alumina paste yielded the best encapsulation properties with fewer cracks, voids, and surface defects. XPS results revealed a higher oxygen bonding percentage in the 10% nanosilica sample than the sample without nanosilica and the binding energy also shows a possibility of the formation of the alumina-silicate bonding. XRD results showed a shift in elemental peak positions when nanosilica was added to the ceramic paste. The peak broadening is the largest (for alumina and nanosilica) at 10% nanosilica sample which resulted in smaller crystallite sizes. The larger lattice spacing for alumina for the 10% nanosilica sample introduced a larger microstrain to its crystal structure. FTIR results showed the presence of alumina-silicate bonds on these samples with the largest amount present in the 10% nanosilica samples. Si-O and Al-O bonds were observed in these 10% nanosilica samples. SEM and EDX results showed a uniform bond line for the 10% nanosilica sample and uniform material distribution in EDX mapping. The number of voids was found to be higher in die-attach samples with no nano-silica.

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CHAPTER 3

High-Temperature Electronics Packaging for Simulated Venus Condition

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3.1 Introduction

Missions to hot planets and surfaces (e.g. Venus, Mercury) require resilient electronics that can process, amplify, and transmit valuable scientific data under extreme conditions. The desired lifetime for Venusian surface probes and landers is 1440 h or 60 d, but the longest surviving Venera 13 lasted only 127 min on Venus before capitulating to the extreme Venusian surface environment [3-1]. In addition to the electronics themselves, the electronic packaging (comprising of the package body/housing, substrates, interconnect, and passivation/encapsulation) must survive the chemical attack from harsh weather conditions (e.g., sulfur haze and clouds). As a result, new material platforms that utilize thermally stable and weather-resistant packaging architectures are required for extended operation within the Venusian environment.

The objectives are to develop a 500°C capable electronic packaging architecture using wide bandgap semiconductor devices such as gallium nitride (GaN) and silicon carbide (SiC) devices. Besides hot planet exploration, the maturation of this high-temperature packaging technology supports numerous commercial industries such as oil and gas exploration, geothermal energy production, and nuclear energy. The electronics and packaging technology currently used in these commercial sectors are often limited by operation limits of silicon-based electronics (typically rated to below 200 °C) and the cost of complex packaging schemes [3-2].

There are various types of substrates for high-temperature applications. Low temperature co-fired ceramics (LTCCs), high-temperature co-fired ceramics (HTCCs), and high-purity (96-

99.99%) alumina substrates are commonly used substrates for high-temperature applications [3-3]. Each substrate has its advantages and disadvantages such as different parasitic noises, dielectric constants, and conductivities at high temperatures. The advantage of LTCC alumina is its low co-firing temperature (~875ºC) and many choices of electrical conductors for the co-firing process. However, the LTCC and HTCC alumina contain glass constituents to allow the co-firing process with a conductor at a temperature below the alumina sintering temperature [3-4]. These glass constituents cause the dielectric constant to increase at high temperatures. The high purity alumina and HTCC substrate have smaller dielectric and conductivity changes at temperatures above 400ºC. The dielectric constant of the LTCC alumina substrate is less than that of 96% alumina substrate from room temperature to 300 ºC, but it drastically increases above 300 ºC which makes it undesirable as a high-temperature substrate beyond 300°C [3-5]. As such, the 96% alumina substrates as well as the HTCC has higher dielectric performance at higher temperatures as high-temperature substrates [3-6].

An un-encapsulated HTCC alumina package with platinum metallization was developed and tested in the simulated Venusian environment in [3-7]. The package electrical insulation resistance was found to substantially degrade due possibly to surface contaminations [3-8]. This work reports on a high-purity (96%) alumina packaging substrate with screen-printed gold conductors encapsulated with ceramic encapsulation.

The investigation begins with the processing of high purity alumina substrates capable of surviving the 500°C caustic environment. Next, die-attach materials such as thick-film gold and alumina-based ceramic pastes were evaluated. Gold wire bonds were used to electrically connect the various electronic dice and packaging substrates. Some of the devices on the packaging substrates were encapsulated by a glob-top ceramic encapsulation. The high-temperature

packaging substrates, with and without encapsulation material, were exposed to 500°C for at least 100 hours as well as thermal cycling from room temperature to 500 °C. These packaging structures were further exposed to a simulated Venus environment test chamber at 465 °C, 96 bar in a CO_2 environment. The test results showed that these packaging materials survived the simulated Venus's surface environment for up to 244 hours. A titanium package to house the high-temperature packaging substrates were fabricated to provide electrical interfaces to the package.

3.2 Experimental Approach

3.2.1 Materials Used

Gold pastes used in this investigation were 8835 gold cermet conductor (ESL 8835 (520C) 9802A, Electro-Science Laboratories, king of Prussia, PA, USA) and 3066 fireable gold thick-film paste (3066/3068N Wire-Bondable Au Conductors, Ferro Corporation, Mayfield Heights, OH, USA). The 98% alumina substrates were purchased from CoorsTeK (CoorsTeK Inc., Golden, CO, USA), and high-temperature alumina-based ceramic adhesives were purchased from Cotronics (3000°F - RESBOND^{TM} 989F Pre-Nano Adhesive, COTRONICS CORP, Brooklyn, NY, USA) and AREMCO (503VFG(very fine grain), Aremco Products, Inc., Valley Cottage, NY, USA). A custom-synthesized ceramic paste was also developed in this investigation [9]. Gold bond wires of 1-mil diameter were purchased from AMETEK (Coining Inc., Montvale, NJ, USA). Ultra-corrosion-resistant grade 2 titanium bars were purchased from McMaster-Carr (tested and certified by Titanium Processing Center, New Baltimore, MI, USA). Packaged samples were tested in a high pressure/high-temperature vessel (500ml, 289 bar at 600°C, series 4650, Parr Instrument Company, Moline, IL, USA).

3.2.2 Test Die Preparation

To evaluate the packaging substrates, different types of dice were prepared. Wide- bandgap gallium nitride (GaN) on sapphire and silicon carbide (SiC) dice capable of high-temperature operation were diced into 2.6 mm x 2.6 mm as test dice to evaluate their die-attach shear strengths, wire bond integrity, and daisy-chain resistance between dice. Since GaN can also grow on silicon substrates, the silicon (Si) dice were also evaluated.

3.2.3. Substrate Process

The 3066 gold paste was screen-printed onto the alumina substrate using an aluminum frame mesh screen to create the gold interconnects for interconnecting various electronic components. After screen-printing, the 3066 gold paste interconnects were cured at 850 ºC for 15 minutes. After firing, the thickness of gold conductors on the alumina substrate was about 10-15 µm.

3.2.4. Die Attach Process

After screen printing the 3066 gold paste, the substrate is ready for the die-attach process. The die-attach material was screen printed on the top of gold pads for the die-attach process. Different types of pastes were evaluated, but alumina ceramic pastes (989F and 503VFG) and 8835 gold paste were selected. The alumina ceramic paste was screen printed onto the substrate (Figure 3.1(a)). After paste screen printing, test devices were placed directly with a pressure of 4 bar onto the die-attach material. The die-attach materials were then cured based on the curing profiles corresponding to each paste. Figure 3.1(b) shows a TiNiAu resistor on alumina die which was attached to the substrate.

The recommended application method for the 8835 thick-film gold die-attach paste with a viscosity of 325 Pa.s is to use a screen of 325µm mesh window. After printing, the paste was left to level itself for about 10-15 minutes, followed by a drying process at 125ºC for 10-15 minutes. The optimum sintering temperature was 580°C with a temperature ramp rate of 25ºC/minute. The thickness of the fired die-attach was about 20-30 µm. Ceramic pastes 503VFG and 989F were selected due to their high shear strengths with the alumina substrate, high-temperature capabilities (1650°C), similar coefficients of thermal expansion (CTE), and fewer voids and crack formation on cured ceramic film. The 503VFG ceramic paste had a curing profile of 1 hour at room temperature followed by 2 hours curing at 94°C, 260 ºC, and 372ºC temperatures in sequence. The 989F alumina paste (600nm particle size) is a combination of ultra-fine alumina with high-temperature colloidal ceramic binders and has a lower curing temperature than 503VFG due to its constituents and solvents.

The 989F alumina paste required a room temperature cure for at least 4 hours followed by 2 hours to burn the binders at 65ºC and 4 hours of sintering at 200ºC. The ramp rate during curing was very important to achieve a desired thick film quality and to mitigate crack and void formation. A lower ramp rate yielded slower solvent evaporation and fewer voids on the ceramic film. The optimized temperature ramp-up and ramp-down rates were 3-5ºC/minute.

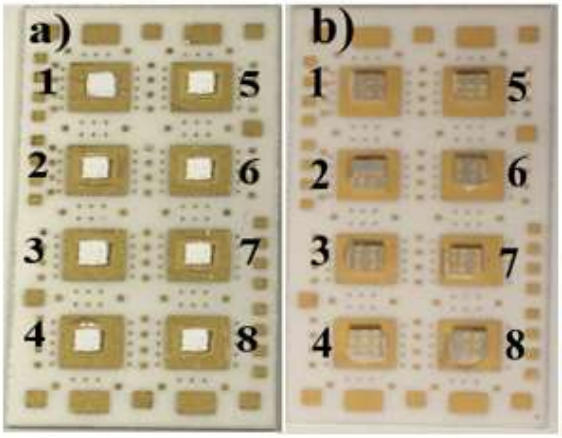

Figure 3. 1. (a) Gold thick-film pads on alumina substrate followed by ceramic paste printing. (b) Test chips attached to the substrate.

3.2.3 Wire Bonding

A K&S 4700 wire and ball bonder were used to form the wire bonds between the test devices and the substrate. Gold bond wires with a diameter of 1 mil were used to make the electrical connections between the daisy chain interconnection patterns on the substrate and the test devices. The wire bonding process used a thermionic wire bonding at 160ºC with ultrasonic energy between 10-15W. The bond wires made connections to the gold metalized pads on the test devices. The wire bond resistance changes were measured using a BK precision model 880 LCR (stands for inductance (L), capacitance (C), and resistance (R)) meter to assess the reliability of these wire bonds before and after environment tests.

3.2.4 Corrosion and Dielectric Test

Some of the substrates were encapsulated using ceramic material to evaluate its encapsulation property under a corrosive environment. An acid immersion test was conducted using 80% and 95% wt. sulfuric acid. For the acid test, a wire-bonded gold-alumina package was encapsulated using the ceramic encapsulation. The wire bond resistances were measured before and after a 24-hour acid immersion.

3.3 Results and Discussion

3.3.1 Die-attach Evaluation

Die shear tests using a Dage 4000 die shear and wire pull tester were used to evaluate the integrity and quality of the die-attach samples. Since there is no existing standard for die shear

strength at 500°C, the MIL-STD-885 2011.9 method was adopted instead. For this test, both the gold thick-film and ceramic die attach pastes were screen printed onto the alumina substrates (bare alumina without the gold metallization). The die shear test was based on the measurement of the applied force perpendicular to the side of the test device to assess different failure modes. Based on the MIL-STD method, all devices with a surface area of 64×10^{-4} in^2 and larger should withstand at least 2.5 kg-F. The die shear strength values versus die area are categorized into three shear strength levels: poor (<2.5 kg-F), medium (between 2.5 kg-F and 5 kg-F), and excellent (>5 kg-F). In our studies, a die shear strength between 2.5 kg-F and 5 kg-F was considering acceptable since our device size was 2.6 mm x 2.6 mm or 105×10^{-4} in^2. A Parr Instruments Model 4650 non-stirred high-pressure and the high-temperature vessel was used to simulate the Venusian environment. This vessel has a 500-ml chamber with a maximum temperature of 600ºC and a maximum pressure of 6000 psi (413 bar).

Cotronic's 989F, AREMCO's 503VFG, and Electro science's 8835 gold thick-film were selected as the die attach materials due to high shear strength and CTE compatibility with die/substrate material. Alumina, sapphire, Si, and SiC test dice were attached to the unmetallized die-attach sites using these die-attach materials. These samples were placed in the Venus simulator at a temperature of 460ºC at 96 bar pressure in CO_2 ambient for 150 hours. Die shear tests were performed before and after the chamber test at room temperature and the results are summarized in Figure 3.2. The 8835 thick-film gold paste die-attach yielded the highest shear strength with the alumina (20.74 kg-F), sapphire (10.74 kg-F), and Si (14.15 kg-F) dice.

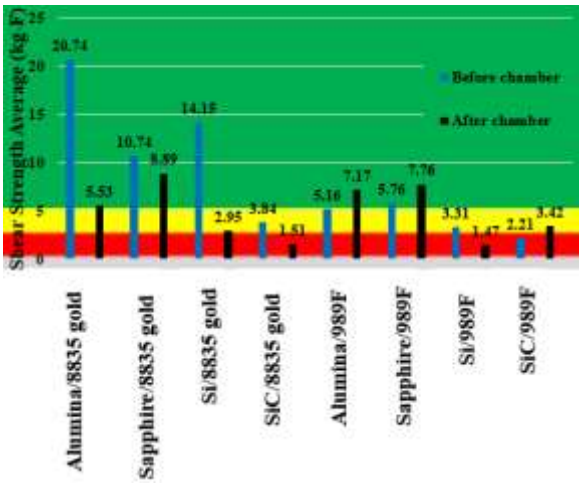

Figure 3. 2. Die shear strength results before and after Venus simulator exposure for 150 hours.

The die shear strength of the Si dice on gold had a significant reduction in die shear strength after the Venusian environmental exposure (73.34% decrease). The shear strength of the SiC degraded after the chamber test (60.68% decrease). The ceramic paste formed an excellent shear strength with the alumina (5.16 kg-F) and sapphire (5.76 kg-F) dice. Their die shear strengths increased after chamber exposure (38.95% and 34.72% increase for alumina/989F and sapphire/989F, respectively). This could be due to the formation of a stronger ceramic-to-ceramic crystal bonding after the high-temperature exposure since the bonding location was on alumina pads of the gold-printed alumina substrates [3-10].

Based on the above results, a second Venus simulator test was conducted on the selected die-attach materials. The Si and SiC dice were attached to the gold-printed alumina substrate (die sites #1 and #2 as shown in Figure 3.3(a), respectively) using the 8835 gold paste and cured at 125ºC and 580ºC, each for 15 minutes. Alumina and GaN/sapphire dice were attached (die sites # 3 and # 4 as shown in Figure 3.3(a)) using the 503VFG and 989F ceramic pastes, respectively, and were cured using their specific curing profiles. The ceramic packaging substrate was placed in the Venus simulator at 460ºC in a CO_2 ambient at 96 bars pressure for 244 hours. Figure 3. 3(b) shows

the discoloration of the gold pads on the ceramic substrate after the test exposure due to possible increase of surface roughness because of gold migration/inter-diffusion of CO_2 reaction with pastes constituents at high-pressure (96 bar) and high-temperature (465°C) test environment.

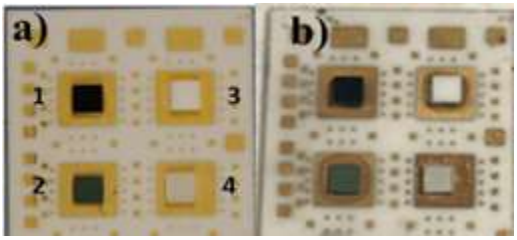

Figure 3. 3. Ceramic test substrate (a) before, and (b) after Venus simulator exposure.

Figure 3.4 shows the die shear strengths, along with their coefficients of variance (CV), before and after the Venus simulator test for the four test dice. These coefficients of variance are based on 6-8 samples each and represent the standard deviations over their mean values. All die shear strengths were above 2.5 kg-F. The die shear strengths decreased after exposure to the Venus stimulator test. The shear strength reduction was more pronounced for the Si and SiC dice attached using the 8835 gold paste, 75.67%, and 37.25%, respectively, compared to the 9.66% and 4.21% reduction in die shear strength for the alumina and sapphire dice attached using the 503VFG and 989F ceramic pastes, respectively.

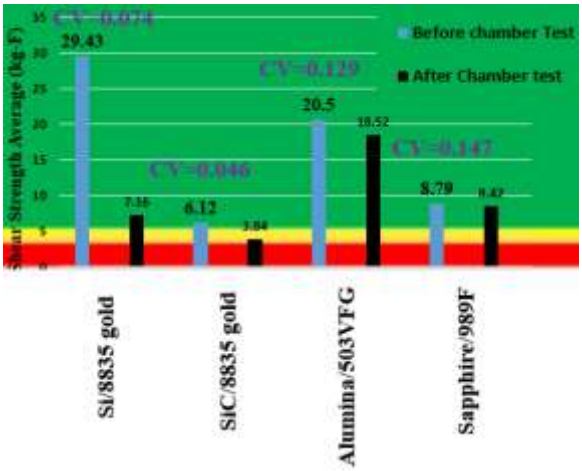

Figure 3. 4. Die shear strength results of different dice on gold printed alumina pads before and after Venus simulator exposure.

The die shear strength decreased after thermal aging or cycling due to a mismatch in CTE between the bonded layers. The other reason was the increase in grain size as a larger grain size allows a larger imperfection movement to reduce its shear strength [3-11]. The ceramic die-attach had excellent shear strengths with the alumina and sapphire dice and their shear strengths decreased after Venus stimulator chamber exposure. The results showed the shear strength of the pastes was higher on gold pads than the alumina pads for all dice/paste combinations. The thick-film gold die-attach shear strength reduction can be reduced by screen printing a Ferro 4007 Brazeable gold conductor layer on the top of 3066 gold paste and fired at 850°C for 10 minutes. This additional Au conductor reduces the delamination of 3066 gold paste from the alumina substrate and provides an Au-rich barrier layer on the substrate.

3.3.2 Wire Bonding

Alumina test dice with gold interconnects were attached to the alumina substrate with gold interconnects. The aluminum test dice were attached using the 989F ceramic paste. The ceramic paste was annealed at 65°C for 2 hours to drive off the binder followed by sintering at 200°C for 4 hours. To evaluate the wire-bond resistance changes, 3 wire bond daisy chains were formed using 1-mil gold bond wires in a K&S 4700 wire and ball bonder. Figure 3.5(a) shows the design of the three daisy-chain wire bonds and Figure 3.5(b) shows the actual daisy chains formed by the 1-mil gold bond wires between the test dice and ceramic substrate. There are eight die sites designated on the substrate coupon. A gold bond wire was pulled out of each die site randomly before and after the chamber exposure to check whether bond pull strength satisfied the minimum of 3 g-F (as specified in MIL-STD-883 method 2011.9 bond strength and destructive bond pull test [3-12]).

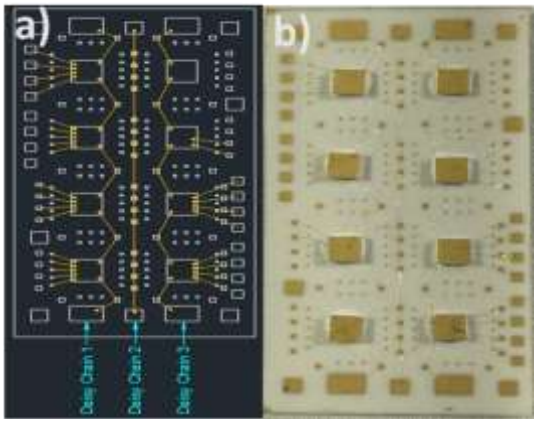

Figure 3. 5. (a) Daisy chain wire bond design. (b) 1-mil gold wires bonded to the gold-alumina die and substrate.

The average wire-pull strengths before and after chamber exposure were 5.78 g-F and 4 g-F, respectively, which were higher than the minimum MIL-STD requirement. Figure 6 shows the distribution plot of the average wire bond pull strength before and after the simulated chamber exposure. These bond wires detached randomly from both the test dice and substrate bond pads.

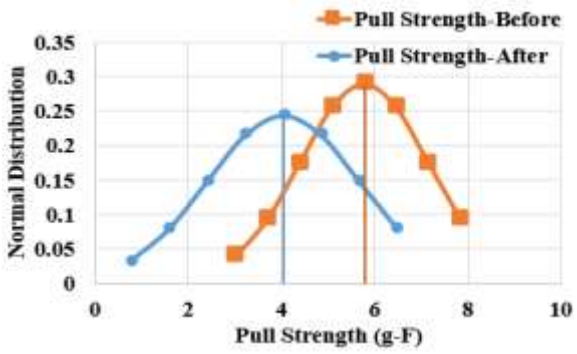

Figure 3. 6. Wire pull test before and after Venus simulator exposure.

3.3.3 Thermal Reliability Test

The wire-bonded test samples were fabricated and encapsulated using the 989F and 503VFG ceramic pastes. To evaluate these ceramic encapsulations, the left column of the dice (dice 1-4 as shown in Figure 3.1) was encapsulated by the 503 VFG ceramic paste while the right

column dice (dice 5 to 8 as shown in Figure 3.1) were encapsulated by the 989F paste. The 503 VFG paste was cured using a 4-step profile: 1-hour room temperature settling time followed by 2 hours at 94°C, 260 °C, and 372ºC in sequence. The 989F ceramic paste was left to settle for 4 hours at room temperature, followed by a 2 hours binder burn-out at 65°C, and 4 hours sintering at 200ºC. These samples were placed in an oven for 100 hours at 500°C for the thermal aging process. After thermal aging, these samples underwent 20 thermal cycles from room temperature to 500°C on a hot plate in the open air. Their wire bond resistances were measured after the initial cure, after the thermal aging, and after the temperature cycling. Figure 3.7 shows the resistance changes of the wire bonds in these samples. The overall wire-bond resistance changes for each chain (three chains in total) varied from 3.9% to 7.5%. The chain resistance dropped after each thermal cure; this could be due to the thermal annealing of the gold bond wires to their contact pads. The chain 3 resistance showed a slight increase between thermal processes, which might be an anomaly.

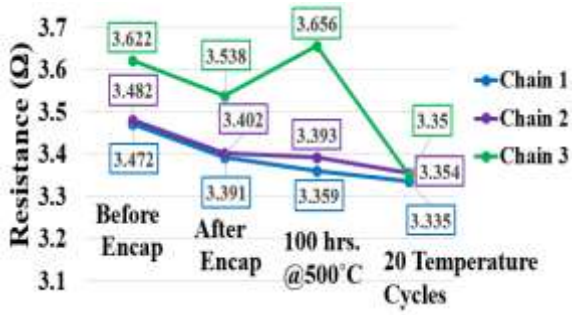

Figure 3. 7. Resistance changes of gold wire bond daisy chains before and after encapsulation, thermal aging, and thermal cycling.

3.3.4 Wire Bond Venus Simulator Test

A daisy chain test structure formed by the interconnection of four dice through the ceramic packaging substrate (as shown in Figure 3.8(a)) was used to evaluate the integrity of the bond

wires and their interconnections on the ceramic packaging substrate after the Venus simulator test. Figure 3.8(b) shows the fabricated wire-bond test structure using 1-mil gold bond wires.

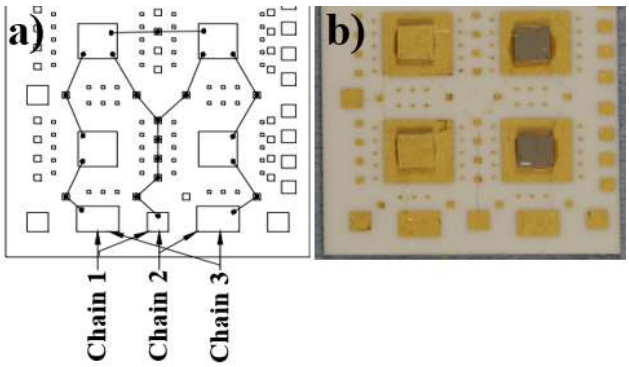

Figure 3. 8. (a) Wire bond daisy chain design, (b) 1-mil gold wires bonded to the gold/alumina and AuPtPd/Si die surfaces, and substrate pads.

The wire-bonded area was encapsulated using an alumina ceramic encapsulation material and cured sequentially at 110°C, 260°C, and 372°C, for 2 hours using a ramp-up rate of 3°C/min. Figure 3.9(a) shows the glob-top encapsulated test sample with some surface cracks on the ceramic encapsulation. Figure 3.9(b) shows the same glob-top encapsulated test sample after the Venus simulator test for 244 hours. A careful inspection indicated that surface cracks changed very little, but a surface discoloration was observed.

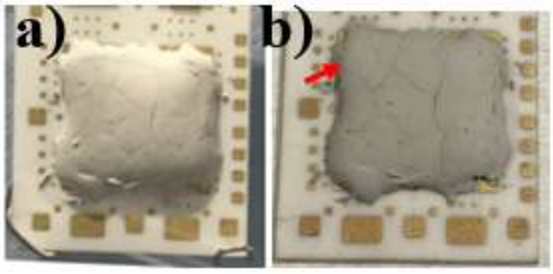

Figure 3. 9. Glob-top encapsulated wire-bonded sample (a) before, and (b) after the Venus chamber test.

The resistance of the 1-mil gold wire daisy chain was measured using a four-point probe resistivity measurement instrument and the resistance change on chain #2 is shown in Figure 3.10.

The resistances of gold daisy chains were measured after the wire bonding, after curing the glob-top encapsulation material, and after the Venus simulator test. As can be seen, the resistance change was negligible at about 0.47%, which is within the measurement errors of the four-point probe. One of the daisy chains (as indicated by the red arrow in Figure 3.9(b)) was open after the Venus simulator test.

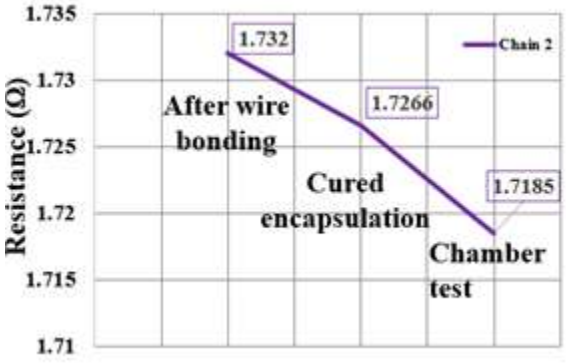

Figure 3. 10. Daisy chain resistance changes after wire bonding, encapsulation, and chamber test.

Note that it is possible to yield an almost crack-free ceramic encapsulation on a package. Figure 3.11(a) shows the ceramic encapsulation material dispensed onto the package using a dispenser with a 400 µm nozzle tip. The ceramic paste was custom synthesized for encapsulation purposes. Figure 3.11(b) shows the same ceramic encapsulation after curing at 110°C, 260°C, and 372°C in an air circulated furnace sequentially for 2 hours with a ramp rate of 3ºC/min. The ramp-up and ramp-down rates are important in ceramic paste uniformity and mitigation of cracks and voids. By increasing the ramp-up rate, the solvent evaporation rate increases, and the air trapped in the ceramic paste creates voids and cracks in the cured ceramic material [3-13]. A thick ceramic encapsulation promotes crack formation due to the greater intrinsic stress/strain on the ceramic material. With a thick die in the gold alumina package, the step coverage of the ceramic material

becomes critical and together with the mismatches in CTE between the die, gold metallization, and ceramic encapsulation, cracks become more pronounced.

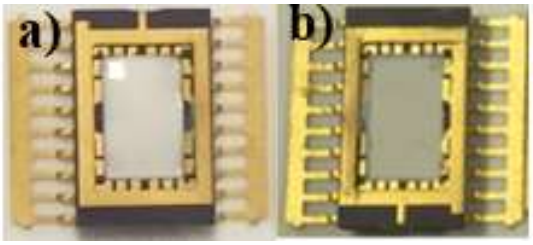

Figure 3. 11. (a) Un-cured and (b) cured encapsulation material on the gold-alumina package, showing no visible cracks.

3.3.5 Corrosion, and Dielectric Tests

3.3.5.1 Corrosion Test

To test the encapsulation material and evaluate how well it protects the encapsulated devices, a corrosion test substrate with copper serpentine conductors (as shown in Figure 3.12) was fabricated to have the top serpentine copper conductor covered with the ceramic encapsulation and the bottom serpentine copper conductor uncovered. The uncovered serpentine copper conductor on the test substrate was completely etched away in a ferric chloride etchant. The resistance of the encapsulated copper serpentine conductor was measured to be 0.2Ω before and after the 90 minutes etch. This indicates the integrity of the ceramic encapsulation.

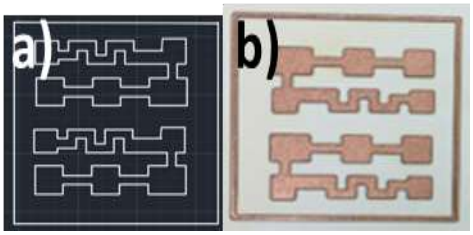

Figure 3. 12 (a) Serpentine conductor design (b) Copper etchant test substrate.

3.3.5.2 Ceramic Feedthrough and Dielectric Test

Electrical feedthroughs are desired in many applications. Figure 3.13(a) shows the fabricated ceramic feedthrough with two levels of printed gold interconnects. The feedthrough has several end-to-end gold connecting pads and the middle part has a gold conductor printed across these interconnects above the second layer of a ceramic insulation layer. These bottom gold interconnects were printed using the 3066 gold paste and cured at 850°C for 15 minutes in a curing oven. The middle interlayer ceramic insulator was screen-printed using the 503VFG paste followed by a 503VFG binder. The 503VFG ceramic paste was cured after screen-printing at room temperature for 1 hour, followed by 2 hours curing at 94°C, 260°C, and 372°C, in sequence. After curing, a very thin-layer of 503VFG binder was applied onto the 503VFG thick-film layer and cured again using the same curing profile as the 503VFG paste. The purpose of the 503VFG binder was to mitigate voids or crevices as well as to enhance adhesion of the top-layer gold conductor and to mitigate the delamination of the gold conductor from the ceramic or gold diffusion into the ceramic interlayer. The top layer gold conductor was screen-printed using the 3066 thick-film gold onto this second layer ceramic and fired at 850°C for 15 minutes.

The ceramic feedthrough substrate underwent a thermal shock (6 cycles) from room temperature to 500°C with a 1-minute soak time at each temperature. The thermal cycling with extended soak time was also conducted on the feedthrough substrate from -50°C to 275°C (30 cycles) with a 5 minutes soak time at each temperature with a temperature ramp-up and ramp-down rates of 13.54°C/min and 23.21°C/min, respectively, to test the multilayer bonding and adhesion as well as to observe any delamination or defect between the gold and ceramic interlayer dielectric. After an initial thermal cycling test on the feedthrough substrate, no delamination or new defect was observed under an optical microscope. A dielectric test was performed on the

ceramic feedthrough substrate to test the integrity of the ceramic insulation. Two test electrodes with a spacing of 15 mm were placed on the top and bottom gold thick films at a relative humidity of 37% as shown in Figure 3.13(b). As the voltage applied to the electrodes slowly ramped up to 1000V, a leakage current of 1nA was measured that corresponded to an insulation resistivity of 2 $\times 10^{14}$ Ω-cm. Hence, the ceramic interlayer yielded a high insulation dielectric strength between the two layers of gold conductors.

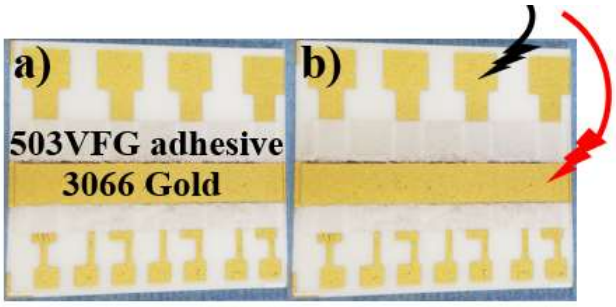

Figure 3. 13. (a) Ceramic feedthrough. (b) Dielectric test performed on the ceramic feedthrough.

3.3.6 Package Design

In a corrosive environment, the package housing material is critical. Titanium was chosen as the package housing material because of its excellent corrosion properties, high shear strength, and low mass. Besides, titanium was utilized in a Venus in-situ explorer [3-14]. Since the ceramic substrate would attach directly to the titanium housing, their substrate/titanium shear strengths were investigated. The shear strengths, along with their coefficients of variance, of the ceramic substrate with different ceramic pastes and 8835 gold paste as the attach materials with titanium housing are shown in Figure 3.14. As shown, the 8835 gold paste had the highest shear strength for the titanium/ceramic substrate than all other ceramic pastes.

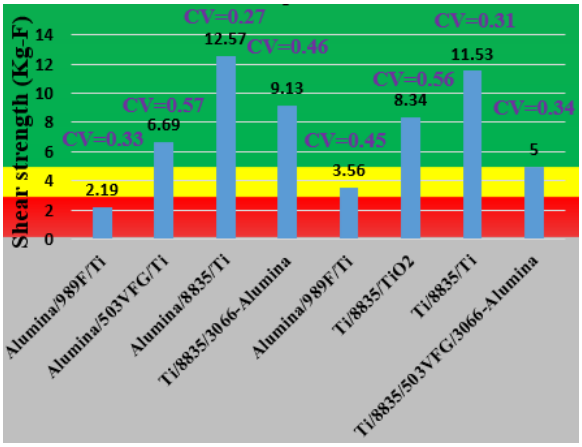

Figure 3. 14. Shear strength of alumina substrates on the titanium housing using different pastes.

The package housing material is an ultra-corrosion-resistant grade 2 titanium bar. The titanium bar was machined to yield a cavity for the alumina packaging substrate and a feedthrough slot for its electrical connections. The alumina substrate was attached to the cavity using the 8835 gold paste and cured at 125°C and 580°C for 15 minutes sequentially. Titanium oxidizes and depending on oxide thickness, its color changes due to light-wave filtration [3-15]. As shown, the color of the housing is bluish, indicating the formation of an oxide layer that serves to protect the titanium housing from the caustic environment. A second gold conductor on top of the top layer of ceramic was used to serve as the seal between the housing and outside electrical connections. The feedthrough substrate was attached to the feedthrough slot using the 8835 gold paste.

Figure 3.15 shows the titanium package with a daisy chain alumina packaging substrate connected to the ceramic feedthrough fixture. After the substrate and feedthrough were attached to the titanium package, 1-mil gold bond wires were used to interconnect the dice and the substrate. A 3-mil gold ribbon was used to attach the alumina substrate connector to the feedthrough substrate. The 3-mil gold ribbon was utilized to increase the integrity of the interconnections due to the length of the interconnections between the substrate module and feedthrough substrate.

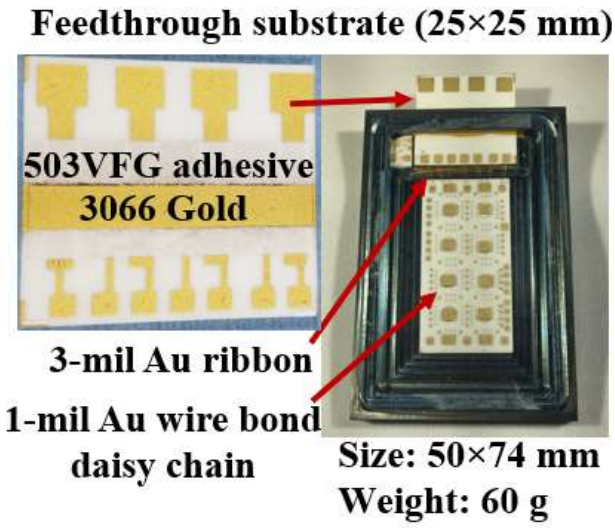

Figure 3. 15. Gold wire-bonded substrate and electrical feedthrough mounted on a titanium package.

3.3 Conclusion

An electronic packaging technology consisting of the substrate, die-attach, interconnections, and encapsulation was developed to survive a test environment of 460°C in CO_2 ambient at 96 bar pressure conditions. The ceramic die-attach showed an excellent shear strength with alumina and sapphire dice on alumina pads, with increasing shear strengths after chamber exposure due to the formation of ceramic crystal bonding after the high-temperature annealing. However, the die shear strengths of the alumina and sapphire dice/ceramic paste on the gold/alumina pads of the gold-alumina substrate decreased after chamber exposure even though they had a higher initial (before chamber exposure) shear strength than those with alumina pads on the substrate. The Si and SiC dice with thick-film gold die attach and alumina and sapphire dice with alumina-based ceramic paste die attach maintained exceeded the minimum of MIL-STD standard of 2.5 kg-F after all tests. The gold bond wire daisy-chain resistance had negligible resistance change (about 0.47% resistance reduction) after the 244 hours environmental test. The average bond wire pull strengths before and after exposure were 5.78 g-F and 4 g-F, respectively,

meeting the minimum MIL-STD standard of 3 g-F for 1-mil gold-wire bond. The ceramic glob-top encapsulation was shown to survive the environmental test with no significant increase in cracks and voids. The ceramic encapsulation material showed promising protection for the underneath electronic devices. The encapsulated package survived acidic and corrosive environments. A titanium package was fabricated to house the ceramic packaging substrate and a two-level metalized feedthrough was fabricated to provide the electrical connections for the package.

3.4 References

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CHAPTER 4

High-Temperature Double-Layer Ceramic Packaging Substrates

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4.1 Introduction

High-temperature resilient electronics are desired to process, amplify, and transfer reliable data under extreme operating conditions. Specifically, high-temperature electronics that can survive 500°C operational temperature require special material and packaging considerations. For high-temperature electronic systems, multi-layer packaging substrates are desired to improve its packaging density. The specific objectives are to develop a multi-layer high-temperature capable ceramic packaging architecture using metal-interconnect technology for harsh environment applications at 500ºC. Besides hot planet applications, this high-temperature packaging technology is applicable in various industries such as geothermal energy production, oil and gas exploration, and nuclear energy. The available packaging technology and electronics which are currently being used in these industries are limited by operational temperature (typically below 300 °C) and the package's reliability issues [4-1].

There are numerous types of substrate for high-temperature applications, the commonly used are high-temperature co-fired ceramics (HTCCs), high-purity alumina substrates, and low temperature co-fired ceramics (LTCCs) [4-2]. Each of these high-temperature substrates has its advantages and disadvantages such as different conductivities, parasitic noises, and dielectric constants at high-temperature and high-frequency operations. For example, having numerous choices of electrical conductors for the co-firing process and low co-firing temperature (~875ºC) are advantages of LTCC alumina substrates. Also, the LTCC alumina consists of glass constituents being able to be co-fired with a conductor with a melting temperature below the alumina sintering

temperature [4-3]. However, the glass constituents cause degradation in dielectric constant at high-temperatures. The high purity (96-99%) alumina substrates have a smaller conductivity and dielectric changes at high-temperatures (above 400 ºC). The dielectric constant of 96% alumina substrate is higher than that of the LTCC alumina substrate from room temperature (RT) to about 300 ºC, but the dielectric constant of the LTCC suddenly increases at the temperatures above 300 ºC [4-4]. Among high-temperature substrates, the 96% alumina substrates have a higher dielectric performance at higher temperatures [4-5]. So, the high purity alumina substrates have been selected as the high-temperature substrates because these substrates are capable of withstanding 500ºC operation temperature. However, the conventional HTCC process requires extreme high firing temperatures around 1,600ºC that renders only certain refractory metals be used as their electrical conductors. Table 4.1 briefly shows the pros and cons of HTCCs, LTCCs, and their applications. These refractory metals have low conductivities and require extensive investigations of the suitability of the conventional wire bonding, die-attach, and encapsulation materials and processes.

Table 4. 1. HTCC and LTCC Comparison and Their Application [4-3, 4-6].

	LTCC	HTCC
Pros	-Low co-firing temperature -Stable permittivity (ε_r = 3-10) -More co-fired conductor choices	-Higher stability at high-temperature and high-frequency applications -Relatively lower conductivity
Cons	-Low thermal conductivity (3-4 W/m-K) -Higher shrinkage rate during the firing -Higher dielectric constant (>300°C)	-Higher firing temperature (>1,600°C) -Fewer co-fired conductor choices
Application	-Microelectronic packaging -Microwave	-High frequency and high temperature -Aerospace

There are different types of substrate and low-temperature bonding techniques that are capable to withstand high temperature. The low-temperature glass powder was directly bonded to

ZnS ceramic (temperature between 400°C - 450°C) which was subjected to have a low mechanical strength but Xu et al. [4-7] suggest doping the $PbTiO_3$ particle to enhance the bonding mechanical strength. There are different applications for ZnS ceramic substrates such as aerospace and aircraft window which used to yield a poor safety and reliability results but Zhang et al. [4-8] used Ni-P coating on ZnS transparent ceramic was bonded using Sn-3Ag-05Cu at low temperature to increase the mechanical and bonding strength reliability. Different types of die attach material can be used for high-temperature electronic packaging such as nano-silver, nano-solder, surface plasma, nano-welding, and carbon nanotubes [4-9]. Each die-attach material and technique have their advantages and disadvantages, and it varies depending on the package's application, operating temperature, and atmospheric condition. For instance, at high-temperature applications, there are common issues that affect the package's performance such as thermo-migration, delamination, mechanical strength and degradation of material properties which could be respectively because of the coefficient of thermal expansion (CTE) mismatch, grain boundaries growth, high-temperature, and harsh environment exposure [4-10].

In this work, a double-layered ceramic packaging technology using gold die-attach, gold conductor, a ceramic substrate, and ceramic interlayer are investigated. The die-attach materials (alumina-based ceramic and thick-film gold pastes) were evaluated on the double-layered ceramic substrates. The ceramic interlayer was used to serve as the interlayer insulator between the top and bottom gold interconnects. Thermal cycling from RT to 450ºC and 500ºC exposure for 115 hours (additional test was performed for 1,540 hours) was performed to evaluate the reliability of these double-layered ceramic substrates. Die shear tests were carried out on the packaging substrate to evaluate the mechanical properties of the ceramic interlayer. A dielectric test was performed to evaluate the ceramic interlayer insulation properties before and after environmental exposure.

4.4.2 Experimental Approach

4.4.2.1 Materials overview

The 98% alumina substrates (CoorsTeK, Golden, C) and the high-temperature ceramic adhesive (503VFG [very fine grain], Aremco Products, Inc., Valley Cottage, NY) were used. The 8835 gold cermet (8835 gold paste) conductor (ESL 8835 [520C] 9802A, Electro-Science Laboratories, King of Prussia, PA), 3066 fireable gold thick-film paste (3066/3068N Wire-Bondable Au Conductors) and 4007 Brazeable Au conductor were purchased from Ferro corporation (Mayfield Heights, OH). Also, the electrical-grade adhesive back Kapton® polyimide film (50 μm thick) was purchased from McMaster-Carr (Robbinsville, NJ).

4.2.2 Substrate fabrication

Figure 4.1 shows the three mask layers for the double-layered ceramic substrate test vehicle. There are two conductor layers, the red conductors are on the bottom of the ceramic substrate whereas the green conductors are on the top of the ceramic interlayer dielectric (blue). The main goal of these interconnect patterns is to check for the interlayer insulation between the top and bottom interconnects. Four die-attach sites were designed as a part of the top gold conductor for die-attach and die shear tests. An aluminum frame mesh screen was used to screen print the 3066 gold paste onto the alumina substrate to create the gold interconnects for interconnecting electronic components. The process flow for the ceramic packaging substrate preparation is shown in Figure 4.2.

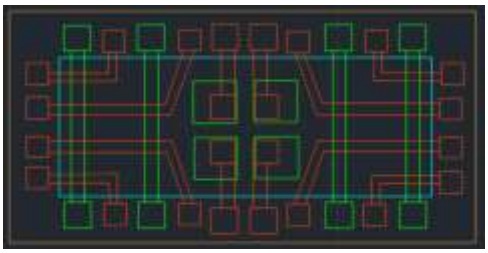

Figure 4.1. Mask layout: red (bottom conductors), green (top conductors), and blue (interlayer ceramic).

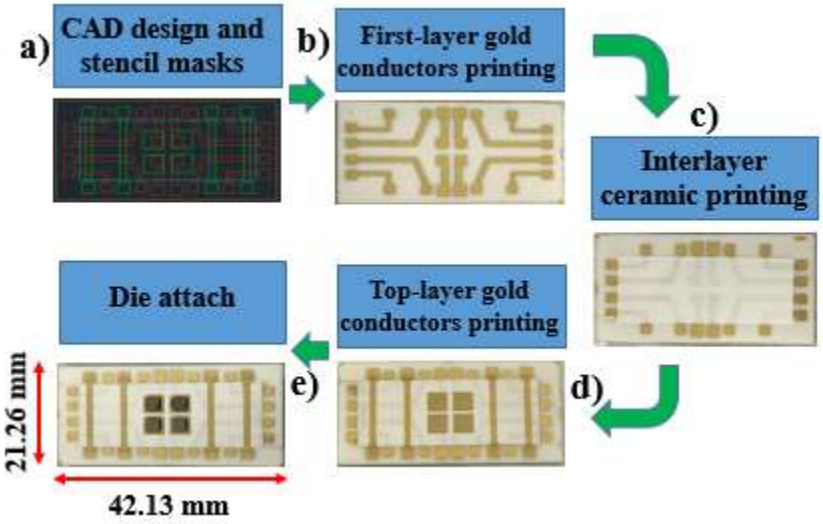

Figure 4. 2. Process flow for the ceramic packaging substrate fabrication.

After the 3066 gold paste screen printing, the gold interconnects were fired using a 3-steps firing profile: 3-4 minutes leveling at RT, 10-15 minutes at 100-120ºC in an air circulated box furnace, and final firing at a peak temperature of 850 ºC for 10 minutes with a heating up and cooling down rate of 45 ºC/min. The first-layer gold interconnects after firing are shown in Figure 4.3(a). A promising adhesion was observed for these gold conductors on the ceramic substrate based on the shear test results. After screen-printing the 3066 gold paste, the ceramic pastes 503VFG were screen printed on the packaging substrate as an interlayer ceramic insulator. The

ceramic layer was cured using a 4-step profile: 1-hour RT settling time followed by 2 hours at 94°C, 260°C, and 372°C sequentially.

Before screen printing, the 3066 gold paste on top of the ceramic interlayer, a diluted 503VFG ceramic paste layer (503VFG:503VFG thinner [503VFG-T], 5:1), was printed on the top of the ceramic interlayer to mitigate voids or crevices to prevent gold diffusion into the ceramic interlayer dielectric. This thin diluted 503VFG layer also helps enhance the adhesion of the top gold conductors to the ceramic interlayer dielectric and mitigates the delamination of the top gold conductors. The diluted 503VFG ceramic paste has a similar four-step curing profile as the non-diluted 503VFG paste: 1-h RT settling time followed by 2 hours at 94°C, 260 °C, and 372ºC, sequentially. The ceramic interlayer thickness including the additional 503VFG thinner is 60µm as shown in Figure 4.3(b). As shown, the bottom gold conductors can be vividly seen through the interlayer ceramic dielectric.

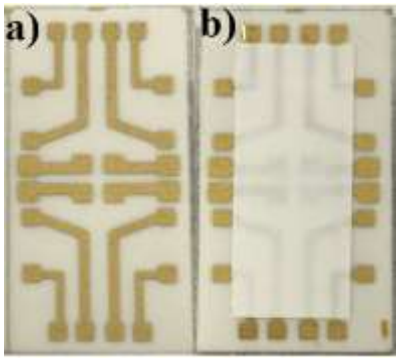

Figure 4.3. (a) Gold thick-film interconnects on the alumina substrate, (b) with a top ceramic interlayer.

Next, the 3066 gold paste was screen printed on the cured ceramic interlayer using aluminum frame screen printing mesh with a stencil and was followed by the same three-step firing profile: 3-4 minutes leveling at RT, 10-15 minutes at 100-120ºC in air circulated furnace, and final firing at a peak temperature of 850ºC for 10 minutes 10 minutes with a heating up and cooling

down the rate of 45ºC/min. The top fired 3066 gold conductor thickness is about 25 µm. Figure 4.4(a) shows the top gold conductor layer after fabrication.

To increase die shear strength for the dice, an additional layer of a 4007 Brazeable conductor was printed on 3066 gold conductors to provide an Au-rich barrier layer on the substrate for the die-attach pads. A three-step firing profile was used: 3-4 minutes leveling at RT, 10-15 minutes at 100-120ºC in an air circulated furnace, and final firing at a peak temperature of 850ºC for 10 minutes with a heating up and cooling down the rate of 45ºC/min. A gold/platinum/palladium (AuPtPd) thick film was screen printed on the backside of the silicon wafer and then diced to 2.6mm by 2.6mm test dice. The gold paste was cured using a two-step curing profile: 10 minutes RT settling time and 15 minutes drying step at 125ºC, followed by 15 minutes firing at a temperature of 580ºC with a temperature ramp-up rate of 25ºC/min. The fabricated substrate with the four attached dice is shown in Figure 4.4 (a) and (b).

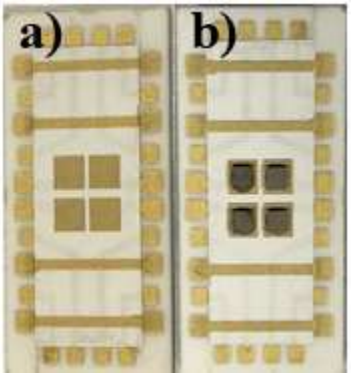

Figure 4.4. (a) top gold conductors, (b) after the die-attach process.

The step coverage of the top gold conductors is an important consideration given the thickness of the interlayer ceramic dielectric is 60 µm. Figure 4.5 (a) and (b) shows a good step coverage of two of the top gold conductors. A continuity test was performed on these top gold

conductors to compare their resistances, which is an indirect indication of the gold step coverage on both sides of the top ceramic layer.

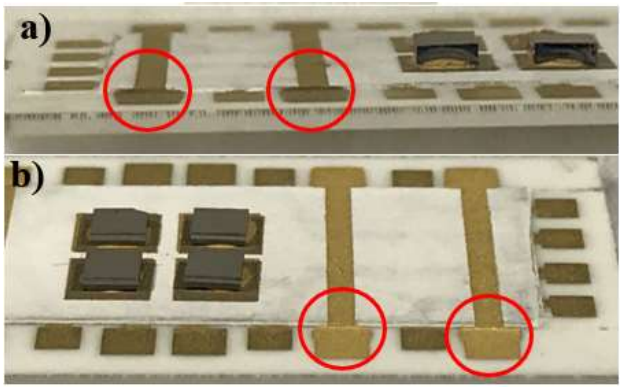

Figure 4.5. Continuity of the top gold conductors.

4.2.3. Dielectric and Die Shear Tests

Dielectric tests were carried out on the double-layer ceramic packaging substrates before and after thermal tests. A direct-current (DC) voltage was applied across the bottom and top gold conductors to measure its leakage current using a Valhalla Scientific Automatic HIPOT tester (model no. 5880A). The DC voltage was applied at a ramp-up rate of 10 V/s up to 600V with a maximum current limit (current trip-out limit) of .1 mA and a test duration of 10s at the maximum applied voltage. All possible test combinations of top and bottom conductors were performed. The resistances between the top and bottom gold conductors were measured before and after thermal tests using a BK precision model 880 LCR meter. Die shear tests were carried out on the four attached dice before and after thermal tests using a Dage 4000 shear and pull bond tester. Temperature cycling was performed on a ceramic top hot plate with a temperature range from RT to 450°C.

4.3. Results and Discussion

4.3.1. Dielectric and Resistance Test

The double-layer packaging substrates were exposed to 115 hours of thermal aging at 500°C and 30 cycles of temperature cycling from RT to 450°C with a temperature ramp-up/down rate of 267°C/min. An aluminum cooling plate was used to cool down the ceramic substrates after each temperature cycle. A Fluke 52 K/J thermometer was used to monitor instant temperature at both the hot plate and heat sink. Figure 4.6 shows the temperature excursion during the temperature cycling test. To facilitate tracking of test results, the top and bottom gold conductors were labeled as shown in Figure 4.7.

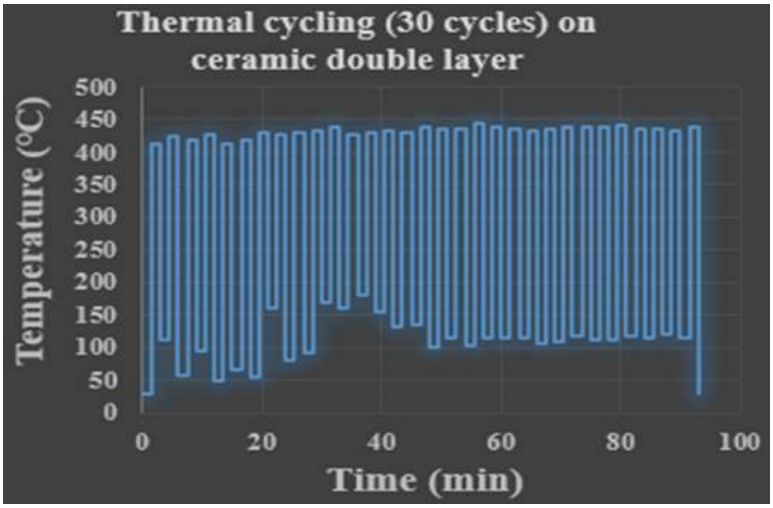

Figure 4. 6. Thermal profile during temperature cycling.

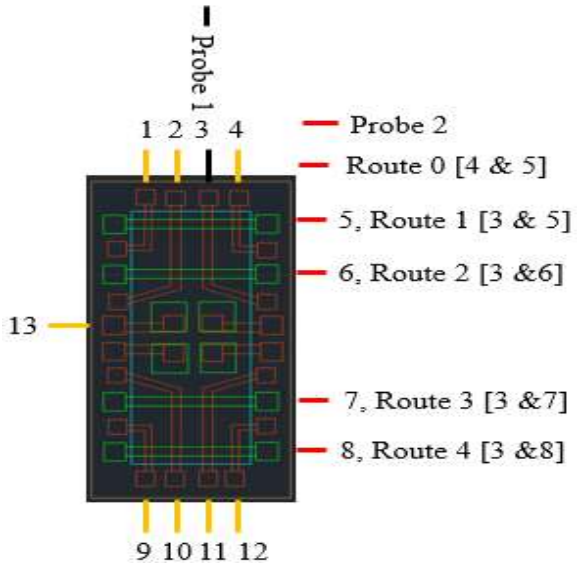

Figure 4. 7. Conductor and route labeling for the double-layered substrate.

After thermal aging and temperature cycling, dielectric tests were performed. A 100V DC voltage was applied on the substrate between "probe #1" at conductor #3 and various routes #1-4 at RT in 37% humidity. Figure 4.8 shows the leakage current densities measured at 100 V DC. The leakage current density drops after each thermal test (thermal aging and cycling) except route 1 after thermal aging which could be a random error. The random error can be a combination of human and equipment error, and/or material defects (imperfections and voids in the ceramic interlayer) which affect the dielectric behavior. The leakage current density drop is probably due to the increase in electrical resistance of the ceramic interlayer dielectric. The measured leakage current density at 100 V DC was between 1×10^{-7} A/cm^2 to 64×10^{-7} A/cm^2.

As is shown in figure 4.7, the distances between the top and bottom conductors on route #1 (the voltage difference is between conductors #3 and #5) and route #2 (the voltage difference is between conductors #3 and #6) are the same height as ceramic interlayer thickness (~60 µm) but the distances between the voltage probes on route #3 (the voltage difference applies between conductors #3 and #7) and route #4 (the voltage difference applies between conductors #3 and #8),

which is about 2-3 cm, are larger than probe's distance on routes #1 and 2. When the voltage applies between the top and bottom conductors by having a ceramic interlayer, the structure is similar to a parallel plate capacitor with an insulator. Based on the electric field and current charge equations ($E=V/d=Q/\varepsilon_0 A$ and $I=dq/dt$), by increasing the distance between charged plates, the electric field strength reduces which results in a smaller leakage current density value. From a material perspective, in a larger distance between the electrodes, the electric field should travel a longer distance and ceramic material's dislocation density might be lower which yields a lower leakage current density [4-11].

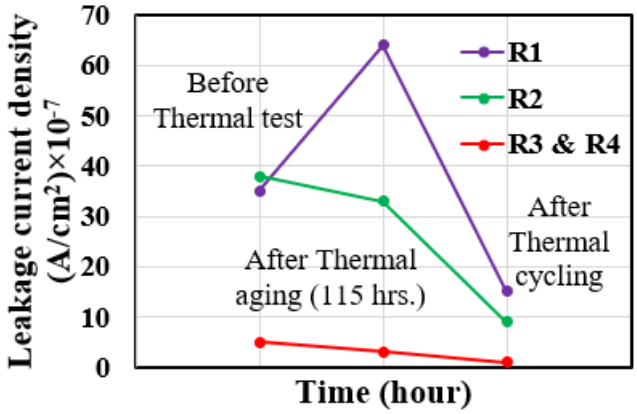

Figure 4. 8. Leakage currents densities on the double-layered substrate by applying 100 V DC.

Gold conductor resistances were measured before and after temperature cycling. The conductors with the same length are grouped for better consistency. Three groups were created as group # 1 (conductors #1, 4, 9, and 12 with the same length of 8.5 mm), group #2 (conductors #2,3,10, and 11 with the same length of 16.3mm), and group #3 (conductors #5,6,7, and 8 with the same length of 17.1 mm). Resistances were measured for each group before and after temperature cycling and average of resistances increased for groups #1, 2, and 3 with a rate of 7.92%, 9.85%, and 10.42% respectively (the percentages increased by conductor length). The bottom gold traces (groups #1 and 2) had higher initial resistance than the top gold conductors (group #3) that can be

because the bottom gold conductors faced more heating and firing process during the fabrication than the top gold conductors. An overall increase in gold conductor resistance after the thermal test (thermal aging and cycling) might be due to the annealing, aging, or structural changes of these conductors [4-12]. Figure 4.9. (a), (b), and (c) show resistance changes for groups #1, 2, and 3, respectively.

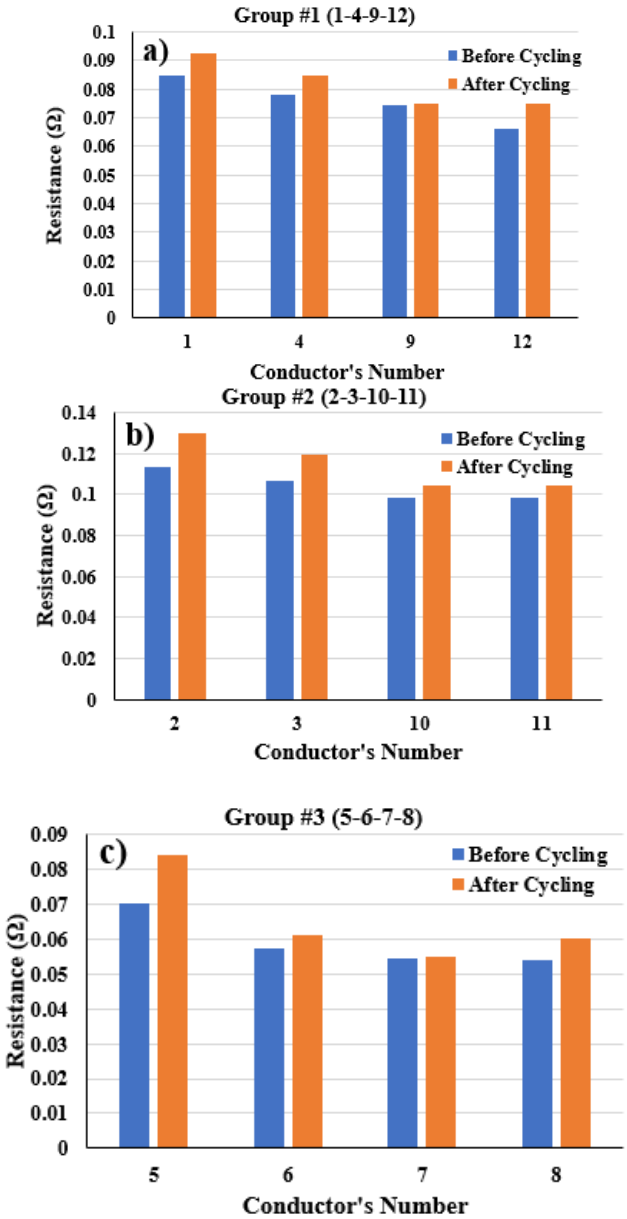

Figure 4.9. Resistance plots of the gold conductors before and after the thermal test for (a) group #1 (1-4-9-12), (b) group #2 (2-3-10-11), and (c) group #3 (5-6-7-8).

Interlayer dielectric tests were performed on the double-layer ceramic packaging substrates before and after temperature cycling by applying a direct voltage from 100 V DC to 600 V DC with a 10 V/s rate and a 10-s dwell time. As shown in Figure 4.10, the leakage current density increases by increasing applied voltage before and after temperature cycling. At 600 V DC, the initial leakage current density before thermal cycling is 158 $\times$ 10^{-7} A/cm^2. The leakage current density calculated for the 1-mm^2 cross-section area. However, the leakage current decreases to 50 $\times$ 10^{-7} A/cm^2 after temperature cycling. As shown, the leakage current densities decreased by an average of 71.61% after temperature cycling. By thermal annealing the interlayer ceramic at about 450-500°C, the alumina ceramic interlayer starts to transform to polycrystalline structure and becomes denser, and then the dislocation (imperfections) density starts to reduce (less void) which leads to lower leakage current density, higher electrical, and thermal stability [4-13].

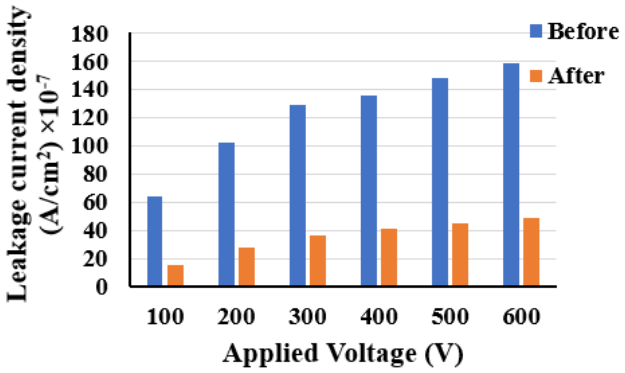

Figure 4.10. Dielectric leakage current density versus applied voltage before and after temperature cycling.

The dielectric test was performed on the ceramic interlayer (distance between probes was 1 cm) and the current reached out the current trip-out limit of .1 mA at 3,921 V DC. The maximum voltages that the substrate could withstand to reach the current trip-out limit of .1 mA was 4,421

V DC and 2673 V DC (on route # 1) for before and after the thermal test (1540 hours thermal aging at 500°C and 30 thermal cycles from RT to 450°C).

4.3.2. Die-Attach Evaluation

Die shear tests were performed to evaluate the integrity and quality of the die-attach before and after thermal tests. The MIL-STD-883 2019.9 die shear strength standard method was adopted for die shear strength at 500°C. The die shear test was based on the measurement of the force applied perpendicular to the side of the test device to assess various failure modes. Based on the MIL-STD 2019 method, all devices with a surface area of 64×10^{-4} in.^{2} and larger shall withstand a minimum force of 2.5 kg-F. The die shear strength values versus die area can be categorized into three shear strength levels: poor (<2.5 kg-F), medium (between 2.5 kg-F and 5 kg-F), and excellent (>5 kg-F). Based on a die size of 2.6×2.6 mm^2 or 105×10^{-4} in.^{2}, a die shear strength between 2.5 Kg-F and 5 Kg-F was considered acceptable. The additional 4007 Brazeable conductor was printed on 3066 gold conductors to provide an Au-rich barrier layer on the substrate for the die attach pads. This additional gold layer has been shown to increase the die shear strength and reduce the gold delamination from the ceramic substrate. A 36.95% increase in die shear strength was found on those dice with the additional 4007 gold layer compared to those on a single layer of 3066 printed gold layer.

The die shear strengths of the test die attached on the double-layer ceramic packaging substrates were evaluated after annealing at 500°C for 115 h and after 30 thermal cycles from RT to 450°C. Figure 4.11 shows the die shear strength before and after thermal aging at 500°C. As shown, the die shear strength decreases from 9.16 kg-F to 6.16 kg-F, a 32.75% reduction, after the thermal aging. However, the decreased die shear strength is still above the 2X line or 5 kg-F. The

decrease in die shear strength after thermal aging could be due to the mismatch in the coefficients of thermal expansion (CTEs) between the bonded layers. Based on the grain growth law [4-14], by increasing the annealing time and temperature, growth in grain size of the die-attach may be another reason as a larger grainsize allows a larger imperfection movement to reduce its shear strength [4-15]. The top dice are made of Si, and the CTE of gold thick film and Si die are 14.4 × 10^{-6}/°C and 2.6 × 10^{-6}/°C, consequently [4-16, 4-17]. In theory, the induced length difference between Si and gold material when the Si/gold interface's temperature reaches 500°C is about 15.34 µm due to their CTE mismatch, and this causes degradation in shear strength.

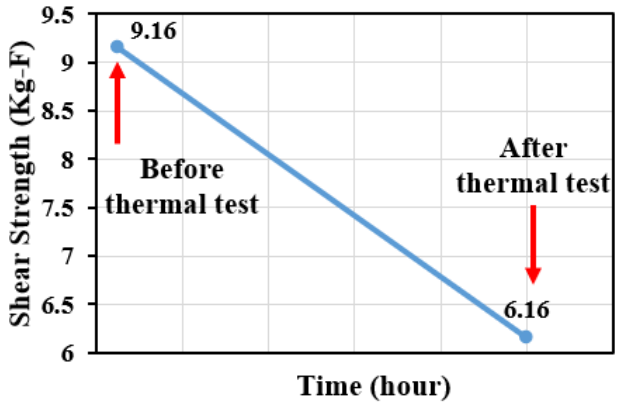

Figure 4. 11. Die shear strength value before and after thermal reliability test.

4.3.3. Morphology and Surface Roughness

The atomic force microscopy (AFM) pictures of the gold surface before (Figure 4.12 (a)) and after (Figure 4.12 (b)) the thermal test at 500°C are shown in Figure 4.12. The surface roughness reduced 19.62% after thermal reliability tests (thermal aging and cycling) which could be due to the thermally induced changes in the gold surface and this results in a larger surface grain size and smaller average roughness amplitude on the gold surface [4-18].

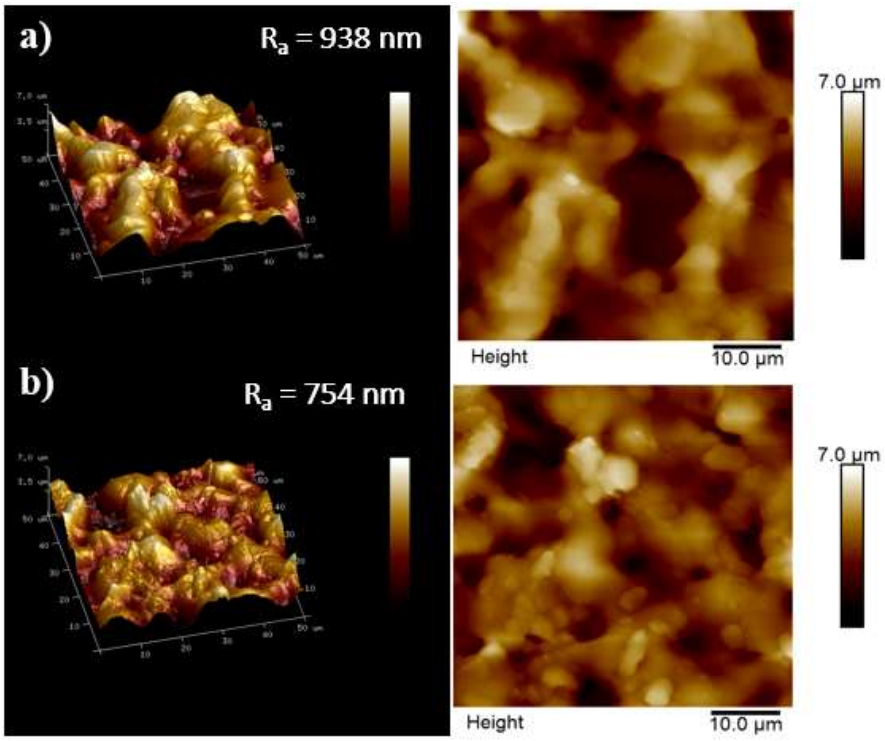

Figure 4. 12. AFM images of the gold surface (a) before and (b) after the thermal test at 500°C.

4.4 Conclusions

A double-layer ceramic packaging substrate with gold conductors and a ceramic interlayer dielectric was successfully fabricated using a 96% high-temperature alumina substrate. The packaging substrates were subjected to thermal aging at 500°C for 115 hours and 30 temperature cycles between RT and 450°C. Both resistance and dielectric measurements were performed before and after thermal tests. The leakage current densities decreased after thermal tests, whereas the gold conductor resistances increased by 8.2%. A dielectric leakage current density of 158×10^{-7} A/cm^2 at 600 V DC was measured with an average decrease of 71.61% of leakage current density after temperature cycling. The die shear test strengths before and after thermal aging and temperature cycling were higher than the MIL-standard value of 5 kg-F.

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CHAPTER 5

Conclusion and Recommendations

5.1 Introduction

Electronic packaging technology consisting of the substrate, die-attach, interconnects, and encapsulation was developed and demonstrated to survive in a Venus environment (corrosive, 460°C, CO_2 ambient with 96 bar pressure). Commercially available ceramic materials were demonstrated to not show reliable die attach and encapsulation properties under the Venus conditions. Therefore, a ceramic material was synthesized for both die-attachment and encapsulation. Multiple thermal and mechanical reliability tests were performed on the fabricated package to meet industry standard reliability requirements. Finally, a double-layered ceramic substrate was designed and fabricated using the developed high temperature ceramic to reduce the wire bond loops and to increase the integrity of the high-temperature electronic packages in a denser platform. This new ceramic was able to facilitate reliable packaging over 500°C, while the current state of art encapsulation materials is limited to below 300°C.

5.2 Dissertation contributions

High-temperature electronic packaging which could survive a 500°C, acidic and corrosive environment was developed. This dissertation started with an overall introduction to electronics packaging along with relevant background and previous works. The ceramic paste for high-temperature (300-500^{o}C) electronic packaging applications. Die-attach and encapsulation materials have been synthesized using alumina powder, nano-AlN (10%), and aluminum dihydric phosphate with various curing promoter percentages (5%, 10%, and 15% wt., and without) of nanosilica. The samples which contain 10% nanosilica exhibited a higher bonding strength and

bonding quality than other percentages. Sintering or curing profile, heating, and sintering temperature, and curing rate have important roles in the die-attach bonding and encapsulation quality. A lower curing rate (2-3 ºC/min) has been shown to yield better bonding quality and fewer voids/microcracks when applied as an encapsulant to electronic packages. Thermal cycle tests were performed from room temperature to 500ºC for 20 consecutive cycles and thermal aging was performed at 500ºC for 100 hours on the alumina and sapphire die samples. Both samples exhibited a decrease in their die shear strengths after thermal cycling (22% and 62% decrease for alumina and sapphire dice) and thermal aging (17.40% and 47% decrease for alumina and sapphire dice).

The 10% nanosilica-alumina paste yielded the best encapsulation properties with fewer cracks, voids, and surface defects. XPS results revealed a higher oxygen bonding percentage in the 10% nanosilica sample than the sample without nanosilica and the binding energy shows a possibility of the formation of alumina-silicate bonding. XRD results showed a shift in elemental peak positions when nanosilica was added to the ceramic paste. This indicated a larger lattice spacing, which was maximum for the 10% nanosilica sample, and as a result, it demonstrated a larger microstrain in its crystal structure. Additionally, the XRD peak broadened the most (for alumina and nanosilica) for the 10% nanosilica sample, which indicated smaller crystallite sizes. FTIR results showed the presence of alumina-silicate bonds on these samples with the largest amount, also present in the 10% nanosilica samples. Si-O and Al-O bonds were observed in these 10% nanosilica samples. Cross-sectional SEM showed the most uniform bond line for the 10% nanosilica sample, while EDX mapping indicated it had the most uniform material distribution. Finally, the number of voids was found to be highest in die-attach samples with no nano-silica.

Chapter 2 addressed an electronic packaging technology consisting of the substrate, die-attach, interconnections, and encapsulation that was developed to survive a test environment of 460°C in CO_2 ambient at 96 bar pressure conditions. The ceramic die-attach showed excellent shear strength for both alumina and sapphire dice on the alumina substrate, with increasing shear strength after chamber exposure due to the formation of bonding between ceramic's crystallites upon high-temperature annealing. However, the die shear strengths of the alumina and sapphire dice when attach on gold printed alumina substrate using ceramic paste decreased after chamber exposure even though they had a higher initial (before chamber exposure) shear strength than those with alumina pads on the substrate. The higher shear strength reduction could be due to a higher CTE mismatch between the ceramic paste and gold pads. The Si and SiC dice with thick-film gold die-attach and alumina and sapphire dice with alumina-based ceramic paste die-attach maintained or exceeded the minimum of MIL-STD standard of 2.5 kg-F after all tests. Additionally, the gold bond wire daisy-chain resistance had negligible resistance change (about 0.47% resistance reduction) after the 244 hours environmental test. The average wire bond pull-strengths before and after exposure were 5.78 g-F and 4 g-F, respectively, meeting the minimum MIL-STD standard of 3 g-F for 1-mil gold-wire bond. Finally, the ceramic glob-top encapsulation was shown to survive the environmental test with no significant increase in cracks and voids. The ceramic encapsulation material showed promising protection for the underlying electronic devices. The encapsulated package survived acidic and corrosive environments. A titanium package was fabricated to house the ceramic packaging substrate and a two-level metalized feedthrough was fabricated to provide the electrical connections for the package. In summary, the materials including die, die-attach, encapsulation materials, and package housing were tested at the Venusian condition and have shown reliable results to operate in high-temperature and harsh environments.

A double-layer ceramic packaging substrate with gold conductors. A ceramic interlayer dielectric was successfully fabricated using a 96% high-temperature alumina substrate. The packaging substrates were subjected to thermal aging at 500°C for 115 hours and 30 temperature cycles between room temperature and 450°C. Both resistance and dielectric measurements were performed before and after thermal tests. The leakage currents decreased after thermal tests while the gold conductor resistances increased by 8.2%. This was due to transforming the ceramic interlayer structure to polycrystalline and becomes denser, by reducing the dislocations density, the leakage current decreases. The gold resistance increase can be due to thermally induced changes on the gold surface. A dielectric leakage current density of 158×10^{-7} A/cm^2 at 600 V DC was measured with an average decrease of 71.61% of leakage current after temperature cycling. The die shear test strengths before and after thermal aging and temperature cycling were higher than the MIL-standard value of 5kg-F. In summary, in the double-layered ceramic substrate, promising material and process were suggested to utilize in the packaging substrate. Different mechanical and electrical reliability tests were carried out on the double-layered ceramic substrate and were tested at 500°C for extended hours (up to 1540 hours which will be expected to operate). The die shear strength value satisfied the required standard (MIL-STD) and dielectric leakage current value (for 600 V DC). All reported results prove the operation of this packaging architecture at the Venusian condition with low-reliability risk.

5.3 Dissertation Recommendations for Future Research Work

High-temperature capable electronic packaging is developing quickly, due to higher demand in high-temperature technologies, such as in automotive, aerospace, etc. The work

presented in this dissertation could be extended with the following recommendations and possible suggestions for future work.

The objective of this research was to fabricate an electronic packaging architecture to withstand Venus's condition for extended hours to evaluate the package's performance and reliability. Die, die-attach, encapsulation material, wire bonds, package housing were evaluated and tested at the Venus chamber simulator and reported reliability results were shown the utilized materials and packaging architecture met the minimum required reliability standards. This packaging technology tested at 500°C for up to 1540 hours, different reliability tests performed on the package and components including thermal aging, temperature cycling, wire bond pull test, acid, and corrosion tests.

The reported packaging architecture is adaptable to different applications including high power, high frequency, and related fields. For instance, by replacing the alumina substrate with high-temperature co-fired ceramic (HTCC) substrate, the package will be an appropriate candidate for high-frequency applications, and high power devices can be utilized along with thicker wire bonds for high power applications. The package and substrate size can be modified to a smaller or bigger scale, for single- or multi-chip applications. The ceramic encapsulation materials can be 3D printed on the top of components to achieve more accurate and uniform encapsulation coverage, this can facilitate the manufacturability of the ceramic encapsulants.

Appendix

Appendix A: Supplementary information for chapter 2

A.1 NOMENCLATURE

FWHM	full-width half-maximum
d_{hkl}	lattice spacing
ג	wavelength of x-ray
T	crystal size in nanometer
K	shape factor
ε	micro-strain in specific Bragg's angle of Θ
B	FWHM (deg)

A.2 XRD, FTIR, and EDX sample preparation

For XRD, FTIR, and EDX process, the sample preparation procedure was identical. The ceramic paste was prepared in two forms of bulk and powders. First, different percentages of nanosilica ceramic pastes were synthesized and cast in a dome shape (hemisphere) form on a bare 5 cm × 5 cm alumina substrate and were cured with their corresponded curing profile. The cured domes were taken off from the alumina substrate by a metal scriber. The dome shape bulks were ground by manual milling jar. The powder and dome shape bulks were used for all tests. For the XRD test, sample thickness should not be exceeded from a certain number (~2mm) to be detectable by -Ray. For the XRD test, the powder form has a privilege than bulk shape material. The XRD sample holder should be a doubled glass coverslip bonded together which was mounted to the XRD sample holder's slot. Double-sided tape was attached to the top of the glass holder and

ground ceramic powder placed on the tape and compacted by a spoon tool. The adhesive tape and compression help to keep powders attached to the sample holder during the test.

A.3 SEM and cross-sectional images: sample preparation

For the SEM imaging system, a conductive surface is required to be detected by the electron beam. For ceramic or non-conductive surfaces imaging, a set of processes is required to make a conductive surface. After the die-attach process on the substrate, resin and activator (5:1) were mixed and poured on the vertically mounted substrate and cured at 50°C for 8 hours. The bond line cross-section was cut by low-speed saw equipment at the bond line interface. The bond line interface was polished by different sizes of the polishing papers using Buehler Surf met Variable speed grinder-polisher. Different sizes of the polishing papers were used such as 45, 15, 9, 6, 3, 1µm. Diamond suspended liquids were frequently sprayed at the polishing interface.

Different cross-sectional images were taken before and after each polishing step for surface quality control. After the final polishing process (1µm size) on the interface using different directions (clockwise and counterclockwise), the samples were transferred for the metal plating process. An IPA cleaning process is required followed by 1-hour baking (outgassing) at 50°C. Copper ribbons were installed around the polymer resins and those were prepared for metal deposition. A 4nm platinum thin film was sputtered by a Hummer sputtering system on the top of hardened resin. The Argon plasma was utilized to sputter the platinum on the surface. The surface was ready at this stage for SEM imaging or any other interface inspections. Figure A.1 shows the polymer resins with an embedded ceramic interface.

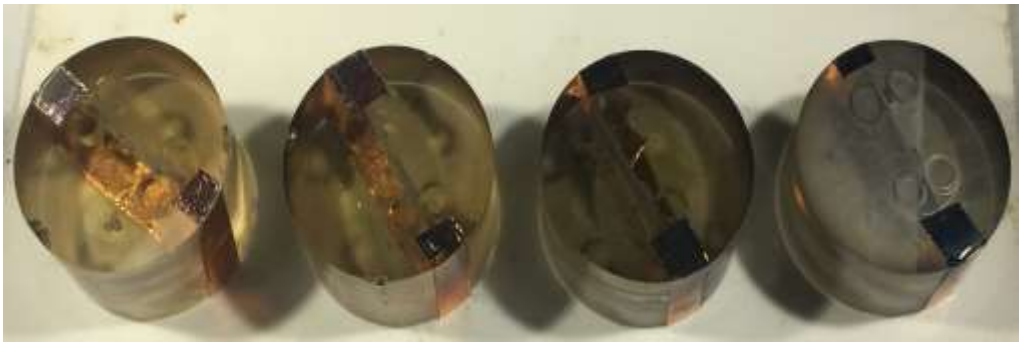

Figure A.1 Ceramic bond line interface embedded in cylindric polymer resin with the platinum and copper metalization

Appendix B: Supplementary information for chapter 3

B.1 Acid test

In addition to section 3.3.5, the acid test was conducted by immersing the encapsulated wire-bonded gold package into the sulfuric acid (80% and 95% wt.% sulfuric acid) for 24 hours. The gold wire bond resistance increased by 26.94 % which could be due to oxidation of the gold material.

B.2 Corrosion test process flow

The copper serpentine resistor was designed by AUTOCAD and the lithography process was carried out on Direct Bonded Copper (DBC) board using a dry film laminator process. The copper etch process was performed by the Chemcut acid etching system. The developer and striper immersion were carried out before and after the Chemcut etching process. After the photolithography process, 6 identical copper serpentine patterns were formed on the DBC board. The DBC board was diced down to dice down to form 6 identical coupons using dicing saw equipment. Two identical serpentine coupons were selected and the same copper traces were covered by Kapton tape. Both coupons were immersed inside the Ferric Chloride and resistance of the copper traces was measured across the encapsulation coverage before and after the corrosion test. A digital handheld multimeter device was utilized to measure electrical resistance. Figure B.1 shows the process flow of the corrosion test.

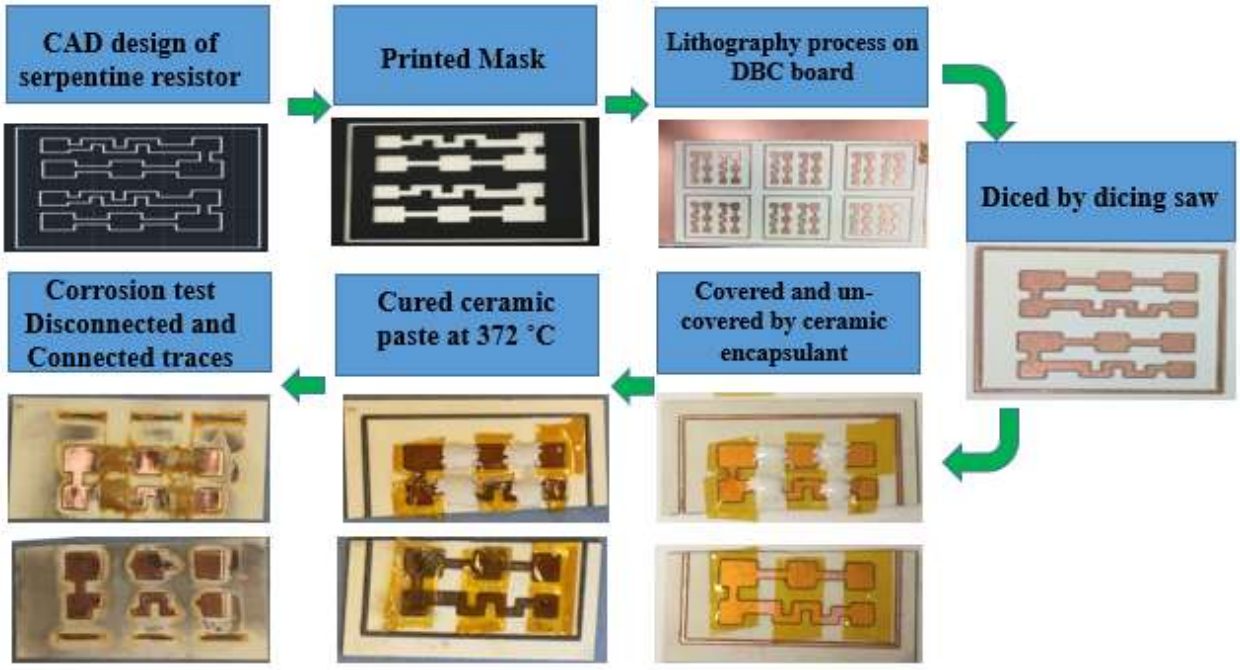

Figure B.1 Process flow for the corrosion test