5-2020

Investigations of New Fault-Tolerant Methods for Multilevel Inverters

Haider Mhiesan
University of Arkansas, Fayetteville

Investigations of New Fault-Tolerant Methods for Multilevel Inverters

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy in Engineering with a concentration in Electrical Engineering

by

Haider Mhiesan
University of Kufa
Bachelor of Science in Electrical Engineering, 2007
University of Arkansas
Master of Science in Electrical Engineering, 2016

May 2020
University of Arkansas

This dissertation is approved for recommendation to the Graduate Council.

H. Alan Mantooth, Ph.D.
Dissertation Director

Roy McCann, Ph.D.
Committee Member

Yue Zhao, Ph.D.
Committee Member

Cynthia Sides, Ph.D.
Committee Member

ABSTRACT

The demands of power electronics with high power capability have increased in the last decades. These needs have driven the expansion of existing power electronics topologies and developing new power electronics generations. Multilevel inverters (MLI) are one of the most promising power electronics circuits that have been implemented and commercialized in high-voltage direct current (HVDC), motor drives, and battery energy storage systems (BESS). The expanding uses of the MLI have lead to creation of new topologies for different applications. However, one of the disadvantages of using MLIs is their complexity. MLIs consist of a large number of switching devices, which can result in a reduction of system reliability. There are significant challenges to the design of a reliable system that has the MLI's capability with integrated fault-tolerance. In other words, design a system that can handle the fault, totally or partially, while maintaining high power capabilities and efficiency.

This aim of this dissertation is to investigate the fault-tolerance of MLIs from two different points of view:

1- Develop new solutions for existing MLI topologies. In other words, add some features to existing MLIs to improve their reliability when a fault occurs.
2- Design new MLIs that have a fault-tolerant capability.

A new open-circuit fault detection is proposed in this dissertation. The new fault detection method is based on monitoring the output voltage of each cell and leg voltage polarity along with each switch state. By monitoring each cell output voltage and leg voltage, the faulty cell can be detected and isolated.

A novel circuit to maintain system operation under the condition of one (or more) components suffering from a faulted condition is also proposed in this dissertation. This results in a topology that continues to operate at full capability.

Additionally, a new topology is proposed that offers reducing the number of batteries by 50%. Also, it has the ability to operate under non-unity power factor, which enables it to be suitable for battery energy storage systems, and static compensator (STATCOM) applications.

Another novel hybrid cascaded H-bridge (CHB), known as the X-CHB, for a fault-tolerant operation is proposed in this dissertation. It ensures seamless operation of the system under an open/short circuit switching fault or dc supply fault.

ACKNOWLEDGMENTS

I would like to express my gratitude to my advisor, Prof. H. Alan Mantooth for helping me along this journey. To my committee, Profs. Roy McCann, Yue Zhao, and Cynthia Sides, thank you for taking the time to be a part of my committee. I appreciate the help from the colleagues, and friends on my dissertation work: Vinson Jones, Chris Farnell, Shuang Zhao, Joe Moquin and Hazzaz Mahmud. My gratitude also goes to my colleagues: Janviere Umuhoza, Kenneth Mordi, Dereje Woldegiorgis, Yuqi Wei, Robert Murphree, Maksudul Hossain, Luciano Garcia, Nicholas Blair, Rosten Sweeting III, Justin E. Jackson, Estefano Soria, and Sloan Becker.

Special thanks to the GRid-connected Advanced Power Electronics Systems (GRAPES) research center for the funding of my dissertation work.

Special thanks to the National Center for Reliable Electric Power Transmission (NCREPT) center for always making sure I have what I need. Thank you, Chris!

Last, but certainly not least, thank you to my entire family for always supporting me with everything that I do, especially my parents. I wouldn't be here if it wasn't for you all. Thank you.

DEDICATION

This dissertation is dedicated to my parents, my wife and my kids.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 Motivation and Problem Statement

The increase in the use of renewable energies for grid-connection applications in recent years has led to a rapid increase in power electronics developments. One instance of this is transformerless power electronics, which increases the cost-effectiveness in grid-tied applications. The high-power requirements and needs also led to the development of a new generation of power electronics, the multilevel inverters (MLIs). MLIs provide a superior solution for high-voltage/power applications due to their modular nature. Other merits of using MLIs are reduction of the losses and electromagnetic interference (EMI), improvement of power quality, and the reduction of the switches' voltage stresses. However, one of the major disadvantages of using MLIs is increasing the system complexity. The high number of switches in MLIs will also increase the number of gate drivers and sensor/conditioning boards. Increasing the number of switches also increases the probability of switching failures, which in turn decreases system reliability.

This dissertation proposes new MLI circuits providing novel methods for maintaining system operation in case of one (or more) fault occurrences. The proposed topologies with fault-tolerant ability leads to a system that can produce the same output voltage/current after the fault happens. The advantages of the new circuit topologies with fault-tolerance capability are more visible in the application such as hospitals, airports, and transportation.

Some of the existing fault-tolerant circuit topologies require backup circuits that have no functionality until a fault occurs, which results in higher implementation costs. Other circuits provide reliable systems for faults, but the power quality of system is reduced.

Also, these methods cannot maintain the same control method after a fault. For instance, in a

battery energy storage system (BESS), it is required to balance all the batteries within their designed values. The battery pack for all the cells in one phase, and in all the phases, should be balanced. If there is fault in one cell, this cell is removed from the system. One of the suggested solutions is to replace the defective cell with a backup battery. The SoC (State of Charge) of the backup batteries is almost 100%, while the system batteries' are not. Consequently, adding the backup batteries to the system with different SoC percentages leads to control issues to maintain the balance of the entire system.

Previous methods in the literature cannot be implemented for all types of MLIs. In fact, most of these circuits are designed for a specific MLI while the proposed method can be implemented for a large variety of MLIs.

This dissertation explores fault-tolerant techniques for MILs. The goal was to both investigate a new fault-tolerant method for the existing topologies and to develop a new topology with fault-tolerance ability. Figure 1.1 demonstrates the goals of this dissertation.

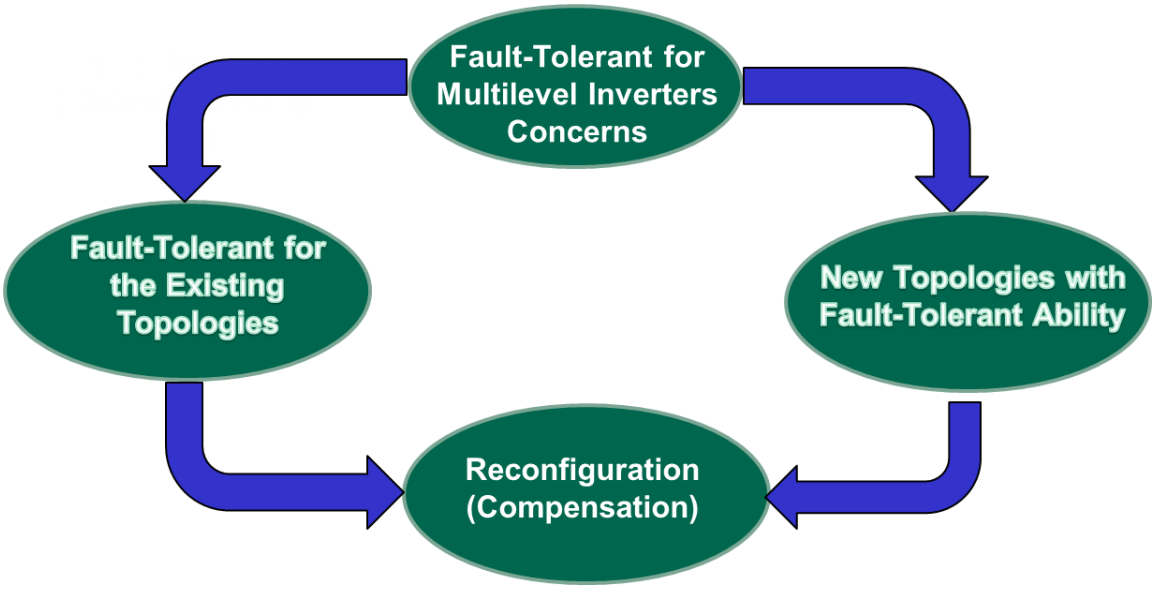


Figure 1.1 Dissertation two-fold goal of achieving fault-tolerant solutions for new and existing multilevel inverters.

The focus of this research work is to develop novel methods and circuit topologies for fault-tolerant operation as follows:

1- A simple and accurate novel switching fault detection and identification method for MLIs,
2- A new fault-tolerant topology that provides a reconfiguration ability for existing power electronics applications,
3- A novel inverter with a lower number of switches and boosting ability for fault-tolerant operation that can be suitable for different power system applications,
4- A novel multilevel inverter with fault-tolerance capability to ensure a reliable and robust operation of the converter in the event of an open/short circuit switching fault or dc supply faults, and
5- A fault detection and identification building block that can be applied to a wide variety of MLI topologies.

1.2 Organization of the Dissertation

The chapters covering the main contributions are organized in Figure 1.2. This work is organized into seven separate chapters. The content of each chapter is summarized below:

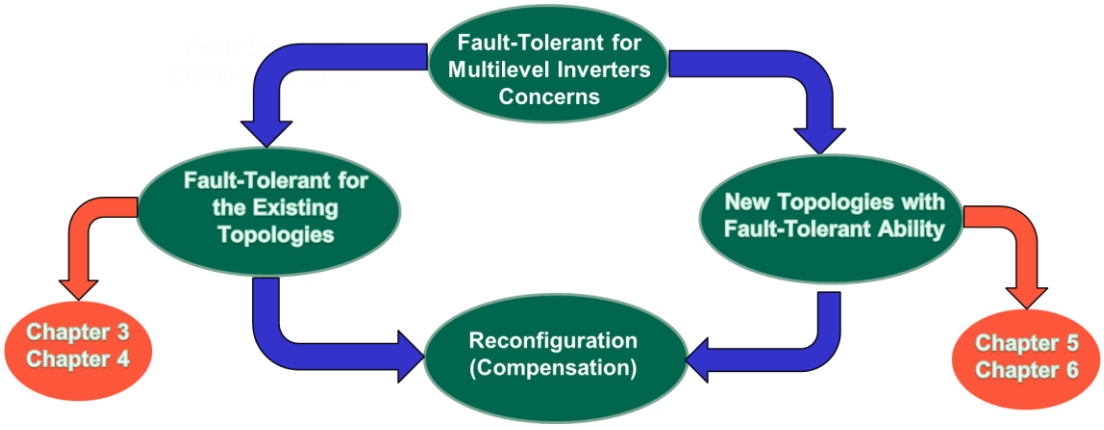


Figure 1.2 Organization of the novelty chapters of this dissertation.

Chapter 2: A comprehensive survey of existing fault-tolerant topologies is presented with emphasis on their drawbacks. The requirements and needs for reliable MLIs are described as well.

Chapter 3: This chapter proposes a novel switching fault detection and identification method for MLIs. It presents a simple method to identify the defective faulty cell and switch in comparison to the existing methods. It is found that there is a relationship between the leg voltage polarity and PWM signals to detect the fault. Simulation and experimental verification of the proposed concept is demonstrated using a seven-level cascaded H-bridge CHB inverter.

Chapter 4: This chapter presents a new fault-tolerant topology that provides reconfiguration capability for power electronics applications. It enables the inverter to isolate the faulty device in a way that the circuit can continue operating as a pre-fault condition and, therefore, reduce the disruption of electrical power delivery upon fault occurrence. It is worth pointing out that all the above is implemented to achieve a cost reduction in the overall system. Simulation and experimental verification of the proposed concept is demonstrated using a seven-level CHB inverter.

Chapter 5: The main objective of this chapter is to develop a novel inverter with a smaller number of switches in combination with output voltage boosting ability. The proposed topology offers a reduction in the number of batteries by 50%. Also, it can operate under non-unity power factor, which makes it suitable for battery energy storage systems and STATCOM applications. Each cell of the proposed topology, the X-CHB topology, can generate either 5-level or 7-level output voltage waveforms.

Chapter 6: A fault-tolerant approach for a CHB inverter is described in this chapter. The added features ensure reliable and robust operation of the converter in the event of faults. The proposed

strategy uses an additional cross-coupled CHB (X-CHB) unit in combination with the existing CHB to support the output voltage and ensure continuity of operation in the event of an open/short circuit fault. The operation of the proposed X-CHB inverter is described in detail. Simulation and experimental verification of the proposed concept is demonstrated using a seven-level CHB inverter. Both simulation and experimental results validate the fault-tolerant operation of the CHB inverter for a battery energy storage system (BESS) in case of switch faults, such as open/short-circuit switch fault or a dc-source or battery failure.

Chapter 7: The final chapter focuses on the conclusions drawn from the efforts presented in this dissertation.

CHAPTER 2

BACKGROUND ON FAULTS IN MULTILIVEL INVERTERS

2.1 Reliability Considerations for MLIs

By March 2017, 10% of US electricity was generated through solar photovoltaics and wind turbines [2.1]. This number is predicted to rise in the upcoming years. The energy produced through renewable sources requires power electronic converters to make it suitable for use in the electricity grid. This precedent has resulted in an expeditious rise of research and development on semiconductor devices. Providentially, the research in SiC devices has provided the capabilities for high switching frequencies and breakdown voltages that open doors to new applications. With the help of the new semiconductor devices, numerous advances have been made in expanding the topologies suitable for medium voltage applications. However, there is still a need for higher voltage switches to be developed. For instance, devices with more than 10 kV breakdown voltage are necessary for integration of Battery Energy Storage Systems (BESS) to a 13.8 kV grid. Since these devices have not been commercialized yet, the series connection of lower-rated devices is used to reach the desired breakdown voltage. Multilevel Inverter (MLI) is the term used for power electronic converters that consist of series-connected, or cascoded, devices to achieve the goal of achieving higher breakdown voltages.

Reliability is defined by the system's ability to maintain a high probability of successful operation with an desired lifetime goal. A reliable converter should be able to survive and tolerate any type of fault [2.2]. Increasing the reliability of power electronics system in a cost-effective and efficient manner has always been one of the main objectives of industrial and academic researchers in power electronics as means to guarantee robust power electronics applications. Consequently, more investigation into highly reliable power electronics is one of the most critical needs in the

power electronics research and industry. For many years, a substantial impediment to widespread deployment of grid-connected power electronics was the lifetime and reliability of silicon power electronics. This was exacerbated by the need to aggressively cool the silicon power electronics, which drives up system costs and further impacts reliability with redundant cooling systems. Wide bandgap power electronics, particularly silicon carbide, offer the opportunity to conquer these issues in electric power grid applications. This dissertation will address the circuit-level aspects of this equation.

Power electronics reliability studies can loosely be categorized into three studies as is described in the following [2.3].

1- Analysis: reliability studies for analysis of the power electronics failure causes.
2- Design: to design a reliable power electronics system. In other words, this is focusing on the reliability during the design stage.
3- Solution: techniques and control methods that ensure a reliable power electronics system that can handle all ramifications.

Other keen insights into the reliability concerns are as the following questions:

1- What electric components should be considered as the most critical components that might cause power electronics' failures and have a negative impact on the system reliability? Are power semiconductors the only device that should be considered?
2- Are the power electronics reliability concerns the same for all power electronics applications and topologies?
3- Are there limitations with the existing reliability solution methods?

Fault in any of the components can result in the failure of the overall power electronic system. These components include semiconductor devices, capacitors, inductors, solder tracks, and PCB

boards. Each component has a different failure rate that can be calculated through various methods using the available standards in conjunction with the element losses, junction temperatures, etc.

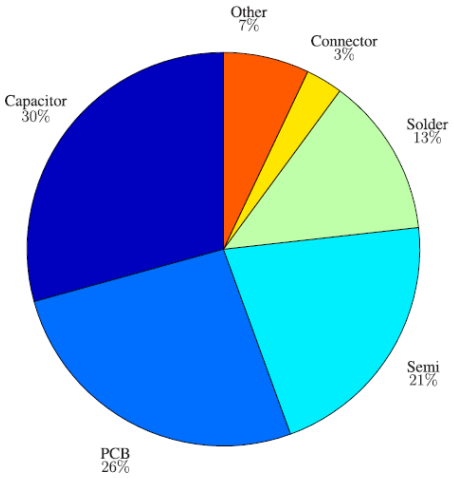


Figure 2.1 Distributions of faults in a power converter [2.7].

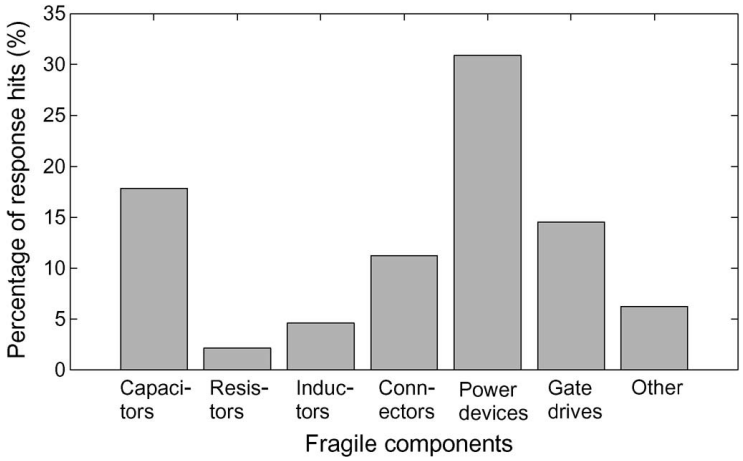
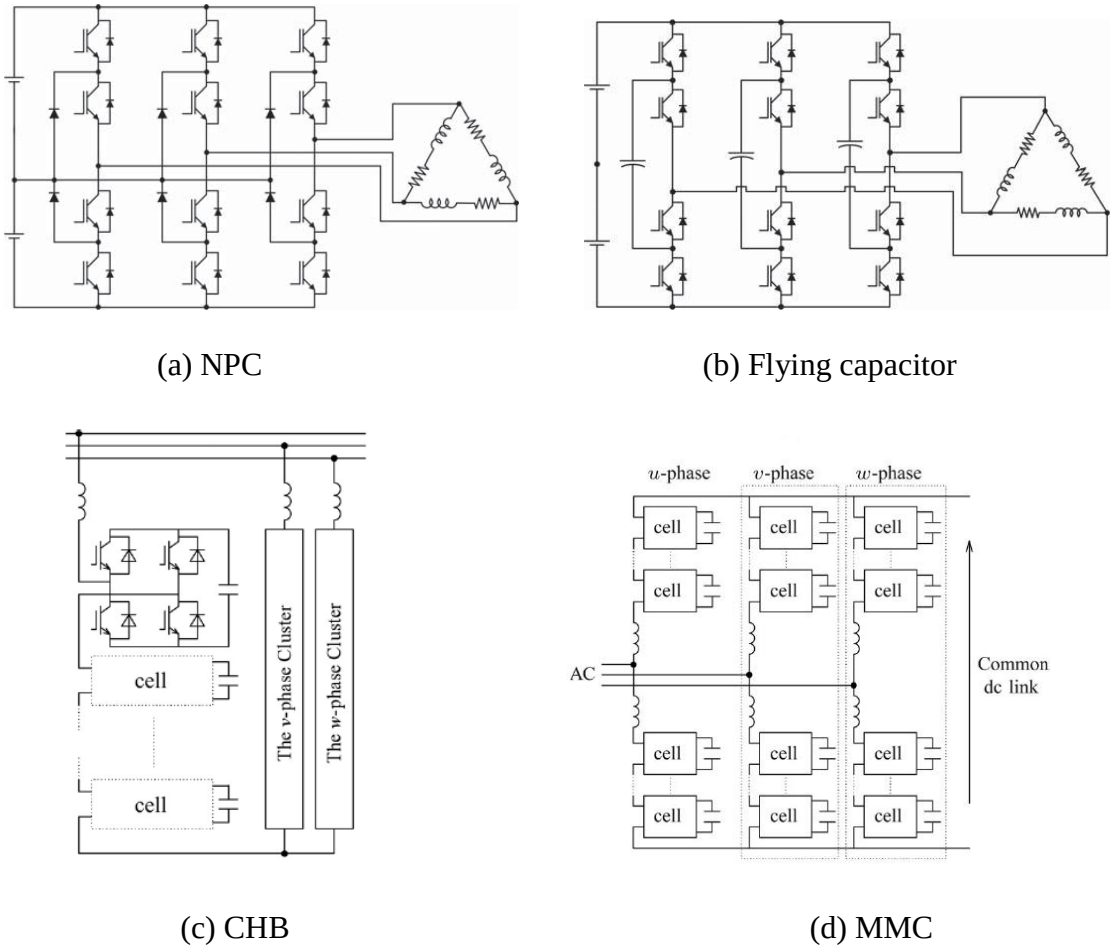


Figure 2.2 Distributions of fragile components [2.6].

[2.4]-[2.5] show that approximately 21% of the power converter failure is due to semiconductor faults as shown in Fig. 2.1. Additionally, 39% of the system failures are caused by the failure in the soldering and PCBs. A survey research conducted of more than 60 companies in [2.6] revealed that the semiconductor power devices have the highest hazard rate amongst power

electronic components and correspond to 31% of system failures. [2.6] further showed that 15% of the power converter failures are due to faults in the gate drivers as shown in Figure 2.2.



(a) NPC (b) Flying capacitor

(c) CHB (d) MMC

Figure 2.3 MLI configurations (a) Neutral Point Clamped (NPC), (b) Flying Capacitor, (c) Cascaded H-Bridge, and (d) Modular Multilevel [2.9].

An increase in the number of components translates into higher failure possibility. Multilevel inverters (MLIs) have been established as one of the most popular topologies in power electronics as they provide high power quality and effective performance. The different types of MLIs presented in the literature are shown in Figure 2.3. Prevalent instances of multilevel inverter topologies are the neutral point clamped (NPC), Flying Capacitor, and cascaded H-bridge (CHB). Among all the types of MLIs, the CHB inverter is the most suitable solution for Battery Energy Storage System (BESS) applications [2.8].

The large number of power semiconductor devices in MLI topologies increase the chance of device faults. These faults can be categorized into two groups: open-circuit and short-circuit faults [2.9]-[2.11]. Short-circuit fault detection and mitigation methods are provided with hardware solutions that are integrated with the commercialized gate drivers.

These methods are designed to soft turn-off off the device as soon as a fault occurs [2.12]. Despite these efforts, there are no hardware solutions capable of open-circuit fault detection. Open-circuit faults are the reason for 15% of the failures and may occur due to wire bond lift-off and cracking of the solder layers [2.13]. When this type of fault occurs with MLIs used for the BESS applications, it causes an unbalanced output current and voltage. This may result in the shutdown of the overall system supplied by the MLI. A system shutdown in medium and high-voltage scenarios can potentially result in disastrous and expensive downtime conditions for industrial and commercial loads.

2.2 Fault Diagnostic Survey

Numerous studies have been conducted on the failures in semiconductors. In order to conquer the reliability concerns in the event of open-circuit device failures, a simple, fast, and accurate solution for fault detection is required. Previous research in [2.14]-[2.15] reports approaches that can successfully identify the faulty cascaded H-bridge cell. However, these methods cannot detect the specific faulty switch. Consequently, these methods cannot lead to sufficient and accurate detection. Other work in [2.16]-[2.17] rely on at least two cycles required to identify the fault. These approaches result in a complicated and complex fault detection strategy. In addition, these methods require many sensor boards, which results in a higher fault location time, and higher overall system cost. The methods in [2.18] are designed for neutral point clamped inverters by monitoring the voltage polarity and its time frame. As a result, it can just detect a

general fault, but it cannot locate the fault.

In [2.19], the authors utilized the comparison of the predicted and measured values of an MLI for fault detection purposes. Once again, this method can only detect the faulted submodule (SM) and not the precise faulty switch. Furthermore, the detection time required for the method is an unsatisfying 33 *ms*. The approach in [2.20] cannot be applied to nonlinear loads, where nonlinear loads are common for most commercial and industrial loads. This approach causes reduced accuracy due to the lack of any other parameters used in the comparison other than the voltage.

Other detection approaches utilize observer and neural-network-based strategies for fault detection. [2.21] uses a sliding mode observer-based method to detect the faulty switch. It monitors the cells' capacitor voltages and each leg voltage. Nevertheless, this method requires a detection time of more than 200 *ms* for evaluating each cell for a fault. A neural-network-based method for switch fault identification is proposed in [2.22] that monitors the CHB output voltage for fault detection. The training data time in this method for covering the large operation regions results in inaccurate results. In [2.23], a detection approach was successfully implemented that could identify the defective switch in NPC converters feeding synchronous motor drives. However, this method requires a large number of current measurement boards in each of the NPC legs.

The method in [2.24] proposed another fault detection method using a neutral shift technique. This method is applicable to a specific kind of PWM (Phase-Shifted) strategy. However, this approach cannot be implemented with other PWM strategies.

All in all, there is a need for a highly reliable and rapid detection method that can guarantee: 1) cost-effective solutions, 2) fast response times, and 3) very high accuracy.

2.3 Reconfiguration Survey

Fault detection methods help find the defective switches, but what happens after the accurate fault detection? An approach is required that, in addition to fault detection, can isolate the defective switch as a means to increase the reliability of the converter and thus the renewable energy system as a whole. Moreover, power electronics are required for grid BESS to shape the voltage and frequency during heavy load, or reduced wind. The previously available literature can be divided into two categories. The first subset focuses on isolation of the defective cell that often causes lost functionality and degraded operation. Another subset revolves around utilization of a backup battery pack that noticeably increases the entire system cost.

As previously indicated, one of the approaches for MLIs facing faults is to bypass the defective cell. This is achievable through the addition of four electromagnetic contactors (relays) in each cell [2.25]-[2.33]. In case of faults, these electromagnetic contactors isolate the faults and connect the faulty dc link to a healthy cell, as displayed in Figures 2.4 and 2.5. This method is not practical in the case of medium-voltage applications for several reasons. The first reason is that adding a battery pack to a healthy cell would result in destroying the semiconductor devices since the voltage stress across each device will be doubled and each device has breakdown voltage limits that cannot be exceeded. Another reason is that in case of photovoltaic systems and BESS applications, the control system is required to balance the charging/discharging status. Transferring the defective cell batteries to a healthy cell will result in issues in the State-of-Charge (SoC) for the system batteries, and the controller may not be able to maintain the same balancing for the entire system's batteries under all circumstances (i.e., stability is not guaranteed). If the control system is adjusted to operate for certain SoC values, the controller cannot maintain the balance of the inverter's battery after the dc-link transfer since the expected SoC would change. The

expensive nature of this solution, due to the high cost of high-voltage circuit breakers, is another reason why this approach is not viable. These circuit breakers need to be capable of handling voltage levels equal to that of the phase voltage. Additionally, in these methods, the switches are required to be designed for higher breakdown voltages for handling the added battery voltages; resulting in an even higher implementation cost. In case of fault occurrence, the inverter voltage level would change significantly.

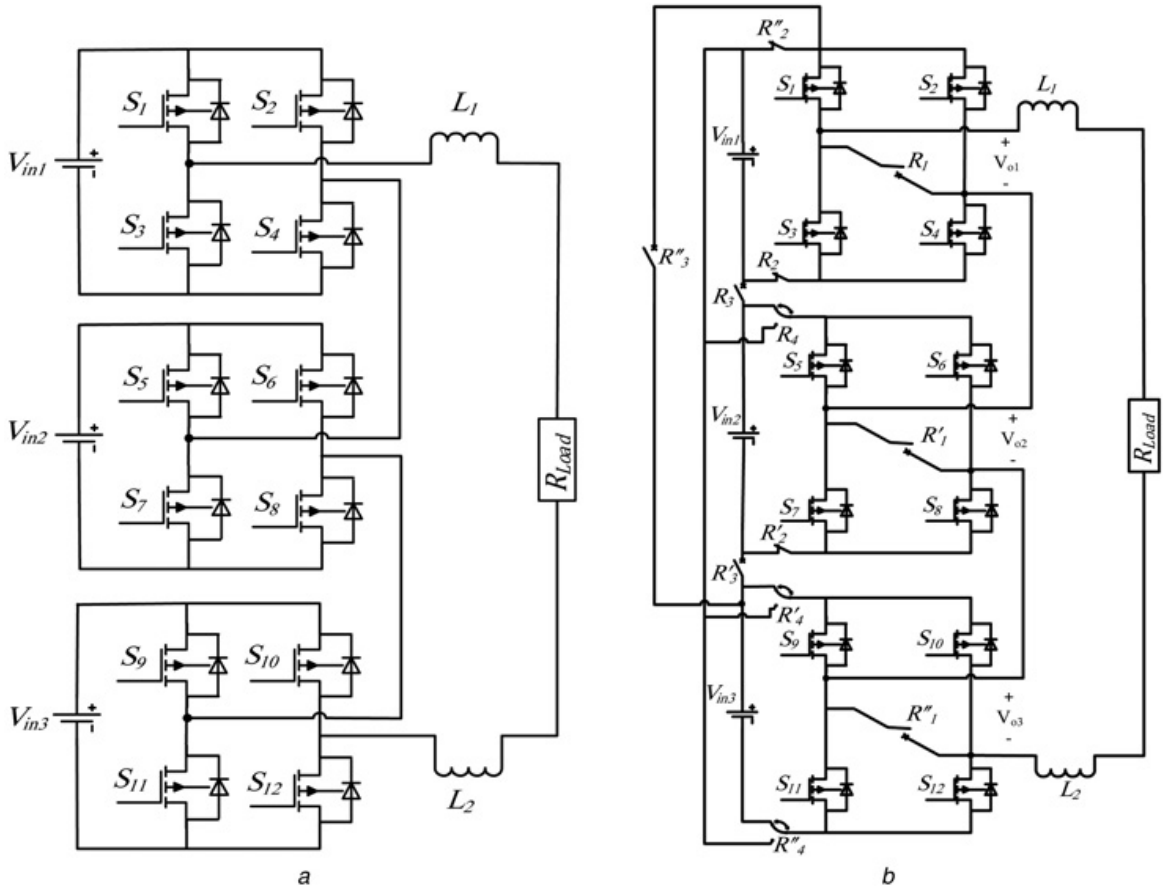


Figure 2.4 A fault reconfiguration method using additional electromagnetic contactors (relays) in each cell [2.25].

After disconnection of a cell, the change in the output voltages, current ripples, and THD are very high. In any power electronics design, the output current ripple and THD must be decreased to meet the standard requirements. For instance, the current ripple should not exceed 5% while

avoiding resonance frequency and maintaining low THD. The THD can be reduced using an output filter, which could be an L, LC, or LCL filter. The filter is required to smooth the output waveforms. With all the above considerations, the bypassing methods still have not addressed the concerns of the inverter output filter to meet worst-case scenarios.

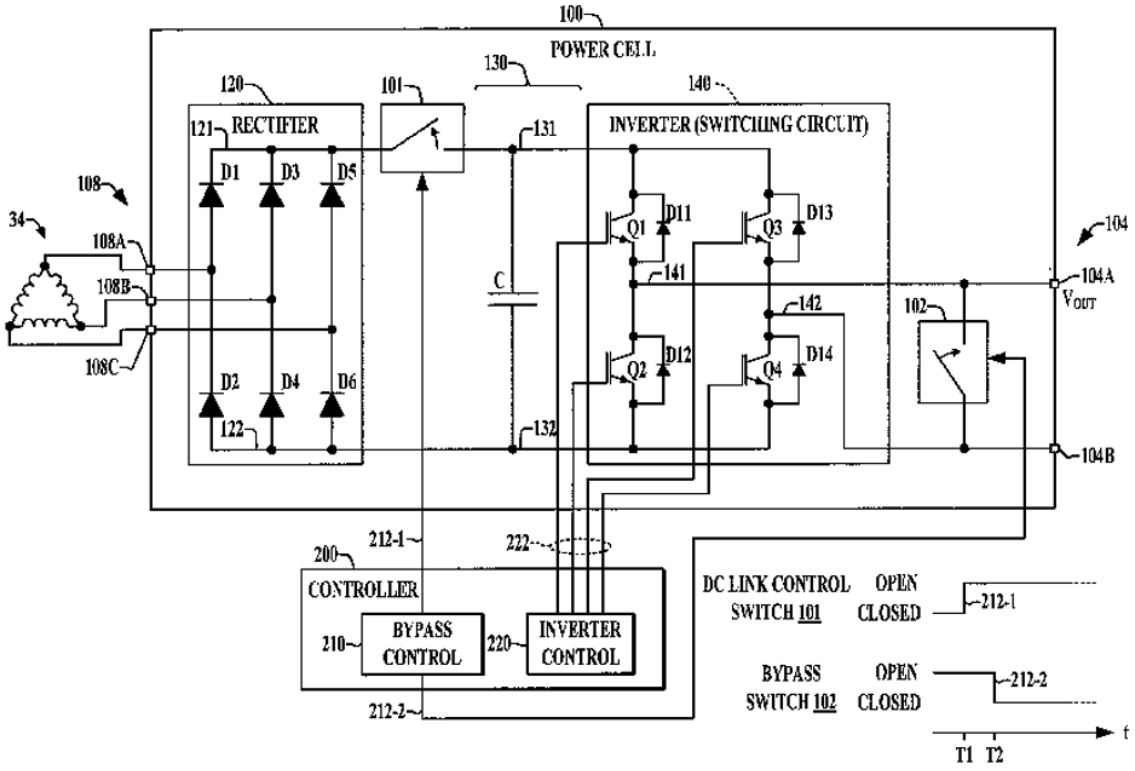
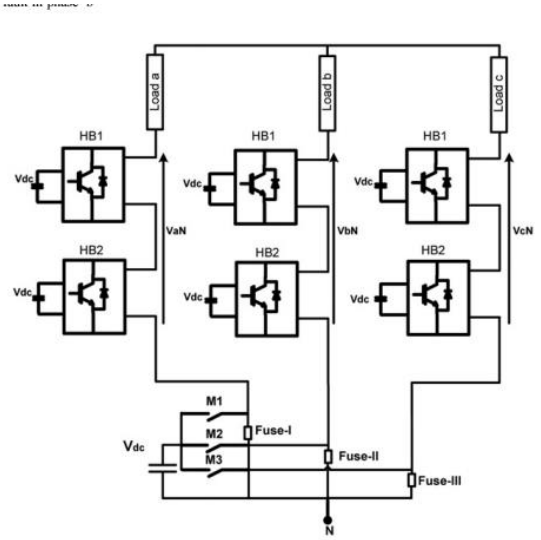


Figure 2.5 A fault reconfiguration method using additional electromagnetic contactors (relays) in each cell [2.27].

The alternative solution is to use redundant sub-circuits, as shown in Figure 2.6. This solution would need either an extra cell of switches or standby batteries [3.34]-[3.36]. The standby sub-circuits would enter operation after the event of a fault. These approaches have multiple disadvantages. External batteries would be too costly for medium and high-voltage applications. Also, these redundant switches or batteries would not be utilized until a fault happens. In the case of a four-cell inverter, the batteries cost with an extra cell is raised by a factor of four for one phase.

Furthermore, these methods cannot continue fault-tolerant operation when another fault happens at the same phase. Consequently, the ability of this type of method is limited to address a fault per phase and cannot guarantee robust operation. To further grasp the problems that these methods cause for the SoC balancing, assume a failure occurs when the SoC is at 40%. The extra newly added battery SoC would be at 100%. In this case, the controllers would not be able to balance the entire system. The premise of the presented novel fault-tolerant reconfiguration method for CHB inverters under fault conditions is to address and solve these concerns.



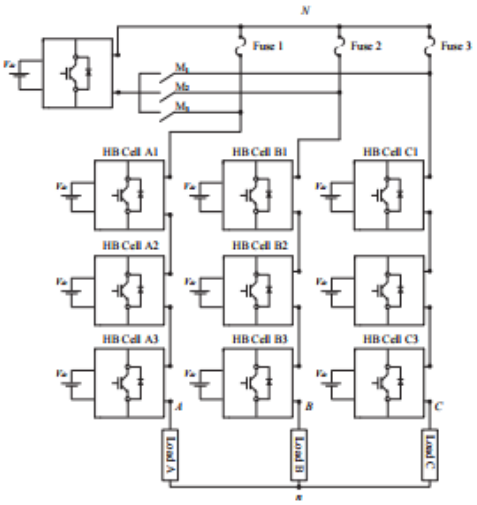


Fig. 2 Structure of presented fault-tolerant solution

Figure 2.6 Redundant reconfiguration methods [2.35]-[2.36].

Having said that, the existing fault-tolerant topologies still need improvement. Also, many studies relate the fault-tolerant topologies with the effect on the system power quality. There are few studies that create new fault-tolerant topologies for MLIs. In addition, there are studies which suggest new topologies that have the fault-tolerant ability. For these reasons, there is a need for a new method for fault-tolerance capability that has:

1- Cost-effectiveness of the designed topology resulting in the affordability of the system,

2- Simple operation under fault conditions where there is no need for changing the system's controllers,

3- A reliable system that operates under multiple fault conditions while maintaining the power quality for the systems,

4- A robust system for some specific military and navy applications that ensure continual operation under fault conditions, and

5- Resilience to operate at medium-voltage applications.

2.4 References

[2.1] EIA ,"Wind and solar in March accounted for 10% of U.S. electricity generation for first time" [Online]. Available at: https://www.eia.gov/todayinenergy/detail.php?id=31632/ [Accessed 9-Apr-2018]

[2.2] D.L. Steiner,"Lay the Foundation for a Truly Reliable Electrical System" [Online]. Available at: http://www.dlsteiner.com/electrical-reliability-study/ [Accessed 9-Apr-2018]

[2.3] U. M. Choi, F. Blaabjerg and K. B. Lee, "Study and Handling Methods of Power IGBT Module Failures in Power Electronic Converter Systems," in *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2517-2533, May 2015

[2.4] H. Dan *et al.*, "Error-Voltage-Based Open-Switch Fault Diagnosis Strategy for Matrix Converters with Model Predictive Control Method," in *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4603-4612, Sept.-Oct. 2017

[2.5] P. Lezana, R. Aguilera and J. Rodriguez, "Fault Detection on Multicell Converter Based on Output Voltage Frequency Analysis," in *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 2275-2283, June 2009.

[2.6] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran and P. Tavner, "An Industry-Based Survey of Reliability in Power Electronic Converters," in *IEEE Transactions on Industry Applications*, vol. 47, no. 3, pp. 1441-1451, May-June 2011.

[2.7] *Handbook for Robustness Validation of Automotive Electrical/Electronic Modules*. Frankfurt, Germany: ZVEL, Jun. 2008

[2.8] H. Akagi, "Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC)," in *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3119-3130, Nov. 2011.]

[2.9] Euzeli dos Santos; Edison R. da Silva, "Power Electronics Converters Processing AC Voltage and Power Blocks Geometry," in *Advanced Power Electronics Converters:PWM Converters Processing AC Voltages* , 1, Wiley-IEEE Press, 2014, pp.376-4.

[2.10] J. He, N. A. O. Demerdash, N. Weise and R. Katebi, "A Fast On-Line Diagnostic Method for Open-Circuit Switch Faults in SiC-MOSFET-Based T-Type Multilevel Inverters," in IEEE Transactions on Industry Applications, vol. 53, no. 3, pp. 2948-2958, May-June 2017.

[2.11] J. Wang, H. Ma and Z. Bai, "A Submodule Fault Ride-Through Strategy for Modular Multilevel Converters With Nearest Level Modulation," in IEEE Transactions on Power Electronics, vol. 33, no. 2, pp. 1597-1608, Feb. 2018.

[2.12] H. Zhao and L. Cheng, "Open-circuit faults diagnosis in back-to-back converters of DF wind turbine," in IET Renewable Power Generation, vol. 11, no. 4, pp. 417-424, 3 15 2017.

[2.13] C. Brunson, L. Empringham, L. De Lillo, P. Wheeler and J. Clare, "Open-Circuit Fault Detection and Diagnosis in Matrix Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2840-2847, May 2015.

[2.14] V. F. Pires, T. G. Amaral, D. Foito and A. J. Pires, "Cascaded H-bridge multilevel inverter with a fault detection scheme based on the statistic moments indexes," 2017 11th IEEE International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Cadiz, 2017, pp. 193-198.

[2.15] H. W. Sim, J. S. Lee and K. B. Lee, "op," 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, 2014, pp. 2101-2106.

[2.16] H. W. Sim, J. S. Lee and K. B. Lee, "Detecting Open-Switch Faults: Using Asymmetric Zero-Voltage Switching States," IEEE Industry Applications Magazine, vol. 22, no. 2, pp. 27-37, March-April 2016.

[2.17] K. Thantirige, A. K. Rathore, S. K. Panda, S. Mukherjee, M. A. Zagrodnik and A. K. Gupta, "An open-switch fault detection method for cascaded H-bridge multilevel inverter fed industrial drives," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 2159-2165.

[2.18] T. J. Kim, W. C. Lee and D. S. Hyun, "Detection Method for Open-Circuit Fault in Neutral-Point-Clamped Inverter Systems," in *IEEE Transactions on Industrial Electronics*, vol. 56, no. 7, pp. 2754-2763, July 2009.

[2.19] F. Deng, Z. Chen, M. R. Khan and R. Zhu, "Fault Detection and Localization Method for Modular Multilevel Converters," in *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2721-2732, May 2015.

[2.20] A. Anand, N. Raj, S. George and G. Jagadanand, "Open switch fault detection in Cascaded H-Bridge Multilevel Inverter using normalised mean voltages," 2016 IEEE 6th International Conference on Power Systems (ICPS), New Delhi, 2016, pp. 1-6.

[2.21]] S. Shao, P. W. Wheeler, J. C. Clare and A. J. Watson, "Fault Detection for Modular Multilevel Converters Based on Sliding Mode Observer," in *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 4867-4872, Nov. 2013.

[2.22] S. Khomfoi and L. M. Tolbert, "Fault Diagnosis and Reconfiguration for Multilevel Inverter Drive Using AI-Based Techniques," in *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2954-2968, Dec. 2007.

[2.23] S. Farnesi, P. Fazio and M. Marchesoni, "A new fault tolerant NPC converter system for high power induction motor drives," *8th IEEE Symposium on Diagnostics for Electrical Machines, Power Electronics & Drives*, Bologna, 2011, pp. 337-343.

[2.24] L. Maharjan, T. Yamagishi, H. Akagi and J. Asakura, "Fault-Tolerant Operation of a Battery-Energy-Storage System Based on a Multilevel Cascade PWM Converter with Star Configuration," IEEE Transactions on Power Electronics, vol. 25, no. 9, pp. 2386-2396, Sept. 2010.

[2.25] Zargari,, N., Xiao,, Y. and Wei,, L., Method and apparatus for bypassing cascaded H-Bridge (CHB) power cells and power sub cell for multilevel inverter. US9425705B2, 2012.

[2.26] M. M. Haji-Esmaeili, M. Naseri, H. Khoun-Jahan and M. Abapour, "Fault-tolerant structure for cascaded H-bridge multilevel inverter and reliability evaluation," in IET Power Electronics, vol. 10, no. 1, pp. 59-70, 1 20 2017.

[2.27] Peter Willard Hammond, "Device and system for bypassing a power cell of a power supply", US8441147B2, 2014.

[2.28] Peter Willard Hammond, "Method for operating a multi-cell power supply having an integrated power cell bypass assembly", UUS20080174182A1, 2006.

[2.29] Lixiang Wei, Yuan Xiao, Haihui Lu, Douglas B. Weber, ", Power cell bypass method and apparatus for multilevel inverter", US20140268928A1, 2013.

[2.30] Peter Willard Hammond, "System for bypassing a power cell of a power supply", US20080079314A1, 2006.

[2.31] Peter Willard Hammond, Integrated power cell bypass assembly and power supply including same, US7568931B2, 2006.

[2.32] Peter Willard Hammond, Method and system for bypassing a power cell of a power Peter Willard Hammond, Integrated power cell bypass assembly and power supply including same, US7568931B2, 2006.supply, US20090073622A1, 2007.

[2.33] P. Moamaei, H. Mahmoudi and R. Ahmadi, "Fault-tolerant operation of cascaded H-Bridge inverters using one redundant cell," *2015 IEEE Power and Energy Conference at Illinois (PECI)*, Champaign, IL, 2015, pp. 1-5.

[2.34] M. Aleenejad, H. Iman-Eini and S. Farhangi, "Modified space vector modulation for fault-tolerant operation of multilevel cascaded H-bridge inverters," in *IET Power Electronics*, vol. 6, no. 4, pp. 742-751, April 2013.

[2.35] W. Song and A. Q. Huang, "Fault-Tolerant Design and Control Strategy for Cascaded H-Bridge Multilevel Converter-Based STATCOM," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2700-2708, Aug. 2010.

[2.36] Zhongyuan Cheng, Navid Reza Zargari "Spare on demand power cells for modular multilevel power converter", US9812990B1, 2016.

CHAPTER 3

A METHOD FOR OPEN-CIRCUIT FAULT DETECTION, IDENTIFICATION, AND ISOLATION IN CASCADED H-BRIDGE MULTILEVEL INVERTERS

3.1 Introduction and Motivation

It was established in the previous chapters that MLIs and, in particular, CHBs are highly popular choices for medium-voltage and high-voltage applications due to the simplicity and ability to provide high power quality. However, due to the high number of semiconductor switches in these topologies, methods are required to be developed for an accurate and high-speed fault detection and isolation. This is due to the fact that a fault leads to a power outage in medium and high voltage levels can have disastrous economical results. Short-circuit fault detection approaches are conventionally implemented through gate driver hardware. However, there is a need for efficient and reliable methods for open-circuit (OC) fault detection for these converters. Consequently, a novel fault detection and isolation method for open-circuit fault detection is developed, implemented, and verified as follows.

3.2 System Description

This section contains a review of the CHB converter operation under healthy and fault conditions along with a brief description of the modulation strategy utilized. The conclusions in this subsection will later be used in an explanation of the proposed open-circuit fault detection method.

3.2.1 CHB Inverter and Modulation Strategy

Figure 3.1 displays the general structure of a CHB leg with N cells per leg that is used to create a 2N+1 level phase output voltage. A single phase of the inverter is displayed for simplification purposes. Each cell is made up of an H-Bridge configuration using four SiC MOSFETs. In the event of a fault in a CHB cell, two isolation approaches are conventionally utilized: soft isolation and hard isolation. Studies make use of relays for hard isolation of faulty cells; however, this study utilized soft isolation due to the faster response time and lower costs than it provides [3.1]-[3.2].

The CHB inverter phase output voltage consists of the sum of the output voltages of the series cells in that leg. The cell switching states can be defined as $\{S_{cn,1}, S_{cn,2}, S_{cn,3}, S_{cn,4}\}$ where *n* is the number of respective cells and $S_{cn,i}(t) \in \{-1,0,1\}$. If the input dc-link voltage of each cell is V_{dc} and the output voltage of cell *n* can be denoted as V_{cn}, then $V_{cn} \in \{-V_{dc}, 0, +V_{dc}\}$ depending on the cell switching states. It should be pointed out that the top switches S_1 and S_3 have complementary operations with S_2 and S_4, respectively. Each cell of the CHB provides four unique cell states $s_n(t)$, as shown in Table 3.1.

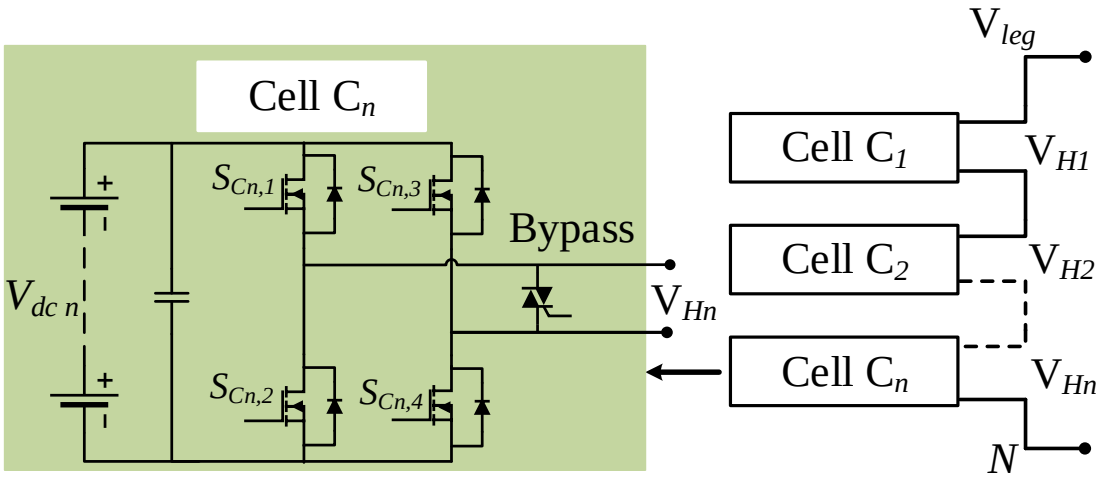


Figure 3.1 Schematic of a CHB inverter leg.

Table 3.1 Cell Switch Configuration and Corresponding Voltage

$[S_{cn,1}, S_{cn,2}, S_{cn,3}, S_{cn,4}]$	**Cell Output Voltage**	**Cell State $S_n(t)$**
[0,1,0,1]	0	0_{Lower}
[0,1,1,0]	$-V_{dc}$	-1
[1,0,0,1]	$+V_{dc}$	+1
[1,0,1,0]	0	0_{Upper}

The phase leg state can be described as a row matrix

$$L(t) = [S_1(t), S_2(t) \dots S_m(t)] \tag{3-1}$$

where $m = 4n$. Therefore, there will be 3^{4n} possible states for switches in each leg. Defining the leg voltage vector as $v_L(t) = [v_{c1}, v_{c2}, \dots, v_{cn}]$, the anticipated leg voltage for each phase could be found as

$$v_{out} = L(t)v_L(t) \tag{3-2}$$

Various Pulse Width Modulation (PWM) strategies, namely, the Space Vector PWM, Level-Shifted PWM, and Adaptive phase-shifted PWM (PS-PWM) can be utilized for control of the CHB inverter. Level-shifted PWM (LS-PWM) is the most common method due to the low harmonic content and the simplicity that it provides. It should be pointed out that some MLIs use variable dc links at the input. The OC fault identification approach proposed in this chapter is compatible with use of variable-time dc-link since this method only requires the dc-link voltage value to be known before the occurrence of a fault. To verify the performance of the presented fault detection technique, LS-PWM with in-phase disposition is used to control a 7-level CHB in sections 3.3 and 3.4. The principles of operation for this modulation scheme are shown in Figure 3.2. It can be

observed that in Figure 3.2, $S_{cn,4}$ and $S_{cn,2}$ are always conducting for $V_{leg} > 0$ and $V_{leg} < 0$. It can further be noticed that for $V_{leg} > 0$, $V_{cn} \geq 0$, and for $V_{leg} < 0$, this would always have $V_{cn} \leq 0$. This covers the basic principle of operation for the presented OC fault detection approach, which is thoroughly elaborated in the following subsections.

Leg voltage using the above scheme for 7-level cascaded H-Bridge inverter can be calculated as

$$V_{leg} = (S_{11} - S_{13})V_{dc1} + (S_{21} - S_{23})V_{dc2} + (S_{31} - S_{33})V_{dc3} \tag{3-3}$$

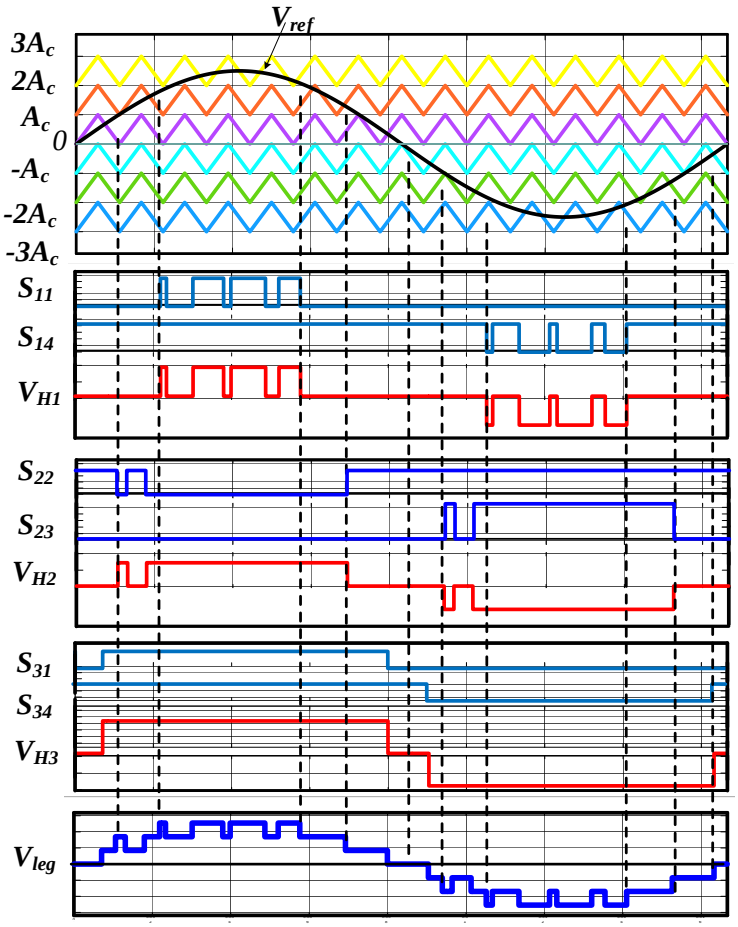


Figure 3.2 Level-Shifted PWM for 7-level CHB.

3.2.2 Behavior Analysis of the CHB under Open-Circuit Faults

As it mentioned previously, Figure 3.1 shows the structure of a CHB inverter leg with *n* H-bridges cells. Each cell can generate three voltage levels ($-V_{dc}, 0, +V_{dc}$). The H-bridge cell generates V_{dc} when switches $S_{cn,1}$ and $S_{cn,4}$ are on, while the output voltage is $-V_{dc}$ when $S_{cn,2}$ and $S_{cn,3}$ are on. However, the CHB behavior during an OC fault differs due to the effect of the anti-parallel diode of the faulty switch, which results in current distortion. This section analyses the behavior of a CHB inverter under normal and OC fault conditions.

From Figure 3.1, one H-bridge cell is selected for analysis of the operation principles during the normal and fault operation conditions. Since each cell has four switches, there are four switching fault possibilities that will be discussed in this section. The current path of an H-bridge cell under normal and OC fault in S_{11}, S_{12}, S_{13}, and S_{14} is shown in Figures 3.3-3.6, respectively. The red dotted line in Figures 3.3-3.6 represents the current path when the output current $i > 0$, and the blue indicates the current path when $i < 0$.

3.2.2.1 Open-Circuit Fault on S_{11}

Figures 3.3 (a) and (b) shows the current path under normal conditions and when there is an open-circuit fault on switch S_{11} when both of the switches S_{11}, and S_{14} are on. Under normal operation, the output voltage is $+V_{dc}$. The current flows through the switches S_{11}, and S_{14}, when $i > 0$, while the current path is through the anti-parallel diodes of the switches S_{11}, and S_{14}, when $i < 0$. However, when there is an open-circuit fault on S_{11}, as shown in Figure 3.3 (b), the current path is blocked by the anti-parallel diode of S_{11}, and the actual current flows through the anti-parallel diodes of switch S_{12} when $i > 0$.

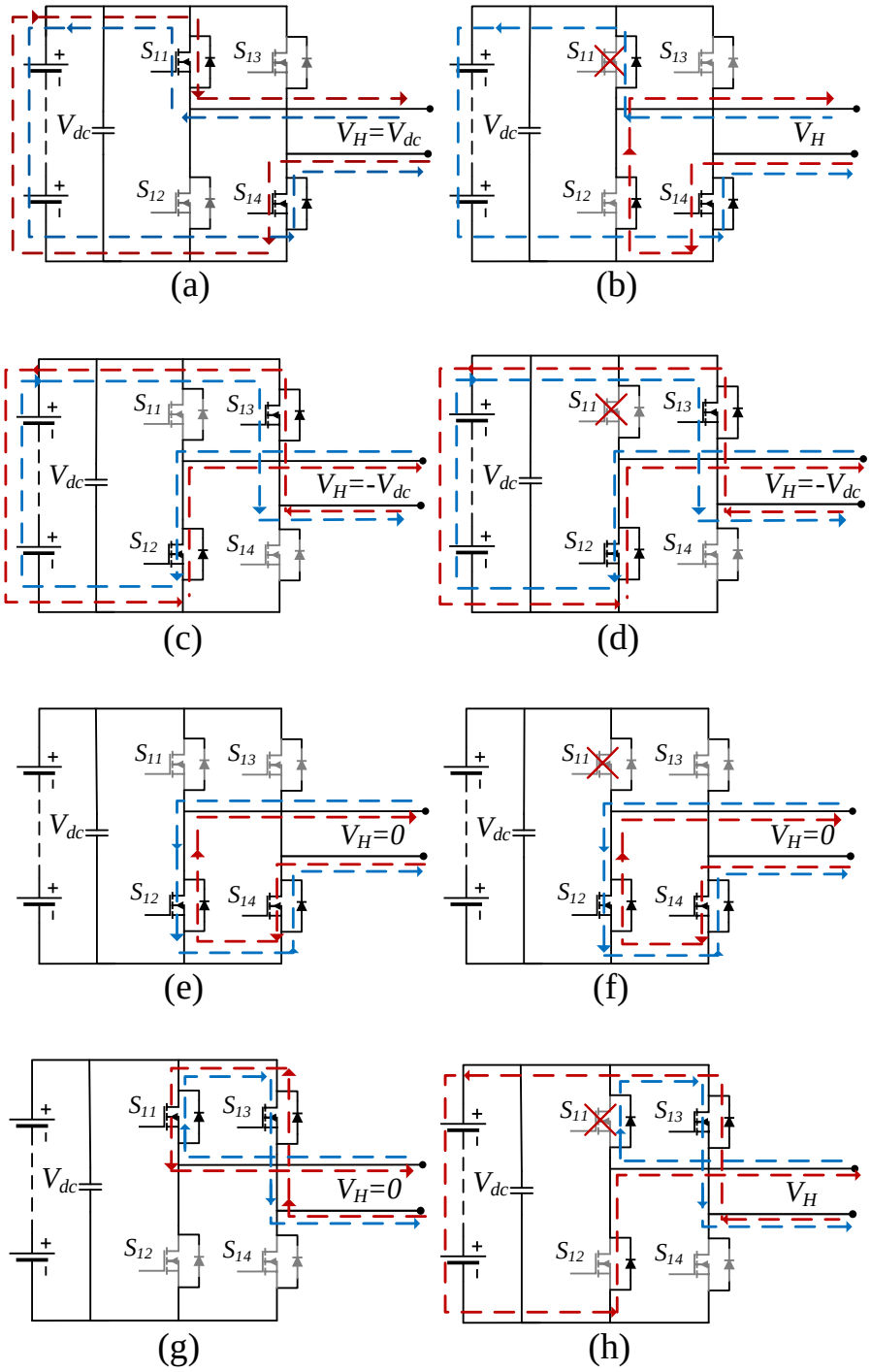


Figure 3.3 Current path of an H-bridge inverter under normal operation and an open-circuit switch fault on S_{11}: (a) Normal operation, S_{11}, and S_{14} are turned-on, (b) an open-circuit switch fault on S_{11}, (c) Normal operation, S_{12}, and S_{13} are turned-on, (d) an open-circuit switch fault on S_{11}, (e) Normal operation, S_{12}, and S_{14} are turned-on, (f) an open-circuit switch fault on S_{11},(g) Normal operation, S_{11}, and S_{13} are turned-on, and (h) an open-circuit switch fault on S_{11}. The red dotted line represents $i > 0$, and the blue $i < 0$.

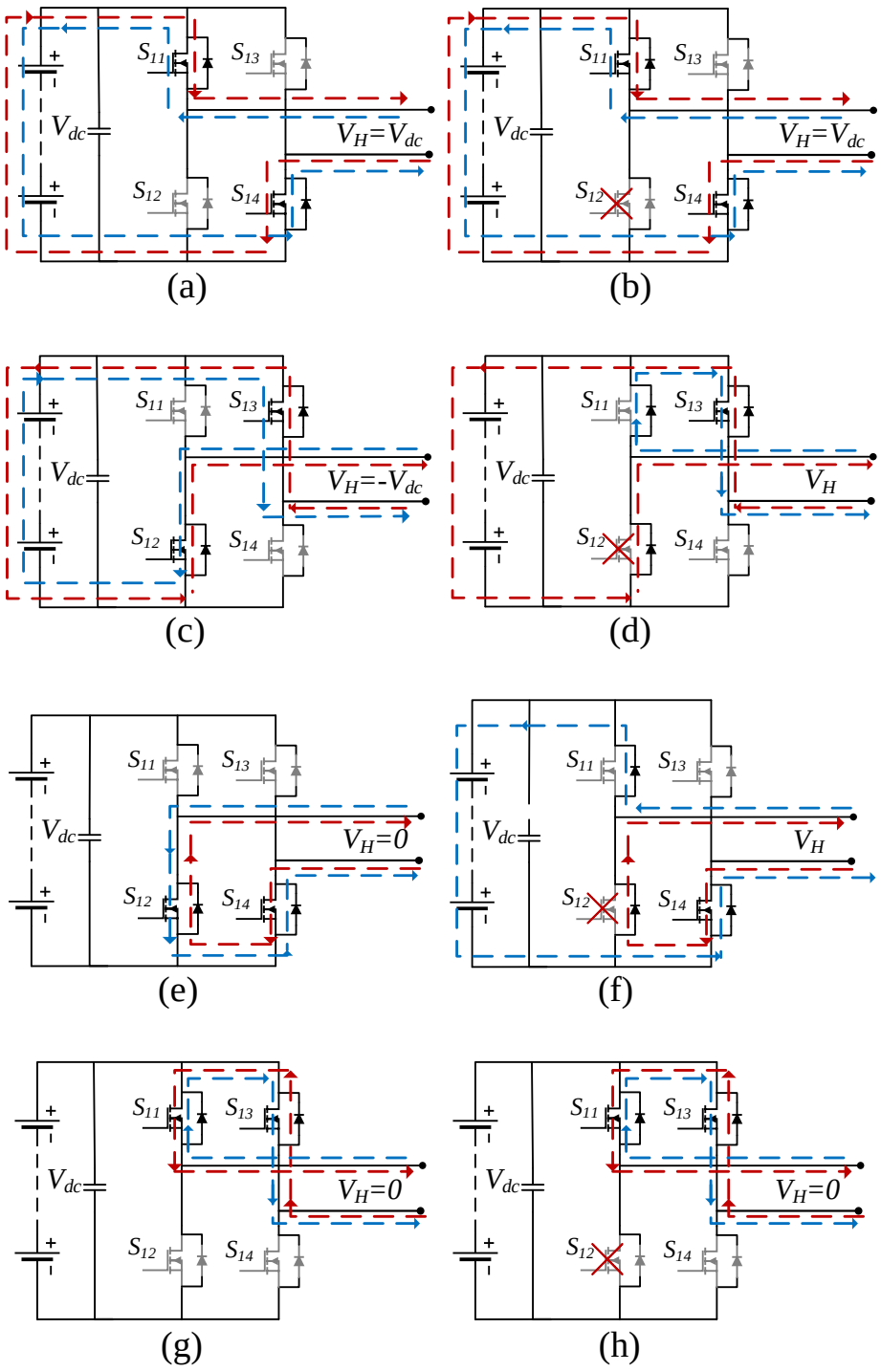


Figure 3.4 Current path of an H-bridge inverter under normal operation and an open-circuit switch fault on S_{12}: (a) Normal operation, S_{11}, and S_{14} are turned-on, (b) an open-circuit switch fault on S_{12}, (c) Normal operation, S_{12}, and S_{13} are turned-on, (d) an open-circuit switch fault on S_{12}, (e) Normal operation, S_{12}, and S_{14} are turned-on, (f) an open-circuit switch fault on S_{12},(g) Normal operation, S_{11}, and S_{13} are turned-on, and (h) an open-circuit switch fault on S_{12}. The red dotted line represents $i > 0$, and the blue $i < 0$.

In this case, the output voltage of the inverter is zero instead of $+V_{dc}$, which results in losing one of the output voltage levels. In other words, there is no path for the current to flow when $i > 0$ only through the anti-parallel diode of switch S_{12}. Although switch S_{12} is turned-off during this state, its anti-parallel diode is naturally commutating. From Figure 3.3 (b), the output voltage of the inverter is the same during the normal operation and the fault conditions when $i > 0$ because the anti-parallel diodes of S_{11} provides the path for the current to flow.

Figure 3.3 (c) and (d) show the operation of the inverter under normal and an open-circuit fault on S_{11} conditions when S_{12}, and S_{13} are turned-on. Under normal operation, the output voltage is $-V_{dc}$, where the current flows through the anti-parallel diodes of S_{12}, and S_{13}, when $i > 0$, while the current path is through S_{12}, and S_{13}, when $i < 0$.

The output voltage and current during this state is the same under OC fault as the normal operation. Another state that the output voltage and current are the same under normal and fault conditions is shown in Figures 3.3 (e) and (f). During this state, S_{12}, and S_{14} are turned-on to generate 0 voltage level. The reasons why there is no effect on the output voltage and current is that even if S_{11} has an OC fault during operation in Figure 3.3 (d) and (f), but it is not a part of the operation modes, because there is no functionality for S_{11}. Figure 3.3 (g) and (h) show the inverter operation under normal and fault conditions when S_{11}, and S_{13} are turned-on. This state provides a zero level for the inverter. The output current and voltage are the same under normal and fault conditions: when $i < 0$, the output voltage is $-V_{dc}$ and when $i > 0$, results in current distortions.

3.2.2.2 Open-Circuit Fault on S_{12}

When there is an open-circuit fault on S_{12}, and it is not a part of the switching modes, the output voltage is the same under both normal and fault conditions as shown in Figures 3.4 (a), (b),

(g), and (h). When the inverter generates $-V_{dc}$, S_{12} and S_{13} are turned-on. There is no effect on the output voltage and current when $i > 0$, while the current is blocked by the anti-parallel diode of S_{12} when $i < 0$, as shown in Figure 3.4 (d). In Figure 3.2 (e), S_{12}, or S_{14} are turned-on. If there is an open-circuit fault on S_{12}, the current path is blocked by the anti-parallel diode of faulty switch as shown in Figure 3.4 (f).

3.2.2.3 Open-Circuit Fault on S_{13}

The behavior of the H-bridge cell under normal and fault conditions is illustrated in Figure 3.5 Two modes are affected (S_{12} and S_{13} are turned-on or S_{11}, and S_{13} are turned-on) when there is an open-circuit switch fault on S_{13}, as shown in Figure 3.5 (d) and (h). The anti-parallel diode of S_{13} is blocking the current when $i < 0$.

3.2.2.4 Open-Circuit Fault on S_{14}

In order to better understand the behavior of CHB inverter under normal and open-circuit fault conditions, the H-bridge cell is examined under fault on S_{14} as shown in Figure 3.6. Under normal operation conditions, the inverter generates $-V_{dc}, +V_{dc}$, and 0 as shown in Figure 3.6 (a), (c), (e),and (g), respectively. The current path of the inverter under an open-circuit fault on S_{14} is shown in Figure 3.6 (b), (d), (f), and (h), respectively.

In Figure 3.6 (a), the output voltage of the inverter is $+V_{dc}$, the current flows through S_{11} and S_{14} and $i > 0$, while the current path is flowing through the anti-parallel diodes of S_{11} and S_{14} when $i < 0$. When there is an open-circuit fault on S_{14}, the current path is the same as the normal operation when $i < 0$. However, when $i > 0$, the current is blocked by the anti-parallel diode of S_{14}, which results in current distortion, and the output voltage is 0 as shown in Figure 3.6 (b).

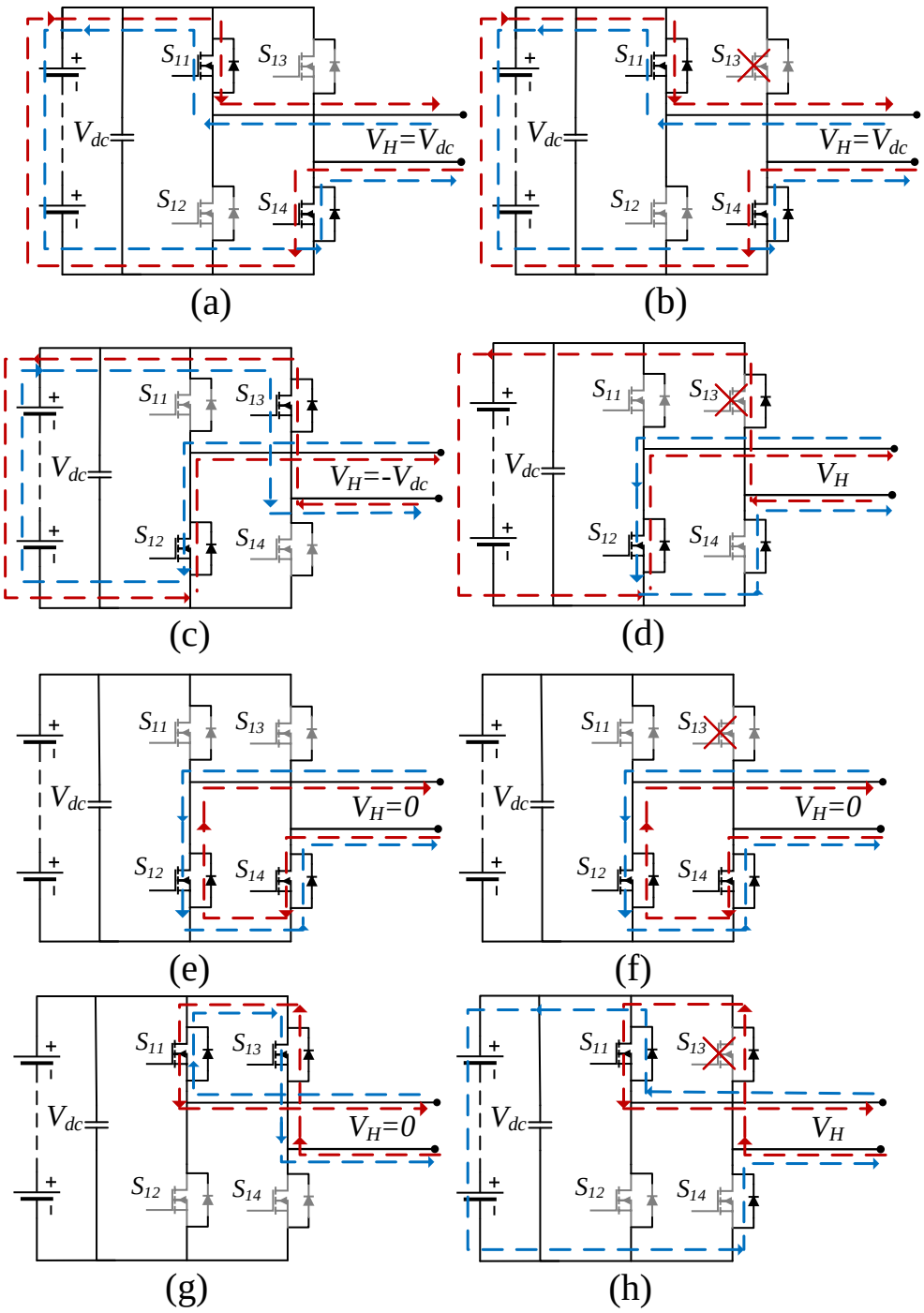


Figure 3.5 Current path of an H-bridge inverter under normal operation and an open-circuit switch fault on S_{12}: (a) Normal operation, S_{11}, and S_{14} are turned-on, (b) an open-circuit switch fault on S_{13}, (c) Normal operation, S_{12}, and S_{13} are turned-on, (d) an open-circuit switch fault on S_{13}, (e) Normal operation, S_{12}, and S_{14} are turned-on, (f) an open-circuit switch fault on S_{13},(g) Normal operation, S_{11}, and S_{13} are turned-on, and (h) an open-circuit switch fault on S_{13}. The red dotted line represents $i > 0$, and the blue $i < 0$.

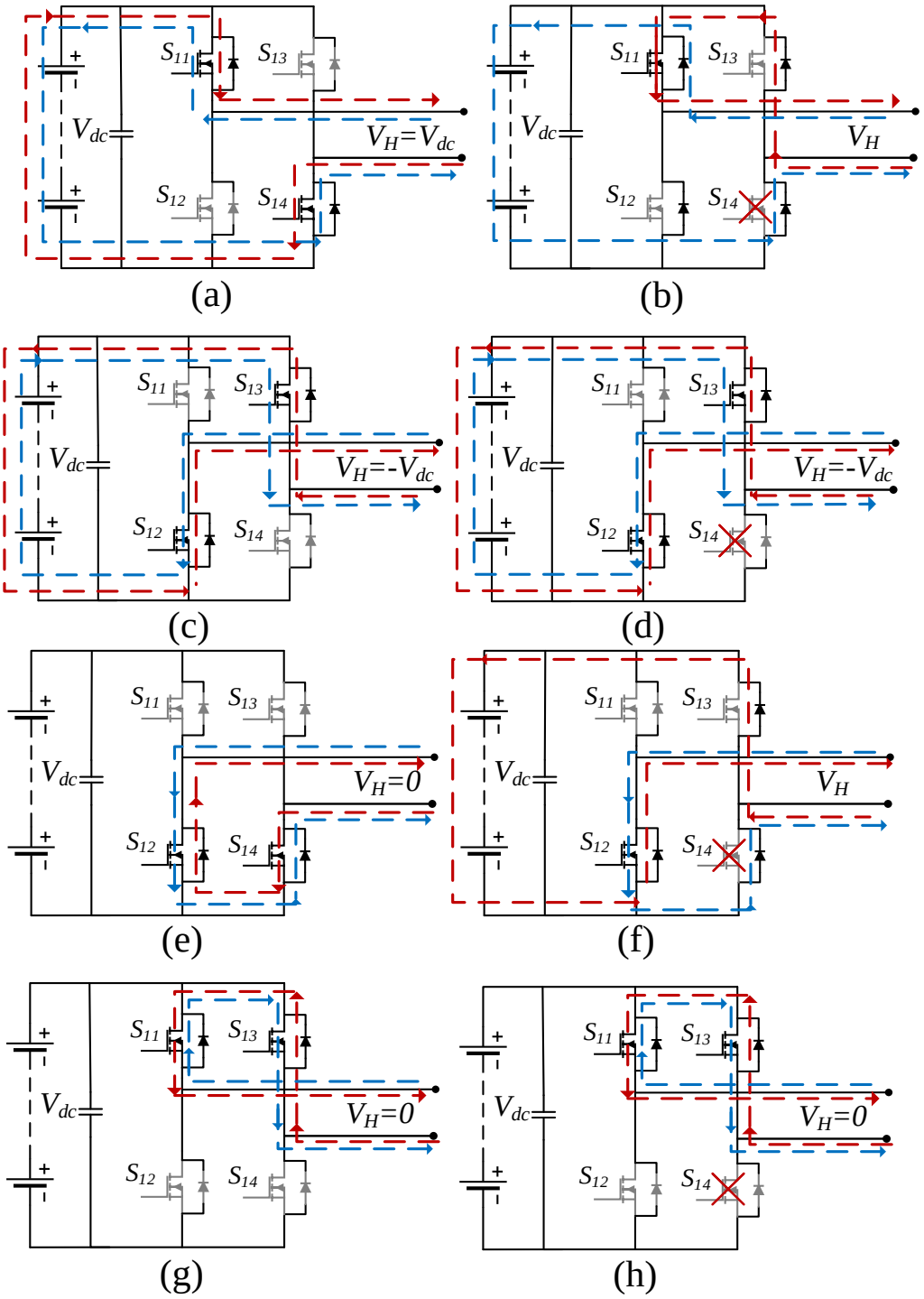


Figure 3.6 Current path of an H-bridge inverter under normal operation and an open-circuit switch fault on S_{12}: (a) Normal operation, S_{11}, and S_{14} are turned-on, (b) an open-circuit switch fault on S_{14}, (c) Normal operation, S_{12}, and S_{13} are turned-on, (d) an open-circuit switch fault on S_{14}, (e) Normal operation, S_{12}, and S_{14} are turned-on, (f) an open-circuit switch fault on S_{14},(g) Normal operation, S_{11}, and S_{13} are turned-on, and (h) an open-circuit switch fault on S_{14}. The red dotted line represents $i > 0$, and the blue $i < 0$.

In Figure 3.6 (c), S_{12} and S_{13} are turned-on, and the output voltage of the inverter is $-V_{dc}$. The current flows through the anti-parallel diodes of S_{12} and S_{13} and $i > 0$, while the current path is flowing through S_{12} and S_{13} when $i < 0$. When the output voltage of the inverter is $-V_{dc}$ (S_{12}, and S_{13} are turned-on), and the there is an open-circuit fault on S_{14}, there is no effect on the output voltage and current during this mode. That is, S_{14} does not impact the switching states, and an open-circuit fault on a switch other than S_{12} or S_{13} results in no waveform distortion as shown in Figure 3.6 (d). That is applied for Figure 3.6 (g) and (h) where under normal conditions, S_{11} and S_{13} are turned-on to generate the zero voltage level. The output voltage and current is the same even there is a fault on S_{14} because the faulty switch has no part in the switching states.

In Figure 3.6 (e), S_{12} or S_{14} are turned-on. If there is an open-circuit fault on S_{14}, the current path is blocked by the anti-parallel diode of faulty switch when $i > 0$ as shown in Figure 3.6 (f).

Table 3.2 Cell *n* Output Voltage Change Due to Fault Occurrence in Each Switch

Faulty Switch	**Current Direction**	**Cell State**			
		$\mathbf{0}_{Lower}$	**-1**	**+1**	$\mathbf{0}_{Upper}$
$\boldsymbol{S_{11}}$	$i > 0$	0	$-V_{dc}$	0	$-V_{dc}$
	$i < 0$	0	$-V_{dc}$	$+V_{dc}$	0
$\boldsymbol{S_{12}}$	$i > 0$	0	$-V_{dc}$	$+V_{dc}$	0
	$i < 0$	$+V_{dc}$	0	$+V_{dc}$	0
$\boldsymbol{S_{13}}$	$i > 0$	0	$-V_{dc}$	$+V_{dc}$	0
	$i < 0$	0	0	$+V_{dc}$	$+V_{dc}$
$\boldsymbol{S_{14}}$	$i > 0$	$-V_{dc}$	$-V_{dc}$	0	0
	$i < 0$	0	$-V_{dc}$	$+V_{dc}$	0

3.2.3 Effect of Open-Circuit Fault

Assuming that the fault does not affect the reverse diode of the switch, the change in the cell output voltage is based on the leg voltage polarity in case of a fault in each switch, which is illustrated in Table 3.2.

According to Table 3.2, each individual OC fault results in voltage deviation for two cell states. Therefore, the combination of cell output voltage and leg voltage polarity considering the modulation technique can be used to find the faulty switch in case of an open-circuit fault.

3.3 Quantified Description of CHB Under OC Fault

An analysis that explains all of the related voltages and currents during the various possible fault conditions is included in this section. From Eq. (3-3) the leg voltage for an H-bridge inverter can be expressed as

$$V_{leg} = (S_{11} - S_{13})V_{dc} \tag{3-4}$$

In order to draw conclusions for the open-circuit switch fault for an H-bridge, mathematical description for all possible open-circuit switch faults in Figures 3.3-3.6 can be express as four circumstances.

Circumstance 1: S_{11} has an open-circuit fault. When the open-circuit switch occurs on S_{11}, there are two possible currents path, $i > 0$ or $i < 0$. The first scenario when S_{11} has an open-circuit fault and $i > 0$. In this case, the output voltage can be written as

$$V_{S_{11},Fault} = -S_{13}V_{dc},\ i > 0 \tag{3-5}$$

where $V_{S_{11},Fault}$ is the output inverter voltage when S_{11} has an open-circuit fault. Eq. (3-5) shows that when S_{11} has an open-circuit fault, and $i > 0$, the output voltage is either

$-V_{dc}$ or 0, and there are no positive output voltages to be generated by the inverter. That is, the anti-parallel diode of S_{11} is blocking the voltage current path as shown in Figure 3.3 (h).

Another possible case is when the open-circuit switch fault happens on S_{11} and $i < 0$. The output voltage of the inverter in this case can be written as

$$V_{S_{11},Fault} = (S_{11} - S_{13})V_{dc},\ i < 0 \tag{3-6}$$

It is clear from Eq. (3-6) that there is no effect on the output voltage and current waveforms when S_{11} has an open-circuit fault and $i < 0$. That is, the anti-parallel diode of S_{11} allow the current to flow, as shown in Figure 3.3 (b).

Circumstance 2: S_{12} has an open-circuit fault. When the open-circuit switch occurs on S_{12}, there are two possible currents path, $i > 0$ or $i < 0$. The output voltage for the inverter under this fault condition when $i > 0$ can be illustrated as

$$V_{S_{12},Fault} = (S_{11} - S_{13})V_{dc},\quad i > 0 \tag{3-7}$$

From Eq. (3-7), the output voltage and current waveforms are the same under normal and fault conditions when $i > 0$, as can be seen in Figure 3.4 (d). The output voltage of the inverter under this fault condition on S_{12} and $i > 0$ can be written as

$$V_{S_{12},Fault} = (1 - S_{13})V_{dc},\ i < 0 \tag{3-8}$$

The inverter can generate either $+V_{dc}$ or 0 voltage levels when $i < 0$, because the current path is blocked by the anti-parallel diode of S_{12}, as shown in Figures 3.4 (d) and (f).

Circumstance 3: S_{13} has an open-circuit fault. The output voltage for the inverter under this fault condition on S_{13} is

$$V_{S_{13},Fault} = (S_{11} - S_{13})V_{dc}\quad i > 0 \tag{3-9}$$

It is clear from Eq. (3-9) and Figure 3.5 that the voltage is the same as the normal condition, and there is no effect of the fault on the output waveforms, because of the available current path by the anti-parallel diode. However, as shown in Figure 3.5 (d) and (h), the current path is blocked by the anti-parallel diode when $i < 0$, and the output voltage is

$$V_{S_{13},Fault} = S_{11}V_{dc},\ i < 0 \tag{3-10}$$

Table 3.3 Change in Cell Output Voltages Due to Fault Occurrence in Each Switch

Faulty Switch	**Current Direction**	**Cell Output Voltages**
$\boldsymbol{S_{11}}$	$i > 0$	$-S_{13}V_{dc}$
	$i < 0$	$(S_{11} - S_{13})V_{dc}$
$\boldsymbol{S_{12}}$	$i > 0$	$(S_{11} - S_{13})V_{dc}$
	$i < 0$	$(1 - S_{13})V_{dc}$
$\boldsymbol{S_{13}}$	$i > 0$	$(S_{11} - S_{13})V_{dc}$
	$i < 0$	$S_{11}V_{dc}$
$\boldsymbol{S_{14}}$	$i > 0$	$(S_{11} - 1)V_{dc}$
	$i < 0$	$(S_{11} - S_{13})V_{dc}$

Circumstance 4: S_{14} has an open-circuit fault. The first scenario when there is an open-circuit fault on S_{14} is when the current following the positive direction as shown in Figure 3.6 (b) and (f). The output voltage of the inverter can be expressed as

$$V_{S_{14},Fault} = (S_{11} - 1)V_{dc},\quad i > 0 \tag{3-11}$$

From Eq. (3-11), the inverter can generate either $-V_{dc}$ or 0 when $i > 0$, as shown in Figure 3.6. However, the output voltage and current are the same when the current flows in the negative direction, and can be expressed as

$$V_{S_{14},Fault} = (S_{11} - S_{13})V_{dc},\ i < 0 \tag{3-12}$$

It is clear from Eqs. (3-6) and (3-12) that the output voltage and current are the same as normal and fault conditions when the current flow is in the negative direction, and the fault on S_{11} and S_{14}. Similarly, when the open-circuit faults occurs on S_{12} and S_{13}, and the current flow is in the positive direction, the output voltage and current is the same under normal and fault conditions as expressed in Eqs. (3-7) and (3-9). All the cases are summarized in Table 3.3.

3.4 Open-Circuit Fault Cell Detection

When an open-circuit switch fault occurs in a CHB converter, the cell voltage along with the polarity of leg voltage can be used to detect the fault so that necessary steps can be taken to isolate the faulty switch.

A combination of sensed cell voltages and leg voltage is used for the detection of fault and as a means to detect and isolate the faulty switch. An OC fault would result in lower output voltage and current than expected. The faulty device would behave as just an anti-parallel diode, and as a result, the cell loses its ability to output the desired voltage. Using the relationship between leg voltage polarity and cell output voltage, the faulty H-bridge cell is detected. Next, the faulty semiconductor device can be identified using the cell switching states. The flowchart for the presented approach is shown in Figure 3.7.

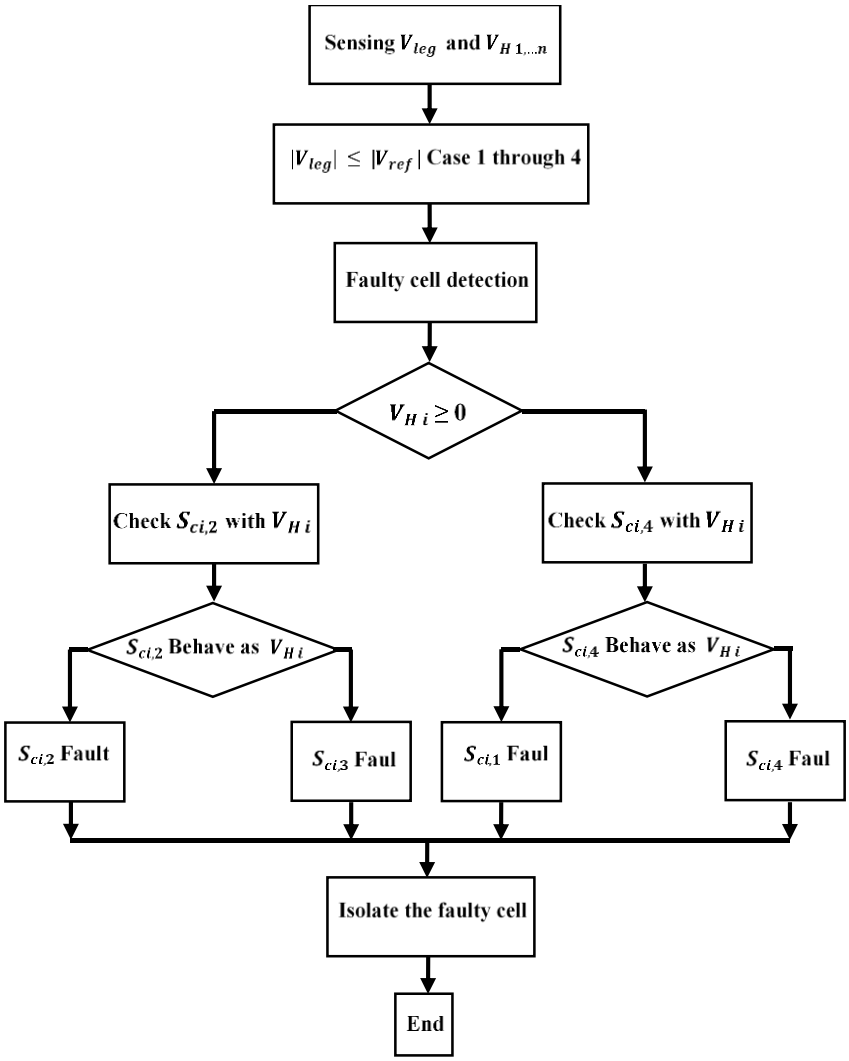


Figure 3.7 Flowchart for the proposed open-circuit fault detection.

To sum up, if the leg output voltage is a match with the predictable value, then this means that one of the inverter's switches has failed. The possible faulty H-bridge cells and switches for a 7-level CHB are listed in Table 3.4.

Table 3.4 Proposed Strategy to Detect the Faulty Cell

	Measured Voltage			**Possible Faulty Cell**	**Possible Faulty Switches**
	v_{H1}	v_{H2}	v_{H3}		
Case 1	<0	v_{H2}	v_{H3}	$H1$	S_{11}, S_{41}
Case 2	>0	v_{H2}	v_{H3}	$H1$	S_{21}, S_{31}
Case 3	v_{H1}	<0	v_{H3}	$H2$	S_{12} , S_{42}
Case 4	v_{H1}	>0	v_{H3}	$H2$	S_{22}, S_{32}
Case 5	v_{H1}	v_{H2}	<0	$H3$	S_{13} , S_{43}
Case 6	v_{H1}	v_{H2}	>0	$H3$	S_{23}, S_{33}

3.4.1 Identification of the Faulted Switch and Isolation

When the faulty H-bridge cell is identified, there are two possible scenarios, one of the switches would be eliminated based on LS-PWM and the exact switch that failed can be identified, and subsequently, the isolation procedure is applied. The detection of the faulty switch procedure to detect the exact faulty switch is summarized in Table 3.5.

The proposed method is applicable to an unlimited number of H-bridge cells in MLIs. Assuming the number of H-bridges in a MLI is *n*, and the H-bridge switches is *x* to summarize the proposed method of operation. Consequently, all of the previous cases in Table 3.4 and Table 3.5 can be summarized in Eqs. (3-13) and (3-14) and Table 3.6.

Table 3.5 Proposed Strategy to Detect the Faulty Switch

	Measured Voltage			**Possible Faulty Cell**	**Possible Faulty Switches**	**Faulty Switch Identification**
	v_{H1}	v_{H2}	v_{H3}			
Case a	<0	v_{H2}	v_{H3}	$H1$	S_{11}, S_{41}	S_{41} is ON, then S_{11} is faulty Otherwise, S_{41} is faulty
Case b	>0	v_{H2}	v_{H3}	$H1$	S_{21}, S_{31}	S_{21} is ON, then S_{31} is faulty Otherwise, S_{21} is faulty
Case c	v_{H1}	<0	v_{H3}	$H2$	S_{12} , S_{42}	S_{42} is ON, then S_{12} is faulty Otherwise, S_{42} is faulty
Case d	v_{H1}	>0	v_{H3}	$H2$	S_{22}, S_{32}	S_{22} is ON, then S_{31} is faulty Otherwise, S_{22} is faulty
Case e	v_{H1}	v_{H2}	<0	$H3$	S_{13} , S_{43}	S_{43} is ON, then S_{13} is faulty Otherwise, S_{43} is faulty
Case f	v_{H1}	v_{H2}	>0	$H3$	S_{23}, S_{33}	S_{23} is ON, then S_{33} is faulty Otherwise, S_{23} is faulty

Table 3.6 Generalized the Proposed Strategy to Detect the Faulty Switch

	Measured Voltage v_{Hn}	**Possible Faulty Cell**	**Possible Faulty Switches**	**Faulty Switch Identification**
Case i	<0	Hn	S_{1n}, S_{4n}	S_{4n} is ON, then S_{1n} is faulty Otherwise, S_{4n} is faulty
Case ii	>0	Hn	S_{2n}, S_{3n}	S_{2n} is ON, then S_{3n} is faulty Otherwise, S_{2n} is faulty

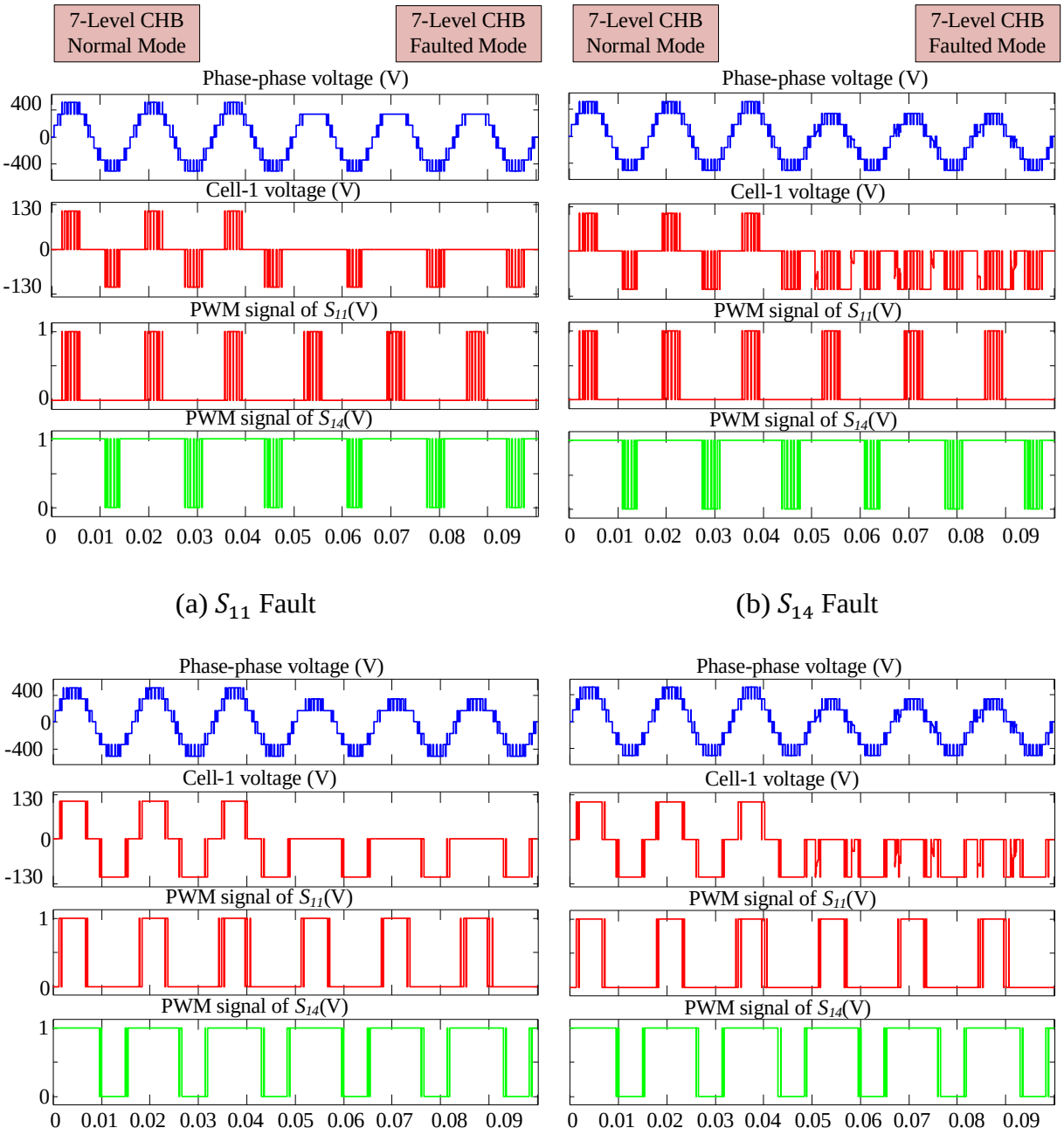
$$\sum_{i=1}^{N} S_{4n} V_{Hn} \leq 0 \tag{3-13}$$

$$\sum_{i=1}^{N} S_{2n} V_{Hn} \geq 0 \tag{3-14}$$

Once the faulty switch is detected, the switch is then soft-isolated [3.2].

3.5 Simulation Results of the Proposed Method

An accurate MATLAB/Simulink® simulation was developed for verification of the proposed fault identification method. An OC fault was applied to various switches from different cells to demonstrate the effectiveness of the presented approach for the detection and isolation of OC faults. Table 3.6 displays the circuit specifications utilized for the simulation. A nine-level CHB inverter connected to an RL load is simulated.



(a) S_{11} Fault (b) S_{14} Fault

(c) S_{21} Fault (d) S_{24} Fault

Figure 3.8 Simulation results of four fault modes.

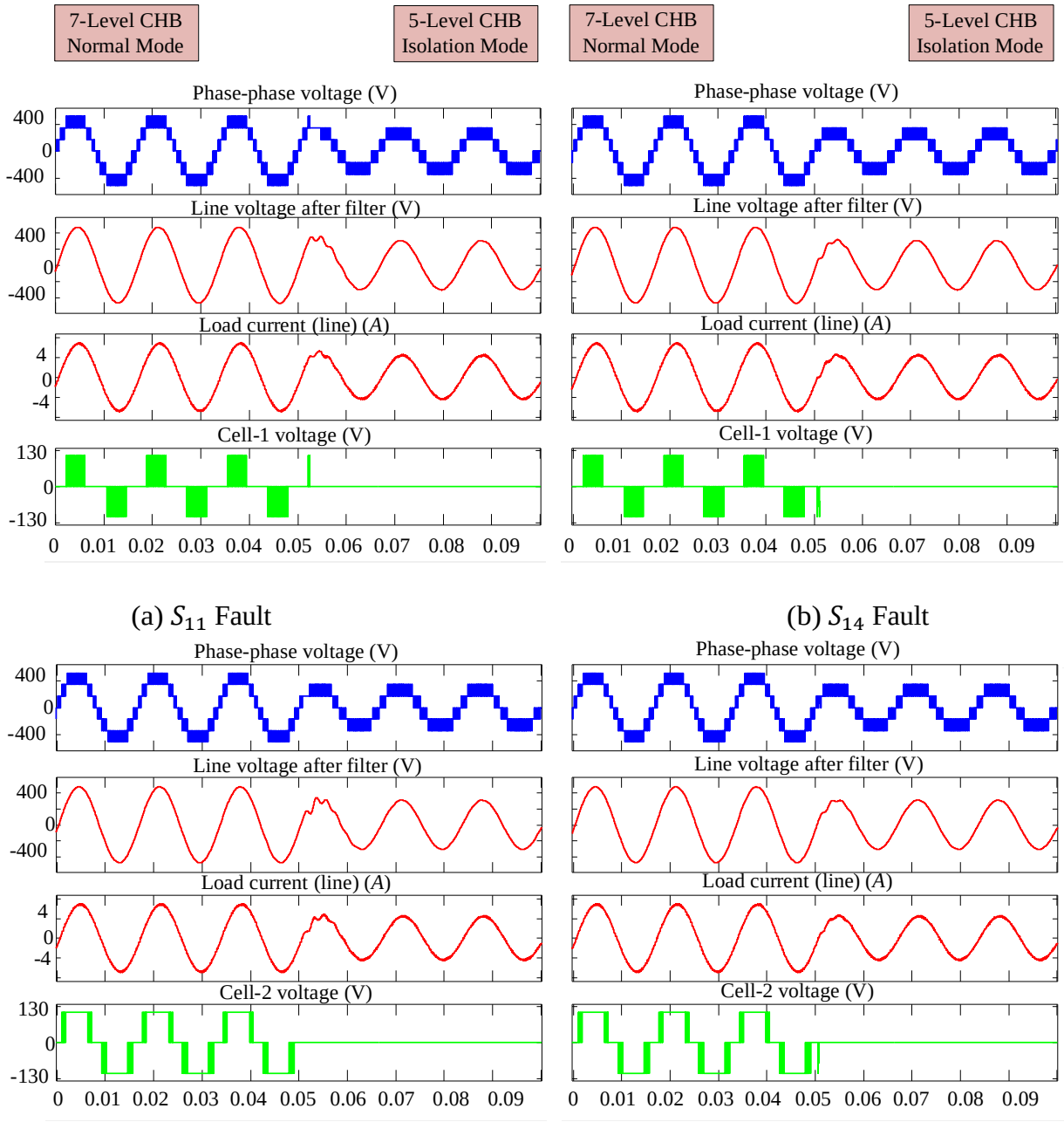
Figure 3.8 illustrates the simulation results for four different faults. For each fault event, an OC fault is placed on the switch at the time t=0.05. The operation of the circuit in pre-fault and post-fault conditions are compared. Figure 3.8(a)-(d) display the operations with faults applied to

S_{11}, S_{14}, S_{21}, and S_{24}, respectively. The leg voltage, cell output voltage, and the two possible faulty switches (upper and lower) gate signals are displayed for each individual fault. Up to t=0.05s, the system is operating in a healthy condition and is producing the normal 7-level voltage and current.

At t=0.05s as a result of the fault occurs, the output voltage harmonics increases, the waveform starts to get distorted, and output voltage loses one level. Figure 3.9 illustrates the simulation results to demonstrate the effectiveness of the proposed fault detection method in each of the switch fault cases demonstrated in Table 3.7. The fault is created in S_{11}, S_{14}, S_{21}, and S_{24} by misfiring them, which results in that individual switch mimicking an open-circuit fault as shown in Figure 3.9 (a)-(d). Once the fault is detected, the isolation is implemented by using a soft-bypassing. As a consequence of the fault, the 7-level CHB operates as a 5-level inverter since one of the cells is bypassed.

Table 3.7 Simulation Parameters

Description	**Value**
Number of cells	3
Input voltage (Vdc)	400 V
Output voltage (Vac)	280 V
Line frequency	60 Hz
Filter inductor,	0.3 mH
Filter Capacitor	50 µF
Carrier frequency	1.5 kHz
Load (inductive)	30 Ω, 10 mH



(a) S_{11} Fault

(b) S_{14} Fault

(c) S_{21} Fault

(d) S_{24} Fault

Figure 3.9 Simulation results for fault detection and isolation.

3.6 Experimental Results of the Proposed Method

In this subsection, the experimental results for the verification of the proposed OC fault identification method are presented. A 7-level CHB with three cells built up of SiC MOSFETs and

a total peak voltage of 400 V is implemented as shown in Figure 3.10. A TMS320F28335 DSP was utilized for the control and fault detection method implementation. Soft isolation was used for isolation of the faulty cell upon detection. An inductive load with leading power factor was used to demonstrate correct operation of the presented method with nonlinear loads. The experimental setup details and values are given in Table 3.8.

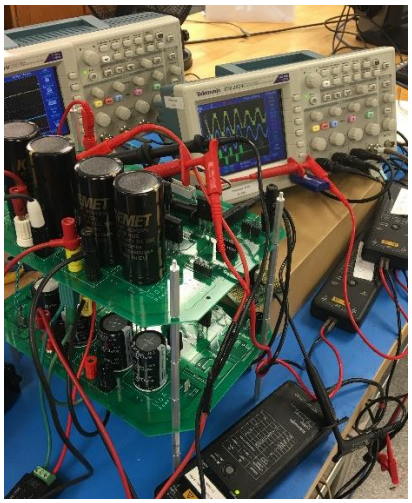


Figure 3.10 Experimental test configuration "Photo by Author."

Four OC faults were generated separately at S_{11}, S_{14}, S_{21}, and S_{24}. Figure 3.7 displays the leg operation under healthy operation and after a fault has occurred in one of the switches, S_{11}, S_{14}, S_{21}, and S_{24}. In each case in Figure 3.11 (a)-(d), the leg voltage (ch1) before the filter, the filter voltage (ch2), the line current (ch3), and the respective cell voltages are displayed.

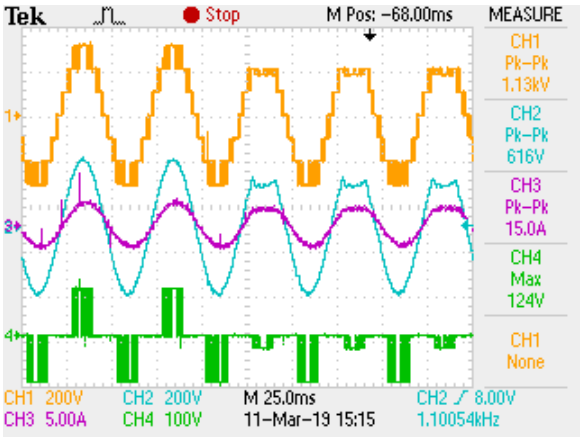
Table 3.8 Experimental Setup Parameters

Description	Value
Input voltage (Vdc)	400 V
Output voltage (Vac)	280 V
Line frequency	60 Hz
Filter inductor,	0.3 mH
Filter Capacitor	50 μF
Carrier frequency	1.5 kHz
Load (inductive)	30 Ω, 10 mH

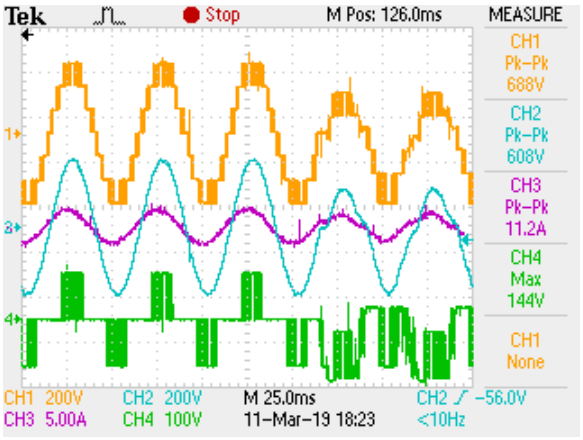
Figure 3.11 (a) and (b) show the normal and post-fault condition operation of Cell-1 when a fault is applied to S_{11}, S_{14}. In Figure 3.11 (a), it can be observed that after the occurrence of the fault, the output voltage of the cell (V_{H1}) is equal to or less than zero. The faulty cell could be detected as Cell-1, according to Case (1) described in Section 3.3.

The results in Figure 3.12 (a)-(d) display the application of the fault detection method and the isolation of the faulty cell. In other words, Figure 3.12 (a)-(d) shows the leg voltage waveform before and after the output filter, the leg current, and the cell output voltages before and after a fault occurred in the system and how the fault is resolved.

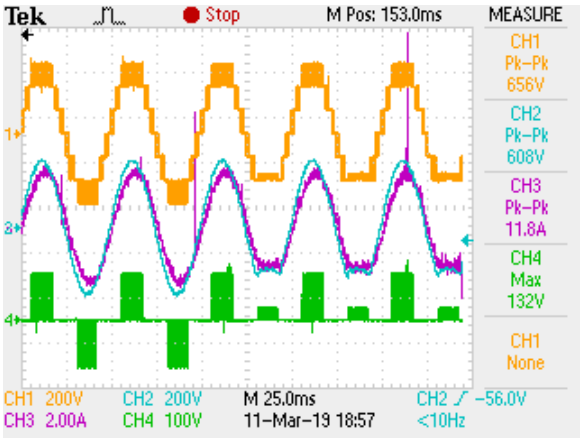
The experimental results verified successful performance of the fault detection method and isolation in all cases. As an example, in case of a fault in S_{11}, Figure 3.12 (a), the $V_{leg} > 0$ and $VH2 < 0$, therefore the possible faulty switches are $S_{11}$and S_{14}. Since S_{14} is always on when cell voltage is positive, the faulty switch is identified as S_{11}. Once the faulty switch is identified, the faulty cell is softly isolated.



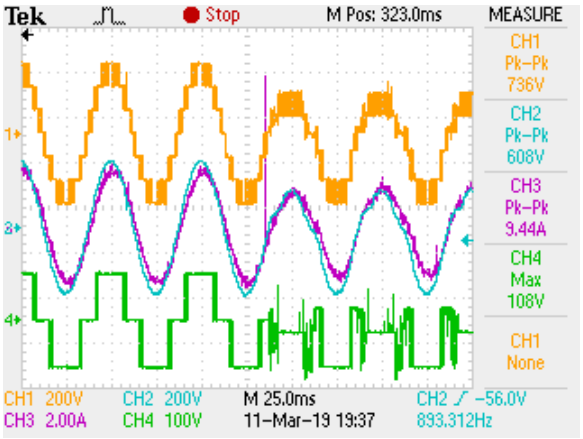
(a) S_{11} Fault



(b) S_{14} Fault

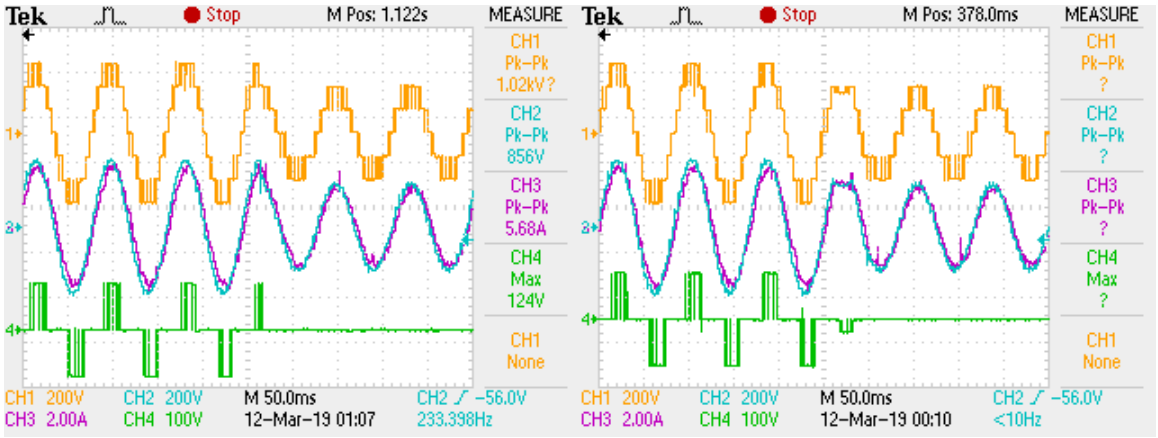


(c) S_{21} Fault

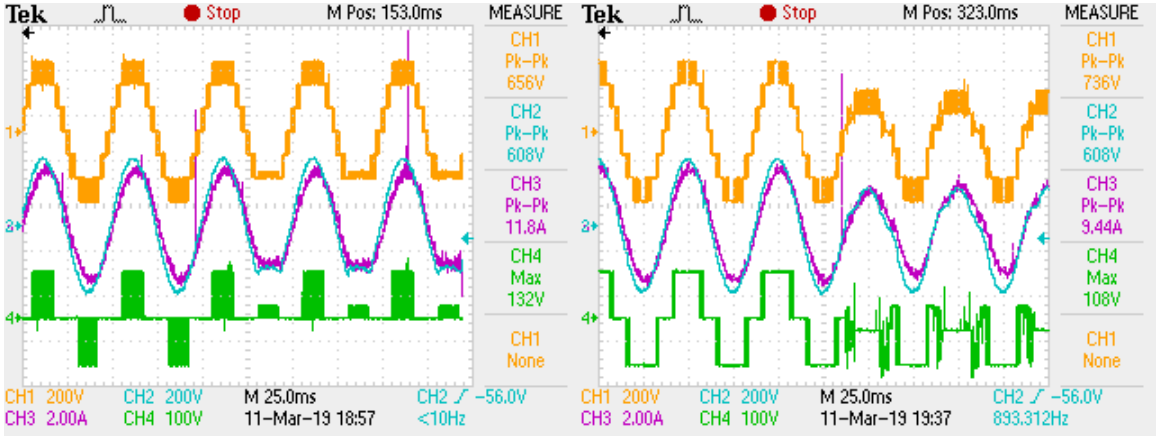


(d) S_{24} Fault

Figure 3.11 Verification of the proposed fault detection method: inverter output voltage (ch1), Line voltage after filter (ch2), Line current (ch3), and (ch4) Output cell voltage.



(a) S_{11} fault (b) S_{14} fault



(c) S_{21} fault (d) S_{24} fault

Figure 3.12 Fault Detection and Isolation Method: (ch1), Line voltage after filter (ch2), Line current (ch3), and (ch4) Output cell voltage.

3.7 Conclusions

This chapter proposes a novel open-circuit fault identification algorithm for a CHB inverter. Simulation and experimental results were reported that confirm the operation of the proposed method using the relationship between the inverter cell voltage, leg voltage, and the switching signals. The proposed algorithm proved to be: 1) Simple for implementation because of its straightforward process, 2) appropriate to an unlimited number of H-bridges in MLI applications, and 3) highly accurate for location of a faulty switch in less than one cycle.

3.8 References

[3.1] H. Mhiesan *et al*., "A Method for Open-Circuit Faults Detecting, Identifying, and Isolating in Cascaded H-Bridge Multilevel Inverters," *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Charlotte, NC, 2018, pp. 1-5.

[3.2] W. Song and A. Q. Huang, "Fault-Tolerant Design and Control Strategy for Cascaded H-Bridge Multilevel Converter-Based STATCOM," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2700-2708, Aug. 2010.

CHAPTER 4

NOVEL CIRCUIT AND METHOD FOR FAULT RECONFIGURATION IN CASCADED H-BRIDGE MULTILEVEL INVERTERS

4.1 Introduction

Solar and wind generation represent an increasing amount of renewable sources that will rise in the coming years. Electricity provided by renewable energy sources require power converters for conditioning and integration to the grid. As a result, fault identification and isolation techniques are needed to be developed for power converters. This will lead to a guarantee of the reliability of electric power provided through renewable energy-based sources. Additionally, there will be a need for battery energy storage systems to operate as stand-by systems for the times when energy is reduced from the renewable resources, and for compensating for the voltage and frequency (voltage shape and frequency regulator applications) during heavy loads.

The literature review provided in Chapter 2 proved the need for fault-tolerant schemes capable of isolation and reconfiguration of circuits with high response times in order to increase the reliability of MLI topologies. This chapter provides a fault tolerant CHB topology for BESS applications developed to achieve these goals.

4.2 Operating of the Proposed Circuit

The proposed novel CHB topology presents a new approach to maintain system operation after multiple component failures. Figure 4.1 illustrates the summary of the presented approach. The idea is implemented by the highlighted relays and switches T1, T2, S_{a1}, S_{a2}, S_{b1}, and S_{b2}, etc. Once a fault has been detected using the method described in Chapter 3, these relays and switches enter the circuit operation to reconfigure the circuit in response to open/short circuit faults on $S_{11,}$ $S_{12,}$

$S_{13,}$ and $S_{14,}$ etc. This leads to an inverter that is capable of continued operation despite fault events. This is particularly significant when BESS is utilized for power delivery of safety critical infrastructure systems.

Oppositely, topologies proposed in the literature either have high implementation costs due to the use of a redundant battery or provide lower power quality with hardly noticeable enhancements to the reliability. The techniques of adding redundant cells would cause control difficulty for SOC balancing. Furthermore, prior fault-tolerant methods can only be applied to CHBs which are a sub-branch of MMCs. However, the presented approach can be applied to all types of MMCs.

The presented topology is implemented through an addition of four switches as displayed in Figure 4.1. T1 and T2 are either contactors or TRIACs, and are normally open. These switches and contactors are turned-on when the fault detection method indicates there is a fault. In case of a fault event in S_{n1} or S_{n3}, the switch S_{an} would begin operation to replace the faulty switch. Similarly, for faults in S_{n2} or S_{n4}, S_{bn} is turned-on in order to make up the lost switch. S_{an} and S_{bn} each consist of oppositely configured devices, and the reasons behind that is to avoid any current path through their anti-parallel diodes when the inverter operates under normal conditions. For better comprehension of this approach, assume the scenario when a fault has occurred in S_{11} and the output voltage has lost one level. There are two main steps necessary for the presented topology to compensate the output voltage level. First, T1 or T2, depending on the fault location, needs to be turned on. Subsequently, the redundant switch respective to the faulty switch would begin operation using the same PWM signal as the failed switched. Hence the system would be capable of continuing seamless operation despite a fault.

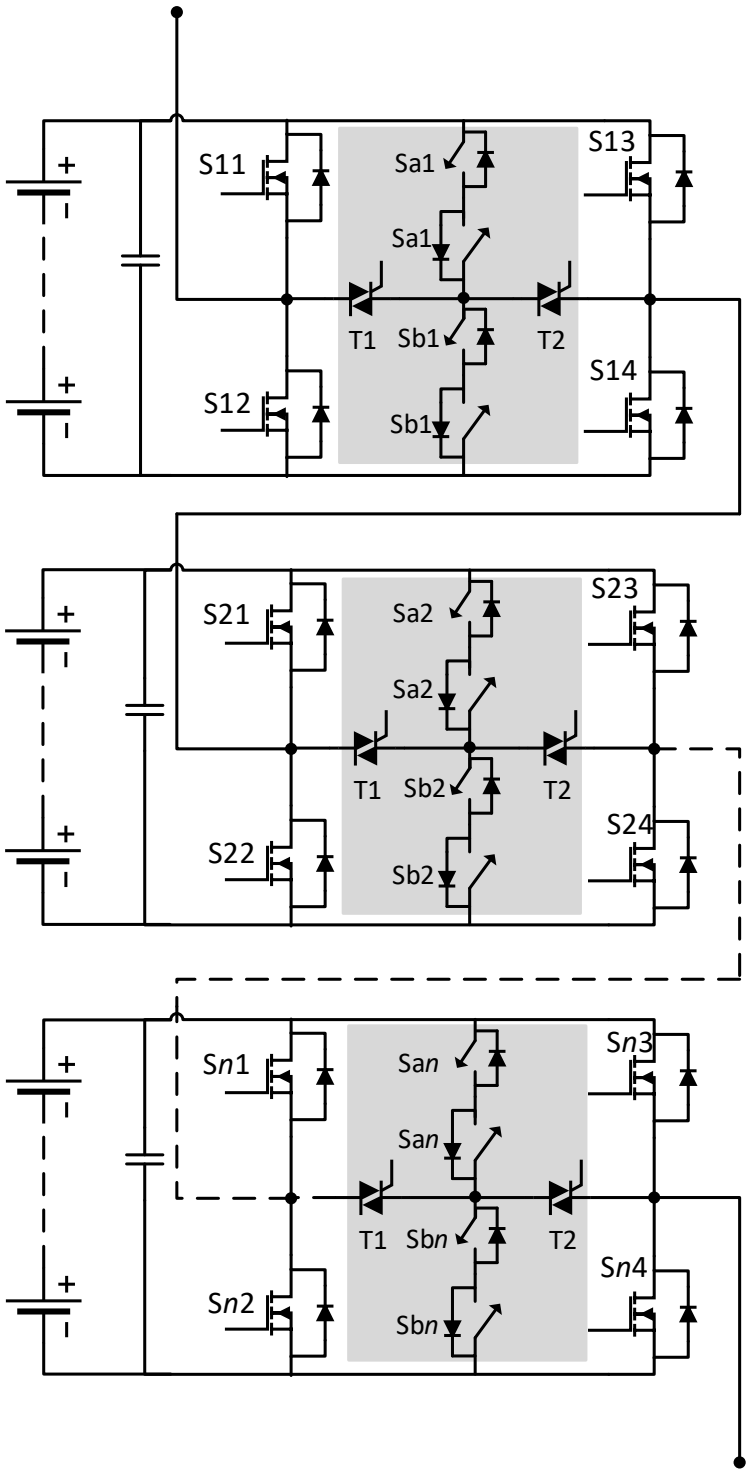


Figure 4.1 Schematic showing a novel reconfiguration CHB multilevel inverter.

4.3 Analysis of Fault-Tolerant Operation in Different Scenarios

The proposed reconfiguration of the CHB inverter for fault-tolerant operation is shown in Figure 4.1. In normal operation, leg voltages could be expressed as a function of the upper or lower switches. The leg voltage from Table 3.1 for the 7-level cascaded H-Bridge inverter can be calculated as a function of the upper switches ($S_{n1}$and S_{n3}) as

$$V_{leg} = (S_{11} - S_{13})V_{dc1} + (S_{21} - S_{23})V_{dc2} + (S_{31} - S_{33})V_{dc3} \quad (4\text{-}1)$$

Also, from Table 3.1 in Chapter 3, the leg voltage could be expressed as a function of the lower switches (S_{n2} and S_{n4}) as

$$V_{leg} = (S_{14} - S_{12})V_{dc1} + (S_{24} - S_{22})V_{dc2} + (S_{34} - S_{32})V_{dc3} \quad (4\text{-}2)$$

In addition to Eqs. (4-1) and (4-2), the leg voltage of a single-phase inverter can be expressed as a function of the all the switches as

$$V_{leg} = \{(S_{11} - S_{13}) + (S_{14} - S_{12})\}\frac{V_{dc1}}{2} + \{(S_{21} - S_{23}) + (S_{24} - S_{22})\}\frac{V_{dc2}}{2} + \{(S_{n1} - S_{n3}) + (S_{n4} - S_{n2})\}\frac{V_{dc3}}{2} \quad (4\text{-}3)$$

The importance of Eq. (4-3) is because it clearly shows a relationship between all the switches and the output voltage. Consequently, it will make is easier for the reader to track the actions mathematically when a fault occurs in the inverter.

To analyze the fault-tolerant operation of the CHB inverter, Figure 4.1 is examined with different fault scenarios. It is worth mentioning that the proposed topology is not limited to the following cases.

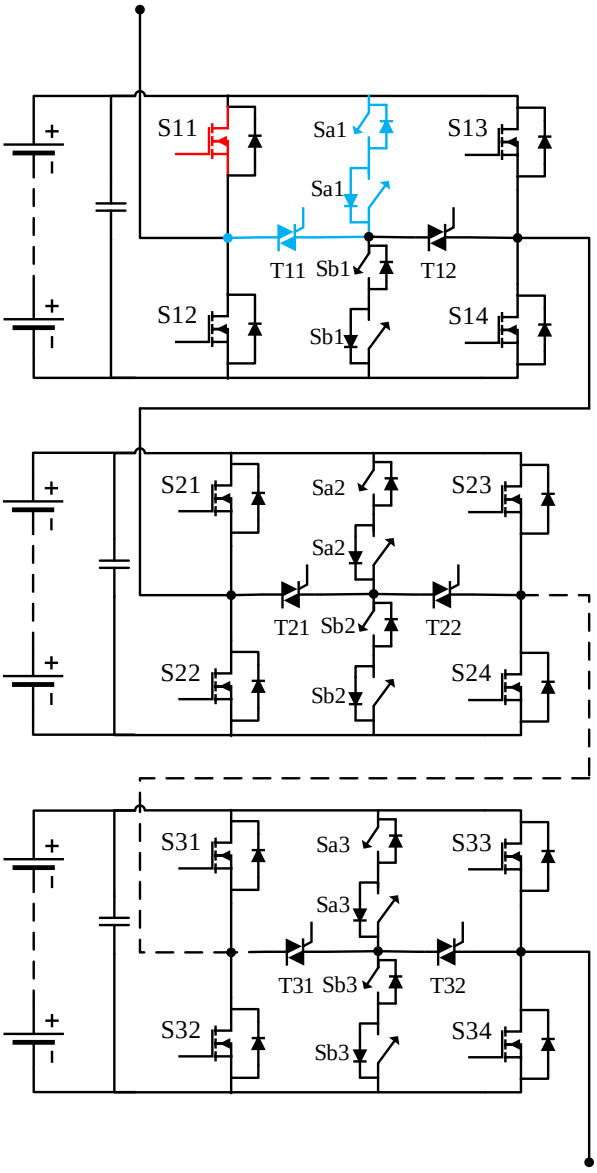


Figure 4.2 Reconfiguration and open-circuit faults switch on S_{11}, where blue lines indicate the reconfigurable path and red lines indicate the fault location.

4.3.1 Case 1 - S_{11} Has an Open-Circuit Fault

When S_{11} has an open-circuit fault and $i > 0$, the output voltage of the upper H-bridge of Figure 4.1 is either $-V_{dc}$ or 0, and there are no possible positive voltages to be generated by the inverter. That is, the anti-parallel diode of S_{11} is blocking the current path and restricting any positive output voltage.

Once the fault is detected, as described in Chapter 3, the reconfigurable circuit is activated through T1 and S_{a1}. That is, T1 is a normally open device, and when there is a fault on S_{11}, T1 is turned on. The PWM for S_{a1} is generated as the PWM signals for S_{11}. Case 1 is shown in Figure 4.2 where the blue lines indicate the reconfigured path, and red lines indicate the fault location.

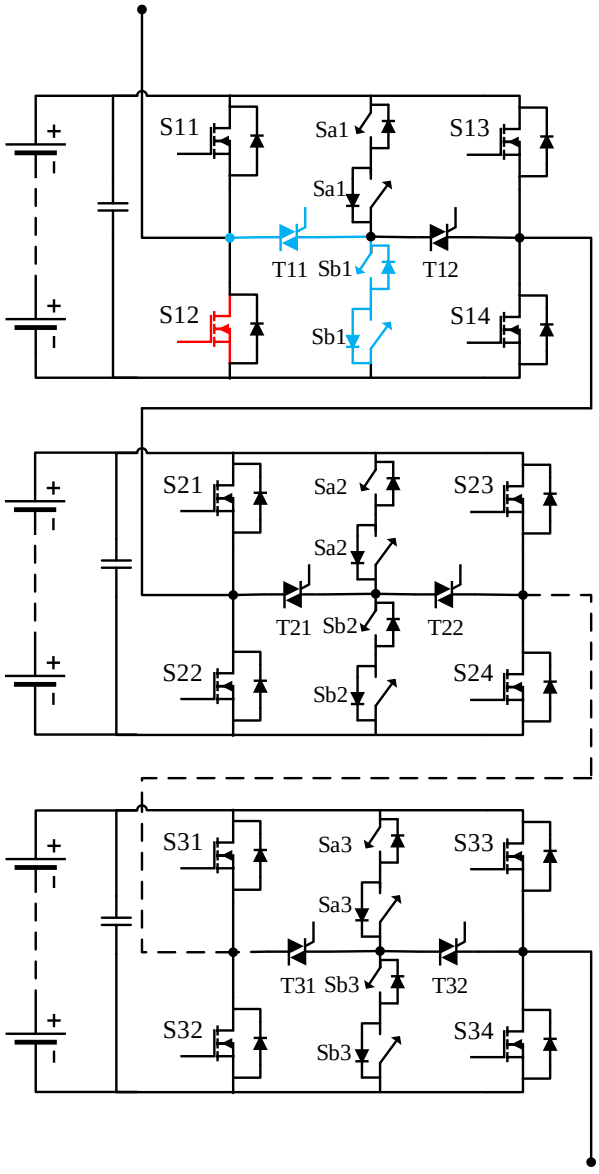


Figure 4.3 Reconfiguration and open-circuit faults switch on S_{12}, where blue lines indicate the reconfigured path and red lines indicate the fault location.

The leg voltage of the inverter can be written as

$$V_{leg} = \{(S_{a1} - S_{13}) + (S_{14} - S_{12})\}\frac{V_{dc1}}{2} + \{(S_{21} - S_{23}) + (S_{24} - S_{22})\}\frac{V_{dc2}}{2} +$$

$$\{(S_{n1} - S_{n3}) + (S_{n4} - S_{n2})\}\frac{V_{dc3}}{2} \quad (4\text{-}4)$$

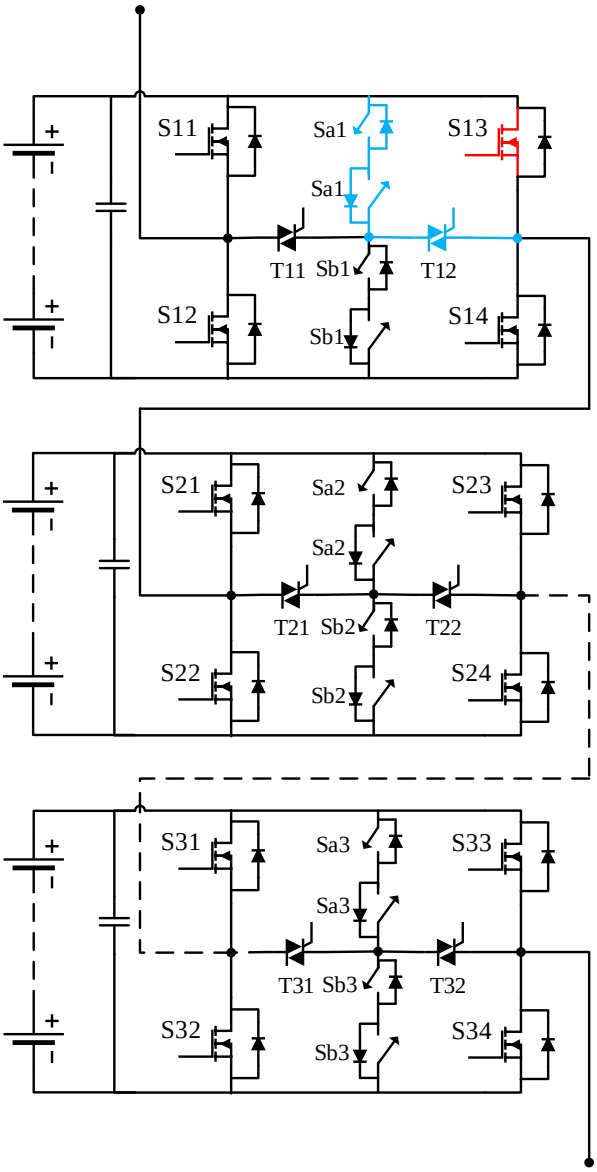


Figure 4.4 Reconfiguration and open-circuit faults switch on S_{13}, where blue lines indicate the reconfigured path and red lines indicate the fault location.

4.3.2 Case 2 - S_{12} Has an Open-Circuit Fault

The first H-bridge cell of the inverter in Figure 4.3 can generate either $+V_{dc}$ or 0 voltage levels, due to the current path being blocked by the anti-parallel diode of S_{12}. Once the fault is identified, the reconfigurable circuit T1 and S_{b1} are activated to provide a current path for inverter.

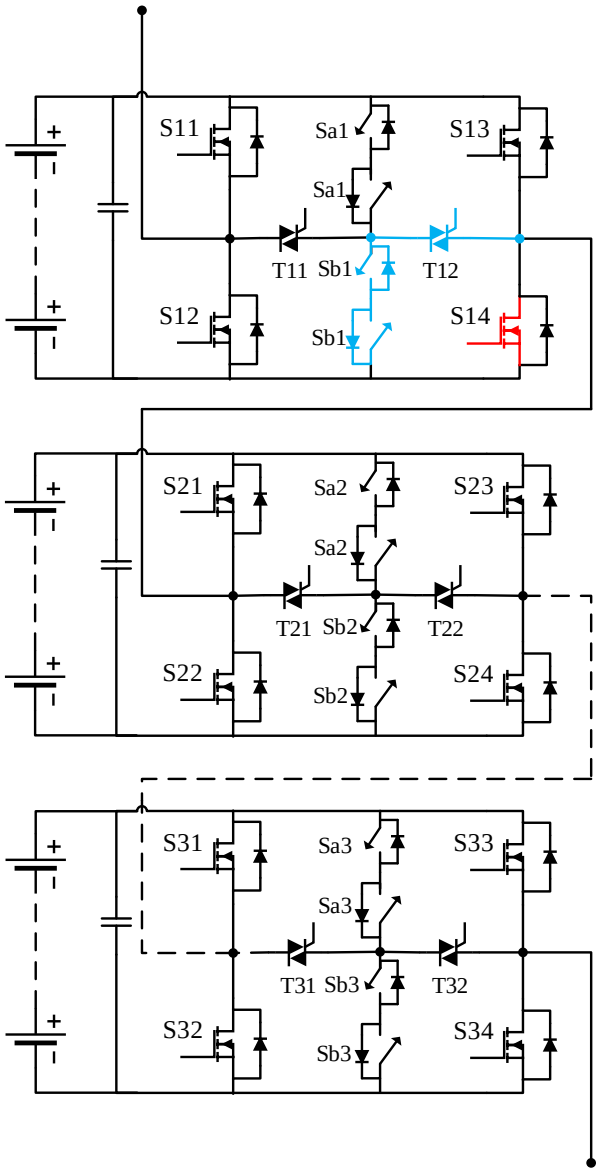


Figure 4.5 Reconfiguration and open-circuit faults switch on S_{14}, where blue lines indicate the reconfigured path and red lines indicate the fault location.

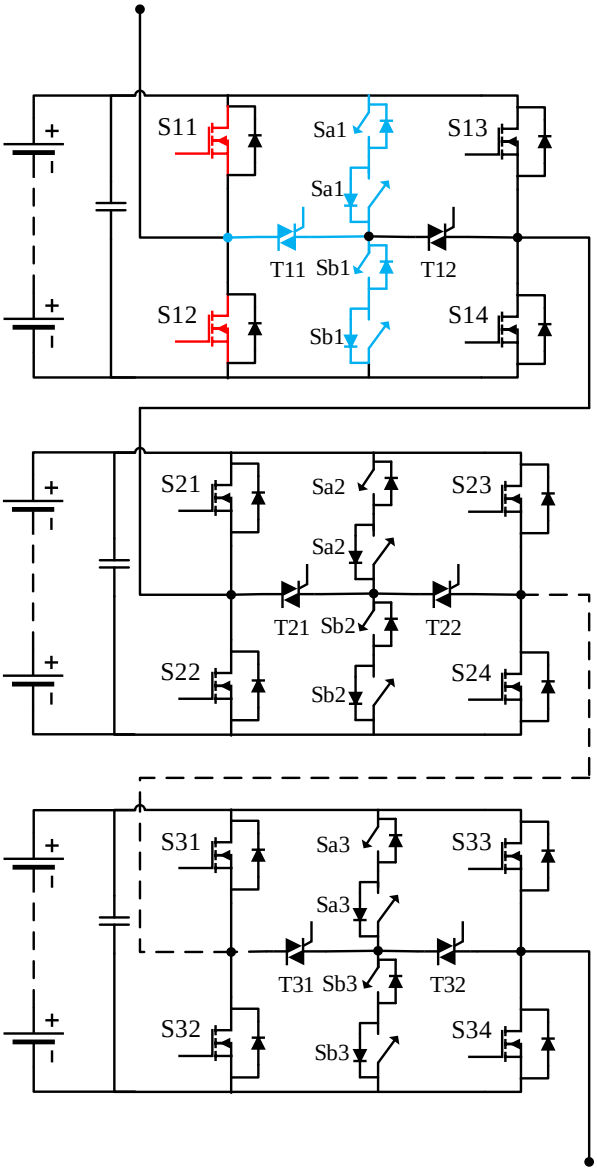


Figure 4.6 Reconfiguration and open-circuit faults switch on S_{11} and S_{12}, where blue lines indicate the reconfigured path and red lines indicate the fault location.

The inverter output voltage can be expressed as

$$V_{leg} = \{(S_{11} - S_{13}) + (S_{14} - S_{b1})\}\frac{V_{dc1}}{2} + \{(S_{21} - S_{23}) + (S_{24} - S_{22})\}\frac{V_{dc2}}{2} + \{(S_{n1} - S_{n3}) + (S_{n4} - S_{n2})\}\frac{V_{dc3}}{2} \quad (4\text{-}5)$$

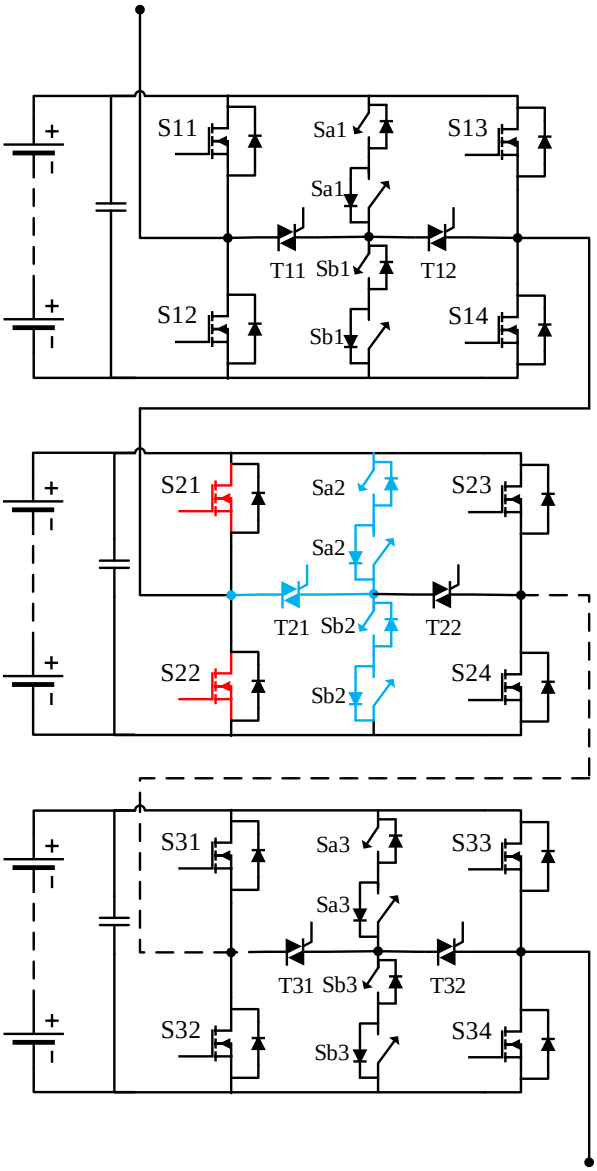


Figure 4.7 Reconfiguration and open-circuit faults switch on S_{21} and S_{22}, where blue lines indicate the reconfigured path and red lines indicate the fault location.

4.3.3 Case 3 - S_{13} Has an Open-Circuit Fault

The upper H-bridge in Figure 4.4 can generate either V_{dc} or 0 voltage level due to the current path being blocked by the anti-parallel diode of S_{13}. After the fault located, the isolation and reconfiguration steps are taking place to compensate for the missing voltage. The reconfigurable

circuits T1 and S_{b1} are activated to provide a current path for inverter. The inverter output voltage can be expressed as

$$V_{leg} = \{(S_{11} - S_{a1}) + (S_{14} - S_{12})\}\frac{V_{dc1}}{2} + \{(S_{21} - S_{23}) + (S_{24} - S_{22})\}\frac{V_{dc2}}{2} + \{(S_{n1} - S_{n3}) + (S_{n4} - S_{n2})\}\frac{V_{dc3}}{2} \quad (4\text{-}6)$$

4.3.4 Case 4 - S_{14} Has an Open-Circuit Fault

The faulty H-bridge of the inverter in Figure 4.5 can generate either $-V_{dc}$ or 0 voltage level due to the current path being blocked by the anti-parallel diode of the anti-parallel diode of S_{14}. The compensation mode for this case can be implemented by activating T2 and S_{b1}. That is, as shown in Figure 4.5, S_{14} is replaced by $S_{b1}$when a fault occurs, and T2 provides a current path for the inverter. The inverter output voltage can be written as

$$V_{leg} = \{(S_{11} - S_{13}) + (S_{b1} - S_{12})\}\frac{V_{dc1}}{2} + \{(S_{21} - S_{23}) + (S_{24} - S_{22})\}\frac{V_{dc2}}{2} + \{(S_{n1} - S_{n3}) + (S_{n4} - S_{n2})\}\frac{V_{dc3}}{2} \quad (4\text{-}7)$$

4.3.5 Case 5 - S_{11}, and S_{12} Have Open-Circuit Faults

One of the advantages of the proposed method is its capability to compensate for multiple faults. In case 5, it is assumed the faults occur in two different switches at the same H-bridge cell, S_{11} and S_{12}. The proposed fault-tolerant reconfiguration circuit compensate for the missing voltages by activate T1, S_{a1} and S_{b1}. In order to ensure stable operation, T1 is turned on, and the faulty switches replace the reconfigurable switches Sa1 and Sb1 as shown in Figure 4.6. That is, S_{a1} replaces the faulty switch S_{11}, while the faulty switch S_{12} is replace by S_{b1}. The leg output voltage of the inverter in case of S_{11} and S_{12} have an open-circuit fault shown below

$$V_{leg} = \{(S_{a1} - S_{13}) + (S_{14} - S_{b1})\}\frac{V_{dc1}}{2} + \{(S_{21} - S_{23}) + (S_{24} - S_{22})\}\frac{V_{dc2}}{2} +$$

$$\{(S_{n1} - S_{n3}) + (S_{n4} - S_{n2})\}\frac{V_{dc3}}{2} \quad (4\text{-}8)$$

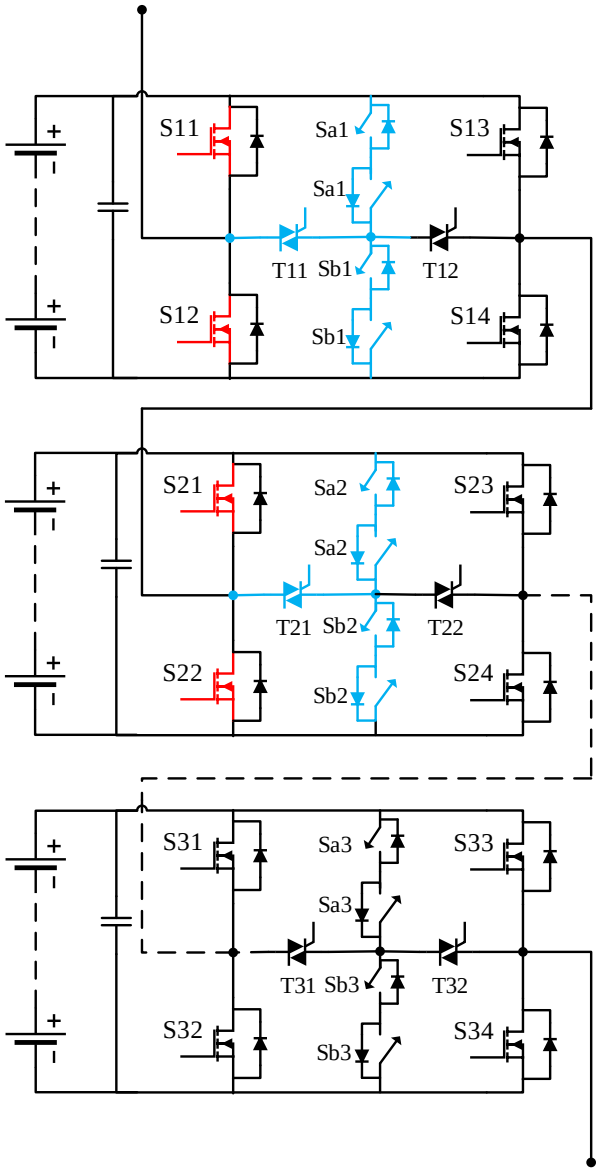


Figure 4.8 Reconfiguration and open-circuit faults switch on S_{11}, S_{12}, S_{21} and S_{22}, where blue lines indicate the reconfigured path and red lines indicate the fault location.

4.3.6 Case 6 - S_{21} and S_{22} Have Open-Circuit Faults

The faulty switches in this case are in the second H-bridge of the inverter in Figure 4.1. T1, S_{a2}, and S_{b2} are activated to compensate for the faults and ensure the output voltage of the inverter as same as the normal operation. In other words, the reconfiguration mode activated by turning on T1, S_{a1}, and S_{b2} of the second H-bridge are shown in Figure 4.7. The output voltage of the inverter is

$$V_{leg} = \{(S_{11} - S_{13}) + (S_{14} - S_{12})\}\frac{V_{dc1}}{2} + \{(S_{a2} - S_{23}) + (S_{24} - S_{b2})\}\frac{V_{dc2}}{2} + \{(S_{n1} - S_{n3}) + (S_{n4} - S_{n2})\}\frac{V_{dc3}}{2} \quad (4\text{-}9)$$

4.3.7 Case 7 - S_{11}, S_{12}, S_{21} and S_{22} Have Open-Circuit Faults

During this case, the fault is assumed to happen in four different switches, two of them in the upper H-bridge, and two in the second H-bridge cell of the inverter in Figure 4.8. During this case, the configuration mode is activated by replacing the faulty switches S_{11}, S_{12}, S_{21}, and S_{22} with S_{a1}, S_{b1}, S_{a2}, and S_{b2}. The output voltage of the inverter can be written as

$$V_{leg} = \{(S_{a1} - S_{13}) + (S_{14} - S_{b1})\}\frac{V_{dc1}}{2} + \{(S_{a2} - S_{23}) + (S_{24} - S_{b2})\}\frac{V_{dc2}}{2} + \{(S_{n1} - S_{n3}) + (S_{n4} - S_{n2})\}\frac{V_{dc3}}{2} \quad (4\text{-}10)$$

4.4 Comparison

In order to present a more comprehensive evaluation, the proposed fault-tolerant scheme is compared with the fault-tolerant schemes in [4.1] and [4.2]. Table 4.1 provides a comparison of the circuit parameters and reliabilities of the aforementioned topologies. V_{dc} is the dc link voltage of each individual cell before occurrence of any faults. Table 4.1 shows clear superiority of the

proposed topology in the number of relays and in the fact that not needing any switches with $2V_{dc}$ or $3V_{dc}$ voltage stress handling capability would decrease the cost of implementation. It can be inferred from Table 4.1 that the proposed fault-tolerant scheme has the highest reliability.

Table 4.1 Comparison of Fault-Tolerant Techniques (7-level – single phase)

Topology	Proposed Topology	[4.2]	[4.1]
Number of Power Switches	24	16	12
Number of Relays	6	20	12
Maximum Voltage Stress on a Switch/Diode	1Vdc	3Vdc	3Vdc
Number of Switches Designed for $0.5V_{dc}$ Voltage Stress	12	0	0
Number of Switches Designed for $1V_{dc}$ Voltage Stress	12	12	0
Number of Switches Designed for $2V_{dc}$ Voltage Stress	0	0	0
Number of Switches Designed for $3V_{dc}$ Voltage Stress	0	4	12
Control Difficulty	Easy	Moderate	Difficult

4.5 Simulation and Experimental Results

In order to prove the concept of the proposed reconfiguration circuit for CHB MLI, a detailed MATLAB/Simulink model was created to investigate the functionality of the proposed topology circuit. The first fault condition was implemented by creating open-circuit switching faults in a 7-level cascaded H-bridge inverter. The faults were applied to S_{11} and S_{12} as shown in Figure 4.9. The fault detection algorithm in [4.3] is applied here to show the closed-loop controller

performance. Figure 4.9 shows the simulation result of the reconfiguration method when S_{11} and S_{12} failed. A delay time of 0.05s for the fault identification method is implemented to ensure that the simulation results are visible for the reader. Consequently, it would be easier to indicate the transition modes, which are: pre-fault condition, fault detection mode, and post-fault condition (reconfiguration). When the first fault occurs at S_{11}, the output waveforms miss one voltage and current levels, which leads to an unbalanced output. However, after the first fault occurs, the reconfiguration topology is activated. It can be seen from Figure 4.9 that the system maintains the same output waveforms compared with the normal operation condition. After the reconfiguration circuit compensated for the first fault, another fault was created on S_{12}. After three fundamental cycles, the reconfiguration method was activated and compensated for the fault. Figure 4.10 shows the result for a similar scenario where two different faults were created on S_{21} and S_{22}. The results verify that this circuit can continue providing fault tolerance for two faults in each cell as long as the second fault in the respective cell occurs in the same leg as the first fault. Therefore, the proposed inverter has the ability to ameliorate the system performance when a fault occurs. Also, it can manage multiple faults at the same time which increases the system reliability. The power quality of the system is another advantage where the same output voltage/current THD is maintained without the need to modify the output filter.

A scaled down 7- level reconfigurable CHB low-power prototype has been built and tested in the laboratory as shown in Figure 4.11 to validate the concept and performance of the new circuit. The created fault has been implemented on S_{11} and S_{12} by misfiring their gate driver. The occurrence of the faults in S_{11} and S_{12} results in missing one voltage level for each fault condition. In other words, the third voltage level is missed in case S_{11} was the faulty switch, while the lowest voltage level is missed when the fault was created in S_{12} as shown in Figure 4.11. To make sure

that the fault detection algorithm can detect the fault with a time that makes the results clear for the reader to recognize the reconfiguration topology, a three-cycle delay is gathered with the detection time. Figure 4.12 shows two switching faults, S_{21} and S_{22}.

The proposed topology has been tested with four faults that were created on S_{11}, S_{12}, S_{21}, and S_{22} as displayed in Figure 4.13. The results show the capability of the proposed topology to handle more than one fault and maintain the output voltage and current the same as the regular operation.

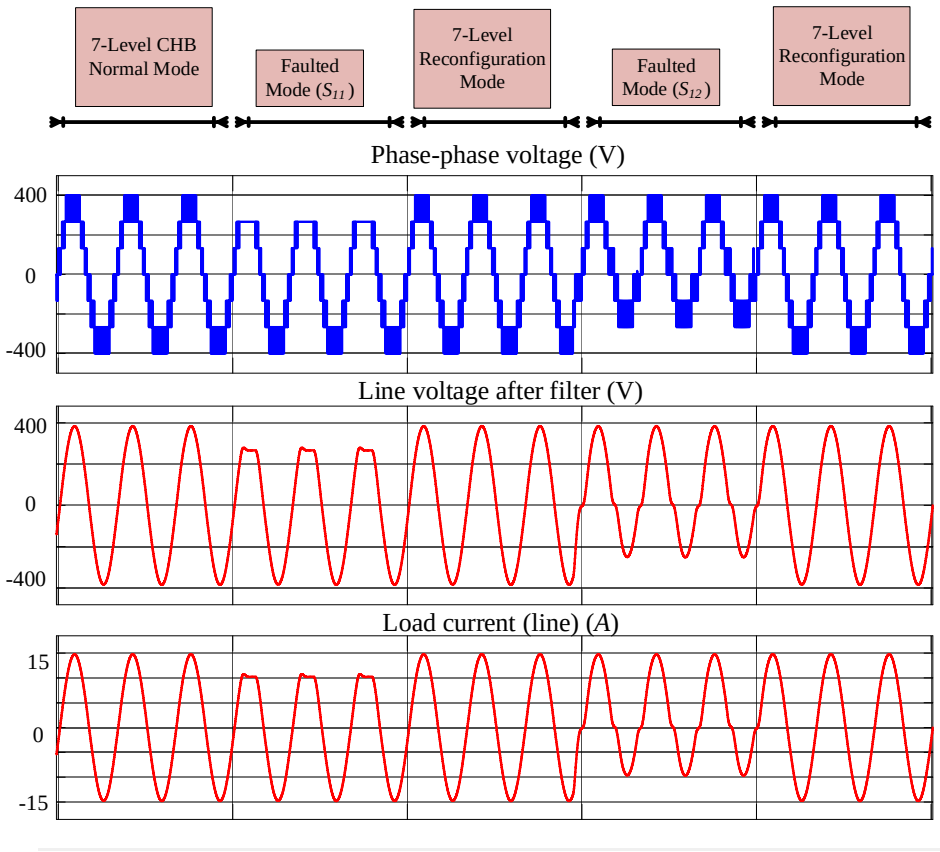


Figure 4.9 Simulation result of reconfiguration and open-circuit faults switch on S_{11} and S_{12}.

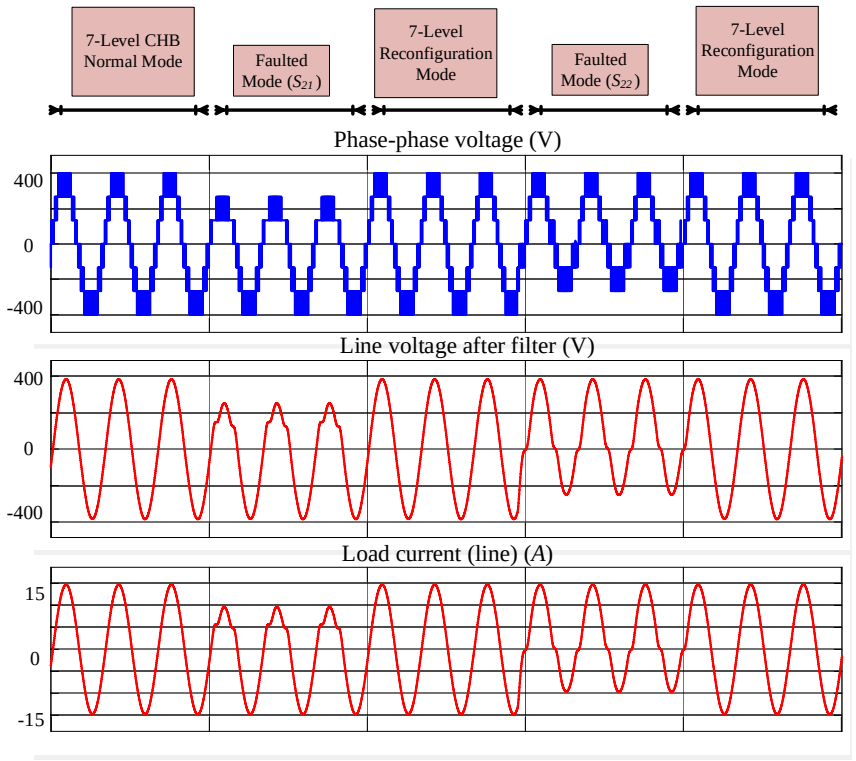
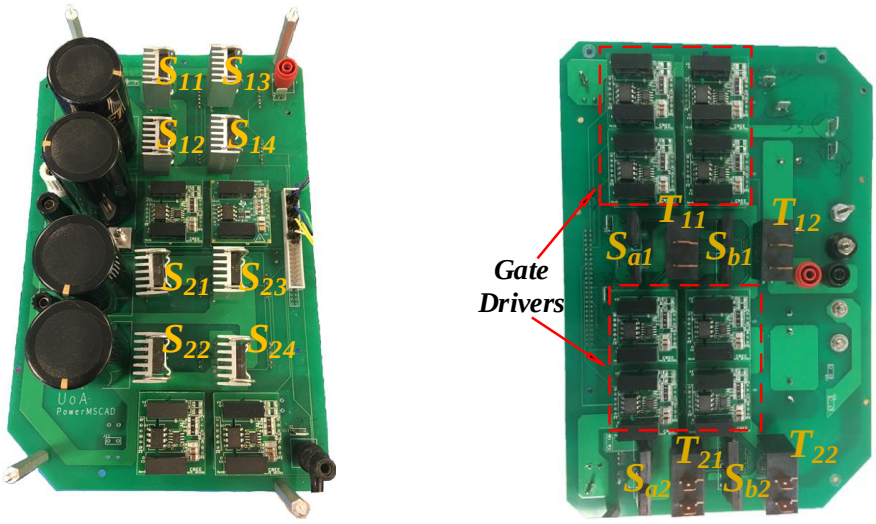


Figure 4.10 Simulation result of reconfiguration and open-circuit faults switch on S_{21} and S_{22}.



(a) (b)

Figure 4.11 (a) Top view shows the proposed reconfiguration circuit for CHB inverter, (b) Bottom view shows the gate drivers and the reconfigurable circuits "Photo by Author."

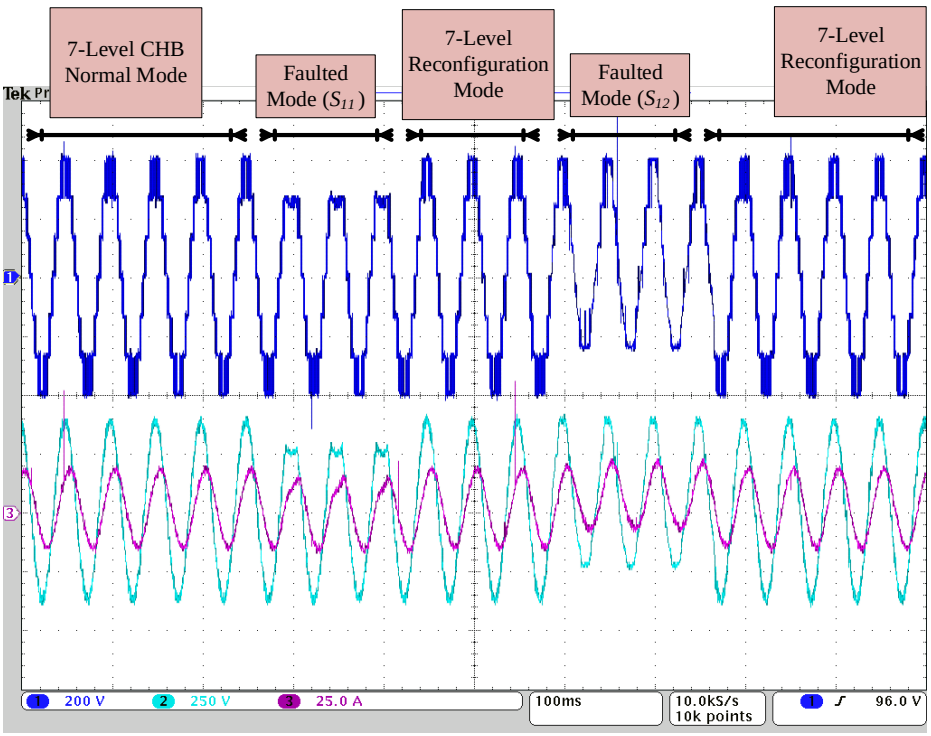


Figure 4.12 Experimental result of reconfiguration and open-circuit faults switch on S_{11} and S_{12}.

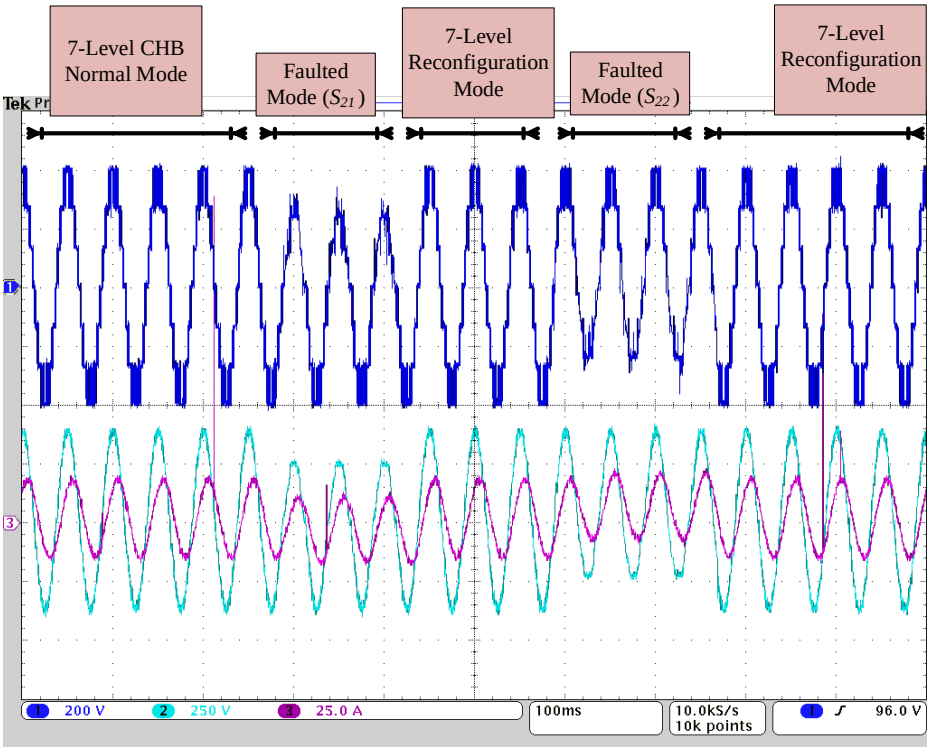


Figure 4.13 Experimental Result of Reconfiguration and Open-Circuit Faults Switch on S_{21} and S_{22}.

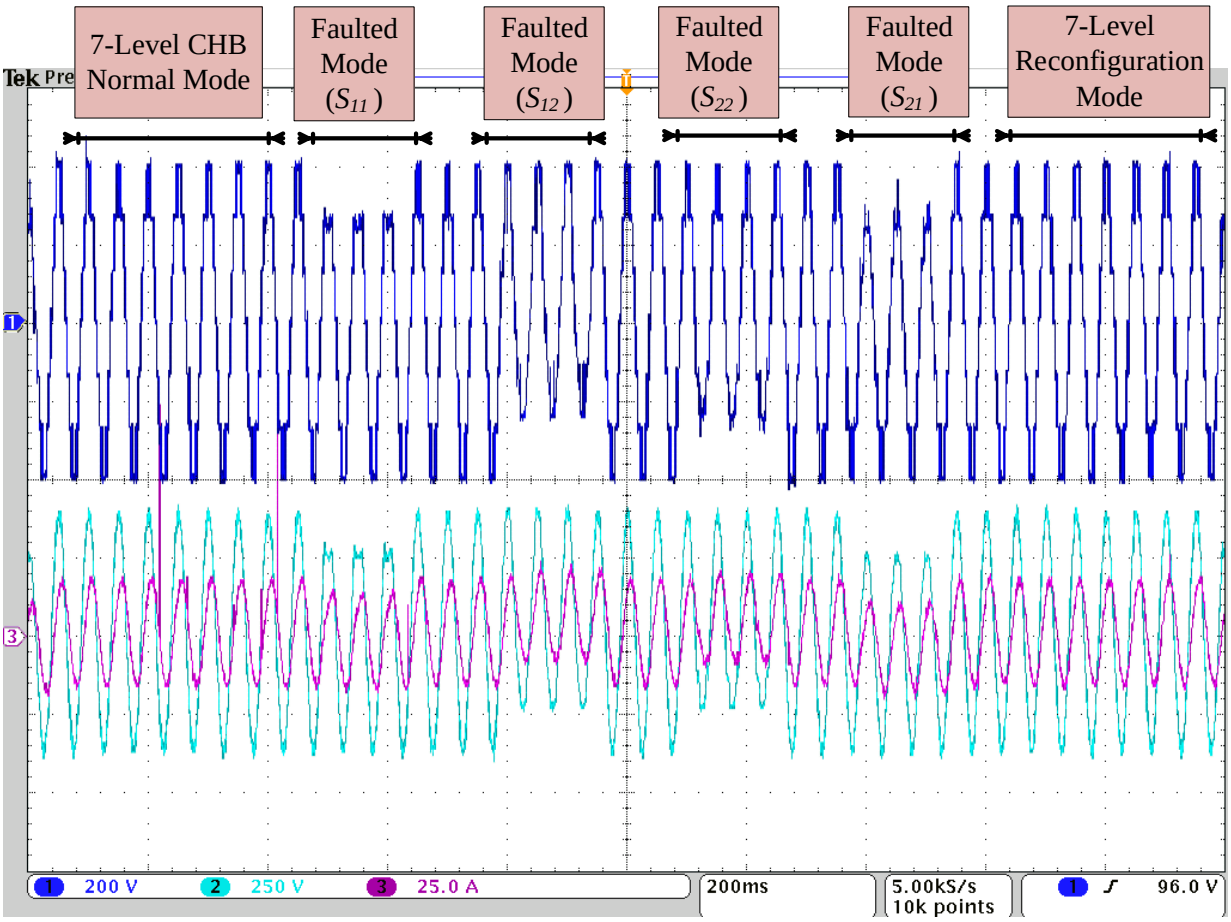


Figure 4.14 Simulation result of reconfiguration and open-circuit faults switch on S_{11}, S_{12}, S_{21}, and S_{22}.

4.6 Conclusions

This chapter presents a novel CHB inverter circuit for the fault-tolerant operation to ensure that it has the ability to compensate for the output voltage/current when a faulted condition occurs. The proposed topology in this chapter also has the ability to maintain the same output power under multiple faults. The operation principles of the proposed topology have been analyzed in detail with simulation and experimental results for a proof of the proposed concept. It shows the advantages of the proposed topology, where the reconfiguration method provides better output power quality.

4.7 References

[4.1] M. M. Haji-Esmaeili, M. Naseri, H. Khoun-Jahan, and M. Abapour, "Fault-tolerant structure for cascaded H-bridge multilevel inverter and reliability evaluation," *IET Power Electronics*, vol. 10, no. 1, pp. 59-70, 20 1 2017.

[4.2] H. K. Jahan, F. Panahandeh, M. Abapour, and S. Tohidi, "Reconfigurable Multilevel Inverter With Fault-Tolerant Ability," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7880-7893, Sept. 2018.

[4.3] H. Mhiesan *et al*., "A Method for Open-Circuit Faults Detecting, Identifying, and Isolating in Cascaded H-Bridge Multilevel Inverters," in *IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pp. 1-5, Charlotte, NC, 2018.

CHAPTER 5

A NOVEL MULTILEVEL X-CHB INVERTER WITH VOLTAGE DOUBLING GAIN

5.1 Introduction and Motivation

Multilevel inverter inverters (MLI) have been widely used in medium and high voltage applications, such as STATCOM, BESS, motor drives, and HVDC transmission systems. There are numerous reasons for why using MLIs over standard inverters are beneficial to the power industry. Some of those reasons are that they improve power quality, reduce the switching stress on semiconductor devices, and allow for boosting the output voltage to a desired value. The main MLI types are: neutral point-clamped (NPC), flying capacitor, and cascaded H-bridge (CHB).

In the BESS application, CHB is the best topology because it has the capability to inject zero voltage sequence and prevents circulating current. Many researchers have been trying to develop new MLIs for renewable applications. New 5-level inverter topologies in [5.1]- [5.14] and 7-level inverter topologies in [5.15]- [5.27] were presented with the goal of reducing the number of semiconductor devices, input power supplies, and passive elements.

However, there is still a need for a new MLI topology to: 1) boost the output voltage with a single power supply without needing an outer boosting stage, 2) reduce the number of active and passive components, 3) operate with different power factors, 4) reduce the volume, weight, and cost for the overall system, and 5) have fault-tolerant operation capability.

The aim of this chapter is to propose a new MLI topology for renewable energy applications. The main contributions of the proposed topology is as follows:

1- The main objective of the proposed topology is to reduce the number of batteries by 50% and provide the option of boosting the output voltage by a factor of 2. These

features introduce many advantages of the proposed topology which are summarized below:

a. Volume reduction due to requiring less batteries

b. Lower implementation cost due to fewer batteries used

c. Simplified battery management system

d. Reduction of fault probability occurrence

2- Has full active power injection ability

3- The proposed modulation technique ensures self-balancing for all of the flying capacitors

4- Ability to operate as 5 or 7-level inverter

5- Fault-tolerant to isolate the faulty switch when a fault has occurred.

5.2 Proposed Multilevel Boost X-CHB Inverter

5.2.1 Generalized X-CHB MLI

The proposed X-CHB topology is derived from the conventional inverter. It combines the well-known H-bridge and flying capacitor inverter topologies as shown in Figure 5-1. In order to enable this combination to have a boosting ability, two X-switches are added to the flying capacitor. The presented topology relies on charging the flying capacitor to the value of the input voltage and then boosting the output voltage by connecting both the flying capacitor and the input voltage in series through the X-switches (S_{11}, S_{12}).

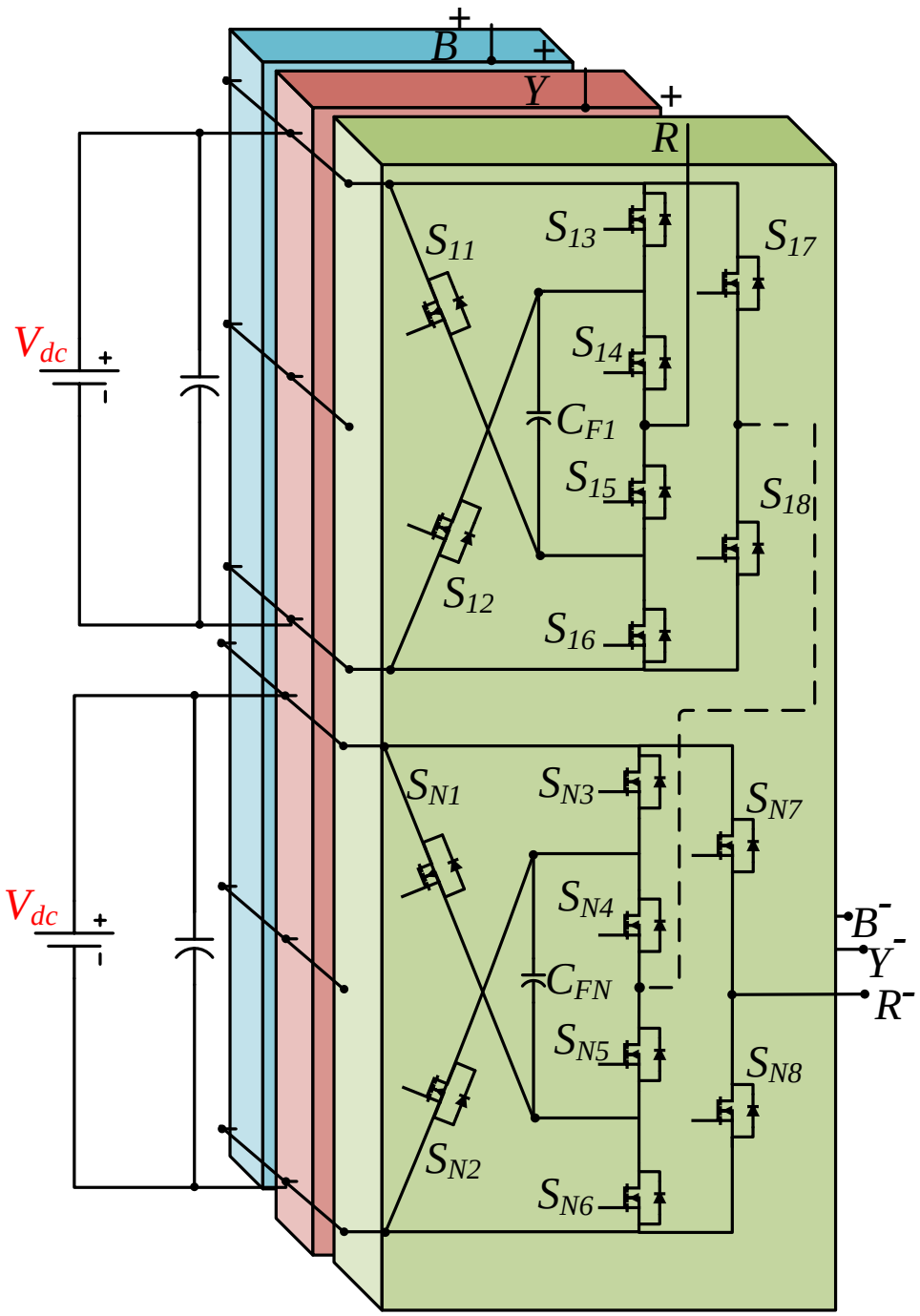


Figure 5.1 Proposed *n*-level three-phase X-CHB inverter.

The proposed X-CHB inverter has the ability to operate as either a 5-level inverter or 7-level inverter without the need for adding more switches, capacitors, or changing the circuit connections.

When the proposed topology operates as a 5-level inverter, it achieves a voltage gain of 2 times the input voltage. While operating as a 7-level inverter, the proposed topology has the ability to boost the output voltage up to 1.5X. It is worth mentioning that in both modes of operation (5-level/7-level), there is no change in the number of switches and the voltage is boosted without the requirement of inductors and/or a transformer.

The generalized proposed X-CHB multilevel inverter is displayed in Figure 5.1, where each phase is a set of series of X-CHB cells. As pointed out previously, each X-CHB has the ability to produce either 5 or 7 levels depending on the modulation strategy. The output of the generalized topology also depends on the modulation technique. When each X-CHB provides 5-level, the number of output voltage levels for the generalized topology is ($m = 4N + 1$). While the number of output voltage levels is ($m = 6N + 1$) for 7-level operation where N denotes the number of cells. It is noteworthy that the proposed generalized X-CHB multilevel inverter has ability to combine different operation modes for different X-CHB cells. In other words, some X-CHB cells may operate in 7-level mode, some in 5-level mode, and some in a combination of both 5-level and 7-level.

For better understanding, suppose the number of X-CHB cells is two. In this case if both X-CHB cells operate as 5-level, the number of output voltage levels of the inverter is nine. While the number of levels would be 13 when the X-CHB is producing 7-levels per cell. Moreover, suppose one X-CHB produces 5-level, and the other 7-level, then the number of the output voltage levels is 11. Below are the equations for the number of voltage levels in the three cases.

$$m = \begin{cases} 4N + 1, & 5\ level \\ 6N + 1 & 7\ level \\ 4N + 6N + 1 & Hybrid \end{cases} \tag{5-1}$$

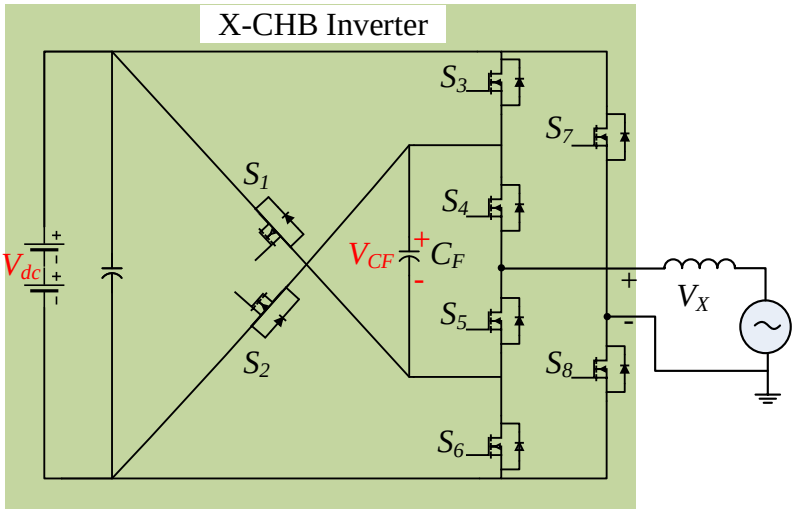


Figure 5.2 A proposed X-CHB inverter cell.

5.2.2 5-L Boost X-CHB Inverter

One X-CHB cell is shown in Figure 5.2. In this mode, each of the proposed X-CHB cells can produce five levels. As a result, the magnitudes of the generated voltage levels by the X-CHB are $2V_{dc}$, V_{dc}, 0, -V_{dc}, and -$2V_{dc}$. In other words, it has the capability to boost the voltage gain up to 2X when operating in 5-level mode. Each X-CHB cell consists of eight switches; S_1, S_2, S_3 , S_4 , S_5, S_6, S_7, and S_8, which are standard semiconductor devices. They could be either IGBTs or MOSFETs. Also, the X-CHB cell requires an additional flying capacitor (FC), C_F, to boost the voltage to 2X. In every switching cycle, C_F is charged to V_{dc} from its input dc-supply through S_3 and S_6. The X-switches (S_1 and S_2) are employed to create the second voltage level by connecting the dc-supply in series with C_F in order to boost the voltage to 2X.

The operation analysis for the proposed X-CHB inverter is illustrated in Figure 5.3. The output voltage of the X-CHB is defined as V_X. The operation analysis reveals six different switching modes (A to H). The red dotted line in Figure 5.3 represents the current path, and the

blue indicates the capacitor charging current path. Table 5.1 lists all possible switching states with their corresponding output voltages for the proposed X-CHB inverter.

The flying capacitor (C_F) is charged by circulating the current from the dc-power supply through switches S_3 and S_6 as shown in Figure 5.3 (a) and (e). The flying capacitor voltage (V_{CF}) is equal to the input voltage V_{dc}. To compensate the voltage level, the C_F voltage is discharged which results in the output voltage of the X-CHB V_X being boosted to $2V_{dc}$, as displayed in Figure 5.3 (c) and (g). This boost operation is carried out by discharging C_F during the positive cycle in series with the input voltage, when S_1, S_4 and S_8 are ON, and hence the X-CHB output voltage would be $2V_{dc}$ (V_X=$2V_{dc}$) as shown in Figure 5.3 (c).

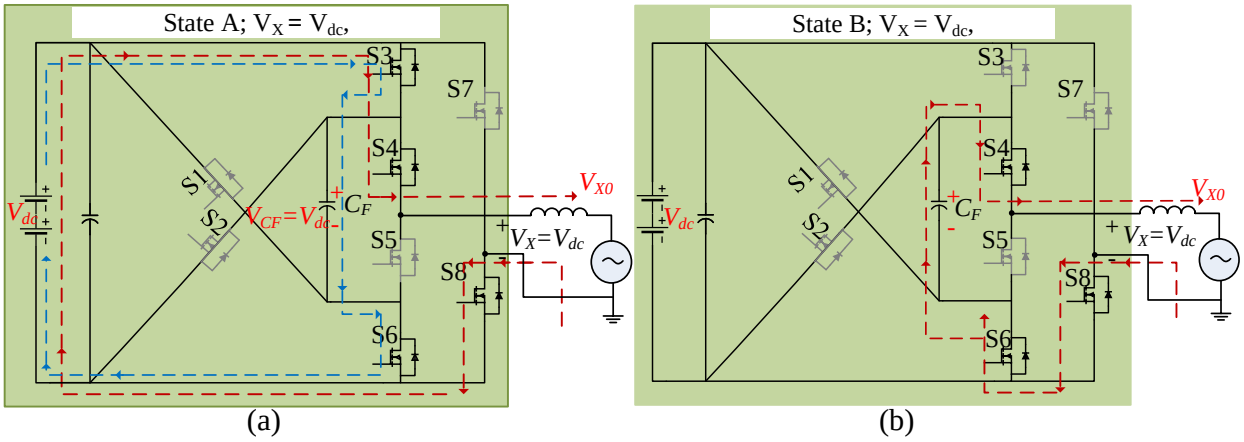


Figure 5.3 Switching analysis of the proposed 5-level X-CHB.

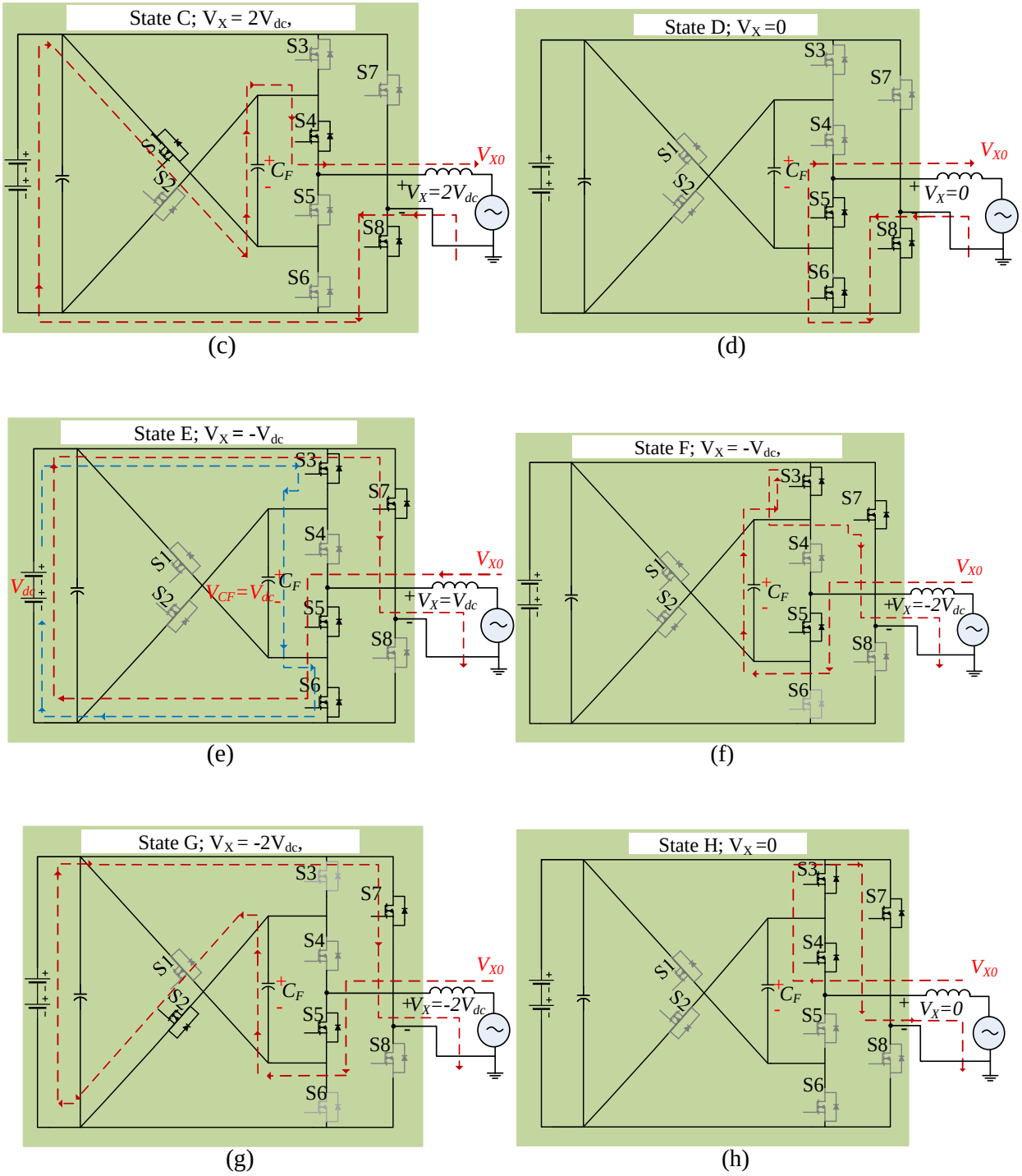


Figure 5.3 Switching states analysis of the proposed 5-level X-CHB (Cont.).

Table 5.1 Switching States of the Proposed 5-Level X-CHB Inverter

Switching States	V_X	**Active Switching States**								**Flying Capacitor**	
		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	$i_{Load} > 0$	$i_{Load} < 0$
A	$+V_{dc}$	0	0	1	1	0	1	0	1	↑	↓
B		0	0	0	1	0	1	0	1	↓	↑
C	$+2V_{dc}$	1	0	0	1	0	0	0	1	↓	↑
D	0	0	0	0	0	1	1	0	1	—	—
E	$-V_{dc}$	0	0	1	0	1	1	1	0	↑	↓
F		0	0	1	0	1	0	1	0	↓	↑
G	$-2V_{dc}$	0	1	0	0	1	0	1	0	↓	↑
H	0	0	0	1	1	0	0	1	0	—	—

Note: "—" means no effect, "↑" means charging, "↓" means discharging

Similarly, during the negative cycle, X-CHB can generate -2V_{dc} by discharging the flying capacitor and connecting it in series with input voltage through S_2, S_5, and S_7 as illustrated in Figure 5.3 (g). The output voltage of the 5-level X-CHB V_X that is shown in Figure 5.2 can be written by the formula below

$$V_X = 2V_{dc}(S_1 - S_2) + V_{dc}(S_4S_6S_8 - S_3S_5S_7) \quad (5\text{-}2)$$

5.2.3 7-L Boost X-CHB Inverter

The proposed 5L-boost X-CHB inverter can easily achieve higher voltage levels without changing the proposed circuit structure. In other words, as mentioned in previous subsections, each X-CHB can either produce 5-level or 7-level. When the proposed inverter produces 7 levels, it can boost the output voltage gain by 1.5X.

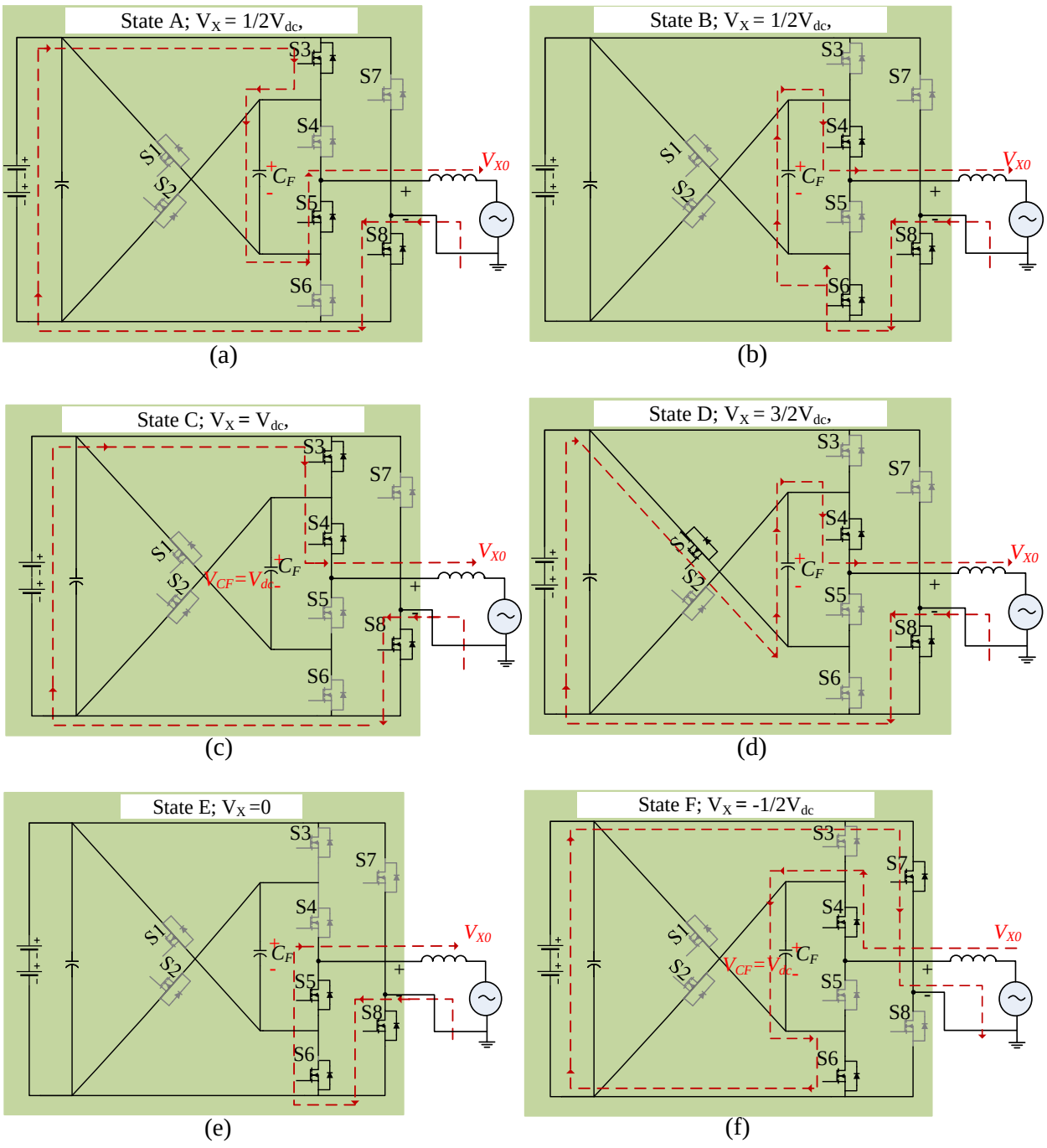


Figure 5.4 Switching states analysis for a 7-level X-CHB inverter.

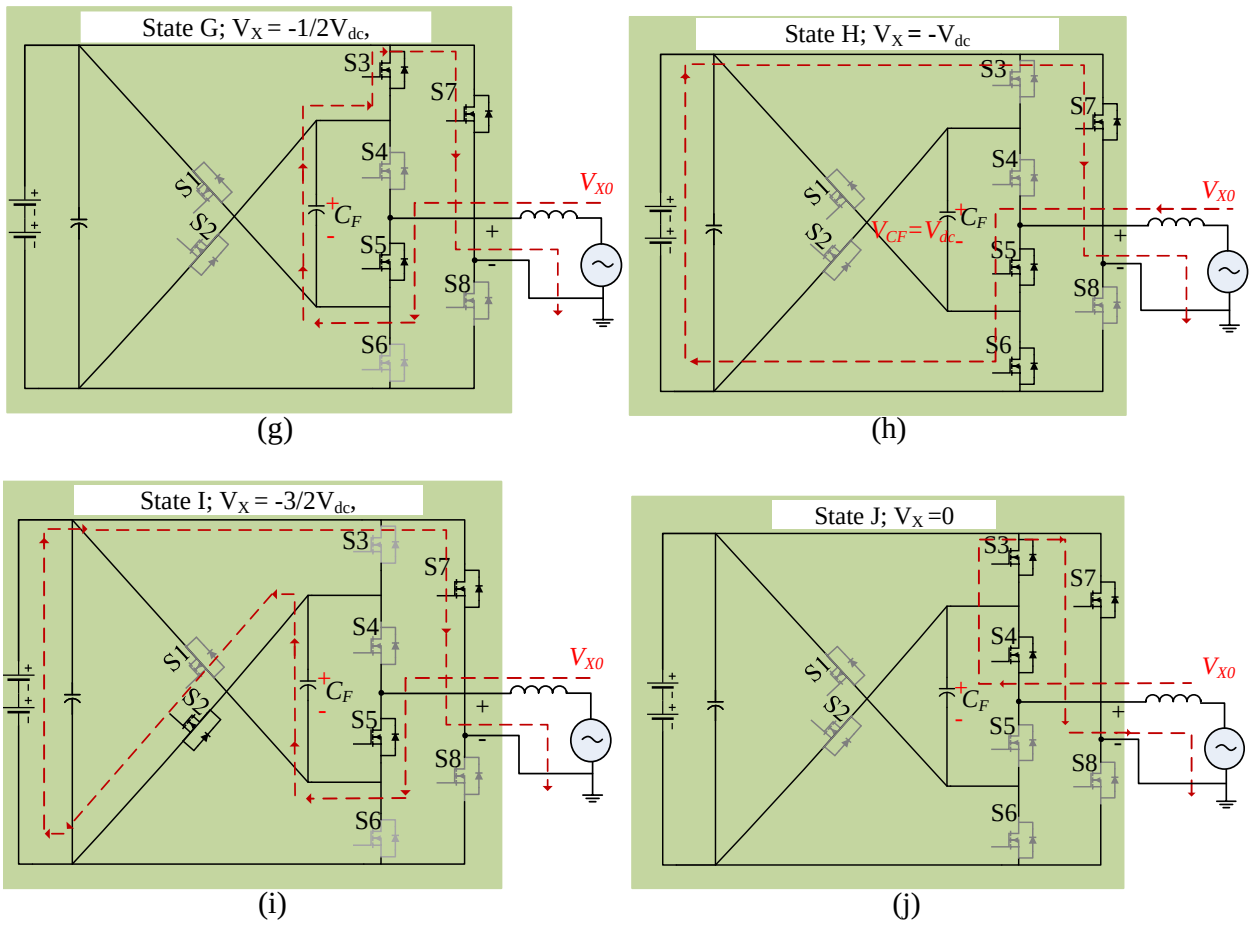


Figure 5.4 Switching states analysis for a 7-level X-CHB inverter (Cont.).

In this mode of operation, the flying capacitor is charged to $0.5V_{dc}$ using the input dc power supply by circulating the current through S_3 and S_6. The X-switches, S_1 and S_2, are employed to create the third voltage level by connecting the dc supply with the flying capacitor in series in order to boost the voltage to 1.5X. The output voltage levels when the proposed topology operates as 7-level inverter are $1.5V_{dc}$, V_{dc}, $0.5V_{dc}$, 0, $-V_{dc}$, $-0.5V_{dc}$and $-1.5V_{dc}$.

The operational analysis for the 7L-Boot X-XHB is illustrated in Figure 5.4. The operational analysis shows ten different switching modes (A to J). The red dotted line in Figure 5.4 represents the current path, and the blue indicates the capacitor charging current path. Table 5.2 lists all possible switching states with their corresponding output voltage for the proposed X-CHB inverter.

Table 5.2 Switching States of the Proposed 7-Level X-CHB Inverter

Switching States	V_X	**Active Switching States**								**Flying Capacitor**	
		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	$i_{Load} > 0$	$i_{Load} < 0$
A	$+1/2V_{dc}$	0	0	1	0	1	0	0	1	↑	↓
B		0	0	0	1	0	1	0	1	↓	↑
C	$+V_{dc}$	0	0	1	1	0	0	0	1	—	—
D	$+3/2V_{dc}$	1	0	0	1	0	0	0	1	↓	↑
E	0	0	0	0	0	1	1	0	1	—	—
F	$-1/2V_{dc}$	0	0	0	1	0	1	1	0	↑	↓
G		0	0	1	0	1	0	1	0	↓	↑
H	$-V_{dc}$	0	0	0	0	1	1	1	0	—	—
I	$-3/2V_{dc}$	0	1	0	0	1	0	1	0	↓	↑
J	0	0	0	1	1	0	0	1	0	—	—

Note: "—" means no effect, "↑" means charging, "↓" means discharging

5.3 Cost/Weight/Volume Analysis

The proposed topology is a combination of CHB and FC that results in a boost inverter. The comparison of the proposed topology and the conventional CHB with regards to the weight, volume, and cost is conducted based on the prototype presented in [5.2]. A 4.16 kV/325 kWh CHB has been evaluated to investigate cost/weight/volume for the system's main components: batteries, cooling system, semiconductor devices, capacitors, sensing/conditioning boards, and gate drivers.

It is clear from Figure 5.5 (a-c) that the highest cost, weight, and volume are associated with the batteries. Cost analysis reveals that the batteries constitute 75% of the total cost, 97% of the total weight, and 94% of the total volume. The proposed X-CHB topology provides a 50%

reduction in the number of batteries, which results in an enormous impact on the system power density.

Table 5.3 Switching Action to Isolate the Cells in Case of a Short Circuit Fault

Faulty Switch	Reconfiguration switching sequence
S_1	S_3, S_4, S_7
S_2	S_5, S_6, S_8
S_3	S_3, S_4, S_7
S_4	S_3, S_4, S_7
S_5	S_5, S_6, S_8
S_6	S_5, S_6, S_8
S_7	S_3, S_4
S_8	S_5, S_6

5.4 Fault-tolerant Ability

As previously mentioned, the proposed topology has the ability to operate with a modular structure to achieve higher output voltage by connecting several X-CHB in series. As pointed out in Chapters 3 and 4, the higher the number of semiconductor devices, the higher the possibility of switching failures. When a switching fault happens, the output voltage and current get distorted, and may result in system shutdown. Reliability and robustness must be kept in mind while designing any new multilevel inverter topology. A reliable inverter topology should be capable of isolating faults and reconfiguring to maintain normal operational characteristics if a fault in the system has occurred.

The modularity of the proposed topology enables it to isolate the faulty X-CHB cell from the entire system and reconfigure the circuit.

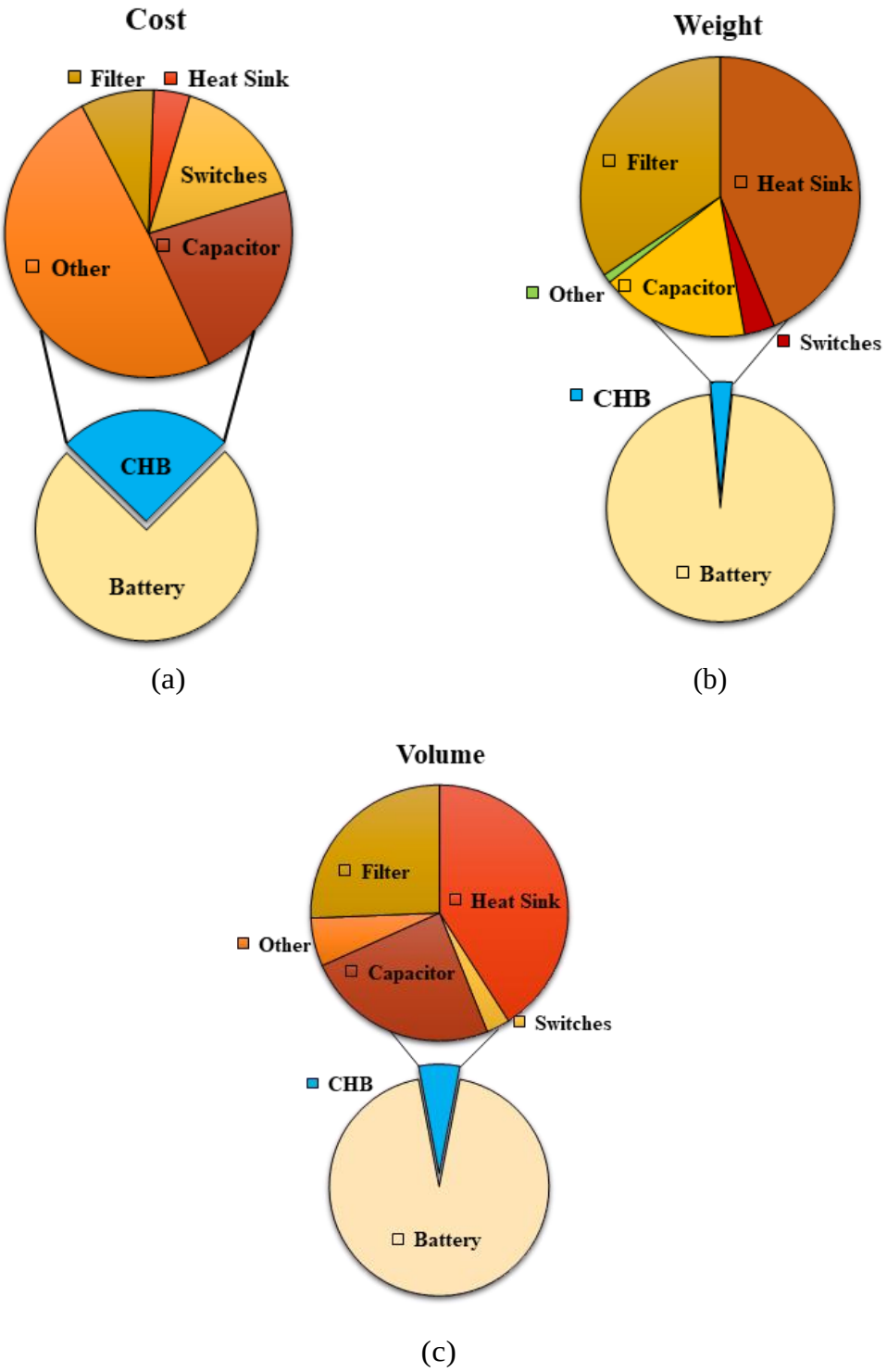


Figure 5.5 (a) Cost, (b) Weight, and (c) Volume for 4.16 kV/325 kW BESS CHB components.

Table 5.3 summarizes the isolation strategy for faults in different switching fault conditions. After completion of isolation, the modulation strategy is reconfigured for the other phases to guarantee voltage balancing.

This means when there is a fault on one switch in the X-CHB, the faulty X-CHB gets isolated, and two X-CHB cells from the healthy legs are updated to ensure voltage balancing. It is worth pointing out that the presented isolation technique is valid for motor drives and STATCOM applications as well. However, the isolation and reconfiguration method for BESS is proposed in the next chapter.

5.5 Comparison with other Topologies

As pointed out previously, each X-CHB inverter can operate as a 5-level or 7-level inverter depending on the modulation strategy. In order to evaluate the proposed X-CHB inverter, two separate comparisons are conducted. One comparison is made between the X-CHB operating at 5 levels and other 5-level topologies while the other comparison is between the 7-level X-CHB and 7-level topologies available in the literature.

5.5.1 5-L Boost X-CHB

To better clarify the features of the proposed 5-L Boost X-CHB topology, a comparison is made between the proposed topology and other MLIs. This is meant to evaluate the proposed topology versus other MLIs in terms of the number of power switches, number of diodes, number of capacitors, number of dc sources, and voltage boosting gain, as summarized in Table 5.4. The parameters given for components in Table 5.4 are just for one phase.

The common 5-level topologies being NPC, FC, and conventional CHB, along with 14 other topologies presented in the literature are compared with the proposed X-CHB while being operated at 5-levels.

Table 5.4 Comparison of 5-Level Topologies with the Proposed Topology

Topology	Switches	Drives	Diodes	Capacitors	Sources	Boosting
NPC	8	8	6	4	1	V_{dc}
FC	8	8	-	5	1	V_{dc}
CHB	8	8	-	2	2	V_{dc}
[5.1]	12	12	-	4	1	$4V_{dc}$
[5.2]	8	7	4	0	2	V_{dc}
[5.3]	8	8	-	0	2	V_{dc}
[5.4]	8	8	2	1	1	V_{dc}
[5.5]	7	7	8	3	1	$1/2V_{dc}$
[5.6]	6	6	7	2	2	V_{dc}
[5.7]	8	6	8	4	2	V_{dc}
[5.8]	16	16	-	-	1	V_{dc}
[5.9]	12	12	-	7	1	$1/2V_{dc}$
[5.10]	8	8	-	3	1	$1/2V_{dc}$
[5.11]	6	6	-	3	1	V_{dc}
[5.12]	5		6	4C/2L	1	
[5.13]	10	10	0	4	1	$1/2V_{dc}$
[5.14]	7	7	4	2	1	$2V_{dc}$
Proposed	8	8	-	1	1	$2V_{dc}$

The conventional CHB and topologies presented in [5.3], [5.4], [5.7], and [5.8] require two dc-power supplies to generate a 5-level voltage output. However, the proposed topology requires only one dc source. In addition, these topologies have no boosting ability as opposed to the proposed topology. In [5.2], the output voltage can be boosted by 4x; however, it requires four capacitors and 12 switches, which results in additional costs and a larger volume. The inverters in [5.11] and [5.6] have either an equal or fewer number of switches compared to the proposed topology, but they lack boosting ability and their output voltage is $0.5V_{dc}$. Other topologies in [5.12] and [5.13] are implemented with 6 and 5 semiconductor devices, respectively, which is

lower than the proposed topology. However, they require more passive components. Four capacitors and two inductors are required for the inverter presented in [5.13] and three capacitors are required in [5.12].

Table 5.5 Comparison of 7-Level Topologies with the Proposed Topology

MLI Topology	Switch	Capacitor	Source	Boosting	Max. Stress
NPC	18	6	1	V_{dc}	$1/2V_{dc}$
FC	12	7	1	V_{dc}	$1/2V_{dc}$
CHB	12	3	2	V_{dc}	$1/2V_{dc}$
[5.15]	8	4	1	V_{dc}	$1/2V_{dc}$
[5.16]	10	4	1	$1/2V_{dc}$	$1/2V_{dc}$
[5.17]	12	6	1	V_{dc}	$1/3V_{dc}$
[5.18]	12	4	1	$1/2V_{dc}$	$1/3V_{dc}$
[5.19]	14	5	1	V_{dc}	$1/3V_{dc}$
[5.20]	18	7	1	$1/2V_{dc}$	$1/2V_{dc}$
[5.21]	10	3	1	$0.75V_{dc}$	$1/2V_{dc}$
[5.22]	8	3	1	$0.75V_{dc}$	V_{dc}
[5.23]	10	4	1	$1.5V_{dc}$	V_{dc}
[5.24]	10	0	3	$3V_{dc}$	V_{dc}
[5.25]	16	2	1	$3V_{dc}$	V_{dc}
[5.26]	10	4	1	$1.5V_{dc}$	$2V_{dc}$
[5.27]	16	2	1	$2V_{dc}$	V_{dc}
Proposed	8	1	1	$1.5V_{dc}$	V_{dc}

5.5.2 7-L Boost X-CHB

A comparison of the conventional and recent 7-level inverters with the presented X-CHB in 7-level operation mode is summarized in Table 5.5. The proposed topology is compared with other topologies in terms of the number of power switches, number of diodes, number of capacitors, number of dc-sources, and voltage boosting gain. The comparison is conducted between a single phase of the aforementioned topologies.

5.6 Flying Capacitor Design

The modulation strategy can ensure capacitor voltage self-balancing for the proposed topology, which keeps the flying capacitor voltage balanced as shown in Figures 5.6 and 5.7. The modulation strategy plays an important role in flying capacitor design. Moreover, the number of voltage levels is also a key to designing the flying capacitor for the proposed topology.

5.6.1 5-Level Inverter

The proposed 5-level inverter can generate $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, and $-2V_{dc}$ from the dc source as summarized in Table 5.1 and Figure 5.6. When the output voltage is switched between 0 and V_{dc}, states A and B are used to generate an output voltage of V_{dc} while state D to generate 0. Using these different redundant states (A and B) to generate V_{dc} enables the controller to regulate the voltage across the flying capacitor. When the flying capacitor voltage is lower than the input voltage (which is also used as a reference voltage to regulate the flying capacitor voltage V_{CF}), state A is selected since this state provides a charging mode for the flying capacitor. Similarly, the switching states A and C are selected to produce $-2V_{dc}$ and $-3V_{dc}$, which ensure self-balancing for the flying capacitor. That is, state C can generate $2V_{dc}$, but the flying capacitor is always being discharged; however, state A provides a charging mode for the flying capacitor.

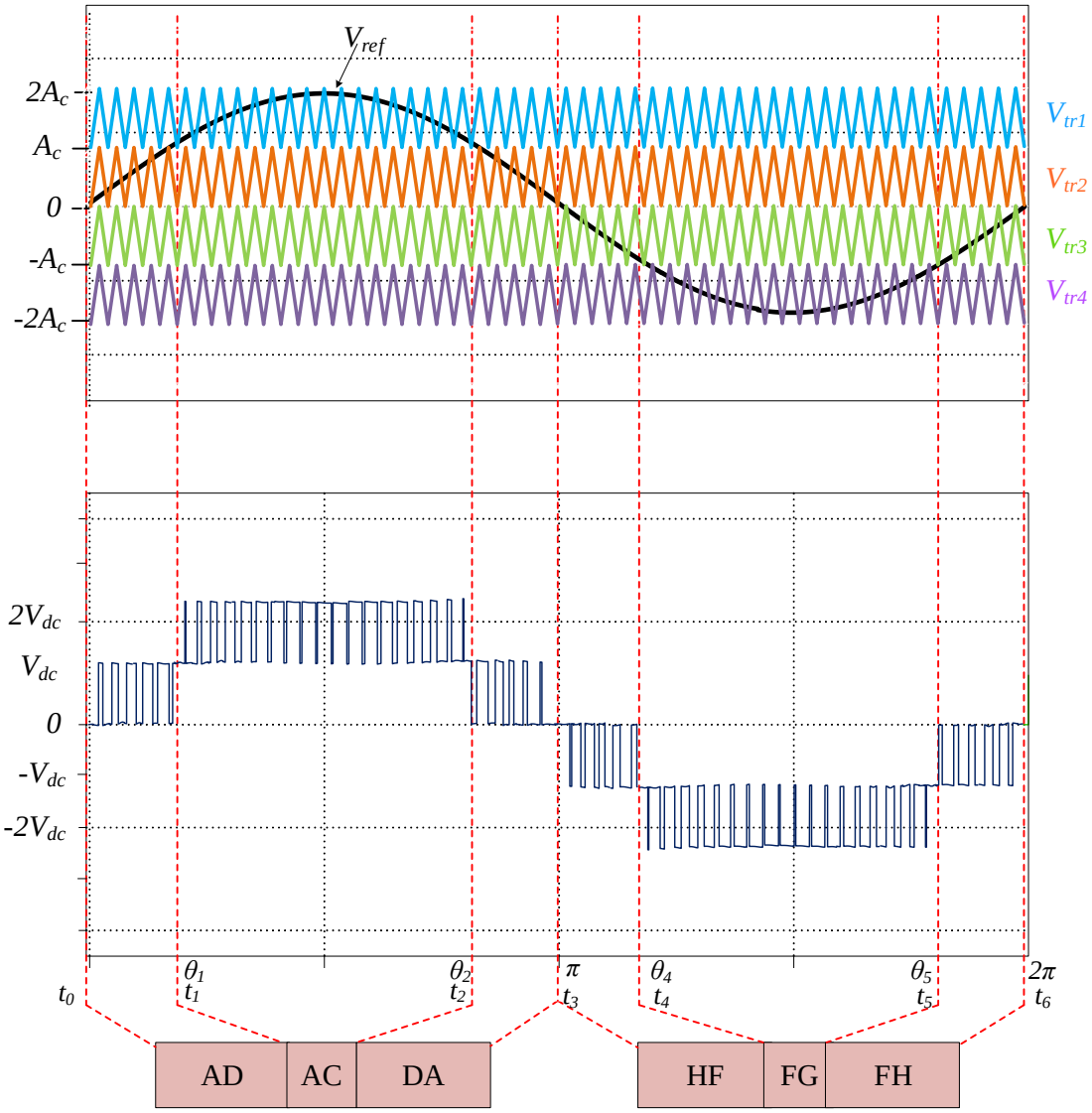


Figure 5.6 Modulation strategy of the proposed 5-level X-CHB inverter.

For the proposed 5-level inverter under reactive power conditions, the flying capacitor can be regulated due to the availability of the redundant states. As mentioned previously, the redundant states A, and B are used to generate V_{dc}. The flying capacitor can be charged and discharged through states A, and B, respectively. However, this assumption will be the opposite when the inverter operates under non-unity power factor conditions. That is, the phase current polarity on

the flying capacitor is flowing in the opposite direction. Consequently, the flying capacitor is charged and discharged during states B and A, respectively, as summarized in Table 5.1.

To summarize, when the flying capacitor voltage is lower than the input voltage, state B is selected since this state provides a charging mode for the flying capacitor under reactive power operation. This assumption is employed for the proposed inverter when it generates five voltage levels. However, it cannot be used when the inverter operates as a 7-level inverter. For that reason, the flying capacitor design consideration is achieved for 7-level inverter as it is described in the next section.

5.6.2 7-Level Inverter

Since the flying capacitor provides the required energy to the load, the capacitor design is an important factor in a high efficiency system. That is, the ripple voltage of the capacitor should be kept to a tolerable limit. The worst case of the capacitor ripple voltage occurs during the maximum discharge time of the flying capacitor.

As shown in Table 5.2 and Figure 5.7, the flying capacitor of the proposed topology when it operates as a 7-level inverter has the maximum discharging period (t_2 and t_3) during the positive half cycle. The output voltage during this period is changing from V_{dc} to 3/2V_{dc}. To generate V_{dc}, and 3/2V_{dc}, states C and D are used, respectively, as shown in Table 5.2. Similarly, during the negative cycle, the largest discharged gap occurs when the output voltage of the inverter is changing from -V_{dc} and -3/2V_{dc} (t_7 and t_8). The switching states H and I are selected to produce -V_{dc} and -3/2V_{dc}.

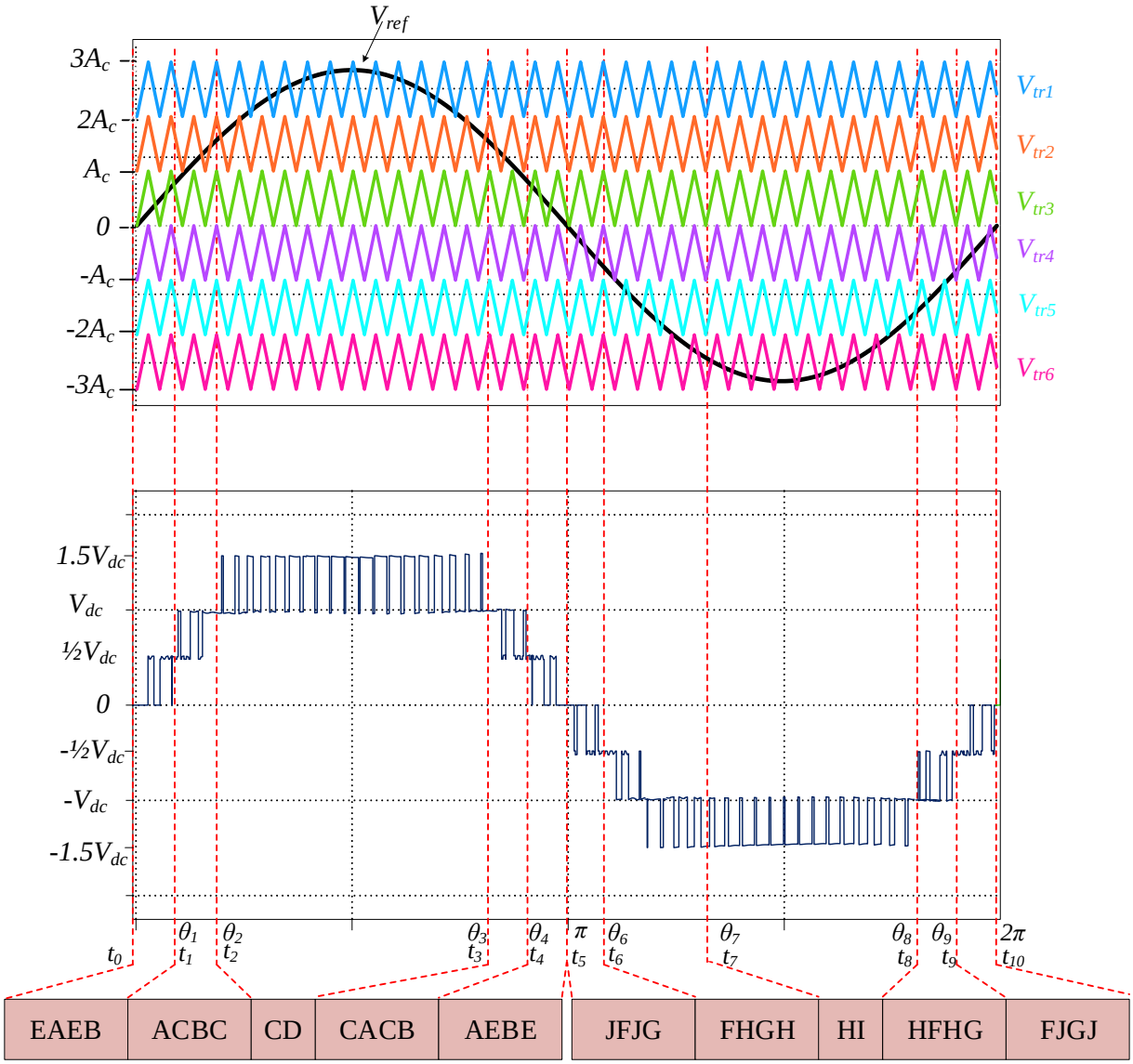


Figure 5.7 Modulation strategy of the proposed 7-level X-CHB inverter.

From Figure 5.7, the modulation index (M) is defined as

$$M = \frac{V_{ref,max}}{3A_c} \tag{5-3}$$

where $V_{ref,max}$ is the maximum amplitude value of the reference waveform, and A_c is the amplitude of the carrier waveform. The maximum amplitude value of the reference can be expressed as

$$V_{ref,max} = 3A_c \sin(2\pi f_{ref} t) \tag{5-4}$$

where f_{ref} is the frequency of the reference waveform. As is shown in Figure 5.7, time t_1, t_2 and t_3 are calculated by

$$t_1 = \frac{sin^{-1}(1/3)}{2\pi f_{ref}} \tag{5-5}$$

$$t_2 = \frac{sin^{-1}(2/3)}{2\pi f_{ref}} \tag{5-6}$$

$$t_3 = \frac{\pi - sin^{-1}(2/3)}{2\pi f_{ref}} \tag{5-7}$$

The maximum discharging value of the flying capacitor is obtained by [5.28]-[5.30]

$$\Delta Q = \int_{t_2}^{t_3} \frac{i_{Load}}{w} dwt \tag{5-8}$$

where i_{Load} is the load current. From Eq. (5-8), the maximum discharge amount, which causes maximum voltage ripple, occurs under a purely resistive load. Therefore, ΔQ can be calculated by

$$\Delta Q = \frac{V_{dc}}{2\pi f_o R}(t_3 - t_2) \tag{5-9}$$

where $f_o$is the output voltage frequency, and *R* is the load resistance. The value of the ripple voltage on the flying capacitor can be expressed as

$$\Delta V_{ripple} = \frac{\Delta Q}{C_F} = \frac{V_{dc}}{2\pi f_o R C_F}(t_3 - t_2) \tag{5-10}$$

Considering ΔV_{ripple} as the maximum allowable value of voltage ripple, the minimum value of the flying capacitor can be calculated as

$$C_{min} = \frac{\Delta Q}{\Delta V_{ripple}} = \frac{V_{dc}}{2\pi f_o R \Delta V_{ripple}}(t_3 - t_2) \tag{5-11}$$

5.7 Simulation Results

To verify the concept of the proposed X-CHB inverter, a detailed MATLAB/Simulink® model for a circuit similar to Figure 5.2 was modeled for both 5-level and 7-level inverter. The parameters and component values of the simulation and experiments are presented in Table 5.6. Figure 5.8

shows the waveforms of the output voltage before and after the filter, line current, and voltage across the flying capacitor for the proposed hybrid 5-level X-CHB inverter under unity power factor. The inverter's capability of operation in lagging and leading power factor has been successfully tested. Figures 5.9 and 5.10 show the proposed 5-level X-CHB inverter operation in lagging and leading power factor, respectively. The presented topology does not require any special consideration or technique for operation with linear/nonlinear loads.

Table 5.6 Simulation Parameters

Description	Value
Number of cells	3
Input voltage (Vdc)	400 V
Line frequency	60 Hz
Filter inductor,	0.16 mH
Filter Capacitor	50 μF
Carrier frequency	15 kHz
Load (inductive)	30 Ω, 10 mH

The proposed 7-level X-CHB has been simulated. Figure 5.11 shows the output voltage before and after the filter, line current, and voltage across the flying capacitor waveforms under unity-power factor. Also, the 7-level X-CHB has been tested under non-unity power factors, as displayed in Figures 5.12 and 5.13. As can be observed, the voltage and current are both purely sinusoidal in each case.

Using the parameters listed in Table 5.6, the efficiency and losses versus the power for the proposed topology are calculated as shown in Figure 5.14. The conduction and switching losses for the semiconductor devices were used for loss and efficiency calculations. Using the devices' datasheet specification, the losses and their effects were calculated using MATLAB/Simulink. While the loss-power diagram is constantly increasing, the efficiency diagram is increasing up to

an optimum point and then begins to decrease. It is clear that the maximum efficiency for the proposed topology is around 98%, which is achieved between a load of approximately 1 kW to 2.5 kW.

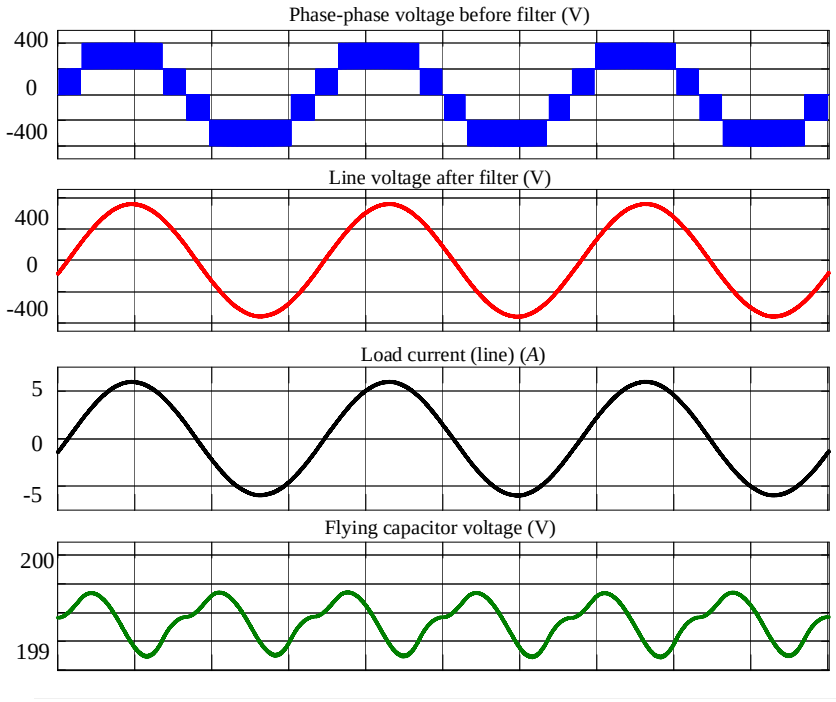


Figure 5.8 Operation of the proposed 5-level inverter under unity power factor.

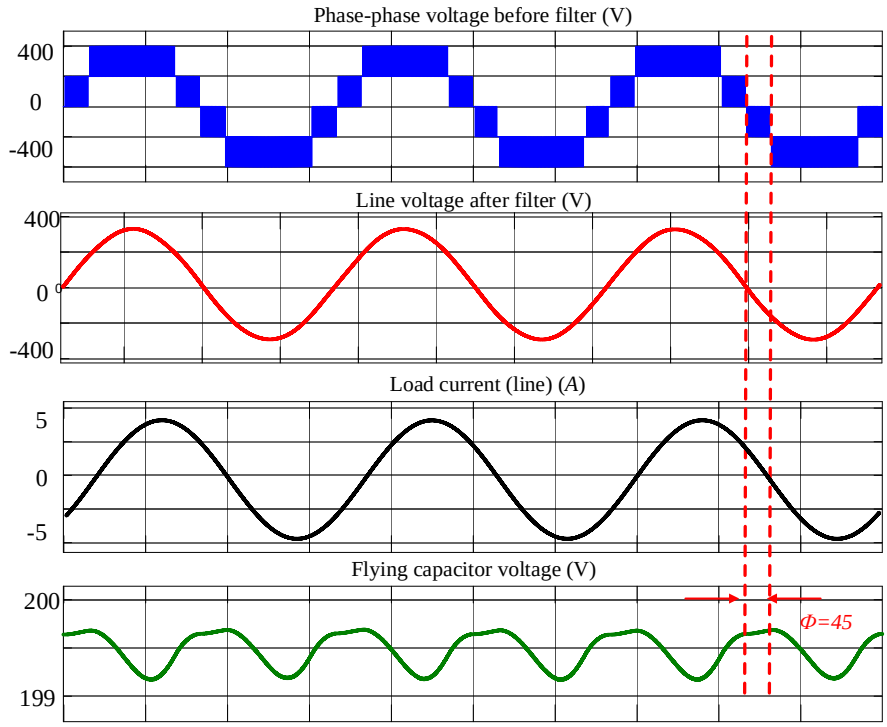


Figure 5.9 Operation of the proposed 5-level inverter under lagging power factor.

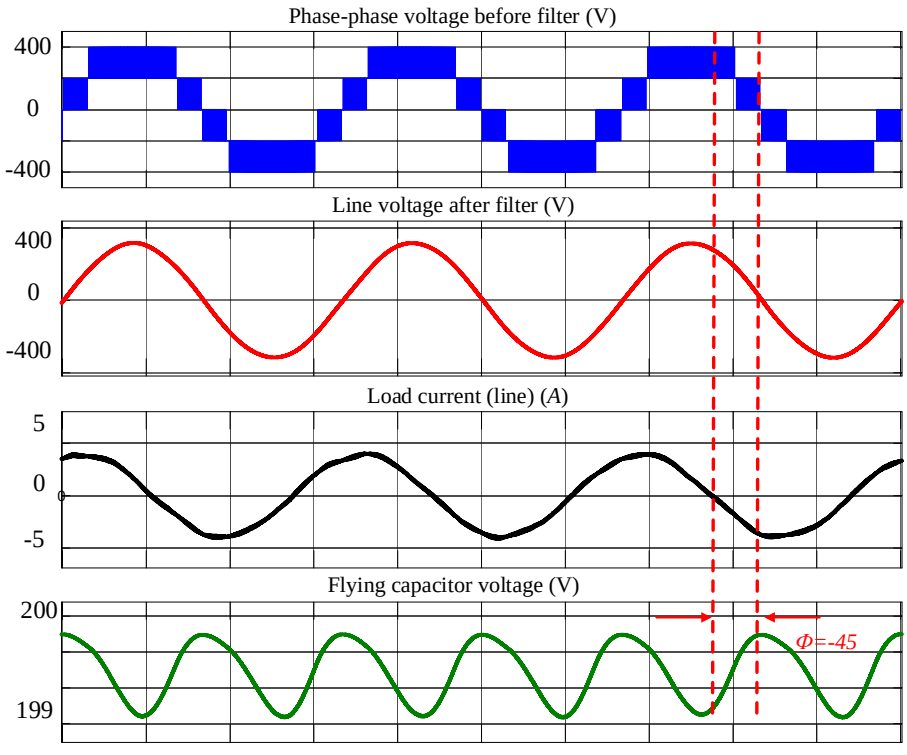


Figure 5.10 Operation of the proposed 5-level under leading power factor.

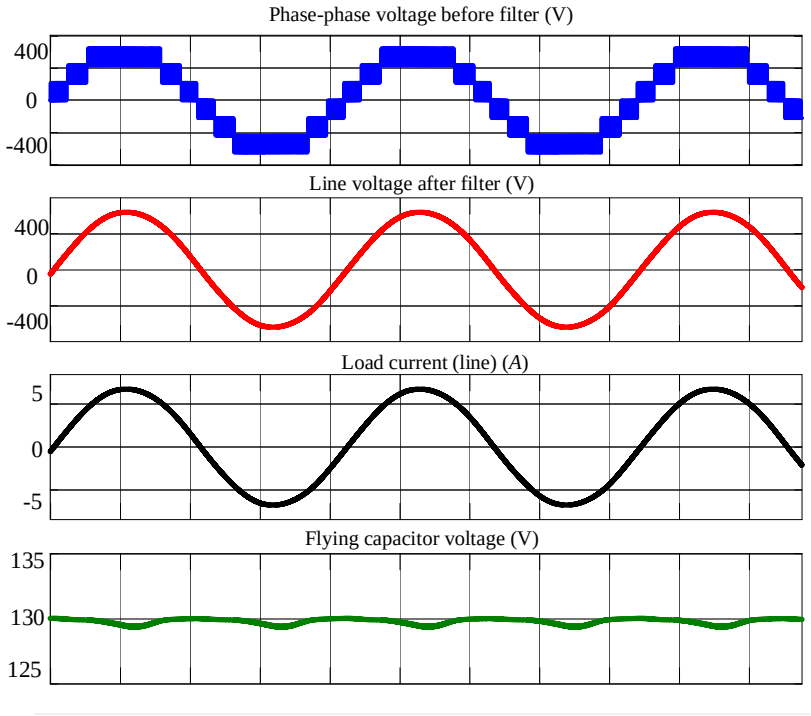


Figure 5.11 Operation of the proposed 7-level inverter under unity power factor.

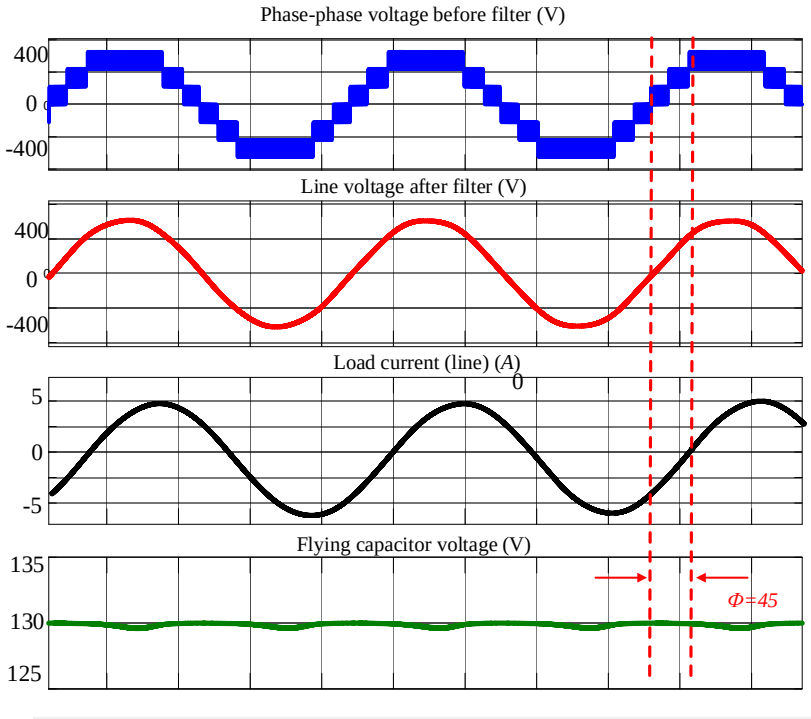


Figure 5.12 Operation of the proposed 7-level inverter under lagging power factor.

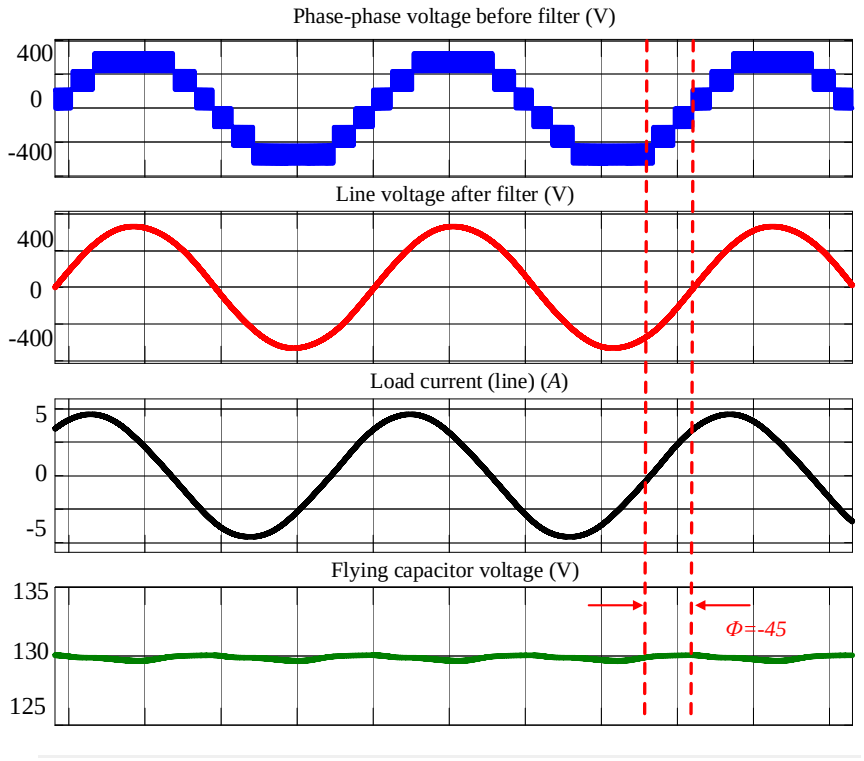


Figure 5.13 Operation of the proposed 7-level inverter under leading power factor.

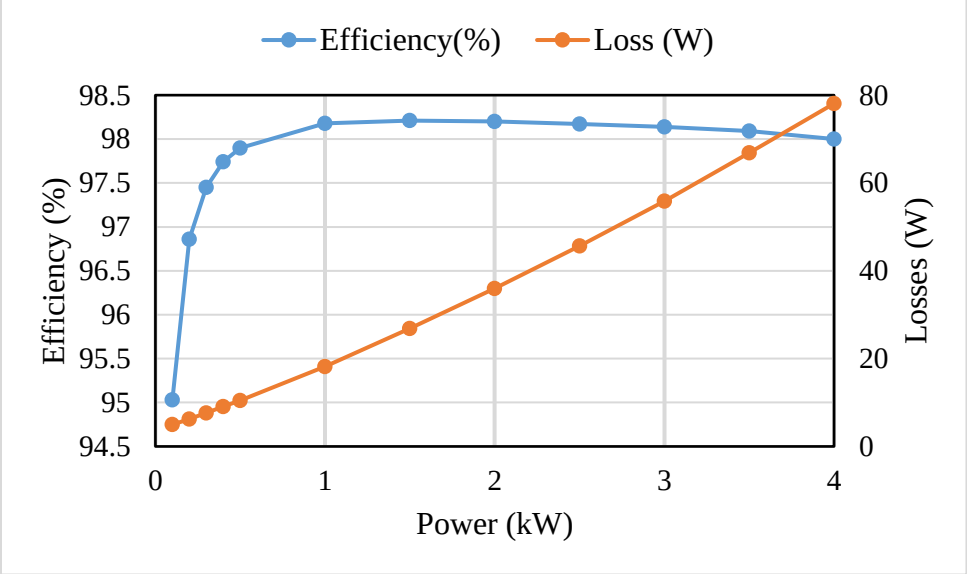


Figure 5.14 Total losses and efficiency of the proposed topology versus output voltage.

The semiconductor devices' loss distribution is illustrated in Figure 5.15. As can be observed, S_3 and S_6 have the lowest losses as they have the lowest conduction times amongst all of the switches. Figure 5.16 displays the total losses in one leg of the proposed topology vs. power. As expected, the switching and conduction losses are in direct relationship with the power.

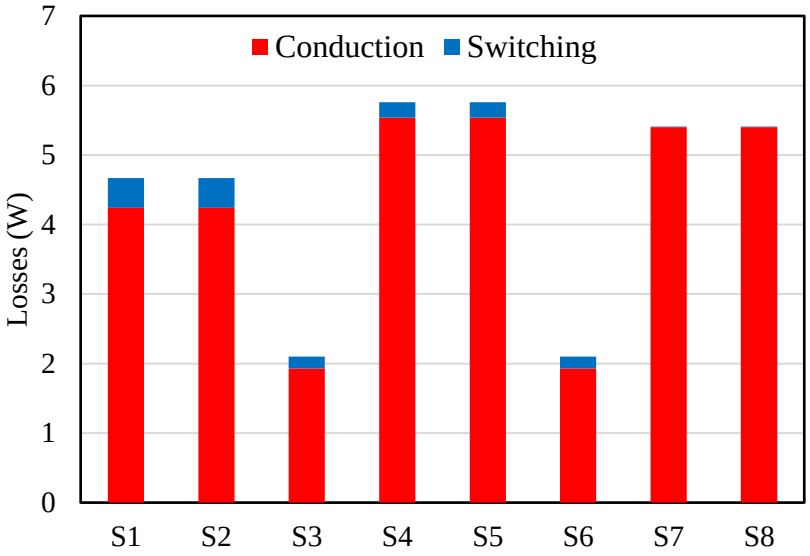


Figure 5.15 Distribution of semiconductor losses of the proposed X-CHB.

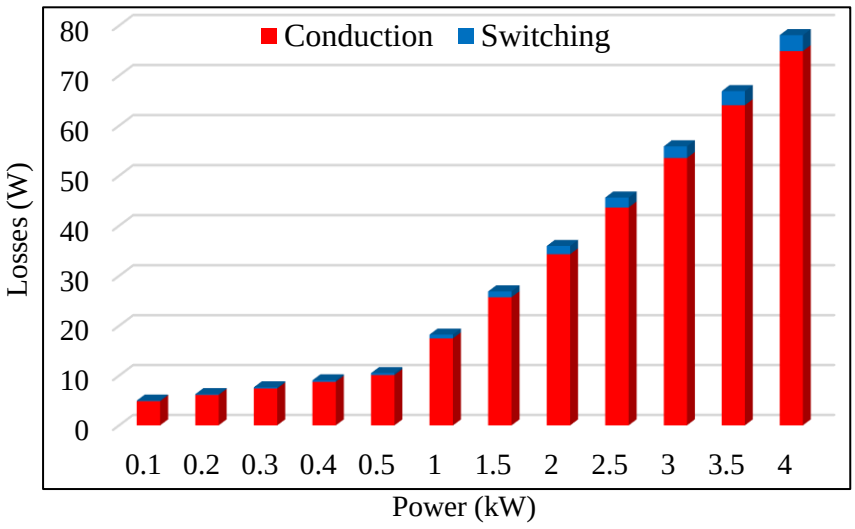


Figure 5.16 Total power losses variations versus output power.

5.8 References

[5.1] M. Saeedian, S. M. Hosseini and J. Adabi, "A Five-Level Step-Up Module for Multilevel Inverters: Topology, Modulation Strategy, and Implementation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 4, pp. 2215-2226, Dec. 2018.

[5.2] L. He and C. Cheng, "A Flying-Capacitor-Clamped Five-Level Inverter Based on Bridge Modular Switched-Capacitor Topology," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 12, pp. 7814-7822, Dec. 2016.

[5.3] M. R. A and K. Sivakumar, "A Fault-Tolerant Single-Phase Five-Level Inverter for Grid-Independent PV Systems," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7569-7577, Dec. 2015.

[5.4] D. A. Ruiz-Caballero, R. M. Ramos-Astudillo, S. A. Mussa and M. L. Heldwein, "Symmetrical Hybrid Multilevel DC–AC Converters With Reduced Number of Insulated DC Supplies," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2307-2314, July 2010. [30]

[5.5] S. P. Gautam, L. Kumar, S. Gupta and N. Agrawal, "A Single-Phase Five-Level Inverter Topology With Switch Fault-Tolerance Capabilities," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 2004-2014, March 2017.

[5.6] H. Wang, L. Kou, Y. Liu and P. C. Sen, "A Seven-Switch Five-Level Active-Neutral-Point-Clamped Converter and Its Optimal Modulation Strategy," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5146-5161, July 2017. [29]

[5.7] R. Samanbakhsh and A. Taheri, "Reduction of Power Electronic Components in Multilevel Converters Using New Switched Capacitor-Diode Structure," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7204-7214, Nov. 2016.

[5.8] R. Barzegarkhoo, E. Zamiri, N. Vosoughi, H. M. Kojabadi and L. Chang, "Cascaded multilevel inverter using series connection of novel capacitor-based units with minimum switch count," *IET Power Electronics*, vol. 9, no. 10, pp. 2060-2075, 17 8 2016.

[5.9] B. Satish Naik, L. Umanand, K. Gopakumar and B. Subba Reddy, "A New Two-Phase Five-Level Converter for Three-Phase Isolated Grid-Tied Systems With Inherent Capacitor Balancing and Reduced Component Count," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 3, pp. 1325-1335, Sept. 2018.

[5.10] E. Burguete, J. López and M. Zabaleta, "A New Five-Level Active Neutral-Point-Clamped Converter With Reduced Overvoltages," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7175-7183, Nov. 2016.

[5.11] S. A. Gonzalez, M. I. Valla and C. F. Christiansen, "Five-level cascade asymmetric multilevel converter," *IET Power Electronics*, vol. 3, no. 1, pp. 120-128, January 2010.

[5.12] Y. P. Siwakoti, "A new six-switch five-level boost-active neutral point clamped (5L-Boost-ANPC) inverter," *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 2424-2430.

[5.13] H. Luong, M. Nguyen and T. Tran, "Single-phase five-levelZ-source T-type inverter," *IET Power Electronics*, vol. 11, no. 14, pp. 2367-2376, 27 11 2018.

[5.14] S. Xu, J. Zhang, X. Hu and Y. Jiang, "A Novel Hybrid Five-Level Voltage-Source Converter Based on T-Type Topology for High-Efficiency Applications," *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4730-4743, Sept.-Oct. 2017.

[5.15] Y. Siwakoti, A. Mahajan, D. Rogers and F. Blaabjerg, "A Novel Seven-Level Active Neutral Point Clamped Converter with Reduced Active Switching Devices and DC-link Voltage," *IEEE Transactions on Power Electronics*.

[5.16] X. Yuan, "Derivation of Voltage Source Multilevel Converter Topologies," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 2, pp. 966-976, Feb. 2017.

[5.17] Fang Zheng Peng, "A generalized multilevel inverter topology with self-voltage balancing," *IEEE Transactions on Industry Applications*, vol. 37, no. 2, pp. 611-618, March-April 2001.

[5.18] W. Sheng and Q. Ge, "A Novel Seven-Level ANPC Converter Topology and Its Commutating Strategies," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7496-7509, Sept. 2018.

[5.19] H. Tian, Y. Li and Y. W. Li, "A Novel Seven-Level Hybrid-Clamped (HC) Topology for Medium-Voltage Motor Drives," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5543-5547, July 2018.

[5.20] M. Saeedifard, P. M. Barbosa and P. K. Steimer, "Operation and Control of a Hybrid Seven-Level Converter," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 652-660, Feb. 2012.

[5.21] S. R. Pulikanti, G. Konstantinou and V. G. Agelidis, "Hybrid Seven-Level Cascaded Active Neutral-Point-Clamped-Based Multilevel Converter Under SHE-PWM," in *IEEE Transactions on Industrial Electronics*, vol. 60, no. 11, pp. 4794-4804, Nov. 2013. [14] [22] H. Yu, B. Chen, W. Yao and Z. Lu, "Hybrid Seven-Level Converter Based on T-Type Converter and H-Bridge Cascaded Under SPWM and SVM," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 689-702, Jan. 2018.

[5.23] S. S. Lee, Y. Bak, S. Kim, A. Joseph and K. Lee, "New Family of Boost Switched-Capacitor 7-Level Inverters (BSC7LI)," *IEEE Transactions on Power Electronics*.

[5.24] S. S. Lee, M. Sidorov, N. R. N. Idris and Y. E. Heng, "A Symmetrical Cascaded Compact-Module Multilevel Inverter (CCM-MLI) With Pulsewidth Modulation," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4631-4639, June 2018.

[5.25] S. S. Lee, "A Single-Phase Single-Source 7-Level Inverter With Triple Voltage Boosting Gain," *IEEE Access*, vol. 6, pp. 30005-30011, 2018.

[5.26] S. S. Lee and K. Lee, "Dual-T-Type Seven-Level Boost Active-Neutral-Point-Clamped Inverter," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6031-6035, July 2019.

[5.27] X. Sun, B. Wang, Y. Zhou, W. Wang, H. Du and Z. Lu, "A Single DC Source Cascaded Seven-Level Inverter Integrating Switched-Capacitor Techniques," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7184-7194, Nov. 2016.

[5.28] M. Saeedian, S. M. Hosseini and J. Adabi, "A Five-Level Step-Up Module for Multilevel Inverters: Topology, Modulation Strategy, and Implementation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 4, pp. 2215-2226, Dec. 2018.

[5.29] J. Liu, J. Wu, J. Zeng and H. Guo, "A Novel Nine-Level Inverter Employing One Voltage Source and Reduced Components as High-Frequency AC Power Source," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2939-2947, April 2017.

[5.30] Y. Zhang, G. P. Adam, T. C. Lim, S. J. Finney and B. W. Williams, "Hybrid Multilevel Converter: Capacitor Voltage Balancing Limits and its Extension," in *IEEE Transactions on Industrial Informatics*, vol. 9, no. 4, pp. 2063-2073, Nov. 2013.

CHAPTER 6

A FAULT-TOLERANT HYBRID CASCADED H-BRIDGE MULTILEVEL INVERTER FOR A BATTERY ENERGY STORAGE SYSTEM

6.1 Introduction and Motivation

Multilevel topologies are considered a promising technology for integrating renewable and clean energy resources, such as battery energy storage systems, solar photovoltaics and wind turbine generators, to the electric power grid. The reasons behind the rapid adoption of the multilevel converters are due to improved output power quality, scalable/modular configuration, and the possibility of implementing low voltage rated components. Several multilevel topologies have been published in the quest for making the system cost-effective, reliable and less complex in control from both the hardware and software perspectives. Among them, the major multilevel topologies are: modular multilevel converter (MMC), flying capacitor (FC), cascaded H-bridge (CHB), and neutral point clamped (NPC) inverters [6.1]-[6.5]. Even though there are several different types of multilevel topologies, they share the same issue of reliability due to the high probability of semiconductor device failures [6.6]-[6.9].

In other words, reliability is a major concern among conventional multilevel topologies due to the higher number of switches and their driving circuitry. Additionally, in cases of open/short-circuit faults, the multilevel output voltage becomes distorted, which results in the malfunction of the inverter that may propagate upstream to the grid and cause subsequently failures [6.10]-[6.12].

The degree of switch failure is also different depending on the circuit topology and application. For instance, in the case of open-circuit faults in CHB, one voltage level is skipped in that particular phase; however, the other two phases continue generating the same output voltage. In the case of a motor drive application, the system can survive for several periods, and a basic

controller can reduce the voltage of the healthy phases as well. Reducing the voltage level in a motor drive application does not damage the motor. However, in the case of a grid-tied multilevel inverter, losing one voltage level results in an unbalanced output voltage, which subsequently can shut down the overall system.

In summary, prior methods fall into one of two categories. The first is to detect and isolate a faulty cell. However, isolation of one cell results in reduced functionality and degraded operation as in [6.13]. The structures in [6.14]-[6.15] use a strategy which bypasses the faulty cell in the case of a fault occurring. This results in having to bypass a cell in each of the other two phases, which results in an inverter working with less voltage levels (losing two voltage levels). In other words, it ensures the output voltage of the inverter when a fault happens in one phase is the same as before the fault occurs but with less voltage levels. It is possible by boosting the voltage in each healthy H-bridge cell in the case of STATCOM applications. However, it is not practical in the case of BESS. The methods presented in [6.16]-[6.17] are also used to isolate the faulty switch and have the ability to compensate for the fault to keep the same output voltage. However, these methods are designed only for inverters that have boosting stages. There are several other methods proposed for fault-tolerant and reconfiguration when a switch fault occurs [6.18]-[6.27]. However, the fault-tolerant strategies presented for the dc-dc inverters [6.18]-[6.21], flying capacitor inverter [6.22], two-stages converter [6.23], T-type inverter [6.24], multi-phase inverter [6.25], and NPC [6.26]-[6.27], cannot be implemented with CHB inverter for BESS.

The structure presented [6.28] adds four switches to bypass the faulty cell. Two of these switches are normally open and two normally closed. The switches used in [6.28] are conductors (electromagnetic switches), which are slow to respond compared with semiconductor devices. Also, this method results in high conduction losses since two switches per H-bridge are always turned-on

in the normal operation, which produces more losses and heat. A method in [6.29] adds four switches to bypass the faulty cell and connects its batteries to the healthy cell. Adding batteries to another cell may damage switches because the input voltage gets doubled, which may exceed the breakdown voltage of the semiconductor. Secondly, in the case of BESS and photovoltaic systems, it should have a controller to balance the charging and discharging process. Adding a battery from a faulty cell to a healthy cell may affect the state of charge (SOC), which could result in controller malfunction.

The second solution involves installing a redundant backup system; however, that significantly increases the overall cost of the system. Redundancy can be achieved when a faulty cell is bypassed and isolated to compensate for the missing voltage level using backup systems (an extra H-bridge, or batteries). This method can keep the continuity of the inverter while producing the same output voltage level. However, using an additional dc source increases the price of the system and the control complexity [6.30], [6.31].

Considering the above aspect in the development of fault-tolerant and robust CHB systems, a novel hybrid CHB is proposed in this digest by adding a novel X-CHB inverter to provide smooth and reliable operation in the case of semiconductor device failure. The proposed X-CHB is a five-level inverter with a maximum voltage gain to 2. One flying capacitor is integrated into the proposed structure that provides voltage boosting ability while maintaining self-voltage balancing in the new system. Even though the application of the proposed topology has been demonstrated with CHB for BESS, it can also be integrated with any type of multilevel topology to achieve fault-tolerant capability.

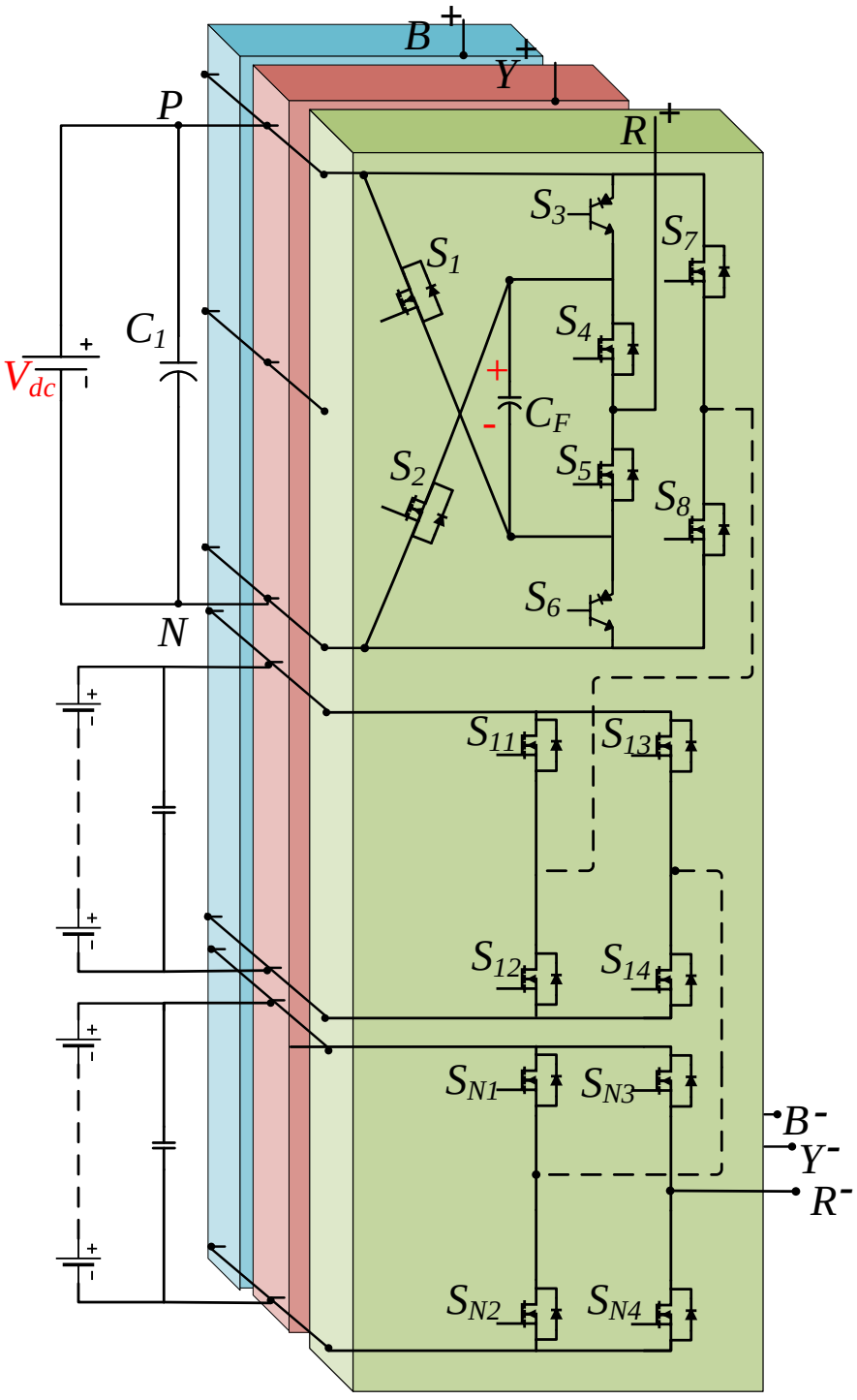


Figure 6.1 Proposed *n*-level three-phase hybrid CHB inverter.

6.2 Proposed Hybrid CHB

The proposed circuit is a combination of an X-CHB (upper cell) and an *n*-level CHB as shown in Figure 6.1, which produces five levels. It consists of eight switches; (S_3, S_6) which are bipolar voltage capability, and (S_1, S_2, S_3, S_5, S_7, and S_8) are standard semiconductor devices, such as either IGBTs or MOSFETs. It also requires an additional flying capacitor C_F to boost the voltage up to 2X. In every switching cycle, the flying capacitor charges to V_{dc} from its input dc supply through S_3 and S_6. The X-switches (S_1 and S_2) are employed to create the second voltage level by connecting the dc supply with the flying capacitor and also to boost the voltage up to 2X. Consequently, the output voltage levels are $2V_{dc}$, V_{dc}, 0, -V_{dc}, and -$2V_{dc}$.

In normal operating conditions, the X-CHB works as three-level inverter producing V_{dc}, 0, -V_{dc} from the dc source. However, during the fault condition such as open/short-circuit fault or battery fault, the system loses one voltage level. During that time, the X-CHB operates as a five-level boost inverter compensating for the missing voltage level. This ensures continuity of operation without any disturbance. Therefore, this topology brings a high degree of reliability to the overall system under different fault scenarios.

Overall, this chapter presents a novel power converter topology with improved features, such as: 1) continuity of operation in the case of a fault (open/short circuit switch fault); 2) full reactive power operation due to its capability of operation in any power factor (lagging/leading); 3) self-balancing for the flying capacitor of the proposed inverter; and 4) boosting the voltage level by factor of 2 without the need of an extra boost stage (inductorless voltage boost).

6.3 Operation Modes for the Proposed Hybrid CHB System

6.3.1 Introduction to the Proposed Topology

A 7-level hybrid cascaded H-Bridge for fault-tolerant operation is shown in Figure 6.2. It consists of the X-CHB (the upper highlighted cell) with two cascaded H-bridge cells. During regular operation, no fault, the inverter is producing seven voltage levels, where the X-CHB operates as an H-bridge inverter producing V_{dc}, 0, -V_{dc}. In other words, the inverter consists of three H-bridge cells and operates as the conventional 7-level CHB inverter.

For a normal 7-level CHB inverter, the output voltage of a single phase can be expressed as a function of the upper switches as

$$V_{leg} = (S_{11} - S_{13})V_{dc1} + (S_{21} - S_{23})V_{dc2} + (S_{31} - S_{33})V_{dc3} \tag{6-1}$$

Also, from Table 3.1 in Chapter 3, the leg voltage can be expressed as a function of the lower switches (S_{12} and S_{14}) as

$$V_{leg} = (S_{14} - S_{12})V_{dc1} + (S_{24} - S_{22})V_{dc2} + (S_{34} - S_{32})V_{dc3} \tag{6-2}$$

In addition to Eqs. (6-1) and (6-2), the leg voltage of a single phase inverter can be expressed as a function of the all the switches as

$$V_{leg} = \{(S_{11} - S_{13}) + (S_{14} - S_{12})\}\frac{V_{dc1}}{2} + \{(S_{21} - S_{23}) + (S_{24} - S_{22})\}\frac{V_{dc2}}{2} + \{(S_{n1} - S_{n3}) + (S_{n4} - S_{n2})\}\frac{V_{dc3}}{2} \tag{6-3}$$

Also, from Chapter 5, the output voltage of the 5-level X-CHB V_X can be expressed as

$$V_X = 2V_{dc}(S_1 - S_2) + V_{dc}(S_4S_6S_8 - S_3S_5S_7) \tag{6-4}$$

A 7-level hybrid cascaded H-bridge for fault-tolerant operation is shown in Fig. 6.2. It consists of the X-CHB (the upper highlighted cell) with two cascaded H-bridge cells. During regular operation with no fault present, the inverter is producing seven voltage levels, where the X-CHB

operates as an H-bridge inverter producing V_{dc}, 0, -V_{dc}. In other words, the inverter consists of three H-bridge cells and operates as the conventional 7-level CHB inverter. Therefore, in the normal operation, the output voltage of the 7-level hybrid CHB inverter can be expressed as

$$V_{leg} = (S_{11} - S_{13})V_{dc} + (S_{21} - S_{23})V_{dc} + (S_3S_4 - S_7)V_{dc} \quad (6\text{-}5)$$

where V_{dc} is the input voltage for each cell.

During a fault condition such as open/short-circuit fault or battery fault, the system loses one voltage level. During the fault time, the X-CHB operates as a five-level boost inverter producing $2V_{dc}$, V_{dc}, 0, -V_{dc}, and -$2V_{dc}$ voltage levels to compensate for the missing voltage level to ensure seven voltage levels at the output of the inverter. The output voltage the X-CHB in this case can be expressed as

$$V_{Xo} = 2V_{dc}(S_1 - S_2) + V_{dc}(S_4S_6S_8 - S_3S_5S_7) \quad (6\text{-}6)$$

The inverter is assumed to have a fault in the second H-bridge (H-bridge 2), and the faulty cell is bypassed by turning ON both of the lower switches, S_{22} and S_{24}, of the faulty cell (software bypassing). The output voltage of the inverter in this case is

$$V_{leg} = (S_{11} - S_{13})V_{dc} + 2V_{dc}(S_1 - S_2) + V_{dc}(S_4S_6S_8 - S_3S_5S_7) \quad (6\text{-}7)$$

6.3.2 Operation of the Proposed Topology

During a fault condition such as open/short-circuit fault or battery fault, the system loses one voltage level. To detect the faulty cell and the switch, a method similar to [6.32] can be adopted. Once the faulty cell/switch is detected, the faulty H-bridge should be bypassed by turning ON its upper or lower switches.

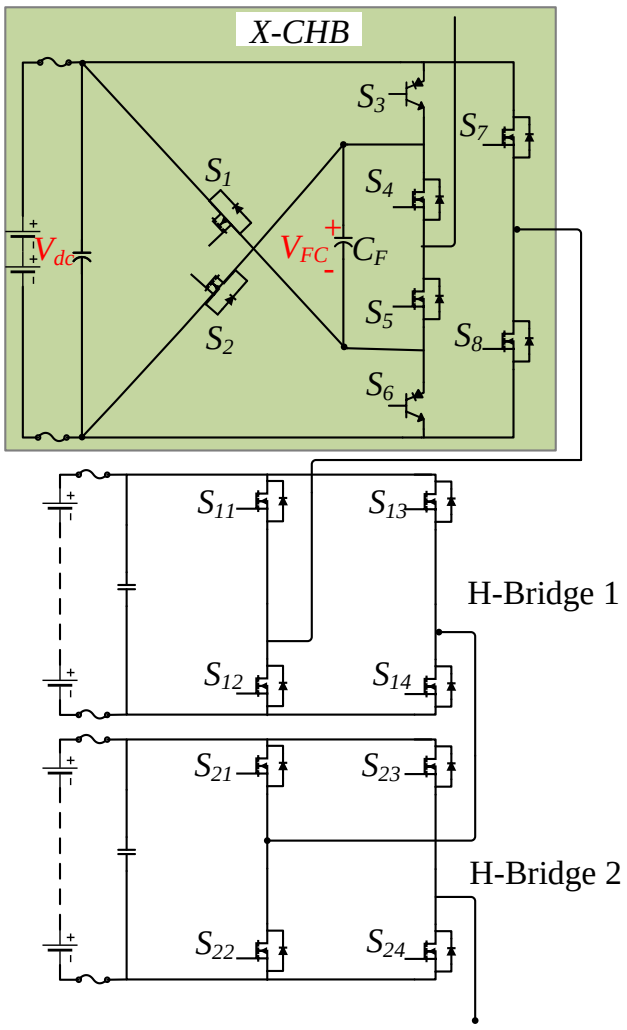


Figure 6.2 A 7-level single-phase hybrid CHB inverter.

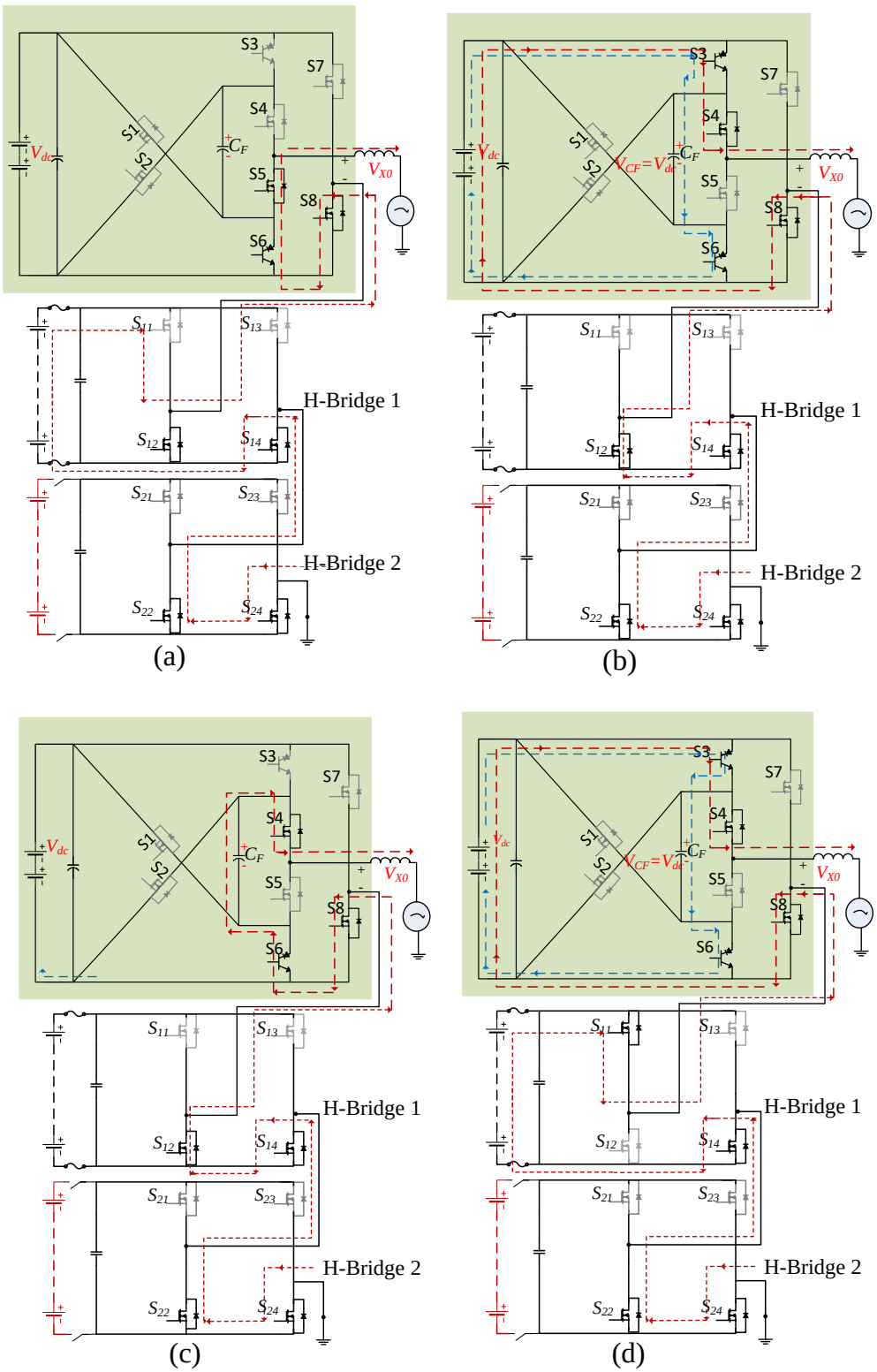


Figure 6.3 Switching states analysis for a positive cycle of the hybrid CHB.

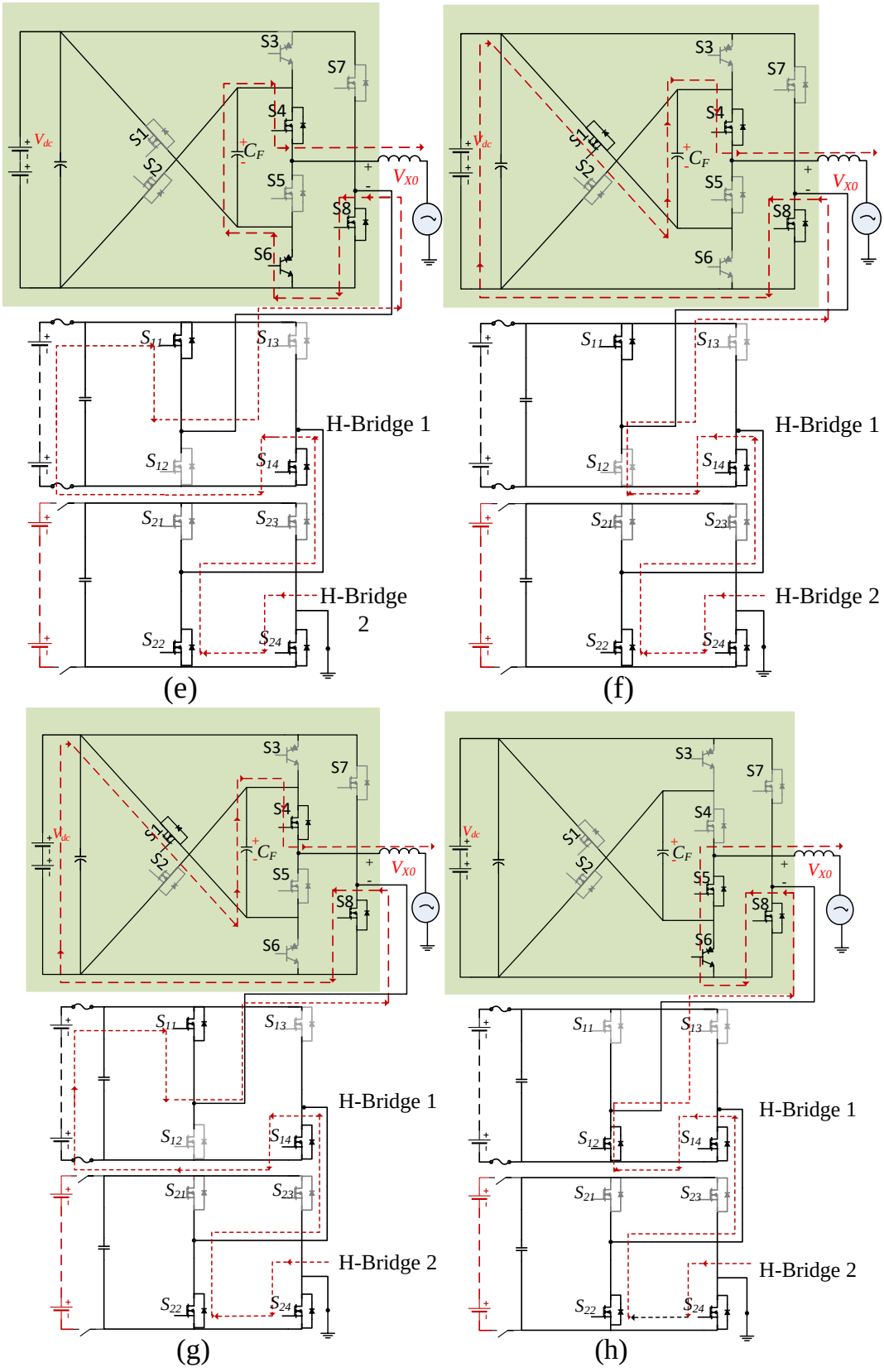


Figure 6.3 Switching states analysis for a positive cycle of the hybrid CHB (Cont.).

During the fault time, the X-CHB operates as a five-level boost inverter producing $2V_{dc}$, V_{dc}, 0, -V_{dc}, and -$2V_{dc}$ voltage levels to compensate for the missing voltage level to ensure seven voltage levels at the output of the inverter.

The operational analysis adopted sixteen different switching modes (state A to P). Table 6.1 lists all possible switching states with its corresponding output voltage for the proposed hybrid CHB inverter. The operation and analysis of the proposed hybrid cascaded H-Bridge during the half-cycle (states A to H) is illustrated in Figure 6.3. The inverter is assumed to have a fault in the second H-bridge (H-bridge 2) and the faulty cell is bypassed by turning ON both of the lower switches, S_{22} and S_{24}, of the faulty cell (software bypassing).

Table 6.1 Switching States of the Hybrid CHB Inverter Under Fault

Switching States	V_X	**Active Switching States**												**Flying Capacitor**
		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_{11}	S_{12}	S_{13}	S_{14}	
A	$+V_{dc}$	0	0	0	0	1	1	0	1	1	0	0	1	—
B		0	0	1	1	0	1	0	1	1	1	0	0	↑
C		0	0	0	1	0	1	0	1	0	1	0	1	↓
D	$+2V_{dc}$	0	0	1	1	0	1	0	1	1	0	0	1	↑
E		0	0	0	1	0	1	0	1	1	0	0	1	↓
F		1	0	0	1	0	0	0	1	1	1	0	0	↓
G	$+3V_{dc}$	1	0	0	1	0	0	0	1	1	0	0	1	↓
H	0	0	0	0	0	1	1	0	1	0	1	0	0	—
I	$-V_{dc}$	0	0	1	1	0	0	1	0	0	1	1	0	—
J		0	0	1	0	1	1	1	0	1	0	1	0	↑
K		0	0	1	0	1	0	1	0	1	0	1	0	↓
L	$-2V_{dc}$	0	0	1	0	1	1	1	0	0	1	1	0	↑
M		0	0	1	0	1	0	1	0	1	0	1	0	↓
N		0	1	0	0	1	0	1	0	0	1	1	0	↓
O	$-3V_{dc}$	0	1	0	0	1	0	1	0	0	1	1	0	↓
P	0	0	0	1	1	0	0	1	0	1	0	1	0	↑

Note: "—" means no effect, "↑" means charging, "↓" means discharging

The red dotted line in Figure 6.3 represents the current path and the blue indicates the capacitor charging current path. The output voltage of the hybrid CHB and the inverter are defined as V_X and V_{XO}, respectively.

The flying capacitor (C_F) is clamped to the dc power supply through switches S_3 and S_6 as shown in Figures 6.3(b), and (d), where the flying capacitor voltage (V_{CF}) is equal to the input voltage V_{dc}. To compensate for the voltage level during the fault, the voltage across C_F gets discharged, and the output voltage of the hybrid CHB V_X is equal to $2V_{dc}$, as shown in Figure 6.3 (g). By discharging C_F during the positive cycle in series with the input voltage (when S_1, S_4 and S_8 are ON), the output voltage of the X-CHB is $2V_{dc}$ ($V_X = 2V_{dc}$) as shown in Figure 6.3(g). Similarly, during the negative cycle, X-CHB can generate $-2V_{dc}$ by discharging the flying capacitor and connecting it in series with input voltage through S_2, S_5 and S_7.

Thus, the proposed hybrid CHB has the ability to boost the voltage up to 2X, and increase the voltage levels by using only eight additional switches and one capacitor in the X-CHB without the need of an inductor. These features make the X-CHB applicable to any type of multilevel inverter to achieve fault-tolerant operation.

6.4 Modulation Strategy

6.4.1 Unity Power Factor Operation

The modulation strategy of the converter in the unity-power factor condition is shown in Figure 6.4. Phase disposition level-shifted PWM is used because it provides lower total harmonic distortion (THD) and simplicity of implementation. Six triangular carrier signals and one sinusoidal reference signal are used to generate the 7-voltage levels of the proposed hybrid CHB. The carrier signals are compared with the reference signal to generate the proper PWM signals

resulting in 7-level inverter. In order to analyze the modulation strategy, one output voltage cycle can be divided into six-time intervals as shown in Figure 6.4.

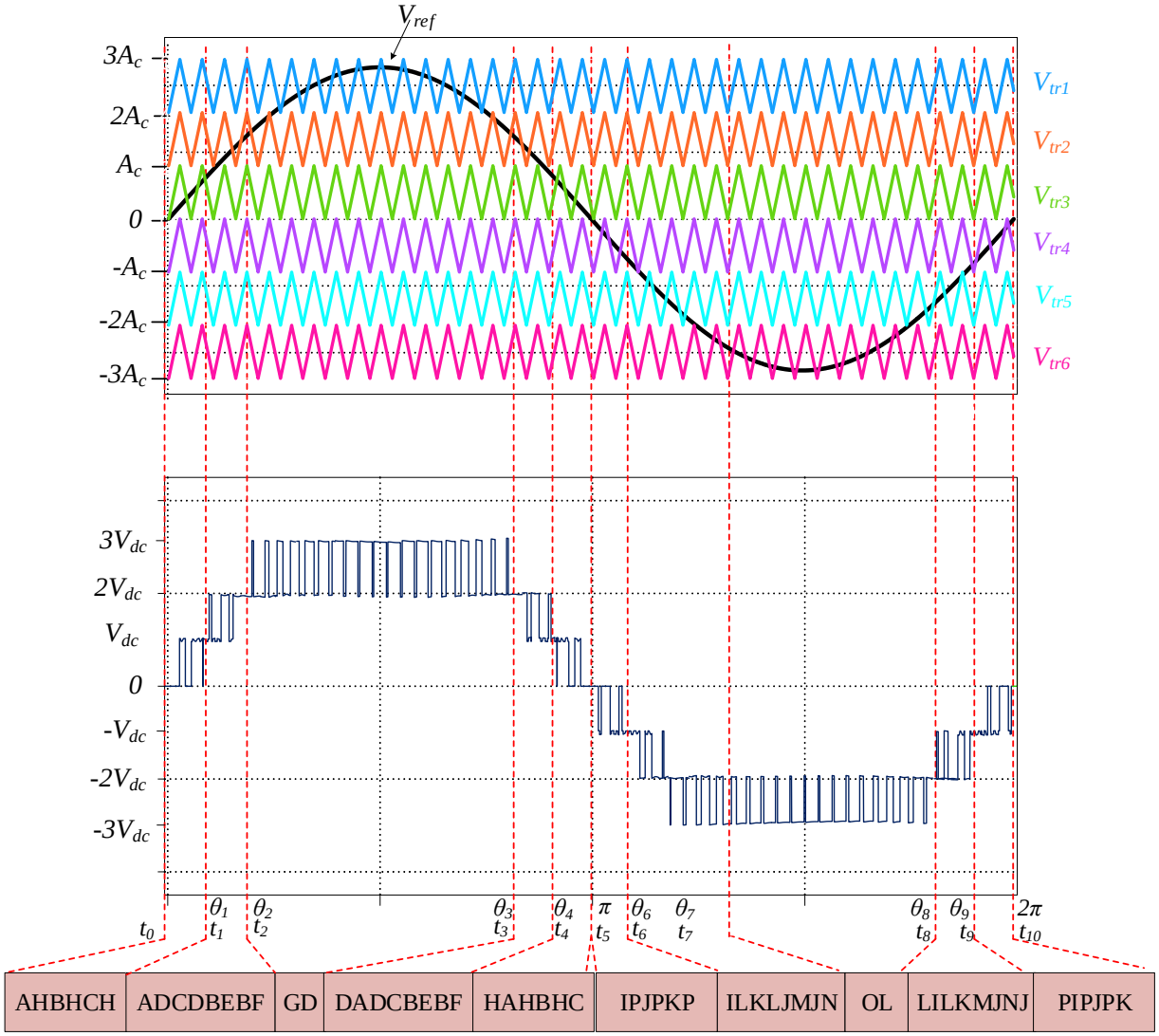


Figure 6.4 Modulation strategy of the proposed inverter under unity power factor.

6.4.2 Interval 1 (t_0 to t_1 and t_4 to t_5)

During this interval, the output voltage is switched between 0 and V_{dc}. States A, B, and C are used to generate V_{dc} while state H is used to generate 0. Using these different redundant states

(A, B and C) to generate V_{dc} enables the controller to regulate the voltage across the flying capacitor. When the flying capacitor voltage is lower than the input voltage, which is also used as a reference voltage to regulate the flying capacitor voltage (V_{CF}), state B is selected since this state provides a charging mode for the flying capacitor. However, when the flying capacitor voltage (V_{CF}) is greater than the reference voltage, states A or C are chosen. As a result, the switching sequence (AHBHCH) for interval (t_0 to t_1), and switching sequence (HAHBHC) for interval t_4 to t_5 helps to balance V_X. The modulation of interval 1 is shown in Figure 6.5.

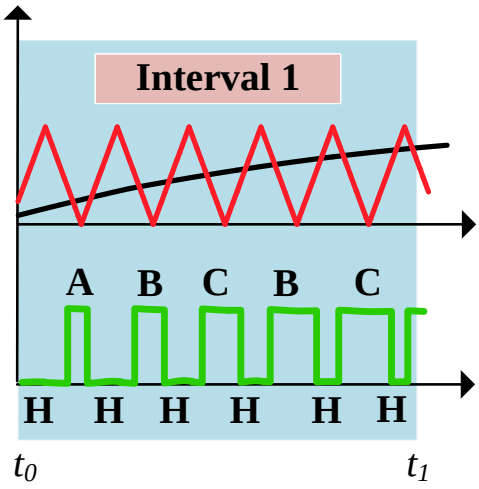


Figure 6.5 The modulation for interval 1.

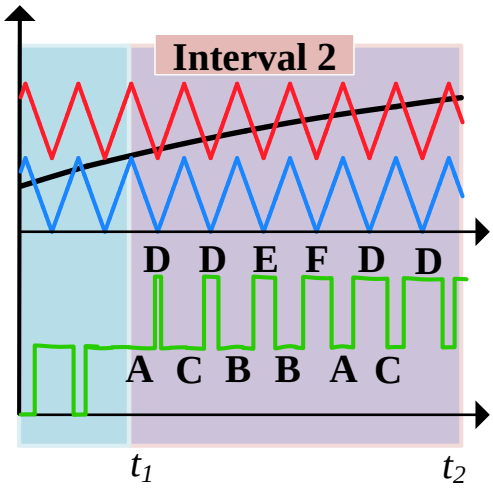


Figure 6.6 The modulation for interval 2.

The inverter output voltage during interval 1 can be express as:

$$V_{XO} = \begin{cases} V_{dc1}, & State\ A \\ V_{dcx}, & State\ B \\ V_{dcx}, & State\ C \\ 0, & State\ H \end{cases} \quad (6\text{-}8)$$

6.4.3 Interval 2 (t_1 to t_2 and t_3 to t_4)

During these operation zones, the output voltage is switched from V_{dc} to $2V_{dc}$. Redundant states (D, E, and F) are used to generate $2V_{dc}$. The switching sequence (ADCDBEBF) for interval (t_1 to t_2), and switching sequence (DADCEBFB) for interval (t_3 to t_4) maintain the voltage between V_{dc} to $2V_{dc}$. Selecting these redundant states provides self-balancing for the flying capacitor.

The inverter output voltages during this interval are:

$$V_{XO} = \begin{cases} V_{dc1}\,, & State\ A \\ V_{dcx}\,, & State\ B \\ V_{dcx}\,, & State\ C \\ V_{dc1} + V_{dcx}\,, & State\ D \\ V_{dc1} + V_X, & State\ E \\ V_{dcx} + V_X, & State\ F \end{cases} \tag{6-9}$$

Figure 6.6 shows the modulation of interval 2 during (t_1 to t_2). The self-voltage balancing during (t_1 to t_2) is implemented using the redundant states (D, E, and F), which generate $2V_{dc}$. Both states E and F can generate $2V_{dc}$ with a flying capacitor being discharged. In other words, the flying capacitor is always discharged during states E and F. Therefore, when using these states during interval 2, and the flying capacitor voltage is lower than the reference voltage, the flying capacitor is charged by using state B. This ensures the charging mode for the flying capacitor is available. However, when the flying capacitor voltage is greater than the reference voltage, states A or C are selected to provide the discharge mode for the capacitor. Consequently, using this redundant state results in self-balancing.

6.4.4 Interval 3 (t_2 to t_3)

The output voltage during this period of time is changing from $2V_{dc}$ to $3V_{dc}$. To generate $3V_{dc}$, state G is used, which generates the voltage by using the proposed novel inverter.

The output voltages during interval 3 are:

$$V_{XO} = \begin{cases} V_{dc1} + V_{dcx}, & State\ D \\ V_{dc1} + V_{dcx} + V_X, & State\ G \end{cases} \quad (6\text{-}10)$$

It is obvious that during this interval just state D is used to generate $2V_{dc}$, but not E or F. That is, states E and F can generate $2V_{dc}$, but the flying capacitor is always being discharged; however, state D provides the charging mode for the flying capacitor. Since there is just one state to generate $3V_{dc}$, state G, and the flying capacitor is always being discharged, the state G should provide charging mode. Consequently, self-balancing for the flying capacitor depends on the state that generates $2V_{dc}$ and charges the capacitor, which makes the flying capacitor ready to be discharged in the next level ($3V_{dc}$).

6.4.5 Interval 4 (t_5 to t_6 and t_9 to t_{10})

The output voltage during this interval is 0 and -V_{dc}. Redundant states H and I are used to generate -V_{dc}, and state P is used for the 0 states. The balancing of this interval is similar to interval 1. The switching state sequences for (t_5 to t_6) is (IPJPKP), and for (t_9 to t_{10}) is (PIPJPK).

The output voltages of the inverter during this interval are:

$$V_{XO} = \begin{cases} -V_{dc1}, & State\ I \\ -V_{dcx}, & State\ J \\ -V_{dcx}, & State\ K \\ 0, & State\ P \end{cases} \quad (6\text{-}11)$$

6.4.6 Interval 5 (t_6 to t_7 and t_8 to t_9)

The switching states sequences (ILKLJMJN) and (LILKMJNJ) during (t_6 to t_7) and (t_8 to t_9), respectively, are used to generate -V_{dc} and -$2V_{dc}$, and also ensure self-balancing for the flying capacitor voltage.

The phase inverter output voltage (V_{XO}) can be written as:

$$V_{XO} = \begin{cases} -V_{dc1}\,, & State\ I \\ -V_{dcx}\,, & State\ J \\ -V_{dcx}\,, & State\ K \\ -V_{dc1} - V_{dcx}\,, & State\ L \\ -V_{dc1} - V_X, & State\ M \\ -V_{dcx} - V_X, & State\ N \end{cases} \tag{6-12}$$

6.4.7 Interval 6 (t_7 to t_8)

The switching states L and O are selected to produce -2V_{dc} and -3V_{dc}. During this interval, self-balancing for the flying capacitor is also implemented using the same strategy as in interval 3.

The phase voltage during this interval can be calculated as the following:

$$V_{XO} = \begin{cases} -V_{dc1} - V_{dcx}\,, & State\ L \\ -V_{dc1} - V_{dcx} - V_X, & State\ O \end{cases} \tag{6-13}$$

6.4.8 Non-Unity Power Factor Operation

An example of a non-unity power factor under a reactive power condition, where the output voltage and current have different polarities is shown Figure 6.7. Four operational zones (Z1 through Z4) can be defined to express the modulation scheme during a complete grid cycle depending on the output current direction and the voltage polarity.

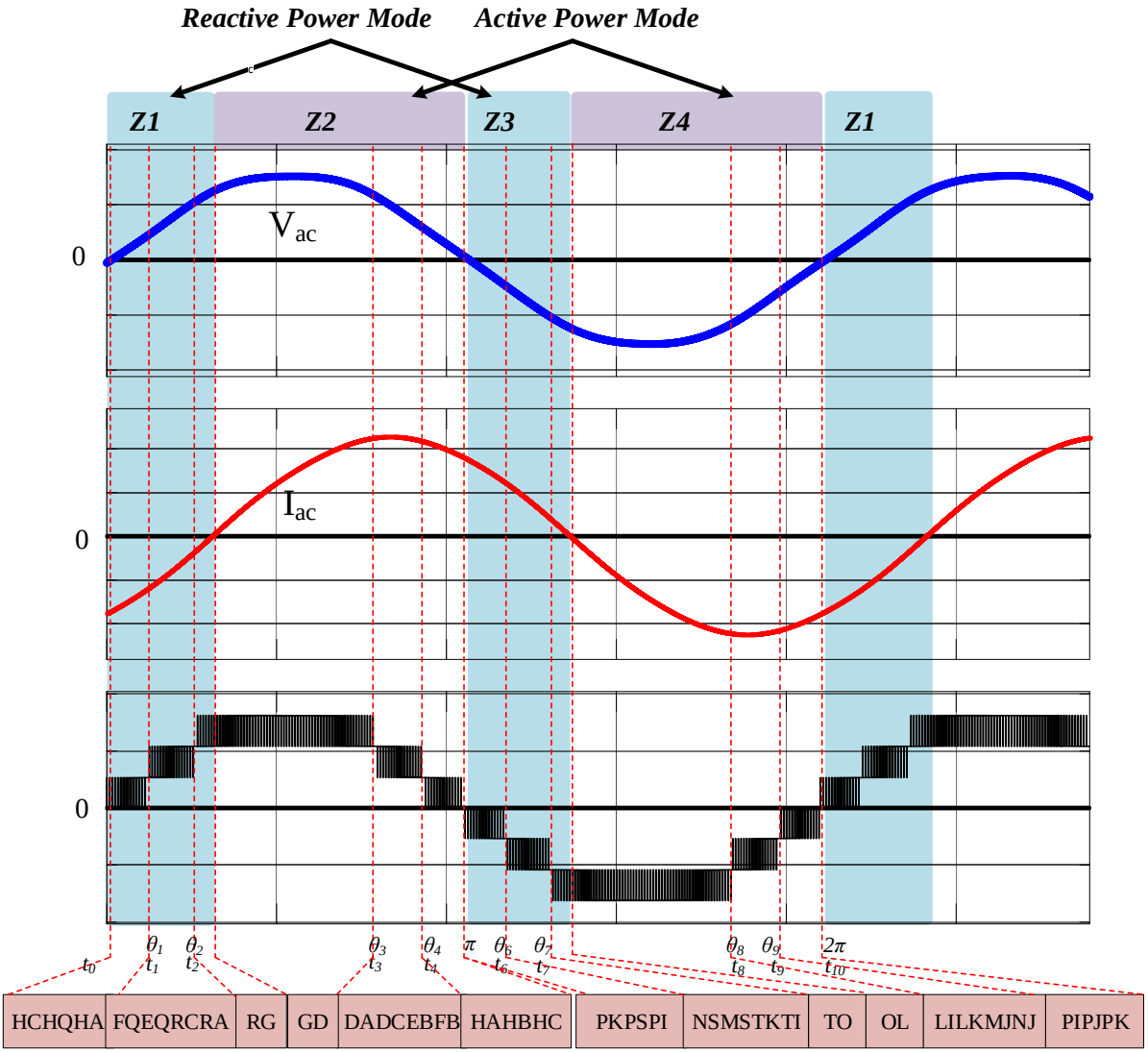


Figure 6.7 Modulation strategy of the proposed inverter under non-unity power factor.

The reactive power region, where the output voltage and current have a different direction, is represented by Z1 and Z3. During Z1, the voltage polarity is positive, while current is in the negative direction. However, the output voltage is positive and current is positive in Z3. The active power region is defined as Z2 and Z4, where both the output voltage and current have the same direction. It is clear that under the active power operation, the switching states have the same sequence as the unity power factor as shown in Figure 6.4.

Even if switches S_3 and S_6 are unidirectional, which does not affect the inverter ability to operate under reactive power mode. When the output voltage and current have different directions, the switching states B, D, J, and L transfer naturally to be Q, R, S, and T as summarized in Figure 6.8.

The output voltage of the inverter during the reactive power mode are:

$$V_{XO} = \begin{cases} V_{dc1}\,, & State\ Q \\ V_{dcx} + V_{dc1}, & State\ R \\ -V_{dc1}, & State\ S \\ -V_{dc1} - V_{dc1}, & State\ T \end{cases} \tag{6-14}$$

The switching states are not part of the main switching states of the inverter that were described in the unity power factor section. The switches naturally commutate due to the fact that the polarity and direction of the output voltage and current are different. The operation stated of the inverter under both unity and non-unity power factor is summarized in Figure 6.9.

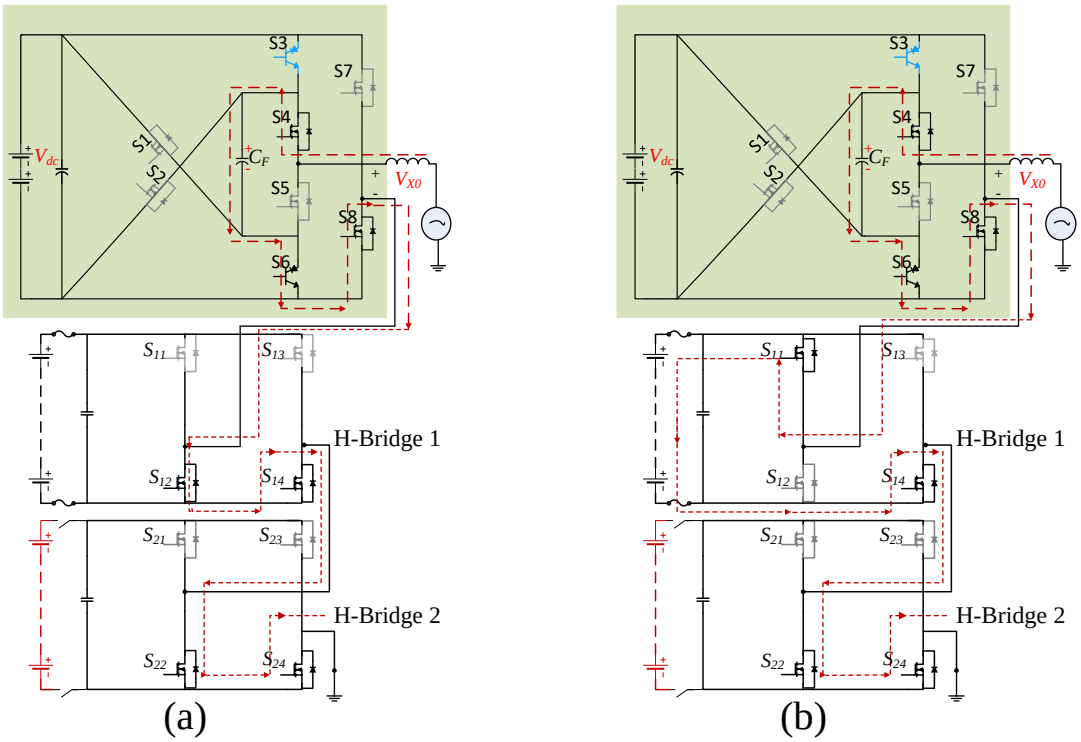


Figure 6.8 Switching states analysis of the proposed 7-L Hybrid CHB inverter.

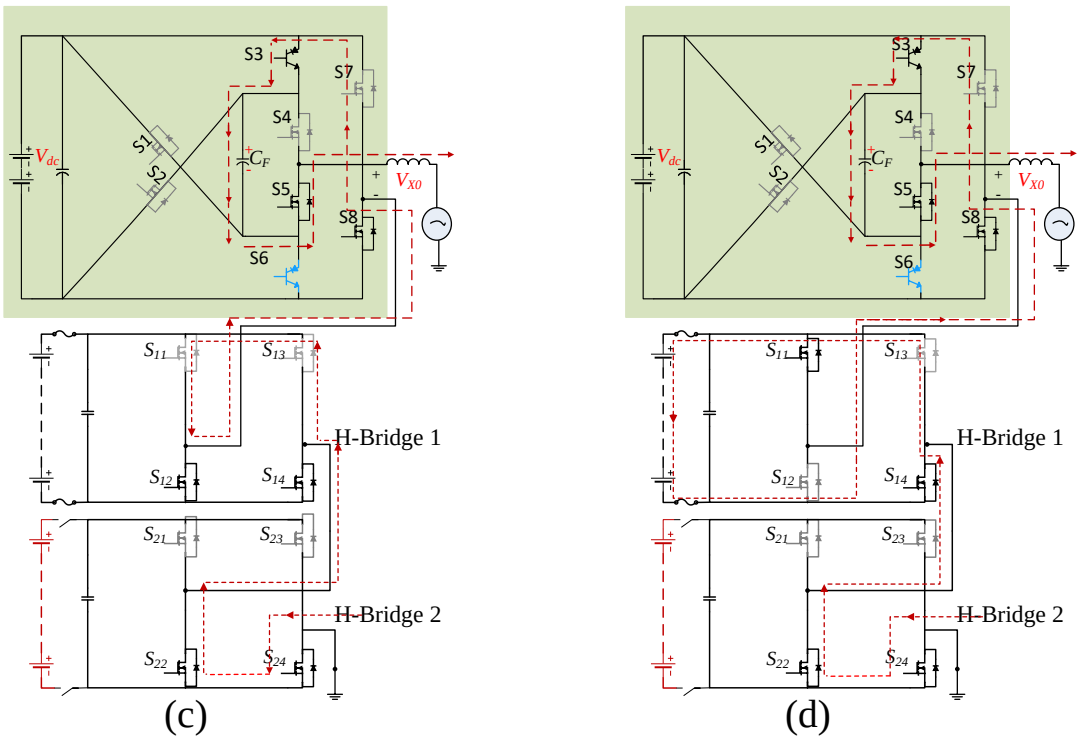


Figure 6.8 Switching states analysis of the proposed 7-L Hybrid CHB inverter (Cont.).

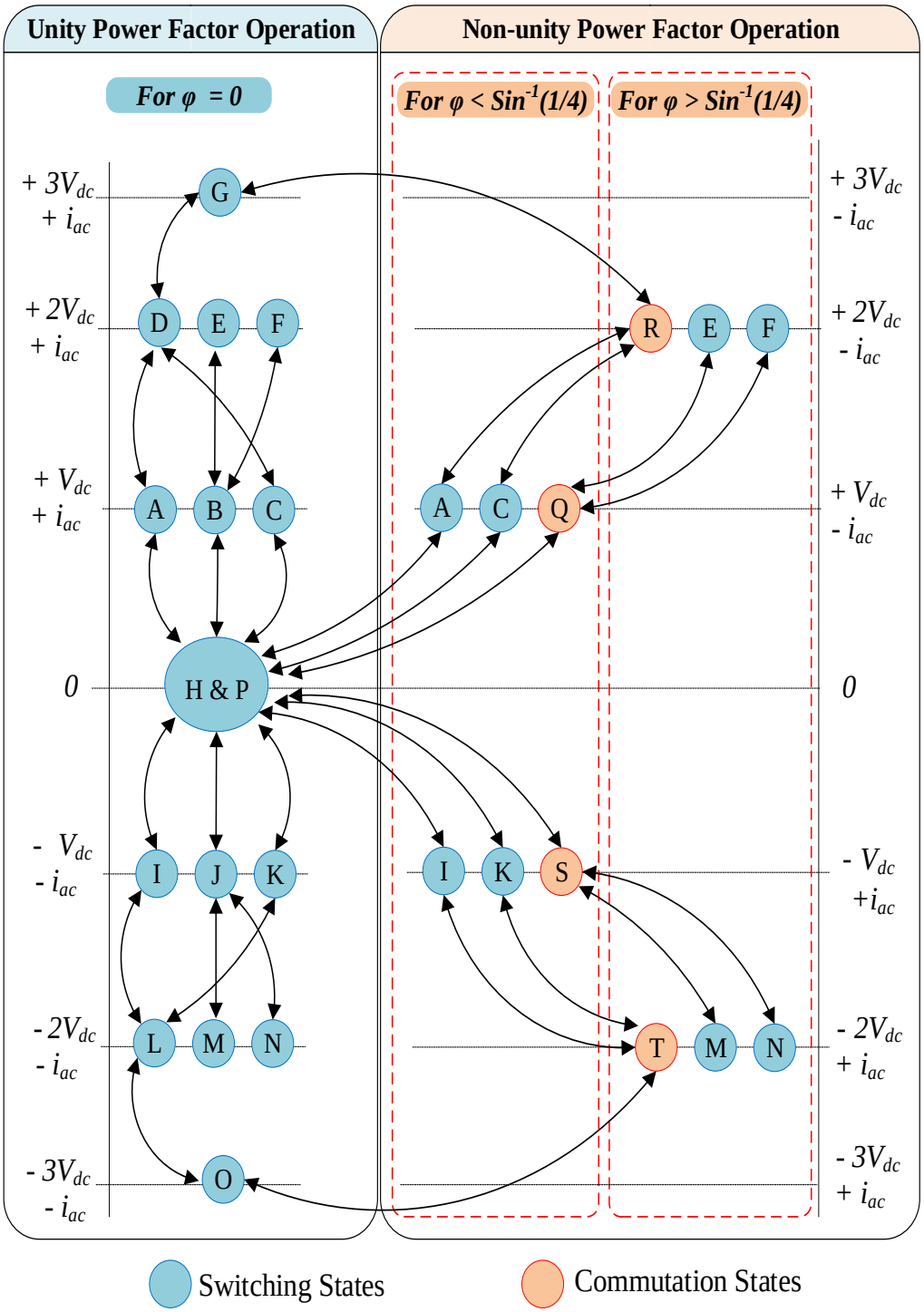


Figure 6.9 Switching states during unity and non-unity power factors.

6.5 Flying Capacitor Design

As mentioned previously, the modulation strategy can ensure capacitor voltage self-balancing for the proposed topology, which keeps the flying capacitor voltage balanced. The flying capacitor selection is an important factor to reduce the voltage ripple and ensure a stable output voltage.

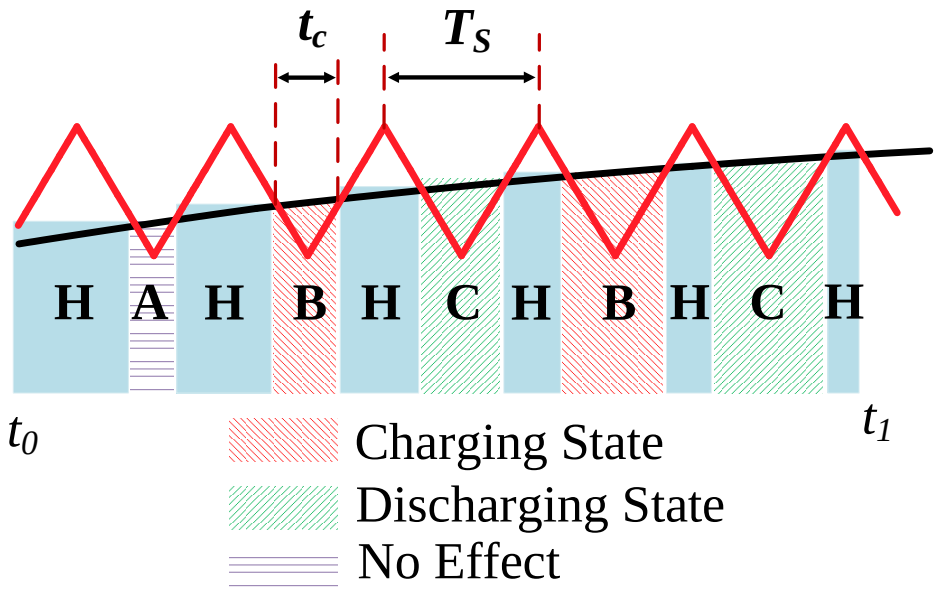


Figure 6.10 Illustration of charging/discharging of Interval 1.

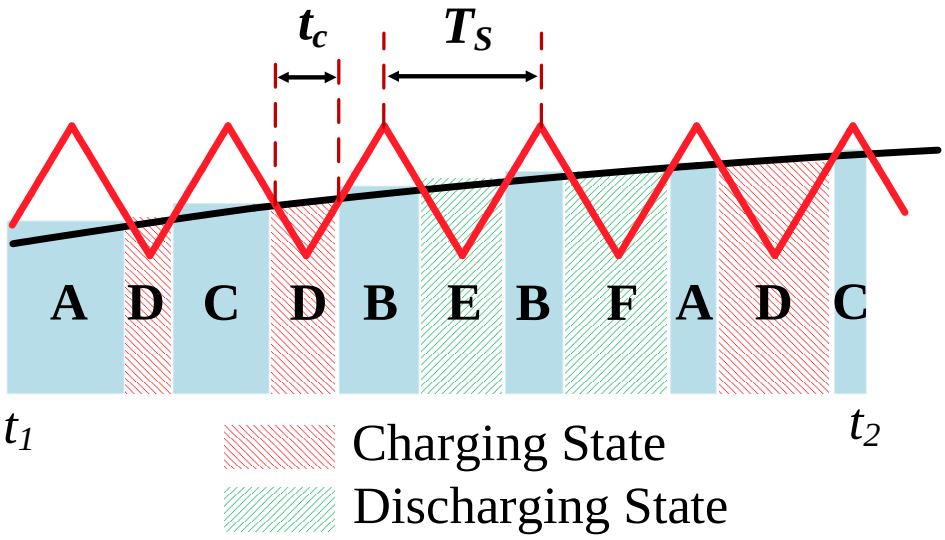


Figure 6.11 Illustration of charging/discharging of Interval 2.

The flying capacitor design is determined by its voltage ripple [6.33]-[6.34]. As shown in Figures 6.10 and 6.11, using different redundant states enables the proposed modulation strategy to regulate the voltage across the flying capacitor. Therefore, the charging time is utilized to obtain the flying capacitor voltage ripple. Figures 6.10 and 6.11 show the switching states of the inverter in intervals 1 and 2, respectively. The charging time (t_c) of the flying capacitor can be expressed as [6.33]-[6.34]:

$$t_c = \begin{cases} = \frac{M \sin\theta}{f_s/2}, & M\sin(\theta) \leq \frac{1}{3} \\ \frac{1-M\sin\theta}{f_s/2}, & M\sin(\theta) \geq \frac{1}{3} \end{cases} \tag{6-15}$$

where f_s is the switching frequency, and θ is the reference phase angle. During the flying capacitor charging time, the FC voltage ripple can be calculated as

$$\Delta V_{CF} = \frac{\Delta Q_{FC}}{C_{FC}} = \frac{I_{pk}\sin(\theta)t_c}{C_{FC}} \tag{6-16}$$

where I_{pk} is the peak value of the output current. Using Eqs. (6-15) and (6.16), the flying capacitor voltage ripple can be written as

$$\Delta V_{CF} = \frac{2I_{pk}\, M \sin^2(\theta)}{C_{FC}\, f_s}, \quad M\sin(\theta) \leq \frac{1}{3} \tag{6-17}$$

$$\Delta V_{CF} = \frac{2I_{pk}\,[\sin(\theta) - M\sin^2(\theta)}{C_{FC}\, f_s}, \quad M\sin(\theta) \geq \frac{1}{3} \tag{6-18}$$

The flying capacitor voltage ripple reaches its peak when $\sin(\theta) = 1/(3M)$. Using this condition, the minimum value of the flying capacitor can be calculated as

$$C_{FC,min} \geq \frac{3I_{pk}}{8\, f_s \Delta V_{CF} M} \tag{6-19}$$

6.6 Simulation and Experimental Results

To verify the concept of the proposed hybrid CHB inverter, a detailed MATLAB/Simulink® model for a circuit of Figure 6.2 was modeled for a 7-level inverter. The parameter and component

values of the simulation and experiments are shown in Table 6.2. The simulation parameters are: input voltage of 133 V, switching frequency of 15 kHz, modulation index of M=0.85. As discussed previously, the value of the flying capacitor in the unity power factor condition is calculated according to Eq. (6-19) and is determined to be 100 µF.

Figure 6.12 shows the output voltage (unfiltered and filtered), line current, and voltage across the flying capacitor waveforms for the proposed hybrid CHB inverter under unity power factor. The inverter capability of operation in lagging and leading power factor has been successfully tested. Figure 6.13 and Figure 6.14 show the inverter operation under lagging and leading power factors, respectively. There is no specific consideration or technique that the proposed inverter requires to operate under any power factor. Figure 6.13 and Figure 6.14 are verifications of the operations as demonstrated in Figure 6.9.

Table 6.2 Simulation and Experimental Parameters

Description	**Value**
Number of cells	3
Input voltage (Vdc)	400 V
Line frequency	60 Hz
Filter inductor,	0.16 mH
Filter Capacitor	50 µF
Carrier frequency	15 kHz
Load (inductive)	30 Ω, 10 mH

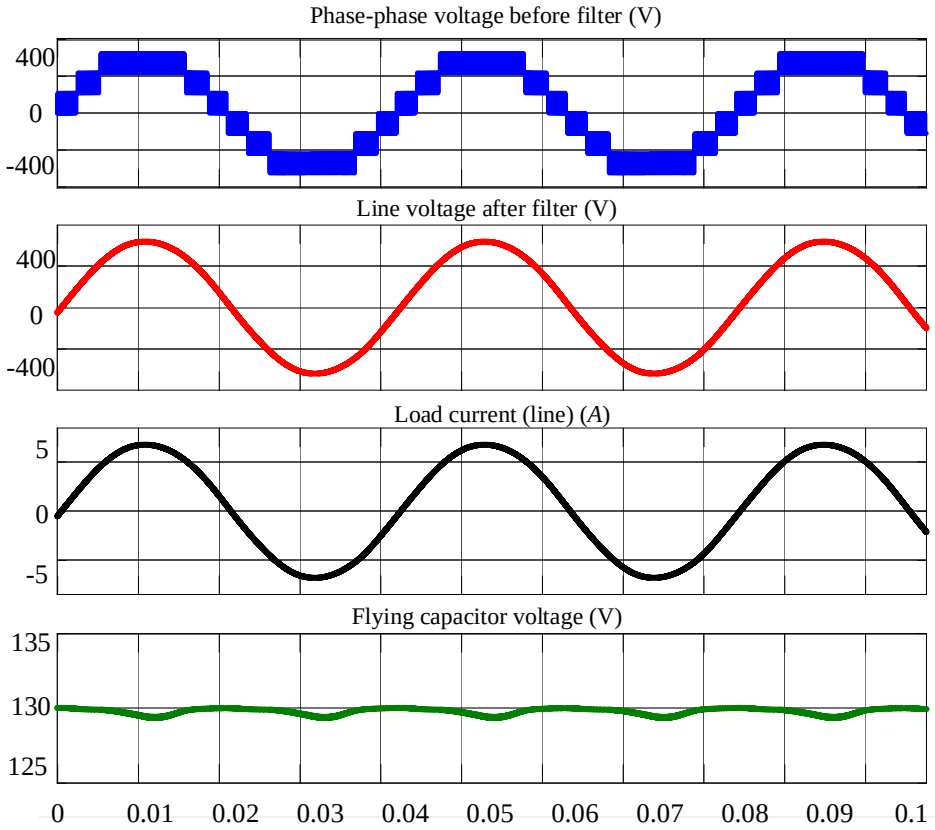


Figure 6.12 Operation of the inverter under unity power factor.

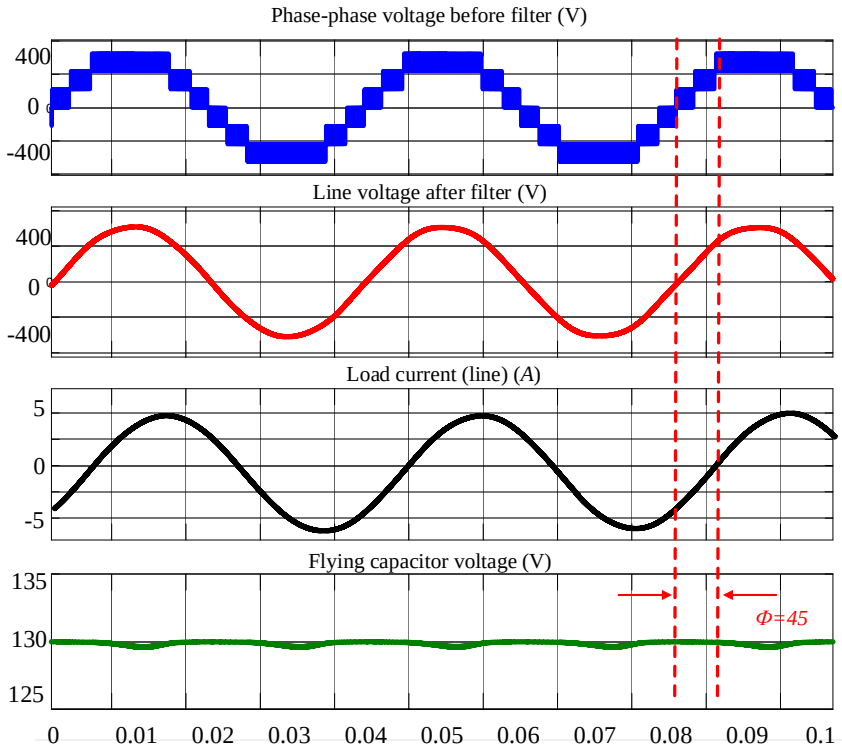


Figure 6.13 Operation of the inverter under lagging power factor.

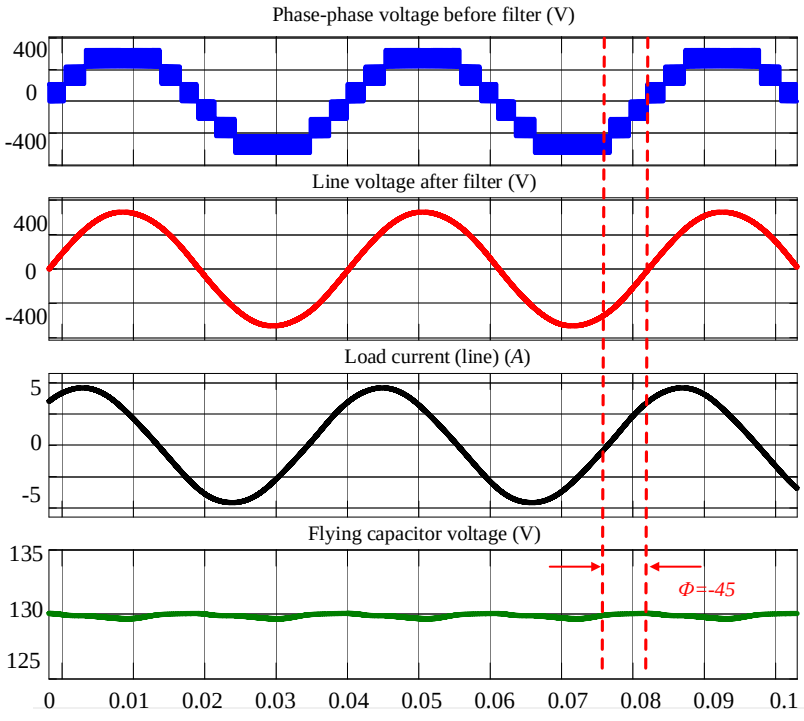


Figure 6.14 Operation of the inverter under leading power factor.

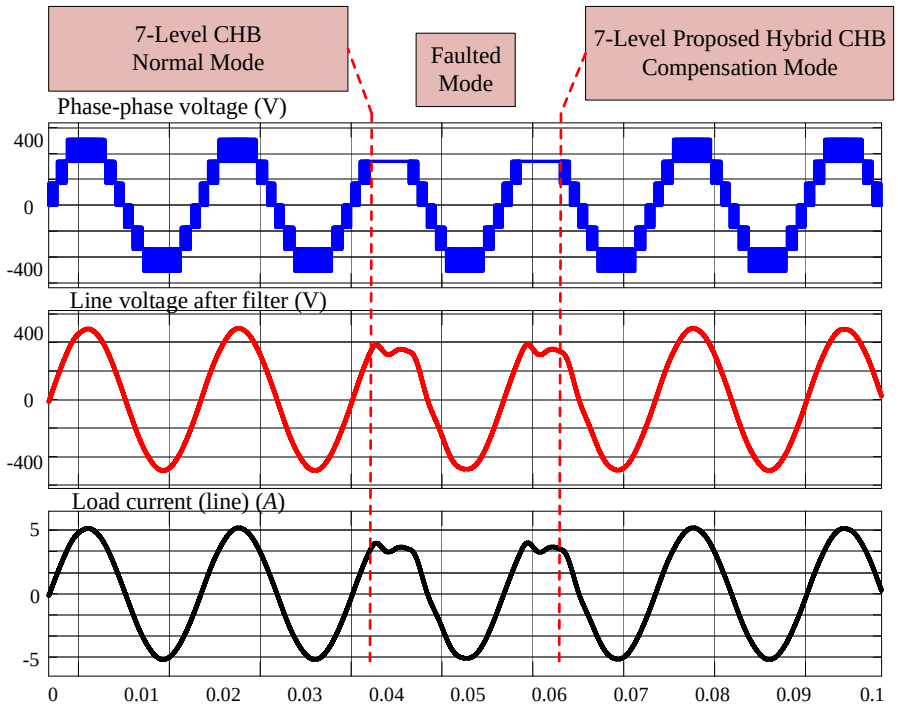


Figure 6.15 Normal, faulted, and compensation modes (resistive load).

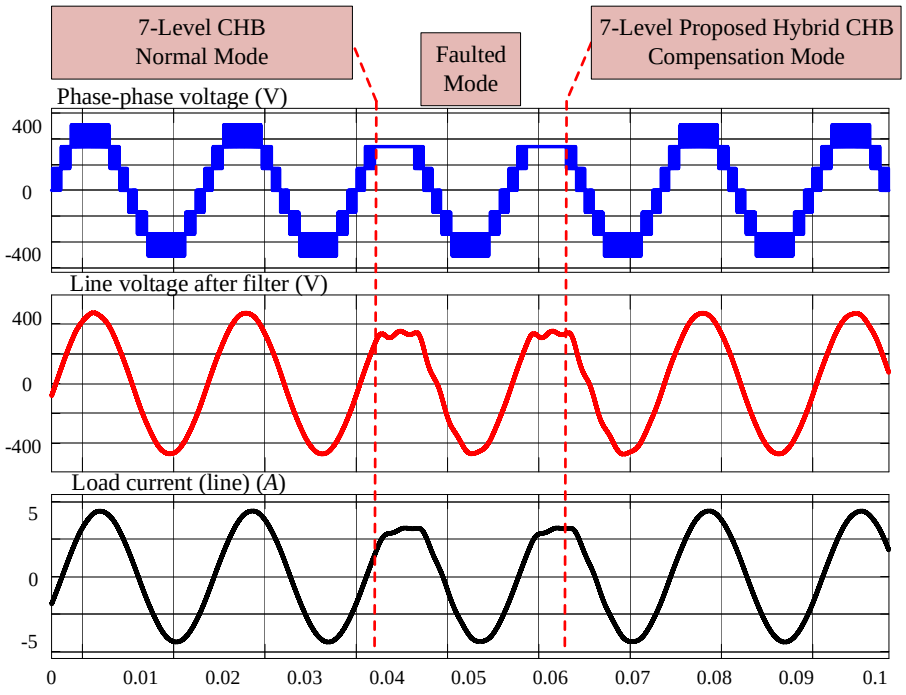


Figure 6.16 Normal, faulted, and compensation modes (inductive load).

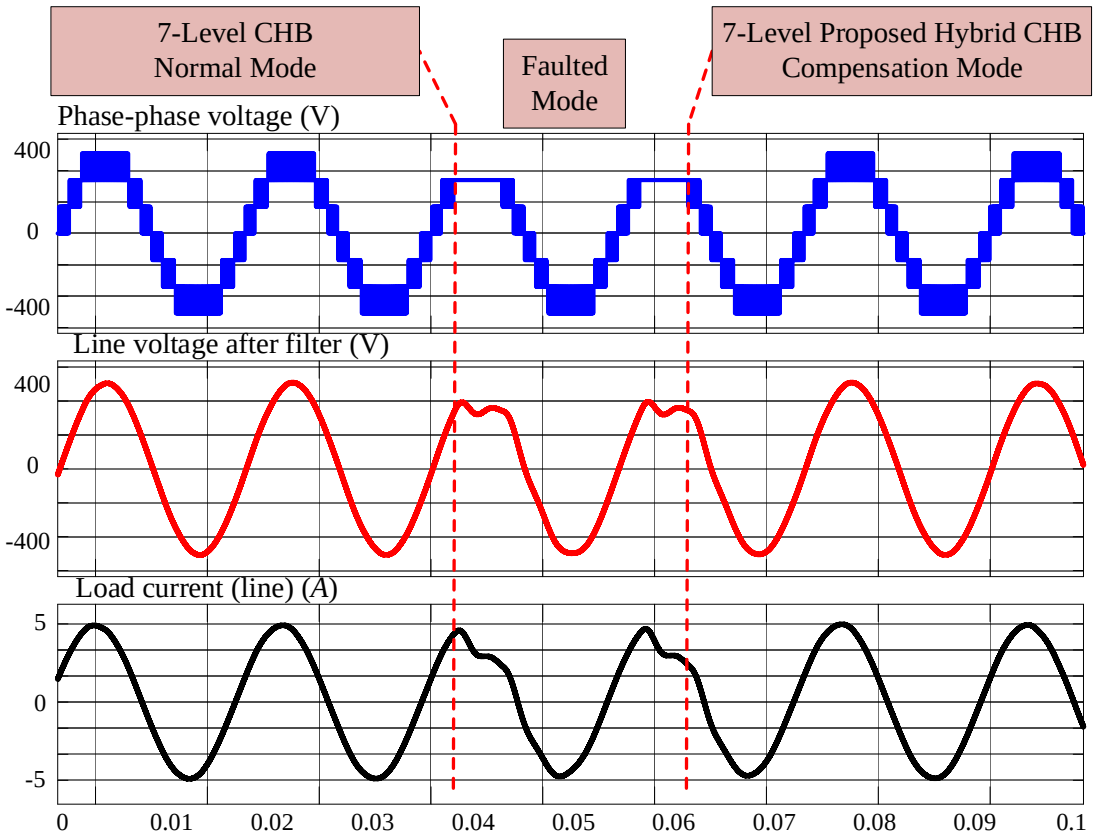
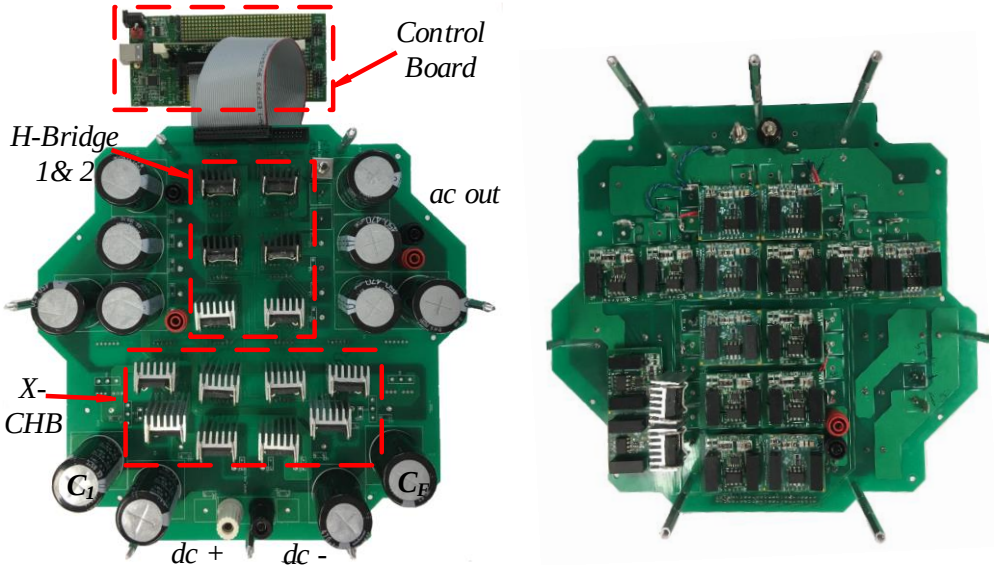


Figure 6.17 Normal, faulted, and compensation modes (capacitive load).

An open-circuit fault scenario has been created in S_{21} in Figure 6.2. As shown in Figure 6.15, the three different modes are: normal operation mode (where the inverter functions as a normal CHB), faulted mode (a fault is induced, and one voltage is lost), and compensation mode (where the proposed hybrid CHB operation starts). During the faulted mode, the output voltage loses one voltage level. The fault is detected and isolated using the method proposed in [6.32]. The X-CHB compensates for the lost output voltage and restores the output voltage to normal levels without affecting the system connected downstream. The proposed inverter was also tested under lagging and leading power factor to show its capability of operating under reactive power conditions. Figure 6.16 and Figure 6.17 show the normal operation, faulted mode, and compensation mode during lagging and leading power factors, respectively.

A scaled-down 7-level hybrid CHB low-power prototype has been built and tested in the laboratory as shown in Figure 6.18 to validate the concept and performance of the new circuit. All the switches are (C2M0040120D) from Cree/Wolfspeed. The output voltage (unfiltered and filtered), and line current under normal operation and unity power factor are shown in Figure 6.19.



(a) (b)

Figure 6.18 (a) Top view shows the proposed hybrid CHB inverter, (b) Bottom view shows the gate drivers "Photo by Author."

To verify the inverter ability to operate under reactive power modes, the inverter has been tested under lagging and leading power factors as shown in Figures 6.20 and 6.21, respectively. The inverter's ability to generate a 7-level output voltage levels with a pure sinusoidal voltage is demonstrated in both of the figures. An open-circuit fault has been created in S_{21} in Figure 6.2. After the fault occurs in S_{21}, the method in [6.32] for fault detection and isolation is used. Figure 6.22 shows the output voltage (unfiltered and filtered) and line current under normal, faulted and compensation modes for power factor. Figure 6.23 and Figure 6.24 show the output voltage

(unfiltered and filtered) and line current under normal, faulted and compensation modes for both lagging and leading power factors, respectively. Figures 6.23 and 6.24 show smooth transition from faulted mode to a compensation mode. Consequently, the output voltage of the inverter is the same before and after the fault happened.

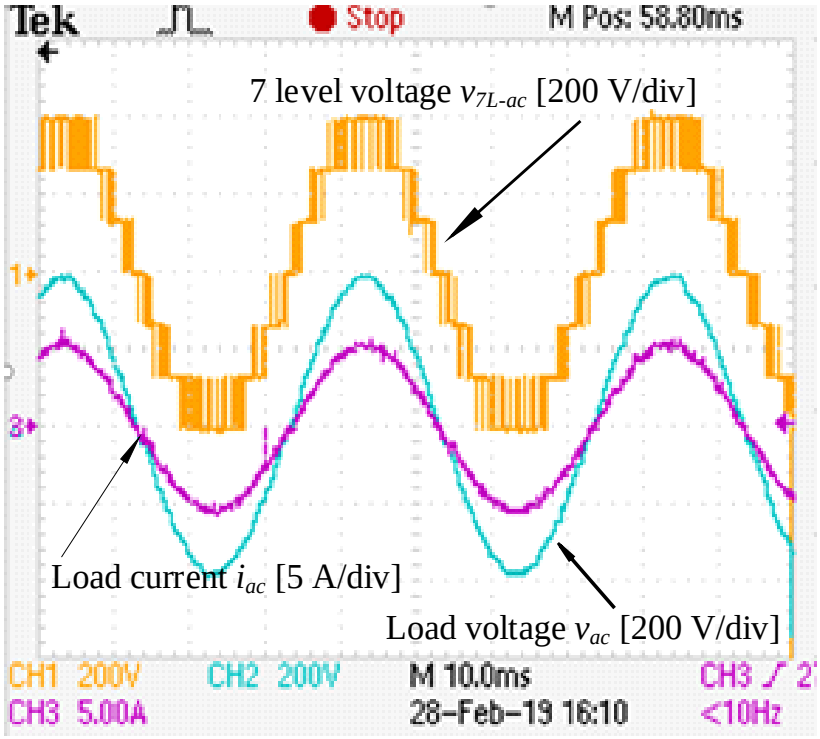


Figure 6.19 Operation of the inverter under unity power factor.

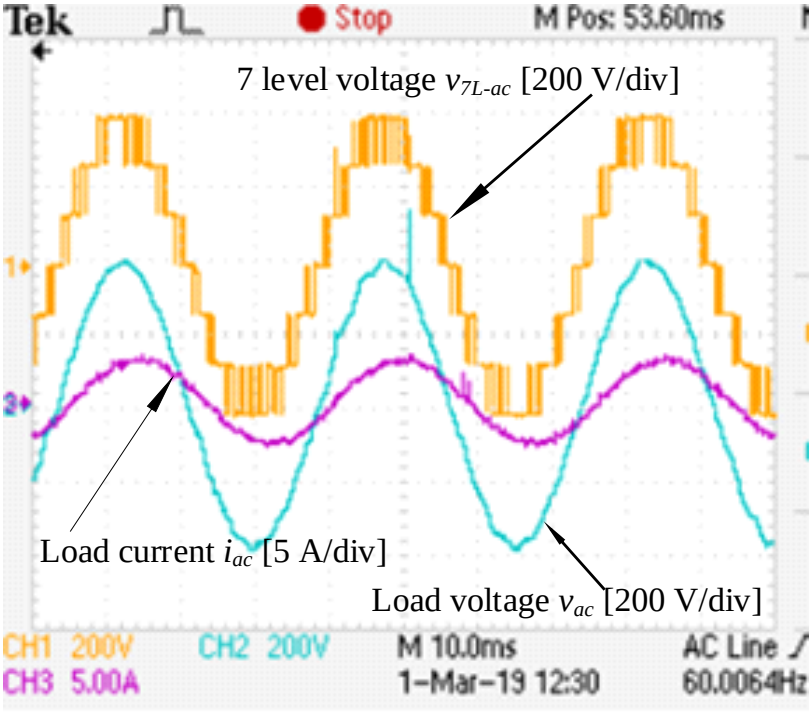


Figure 6.20 Operation of the inverter under lagging power factor.

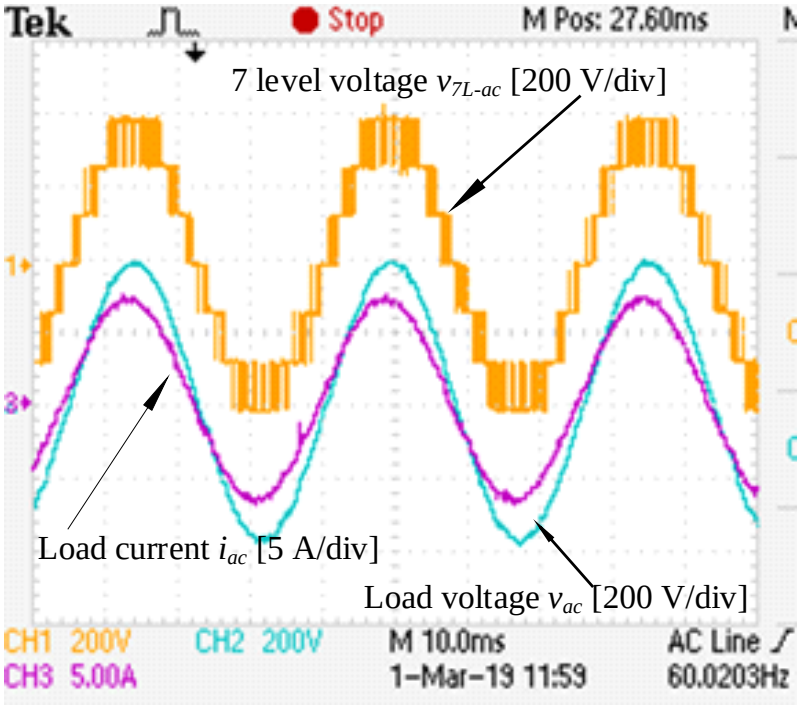


Figure 6.21 Operation of the inverter under leading power factor.

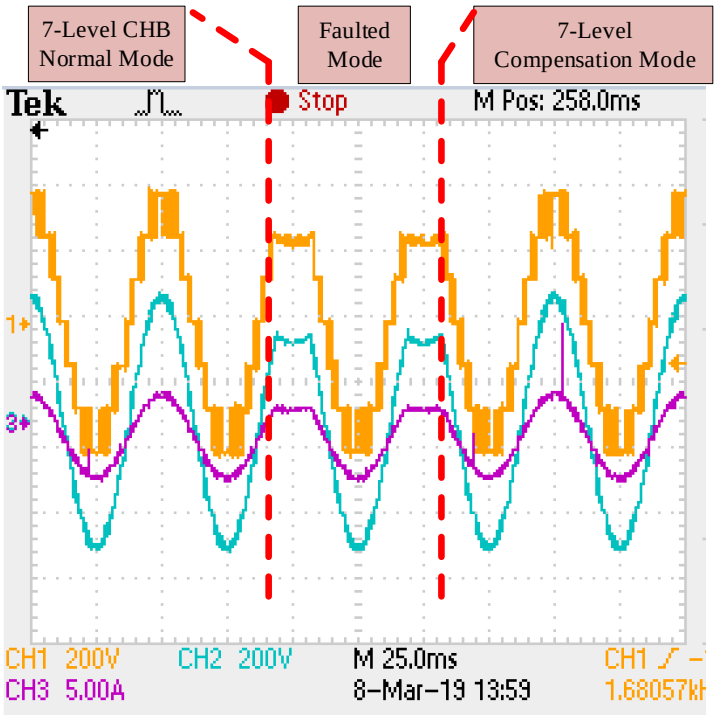


Figure 6.22 Normal, faulted, and compensation modes (resistive load).

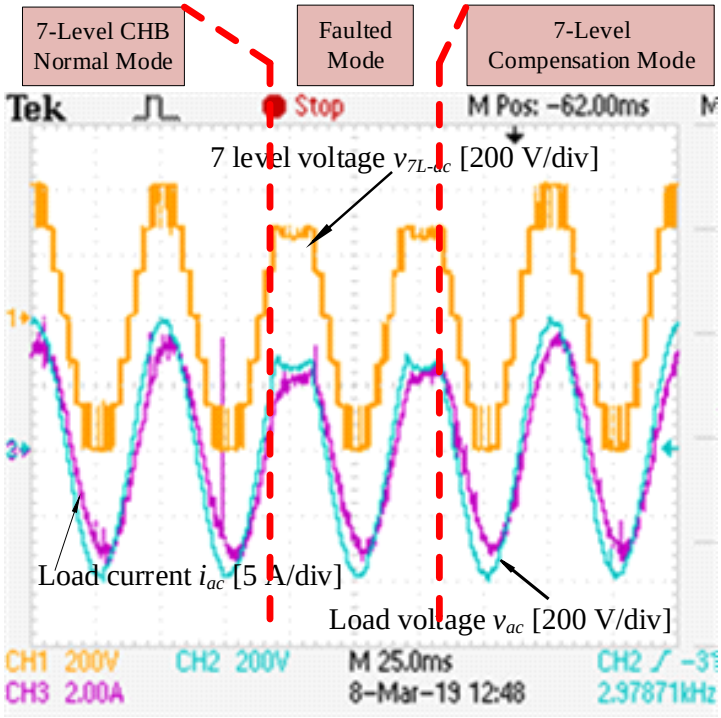


Figure 6.23 Normal, faulted, and compensation modes (inductive load).

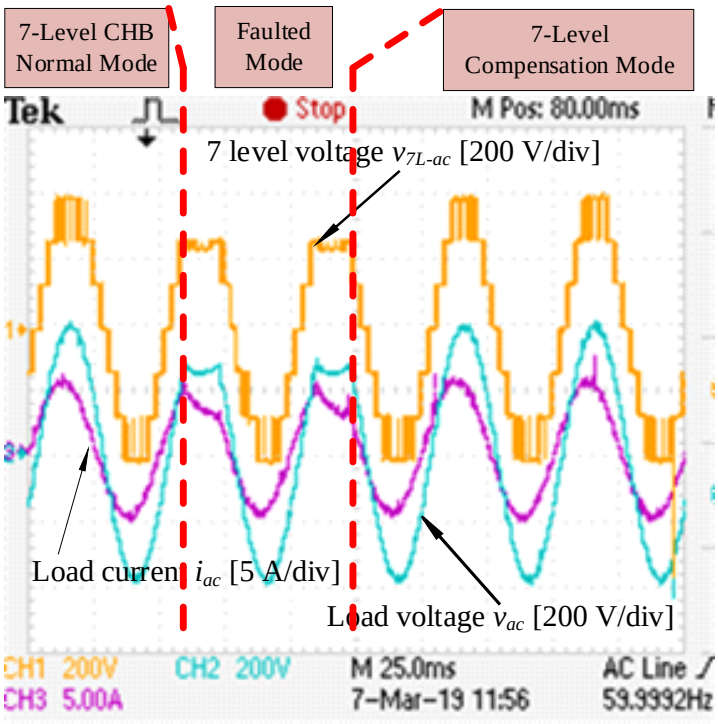


Figure 6.24 Normal, faulted, and compensation modes (capacitive load).

6.7 Conclusions

This chapter presents a novel hybrid CHB for fault-tolerant operation to ensure seamless operation of the system under an open/short circuit-switching fault or dc supply fault using a novel X-CHB circuit. In addition to fault-tolerant ability, the proposed inverter has the ability to boost the voltage by a factor of two, which compensates for the missing voltage level in the case of open/short circuit faults. Moreover, the proposed topology has full reactive power operation due to its capability of operation in any power factor (lagging/leading). Furthermore, the presented modulation strategy enables self-balancing for the flying capacitor of the proposed X-CHB. Simulation and experimental results validate the performance of the proposed topology.

6.8 References

[6.1] S. Kouro *et al*., "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553-2580, Aug. 2010.

[6.2] S. Rivera *et al*., "Multilevel Direct Power Control—A Generalized Approach for Grid-Tied Multilevel Converter Applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5592-5604, Oct. 2014.

[6.3] J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724-738, Aug. 2002.

[6.4] H. Abu-Rub, J. Holtz, J. Rodriguez and G. Baoming, "Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581-2596, Aug. 2010.

[6.5] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo and M. A. M. Prats, "The age of multilevel converters arrives," in *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28-39, June 2008.

[6.6] B. Mirafzal, "Survey of Fault-Tolerance Techniques for Three-Phase Voltage Source Inverters," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 10, pp. 5192-5202, Oct. 2014.

[6.7] P. Lezana, J. Pou, T. A. Meynard, J. Rodriguez, S. Ceballos and F. Richardeau, "Survey on Fault Operation on Multilevel Inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2207-2218, July 2010.

[6.8] H. Wang *et al*., "Transitioning to Physics-of-Failure as a Reliability Driver in Power Electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 1, pp. 97-114, March 2014.

[6.9] P. Tu, S. Yang and P. Wang, "Reliability- and Cost-Based Redundancy Design for Modular Multilevel Converter," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2333-2342, March 2019

[6.10] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran and P. Tavner, "An Industry-Based Survey of Reliability in Power Electronic Converters," *IEEE Transactions on Industry Applications*, vol. 47, no. 3, pp. 1441-1451, May-June 2011.

[6.11] A. Hanif, Y. Yu, D. DeVoto and F. Khan, "A Comprehensive Review Toward the State-of-the-Art in Failure and Lifetime Predictions of Power Electronic Devices," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4729-4746, May 2019.

[6.12] T. Peng *et al*., "A Uniform Modeling Method Based on Open-Circuit Faults Analysis for NPC-Three-Level Converter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 3, pp. 457-461, March 2019.

[6.13] J. Zhang, Z. Liu, T. Wang, M. E. H. Benbouzid and Y. Wang, "An Arm Isolation and Reconfiguration Fault Tolerant Control Method Based on Data-driven Methodology for Cascaded Seven-level Inverter," *2018 IEEE 7th Data Driven Control and Learning Systems Conference (DDCLS)*, pp. 939-943, Enshi, 2018.

[6.14] W. Song, A. Q. Huang, "Fault-tolerant design and control strategy for cascaded H-bridge multilevel converter-based STATCOM", *IEEE Transactions on Industrial Electronic.*, vol. 57, no. 8, pp. 2700-2708, Aug. 2010

[6.15] A. Yazdani, H. Sepahvand, M. L. Crow and M. Ferdowsi, "Fault Detection and Mitigation in Multilevel Converter STATCOMs," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1307-1315, April 2011.

[6.16] S. Rahman, M. Meraj, A. Iqbal and L. Ben-Brahim, "Novel voltage balancing algorithm for single-phase cascaded multilevel inverter for post-module failure operation in solar photovoltaic applications," in *IET Renewable Power Generation*, vol. 13, no. 3, pp. 427-437, 25 2 2019.

[6.17] M. Jalhotra, L. K. Sahu, S. P. Gautam and S. Gupta, "Reliability and energy sharing analysis of a fault-tolerant multilevel inverter topology," in *IET Power Electronics*, vol. 12, no. 4, pp. 759-768, 10 4 2019.

[6.18] E. Jamshidpour, P. Poure and S. Saadate, "Photovoltaic Systems Reliability Improvement by Real-Time FPGA-Based Switch Failure Diagnosis and Fault-Tolerant DC–DC Converter," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 7247-7255, Nov. 2015.

[6.19] S. Siouane, S. Jovanović, P. Poure and E. Jamshidpour, "An Efficient Fault Tolerant Cascaded Step-Up Step-Down Converter for Solar PV Modules," *2018 IEEE International Conference on Environment and Electrical Engineering and 2018 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe)*, Palermo, 2018, pp. 1-5.

[6.20] M. M. Haji-Esmaeili, M. Naseri, H. Khoun-Jahan and M. Abapour, "Fault-Tolerant and Reliable Structure for a Cascaded Quasi-Z-Source DC–DC Converter," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6455-6467, Aug. 2017.

[6.21] K. Ambusaidi, V. Pickert and B. Zahawi, "New Circuit Topology for Fault Tolerant H-Bridge DC–DC Converter," *IEEE Transactions on Power Electronics*, vol. 25, no. 6, pp. 1509-1516, June 2010.

[6.22] J. Amini and M. Moallem, "A Fault-Diagnosis and Fault-Tolerant Control Scheme for Flying Capacitor Multilevel Inverters," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 1818-1826, March 2017.

[6.23] M. Farhadi, M. T. Fard, M. Abapour and M. T. Hagh, "DC–AC Converter-Fed Induction Motor Drive With Fault-Tolerant Capability Under Open- and Short-Circuit Switch Failures," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1609-1621, Feb. 2018.

[6.24] R. V. Nemade, J. K. Pandit and M. V. Aware, "Reconfiguration of T-Type Inverter for Direct Torque Controlled Induction Motor Drives Under Open-Switch Faults," *IEEE Transactions on Industry Applications*, vol. 53, no. 3, pp. 2936-2947, May-June 2017.

[6.25] B. P. Reddy, M. Rao A, M. Sahoo and S. Keerthipati, "A Fault-Tolerant Multilevel Inverter for Improving the Performance of a Pole–Phase Modulated Nine-Phase Induction Motor Drive," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1107-1116, Feb. 2018.

[6.26] W. Chen, E. Hotchkiss and A. Bazzi, "Reconfiguration of NPC multilevel inverters to mitigate short circuit faults using back-to-back switches," *CPSS Transactions on Power Electronics and Applications*, vol. 3, no. 1, pp. 46-55, March 2018.

[6.27] M. Aly, E. M. Ahmed and M. Shoyama, "A New Single-Phase Five-Level Inverter Topology for Single and Multiple Switches Fault Tolerance," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9198-9208, Nov. 2018.

[6.28] M. M. Haji-Esmaeili, M. Naseri, H. Khoun-Jahan and M. Abapour, "Fault-tolerant structure for cascaded H-bridge multilevel inverter and reliability evaluation," *IET Power Electronics*, vol. 10, no. 1, pp. 59-70, 1 20 2017.

[6.29] H. K. Jahan, F. Panahandeh, M. Abapour and S. Tohidi, "Reconfigurable Multilevel Inverter With Fault-Tolerant Ability," in *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7880-7893, Sept. 2018.

[6.30] M. Aleenejad, H. Iman-Eini and S. Farhangi, "Modified space vector modulation for fault-tolerant operation of multilevel cascaded H-bridge inverters," *IET Power Electronics*, vol. 6, no. 4, pp. 742-751, April 2013.

[6.31] P. Moamaei, H. Mahmoudi and R. Ahmadi, "Fault-tolerant operation of cascaded H-Bridge inverters using one redundant cell," *2015 IEEE Power and Energy Conference at Illinois (PECI)*, Champaign, IL, pp. 1-5, 2015.

[6.32] H. Mhiesan *et al*., "A Method for Open-Circuit Faults Detecting, Identifying, and Isolating in Cascaded H-Bridge Multilevel Inverters," in *IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pp. 1-5, Charlotte, NC, 2018.

[6.33] Y. Siwakoti, A. Mahajan, D. Rogers and F. Blaabjerg, "A Novel Seven-Level Active Neutral Point Clamped Converter with Reduced Active Switching Devices and DC-link Voltage," *IEEE Transactions on Power Electronics*.

[6.34] H. Wang, L. Kou, Y. Liu and P. C. Sen, "A New Six-Switch Five-Level Active Neutral Point Clamped Inverter for PV Applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6700-6715, Sept. 2017.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

The key contributions in this dissertation are as follows:

(a) Presentation of a new method for open-circuit fault detection in a CHB inverter. This method was shown to be: 1) Straightforward for implementation due to its simple algorithm, 2) accurate for detection and location of the fault within one cycle, and 3) applicable to an unlimited number of CHB cells.

(b) Presentation of a novel power electronic circuit and method for fault-tolerance in power electronic inverter-rectifiers. This circuit provides a significant improvement over the existing techniques by isolating faulted devices and reconfiguring the converter so that the circuit can continue operation as it did during a pre-fault condition and, therefore, reduce the disruption of electricity delivery upon fault occurrence.

(c) Development of a new inverter (X-CHB) with a smaller number of switches and boosting ability. The proposed topology provides a 50% reduction in the number of batteries. Also, it possesses the ability to operate under a non-unity power factor, which enables it to be suitable for battery energy storage systems and STATCOM applications. Each cell of the proposed topology (X-CHB) can generate either 5-level or 7-level of output voltages.

(d) Presentation of a novel hybrid CHB for a fault-tolerant operation to ensure seamless operation of the system under an open/short circuit switching fault or dc supply fault using a novel circuit. In addition to fault tolerance ability, the proposed inverter is capable of

boosting the voltage by a factor of two, which compensates for the missing voltage level in the case of open/short circuit faults.

7.2 Future Work

Multilevel inverters have one of the most promising future outlooks amongst power electronics technologies due to their enabling ability for integration of renewable energy sources to medium and high voltage grids. The high-bandwidth devices and batteries technologies are developing at a rapid rate and will continue to progress in the future. Meanwhile, power electronic researchers and engineers must endeavor to find new methods for producing systems that are more reliable, less costly, and more efficient. In this work, multiple methods for fault detection and circuit reconfiguration in case of fault occurrence have been developed and investigated. This research calls for further investigation into the areas that follow.

7.2.1 PV Inverters

Multilevel inverters, particularly modular multilevel inverters, have been receiving great attention for many years. In conventional applications, decreasing the number of elements and cost of implementation along with increasing the efficiency are the main concerns. Leakage current reduction is also a point of concern in these circuits. Further investigation into development of multilevel inverter topologies is required.

One of the last investigated applications of PV inverters is aerospace. Reliability and EMI are paramount issues that need to be addressed in application of PV inverters in space. Multiple fault-tolerant methods for MLIs in BESS applications were proposed in this work. Future investigation into the development of faster fault detection methods and more reliable fault-tolerant topologies in PV inverters is necessary.

7.2.2 Electric Drives

One main focus of power electronics is the electric drive; specifically high voltage drives. These converters have multiple considerations and issues, namely the EMI and dv/dt. One of the proposed solutions for decreasing the EMI and dv/dt in these converters is the use of MLIs. However, in many cases, the failure of the multilevel inverter could lead to disastrous economic losses for the investor. Future research is required into the development of fault-tolerant multilevel inverters for electric drive applications.

7.2.3 High Power SiC Modules and Batteries

The highest-rated SiC power module available now is rated for 10 kV. Modular Multilevel Inverters, for instance the CHB inverter, have significantly simplified the control complexity of previous multilevel topologies. However, this simplification is subject to a trade-off with the dc bus requirements. A minimized number of modules translates into higher voltage ratings for these switches. Higher voltage SiC MOSFETs need to be developed for transformerless applications in MLIs in 33 kV, 66 kV, and 110 kV.

Batteries play a major role in BESS applications. Battery technologies are currently being developed by many companies including Tesla^{TM}. However, more investigation is required into the topic to develop more durable, higher voltage, and less costly batteries. This will enable the BESS to eventually have high voltage grid connection capabilities with higher reliability and less cost.