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Area Efficient Device Optimization for ESD Protection in High Speed Interface ICs

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Area Efficient Device Optimization for ESD Protection in
High Speed Interface ICs

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ABSTRACT

Electrostatic discharge (ESD) protection is considered as a vital step in integrated circuit (IC) manufacturing process. IC chips are unable to overcome the effects of transient events without adequate discharge protection. Recent trend in the industry has seen the incorporation of system level ESD protection within the IC chip. Incorporating system level on-chip ESD protection often increases cost, degrades circuit performance and consumes layout area which could otherwise be used for improving the circuit performance. These design challenges could be easily overcome if the parasitic components in a circuit were used for ESD protection. Despite the various design challenges, on-chip ESD protection is still desirable as it saves the area on the circuit board by eliminating the traditional ESD protection devices resulting in more compact circuits. Furthermore, using parasitic components while designing on-chip system level ESD protection can save layout area.

In order to effectively implement this solution, a study on ESD events, protection circuits and high-speed ICs was carried out. Different types of ESD events and the different models pertaining to ESD events were studied and are discussed in detail. An overview of high-speed integrated circuits was also carried out with emphasis on the protection topologies that are commonly used. The ESD characteristics of parasitic PNP devices in rail-based ESD protection structure was then studied to summarize its viability as a protection circuit. The turn-on or breakdown voltage of the parasitic PNP is studied by technology computer aided design (TCAD) simulations performed in Silvaco software. The breakdown voltage, holding voltage, on resistance and failure current were studied and modeled to maximize ESD protection.

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to my graduate advisor and thesis director, Dr. Zhong Chen for providing me the opportunity to work on electrostatic discharge reliability for integrated circuits. I am greatly thankful to Dr. Chen for his guidance, motivation and patience which enabled me to persevere and apply myself in my research.

I would also like to acknowledge Dr. Simon Ang and Dr. Fisher Yu who serve as my master's thesis committee members and have made my study here intellectually challenging and delightful.

Finally, I must express my profound gratitude to my parents for providing me with emotional support and continuous encouragement through my years of study. Thank you.

DEDICATION

This thesis is dedicated to my loving parents for their unwavering trust and support. Continuous encouragement, motivation and valuable advices from my parents helped me to focus on my graduate career.

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I. INTRODUCTION

A. ELECTROSTATIC DISCHARGE

Electrostatic discharge (ESD) is the flow of static electricity between differently charged objects in a very short interval of time [1]. Static electricity is caused by the imbalance of electrons in the surface of a material. If a material has such an imbalance, an electric field will be created that can be measured. This electric field can act across a distance to interact with other objects. An electrostatic potential may be developed by an object due to tribocharging or electrostatic induction.

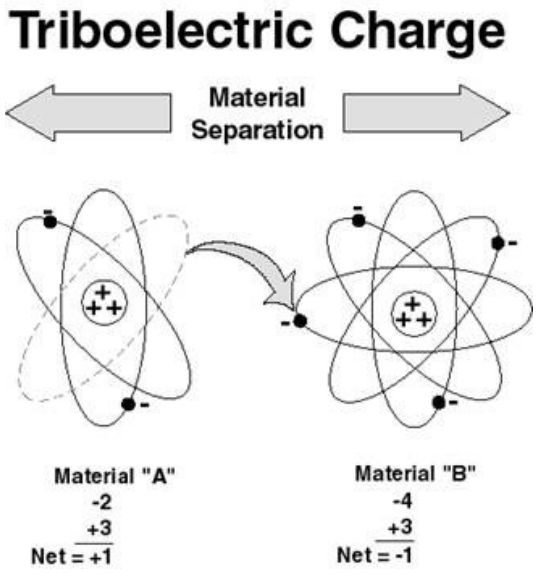

Figure 1: Principle of triboelectric charging [1].

Triboelectric charging is the process of creating electrostatic charges by contact and separation of materials. The electrostatic discharge event created by tribocharging is limited by the accumulated charge, area of contact, speed of separation and relative humidity. Electrostatic induction is seen when objects of different electric potentials discharge their accumulated charge by grounding.

ESD is one of the primary causes of failure in electronic devices [2], [3]. Failures attributed to ESD are of two types. Soft failures are malfunctions in semiconductor devices leading to a temporary loss in functionality (memory resets) while being able to function and perform the assigned task. Catastrophic failure occurs when the device that is exposed to an ESD event no longer functions. In such cases, it leads to failures such as oxide failure, melting of metallic contacts and metallization layers.

Any electronic device without enough ESD protection run the risk of being damaged during normal operation. It has been noted that on an average the component manufactures report 16 – 22% product loss due to ESD events. Whereas, end users report an average of 27 – 33% product loss due to ESD events [4]. As such, it can be inferred that a large percentage of product loss can be attributed to ESD even with extensive efforts to mitigate such losses. This outlines the importance of understanding ESD and creating adequate protection measures.

Table 1 Informal summary of static losses [4].

Description	Min. Loss	Max. Loss	Est. Avg. Loss
Component manufacturers	4%	97%	16 – 22%
Subcontractors	3%	70%	9 – 15%
Contractors	2%	35%	8 – 14%
User	5%	70%	27 – 33%

Damage due to ESD can occur at any anytime of the product life cycle of a device due to improper handling. ESD events may limit the reliability and life of a device leading to losses for both the manufactures and the end users. As seen from Table 1, the reliability of a device can be substantially increased by limiting device failure due to ESD events.

B. HIGH CURRENT TRANSIENT v/s NORMAL DC OPERATION

An ESD or a transient event is a momentary burst of energy that can occur during the normal operation of a device due to multiple factors. During an ESD event, a large amount of voltage drives a large amount of current through a device in a very short period. Such transient events stress a device much beyond its tolerance capabilities. The human body model (HBM) is an example of such a transient event. HBM transient events typically introduce 1.5 kV of voltage and 1.33 A of current into a circuit under a duration of 100 ns. This is a very large burst of energy for a small DC device such as an op-amp to dissipate. To gain perspective, an op-amp has a maximum input voltage rating of 18 – 22 V and a maximum input current rating of a few hundred nano – amperes. Therefore, under normal operating conditions an op-amp cannot handle such high voltage and current. Even then, small DC circuits are still expected to handle high current transient events for the sake of reliability.

These devices are made capable of handling transient events using various transient suppression circuits. The simplest of these transient suppression circuits make use of a zener diode in reverse bias. The zener diode when used as a transient suppression device has a high impedance during normal circuit operating conditions. When a transient event increases the voltage in the circuit above the reverse breakdown voltage of the zener diode, it clamps onto the high transient voltage allowing it to dissipate into the ground thereby protecting the device.

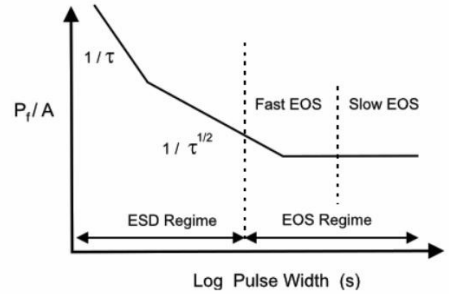

Figure 2 Wunsch – Bell curve [5].

As evident from figure 2, every DC circuit can handle such large amounts of voltage and current for a very small duration of time. The power to failure is dependent on the pulse width of the transient event and the thermal diffusion time of the semiconductor device. As the magnitude of the power to failure decreases with respect to the increment in the pulse width, the time to failure of the device increases. As the pulse width of the transient becomes comparable to the thermal diffusion time, failure due to ESD transitions to failure due Electrical overstress (EOS). Different types of ESD protection circuits can be used to increase the reliability of devices. A trade – off in on – chip area to incorporate a diode and an ESD cell is typically used to protect a device from transient event. However, only increasing the active area of these devices to handle the increased current is not a favorable approach as it is detrimental to the operating speed of the device.

C. ESD PROTECTION CIRCUITS

Protection against transient ESD events is a necessary precaution undertaken when manufacturing ICs. As such, a considerable on-chip area is reserved for ESD protection circuits [6]. Improper protection schemes have a negative impact on the reliability of the device. As a result, a need arose for on-chip ESD protection schemes that had minimal effect on the performance of the device [7], [8]. These protection schemes are primarily based on layout optimizations. Few instances of device area optimization were reported [9]. An ESD protection circuit works based on the principle of an ESD protection window. A protection window is a range of voltage which lies between the turn – on voltage of the device and its failure voltage. A protection scheme aims to trigger the ESD circuit within this voltage range for optimum protection. Figure 3 shows an example ESD protection window.

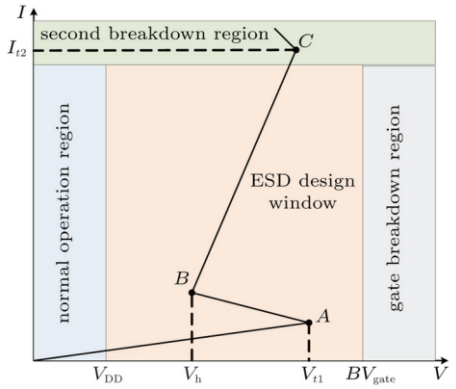

Figure 3 ESD protection window [10].

In the above figure, V_{DD} denotes the maximum limit of the voltage during normal operation of the internal circuitry. BV_{gate} denotes the maximum failure voltage for the device and its protection circuit. Points A and B lie on the IV curve of the ESD protection device. The optimal ESD protection window in this example is shaded in pink. This shaded region denotes that the ESD protect device turns on and sinks the transient current before the input voltage can damage the device permanently.

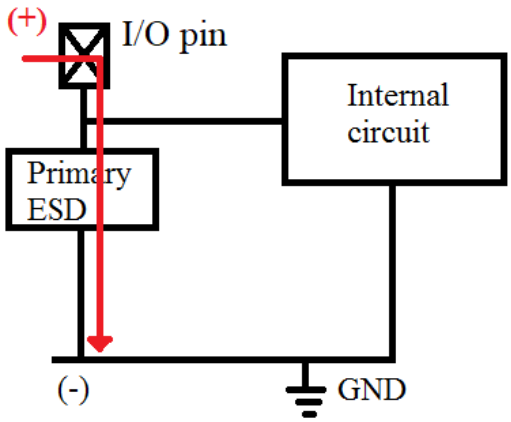

Figure 4 A sample ESD protection circuit.

An ESD protection circuit has multiple configurations. Rail based, and pad based ESD protections schemes are some of the common forms of ESD protection. A sample ESD

protection circuit is shown in figure 4. The ESD cell connected with the I/O pin redirects the transient current to ground thereby protecting the internal circuits. An understanding of the ESD protection window and protection schemes are important in designing an apt ESD protection circuit.

D. SEMICONDUCTOR INSTABILITY

Unprotected semiconductor devices are damaged after an ESD event. It is worth to note the ESD affects semiconductor devices. Two of the most common elements of any semiconductor device are resistors and Bipolar junction transistors (BJT). A resistive element is useful in limiting the current and dropping the voltage in a circuit. Similar concept is utilized in semiconductor technology using thin film resistors and diffused resistors. BJTs appear in CMOS circuits as parasitic devices.

Thin film resistors when exposed to ESD can be damaged because of self-heating due to high current density [11]. Diffused resistors in semiconductor devices show a different I-V curve as seen from Figure 5.

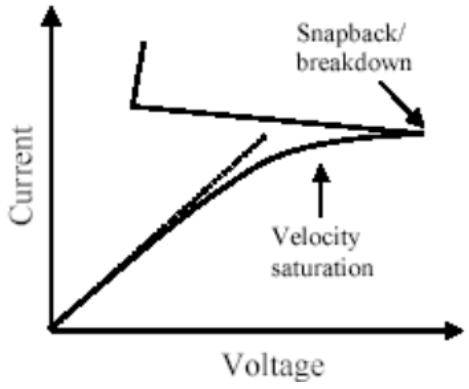

Figure 5 I-V behavior of a diffused resistor [11].

For a large input voltage i.e., when the applied electric field is larger than the critical electric field of the semiconductor material, there is an induced mobility degradation for electrons. This leads to a velocity saturation of the electrons thereby saturating the current at high input voltages. If the input bias is further increased, it leads to thermal failure. In the case of ESD protection, diffused resistors are preferred over thin film resistors due to their large current handling capability. In CMOS devices, ESD can cause the parasitic BJT to turn on due to impact ionization.

E. CHARACTERIZATION TECHNIQUES

DC characterization is not preferred to characterize an ESD event as they can cause severe self-heating issues. TLP technique allows for the detailed characterization of the device under test (DUT). It provides quasi-static current-voltage characteristics that show the behaviors of the device under test. Figure 6 shows the setup of a basic TLP system [12]. The TLP system uses a specific sequence to measure the characteristics of a device. Initially a transmission line is charged to a predetermined voltage level and the switch SW in figure 2 is closed creating a TLP pulse. The generated pulse travels through the attenuator and the coaxial cable to reach the device under test. The attenuator is used so that the reflected pulse does not stress the DUT repeatedly. The pulses when studied with the help of the oscilloscope allows the determination of the electrical characteristics of the DUT under ESD stress. The pulse used in characterizing the ESD event usually has a time period of a few nanoseconds to hundred nanoseconds. This is one of the major reasons to use pulsed measurement techniques to characterize the transient response during an ESD event.

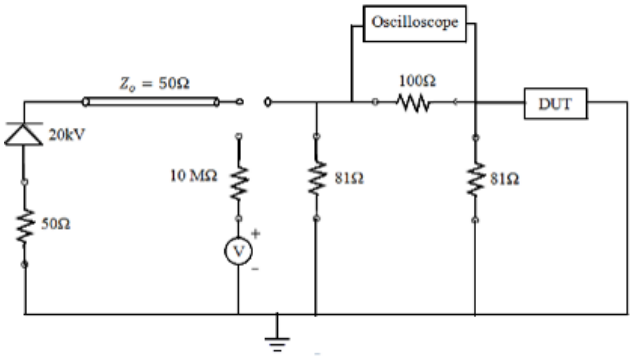

Figure 6: A basic TLP System [12].

Square waves are typically preferred to measure the current and voltage across the device under test. The width of the test pulse is determined by the length of the transmission line. As such, the pulse width and the amplitude of the input voltage to the device can be controlled by physical length of the transmission line and the initial voltage applied on the line. Thus, depending on the type of input pulse, various models such as HBM and CDM can be tested. TLP systems that use standard 100 ns pulses can be used to test HBM model whereas very fast TLP (VFTLP) systems that use 1.25 ns pulses can test CDM model [13].

The TLP system by itself does not recreate any real-world environment. Instead a TLP system can be used to transfer adequate amount of charge as per the standards pertaining to any of the ESD models thereby corelating to real world ESD events [13]. The ESD tests performed on the DUT allow for the classification of the device based on the outcome of the ESD test. Such test provides a means to record the failure level of a device that has been exposed to an ESD event. A TLP test differs from an ESD test. The device when stressed using TLP techniques not only provides a failure level but it also characterizes the DUT. A device characterized through TLP techniques provide data pertaining to its turn on time, snapback voltage and performance changes with time. A standard flowchart is seen in figure 7 representing the data collection method used in a TLP measurement [12], [14].

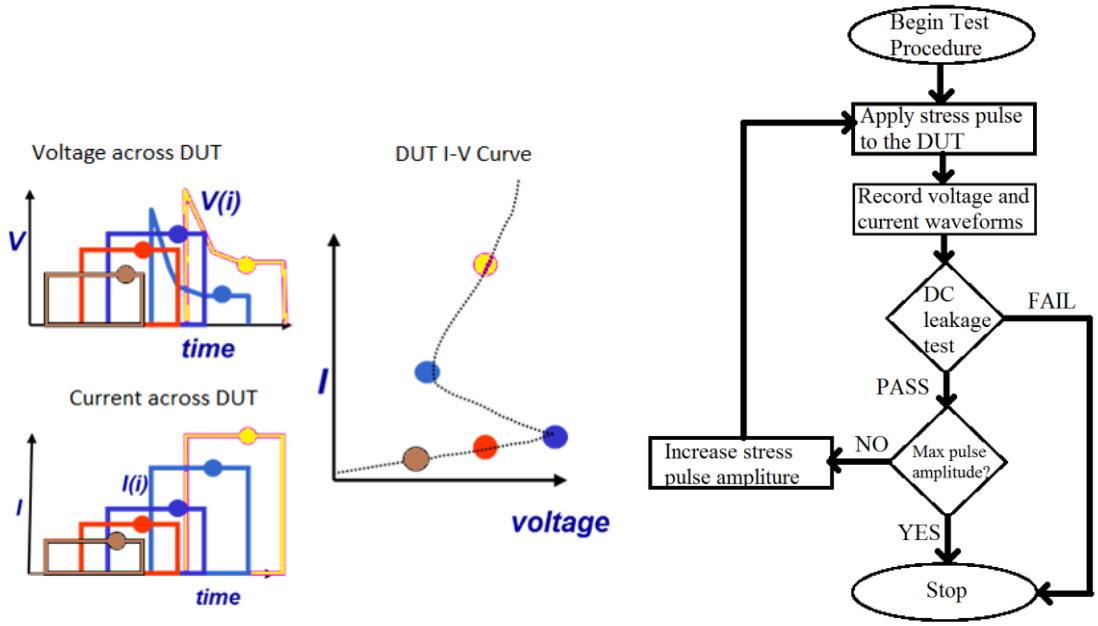

Figure 7 Data collection method used in a TLP characterization [12], [14].

F. FIGURES OF MERIT

Electrical characterization of devices through transient events result in current-voltage plots that provide detailed behavior of the device under test. Triggering current (I_{t1}), triggering voltage (V_{t1}), failure current (I_{t2}) and secondary breakdown voltage (V_{t2}), holding voltage (V_h) and on resistance are the main parameters of interest in a transient I-V characteristic of a device. Device failure point is determined by the shift of the leakage current observed from the device. An example of a snapback curve and the corresponding leakage current obtained from a TLP test is shown in figure 8.

The snapback curve shows the triggering and failure currents, voltages, the holding voltage and the ON resistance. The device under test when in the snapback mode operates as a voltage-controlled switch with a resistive load. The turn on of the device is described by parameters V_{t1} and I_{t1} that are also known as the critical triggering voltage and triggering current respectively. The triggering voltage and current are important parameters as they are critical in

providing the protection window that guarantees latch-up prevention during the normal circuit operation.

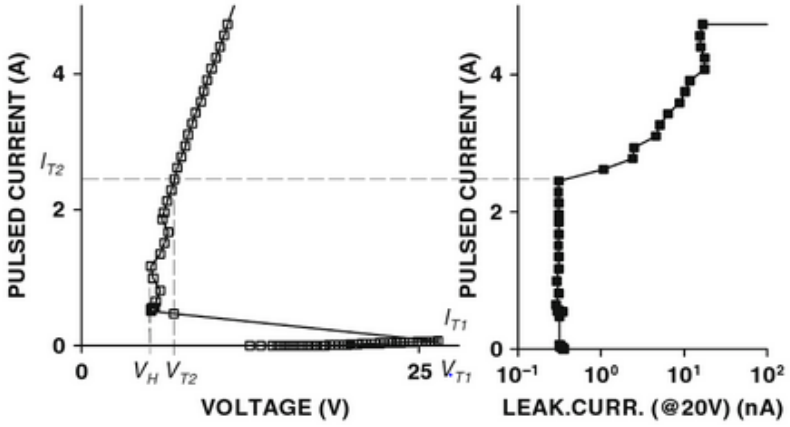

Figure 8: Major figures of merit indicated on a typical TLP snapback curve [15].

The holding voltage is another important figure of merit. The holding voltage of a device is determined by its load resistance and snapback voltage. At the holding voltage the device turns on to a high current state. The device then provides an ON resistance due to the positive feedback by the avalanche process. A saturation region is setup within the device that determines the voltage waveform at high current levels. The physical limit of the device is denoted by the I_{t2} and V_{t2}. At this point the device operation results in irreversible damage in the device structure. Parameters I_{t2} and V_{t2} are not readily deduced from the snapback curve as the curve may keep trend even after the failure of the device. The secondary breakdown points are usually determined by monitoring the leakage current of the device as seen in figure 8. The failure limit is set monitoring the leakage current till there is an order of magnitude increase from the nominal value.

II. IC AND SYSTEM LEVEL ESD PROTECTION

A. ESD MODELS AND STANDARDS USED

Innovations in ESD protection circuits began since the 1970s when methods developed to reduce gate – oxide stress in thin gate oxide FETs which were used in highly integrated ICs [16], [17]. IC level ESD protections are used to shield the ICs from ESD events that may occur during the manufacturing process. IC level transient events can be emulated using three models. The human body model (HBM) is used to emulate the ESD event that occurs due to handling of the ICs by human workers. The machine model (MM) is used to emulate ESD events that occur due to automated handling. Charged device model (CDM) emulates ESD events due to charging/discharging of an IC. IC level ESD protection is meant to protect the device during the manufacturing process in a factory. It is inadequate for end user environments. System level ESD protection circuits are used to protect a device during real world applications. IEC61000 – 4 – 2 is an example of system level ESD model. System level ESD protection requires the protection scheme to withstand and dispatch much larger amounts of current than the IC level protection schemes. IEC ESD model encompasses protection of multiple devices within a system. These parameters/benchmarks are known as standards and have a wide range of topics covered under them with an attention to details. Standards help in assuring consistent ESD protection. In addition, standards help in developing, implementing, auditing and certifying ESD procedures.

Human Body Model

The circuit consists of a charging capacitor, a contact resistance between a charged body and the DUT. The HBM standard to simulate a charged human body handling an IC. The equivalent electric circuit consists of a 100 pF capacitor and a 1500 Ω resistor which forms the

discharge path. The effective inductance of the discharge path is also modeled in the circuit shown in figure 9. HBM is differentiated from the other models by its characteristically longer pulse. The HBM model uses a pulse that has a rise time of 5 – 10 ns and a decay time of approximately 150 ns.

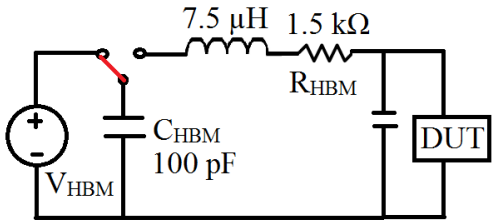

Figure 9: Equivalent electrical circuit for HBM [18].

Machine Model

MM event, which represents the ESD event due to mechanical arm's handling. Even though MM is different from HBM, their discharge processes are similar. The circuit varies from figure 9 with respect to the value of the charging capacitor and resistance of the discharge path. The charging capacitor has a capacitance of 200 pF. Machine model recreates the electrical interaction between a charged conductive surface and a device. The capacitor represents the charged conductive material such as a metallic arm of an assembly line. An arc event typically has a low resistance value. Therefore, the MM has a faster response than the HBM.

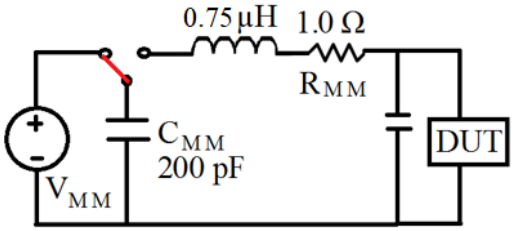

Figure 10: Equivalent electrical circuit for MM [18].

The MM has a significantly higher current rating than HBM event. Standardization of MM is difficult compared to HBM as the parasitic capacitance and inductance of the test equipment and the impedance of the DUT may change the current waveform. This similarity in the discharge process leads to a similarity in the failure signatures for the MM and HBM events.

Charged Device Model

CDM is a test based on a single pin of a device. The MM and HBM involves two separate pins on the module. As such, the MM and HBM events discharge a pulse into one of the pins with another pin grounded and all other pins left floating. In the CDM a chip is charged and then discharged to ground out of a single pin. Discharging of the current takes place through an electrical contact that mimics the contact between the pin of a device and the metallic handler of the assembly line.

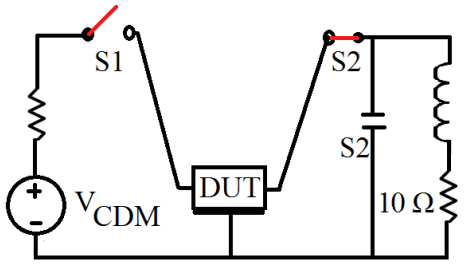

Figure 11: Equivalent electrical circuit for CDM [18].

As seen from figure 12, the CDM pulse has a very short time interval and a very high current. The CDM discharge event occurs under 5 ns with a rise time of 250 ps. Since the waveform of CDM event is different from HBM and MM the failure mode is also different. Figure 12 shows a comparison between the waveforms of HBM, MM and CDM.

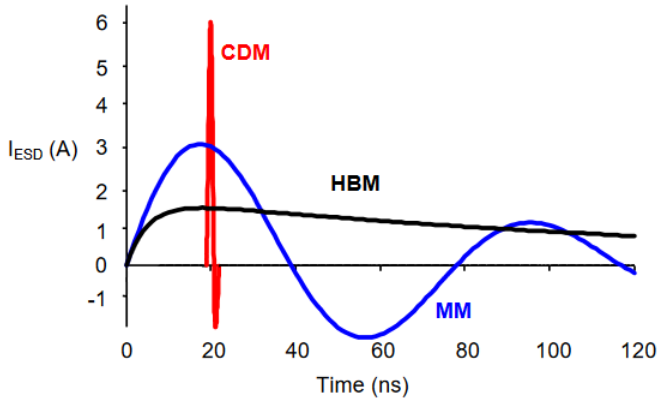

Figure 12: Idealized current waveforms for HBM, MM and CDM events [18].

System-Level ESD Protection

IEC 61000 – 4 – 2 is the system level ESD protection standard for normal application and ISO 10605 is the system level ESD protection standard for automotive applications. The IEC standard replicates the effect of a charged human discharging to a system in an end user environment without taking any precaution to reduce ESD stress to the system [20]. The IEC standard is subdivided into contact and air discharge. Figure 13 shows the simulation circuit and the pulse waveform for the IEC standard.

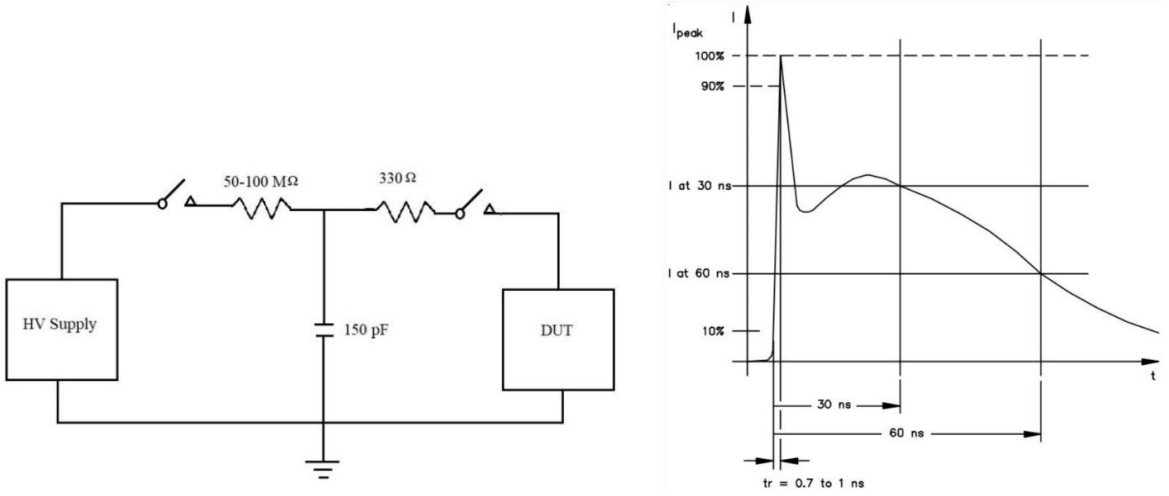

Figure 13: Equivalent electrical circuit and pulse waveform for IEC 61000 – 4 – 2 [19].

The ISO 10605 is derived from the IEC standard and is used in automotive applications. It accounts for ESD caused during vehicle assembly, ESD caused by service staff and

passengers. The ISO standard is also divided into air and direct discharge events. Test voltages range from 2 – 15 kV for direct discharge and 15 – 25 kV for air gap. Figure 14 shows the equivalent circuit for the ISO 10605 standard.

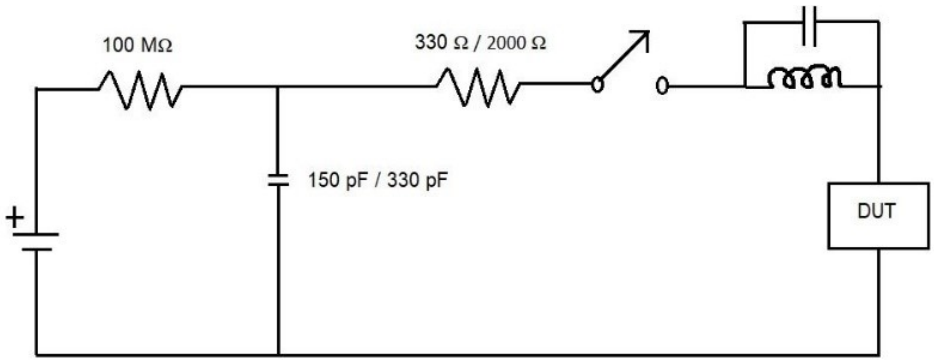

Figure 14: Equivalent electrical circuit ISO 10605 [20].

B. SYSTEM-LEVEL ESD v/s IC-LEVEL ESD PROTECTION

System level ESD and IC level ESD test are distinctly different and serves different purposes. System level ESD tests have much higher peak current than IC level ESD tests. IC level testing performs the ESD test without powering the device under test. Moreover, IC level testing assumes that there are no external components and it does not address soft failures. System level ESD testing assures the robustness of the entire system. It is mainly carried out by powering the DUT. The robustness of a system level testing accounts for all the components within the system. Both hard and soft failures are scrutinized when performing the system level ESD test. Table 2 outlines the major differences between system level and IC level ESD testing.

Table 2 IC level v/s IEC system level ESD models [17].

	HBM	MM	CDM	IEC 61000 – 4 – 2
Test Levels (V)	500 to 2000	100 to 200	250 to 2000	2000 to 15000
Pulse Width (ns)	~150	~80	~1	~150
Peak Current at Applied 2 kV (APK)	1 .33	—	~5	7 .5
Rise Time	25 ns	—	< 400 ps	< 1 ns
Number of Voltage Strikes	2	2	2	20

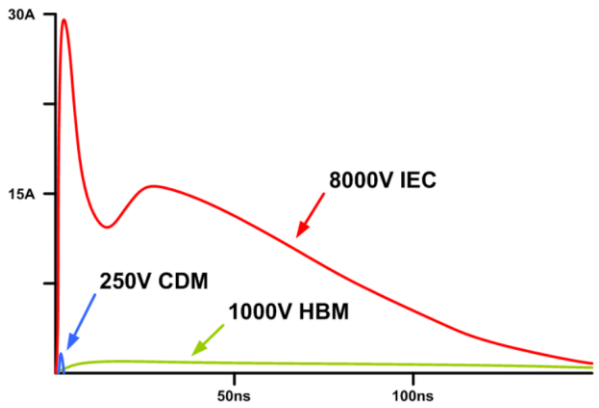

Figure 15: Standard waveforms for HBM, CDM and IEC discharge pulses [18].

Figure 15 shows the comparison between standard discharge pulses for HBM, CDM and IEC discharge pulses. An HBM current waveform has a rise time between 2 ns and 10 ns whereas the CDM pulse is quicker with a rise time of 50 ps to 500 ps. The IEC pulse is different from HBM and CDM pulses. The initial pulse in an IEC waveform has a rise time of 0.6 ns to 1ns. In most IEC ESD protection devices, the turn on response to an IEC discharge is based on the rise time of the initial pulse. Another major difference in an IEC discharge event is that the

energy involved is much higher than IC level ESD event. In addition, the frequency spectrum involved is different for a system level transient event. An IEC waveform can include both low and high frequency components. In short, IEC ESD protection circuits should be able to sink very high energy levels at faster transients that have higher peak currents than component level ESD events.

C. DESIGN CHALLENGES

Advancement of semiconductor technology through scaling has inadvertently caused deep impact on ESD protection in high – speed circuits. When the oxide thickness is decreased for better scaling of an IC, the gate – oxide breakdown of the MOSFET is also reduced, leading to lower ESD tolerance in devices. Constraints in the on – chip area limits the current shunting capability of power clamping and ESD protection circuits. As metal interconnects are made thinner to reduce parasitic capacitance, the failure current noticeably decreases during an ESD event [21].

Package scaling introduces another constraint for developing ESD protection devices. A significant increase in the peak ESD current is observed as the magnitude of the stored charge increases with total pin count in an IC [22]. Another constraint in designing ESD protection devices is the total capacitance at any I/O pin. To achieve a high data rate at any I/O pin, the allowance for capacitance is reduced below 200fF [23].

Parasitic bipolar devices in CMOS devices can create silicon controlled rectifiers (SCR). Triggering of these parasitic devices can cause latch – up. When the SCR is latched, there is a low impedance path between the positive to the negative supply. Generally, SCR's do not respond to transient events, however, scaling improves the frequency response of the parasitic components. As a result, ESD events can lead to latch – up issues [24].

Another design constraint is including effective shielding to prevent coupling issues due to indirect ESD through electromagnetic radiation. Coupling issues are broadly classified into conduction and radiation coupling [25]. Conduction coupling is caused due to parasitic elements like resistance, capacitance and inductance when the ESD current flows on the enclosure. Radiation coupling occurs when the electromagnetic field produced by an ESD event interacts with a device.

The sudden change in current per unit time during an ESD event can cause an inductive drop at the inductive element formed by the lead wires between the chip and the lead carrier of the packaging. This inductive drop causes an effect called ground bounce where the local ground is raised above the actual ground. This is another design constraint. The choice between rail – based and pad – based protection scheme is the major design challenge while designing ESD protection.

III. ESD PROTECTION IN HIGH-SPEED INTERFACE ICs

A. HISTORY AND BACKGROUND OF INTERFACE IC

Interface ICs were developed to bridge communication between two systems or parts of systems that are incompatible with each other. Initially, interface between systems were achieved using serial and parallel ports. The development of universal serial bus (USB) was started in 1994 to meet the ever – increasing requirement for faster communication between devices. USB technology was first marketed by Intel in 1995. USB was developed with the intention to simplify and improve the communication and connection between two systems.

Each generation of USB used different types of interface ICs. USB 2.0 utilized the high-speed inter-chip (HSIC) whereas USB 3.0 switched to superspeed inter-chip (SSIC) technologies. Alternatives to USB include FireWire, Ethernet, Music Instrument Digital Interface (MIDI), Serial Advanced Technology Attachment (SATA) and Thunderbolt. The common factor of all these high-speed interface technologies is the various interface ICs that are used as microcontrollers. With each generation of interfaces aiming for higher operating speeds, ESD protection becomes a major design challenge.

B. OVERVIEW OF ESD PROTECTION IN HIGH SPEED CIRCUITS

The IEC standard 61000-4-2 is the benchmark when ensuring system level ESD protection in interface ICs. During the system level ESD test, the device under test (DUT) is exposed to both contact and air gap discharges. Contact discharge may be used to stress the conductive surfaces of the system such as the metal casing or the metal connectors leading to the interface ICs. Air gap testing is conducted over likely ESD paths such as the seams of the casing. Test voltages range from 2-8 kV for direct discharge and 2-15 kV for air gap [17].

High-Speed Circuit Requirements

High-speed circuit is the label given to a circuit when it is expected to work much faster than conventional circuits. The different types of high-speed circuits are innumerous with multiple classifications within them. There are a set of characteristics that are common for all high-speed circuits. They are, low capacitance requirements at the I/O pins, small ON resistance, and bandwidth. To gain perspective, the requirements for USB 3.0 is discussed. As per the IEC standard, USB 3.0 is rated for 8kV contact discharge and 15kV airgap discharge. Capacitance shares an inverse relationship with frequency. Hence for larger capacitance the frequency is reduced thereby reducing the bandwidth. The data rate requirement for a USB 3.0 is 5Gbps with a signal frequency of 2.5GHz. Due to the higher data transfer rate compared to USB 2.0, USB 3.0 requires very low capacitance at the I/O pins [26], [27]. The maximum permissible capacitance at the I/O pins is 2pF. Similarly, USB 3.1 has a low capacitance requirement of < 0.5 pF. USB 3.0 also requires low dynamic resistance (~ <1Ω) and good clamping performance. The capacitive requirements alone at the I/O pins when compared to USB 2.0 (30-120 pF) show one of the major design challenges for ESD protection in high-speed circuits.

C. REVIEW OF ESD PROTECTION IN HIGH-SPEED CIRCUITS

Pad Based ESD Protection

Protection schemes vary in different ways to protect a device from ESD strikes. Pad based ESD protection is one such method. In this method, each input-output pad is connected to the ground through an ESD cell. Since the current discharged during an ESD event will flow directly from the input – output pad to ground it is known as a pad based ESD protection. In this type of protection method, the voltage clamp provided by the ESD cell must hold the pad voltage below the failure voltage of the devices in parallel. It is necessary that every pair of pins must

have an ESD cell between them for transferring discharges of both polarities during an ESD event. Devices that exhibit snapback behavior are usually chosen as ESD protection devices. The CMOS technology favors NMOS based devices such as gate-grounded NMOS, gate-coupled NMOS and substrate triggered NMOS. Silicon controlled rectifiers are also frequently used as protection devices as they have a very high current handling capability. Figure 16 shows the discharge path of the ESD current.

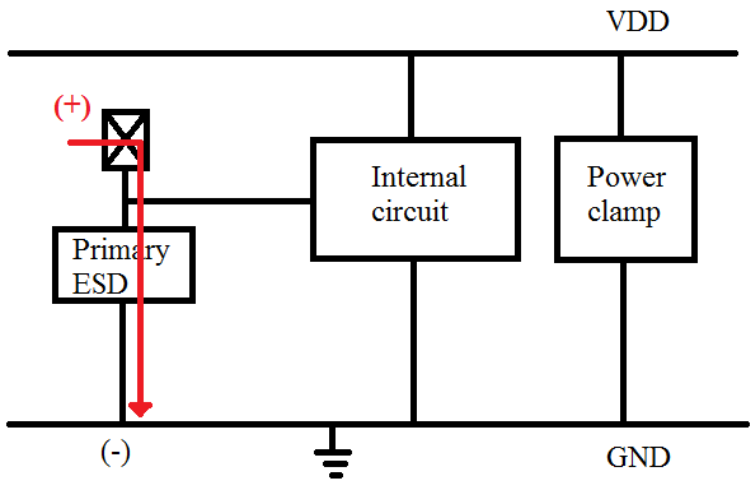

Figure 16 Simplified pad based ESD protection scheme [18].

Rail Based ESD Protection

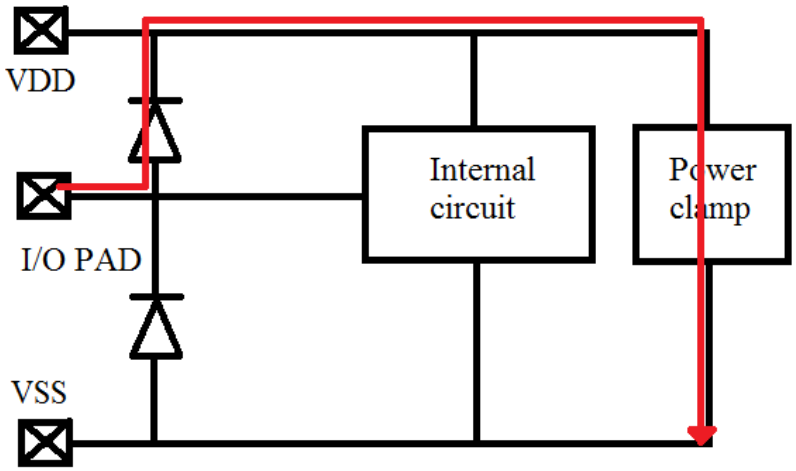

Figure 1 Simplified rail based ESD protection scheme [18].

The rail-based protection scheme employs forward biased diodes to direct the discharge current to the ground through the ESD protection cell. Unlike the pad-based scheme there is a common ESD cell which is used to handle the ESD current. When a positive strike is induced at the input pad there exists no direct current path as in the pad-based scheme. The discharge current instead is directed by a small forward diode through the V_{DD} rail. The discharge current passes through the V_{DD} rail to reach the primary ESD cell through which it passes to the ground. Due to the discharge path, the forward diode and the ESD cell are required to have a voltage limiting criterion in order to protect the internal circuitry. For a negative pulse with respect to the ground, the current path includes the lower diode. The effectiveness of the rail-based system scheme is dependent on the placement of the power supply clamps. By effectively distributing power supply clams and accurately estimating the bus resistance from the input-output pins it is possible to provide an effective ESD protection to the device.

Pad-based v/s Rail-based Protection

Pad based and rail based ESD protections are the most used types of protection circuits. Both pad-based and rail-based protection has its own merits and demerits. Pad based systems are straightforward as the protection cell is the only device that is engaged during an ESD strike. Due to the current discharge path it is possible to self-contain the ESD protection cell within the input-output pins. Since there are no diodes between the pins and the V_{DD}-power rail it is suitable for fail safe applications.

As diodes are simple structures, rail-based systems can be easily created using many of the process variations. Such conventional devices are easy to scale and thus enables the protection structure to be upgraded to a more advanced technology. However, as the number of

pins increase the number of power clamps also must be increased. This approach requires additional area on the chip causing large leakage currents. Moreover, power clamps tend to be falsely triggered and thus calls for increased engineering effort to mitigate it. Unlike the pad-based structure this structure cannot be used in fail safe applications due to power sequencing issues. Choosing between the two strategies require deliberation and is dependent on the type of application in which they are expected to be used.

D. TRADITIONAL v/s PROPOSED ESD PROTECTION STRUCTURE

Traditional ESD Protection Devices

Parameters required for creating an ESD protection cell is dependent on the type of application involved. Typical protection circuits involve devices such as NMOS, SCRs, and diodes. Each of these devices have their merits and demerits. The SCR devices have low holding voltage that are desirable but have modest switching voltage and turn on speed that needs to be customized for each improvement in processing technologies [28]. The advancements in NMOS devices such as shallower junctions, thin gate oxides and lightly doped drains have had a negative impact on NMOS ESD protection solutions [29]. Each device requires a primary set of survivability specifications such as peak pulse current, ESD rating, transient clamping voltage and ESD clamping voltage [28]. These parameters are further dependent in the intended operation of the pin that is protected by the ESD protection circuit.

Forward diodes placed in series with the input-output pins are used to handle the transient current during a current surge [30]. Protection circuits utilize the unidirectional property of diodes to redirect the ESD current to the primary protection cell. There are multiple types of primary protection cells available, an example is the gate-grounded n-channel metal oxide semiconductor with minimal gate capacitance. Capacitance is a major factor limiting the

performance of a high-speed circuit. Capacitive elements included in a circuit causes a lag in signal propagation. The lag in signal propagation is mainly due to the time required to charge and discharge the capacitors in an IC. Capacitive elements that are formed unintentionally during an IC manufacturing process are known as parasitic capacitors. Parasitic capacitors add to the existing capacitive elements in a circuit to form substantial delays in signal propagation.

Initial work on improving ESD protection circuits was carried out by modifying the layout of the forward diodes [31], [32], [33]. Diode layouts were modified to reduce the formation of parasitic capacitors. Layout optimization of diodes was performed by stacking the diodes for optimum performance. Diode stacks are a combination of stacked diodes that pass the required ESD current. Smaller diodes that passes the required ESD current introduced less parasitic capacitance than a single large diode. Bulky protection circuits resulted in higher capacitance across the I/O pins leading to a drop in the operating speed. Improvements in protection schemes for high-speed ICs depended on reducing the size of the forward diode. The goal of reducing the size of the forward diode is to reduce the total capacitance to facilitate higher operating speeds.

Silicon controlled rectifiers (SCR) are usually preferred for ESD protection. Due to their low holding voltage and small area. The power dissipated by an SCR device is significantly lower than a MOS, BJT, diode or oxide-based device [34]. These enable the SCR devices to sustain much higher ESD stress levels making them one of the most common ESD protection structures. Since the SCR based devices gained popularity there are many variants that are used for a variety of applications. Few examples of these SCR devices are, the lateral SCR device, hot carrier triggered SCR device, low voltage triggering SCR, gate coupled low voltage triggering SCR and gate grounded N-MOS triggered SCR [34].

A Novel Approach

High speed ICs have stringent pin requirements and as a result the capacitance, leakage current, protection window and device area of the protection scheme should be well defined. Currently, SCRs are preferred for area efficient primary IEC ESD cells. Improving the system level on-chip protection for these structures has been focused on streamlining their device parameters such as V_h, I_{t2} and V_{t1}. The SCR structures are preferred as they have higher I_{t2}. However, its low holding voltage and increased breakdown voltage under strong injection conditions create concerns during normal operation and transient events.

Furthermore, substantial progress in the automotive and medical industry demanded on-chip protection for system level ESD events. This growing trend requires IC manufactures to incorporate the protection provided by traditional components such as transient suppression diodes into an IC. As seen earlier, system level ESD protection requires large amounts of current to be dissipated by the limited on-chip area. Usual protection strategies such as substrate SCRs and diode stacks are inadequate the handle the system level ESD events. To overcome these difficulties a new method is proposed.

In this work, we report on the benefits of using a parasitic bipolar transistor formed between the high-side diode and the substrate in rail – based structures for ESD protection [35]. A parasitic bipolar transistor forms a parallel path to conduct the transient current. This parallel path formed by the parasitic transistor works in tandem with the on-chip area allocated for current surge protection as seen in figure 18. The additional path can be configured to conduct a major portion of the transient current. By dividing the current path, it is possible to reduce the area of the on-chip protection cell. A reduction in the area allocated for ESD protection leads to a decrease in capacitance between the input-output pins. The parallel current path can be

effectively used for surge protection by optimizing its turn-on voltage. An optimum turn-on voltage for the PNP inherently present in a device can be found by modulating the device parameters. Incorporating the PNP saves area on the chip. This additional area can be used to improve the desired functionality of the IC chip.

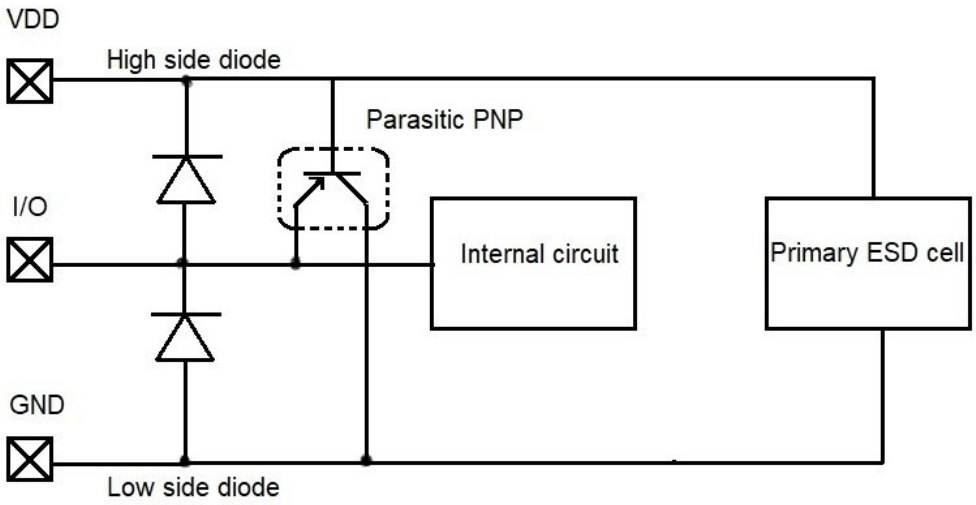

Figure 2 Rail based ESD protection with parasitic PNP [35].

IV. RAIL BASED ESD PROTECTION FOR SYSTEM LEVEL IEC

A. PROPOSED METHOD

The rail based ESD protection is usually preferred in high-speed ICs due to their low leakage current and capacitance. The additional strain introduced by the system level ESD events are to be contained by the parasitic PNP structures with large peripheries. These parasitic bipolar devices are formed in the layout as a result of the high-side diodes present in the rail-based structures. The large periphery of this parasitic PNP can be used to sink the substantial current associated with an ESD event. Figure 19 shows a common diode layout with the corresponding parasitic transistors.

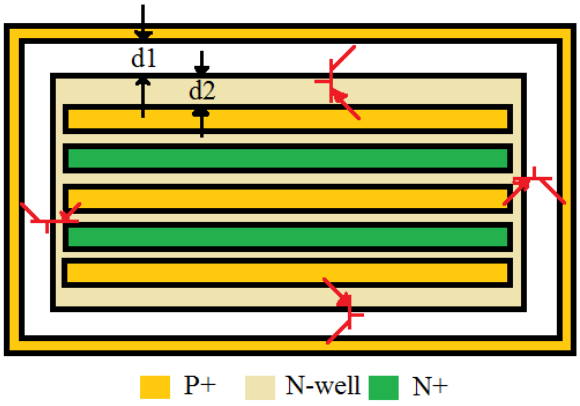

Figure 3 Sample layout for high-side diode [35].

A stripe configuration consists of a P+/N-well junction formed by alternating fingers of P+ and N+ diffusions. The active area is surrounded by a P+ isolation diffusion forming the substrate contact. It can be inferred that the stripe layout has a large device periphery. The geometrical parameters of the layout and the substrate contact dictates the electrical parameter of the diode. The parasitic bipolar transistors are represented in red as seen in the figure. The high-side diodes play an important role in ESD protection for high-speed circuits. The I/O pins of high-speed circuits are expected to have low parasitic capacitance for optimum circuit

performance. The capacitance seen at the pin of an IC is largely due to the ESD protection cell. High-side and low-side diodes contribute heavily toward the capacitance of these ESD structures. With a sound design strategy for parasitic PNP structures the area and thereby the capacitance of a primary ESD cell can be minimized. Grid or island topology is a suitable method to reduce the area of the diode while maintaining a comparable I_{t2} with respect to the finger layout. Island diodes also have the potential to provide a larger device periphery and better uniformity.

The proposed approach aims at tailoring the parasitic PNP structure to achieve proper triggering voltage and high I_{t2} with uniform turn-on characteristics. The electrical and physical characteristics of the parasitic PNP is determined by the layout of the high-side diode. The base width of the parasitic PNP is dependent on the distance between the N-well and the P-well contact (d1 in figure 19). Width of the emitter corresponds to the width of the P+ finger in the high-side diode. The variation in the type of N-well diffusion, guard ring and substrate contact determines the doping of the base in a parasitic PNP. The primary goal of this novel approach is to utilize the inherent parasitic PNP formed by the high-side diodes to create a parallel ESD discharge path. The goal is achieved by studying and modelling the characteristics of the substrate PNP structures to confine its triggering and clamping voltages within the specified ESD protection window. The parallel ESD discharge path formed by the large periphery of the high-side diode is viewed as a viable IEC ESD protection structure.

B. PRINCIPLE OF THE ESD PROTECTION WINDOW

An ESD protection window is a plot that shows the different voltage and current levels that pertain to a device detailing its optimal operating conditions, window of protecting the device from failure and internal failure. An ESD protection window allows for designing

effective triggering and clamping voltage of the protection circuit. As seen from figure 20, to ensure the turn-on of the parasitic PNP, the clamping voltage of the primary ESD protection path should be higher than the triggering voltage of parasitic PNP.

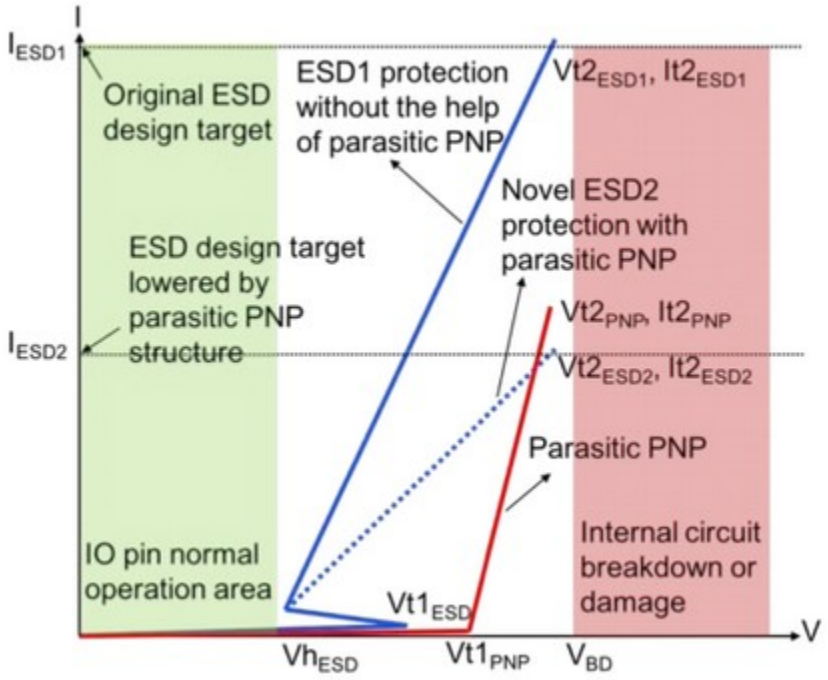

Figure 20 ESD protection window [35].

The normal operating area of the circuit is shown in green. The red area denotes the failure region for the internal circuits. The ESD protection circuit should be designed in such a way that it does not hinder the normal operation of the circuit and saves the internal circuit from failure. In conventional on-chip IEC protection circuits the dual diodes and primary ESD cell are scaled to increase the current handling capability and to reduce the ON resistance. The curve in blue shows the snapback based ESD structure used for IEC protection circuits that does not utilize the parasitic PNP structure. An 8kV primary ESD cell can take around $0.2mm^2$ in area for on-chip IEC ESD protection. It is inferred that in order to decrease the device area a different approach must be considered. By using the inherent parasitic PNP structure in high-side diodes the total ESD device area is expected to reduce. The electrical characteristics of the parasitic

PNP will be adjusted to fit the ESD protection window. The curve in red shows the characteristic non-snapback IV curve of the parasitic PNP structure. Snapback rarely occurs in PNP structures as opposed to NPN structures as its current gain is relatively lower. To effectively use the parasitic PNP structure for IEC ESD protection its current gain, uniformity and scalability needs to be improved. These improvements are brought about by optimizing the substrate contacts, diffusion type, and high-side diode layout of the parasitic PNP structure.

Device simulation is sought to help model a uniform current flow with high It_2 for the parasitic PNP to discharge the ESD current. The triggering voltage of the parasitic PNP is denoted by V_{t1PNP}. The turn-on voltage of the parasitic bipolar is required to be below the breakdown voltage of the internal circuit. The breakdown voltage of the parasitic PNP structure must be modelled with care. If the breakdown voltage is too low, then the parasitic transistor hinders the normal operation of the circuit by bleeding the base current into the substrate [36]. If the breakdown voltage exceeds the protection window, the parasitic bipolar fails to turn-on during an ESD event leading to device failure. The parasitic PNP structure shunts a significant amount of IEC ESD current without the help of any additional device area or metal interconnects leading to a reduced design target I_{ESD2}. This approach helps to significantly reduce the area of the high-side diode and the primary ESD cell.

C. PHYSICAL PARAMETERS AND FIGURES OF MERIT

Electrostatic discharge protection using the parasitic bipolar transistor was initially discussed by Avery *et al*, in 1984 [37]. The idea utilized the avalanche breakdown mechanism in a bipolar device to channel the discharge current. This idea was conceptualized by many and have been widely used since [38 – 43]. The main factor that varied between each protection scheme is the type of lateral device being used. While bipolar devices were popular it was SCRs

that were preferred [38]. The SCR device can be triggered from the OFF state to ON state by the charges injected in the base region. During an ESD event, protection schemes using SCR derives the injected charge to the base from the avalanche process. The avalanche breakdown is as a result of the reverse breakdown of junction formed by the twin wells.

Protection schemes using bipolar devices have recently been studied in detail [40]. The behavior of the lateral bipolar transistor is defined by an avalanche-injection conductivity mechanism. The mechanism is explained by the positive feedback due to the impact ionization and injection process in bipolar devices. The protection scheme described in this paper talks about an area efficient ESD protection device formed by the high-side diodes and the substrate. The high-side diodes are the diodes that are found on the pins of a high-speed IC. These diodes are used to direct the discharge current to the ground during a transient event. In order to maximize the efficiency of this proposed structure a low V_{t1} and I_{t1} is required for the parasitic bipolar transistor that is within the ESD window. A low breakdown voltage is required as the protection structure is to be turned on before the breakdown of the internal circuit. Additional parameters such as a low on resistance and high I_{t2}, V_{t2} is preferred for optimized performance of the protection circuit. As such, the simulated results support the use of the proposed structure by describing the physical parameters that are required to optimize the protection circuit.

D. ANALYSIS OF PARASITIC PNP DEVICE

In the traditional substrate bipolar device, the junction between P+ diffusion and N-well has a low breakdown voltage since the P+ diffusion region is heavily doped. But, the junction between N-well and P-substrate has high breakdown voltage since both are lightly doped. The junction between N-well and P-substrate with high breakdown voltage is disadvantageous for ESD current discharging. When a voltage is applied to the P+ diffusion in the N-well, the

emitter junction of the parasitic bipolar structure is forward biased and the junction between the well reversed biased.

When the collector-to-emitter voltage of the PNP is below the collector-to-emitter breakdown, no current flows in the structure. The resistance of the P-well holds the potential of the collector region of the PNP structure in reference to the potential applied at the P+ diffusion in the N-well. When the voltage at the emitter of the structure exceeds the emitter-to-collector breakdown voltage, many holes and electrons are generated at the emitter junction of the PNP structure. The hole current flows into the P-well through the forward biased emitter junction of the PNP structure. The electron current flows into the collector through the N-well and P-well regions. The voltage drop in the N-well region due to the electron current flow forward biases the P+/N – well junction, this creates an avalanche process leading to breakdown. Since the avalanche breakdown occurs as a result of the P+ to N-well region, a change in the length of this region leads to a change in the breakdown voltage. This change in the breakdown voltage due to the change in the base width is caused by a change in the current gain of the parasitic PNP device. The current gain of a parasitic PNP transistor and its relation to the breakdown voltage can be defined by the following expressions.

$$\beta_{DC} = \frac{D_n W_E n_{i,B}^2 N_E}{W_B D_p n_{i,E}^2 N_B}$$

$$V_{br,CEO} = \frac{V_{br,CBO}}{(\beta_{DC}+1)^{\frac{1}{m}}}$$

Where β_{DC} is the current gain, $D_n$and D_p are the electron and hole diffusion coefficient, W_E is the emitter length, W_B is the base width, $n_{i,B}, n_{i,E}$ are the electron and hole concentration at the base, emitter, N_E and N_B are the emitter and base doping respectively. $V_{br,CEO}$ and

$V_{br,CBO}$ are the common emitter and open base breakdown voltage and m is the avalanche multiplication factor. Assuming that the emitter length is kept constant, the base width and doping of the emitter and base regions control the current gain of the parasitic PNP transistor. As mentioned earlier, N-well and P-substrate has high breakdown voltage. Hence, a change in the distance between the wells introduces an increased interaction of the substrate resulting in an increased breakdown voltage. Through the expected similarity in breakdown voltages for both transient and DC characterization the simulation is validated.

E. THEORITICAL BREAKDOWN VOLTAGE CALCULATION

The mathematical expression for the avalanche breakdown voltage is dependent on the configuration type of the PNP transistor. The avalanche breakdown voltage for the common base configuration is given by the following expression.

$$BV = \frac{k_s \varepsilon_0 F_{BR}^2}{q} * (\frac{1}{N_B} + \frac{1}{N_C})$$

Where, $k_s \varepsilon_0$ is the permittivity of silicon, F_{BR}^2 is the maximum field of silicon, q is the elementary charge, N_B and N_C are the semiconductor doping in the low doped and high doped regions respectively [44]. The maximum electric field for a given semiconductor changes negligibly with respect to the background doping. For a first approximation it is assumed that the maximum field of a semiconductor is a constant value with $F_{BR\ Si}$ at 3E+5 V/cm [44].

F. SIMULATION ENVIRONMENT AND DEVICE STRUCTURES

Simulation Environment

The simulation of a parasitic bipolar device is carried out on a standard desktop computer with the help of Silvaco Atlas software version 5.22.1.R. Silvaco is a software platform that combines multiple software packages to characterize the electrical properties pertaining to a

material or a device. Silvaco software can be used to perform technology computer aided design (TCAD) simulations of semiconductor devices. The fabrication of semiconductor devices without a simulated and tested tape-out plan is expensive. Silvaco enables users to simulate and plan for tape-outs thus reducing the cost of production.

Deckbuild 3.20.2.R and Tonyplot 3.10.6.R are the software packages from Silvaco that are used to characterize the breakdown voltage and the ON resistance of a PNP. Deckbuild is a command – based software that is used to specify the material and device parameters. A code is written and compiled using Deckbuild to simulate the electrical characteristics of a parasitic bipolar device. The code used for simulation consist of the device structure, material and model definitions followed by a set of execution parameters. The execution parameter defined in the code is the vital step of the simulation. The current-voltage characteristics of the parasitic bipolar transistor is measured and saved for various changes in the device structure. Analysis of the current-voltage characteristics provide insight to the usefulness of the simulated structure as an ESD protection circuit. Tonyplot is the software package used to display the output generated by Deckbuild. Together, the Deckbuild and Tonyplot software packages are used to study the electrical characteristics of a parasitic bipolar transistor.

Device Structures

Three different devices with varying well configuration were simulated. The structures are named A-C. Each configuration is shown below with its respective doping parameters. Each set of structure is simulated for a predefined set of parameters D1-D3 and L1-L3. The distance between the collector and the junction is named D1. The emitter to junction distance is termed as D2. The base-emitter width is denoted by D3. Parameters L1-L3 stands for the collector, emitter and base widths respectively.

Structure A

Structure A is a 2D single well PNP device with 25 µm x 7µm dimension. The deck was created by modelling a parasitic PNP transistor by analyzing example files on BJT and MOSFET structures available in Silvaco repository. The substrate is doped with a uniform p-type impurity with a concentration of 5E+15 cm^{-3}. The N-well is doped at a concentration of 1E+18 cm^{-3} to form a junction. The collector and emitter are doped with p-type impurities with a concentration of 1E+19 cm^{-3} and 5E+19 cm^{-3} respectively. The base diffusion is doped with an n-type impurity with a concentration of 5E+19 cm^{-3}. The structure has a mesh of 0.3µm default spacing in x-axis, 0.2µm spacing for the junction in y-axis and 0.5-1 µm spacing for remaining points in y-axis.

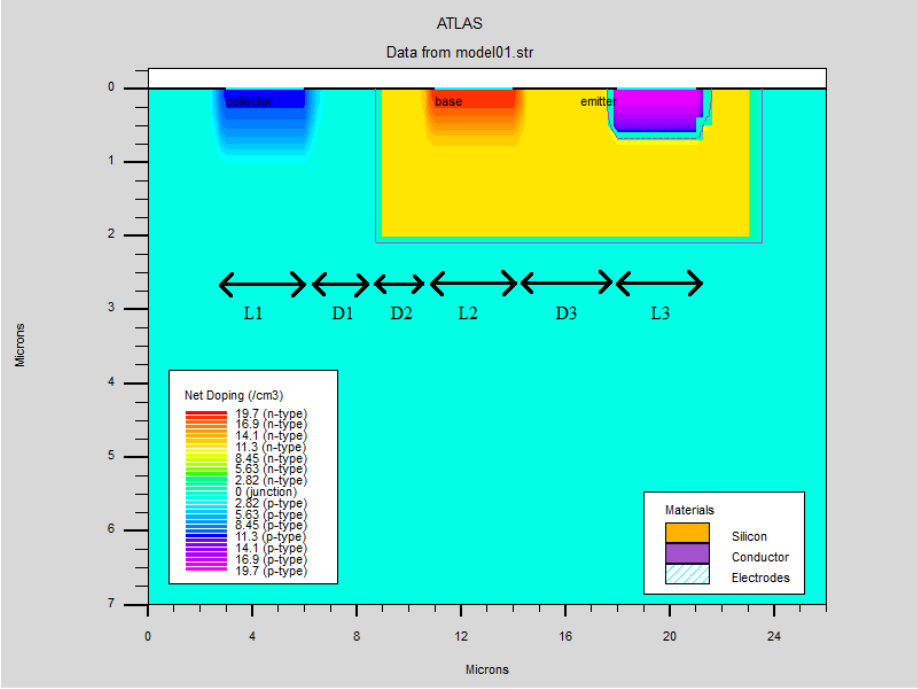

Figure 21 Device structure A.

Structure B

Structure B is a 2D twin well PNP device with 4 µm x 0.6 µm dimension. The deck was created by modelling a parasitic PNP transistor by analyzing example files on BJT and MOSFET structures available in Silvaco repository. The substrate is doped with a uniform p-type impurity with a concentration of 5E+15 cm^{-3}. The N-well and P-well are doped at a concentration of 1E+18 cm^{-3} to form a junction between the substrate and the two wells. The collector and emitter are doped with p-type impurities with a concentration of 1E+19 cm^{-3} and 5E+19 cm^{-3} respectively. The base diffusion is doped with an n-type impurity with a concentration of 5E+19 cm^{-3}. A customized mesh statement is used to help reduce the time taken to execute the code.

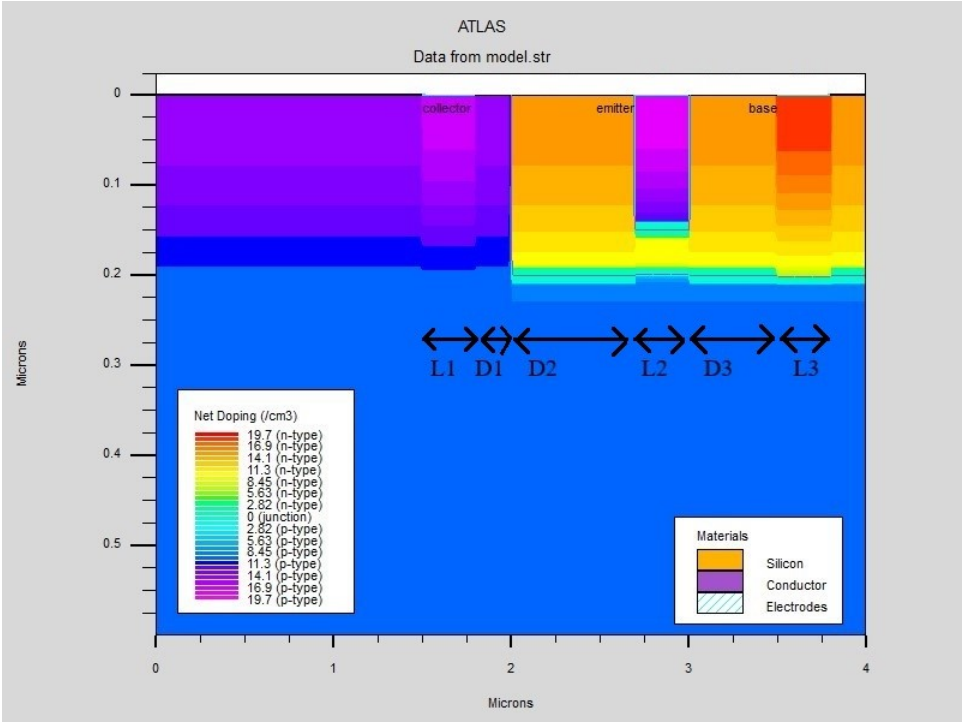

Figure 22 Device cross section of structure B.

Structure C

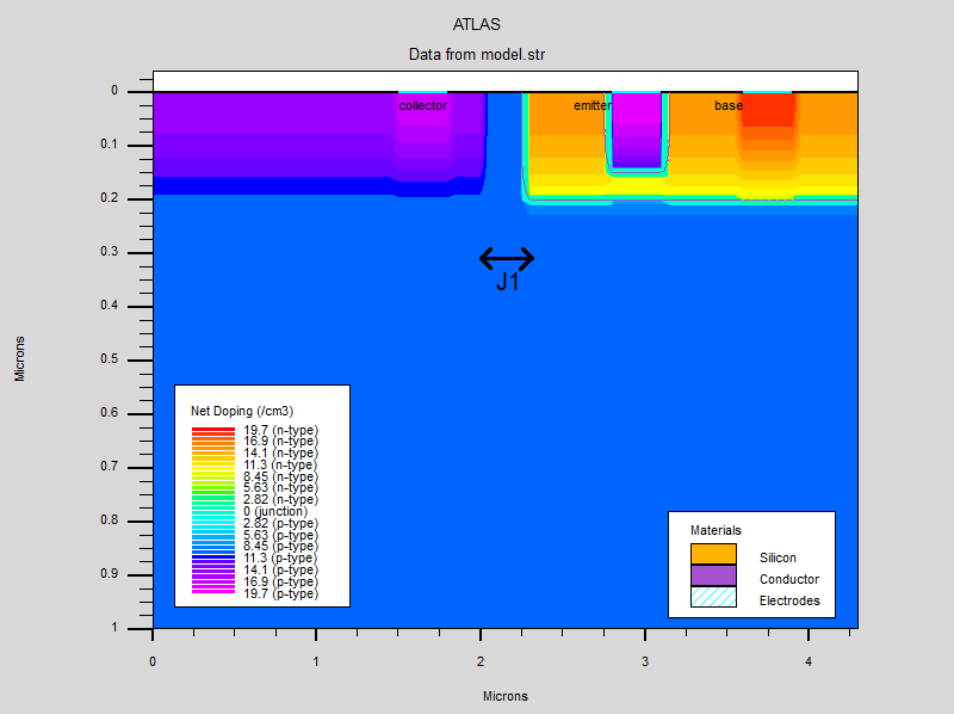

Figure 23 Device cross section of structure C.

Structure C is a modified version of structure A. The purpose of simulating this structure is to show the interaction of the substrate in the avalanche breakdown for the twin well process. The deck is a 2D twin well PNP device with 4.2 µm x 0.6 µm device dimension. A customized mesh statement is used to help reduce the time taken to execute the code.

G. PHYSICAL MODELS USED

As discussed earlier, any Silvaco code requires a mesh definition followed by doping statements, electrodes, contacts, models and execution statements. The models used in a simulation describes how the simulation deck responds to stimulus. The MODELS statement under Atlas-Silvaco has multiple parameters that define a device. BIPOLAR is one such parameter under the MODELS statement. The BIPOLAR statement includes and utilizes models such as concentration dependent mobility (CONMOB), field dependent mobility (FLDMOB), bandgap

narrowing (BGN), concentration-dependent lifetime (CONSRH) and Auger recombination (AUGER).

H. SIMULATED RESULTS

Structure A

Figure 24 is a DC breakdown voltage curve. The variations in the breakdown voltage curve is due to the changes in length from collector to junction region of the structure. The device under test is a parasitic bipolar structure formed of silicon and has different doping densities at each terminal. The breakdown voltage for each of the curves vary for changes in parameter D1 for the single well process. The on resistance of the PNP can be changed by varying the distance between the collector and the junction. Failure current (I_{t1}) and the failure voltage (V_{t1}) also varies for modulation in parameter D1. Negative resistance characteristics are not observed irrespective of the width of D1. The breakdown voltage of the device obtained from the simulations correspond with the estimated values obtained from standard models.

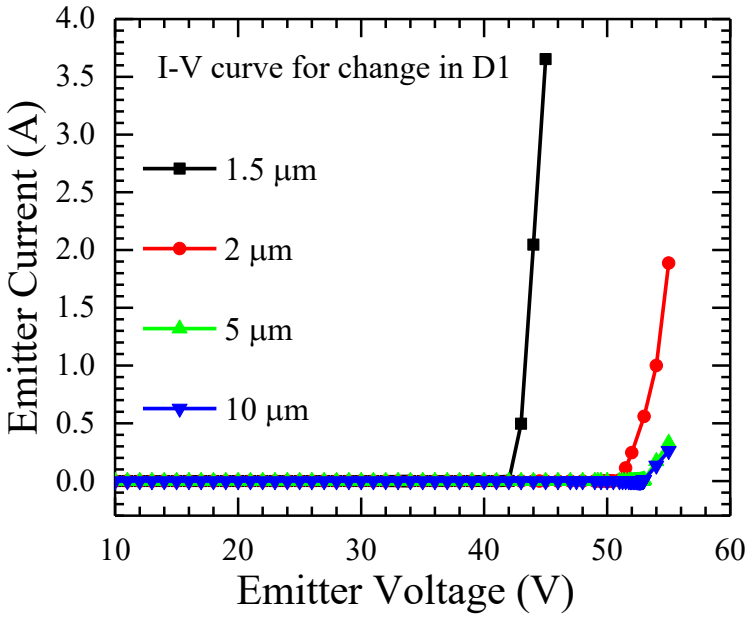

Figure 24 Breakdown voltage of substrate bipolar transistor for change in D1.

Figure 25 also represents the DC electrical characteristics of a parasitic bipolar device. The change in the breakdown voltage of the curves occurs due to the modulation of D2. The breakdown voltage characteristics is obtained for a device formed of silicon with different doping types and concentrations for each terminal. The breakdown voltage increases with an increase in length of parameter D2. Minimal change in the on resistance of the device under is observed under test conditions.

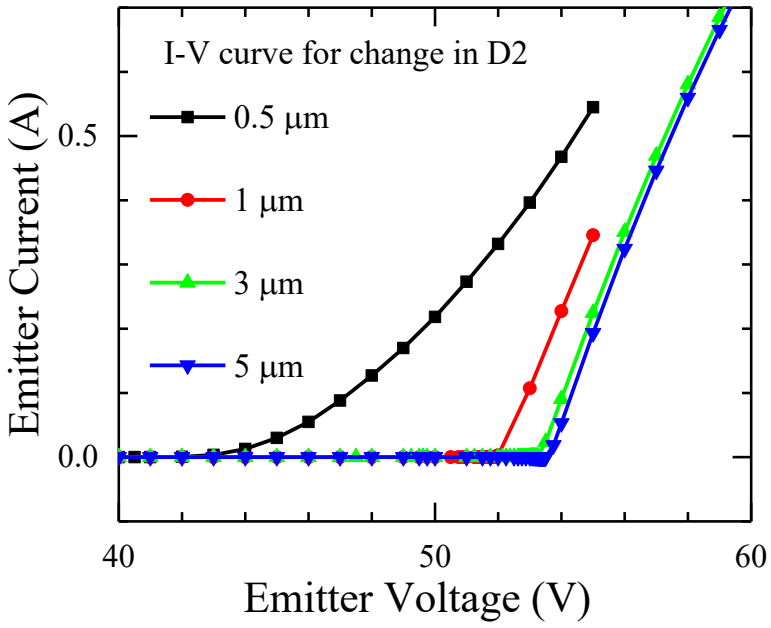

Figure 25 Change in breakdown voltages for different lengths of the junction-emitter region(D2).

Additional parameter such as D3 and L1-L3 have minimal effect on the figures of merit of the single well parasitic bipolar transistor. The total current density plot shows the forward biased emitter - base region. It also shows the reverse biased collector – base region. Most of the current is seen to flow in the regions between the collector and base. This shows that parameters D1 and D2 will affect the current flow within the parasitic transistor as seen in figure 26. Structure A is a precursor to the other two structures and is necessary for assessing the

electric characteristics of structure B and C. As such, structure A by itself is not considered for ESD protection as most processes use the twin well approach to fabricate their devices.

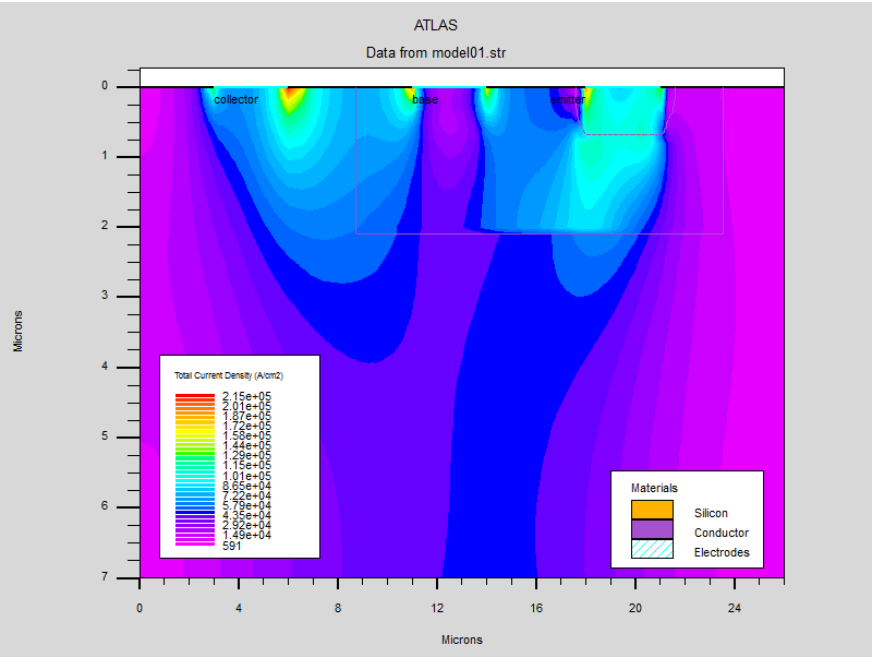

Figure 26 Total current density plot for structure A.

Structure B

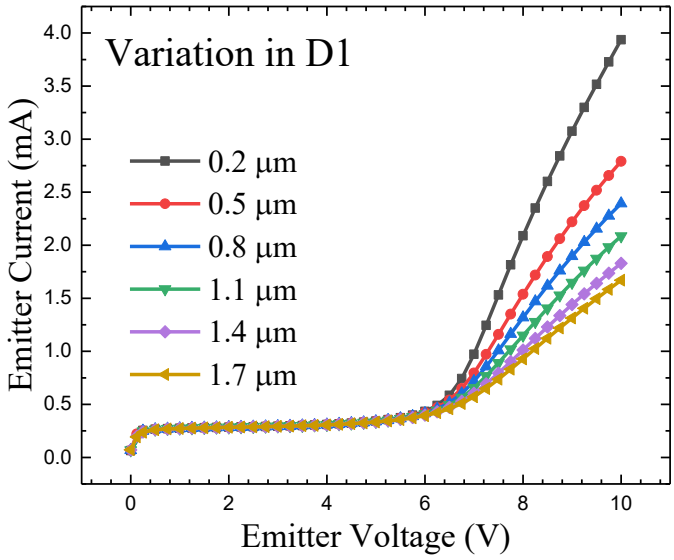

Figure 27 DC simulation of structure B by varying parameter D1.

Figure 27 is a DC breakdown voltage curve. As expected, the breakdown voltage is not sensitive to the changes in length from collector to junction region of the structure. The device under test is a parasitic bipolar structure formed of silicon and has different doping densities at each terminal. The breakdown voltage for each of the curves do not vary for changes in parameter D1. The on resistance of the PNP can be greatly changed by varying the distance between the collector and the junction. The breakdown voltage of the device obtained from the simulations correspond with the estimated values obtained from standard models.

Figure 28 shows the current density plots for changes in D1. A device with greater D1 has a wider current spread between the well junctions and the collector. This wider current spread helps for lowering the resistance between the junction and the collector leading to a lower ON resistance.

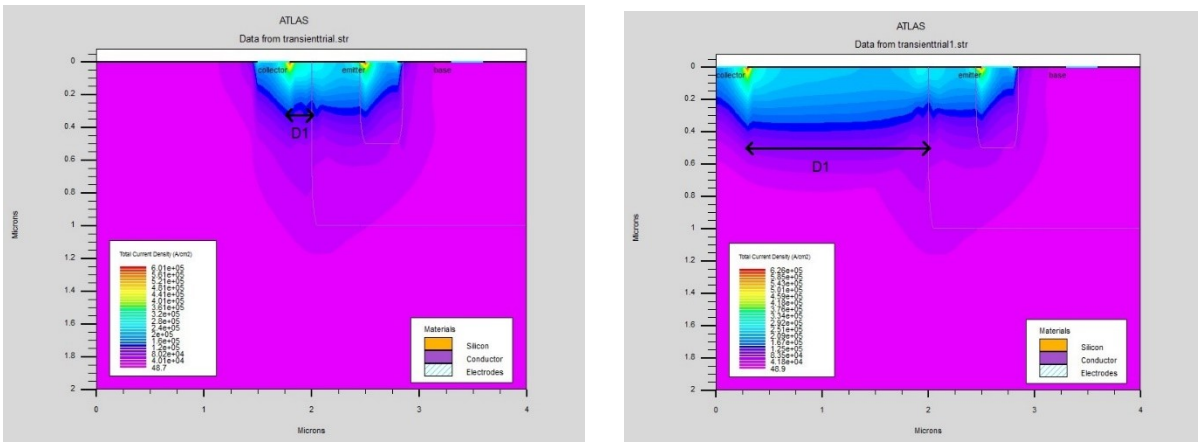

Figure 28 Current density plots for D1=0.2 um and D1=1.7 um.

Figure 29 is the transient breakdown voltage curve for structure B. The variations in the breakdown voltage curve is due to the changes in length from collector to junction region of the structure. The device under test is a parasitic bipolar structure formed of silicon and has different doping densities at each terminal.

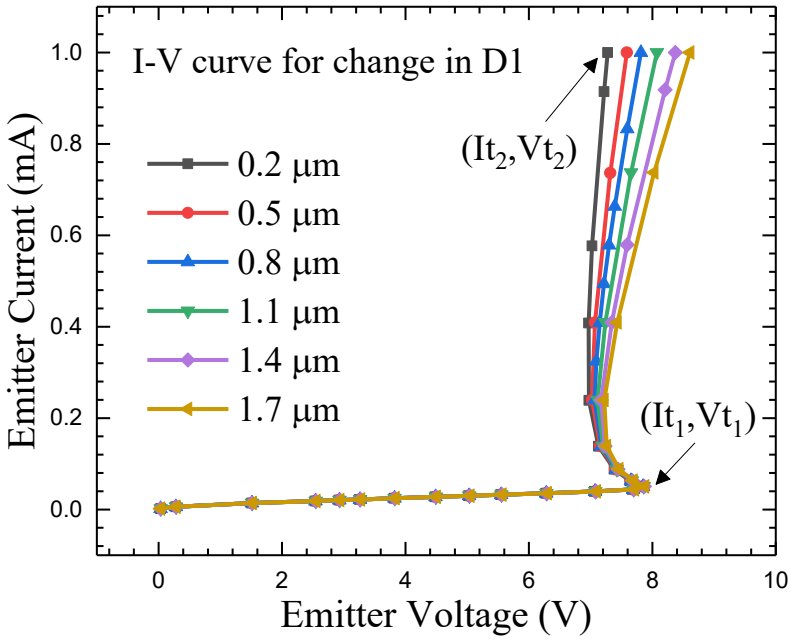

Figure 4 Transient breakdown voltage of substrate bipolar transistor for change in D1.

The breakdown voltage for each of the curves do not vary for changes in parameter D1. The on resistance of the PNP can be changed by varying the distance between the collector and the junction. Failure current (I_{t1}) and the failure voltage (V_{t1}) is constant for modulation in parameter D1. Negative resistance remains constant irrespective of the width of D1. The breakdown voltage of the device obtained from the simulations correspond with the estimated values obtained from standard models.

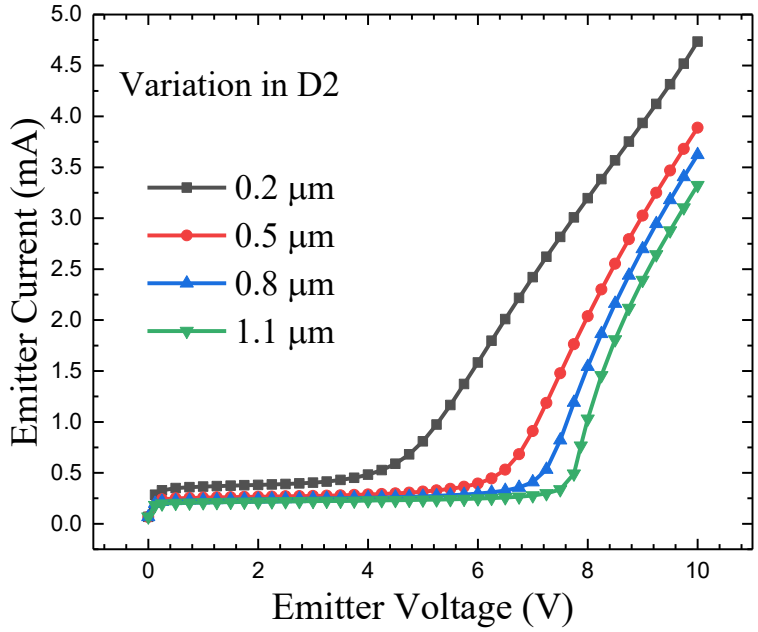

Figure 30 DC breakdown for changes in parameter D2.

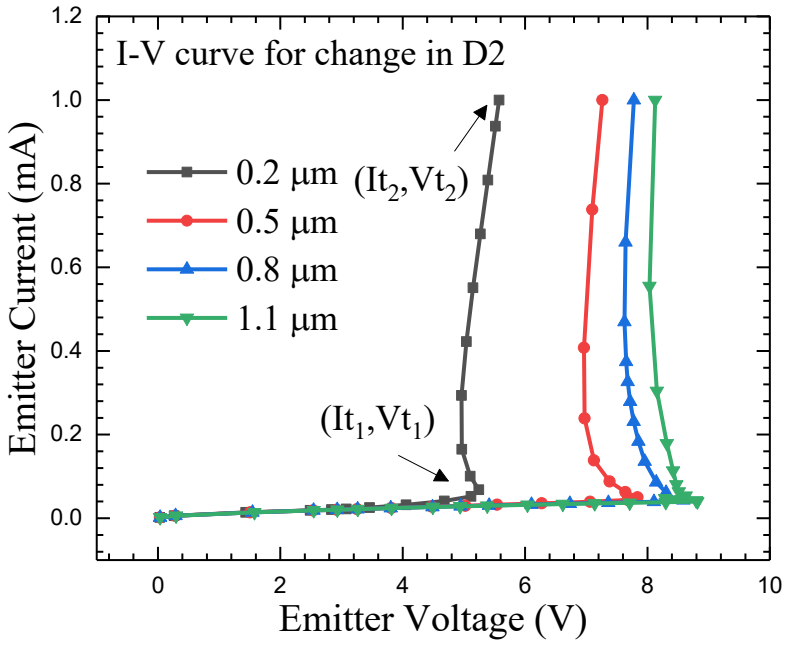

Figure 31 Transient breakdown for changes in parameter D2.

Figure 30 and 31 represents the DC and transient electrical characteristics of a parasitic bipolar device. The change in the breakdown voltage of the curves occurs due to the modulation of D2. The breakdown voltage characteristics is obtained for a device formed of silicon with different doping types and concentrations for each terminal. The breakdown voltage increases with an increase in length of parameter D2. There is minimal change in the on resistance of the device under these conditions of simulation. The failure voltages for each curve increase in accordance with the increase in length of the collector to junction region of the device.

Structure C

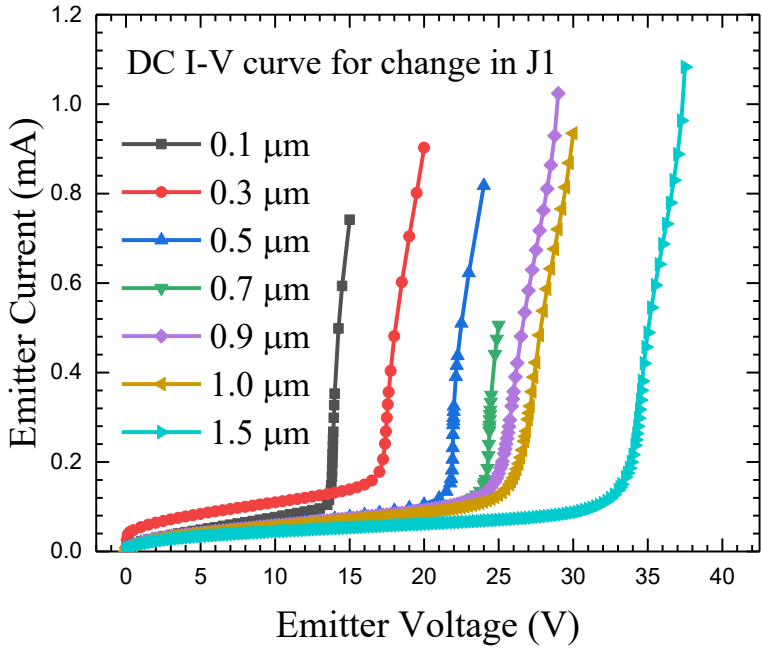

Figure 32 DC IV curve for structure C.

Figure 32 is a DC I-V curve. The plot shows the variation in the electrical characteristics for different junction widths. There is a substantial change in the breakdown voltage as the length of parameter J1 is varied. As the junction width increases there is an increase in the negative resistivity of each curve. The on resistance associated with each curve does not vary for

a change in the junction width. The secondary failure current is constant throughout the simulation. The primary and secondary failure voltages are seen to vary with changes in parameter J1.

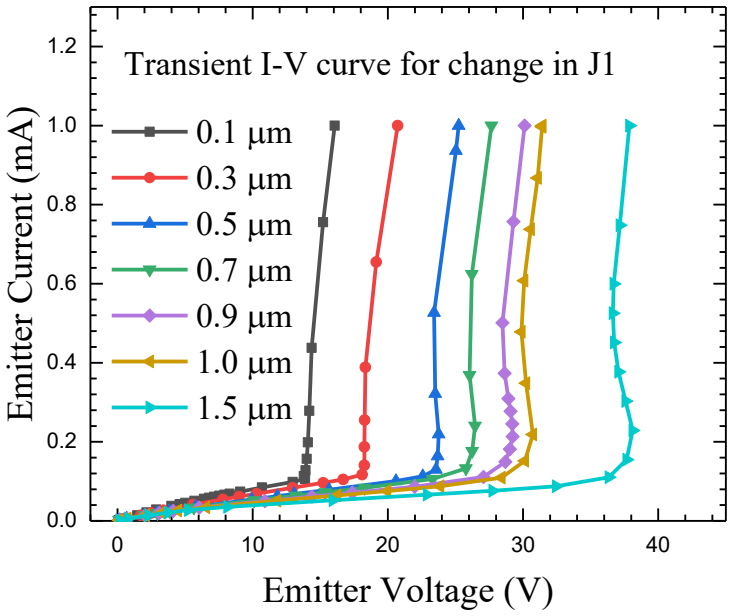

Figure 33 Transient curve for structure C.

Simulation for both DC and transient event was carried out on structures B and C. The main parameters that affect the characteristics were found to be D1, D2 and J1. Other parameters have very negligible effect on the electrical characteristics of the structures under test. Both DC and transient simulations were seen to have similar breakdown voltages as expected.

V. ELECTROSTATIC DISCHARGE PROTECTION IN INTEGRATED CIRCUITS USING WIDE BANDGAP MATERIALS

A. INTRODUCTION

Electrostatic discharge protection imposes few restrictions on chip designing. In the case of high-speed circuits these restrictions come in the form of total capacitance at the input - output pins and the device area in general. As mentioned before, high speed circuit manufacturers need effective on-chip system level IEC ESD protection. Similarly, wide bandgap device manufactures see the need for monolithic integration of driven and driver circuits. The technology that brought forth this integration in wide bandgap devices was developed by Raytheon systems limited [45]. By monolithic integration of low voltage driver circuit with the high-power counterpart it is possible to introduce wide bandgap devices into the low voltage regime. Wide bandgap materials such as silicon carbide (SiC) are inherently superior to silicon in characteristics such as higher operation temperatures, higher switching frequencies and higher power densities [12].

Using SiC in low voltage devices allows for better current handling capability and device densities. Monolithic integration of driver circuit is beneficial in multitude of applications. If such a trend establishes itself, ESD protection for these devices would be paramount. As such, the electrical characterization of the safe operating area (SOA) of wide bandgap materials is of high importance. The paper discussed in this chapter is our first approach to analyze and quantify ESD protection devices in wide bandgap regime. Different NMOS devices with varying device parameters were fabricated and tested to understand their feasibility in ESD protection. It is important to quantify the ESD protection capabilities of wide bandgap materials as it assures device reliability and robustness without added material and processing costs.

B. DISCUSSION AND FUTURE SCOPE

Integration of SiC in low voltage regime was made possible through the new CMOS process developed by Raytheon systems. A total of twenty NMOS devices were fabricated using the HiTSiC process onto a 4H-SiC wafer [12]. The NMOS devices were designed onto a test structure having a common gate and source connection for easy characterization. The NMOS devices differ from each other with respect to their channel length and width. The devices were characterized using a TLP system to study the changes in I_{t1}, V_{t1} and I_{t2}, V_{t2} with respect to the scaling channel dimensions.

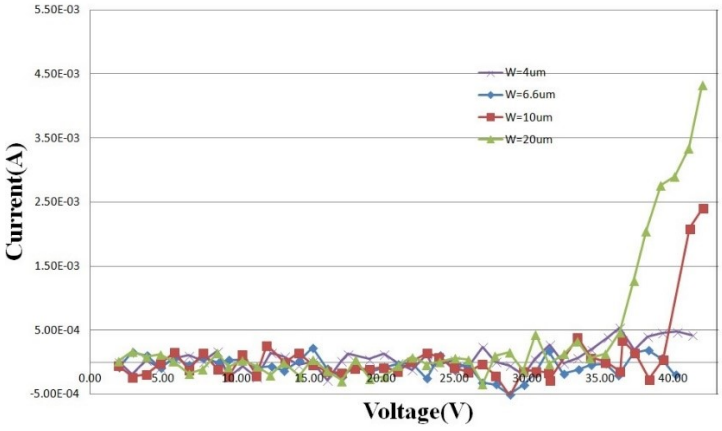

Figure 34 TLP curve for different channel width at gate bias=0V [12].

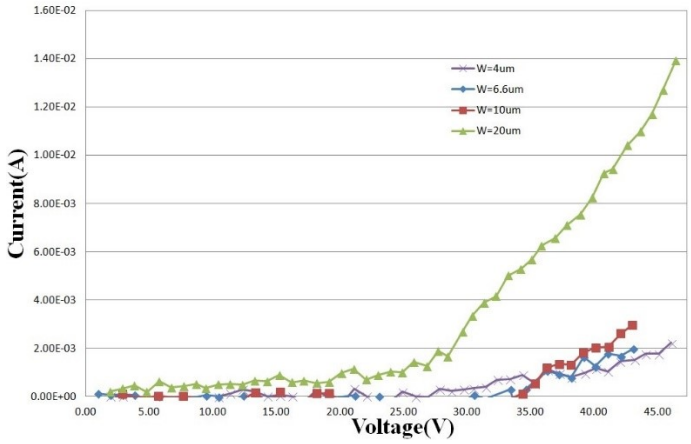

Figure 35 TLP curve for different channel width at gate bias=15V [12].

Figures 34 and 35 shows the current scalability of the devices for different gate biases. All the devices mentioned in figures 33 and 34 have the same channel length of 1µm. The failure voltages of all the devices are the same as seen from figure 34 as each of these devices have the same channel lengths leading them to have the same current gain of parasitic BJT. The final failure current increase in both cases when the channel width is increased. This scalability of It_2 is increase when the gate bias is increased. The scalability of the device with W/L=20 µm/1 µm is seen to increase from 0.2 mA/µm to 0.7 mA/µm for an increase in gate bias from 0 V to 15 V. This phenomenon suggests of a strong gate effect on the failure current for short channel devise that are assisted by the parasitic bipolar transistors [12].

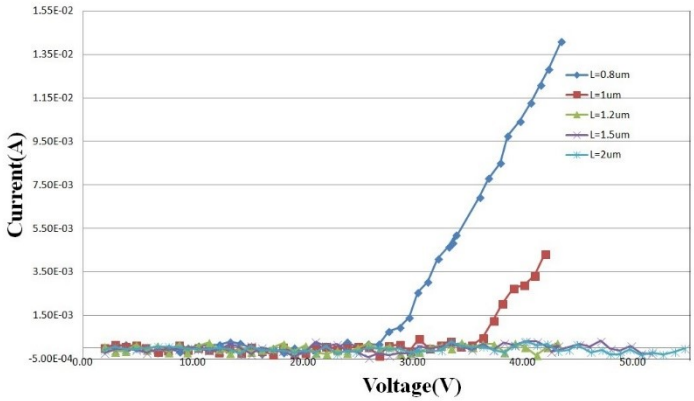

Figure 36 TLP curve for different channel length at gate bias=0V [12].

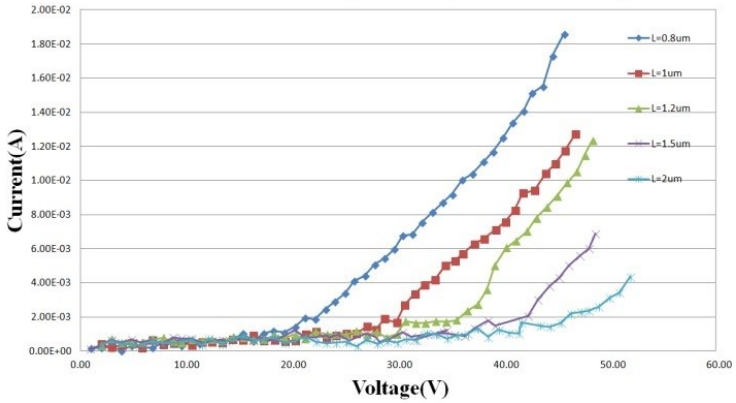

Figure 37 TLP curve for different channel length at gate bias=15V [12].

Figures 36 and 37 shows the scalability of breakdown voltage of for different gate biases. All the devices mentioned in figures 36 and 37 have the same channel width of 20μm. From figure 36 it can be inferred that when no gate bias is applied for short channel lengths, the current gain of the parasitic BJT is high leading to a high I_{t2}. With increase in channel length, the gain reduces leading to negligible I_{t2}. This effect is magnified when a gate bias is applied as can be seen in figure 37. Scalability of I_{t2} is clearly discernible from 0.2mA/μm to 0.9mA/μm for change in channel length from 2μm to 0.8μm. The change in the channel length corresponds to the base length of the parasitic BJT device. With smaller base lengths, breakdown due to avalanche multiplication is possible for lower voltages [46].

The scalability of ESD protection as seen by the TLP characterization of the fabricated devices show promise for the use of wide bandgap materials as ESD protection devices in monolithic integration. The SOA benchmark suggested by the result of TLP characterization may be used to expand the SOA for wide bandgap materials other than SiC. The increased current handling capability of the wide band gap materials in low voltage application when combined with the increased control over current gain in parasitic BJT through our proposed method may open avenues for improved ESD protection circuits.

VI. CONCLUSION AND FUTURE WORK

One of the primary goals of this project was to have a measure of control over the current gain of the parasitic PNP structure. By controlling the gain of the PNP it is possible to control the triggering of the parasitic PNP device. The ESD protection scheme design based on the parasitic PNP device is efficient and reliable only when it is possible to manipulate its breakdown voltage to fit the ESD protection window. To this measure, device parameters such as distance between the terminals, junctions and the widths of the diffusions were studied and simulated to form a knowledge repository on the characteristics of the parasitic PNP device. It was found that parameter D1 influences the ON resistance of the PNP. Parameter D2 and J1 directly affects the breakdown voltage of the parasitic PNP device. A measure of negative resistance was observed when parameter D2 was modified leading to control over the current gain of the PNP. The maximum shift in V_{t1} from 12 V to 36 V was observed for a change in parameter J1 from 0.1 µm to 1.5 µm. A less pronounced though more important change in V_{t1} from 5 V to 9 V occurred for a change in D2 from 0.2 µm to 1.1 µm. Parameter D2 offers more merit as it based on the base width modulation than through the interaction form the substrate.

Future work includes the calculation of the device capacitance at each pin to determine the best option for ESD protection in high speed circuits. Many design rules can also be implemented to find the best fit for on-chip IEC ESD protection. Furthermore, the type of unit cell can be changed (finger to island) to achieve the most area efficient parasitic PNP structure for ESD protection.

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