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A Virtual Space Vectors based Model Predictive Control for Three-Level Converters

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A Virtual Space Vectors based Model Predictive Control for Three-Level Converters

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ABSTRACT

Three-phase three-level (3-L) voltage source converters (VSC), e.g., neutral-point clamped (NPC) converters, T-type converters, etc., have been deemed to be suitable for a wide range of medium- to high-power applications in microgrids (MGs) and bulk power systems. Compared to their two-level (2-L) counterparts, adopting 3-L VSCs in the MG applications not only reduces the voltage stress across the power semiconductor devices, which allows achieving higher voltage levels, but also improves the quality of the converter output waveforms, which further leads to considerably smaller output ac passive filters.

Various control strategies have been proposed and implemented for 3-L VSCs. Among all the existing control methods, finite-control-set model predictive control (FCS-MPC) has been extensively investigated and applied due to its simple and intuitive design, fast-dynamic response and robustness against parameter uncertainties. However, to implement an FCS-MPC on a 3-L VSC, a multi-objective cost function, which consists of a term dedicated specifically to control the dc-link capacitor voltages such that the neutral-point voltage (NP-V) oscillations are minimized, must be designed. Nevertheless, selecting proper weighting factors for the multiple control objectives is difficult and time consuming. Additionally, adding the dc-link capacitor voltages balancing term to the cost function distributes the controller effort among different control targets, which severely impacts the primary goal of the FCS-MPC. Furthermore, to control the dc-link capacitor voltages, additional sensing circuitries are usually necessary to measure the dc-link capacitor voltages and currents, which consequently increases the system cost, volume and wiring complexity as well as reduces overall reliability.

To address all the aforementioned challenges, in this dissertation research, a novel FCS-MPC method using virtual space vectors (VSVs), which do not affect the dc-link capacitor voltages of the 3-L VSCs, was proposed, implemented and validated. The proposed FCS-MPC strategy has the capability to achieve inherent balanced dc-link capacitor voltages. Additionally, the demonstrated control technique not only simplifies the controller design by allowing the use of a simplified cost function, but also improves the quality of the 3-L VSC output waveforms. Furthermore, the execution time of the proposed control algorithm was significantly reduced compared to that of the existing one. Lastly, the proposed FCS-MPC using the VSVs reduces the hardware cost and complexity as the additional dc-link capacitor voltages and current sensors are not required, which further enhances the overall system reliability.

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DEDICATION

This dissertation is dedicated to

my parents, my siblings, my wife and my son “Saad”.

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CHAPTER 1

INTRODUCTION AND LITERATURE REVIEW

1.1 Traditional AC Power Grid and AC Microgrids

The electric power grid has been experiencing tremendous development since the Pearl Street Electric Station was officially operated in early 1880s [1]-[3]. Ever since, a significant amount of money and effort have been invested to expand the electric grid from a small town to a nationwide network. As a result, the dramatic expansion of today's electric grid has allowed it to be seen as the largest system human beings have ever made [4]. This expansion could not have been achieved without the continuous advancements in power electronics technologies, protection systems, control theory and communication systems, to name a few [5].

Traditionally, the legacy power system, presented in Figure 1.1, consists of power generation systems, power transmission systems and power distribution systems. The power generation is usually centralized. The produced electric power is normally transmitted through a transmission network to the distribution systems, which are usually featured as radial feeders, and reticulate the electric power to the end-users [6]. The power substations, which mainly have power transformers, are utilized to connect the three systems together forming the traditional electric power system [7]. While the step-up power transformers are used to achieve high-voltage level such that the power losses, especially the I^2R, at the transmission lines are significantly reduced, the step-down power transformers are mandatory to convert the high voltage at transmission level to the distribution voltage levels in order to allow various loads, which can be residential, commercial or industrial, to connect with the electric grid [8], [9].

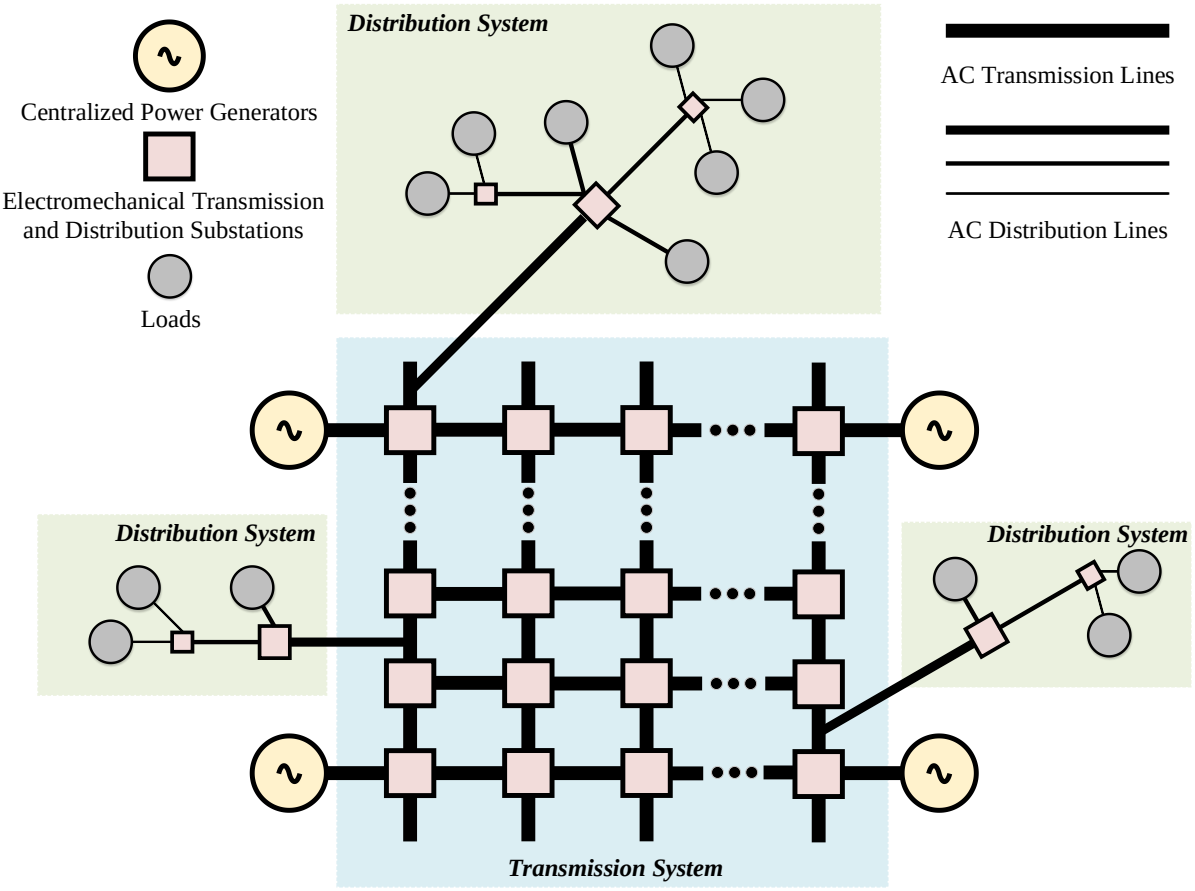


Figure 1.1: An illustration of the traditional electric power system.

Centralized generations (CGs), as the ones demonstrated in Figure 1.1, are usually used to generate electric power, which is delivered to the end-users through massy passive transmission and distribution systems [10]. As such, the use of the CGs, transmission and distribution systems, results in unidirectional power flow. This hierarchical structure of the traditional electric power system is disadvantageous since large-scale power outages can result from extreme natural disasters such as hurricanes, severe thunderstorms, flooding, etc. [11]. Restoring the functionality of the electric power system from grave damage could last for weeks, which substantially reduces the reliability of the electric power system [12]. In addition, the passive transmission and distribution lines contribute in a significant reduction in the system overall efficiency due to the high power losses on the lines impedance, represented by I^2R [13]. The secure supply for the

rapidly and consistently growing power demand, which may lead to electric grid instability and/or electric power outages, is another challenging obstacle, which cannot always be addressed by increasing the capacity of the CGs due to the high cost of adding and operating enormous infrastructure of new power plants and transmission networks [14]. Furthermore, the major constituents of the conventional electric power system such as governors, automatic load tap changers, switched capacitor banks, etc. are electromechanical equipment, which decreases the operational life of these devices, and eventually leads to failure due to the excessive applied control actions [6]. The increased greenhouse gas emissions as well as the rapid depletion of fossil fuel reserves are also two primary challenges, attributed with the dependence on traditional fossil fuel based CGs [15], [16]. Consequently, the classical electric grid is facing many challenges to enhance the system reliability, resiliency, efficiency, sustainability, while reducing costs.

Therefore, in order to meet the considerably increasing challenges associated with the classical CGs and the massive transmission and distribution systems, distributed energy resources (DERs), which consist primarily of renewable energy sources (RESs) and energy storage systems (ESSs), have been recognized as a better alternative to the fossil fuels based CGs [17]. First, the development of the non-intermittent DERs technologies, e.g., ESSs, offers more advantages to the electric power system including electric system reliability improvement and electric power quality enhancement [18], [19]. Second, the DERs are usually installed at or near the end-use consumer [20], such that a significant improvement in the electric system efficiency can be achieved without routing the energy through the bulk transmission and distribution systems [21]. Additionally, compared to the conventional CGs, whose power capacity is costly and difficult to increase, the DERs, which are composed of technologies with accelerated price reduction [22], are easily installed next to the demand side to supply the rapidly growing loads [23]. Also, unlike the classical

CGs, which cause the rapid depletion of fossil fuel reserves and the increased harmful CO_2 emissions, the DERs are considered more sustainable solutions due to their capabilities to integrate the environmentally-friendly RESs such as photovoltaic (PV) systems, wind turbine (WT) technologies, etc. to the ac mains [24]-[26]. In addition, in contrast to the typical electric grid, which is equipped with the electromechanical devices, which has limited daily control actions [27], the reliable static power electronics technologies are the key components of the DERs [28]. Lastly, the strategic deployment of the DERs in the distribution system could also contribute in many advantages to today's electric power network such as enhanced electric grid voltage profile [29], improved power factor [30], fully-supplied peak load demand [31], etc.

However, despite the facts that 1) the cost of the various DERs technologies has recently seen drastic reduction [22]; 2) the high-power electronics technologies have undergone dramatic development due to the fast-switching and high-power semiconductor devices evolution and real-time digital controllers advancement [32]-[34]; and 3) governments have encouraged and supported the DERs installations by establishing new polices and providing incentives [35], the integration of the DERs with intermittent nature to the distribution system may result in multiple detrimental impacts on the low-voltage distribution system: among them 1) the reverse power flow, which impacts the protection equipment since they are not typically coordinated for a bidirectional power flow system; 2) the voltage rise and fluctuations, which change the feeder voltage profile and affect the connected loads; 3) the interference with the load-tap changers, voltage regulators and switched capacitor banks, which results in excessive use of these electromechanically devices [36], [37]; and 4) the increase of the harmonics contents, which may cause power quality issue and distribution lines overheat [22].

Therefore, since the integration of the various DERs into the electric grid has been experiencing drastic growth globally, and considering the uncontrollability of the DERs due to the intermittent nature of the RESs is a dilemma, numerous studies have recently focused on developing new and advanced control schemes to manage and operate the electric grid with high penetration of DERs [38], [39].

Hence, the concept of microgrids (MGs) was firstly proposed in [40] to exploit the advantages of the DERs. An MG is a small-scale electric grid, which consists mainly of one or more DER(s) managed and operated together to supply power to the load(s) with and/or without the main electric grid being connected [41]-[44]. This cluster of DERs leverages the advancement in power electronics technologies and their control strategies to ensure the efficient, reliable and safe operation for such DERs with the legacy electric grid, and also to secure the power supply for the critical loads during fault events [45], [46]. To explicate, an MG can be operated to regulate the line voltage by controlling the reactive power flow of the DERs along the distribution feeder [23]. In addition, the power drawn from the power substation can be minimized by means of MGs resulting a more efficient electric power distribution system [47]. The electric grid frequency regulation is another target, which can be accomplished using an islanded MG [48], [49], [50]. Resiliency, which is defined as the capability of the electric power system to adjust to unusual incidental situations and rapidly restore the electric distribution system from the disruptive events, is also achievable using the MG concept [51]-[54]. Generally, depending on how voltage source converters (VSCs) of an MG interact with the main grid, three different operating modes of power converters can be specified. These VSC operating modes are grid-following, grid-forming and grid-supporting [55]-[57].

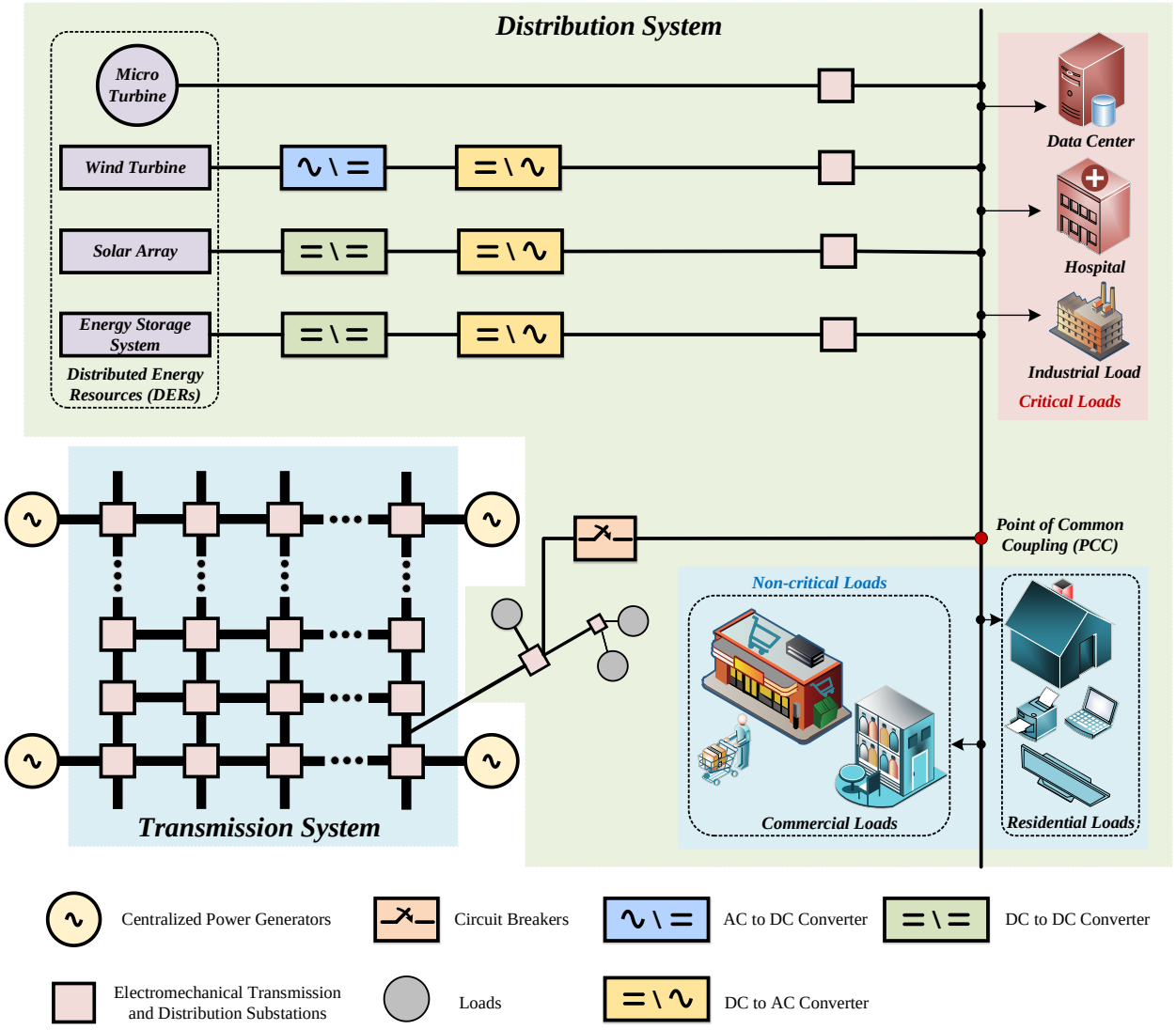


Figure 1.2: An illustration of an ac MG connected to the electric power system.

Figure 1.2 presents an illustration of a notional ac MG connected to the legacy electric grid through a circuit breaker. Both critical and non-critical loads are assumed to be connected to the point of common coupling (PCC), which is the point of interference of the DERs with ac mains. As demonstrated in Figure 1.2, different types of the DERs, i.e., intermittent and non-intermittent, can be used to supply power to the distinct loads. The non-intermittent power sources, i.e., the micro-turbine generator and the ESS, are critical in the MG design to secure the operation of the MG when the main electric grid is unavailable, and to smooth out the intermittent generated power

by the RESs. As displayed in Figure 1.2, various types of power electronics converters, i.e., dc-ac, ac-dc and dc-dc converters, can be utilized in the MG to perform the energy conversion.

1.1.1 Classification of Control Schemes of VSCs in AC MGs

An ac MG is capable of integrating and operating multiple VSCs, which are controlled to have different operating modes, i.e., the grid-following mode, the grid-forming mode, and the grid-supporting mode [58]. The vast majority of the VSCs in an MG are classified as the grid-following VSCs. The grid-forming VSCs are also essential in an MG to ensure secure and continuous power supply for critical loads during the main grid faulty events [59]. The grid-supporting VSCs also play also an important and decisive role in an MG as they can be controlled to maintain the variations of the MG voltage magnitude and frequency to be within the allowed levels [60]. In the work proposed in this dissertation, both the grid-following and grid-forming VSCs are considered to verify the proposed control algorithms. In this section, unlike the grid-supporting VSCs, which are briefly described, the grid-following and the grid-forming VSCs are explained in detail.

1.1.1.1 Control of Grid-Following VSCs

In MG applications, the grid-following, also referred to as grid-connected, grid-tied, grid-feeding or grid-interfaced, VSCs have been widely accepted and applied in various power electronics applications such as grid-connected PV [61], WT [62] technologies, etc. Having the VSCs to operate in the grid-connected mode, similar to the one presented in Figure 1.3, simply means the operation of these VSCs is strictly synchronized to the stiff electric grid, and the VSCs are controlled in current-control mode to inject specified power to the PCC, where the power converters are tied to the electric grid [63]. The generic model of a grid-following VSC is a current source in parallel with a high-output impedance. The operation of this kind of VSCs cannot be

accomplished without having these VSCs connected to a voltage source, which provides the voltage amplitude and frequency of the MG [64].

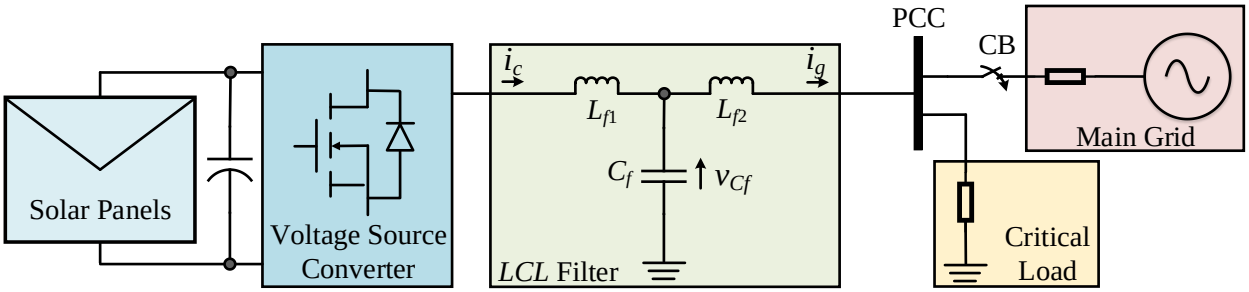


Figure 1.3: One-line diagram of a grid-following PV inverter connected to the main grid.

The grid-following VSCs are usually integrated with the electric grid through either an *L* or an *LCL* filter to suppress the harmonic contents resulting from the fast-switching power semiconductor devices. The first-order *L* filter is known for its easy design and control. Since the electric grid has an inductive impedance, resonances do not exist in such inductive systems. However, to suppress the high-frequency switching ripples, a bulky *L* filter, which increases the volume and the cost of the passive filter, is inevitable. Additionally, using the large *L* filters to connect the VSCs to the electric grid leads to high-voltage drop across the passive filter, which reduces the system efficiency and dynamic response [65]. On the contrary to the first-order *L* filter, the high-order low-pass *LCL* filter, which was firstly proposed in [66], has been determined to be more cost-effective and efficient to meet the electric grid interference standards, specified by IEEE Std. 519 and IEEE Std. 1547 [67]. This significant reduction in the *LCL*-filter inductors' size is the result of the high-harmonic contents attenuation of such filters. Nonetheless, the third-order *LCL* filters express more complexity in the closed-loop controller design due to the existence of the *LCL*-filter resonances. Thus, to limit the resonance effect on the closed-loop controller performance, two damping techniques, categorized as passive [68] and active [69], are established.

Demonstrated in Figure 1.4 is a generic control block diagram of the grid-interfaced solar inverter with the passive damping resistor, R_d, included in the system design. Though several configurations have been proposed to add the passive R_d to the circuit design, a common practice is to include the R_d in series with *LCL*-filter capacitor as depicted in Figure 1.4 [70]. Although the passive damping technique enhances the stability of the closed-loop controller by attenuating the peak resonances of the *LCL* filter [71], the R_d value should be selected carefully to minimize the power losses [72]. Another drawback of passively damping the *LCL*-filter resonances is that at high frequencies, the *LCL* filter behaves as a second-order system, and this deteriorates the ability of the filter to attenuate resonances [70].

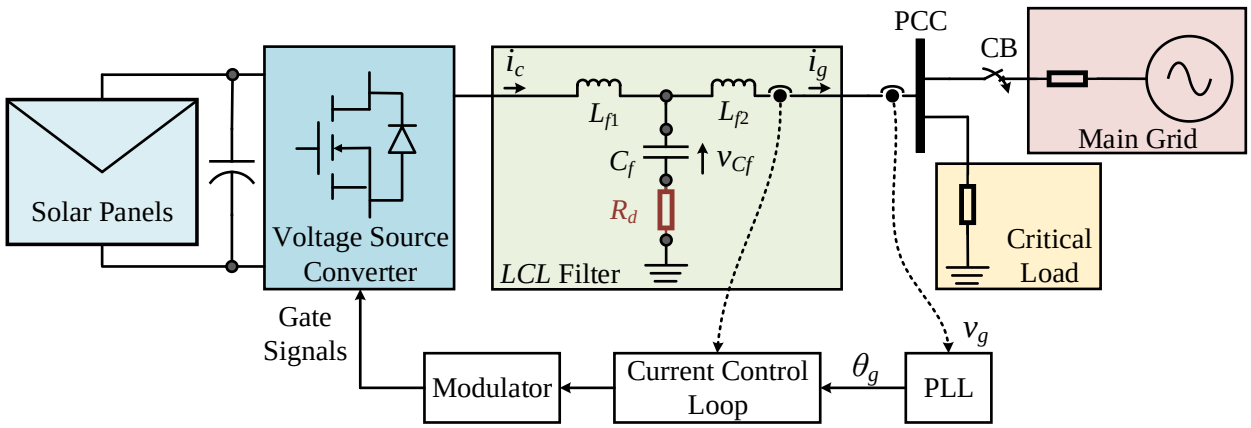


Figure 1.4: Passive-damping based control block diagram of a grid-following PV inverter.

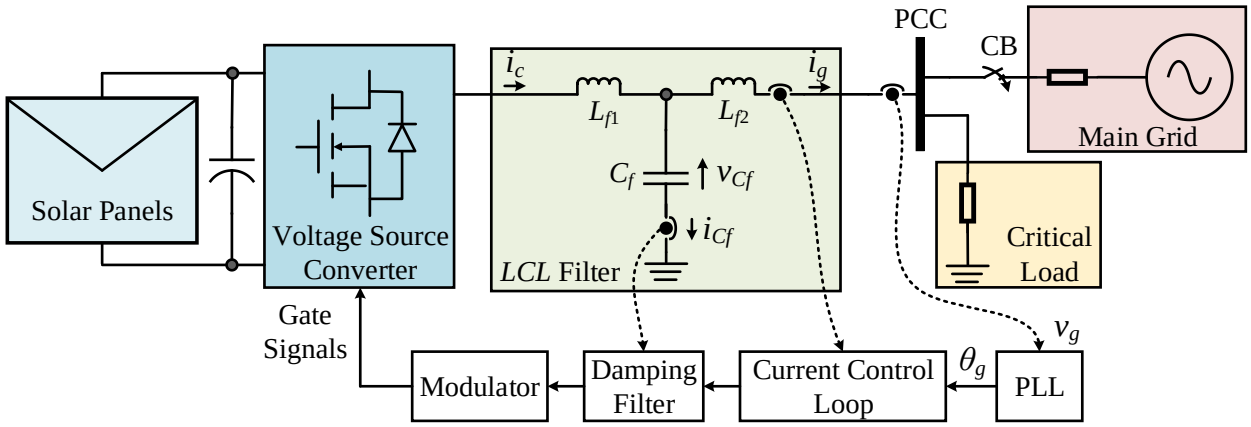


Figure 1.5: Active-damping based control block diagram of a grid-following PV inverter.

In contrast to the passive damping strategy, active damping algorithms have been proposed to avoid the cost and power losses associated with using an actual damping resistor [73]. A simple and straightforward design for the active damping scheme is to feed the output of the current-control loop to a damping filter, which can be a low-pass filter or a notch filter. The drawback of this kind of active damping techniques is that the controller performance is substantially sensitive to the parameter uncertainties [74]. Another active damping strategy, which has been commonly implemented due to its high robustness, is the capacitor-current feedback active damping. Using this control method, a virtual resistor is emulated by the proportional feedback of the *LCL*-filter capacitor current [75]. A generic control block diagram of this control technique is displayed in Figure 1.5.

1.1.1.2 Control of Grid-Forming VSCs

Recently, with the advancement of the ESSs technologies, grid-forming VSCs, presented in Figure 1.6, have become essential for any MG design since they ensure that critical loads are not affected by power outages [76]. Typically, when the MG is operated in the islanded operating mode, the grid-forming VSCs are responsible for establishing the voltage amplitude and frequency of the disconnected electric grid. The generic model of a grid-forming VSC is an ac voltage source, which has a low-output impedance. A common application for grid-forming VSCs is uninterruptible power supplies (UPSs) [58], which is normally included in applications like hospitals, data centers, etc. Since the applications, which have the VSCs operated in a grid-forming mode, require stable and high-quality sinusoidal ac voltage, numerous control schemes, which use *LC* filters to suppress switching ripples generated by the power switches, have been proposed. Typically, the control of the grid-forming VSCs concentrates only on rejecting the disturbance,

which is caused by the load variations [58]. Generally, the control strategies of grid-forming VSCs are classified as either dual-loop [77]-[82], or single-loop [83]-[88] controllers.

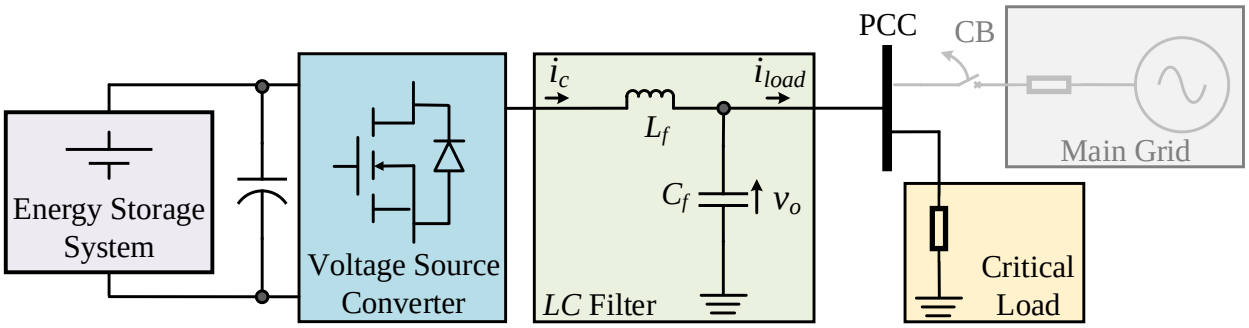


Figure 1.6: One-line diagram of a grid-forming inverter connected to a critical load.

On the one hand, dual-loop, referred to as double-loop, control strategies consist of an inner-current feedback loop and an outer-voltage feedback loop as shown in Figure 1.7. The *LC*-filter inductor current is mostly used as a controlled variable with the inner-current control loop; the *LC*-filter capacitor voltage is the controlled variable used in the outer-voltage control loop. In specific controller designs, the *LC*-filter capacitor current is selected as an inner-loop controlled variable so that disturbance rejection properties are improved. In order to achieve an accurate dual-loop controller design, the outer-voltage control loop should be characterized to have slower dynamics than the inner-current control loop so there is no potential interference between the two control loops. The drawbacks of these control strategies are the design complexity, which relies on the serial tuning for the current and voltage controllers and the slow dynamic response, which is caused by the different [80], [81]. However, the inherent damping effect, which attenuates the resonance occurs due to the *LC* resonant frequency variations, is achieved by the inner-current loop, which enhances the stability of the closed-loop controller against the load variations as it provides active damping [82].

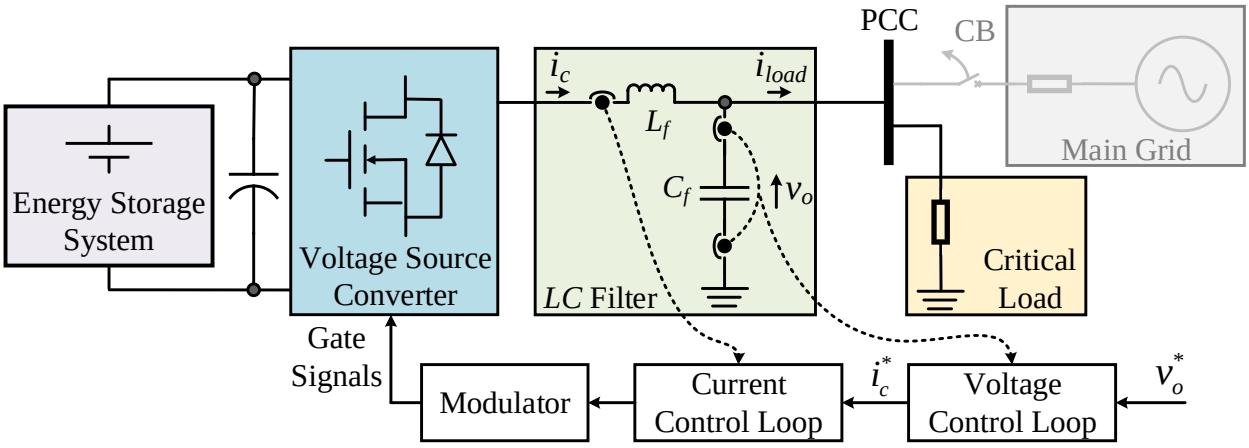


Figure 1.7: Dual-loop control block diagram of a grid-forming inverter.

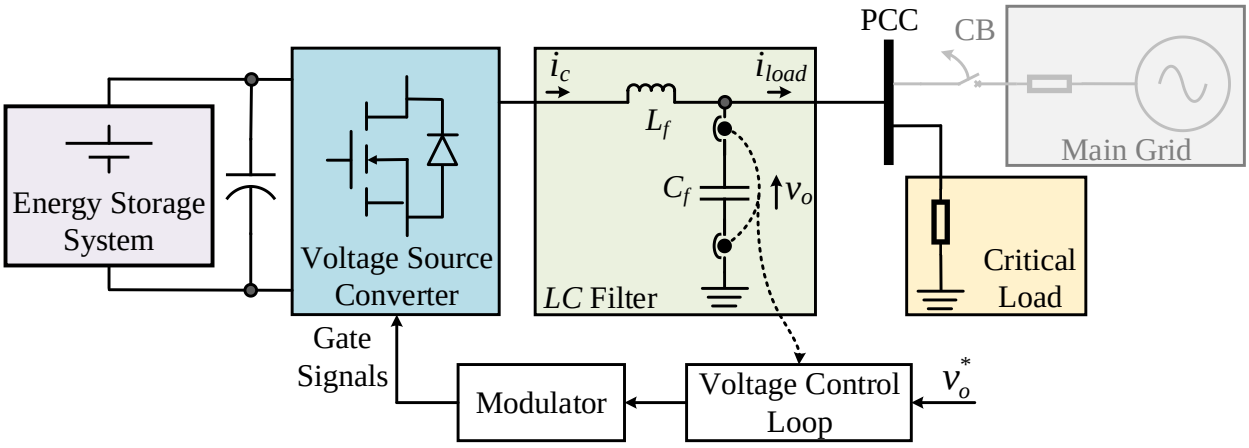


Figure 1.8: Single-loop control block diagram of a grid-forming inverter.

On the other hand, single-loop control techniques, demonstrated in Figure 1.8, have also been considered in the literature to provide alternative solutions to the classical dual-loop control methods. In this control strategy, the capacitor voltage is the only feedback signal to be used within the controller design. As a result, significant reduction in the controller design complexity is achieved. Because current sensors are not needed, a reduction in the system cost is also achieved. In addition, single-loop control methods present fast-dynamic response due to the fact that cascaded current-voltage control loops, which have different dynamics, are not part of the controller design. However, the hindrance of these control approaches is the high parameter

sensitivity; thus, a large *LC*-filter capacitor has to be considered in the passive filter design to guarantee high-quality output voltage [86], [88].

1.1.1.3 Control of Grid-Supporting VSCs

Two different representations are usually used to describe grid-supporting VSCs. The distinct representations aim to regulate the voltage and frequency of the ac MG. Firstly, a grid-supporting VSC can work as a current source such that not only supplies power to loads, but also provides support for the MG voltage and frequency [60]. Secondly, operating the parallel grid-supporting VSCs as ac voltage sources allows sharing loads among the parallel converters according to the converters power ratings [89].

1.1.2 Synchronization of VSCs in AC MGs

Typically, for grid-feeding VSC control, properly synchronizing the grid-following VSCs with the voltage of the electric utility is an essential task to accomplish accurate grid integration and efficient operation of the DERs with the ac mains. To illustrate, in a three-phase electric system, the positive-sequence component of the electric utility voltage must be detected and used to ensure the energy transfer between the grid-tied VSC and the electric utility is well-synchronized. A synchronization method, hence, is mandatory to be included in the grid-tied VSC controller design to extract the electric utility positive-sequence voltage amplitude and phase angle so that the distinct DERs, which form the grid-interfaced MG, are carefully synchronized with the ac mains [90], [91]. A common synchronization strategy, which has been used in many electrical applications including the grid-connected VSCs, is the phase-locked loop (PLL). The PLL can be simply realized as a closed-loop system, whose output signal follows its input reference signal's phase and frequency. The three primary components of a generic three-phase PLL, which is

displayed in Figure 1.9 are a phase detector (PD), a filter loop (FL) and a voltage-controlled oscillator (VCO) [92], [93]. Chapter 2 of this dissertation will provide a detailed explanation for each part of the PLL. It is worth noting that the performance of the grid-interfaced MG is highly affected by the accuracy of the selected synchronization technique, a precise synchronization method should result in a more reliable MG operation and vice versa [60].

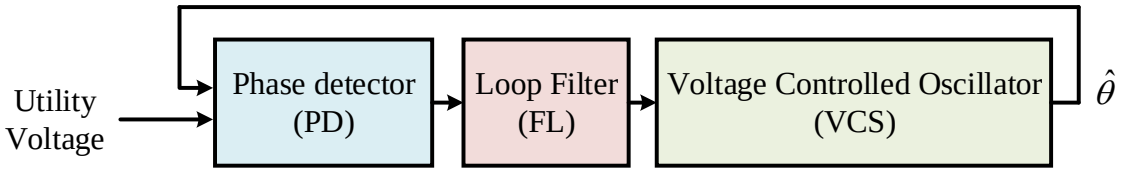


Figure 1.9: Block diagram of a generic three-phase PLL system.

When a fault occurs at the main electric grid, the MG is usually expected to operate independently in the islanded operating mode. Thus, for grid-forming VSCs, the synchronization method should have the capability to ensure precise signals during the islanding transition such that the electric grid voltage amplitude and frequency can be initiated by the grid-forming VSC [94]. When a complete stand-alone operating mode is accomplished, the synchronization method operates as an oscillator, which provides a reference voltage with a determined voltage amplitude and frequency. As soon as the fault is cleared out, and main electric grid is back in operation, the voltage of the grid-forming VSC has to be resynchronized with that of the mains [95].

Due to its simple design and high performance during ideal electric grid conditions [96], the conventional synchronous-reference-frame phase locked loop (SRF-PLL) is selected to synchronize different VSCs in the work demonstrated in this dissertation . A more comprehensive description for the SRF-PLL approach will be presented in Chapter 2.

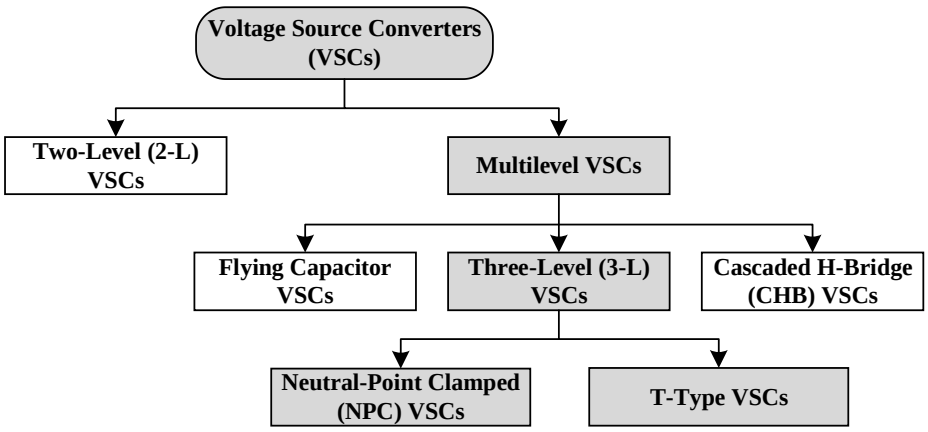


Figure 1.10: Flow chart of the commonly used VSCs in MG applications.

1.2 Classification of VSC Topologies for AC MGs

The integration of the various DERs with the electric utility cannot become reality without the critical role, which is played by the power electronics converters. In MG applications, the most commonly adopted VSC topologies, which work as an interface for the DERs and the ac mains, can be classified into two major categories; two-level (2-L) and multi-level (M-L) VSCs. While the 2-L VSCs are mostly used in low- to medium-voltage applications, the M-L VSCs are usually preferred for medium- to high-voltage power electronics applications. As shown in Figure 1.10, unlike the single 2-L VSC topology, the M-L VSC topologies are further classified into three categories. The commonly adopted M-L VSC topologies include flying capacitor, cascaded H-bridge and 3-L VSCs. In the work presented later in this dissertation, the latter are selected due to their various advantages, which distinguish the 3-L VSCs from their 2-L counterparts. This section provides some backgrounds regarding the 2-L and 3-L VSC topologies.

1.2.1 Three-Phase 2-L VSCs

The classical 2-L VSCs dominate the market of low-voltage industrial applications since these VSCs present substantially simpler circuit design and significantly reduced cost [97]. Compared

to the conduction losses of a 3-L VSCs, the considerably reduced conduction losses of the power semiconductor devices in a 2-L VSC is another advantage, which contributed in making the 2-L VSCs become a standard industry choice to achieve the standard of grid-interfaced DERs. In addition, unlike the M-L VSCs, the control design for the 2-L VSCs is relatively simple since these power converters do not have a neutral point in the dc-link capacitor, which needs special attention and control. However, several limitations are hindering the adoption of this topology for the medium- and high-voltage applications. First, the power semiconductor devices in the 2-L topology have to be rated to block the full dc-bus voltage, which results in high dv/dt. This high dv/dt not only contributes in significant current ripples, but may also result in damaging the expensive power switches. Additionally, in applications, which require high-switching frequency, excessive switching losses across the power semiconductor devices are experienced. Moreover, bulky ac output passive filters have to be used to interface these VSCs with the electric grid, since the 2-L VSC output waveforms have higher total harmonic distortion (THD) [98].

1.2.2 Three-Phase 3-L VSCs

Two-level (2-L) voltage source converters (VSC) are widely adopted as an interface to connect DERs to MGs. However, for medium- and high-power applications, multilevel (M-L) VSCs are alternatives to typical 2-L converters due to their improved output waveform quality and reduced voltage stress across power semiconductor devices. Also, compared to 2-L VSCs, adopting M-L converters results in using smaller ac filters [99], [100]. Commonly used M-L converter topologies include flying capacitor converters, cascade H-bridge and three-level (3-L) neutral-point clamped (NPC) converters; the latter has been extensively used in a wide range of industrial applications [98], [101]. Nevertheless, as a result of the increase number of power semiconductor devices, 3-L NPC converters suffer from higher conduction losses relative to the

2-L converters. Thus, the 3-L T-type VSCs, which combine advantages of the 3-L NPC converters and the 2-L converters, have been used lately in high-power low-voltage applications [102], [103]. In the work presented throughout this dissertation, the most commonly used 3-L converter topologies, i.e., NPC VSCs and T-type VSCs, are utilized later to verify different control algorithms.

1.2.2.1 Three-Phase 3-L NPC VSCs

In the early 1980s, 3-L NPC converter was first introduced by Nabae [104]. Ever since, this topology has shown its superiority over the conventional 2-L VSCs [105]. To explain, unlike the 2-L converters, this converter has been determined to be suitable for wide range of medium-voltage high-power applications. To start with, the power semiconductor devices, which compose the 3-L NPC, are exposed to low voltage stress, i.e., only half of the dc-bus voltage. Compared to 2-L converters, the same power semiconductor device in a 3-L NPC VSC can handle twice the power as if it is used in a 2-L topology [105]. This feature allows the converter to be connected to a higher voltage dc-bus resulting in achieving higher power. The 3-L converters output waveform quality is also significantly improved relative to that of the 2-L converters. Therefore, a substantially smaller ac output filter can be utilized. In addition, using 3-L NPC converter leads to reduced switching losses compared to switching losses generated by a traditional 2-L converter.

However, as a result of utilizing more power semiconductor devices in the 3-L NPC VSC, the cost will be increased. In addition, having high number of these power switches reduces the converter overall reliability and efficiency since the switching device conduction losses are significantly increased [106]. The power circuit of this topology with a comprehensive description of this topology will be provided in Chapter 2.

Table 1.1
Characteristics of 2-L and M-L Power Converters

Topology	Switching Losses	Conduction Losses	Waveform Quality	Output Filter	Control Complexity	Extra Hardware
2-L Converters	High	Low	Low	Bulky	Simple	None
Fly Capacitor Converters	Low	High	High	Small	Complex	Flying Capacitors
CHB Converters	Low	High	High	Small	Complex	Separate DC Sources
3-L NPC Converters	Low	High	High	Small	Complex	Clamping Diodes
3-L T-Type Converters	Medium	Medium	High	Small	Complex	None

1.2.2.2 Three-Phase 3-L T-Type VSCs

As a result of the increased number of power semiconductor devices in the 3-L NPC VSCs, these converters suffer from higher conduction losses relative to the 2-L converters, which sacrifice the converter efficiency. As thus, the 3-L T-type converter, which combines advantages of the 3-L NPC converters and the 2-L converters, has been used lately in low- and medium-voltage high-power applications [103]. To clarify, the 3-L T-type converter has the major advantages of the 3-L NPC converter, which are reduced switching losses, improved VSC output waveform quality and reduced output ac filter. At the same time, the 3-L T-type converter shares the low conduction loss feature with the conventional 2-L converter [102]. This makes 3-L T-type converters a solution, between 2-L and 3-L NPC converters, for low-medium voltage medium-high power applications. The schematic and the detailed model of a typical T-type converter are presented in Chapter 2. Finally, Table 1.1 summarizes the main advantages and drawbacks of each

topology. The comparison is performed based on switching losses, conduction losses, output waveform quality, ac filter size, control complexity, and required extra hardware.

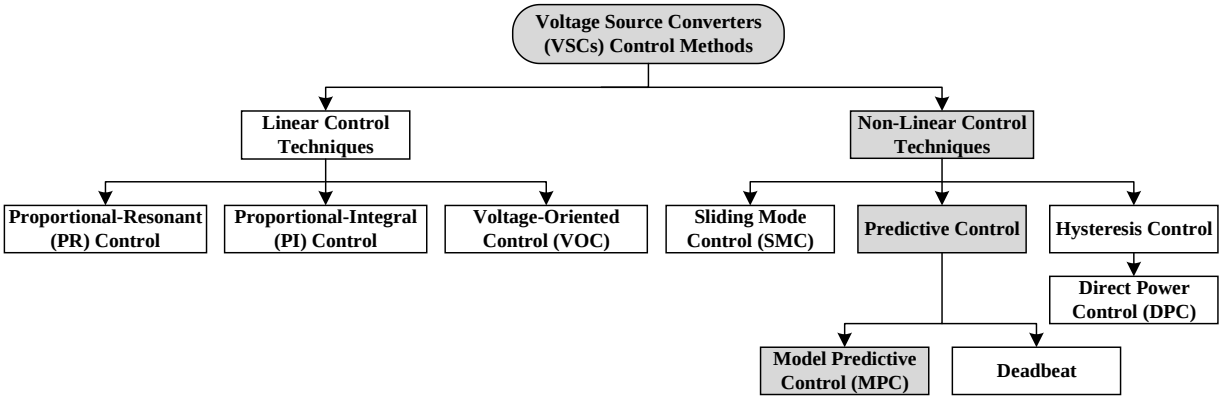


Figure 1.11: Flow chart of common control methods for VSCs.

1.3 Classification of Three-Phase 3-L VSC Control Methods

Various control techniques have been proposed for 3-L converters since the NPC converter was introduced. Usually, the same control strategies, which are used for the 2-L VSCs can be extended and implemented for the 3-L VSCs [107]. Generally, the control strategies which are applied on the 3-L VSCs can be either linear on nonlinear [108]. Shown in Figure 1.11 is a chart which categorizes and demonstrates the different types of control methods used for grid-following and grid-forming 3-L power converters.

1.3.1 Conventional Linear and Nonlinear Control Methods

As depicted in Figure 1.11, control schemes for 3-L VSCs can be in general classified as linear and nonlinear control strategies. Most of these control strategies are well developed, and they have been in use with different power electronic applications for decades [109].

Typically, to implement linear control strategies, a PWM modulator has to be cascaded with the current regulator. Following this design structure, the controller can exploit the merits of an open-loop modulator. These advantages mainly include a constant switching frequency and fixed harmonic spectrum [110]. The commonly deployed linear control schemes are the rotating-reference frame (RRF) and stationary-reference frame (SRF) proportional-integral (PI) control. The former is known for zero steady-state error since it forces the error, between the measured and reference signals, to be zero and ultimately achieves a good steady-state performance. Nevertheless, (RRF) transformation has to be applied such that the sinusoidal signals are converted to dc signals to be used in the control [111]. Since the dc signals, which are the direct and quadratic (*d* and *q*) axes, are time-invariant and dependent on each other, they disturb each other during the transient events, which deteriorates the controller overall performance [112]. The latter, i.e., SRF PR control, on the other hand, eliminates the steady-state error of a sinusoidal signal at a particular frequency by using infinite gains at the targeted frequency [113]. This simple control approach is sensitive to the fluctuations in the electric grid frequency, which may lead to instability during transients [112].

However, the main idea of linear control is to assume that the linearized system model is valid at a small range of operation. This limitation is exposed once a large operation range is the case. Operating a linear controller at a wider range could lead to instability or at most, poor performance. Assuming the model is fully linearizable is another problem associated with linear controllers. This is due to the fact that there are hard nonlinearities, which cannot be linearized due to their discontinuous nature. Model uncertainties contribute significantly to the deterioration of the linear controller's performance. Finally, linear control typically exhibits a complex control design due to the need for a modulation stage and signal transformations.

Therefore, for applications related to 3-L converters, where the fast-dynamic response and the certainty against parameter changes are desirable, nonlinear control strategies have shown considerable improvement in the system operation [108]. Some of the well-known nonlinear control methods are sliding mode control (SMC) and hysteresis control. Similar to the linear control methods, some of these nonlinear control strategies are known for being mature and well-established. For instance, hysteresis control, which includes direct power control (DPC), has been deployed on multiple power electronic applications. This control approach is known for being simple and effective in some applications. However, it suffers from the variable switching frequency, which may lead to resonance problems. Also, in order to improve the output waveform quality, hysteresis control has to be operated using high sampling time such that the controlled signal can always be within the defined hysteresis bands. Another powerful nonlinear control technique, which has been extensively implemented to 3-L VSCs, is model predictive control (MPC), which belongs to the family of predictive control. This control method is the core of this dissertation.

1.3.2 Finite Control Set Model Predictive Control (FCS-MPC)

Recently, with the advancement of microprocessors, finite-control-set model predictive control (FCS-MPC) methods have been extensively studied and implemented for various power electronics applications including motor drives, active power filters, grid-connected and stand-alone converters, etc. [114]-[117]. Several advantages of FCS-MPC, hereafter referred to as MPC, have contributed to the widespread use of MPC in power electronics including the fast-dynamic response and robustness against disturbances. The intuitive implementation of MPC and the ease in including the nonlinearities and the constraints in the controller design have also increased the popularity of this control method. Additionally, within the same control loop, multiple objectives

can be achieved simultaneously by using MPC, which augments the usefulness of MPC [114]-[117]. The main merits and demerits of MPC are demonstrated in Figure 1.12.

Generally, MPC exploits the discrete nature of power converters. The discrete-time converter model is usually used to predict the future behavior of state variables over a time horizon with a fixed step size, which is an integer-multiple of the controller sampling time. Then, a cost function with either sole or multiple objectives is required to evaluate the error between the controlled variables and their corresponding references. Finally, a finite number of possible switching states is evaluated using the cost function, sometimes referred to as a quality function, to select the optimal switching state, which results in the minimal value of the cost function [114]-[117].

Finally, it can be summarized that two main reasons, depicted in Figure 1.13, have contributed to the dramatic increase of MPC in power electronics applications. The first reason is that the power electronic converter characteristics which are the nonlinear model, the discrete nature, and the need to control different objectives. Secondly, the excessive development in today's control platforms, which has led to overcoming the high number of mathematical calculations dilemma.

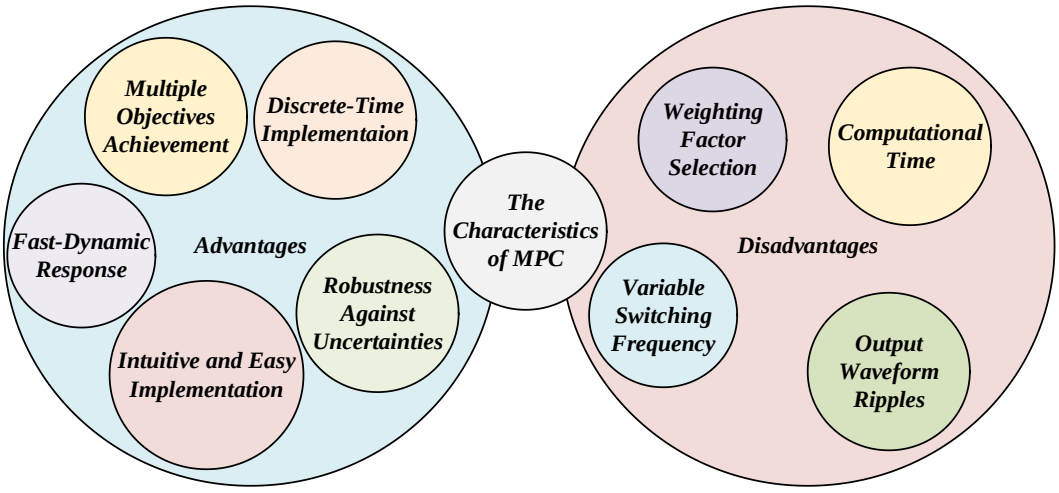


Figure 1.12: Advantages and drawbacks of FCS-MPC.

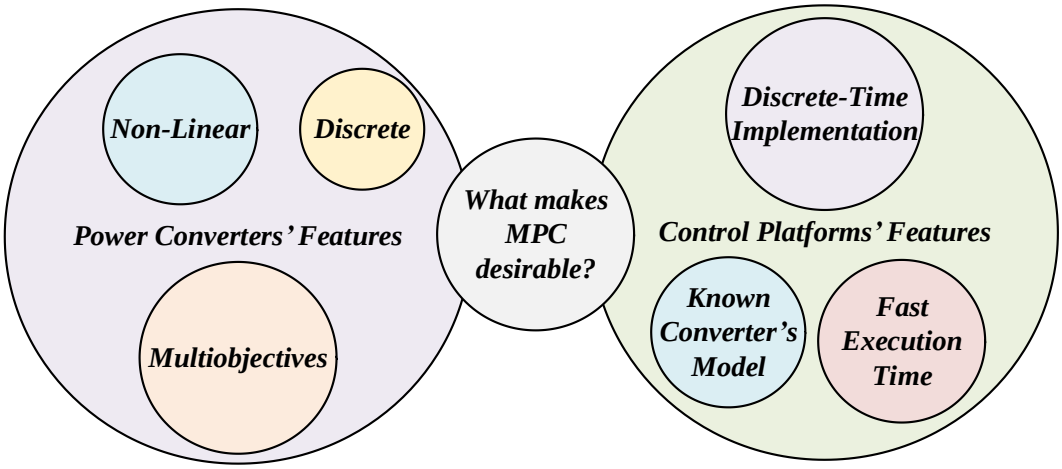


Figure 1.13: Reasons for FCS-MPC popularity in power electronics applications.

1.3.3 DC-Link Capacitor Voltages Control

Taking into considerations all the merits of 3-L VSCs and MPC, which have been previously described, this combination, MPC and 3-L converters, has been determined to be attractive for applications related to the DERs. However, other challenges are amplified as a result of this selection. To be more specific, despite the advantages of using 3-L VSCs, these converters may suffer from the unequal voltages between the two dc-link capacitors if the neutral-point voltage (NP-V) is not well-controlled [118]. The NP-V oscillations may even result in damaging the power semiconductor devices since some of them experience higher voltage stress than the others. Also, even moderate NP-V fluctuations can increase the harmonics in the converter output waveforms [99]. Therefore, to entirely exploit the advantages of the 3-L VSCs, the NP-V should be well-regulated. As a result of that, much research has been conducted to solve the NP-V oscillation issue for 3-L VSCs. Both linear and non-linear control methods such as the proportional-integral (PI) control and hysteresis control have been proposed [119]-[121]. This section focuses on the dc-link capacitor voltages control of the 3-L converters.

Thus far, the usefulness of the MPC has been validated on the 3-L VSCs. Typically, a 3-L VSC energized with a single dc voltage source requires MPC to use at least a dual-objective cost function, i.e., with one term dedicated to regulate the NP-V oscillations and other term(s) to achieve the primary control target(s) [122], [123]. Despite all advantages associated with MPC, the selection of weighting factors poses challenges, particularly when the number of the objectives is increased. In addition, an optimal selection for different weighting factors at a certain operating condition may be susceptible to the external disturbances and/or dynamic changes. Normally, designing proper weighting factors consumes a considerable amount of time and effort [124], [125].

Because the performance of the MPC is highly dependent on weighting factors, various MPC methods have been introduced to eliminate the weighting factors to enhance the performance of MPC. In [126], the weighting factor of the dc-link capacitor voltages balancing term has been eliminated from the cost function using a hierarchical control method. Nonetheless, a PI control, which is designed considering dc-link voltage dynamics that is ten times slower than that of MPC, was used specifically to regulate the NP-V fluctuations. This PI regulator not only increases the control complexity, but also decreases the system dynamic response. In [127], an MPC method using the discrete space vectors (DSVs) for a 3-L T-type VSC is proposed, which can reduce both the computational time and the output current ripples. However, the DSVs are designed without taking into consideration their impact on NP-V. Thus, a cost function is designed specifically to balance the dc-link capacitors voltages. In [128] and [129], the redundant voltage vectors are used to regulate the NP-V fluctuations without adding a term for the dc-link voltage balancing in the cost function. Nevertheless, this method cannot work if a medium voltage vector is the candidate to be selected by MPC, which limits the working region of the MPC to certain modulation indices.

Also, a vector shifted MPC method was proposed in [130] to simplify the cost function design. However, a proportional control, which requires tuning, is mandatory to adjust the dc-link capacitor voltages.

1.4 Research Objectives

The primary objective of the work presented in this dissertation is to develop a robust and effective MPC strategy specifically for the 3-L VSCs. The proposed MPC technique has the ability to overcome the challenges associated with the implementation of the classical MPC scheme on the 3-L VSCs. These resolved issues primarily include the complex cost function design, the high converter output waveform ripples, the expensive voltage/current sensors and the high execution time of the controller algorithm. The proposed MPC strategy, on the other hand, should retain the merits of the traditional MPC method, which essentially include the fast-dynamic response and robustness against parameter uncertainty.

The key objectives of the proposed MPC approach include

- Simplifying the MPC cost function design for the 3-L converters. This merit is accomplished by achieving inherent balanced dc-link capacitor voltages. As a result, the time-consuming weighting factors selection and tuning can be eliminated.
- Achieving significantly reduced NP-V oscillations of the dc-link capacitor voltages. This major advantage can be achieved by using the concept of the virtual space vectors (VSVs), which generate zero NP-C, which ultimately does not contribute in the NP-V oscillations.
- Reducing the converter output waveforms ripples. This merit can be realized as a result of the increased average switching frequency due to the use of the VSVs as well as the significantly reduced NP-V fluctuations. Having a smaller number of objectives in the cost

function also ensures the controller primary objective(s) receive more control attention and effort.

- Decreasing the system overall cost as less voltage/current sensors are used. This advantage is accomplished because the proposed MPC algorithm can achieve inherent dc-link capacitor voltages balancing, which eliminates the need to using voltage/current sensors to regulate the dc-link capacitor voltages.
- Improving the system overall reliability as less sensor boards and feedback signals are used. This contribution reduces the chances of hardware failure. This advantage not only reduces the total cost and improves the system reliability as less hardware is required, but also decreases the size, weight and wiring complexity of the system.
- Reducing the controller execution time, which is accomplished as a result of the simplified MPC algorithm design. Since the cost function of the proposed MPC strategy does not include terms related to the NP-V regulation, predictive equations of the dc-link capacitor voltages are eliminated from the code, which reduces the number of calculations to be performed within a control sampling period.

1.5 Dissertation Organization

The rest of this dissertation is structured in the following manner

- Chapter 2 provides a comprehensive description for two common 3-L converter topologies; NPC and T-type converters. These topologies are modeled in this chapter considering the discrete nature of the power converters. Then, the dc-link of 3-L VSC topologies is modeled in continuous and discrete time. Brief reviews for different converter output ac filters followed by the continuous- and discrete-time derivation for these filters' models

are also provided. After that, a synchronization technique, i.e., synchronous reference frame phase locked loop (SRF-FLL), has been reviewed in detail. The control gains of the SRF-PLL have been also derived in continuous and discrete time.

- Chapter 3 describes the conventional MPC for 3-L NPC converters considering different power converter operating modes. An enhanced MPC for 3-L NPC converters, which uses the concept of the VSVs, is then described and compared with the conventional one. The implementation of the proposed MPC gate signals is also presented in this chapter. The 3-L NPC VSC efficiency analysis is also demonstrated. This chapter is concluded by providing simulation results which are validated using controller hardware-in-the-loop (HIL) studies.
- Chapter 4 explains and introduces both the conventional and proposed model predictive voltage control (MPVC) methods for the 3-L T-type converters. Additionally, the T-type gating signals generation is demonstrated. The topology efficiency analysis is also discussed, considering the typical and proposed MPVC. Comprehensive simulation results are also included. Finally, the experimental test setup is shown followed by comprehensive experimental results which verify the theoretical analysis and simulation studies.
- Chapter 5 includes the dissertation conclusions, contributions and recommendations for future research wok.

CHAPTER 2

MODELING OF THE GRID-CONNECTED AND STAND-ALONE CONVERTER SYSTEMS

2.1 Introduction

Three-level (3-L) VSC topologies, which include the neutral-point clamped (NPC) and the T-type VSCs, have been extensively used in grid-connected and stand-alone microgrids (MG) applications despite the advantages and drawbacks, which distinguish these topologies. Typically, the common control schemes of the VSCs in an MG are the grid-following and grid-forming VSCs. On the one hand, when a VSC is operated in a grid-following mode, an *LCL* filter is usually used as an interface between the VSC topology and the main electric grid to suppress the high-frequency harmonic contents, generated by the power switches of the VSCs. The main control objective in the grid-interfaced VSCs is usually the *LCL*-filter input/output current. On the other hand, when designing a system for grid-forming applications, an *LC* filter can serve as an interface between the selected topology and the load to provide high-quality output voltage. For stand-alone systems, the *LC*-filter capacitor voltage is usually the control aim.

Therefore, in order to design a finite-control-set model predictive control (FCS-MPC) strategy for grid-connected and stand-alone MG applications, it is essential to not only determine the model for the selected topology, but also the models for the chosen ac passive filter, which can be either *LCL* or *LC* filter. Since the work of this dissertation concentrates on 3-L VSC topologies, developed models for the dc-link capacitors are also unavoidable to be used for the neutral-point voltage (NP-V) regulations. As a result, this chapter starts by providing a generic discrete model for the 3-L VSC. Then, the continuous- and discrete-time mathematical models for the 3-L VSC dc-link capacitors are explained. Because the different VSCs are tied to the load/grid through ac

LC/*LCL* filters, the continuous- and discrete-time mathematical models for such ac passive filters have been also derived and presented in this chapter so that they can be used in the digital controller. Finally, for an MG with the grid-connected VSCs, it is always important to ensure the synchronization of the various VSCs with the electric utility voltage in order to accomplish efficient energy transfer between the converter and the ac mains. Thus, a continuous-time model, represented in the S-domain followed by a discrete-time model, shown in the Z-domain, for the synchronous-reference frame phase-locked loop (SRF-PLL) have been derived and presented in this chapter.

2.2 Modeling of Generic Three-Phase 3-L VSCs

On the one hand, for medium- to high-voltage high-power MG applications, the 3-L NPC VSCs, similar to the one displayed in Figure 2.1, have replaced the traditional 2-L VSCs due to multiple advantages. First, in a 3-L VSC topology, the voltage stress across the power semiconductor switches is reduced by half compared to the voltage, which is seen by the power switches of a 2-L VSC topology. This merit not only allows increasing the dc-bus voltage of a 3-L VSC so that more power can be transferred, but also contributes in substantial reduction in the power semiconductor devices switching losses. Relative to the typical 2-L VSCs, the use of the 3-L VSCs has also resulted in high-quality VSC output waveforms. Hence, the size of the ac passive filters, used to link various VSCs in the MG, is considerably reduced, which improves the system efficiency. Therefore, all the aforementioned merits have contributed in the wide-spread use of 3-L VSCs for MG applications. However, despite the merits of using 3-L NPC in MG applications, the conduction power loss associated with the 3-L VSCs are higher than those generated by classical 2-L VSCs due to the increase number of the switching devices per phase leg. Thus, for low- to medium-voltage high-power applications, a 3-L T-type VSC topology, has been lately

proposed to be an alternative to the conventional 2-L and 3-L NPC VSCs. This topology presents low conduction losses, similar to 2-L converters, while maintaining the advantages of 3-L NPC converters.

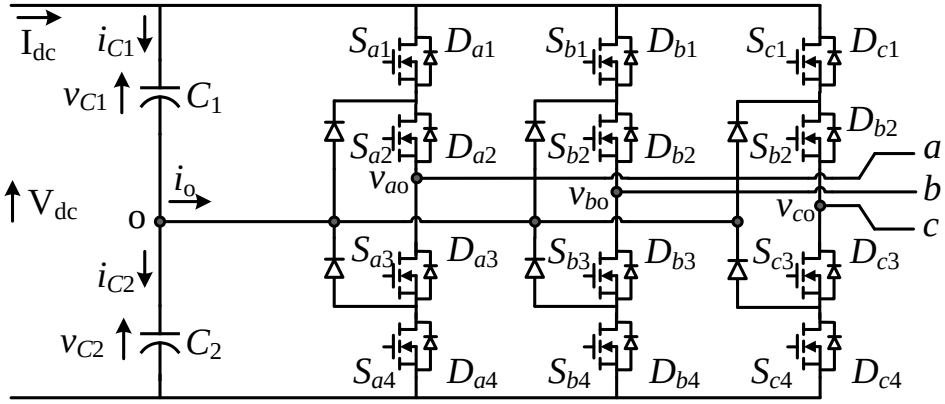


Figure 2.1: Schematic of a three-phase 3-L NPC VSC.

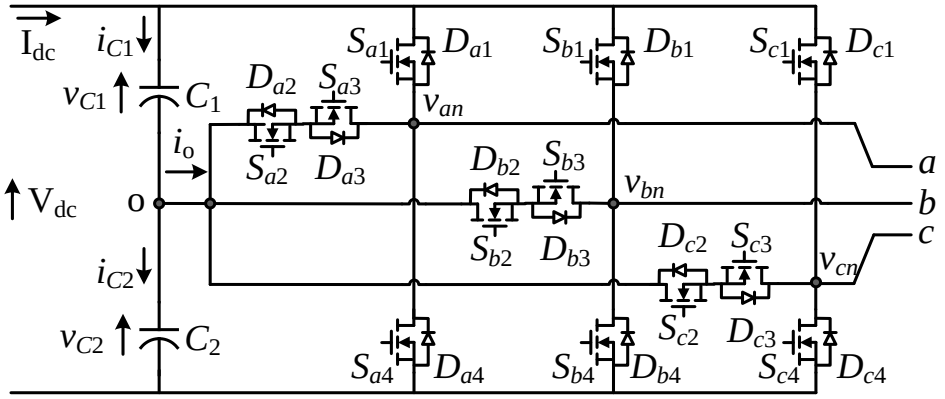


Figure 2.2: Schematic of a three-phase 3-L T-type VSC.

Shown in Figure 2.1 is the schematic of the three-phase 3-L NPC VSC. Each phase of this topology is composed of four power semiconductor devices, S_{x1}, S_{x2}, S_{x3} and S_{x4}, with four anti-parallel diodes, D_{x1}, D_{x2}, D_{x3} and D_{x4}, and two clamping diodes. Taking phase leg *a* of the NPC VSC topology that is shown in Figure 2.1 as an example, the four active power electronics switches are S_{a1}, S_{a2}, S_{a3} and S_{a4} while the anti-parallel diodes, connected across each of the four power switches, are D_{a1}, D_{a2}, D_{a3} and D_{a4}. Additionally, the clamping diodes can be seen connecting the

point between the upper power switches and the point between the lower power switches to the dc-link neutral point (NP). Similarly, the complete circuit diagram of a generic three-phase 3-L T-type VSC is depicted in Figure 2.2. Unlike the 3-L NPC VSCs, the 3-L T-type VSC does not require having clamping diodes, which reduces the components needed to structure the topology. Nonetheless, the 3-L T-type VSC still require four active power electronic switches with their anti-parallel diodes to compose one phase leg, as displayed in Figures 2.2.

Although the structure of the 3-L NPC VSC is different than that of the 3-L T-type VSC, both topologies share the same converter discrete model. Thus, the rest of section 2.2 in this chapter focuses on describing a generic model for the three-phase 3-L VSCs. To illustrate the 3-L VSC model, each phase of the NPC and T-type VSCs has four switch positions, e.g., S_{a1}, S_{a2}, S_{a3} and S_{a4} in phase *a*. The inverter output phase voltage with respect to the dc-link NP o, which is denoted by v_{xo}, is determined by the applied switching state variable (S_x) of the phase leg *x*, where x = [12]. For a 3-L VSC, which can be either NPC or T-type inverter, the S_x has three possible values, i.e., +1, 0, and –1, which were denoted as +, 0, and –, in this work. Assuming equal dc-link capacitor voltages, i.e., $v_{C1} = v_{C2}$, the three possible values of S_x, which result in $V_{dc}/2$, 0, and $-V_{dc}/2$ at the terminals of the inverter, are defined as in (2.1). Summarized in Table 2.1 is the relationship among the state of each switch position, S_x, and the converter output phase voltage v_{xo} [122]-[132].

$$v_{xo} = S_x \frac{V_{dc}}{2} \tag{2.1}$$

where

$V_{dc} = v_{C1} + v_{C2}$;

$x = \{a, b, c\}$.

Table 2.1
Relationship Between Switching State (S_x) and Terminal Voltage (v_{xo})

S_x	S_{x1}	S_{x2}	S_{x3}	S_{x4}	v_{xo}
+	1	1	0	0	$V_{dc}/2$
0	0	1	1	0	0
–	0	0	1	1	$-V_{dc}/2$

Considering all possible combinations of the switching states among the three phases of the 3-L converter, a total of 27 active voltage space vectors are produced. By using (2.2), the voltage space vectors are generated to be used in the converter model.

$$\mathbf{V} = \frac{2}{3}(v_{ao} + \mathbf{a} \cdot v_{bo} + \mathbf{a}^2 \cdot v_{co}) \tag{2.2}$$

where

v_{ao}, v_{bo} and v_{co} inverter L-to-N output voltages;

$\mathbf{a} = e^{j2\pi/3}$ unitary vector.

Presented in Figure 2.3 is the SV diagram of the three-phase 3-L VSCs, which has 19 non-redundant voltage space vectors. In this SV diagram, the voltage space vectors are classified into four categories. These categories include the zero voltage vectors V_0, the small voltage vectors V_{Si}, the medium voltage vectors V_{Mi} and the large voltage vectors V_{Li}, where j = 1,2,3 and i = 1, …, 6. The neutral-point current (NP-C) associated with every switching state of these 27 voltage vectors are also presented in brackets as shown in Figure 2.3. Although the three-phase 3-L NPC converters have different configuration than the three-phase 3-L T-type converters, they both share the same converter model and SV diagram, which is presented in Figure 2.3. Finally, summarized in Table 2.2 is the 27 different switching states and the corresponding voltage space vectors of every switching state.

Table 2.2
The Switching States (S_x) and the Voltage Space Vectors ($\mathbf{V}_i$) of the Three-Phase 3-L VSC

S_a	S_b	S_c	$\mathrm{V_i}$
–	–	–	$\mathbf{V}_0 = 0$
0	0	0	
+	+	+	
+	0	0	$\mathbf{V}_{S1} = (1/3)\,\mathrm{V_{dc}}$
0	–	–	
+	+	0	$\mathbf{V}_{S2} = (1/6)\,\mathrm{V_{dc}} + j(\sqrt{3}/6)\,\mathrm{V_{dc}}$
0	–	–	
0	+	0	$\mathbf{V}_{S3} = (-1/6)\,\mathrm{V_{dc}} + j(\sqrt{3}/6)\,\mathrm{V_{dc}}$
–	0	–	
0	+	+	$\mathbf{V}_{S4} = (-1/3)\,\mathrm{V_{dc}}$
–	0	0	
0	0	+	$\mathbf{V}_{S5} = (-1/6)\,\mathrm{V_{dc}} - j(\sqrt{3}/6)\,\mathrm{V_{dc}}$
–	–	0	
+	0	+	$\mathbf{V}_{S6} = (1/6)\,\mathrm{V_{dc}} - j(\sqrt{3}/6)\,\mathrm{V_{dc}}$
0	–	0	
+	0	–	$\mathbf{V}_{M1} = (1/2)\,\mathrm{V_{dc}} + j(\sqrt{3}/6)\,\mathrm{V_{dc}}$
0	+	–	$\mathbf{V}_{M2} = j(\sqrt{3}/3)\,\mathrm{V_{dc}}$
–	+	0	$\mathbf{V}_{M3} = (-1/2)\,\mathrm{V_{dc}} + j(\sqrt{3}/6)\,\mathrm{V_{dc}}$
–	0	+	$\mathbf{V}_{M4} = (-1/2)\,\mathrm{V_{dc}} - j(\sqrt{3}/6)\,\mathrm{V_{dc}}$
0	–	+	$\mathbf{V}_{M5} = -j(\sqrt{3}/3)\,\mathrm{V_{dc}}$
+	–	0	$\mathbf{V}_{M6} = (1/2)\,\mathrm{V_{dc}} - j(\sqrt{3}/6)\,\mathrm{V_{dc}}$
+	–	–	$\mathbf{V}_{L1} = (2/3)\,\mathrm{V_{dc}}$
+	+	–	$\mathbf{V}_{L2} = (1/3)\,\mathrm{V_{dc}} + j(\sqrt{3}/3)\,\mathrm{V_{dc}}$
–	+	–	$\mathbf{V}_{L3} = (-1/3)\,\mathrm{V_{dc}} + j(\sqrt{3}/3)\,\mathrm{V_{dc}}$
–	+	+	$\mathbf{V}_{L4} = (-2/3)\,\mathrm{V_{dc}}$
–	–	+	$\mathbf{V}_{L5} = (-1/3)\,\mathrm{V_{dc}} - j(\sqrt{3}/3)\,\mathrm{V_{dc}}$
+	–	+	$\mathbf{V}_{L6} = (1/3)\,\mathrm{V_{dc}} - j(\sqrt{3}/3)\,\mathrm{V_{dc}}$

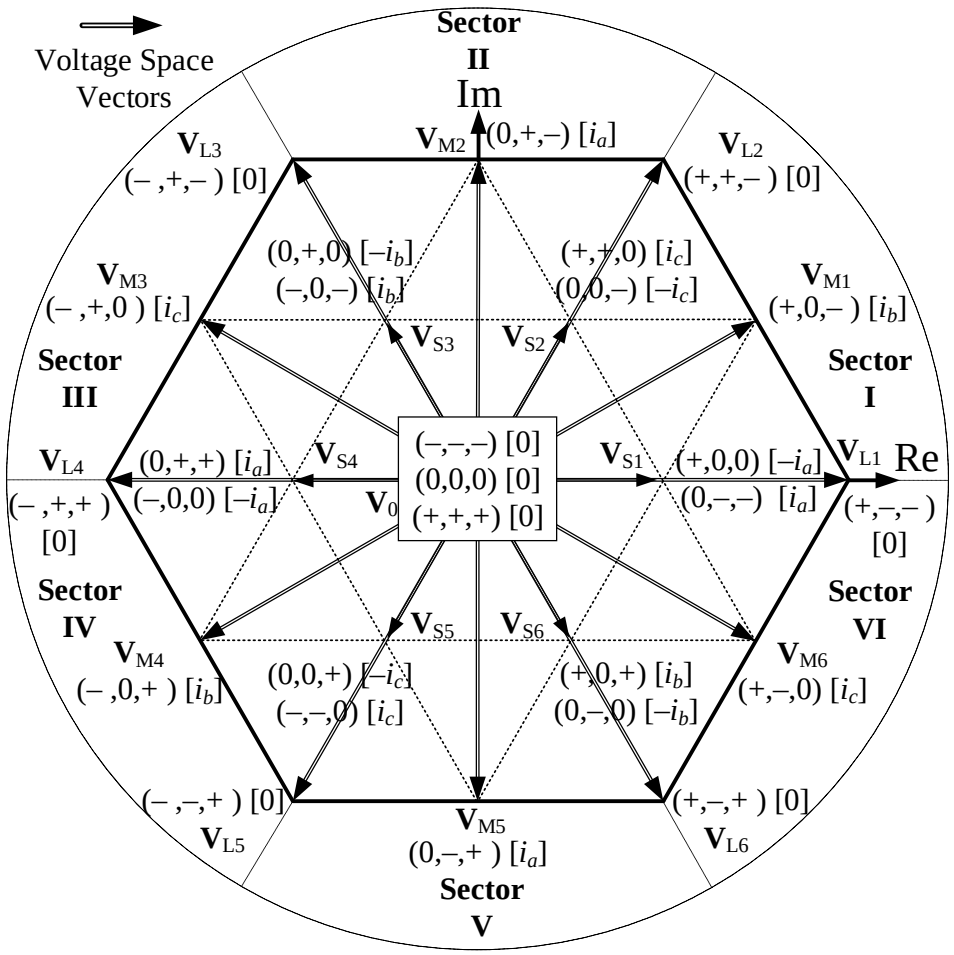


Figure 2.3: SV diagram of the three-phase 3-L VSCs.

2.3 Modeling of the DC Link

One main challenge when controlling a 3-L VSC is balancing the dc-link capacitor voltages. Therefore, to properly regulate the voltages across the two dc-link capacitors, the discrete models for the dc-link capacitor voltages have to be derived. As a result, in this section, the continuous-time model for the dc-link capacitor voltages firstly derived before it is discretized such that it can be used in the digital controller practical implementation.

2.3.1 Continuous-Time Model for the DC-Link

By applying the Kirchhoff Current Law (KCL) on the upper and lower dc-link capacitors, the dc-link capacitor voltages differential equations for the upper and lower capacitors, i.e., v_{C1} and v_{C2}, respectively, can be determined as expressed in (2.3) and (2.4).

$$\frac{dv_{C1}}{dt} = \frac{i_{C1}}{C_1} \tag{2.3}$$

$$\frac{dv_{C2}}{dt} = \frac{i_{C2}}{C_2} \tag{2.4}$$

where

C_1 and C_2	upper and lower dc-link capacitors;
v_{C1} and v_{C2}	voltages across the dc-link capacitors;
i_{C1} and i_{C2}	currents flowing through the dc-link capacitors.

2.3.2 Discrete-Time Model for the DC-Link

After deriving the continuous-time differential equations of the dc-link capacitor voltages, the Forward Euler approximation method with a sampling time T_s, which is expressed in (2.5), is used to obtain the discrete-time differential equations of the dc-link capacitor voltages as presented in (2.6) and (2.7).

$$\frac{dv_{C1,2}}{dt} \approx \frac{v_{C1,2}(k+1) - v_{C1,2}(k)}{T_s} \tag{2.5}$$

$$v_{C1}(k+1) \approx v_{C1}(k) + \frac{T_s}{C_1} i_{C1}(k) \tag{2.6}$$

$$v_{C2}(k+1) \approx v_{C2}(k) + \frac{T_s}{C_2} i_{C2}(k) \tag{2.7}$$

where k and $k + 1$ represent two consecutive sampling periods.

The currents flowing through the upper and lower dc-link capacitors, i.e., i_{C1} and i_{C2}, at sampling instant k are also predicted to avoid using current sensors. The dc current, I_{dc}, supplied by the dc voltage source, V_{dc}, the applied switching state variable, S_x, and the measured three-phase inverter current, $i_{c,abc}$ at sampling instant k, are used in (2.8) and (2.9) to calculate the dc-link capacitor currents as follows

$$i_{C1}(k) = \mathrm{I}_{\mathrm{dc}}(k) - H_{1a} i_{c,a}(k) - H_{1b} i_{c,b}(k) - H_{1c} i_{c,c}(k) \tag{2.8}$$

$$i_{C2}(k) = \mathrm{I}_{\mathrm{dc}}(k) + H_{2a} i_{c,a}(k) + H_{2b} i_{c,b}(k) + H_{2c} i_{c,c}(k) \tag{2.9}$$

where

$H_{1x} = 1$ if $S_x =$ "+", otherwise $H_{1x} = 0$;

$H_{2x} = 1$ if $S_x =$ "–", otherwise $H_{2x} = 0$;

$x = \{a, b, c\}$.

2.4 Modeling of the VSC Output *LC* and *LCL* Filters

For MG applications, the most common kinds of harmonic filters are *L*, *LC* and *LCL* filters. Typically, the *L* and the *LCL* filters are used to interface VSCs, which have the grid injected current as a controlled variable, with the main electric grid [133]. On the contrary, the *LC* filters are used to help operating power converters as grid-forming VSCs, which perform voltage control [134], [135]. In this section of this chapter, the two common kinds of the harmonics filters, which are the *LC* and the *LCL* filters, are described in detail. The continuous-time modeling of these filters is firstly derived. Then, the discrete-time of these models are obtained.

2.4.1 Modeling of the LC Filter

For stand-alone VSC systems such as uninterruptible power supplies (UPSs), the *LC* filters are usually used at the output of these converters to serve as a connection between the topology and the critical loads so that converters switching ripples are mitigated [136]. The *LC* filter is typically made of a single inductor and a single capacitor. While the *LC*-filter inductor, i.e., *L*, is used to provide considerably high impedance, which can block the high-frequency current components, the *LC*-filter capacitor, i.e., *C*, ensures substantially low impedance to bypass the current components at high frequencies [137].

In general, the UPSs, which have the *LC*-filter capacitor voltage as the controlled variable, have to be well-controlled; otherwise resonances may lead to an oscillatory behavior, which can eventually cause to system instability [138]. Typically, for control techniques, which have a fixed switching frequency, designing the *LC* filter should be simple as the *L* and *C* can be selected to have a resonant frequency that is considerably lower than the switching frequency. Following this design method ensures that the frequency of the lowest harmonic component is always higher than the controller resonant frequency. In the contrary, designing the *LC* filter for control methods with variable average switching frequency is more challenging since the lowest harmonic component may have a frequency that is lower than the controller average switching frequency [139].

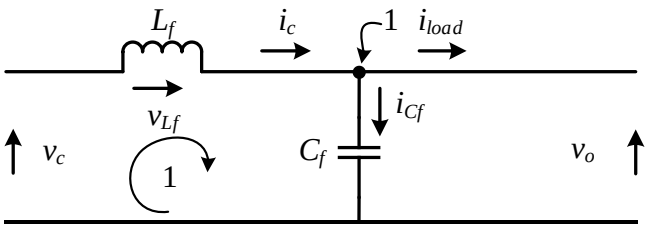


Figure 2.4: One-line diagram of an *LC* filter.

Figure 2.4 shows the one-line diagram of an output *LC* filter, which is made of an inductor, *L* and a capacitor *C*. The continuous-time state-space model of this *LC* filter is derived in this chapter; the discrete-time state-space model, then, is calculated.

2.4.1.1 Continuous-Time Model for the LC Filter

The continuous-time model for the *LC* filter can be determined by deriving the differential equations for the *LC*-filter input current, i_c, and *LC*-filter capacitor voltage, v_o. This can be achieved by applying the Kirchhoff Voltage Law (KVL) and the Kirchhoff Current Law (KCL) on loop 1 and node 1, shown in Figure 2.4, respectively. Then, the derived differential equations are organized in the state-space form as expressed in (2.10) [140].

$$\frac{dx}{dt} = Ax + B_1 v_c + B_2 i_{load} \tag{2.10}$$

where

$$x = \begin{bmatrix} i_c \\ v_o \end{bmatrix};$$

$$A = \begin{bmatrix} 0 & -1/L_f \\ 1/C_f & 0 \end{bmatrix};$$

$$B_1 = \begin{bmatrix} 1/L_f \\ 0 \end{bmatrix};$$

$$B_2 = \begin{bmatrix} 0 \\ -1/C_f \end{bmatrix}.$$

where

L_f *LC*-filter inductor;

C_f *LC*-filter capacitor;

v_c converter output voltage;

i_c converter-side current;

i_{load} load-side current;

v_o load voltage.

2.4.1.2 Discrete-Time Model for the LC filter

The discrete-time state-space model of the *LC* filter is obtained by discretizing (2.10) with a sampling time, T_s, and expressed [140] as expressed in (2.11). This discretized model is used in the digital controller implementation.

$$x(k+1) = Ax(k) + B_1 v_c(k) + B_2 i_g(k) \tag{2.11}$$

where

$$A = e^{AT_s};$$

$$B_1 = \int_0^{T_s} e^{AT_s} B_1 dt;$$

$$B_2 = \int_0^{T_s} e^{AT_s} B_2 dt.$$

where

k and $k + 1$ two consecutive sampling periods;

T_s controller sampling time.

2.4.2 Modeling of the LCL filter

For grid-connected VSCs, the converter switching harmonics are usually attenuated using either an *L* filter or an *LCL* filter. On the one hand, the *L* filter, which can be modeled as a first-

order system, is simply designed using a single inductor. The merit of this simple design is the use of an uncomplicated controller with such system. On the other hand, the *LCL* filter, which is formed using a combination of two inductors and a single capacitor, can be realized as a third-order system. This system has two complex poles, which contribute into resonant frequencies. These resonant frequencies require careful attenuation when designing the controller such that a stable closed-loop system is accomplished [141]. Although the *L* filter has a much simpler design compared to the *LCL* filter, the latter presents considerably better attenuation for the harmonics, and it substantially reduces the ac filter volume [142]. These advantages of the *LCL* filter have contributed in the wide employment of this passive filter in grid-connected VSC applications [133].

Considering the *LCL* filter operation, the high-frequency harmonics of the current waveforms are bypassed using the capacitor since it provides a near-zero impedance path for these contents. The use of the *LCL* filter results in improving the quality of the VSC output waveforms, and it allows using significantly smaller inductors values relative to the *L* filter. However, using the *LCL* filter leads to have resonance at a certain range of frequencies, which may result in having current waveforms oscillations. These oscillations can further lead to have system instability if the resonant peaks are not damped. Therefore, different damping techniques have been proposed. Traditionally, passive damping, which can be achieved by including an actual resistor into the filter design, has been firstly used. The two common ways to connect the passive resistor is either in series or in parallel with the filter capacitor. Later, active damping, which uses a virtual resistor, have been implemented to improve the converter overall efficiency [75], [143].

In this work, the classical passive damping method, using a resistor connected in series with the *LCL*-filter capacitor, has been chosen due to the easy implementation and effectiveness in

damping the peak resonances. Presented in Figure 2.5 is the one-line diagram of an *LCL* filter, which is composed of two inductors, L_1 and L_2, a capacitor C_f and a damping resistor, R. Similar to the *LC* filter, the continuous-time state-space model of the *LCL* filter has to be derived. Then, the discrete-time state-space model for the *LCL* filter can be obtained from the continuous-time model such that it can be practically implemented in the controller.

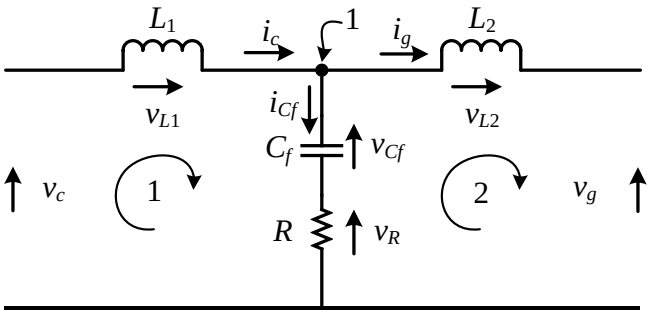


Figure 2.5: One-line diagram of an *LCL* filter.

2.4.2.1 Continuous-Time Model for the LCL filter

By applying the KVL on loop 1 and loop 2, shown in Figure 2.5, the converter-side current, i_c, and the grid-side current, i_g, differential equations are derived. Then, the KCL has been applied on node 1, shown in Figure 2.5, to derive the *LCL*-filter capacitor voltage, v_{Cf}, differential equation. After that, the continuous-time state-space system of the *LCL* filter is formed in a continuous-time state-space model as expressed in (2.12).

$$\frac{dx}{dt} = Ax + Bu \tag{2.12}$$

where

$$x = \begin{bmatrix} i_c \\ i_g \\ v_{Cf} \end{bmatrix};$$

$$A = \begin{bmatrix} -R/L & R/L & -1/L \\ R/L & -R/L & 1/L \\ 1/C_f & -1/C_f & 0 \end{bmatrix};$$

$$u = \begin{bmatrix} v_c \\ v_g \end{bmatrix};$$

$$B = \begin{bmatrix} 1/L_1 & 0 \\ 0 & -1/L_2 \\ 0 & 0 \end{bmatrix}.$$

where

L_1 and L_2	*LCL*-filter inductors;
C_f	*LCL*-filter capacitor;
R	*LCL*-filter damping resistor;
v_c	converter output voltage;
v_{Cf}	*LCL*-filter capacitor voltage;
i_c	converter-side current;
i_g	grid-side current;
v_g	grid voltage.

2.4.2.2 Discrete-Time Model for the LCL filter

Then, the discrete-time state-space model of the *LCL* filter is obtained by applying the forward Euler approximation approach with a sampling time T_s and expressed in (2.13).

$$x(k+1) = A_d x(k) + B_d u(k) \tag{2.13}$$

where

$$x(k+1)=\begin{bmatrix} i_c(k+1) \\ i_g(k+1) \\ v_{Cf}(k+1) \end{bmatrix};$$

$$x(k)=\begin{bmatrix} i_c(k) \\ i_g(k) \\ v_{Cf}(k) \end{bmatrix};$$

$$A_d=\begin{bmatrix} 1-RT_s/L_1 & RT_s/L_1 & -T_s/L_1 \\ RT_s/L_2 & 1-RT_s/L_2 & T_s/L_2 \\ T_s/C_f & -T_s/C_f & 1 \end{bmatrix};$$

$$u(k)=\begin{bmatrix} v_c(k) \\ v_g(k) \end{bmatrix};$$

$$B_d=\begin{bmatrix} T_s/L_1 & 0 \\ 0 & -T_s/L_2 \\ 0 & 0 \end{bmatrix}.$$

where

k and $k+1$	two consecutive sampling instants;
T_s	controller sampling time.

2.5 Modeling of the SRF-PLL

In grid-tied VSC applications, the electric grid synchronization is a critical concept for having accurate and safe operation for the grid-interfaced MGs, which consist normally of various grid-connected VSCs, with the electric grid [64]. The electric grid synchronization is defined as an instantaneous monitoring for the status of the electric grid, to which one or multiple VSCs are connected. To explain, the synchronization of the VSCs with the electric utility is a mandatory task to ensure that the DERs are actively connected to the electric grid. Among different power

synchronization techniques, the PLLs have been dominantly used in several electrical applications, such as the grid-tied VSC applications. A PLL is generally defined as a non-linear closed loop system, which has an output signal that is synchronized with the input reference signal's angle and frequency. To illustrate, the PLL is utilized in the grid-tied MG applications to provide an instantaneous information regarding the phase angle and the amplitude of the electric grid fundamental voltage [144]. Typically, a PLL is designed using a phase detector (PD), a loop filter (LF) and a voltage-controlled oscillator (VCO). The implementation of the PD is usually the main difference among the different types of the PLLs. In the work presented in this dissertation, the SRF-PLL, which has the detailed structural block diagram displayed in Figure 2.6, is considered to be implemented in the grid-connected MGs due to the fact that it has an easy and straightforward implementation [145]. The SRF-PLL shows also a good performance during ideal electric grid conditions whose balanced three-phase voltage is purely sinusoidal [146]. The three essential components of the SRF-PLL are described as follows [147].

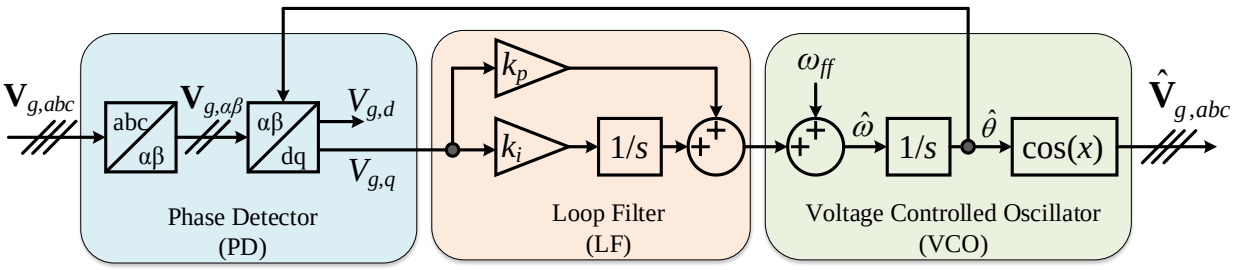


Figure 2.6: Control block diagram of an SRF-PLL.

- **A phase detector (PD)**: This block has two inputs, which are the input signal, $\mathbf{V}_{g,abc}$, and the output of the voltage-controlled oscillator (VCO), $\hat{\mathbf{V}}_{g,abc}$. The output of the PD is described as a signal which is proportionally related to the input signals' phase difference.

- **A loop filter (LF)**: The main purpose of using this block is to provide attenuation against the high-frequency components in the ac waveform coming from the PD. Normally, either a low-pass filter or a PI controller is used in this block.
- **A voltage-controlled oscillator (VCO)**: The ac signal, $\hat{\mathbf{V}}_{g,abc}$, is produced using this block. The frequency of the produced ac signal, $\hat{\omega}$, is determined by a reference frequency, ω_{ff}, that is shifted by the output of the LF.

In this section of this chapter, the S-domain model for an SRF-PLL has been first introduced. Then, the Z-domain model has been derived so that the SRF-PLL can be applied in the digital controller [148].

A closed loop SRF-PLL is designed using the Park and the Clarke transformations to work as a PD, a PI controller to represent the LF, and an integrator, which can work as a VCO. To design an SRF-PLL, similar to the one demonstrated in Figure 2.6, a two-step transformation, i.e., the Park and Clarke transformations, are firstly used to detect the phase difference between the input and the output signals. This phase error is represented by the electric grid quadrature voltage, $V_{g,q}$. Then, in order to lock the input and output signals together, $V_{g,q}$ must be forced to zero. In order to achieve that, the output of the PD, $V_{g,q}$, is passed through a PI controller, which regulates the phase error to zero. The output of the PI controller is then passed through the VCO. In the VCO, the estimated frequency, $\hat{\omega}$, is produced by adding the PI controller output to the defined reference frequency, ω_{ff}, before it is integrated such that an estimated phase angle, $\hat{\theta}$, is finally accomplished.

The Park and Clarke transformation have to be applied for the three-phase voltage vector, $\mathbf{V}_{g,abc}$ expressed in (2.14), which is assumed to be the PLL input voltage.

$$\mathbf{V}_{g,abc} = \begin{bmatrix} v_{g,a} \\ v_{g,b} \\ v_{g,c} \end{bmatrix} = \begin{bmatrix} V_g \cos(\theta_g) \\ V_g \cos(\theta_g - (2\pi/3)) \\ V_g \cos(\theta_g + (2\pi/3)) \end{bmatrix} \tag{2.14}$$

First, the Clarke transformation is implemented to obtain the matrix form of the three-phase voltage vector, $\mathbf{V}_{g,abc}$, in the stationary-reference frame, αβ0-reference frame, by applying (2.15).

$$\mathbf{V}_{g,\alpha\beta 0} = \begin{bmatrix} v_{g,\alpha} \\ v_{g,\beta} \\ v_{g,0} \end{bmatrix} = \frac{2}{3} \overbrace{\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & -\sqrt{3}/2 & \sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix}}^{T_{\alpha\beta 0}} \times \mathbf{V}_{g,abc} \tag{2.15}$$

Second, the Park transformation is applied such that the output of the PD is two dc quantities, which are represented in the synchronous-reference frame, dq0-reference frame. Presented in (2.16) is the dq0-reference frame voltages, $\mathbf{V}_{g,dq0}$.

$$\mathbf{V}_{g,dq0} = \begin{bmatrix} V_{g,d} \\ V_{g,q} \\ V_{g,0} \end{bmatrix} = \frac{2}{3} \overbrace{\begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 \\ -\sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix}}^{T_{dq0}} \times \mathbf{V}_{g,\alpha\beta 0} \tag{2.16}$$

Solving (2.16) and neglecting the zero component, $V_{g,0}$, yields

$$\mathbf{V}_{g,dq} = \begin{bmatrix} V_{g,d} \\ V_{g,q} \end{bmatrix} = \begin{bmatrix} V_g \cos(\hat{\theta} - \theta_g) \\ V_g \sin(\hat{\theta} - \theta_g) \end{bmatrix} \tag{2.17}$$

Now, having a phase difference between the estimated output signal and the input signal that is equal to zero, i.e., $\hat{\theta} = \theta_g$, means both signals are locked with each other. Furthermore, it is possible to calculate the voltage vector magnitude by using (2.18).

$$V_g = \sqrt{V_{g,d}^2 + V_{g,q}^2} \tag{2.18}$$

Since having a zero-error phase difference, i.e., $\hat{\theta} = \theta_g$, yields to have $V_{g,q} = 0$, the magnitude of the voltage vector is calculated as $V_g = V_{g,d}$. Therefore, it can be concluded that during ideal electric grid conditions, i.e., purely sinusoidal and balanced three-phase voltage, an SRF-PLL has the capability to output the information, which includes the frequency, $\hat{\omega}$, the phase angle, $\hat{\theta}$, and the voltage amplitude, $V_{g,d}$.

2.5.1 Design of the Proportional-Integral (PI) Control Gains in S-Domain

In this subsection, the design of the PI control gains, i.e., k_p and k_i, is demonstrated in the continuous time, referred to as the s-domain. Since the PI controller is designed for the SRF-PLL, which is used for grid-connected applications, the electric grid voltage vector, $\mathbf{V}_{g,abc}$, expressed in (2.14), is assumed to be the SRF-PLL input signal [148].

Now, defined in (2.19) is the reference voltage vector, $\mathbf{v}_{abc}$, which has an amplitude that is equal to V_g.

$$\mathbf{v}_{abc} = V_g e^{i\theta(S)} \tag{2.19}$$

From Figure 2.6, the output of the SRF-PLL is known to be the estimated phase angle is $\hat{\theta}$, which can be represented using

$$\hat{\theta}(s) = \frac{1}{s}\hat{\omega}(s) \tag{2.20}$$

If the estimated frequency, $\hat{\omega}$, shown in (2.20), is used as the action applied by the controller, the plant to be controlled becomes

$$H_p(s) = \frac{1}{s} \tag{2.21}$$

If the transfer function of the PI control, which is utilized in the SRF-PLL design that is shown in Figure 2.6, is given as in (2.22),

$$H_c(s) = \frac{k_p s + k_i}{s} \tag{2.22}$$

The open-loop transfer function of the system can be determined by multiplying both transfer functions, $H_p(s)$ and $H_c(s)$, which are presented in (2.21) and (2.22), and it is expressed as in (2.23).

$$H_{OL}(s) = H_c(s)H_p(s) = \frac{k_p s + k_i}{s} \cdot \frac{1}{s} \tag{2.23}$$

Taking into account the generic form of the second-order closed-loop transfer function for a system with a unity loop, which is expressed in (2.24),

$$H_{CL}(s) = \frac{H_{OL}(s)}{1 + H_{OL}(s)} \tag{2.24}$$

The normalized closed-loop transfer function, $H_{CL}(s)$, is calculated and presented in (2.25).

$$H_{CL}(s) = \frac{k_p s + k_i}{s^2 + k_p s + k_i} \tag{2.25}$$

Finally, the s-domain PI control gains, i.e., k_p and k_i, are determined by means of the generic form of the second-order transfer function, which is expressed in (2.26).

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.26}$$

where

ω_n the natural frequency;

ζ the damping factor.

If the coefficients in denominator of (2.25) are matched with those of (2.26), the PI control gains can be calculated using (2.27) and (2.28).

$$k_p = 2\zeta\omega_n \tag{2.27}$$

$$k_i = \omega_n^2 \tag{2.28}$$

2.5.2 Design of the Proportional-Integral (PI) Control Gains in Z-Domain

The continuous-time PI controller, which are described in the previous subsection, has to be converted to the discrete-time, referred to as z-domain, for proper digital implementation. In order to properly convert the system to the z-domain, the Forward Euler approximation technique, presented in (2.29), is utilized [148].

$$s \rightarrow \frac{z-1}{T_s} \tag{2.29}$$

Now, let the estimated phase angle, $\hat{\theta}$, which is expressed in (2.20), be discretized using (2.29) and expressed as in (2.30).

$$\hat{\theta}(z) = \frac{T_s}{z-1}\hat{\omega}(z) \tag{2.30}$$

Considering $\hat{\omega}(z)$ and T_s to be the control action, which is the estimated frequency, and the controller sampling time, respectively, this yields to have the plant in the z-domain to be

$$H_p(z) = \frac{T_s}{z-1} \tag{2.31}$$

The PI controller transfer function presented in (2.22), can also be determined in z-domain by applying the Forward Euler approximation as follows

$$H_c(z) = \frac{k_p(z-1) + k_i T_s}{z-1} \tag{2.32}$$

From (2.31) and (2.32), the open-loop transfer function of the SRF-PLL in z-domain, expressed in (2.34), can be calculated using the generic form of the open loop transfer function, which is presented in (2.33).

$$H_{OL}(z) = H_c(z) H_p(z) \tag{2.33}$$

$$H_{OL}(z) = \frac{k_p(z-1) + k_i T_s}{z-1} \cdot \frac{T_s}{z-1} \tag{2.34}$$

Similar to the s-domain closed-loop transfer function, the z-domain closed-loop transfer function, which is explained in (2.36), is calculated using the general form of a closed loop transfer function, presented in (2.35).

$$H_{CL}(z) = \frac{H_{OL}(z)}{1 + H_{OL}(z)} \tag{2.35}$$

$$H_{CL}(z) = \frac{(k_p T_s)z + (k_i T_s^2 - k_p T_s)}{z^2 - (k_p T_s - 2)z + (k_i T_s^2 - k_p T_s + 1)} \tag{2.36}$$

From (2.36), the PI control gains in discrete time can be solved as

$$k_p = \frac{-2e^{-\zeta \omega_n T_s} \cos(\omega_n T_s \sqrt{1-\zeta^2}) + 2}{T_s} \tag{2.37}$$

$$k_i = \frac{e^{-2\zeta \omega_n T_s} + k_p T_s - 1}{T_s^2} \tag{2.38}$$

2.6 Concluding Remarks

This chapter starts by describing the reasons, which make the 3-L VSC topologies more popular for medium- to high- voltage MG applications. Then, the structural design for the commonly used three-phase 3-L VSCs, which are the 3-L NPC and the 3-L T-type power converters, was described in detail. A brief comparison between the NPC and T-type VSC topologies was also mentioned. Then, the model design of these 3-L VSCs has been explained and presented in Figure 2.3 and Table 2.2. Since the 3-L VSCs have two dc-link capacitors, a continuous-time design for these dc-link capacitors followed by a discrete-time design have been derived in this chapter. After describing the design of the 3-L VSC topology and the dc-link capacitors, different kinds of converters output ac filters are explained with focus on the two common and most effective filters, which are the *LC* and the *LCL* filters. Similar to the dc-link capacitor design, the continuous-time designs for the *LC* and the *LCL* filters have been explained. Then, these continuous-time systems have been discretized with a fixed sampling time. Finally, since the phase synchronization is significant for grid-tied VSCs, the basic operation of a generic PLL has been firstly demonstrated. After that, the design of the SRF-PLL has been shown in the s-domain before it was discretized and presented in the z-domain such that it can be properly implemented in the digital controllers.

CHAPTER 3

AN ENHANCED MPC USING VIRTUAL SPACE VECTORS FOR GRID CONNECTED 3-L NPC CONVERTERS

3.1 Introduction

Compared to controllers, which have modulators with a fixed switching frequency such as PWM techniques, finite-control-set model predictive control (FCS-MPC) is a variable switching frequency control scheme. Thus, in microgrid (MG) applications, where voltage source converters (VSCs) have to be interfaced with the electric grid through well-designed passive filters, the variable average switching frequency could contribute in substantially increased output waveform ripples due to the fact that the passive filters are often design to target harmonics contents at specific frequencies [149]. Additionally, despite the fact that MPC is a multi-objectives control strategy, which can include more than one target in a single quality function, designing a classical MPC approach for a topology, similar to the three-phase three-level (3-L) neutral-point clamped (NPC) VSCs, requires careful consideration and proper selection to the weighting factors of the multiple objectives [123]. To further explain, the different objectives in the cost function of the MPC method have to be weighted carefully against each other to have a compromised controller performance. Considerable amount of time and effort, therefore, are needed to select the different optimal weighting factors. Hence, this iterative process not only increases the controller complexity design, but also reduces the MPC performance since one weighting factor cannot be optimal for multiple VSC operation conditions [150].

As a result, an enhanced MPC using virtual space vectors (VSVs) method has been proposed in this chapter to address some of the challenges related to the implementation of the classical MPC technique on the 3-L NPC VSCs [151], [152]. In the presented MPC method, a set of six

VSVs have been created and added to the controller deign. In spite to the fact that including the six VSVs into the classical MPC design increases the number of evaluations for the cost function from 27 to 33 times, which ultimately results in having higher digital controller execution time, major contributions have been verified when adopting the proposed MPC strategy. These contributions are listed as follows

- Enhanced VSC output waveform quality;
- Reduced neutral-point voltage (NP-V) fluctuations;
- Simplified weighting factor design;
- Reduced ac filter size.

The notional MG, which is investigated in this work and displayed in Figure 3.1, consists of a utility-scale photovoltaic (PV) inverter, an energy storage system (ESS) inverter and a local unknown critical load, which is connected to the point of common coupling (PCC). A circuit breaker (CB) is used to connect and disconnect the MG to/from the main electric grid. The 3-L NPC VSC, which has the power circuit shown in Figure 2.1 of Chapter 2, has been selected to interface the solar panels and the ESS with the ac mains.

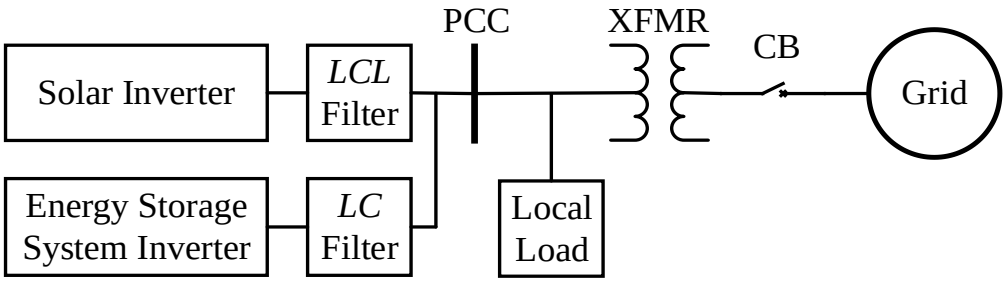


Figure 3.1: One-line diagram of the MG systems studied in this chapter.

This chapter firstly reviews the various operating modes of the three-phase 3-L NPC VSCs in the MG, which are mainly categorized as grid-feeding and grid-forming operating modes, when

the conventional model predictive current control (MPCC) and model predictive voltage control (MPVC) methods are used. Further, a detailed explanation for the proposed MPCC/MPVC strategies and the gating signal generation method have been included. Moreover, increasing voltage vectors application within the same control period, gives rise to a corresponding increase in the average switching frequency. Hence, a converter switching and conduction power loss model have been included in this chapter. The developed converter loss model is used to compare and analyze the switching and conduction losses of the power switch devices considering both typical and proposed MPC techniques. Then, various simulation studies have been shown to demonstrate the performance of the classical and enhanced MPC strategies. A controller hardware-in-the-loop (C-HIL) test setup, which is used in this work, has also been explained. Furthermore, the C-HIL studies have been displayed and discussed in this chapter. Finally, this chapter is concluded with some concluding remarks which summarize the work proposed in this chapter and the findings.

3.2 Conventional MPC Strategies for 3-L NPC VSCs

The control algorithms of the conventional MPCC and MPVC methods are shown in Figures 3.2(a) and 3.2(b), respectively. The detailed control block diagram of these typical MPC approaches, which are applied to the grid-connected and islanded MG systems, is also provided in Figure 3.3. To ensure fast-dynamic response against variations in solar generation and loads, both VSCs, i.e., the solar inverter and the ESS inverter, in the MG system under investigation, are controlled using the conventional MPCC/MPVC methods although the objectives of the designed MPC strategies are different. To be more specific, the output current of the grid-connected PV VSC is controlled to ensure maximum power delivery to the load, which means the PV VSC is controlled as a grid-feeding VSC, whose reference current signal is produced using the maximum

power point tracking (MPPT) technique. On the contrary, the ESS VSC is controlled in the grid-forming operating mode, which not only establishes the electric grid voltage and frequency in the MG islanded mode, but also provides power support to the PCC if needed. A comprehensive description for both VSC control schemes is provided next in order to draw a full picture for the control techniques [152], [153].

3.2.1 Control of the Grid-Following VSC

As illustrated in Figure 3.3, the MPCC strategy is designed to control the grid-tied solar inverter output current. In order to achieve that, multiple feedback signals have to be measured instantaneously. Therefore, the feedback signals, the solar inverter-side current, i_{c1}, grid-side current, i_{g1}, voltage across the *LCL*-filter capacitor, v_{Cf1}, and the dc-link capacitor voltages, v_{C11} and v_{C12}, are measured at sampling instant k. Then, v_{C11}, v_{C12} and i_{c1} can be predicted at the sampling instant $k + 1$ by using (2.6), (2.7) and (2.11), which were derived and presented in Chapter 2. Finally, an optimal voltage vector, which minimizes the cost function that is designed for the MPCC method, i.e., g_1 expressed in (3.1), can be determined. In the conventional MPC strategies, to ensure well-regulated NP-V oscillations, a specified term evaluating the difference between the voltages across the two dc-link capacitors is required. The term's weighting factor, i.e., λ_{dc1} shown in (3.1), needs to be carefully selected to trade the NP-V fluctuations performance against the main goal of MPCC, which is the VSC-side current [122]. In addition, it is worth noting that, since the controller sampling time, T_s, of the reference current is particularly small compared to the fundamental period of the supplied current, it can be assumed that the value of $i_{\alpha\beta}^{*}$ remains the same over one sampling period, which is T_s presented in Table 3.3, which means that there is no

need for extrapolation of the reference current signal. Finally, the MPCC control algorithm is presented in Figure 3.2(a) [123].

$$g_1 = (i_\alpha^* - i_{c1,\alpha}^p)^2 + (i_\beta^* - i_{c1,\beta}^p)^2 + \lambda_{dc1}(v_{C11}^p - v_{C12}^p) \tag{3.1}$$

where

i_α^* and i_β^*	real and imaginary parts of the converter reference current;
$i_{c1,\alpha}^p$ and $i_{c1,\beta}^p$	real and imaginary parts of the converter predicted current;
v_{C11}^P and v_{C12}^P	predicted dc-link capacitor voltages of the solar inverter;
λ_{dc1}	weighting factor for the dc-link voltages balancing term.

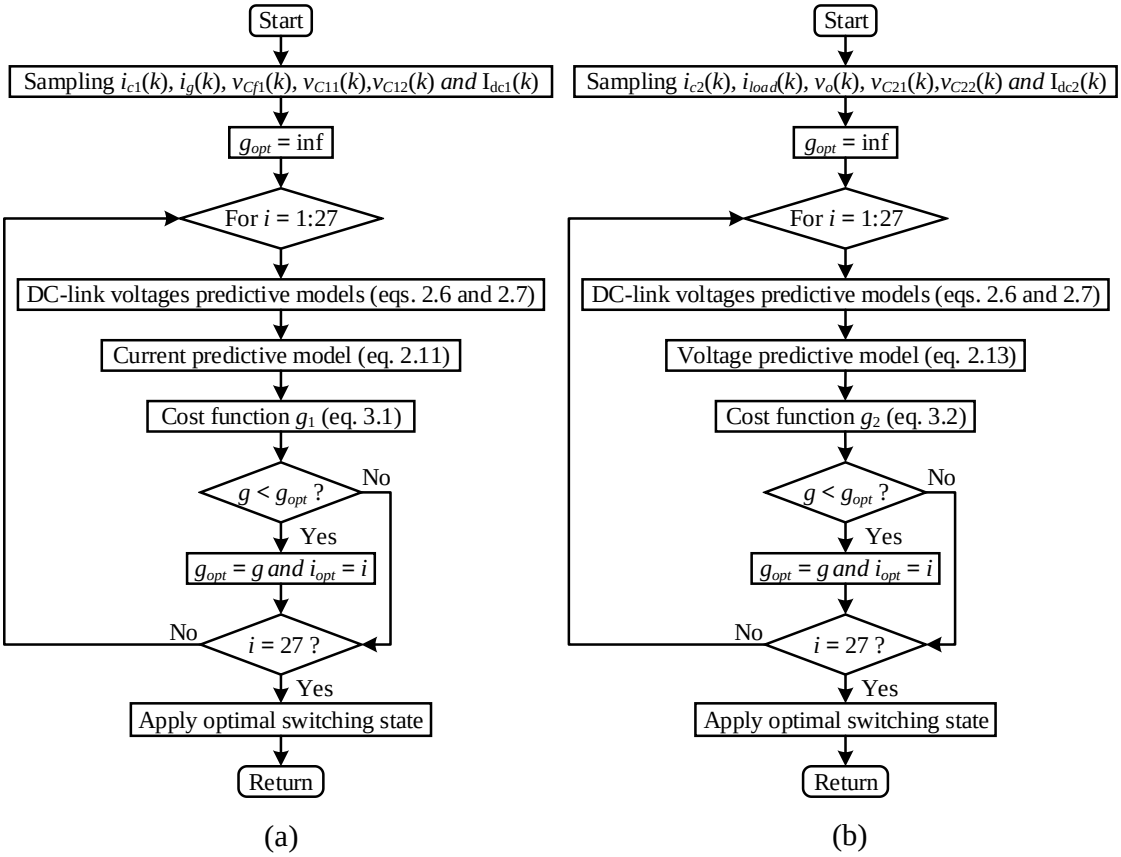


Figure 3.2: Control algorithms of the typical MPC methods (a) MPCC and (b) MPVC.

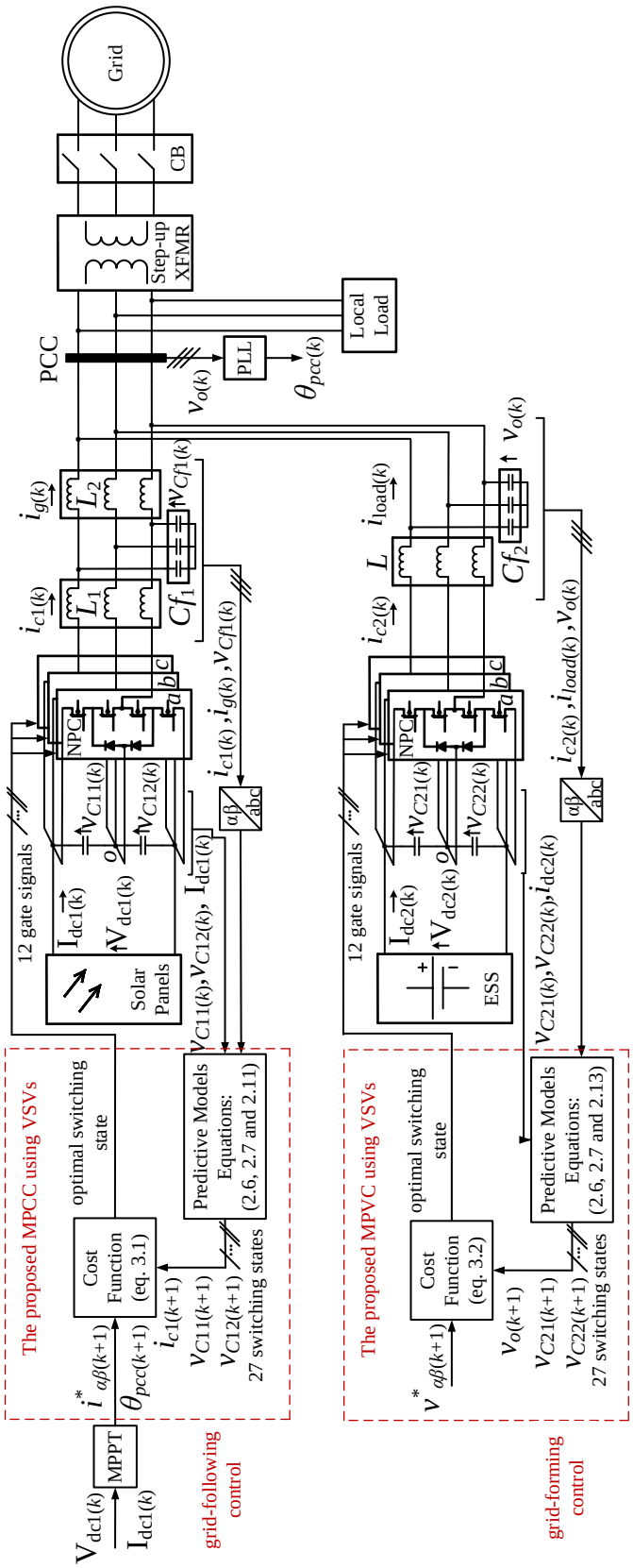


Figure 3.3: Control block diagram of typical MPC methods for the MG systems.

3.2.2 Control of the Grid-Forming VSC

In regard to the grid-forming ESS inverter, the MPVC scheme, whose flow chart algorithm is shown in Figure 3.2(b), is developed with the complete control block diagram presented also in Figure 3.3. As demonstrated in Figure 3.3, the VSC-side current, i_{c2}, the *LC*-filter capacitor voltage, v_o, the grid-side current, i_{g2}, and the dc-link capacitor voltages, v_{C21} and v_{C22}, are measured at sampling instant *k*. Using (2.6), (2.7) and (2.13), which were derived in Chapter 2, the v_{C11} and v_{C12} as well as the load voltage, v_o, at sampling instant $k + 1$ can be predicted. The cost function g_2, which is expressed in (3.2), is designed to achieve the two control objectives, i.e., the load voltage and the dc-link capacitor voltages balancing. The weighting factor, λ_{dc2}, is used in the term related to the dc-link capacitor voltages balancing [140].

$$g_2 = (v_\alpha^* - v_{o,\alpha}^p)^2 + (v_\beta^* - v_{o,\beta}^p)^2 + \lambda_{dc2}(v_{C21}^p - v_{C22}^p) \tag{3.2}$$

where

v_α^* and v_β^*	real and imaginary parts of the load reference voltage;
$v_{o,\alpha}^p$ and $v_{o,\beta}^p$	real and imaginary parts of the load predicted voltage;
v_{C21}^P and v_{C22}^P	predicted dc-link capacitor voltages of the ESS inverter;
λ_{dc2}	weighting factor for the dc-link voltages balancing term.

3.3 Proposed MPC Strategies for 3-L NPC VSCs

Shown in Figure 2.1, which was presented in Chapter 2, is the schematic of the three-phase 3-L NPC VSC. Over a sampling period, T_s, if the average value of the neutral-point current (NP-C), which is i_o in the middle wire of the dc-link capacitors shown in Figure 2.1 of Chapter 2, is non-zero, the NP-V oscillations will occur in the 3-L NPC VSC [154]. Therefore, in both cost functions

presented in this chapter, i.e., (3.1) and (3.2), a dedicated term is included to mitigate the NP-V fluctuations. The specified terms' weighting factors, i.e., λ_{dc1} and λ_{dc2}, are critical to the performance of the MPCC and MPVC methods since it is usually complicated to trade the dc-link capacitor voltages balancing against the main goal of the MPCC and MPVC schemes, i.e., either current or voltage reference tracking. The overall control block diagram of the notional MG with the proposed control schemes is presented in Figure 3.4.

In order to provide a complete description for the proposed MPC strategies, in this section of this chapter, the concept of the VSVs is explained first. The gating signals implementation is then demonstrated; followed by a space vector (SV) diagram comparison of the typical and proposed MPC techniques.

3.3.1 VSVs and Extended Switching States Synthetization

As an alternative to the typical MPC method, the concept of the VSVs, which was firstly introduced in [155] and implemented for the space vector pulse-width modulation (SV-PWM), has been adopted in this work. The VSVs are defined as a set of space vectors synthesized by using the three-nearest original voltage space vectors, e.g., the $\mathbf{V}_{\mathrm{x}}$, $\mathbf{V}_{\mathrm{y}}$, and $\mathbf{V}_{\mathrm{z}}$ shown in Table 3.1, however, the resulting i_o is zero over one sampling period, T_s, when any of the VSV is applied. Following this concept, in this chapter, six VSVs, which are $\mathbf{V}_{\mathrm{V1}}$ to $\mathbf{V}_{\mathrm{V6}}$ shown in Figure 3.5, are added to the 3-L NPC VSC finite control set (FCS) such that the number of possible switching states is increased from 27 to 33, when compared with the conventional MPC method. Using the VSV $\mathbf{V}_{\mathrm{V1}}$ as an example, the $\mathbf{V}_{\mathrm{V1}}$ is synthesized as

$$\mathbf{V}_{\mathrm{V1}} = \frac{(\mathbf{V}_{\mathrm{S1}}[i_a] + \mathbf{V}_{\mathrm{S2}}[i_c] + \mathbf{V}_{\mathrm{M1}}[i_b])}{3} \tag{3.3}$$

In this work, to generate gate signals in a convenient way, the concept of the extended switching state of an original voltage space vector $\mathbf{V}_m$ (m = 1, 2, … , 19) is defined using the form of

$$S^* = \begin{pmatrix} S_{a1} & S_{a2} & S_{b1} & S_{b2} & S_{c1} & S_{c2} \end{pmatrix} \tag{3.4}$$

The generic form, expressed in 3.4, contains the switching states of both top devices in each phase leg as shown in 3-L NPC VSC schematic, which was presented in Chapter 2. Now, the generic model of the extended switching states can be applied for all the VSVs. For instance, the extended switching state for the $\mathbf{V}_{V1}$ can be easily determined as

$$\begin{aligned} S^*(\mathbf{V}_{V1}) &= \frac{S^*(\mathbf{V}_{S1}[i_a])}{3} + \frac{S^*(\mathbf{V}_{S2}[i_c])}{3} + \frac{S^*(\mathbf{V}_{M1}[i_b])}{3} \\ &= \begin{pmatrix} \frac{0+1+1}{3} & \frac{1+1+1}{3} & \frac{0+0+1}{3} & \frac{0+1+1}{3} & \frac{0+0+0}{3} & \frac{0+0+1}{3} \end{pmatrix} \\ &= \begin{pmatrix} \frac{2}{3} & 1 & \frac{1}{3} & \frac{2}{3} & 0 & \frac{1}{3} \end{pmatrix} \end{aligned} \tag{3.5}$$

When a VSV is selected as the optimal voltage vector to be applied in the next control iteration, it will generate zero average NP-C, i.e. $I_o = 0$, over a switching cycle, such that NP-V is not influenced. Therefore, when the six VSVs are added into the SV diagram, the NP-V fluctuations can be mitigated due to the fact that these voltage space vectors do not contribute in arbitrary charging and/or discharging for the dc-link capacitors. Additionally, the total harmonic distortion (THD) of the 3-L NPC VSC output waveforms is noticeably reduced as the NP-V oscillations are mitigated and the average switching frequency is increased. The reference signals tracking is also improved since more voltage space vectors are included in the SV diagram, which reduces the tracking error. Finally, since the use of the VSVs noticeably increases the average switching frequency of the power switches, the size and weight of the passive ac filters, which are the *LC* and *LCL* filters, can be significantly minimized, which improves the systems overall efficiency.

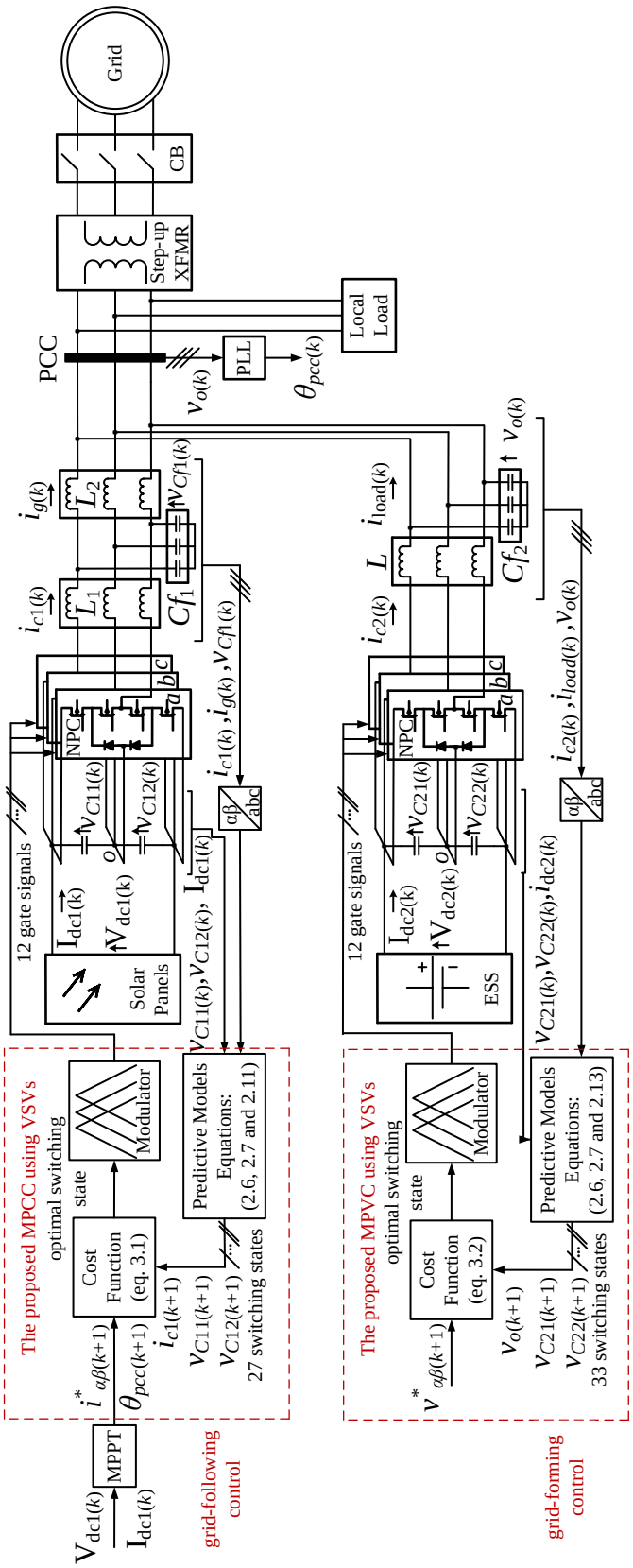


Figure 3.4: Control block diagram of proposed MPC methods for different MG systems.

Table 3.1
Summary for the Additional Six VSVs and Their Extended Switching States

VSV	$\mathbf{V_x}$	$S(\mathbf{V_x})$	$\mathbf{V_y}$	$S(\mathbf{V_y})$	$\mathbf{V_z}$	$S(\mathbf{V_z})$	*Extended Switching States*					
							S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}
$\mathbf{V}_{V1}$	$\mathbf{V}_{S1}[i_a]$	(0,–,–)	$\mathbf{V}_{S2}[i_c]$	(+,+,0)	$\mathbf{V}_{M1}[i_b]$	(+,0,–)	2/3	1	1/3	2/3	0	1/3
$\mathbf{V}_{V2}$	$\mathbf{V}_{S2}[i_c]$	(+,+,0)	$\mathbf{V}_{S3}[i_b]$	(–,0,–)	$\mathbf{V}_{M2}[i_a]$	(0,+,–)	1/3	2/3	2/3	1	0	1/3
$\mathbf{V}_{V3}$	$\mathbf{V}_{S3}[i_b]$	(–,0,–)	$\mathbf{V}_{S4}[i_a]$	(0,+,+)	$\mathbf{V}_{M3}[i_c]$	(–,+,0)	0	1/3	2/3	1	1/3	2/3
$\mathbf{V}_{V4}$	$\mathbf{V}_{S4}[i_a]$	(0,+,+)	$\mathbf{V}_{S5}[i_c]$	(–,–,0)	$\mathbf{V}_{M4}[i_b]$	(–,0,+)	0	1/3	1/3	2/3	2/3	1
$\mathbf{V}_{V5}$	$\mathbf{V}_{S5}[i_c]$	(–,–,0)	$\mathbf{V}_{S6}[i_b]$	(+,0,+)	$\mathbf{V}_{M5}[i_a]$	(0,–,+)	1/3	2/3	0	1/3	2/3	1
$\mathbf{V}_{V6}$	$\mathbf{V}_{S6}[i_b]$	(+,0,+)	$\mathbf{V}_{S1}[i_a]$	(0,–,–)	$\mathbf{V}_{M6}[i_c]$	(+,–,0)	2/3	1	0	1/3	1/3	2/3

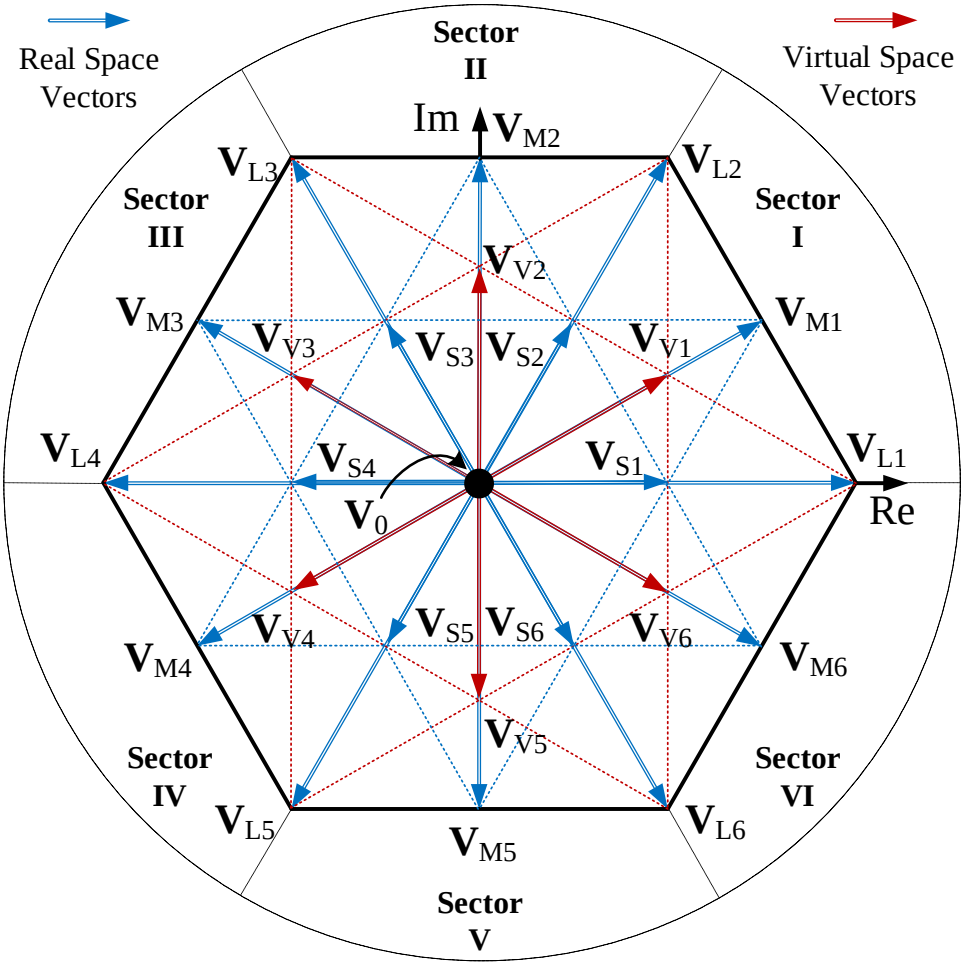


Figure 3.5: SV diagram of a three-phase 3-L NPC VSC with the six VSVs.

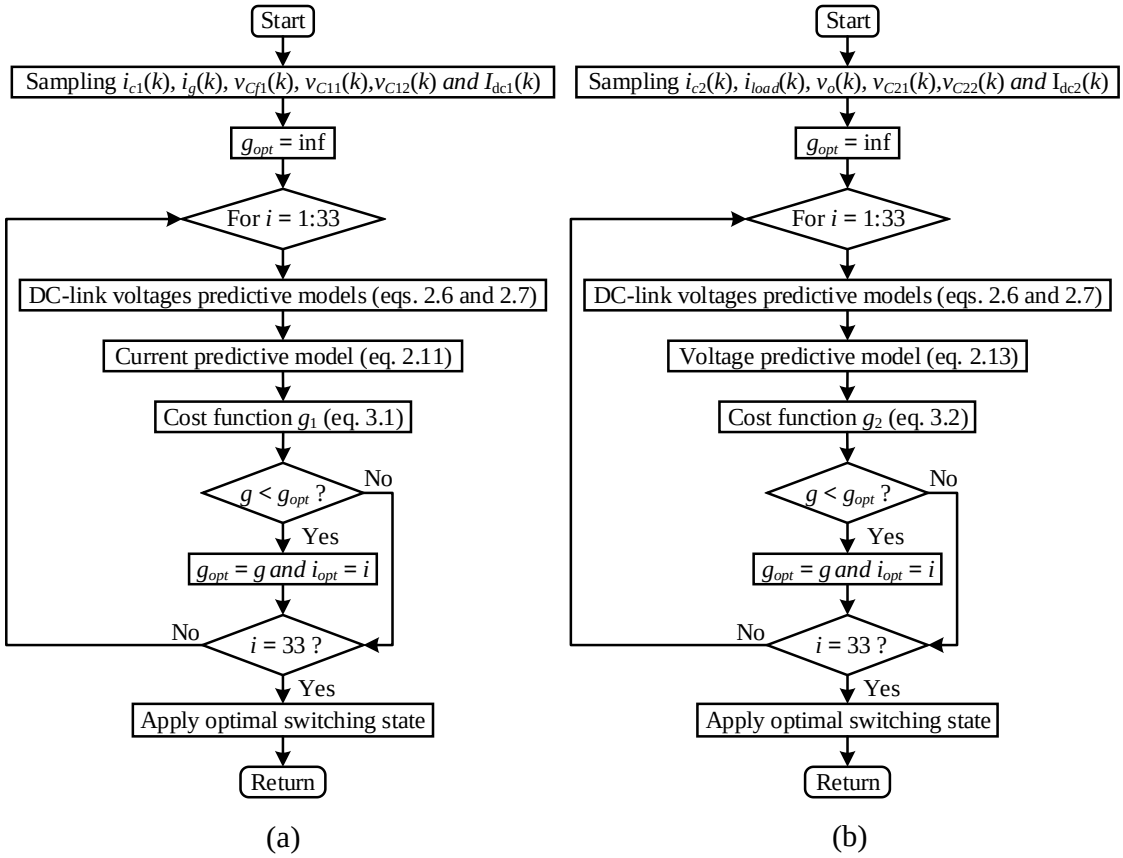


Figure 3.6: Control algorithms of the proposed MPC methods (a) MPCC and (b) MPVC.

Since the number of the voltage space vectors to be evaluated in the cost function has been increased from 27 to 33 voltage space vectors, the controller execution time, i.e. T_{MPC}, is expected to be increased due to the higher number of the controller algorithm calculations relative to that of the traditional MPC algorithm. Therefore, the flow chart algorithms of the classical MPCC and MPVC methods, which were demonstrated in Figure 3.2, have to be updated to include the VSVs. Hence, the new control algorithms of the proposed MPCC and MPVC are shown in Figures 3.6(a) and 3.6(b), respectively.

3.3.2 Gate Signals Implementation

All the extended switching states of the six VSVs are summarized in Table 3.1. Using the extended switching states, all VSVs and the real voltage space vectors can be translated to the gate signals using an external modulator as presented in Figure 3.4. This modulator compares the extended switching state of the optimal voltage vector selected by the MPC algorithm with a carrier waveform which has a fixed switching frequency. An example to generate gate signals for $\mathbf{V}_{V1}$ is shown in Figure 3.7.

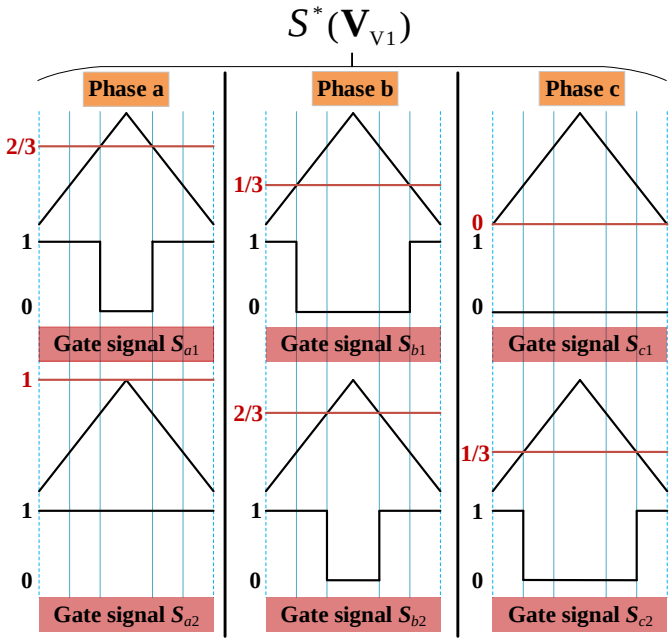


Figure 3.7: An illustration of gate signal generation for $\mathbf{V}_{V1}$.

3.3.3 SV Diagram Comparison of Different MPC Strategies

To further clarify the proposed VSVs' concept, the presented SV diagram of the proposed MPC method has been compared with the original space vector diagram and presented in Figure 3.8. The original voltage space vectors, which generate zero i_o are depicted in black circles while the blue crosses represent original voltage space vectors with non-zero i_o. The additional virtual

space vectors are shown in the red circles. The impact of every voltage space vector on the converter NP-C, i_o, is summarized in Table 3.2.

Table 3.2
Impact of Different Voltage Space Vectors on the VSC NP-C

Impact of Voltage Space Vectors on NP-C	Typical MPC	Enhanced MPC
Non-zero NP-C ($I_o \neq 0$)	$\mathbf{V}_{S1} \sim \mathbf{V}_{S6}$ $\mathbf{V}_{M1} \sim \mathbf{V}_{M6}$	$\mathbf{V}_{S1} \sim \mathbf{V}_{S6}$ $\mathbf{V}_{M1} \sim \mathbf{V}_{M6}$
Zero NP-C ($I_o = 0$)	$\mathbf{V}_0$ $\mathbf{V}_{L1} \sim \mathbf{V}_{L6}$	$\mathbf{V}_0$ $\mathbf{V}_{L1} \sim \mathbf{V}_{L6}$ $\mathbf{V}_{V1} \sim \mathbf{V}_{V6}$

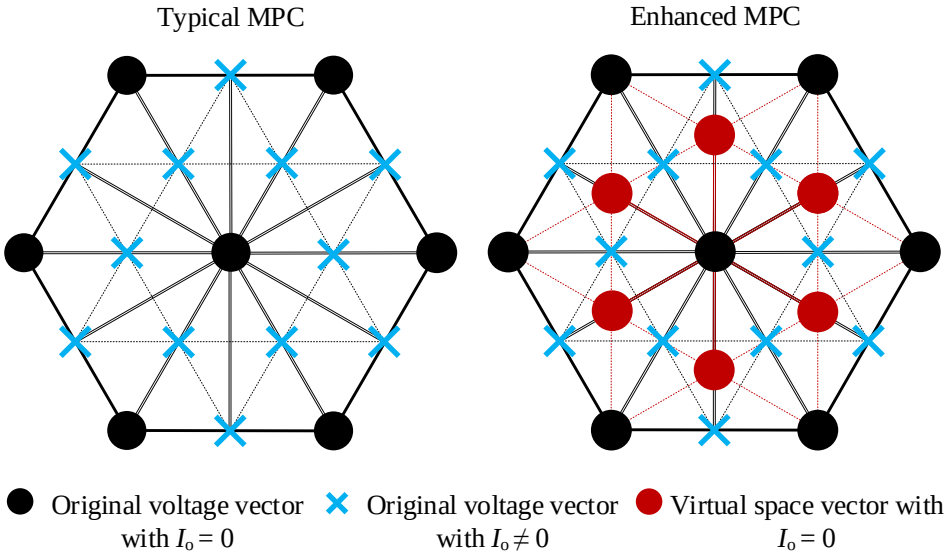


Figure 3.8: An illustration of the impact of different voltage space vectors on the VSC NP-C.

3.4 Power Loss Analysis

In this chapter, the loss analysis for 3-L NPC VSCs was performed to address the trade-off among the 3-L NPC VSC switching and conduction losses, the NP-V fluctuations and the 3-L

NPC VSC output waveforms quality. A generic structural block diagram model [156] of a single power semiconductor device switching and conduction power losses, i.e., P_{sw} and P_{cond}, is demonstrated in Figure 3.9. Using this power loss model, P_{sw} and P_{cond} are calculated separately before they are added together so that a total loss for a discrete power semiconductor device is determined.

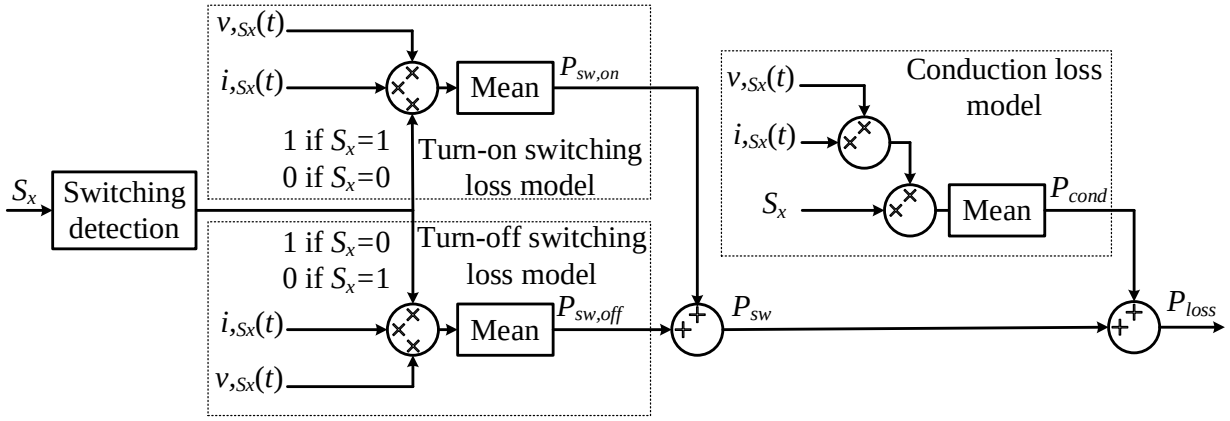


Figure 3.9: Power loss model of a discrete power semiconductor device, S_x.

3.4.1 Switching Power Loss Model

As shown in Figure 3.9, the switching loss model is divided into two different parts, which are the turn-on and turn-off switching loss models. Taking the gating signal of phase leg *a* top switch, i.e., S_{a1}, as an example, a switching detection method is used to detect the rising and falling edges of S_{a1}. On the one hand, if S_{a1} rising edge is determined to be 1, i.e., S_{a1} turns on, the turn-on switching loss, $P_{sw,on[Sa1]}$, of S_{a1} is calculated by multiplying the instantaneous voltage and current of S_{a1}, i.e., $v_{Sa1}(t)$ and $i_{Sa1}(t)$, respectively. The result of this multiplication is, then, averaged over a fundamental switching period, i.e., T_s. On the other hand, when the falling edge is detected, which means S_{a1} turns off, the turn-off switching loss, $P_{sw,off[Sa1]}$, of S_{a1} can be determined by multiplying $v_{Sa1}(t)$ and $i_{Sa1}(t)$ of S_{a1}. After that, the result of this multiplication is averaged in a

similar way when $P_{sw,on[Sa1]}$ was calculated. The addition of $P_{sw,on[Sa1]}$ and $P_{sw,off[Sa1]}$, which can be represented by $P_{sw[Sa1]}$, is the overall switching loss of S_{a1}.

3.4.2 Conduction Power Loss Model

The conduction power loss, $P_{cond[Sa1]}$, of phase leg *a* top power switch device, i.e., S_{a1}, is simply determined by firstly calculating the instantaneous power, which is the result of multiplying the instantaneous voltage and current of S_{a1}, i.e., $v_{Sa1}(t)$ and $i_{Sa1}(t)$. Then, the calculated instantaneous power is multiplied by the switch device status, which can be either 0 or 1. The result of these multiplications can then be averaged over a fundamental switching period, T_s, to form the conduction power loss of the single power semiconductor device, i.e., S_{a1}.

3.4.3 Three-Phase Power Loss Model

Now, the total switching and conduction power losses of the discrete power semiconductor device S_{a1}, i.e., $P_{loss[Sa1]}$, is calculated by adding $P_{sw[Sa1]}$ to $P_{cond[Sa1]}$ as presented in Figure 3.9. As previously described in Chapter 2, the phase leg *a* bottom switching devices, i.e., S_{a3} and S_{a4}, are always operating in a complementary mode for the phase leg *a* top switching devices, i.e., S_{a1} and S_{a2}. Therefore, only the total switching and conduction power losses for S_{a1} and S_{a2} are calculated and analyzed. The other two complementary switching devices should have similar total power losses to that of the S_{a1} and S_{a2}. Thus, the total switching and conduction power losses of phase leg *a* can be determined as

$$P_{loss,a} = 2(P_{loss[S_{a1}]} + P_{loss[S_{a2}]}) \tag{3.6}$$

Assuming the power VSC, on which the individual switching and conduction losses are analyzed, is feeding a balanced three-phase load, the total three-phase switching and conduction

power losses of the three-phase 3-L NPC VSC without considering the clamping diodes losses is calculated as

$$P_{loss} = 3P_{loss,a} \tag{3.7}$$

3.5 Simulation Studies

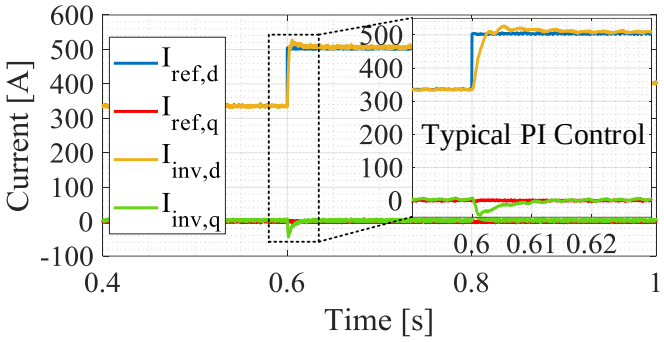
Simulation studies have been performed to validate the effectiveness of the proposed MPCC and MPVC using the VSVs and the corresponding performance of the MG system. The system parameters, which are presented in Table 3.3, have been utilized in the simulation model. The ESS inverter is assumed to work as an uninterruptable power supply (UPS), which has the capability to provide more power than the PV inverter since the latter has intermittent generated power.

Table 3.3
Investigated System Parameters

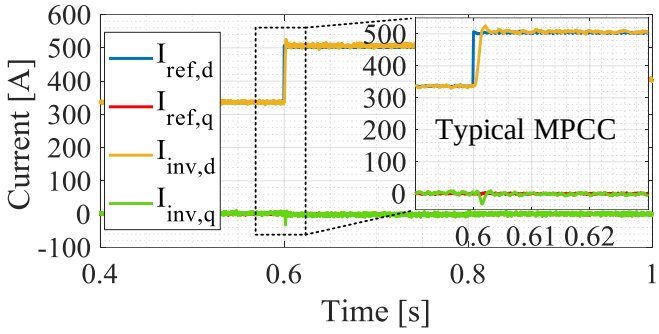
Parameters	Values	Parameters	Values
Solar Inverter		ESS Inverter	
rated active power	200 kW	rated active power	300 kW
dc-link voltage	480 V	dc-link voltage	480 V
L_1, L_2	200, 67 μH	L	500 μH
C_{f1}	200 μF	C_{f2}	480 μF
MPC		PI Controller	
sampling time T_s	50 μs	K_p, K_i	0.006, 0.8
		f_{sw}	2 kHz

- ***Dynamic Response Analysis of MPC and PI Control During Reference-Step Change***

Figure 3.10 shows a comparison between the current step response of the typical MPCC at an average switching frequency of 2 kHz, and a traditional PI controller using 2 kHz fixed switching frequency. The PI controller gains, shown in Table 3.3, are carefully tuned to achieve similar overshoot with that of the typical MPCC method and fast-raising time without oscillations.



(a)



(b)

Figure 3.10: Current dynamic response using the typical (a) PI controller and (b) MPCC.

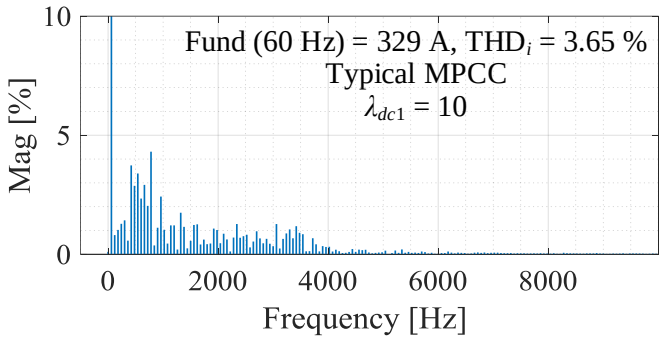
At t = 0.60 s, when the reference current signal of the PV inverter has changed, the MPCC method shows faster dynamic response relative to the classical PI controller. To explain, when applying the PI controller, it can be seen from Figure 3.10(a) that $I_{inv,d}$ has reached the steady-state condition at t = 0.62 s, which means the actual current, $I_{inv,d}$, using the PI controller required 0.20 s to track its reference signal $I_{ref,d}$. On the contrary, when the traditional MPCC approach is tested, as demonstrated in Figure 3.10(b), $I_{inv,d}$ could track its reference signal, $I_{ref,d}$, in less than 0.03 s, which clearly validates the fast-dynamic response of the MPCC compared to the PI control. Additionally, from Figures 3.10(a) and (b), it can be concluded that the MPCC generally has better decoupling characteristics between the active and reactive current components when compared with the PI control. To explain, the reactive quantity of the PV inverter injected current, $I_{inv,q}$, has been kept zero when testing the active component of the PV inverter injected current, $I_{inv,d}$, during the current step response test. However, as shown in Figure 3.10(a) and (b), by comparing the

response of the reactive PV inverter current, $I_{inv,q}$, one can see that the using the PI control has by far more influence on the $I_{inv,q}$ compared to the MPCC. To illustrate, when the current step test is applied using the PI control, the value of the $I_{inv,q}$ significantly dropped before it went back to zero. However, using the MPCC method has almost negligible effect on the $I_{inv,q}$ value when the current step change test was conducted.

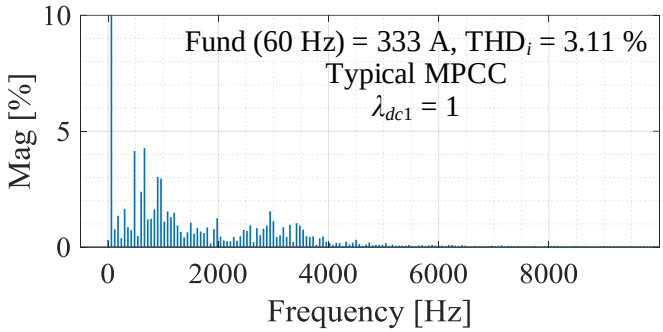
- ***Steady State Analysis of the Various MPC Strategies***

When the MG is operated in the islanded mode, the three-phase voltage and frequency at the PCC are established by the ESS inverter since the main electric grid is disconnected while the PV inverter is controlled to support the ESS inverter by supplying the maximum generated active power to the PCC, where the load and the utility grid are tied. As shown in Figures 3.11 and 3.12, the performance of the conventional and proposed MPCC methods is evaluated considering different values of the weighting factor, λ_{dc1}, which is used with the dc-link capacitor voltages balancing term.

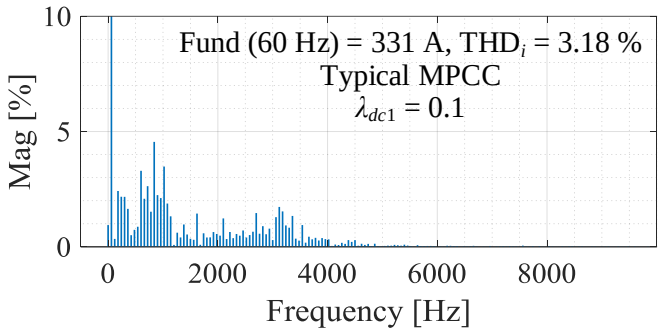
To start with, on the one hand, as displayed in Figure 3.11(a), using a large λ_{dc1}, e.g., $\lambda_{dc1} = 10$, has affected the quality of the PV VSC output current quality as high THD_i has been observed. On the other hand, having $\lambda_{dc1} = 10$ has allowed a perfectly balanced dc-link capacitor voltages as it can be seen in Figure 3.12(a). To put it differently, the THD_i of the PV output current has the value of 3.65 % while the NP-V oscillations are within only 6 V. When λ_{dc1} is reduced 10 times to the value of 1, the THD_i of the solar inverter current is improved by 0.54 % while the NP-V fluctuations have been increased by 18 V compared to the case when $\lambda_{dc1} = 10$. This happened due to the fact that both objectives, which are the PV VSC injected current and the dc-link capacitor voltages balancing, have equal importance to the controller.



(a)



(b)



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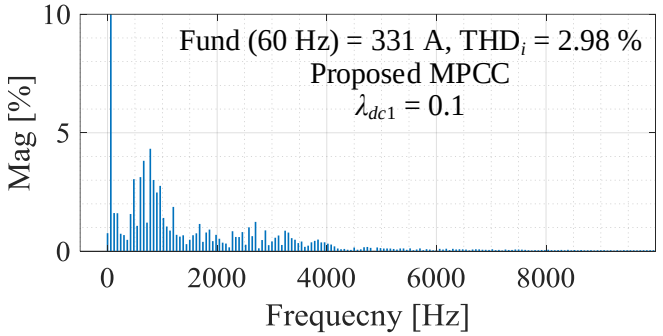


(d)

Figure 3.11: PV inverter current spectra using (a) typical MPC with λ_{dc1} = 10, (b) typical MPC with λ_{dc1} = 1, (c) typical MPC with λ_{dc1} = 0.1 and (d) proposed MPC with λ_{dc1} = 0.1.

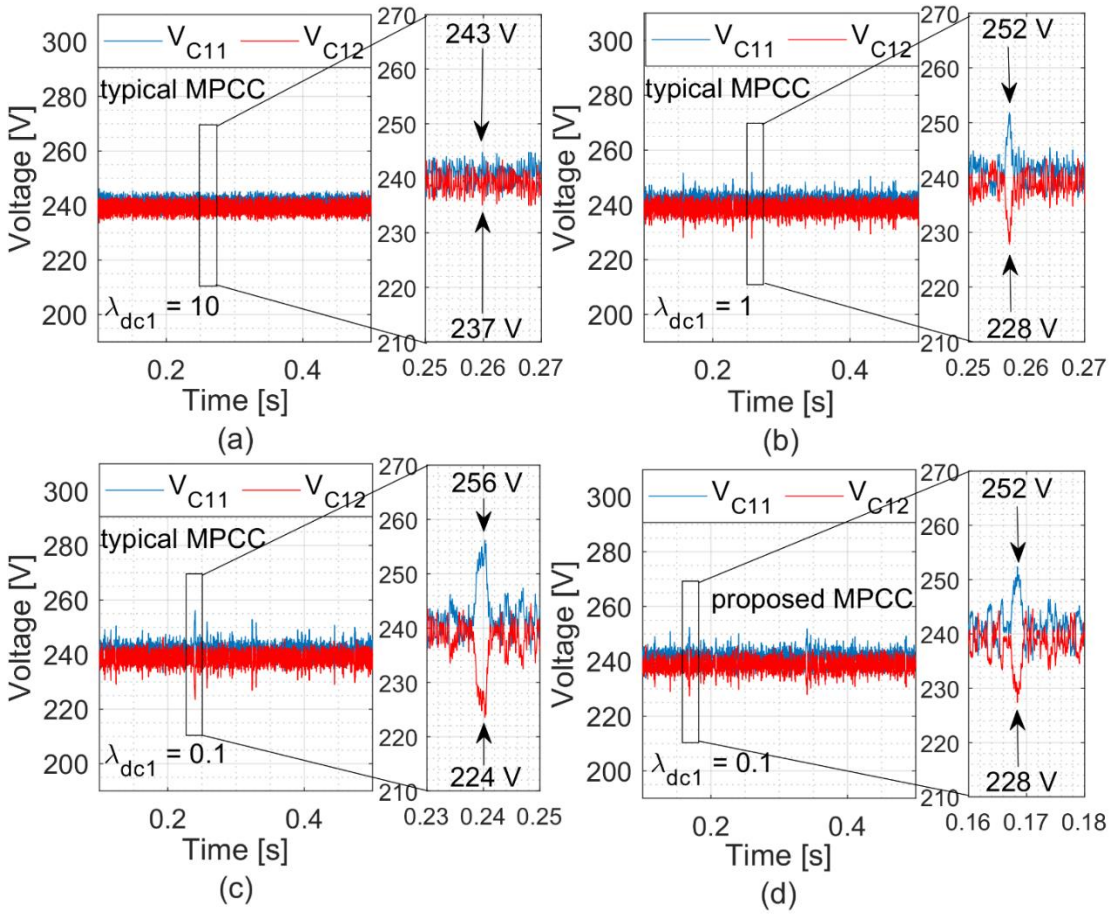


Figure 3.12: PV inverter dc-link capacitor voltages using (a) typical MPC with λ_{dc1} = 10, (b) typical MPC with λ_{dc1} = 1, (c) typical MPC with λ_{dc1} = 0.1 and (d) proposed MPC with λ_{dc1} = 0.1.

Shown in Figure 3.11(b) is the current spectrum considering λ_{dc1} = 1, while Figure 3.12(b) represents the NP-V fluctuations. The THD_i of the PV VSC output current has the value of 3.11 %, whereas the NP-V oscillations are at 24 V. Using a small λ_{dc1}, e.g., 0.1, has increased both the THD_i of the PV inverter current as well as the NP-V fluctuations as displayed in Figures 3.11(c) and 3.12(c), respectively. While the THD_i of the solar inverter current has been determined to be 3.18 %, the NP-V oscillations are at 32 V. Finally, with the proposed MPCC using VSVs being used, even though the value of λ_{dc1} = 0.1, both the THD_i of the solar inverter output current, shown in Figure 3.11(d), and the fluctuations of the dc-link voltages, shown in Figure 3.12(d), are reduced. Compared to the case when traditional MPCC is used with λ_{dc1} = 0.1, the quality of the

solar inverter output current has been improved by 0.20 %. The dc-link voltage fluctuations have also been reduced by 8 V.

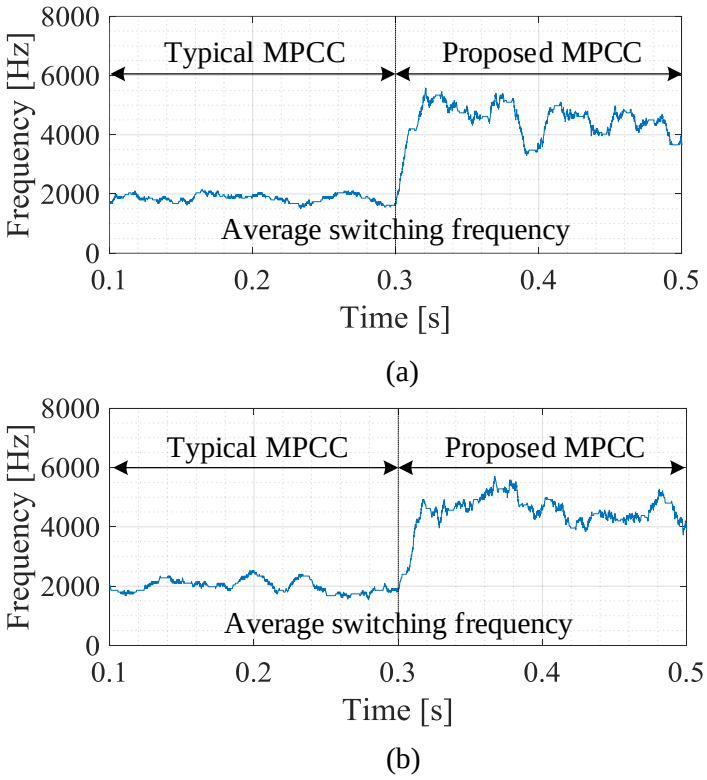


Figure 3.13: Switching frequency of phase leg *a* (a) upper switch S_{a1} and (b) upper switch S_{a2}.

- ***Power Loss Analysis of the Various MPC Strategies***

The power loss analysis is also performed for the proposed MPC methods using the model, which is developed in this chapter and presented in Figure 3.9. This power loss model considers the switching loss and the conduction loss for a discrete power semiconductor device. Then, the single-phase and three-phase power losses have been calculated to evaluate the converter overall efficiency. This analysis is based on CREE CAS325M12HM2 SiC power module. The characteristics of this power module is retrieved from the data sheet supplied by CREE [157].

Figure 3.13 shows the average switching frequencies of S_{a1} and S_{a2}, which are the upper switches of phase leg *a* from the 3-L NPC VSC topology, which is shown in Figure 2.1 of Chapter 2. As demonstrated in Figure 3.13, the average switching frequency of either of the power switching devices, S_{a1} and S_{a2}, is around 2 kHz when the traditional MPC method is applied. When the control method has been switched from the conventional MPC strategy to the proposed one, the average switching frequency of the same power semiconductor devices has increased to around 5 kHz. As a result, the switching losses of these switching devices will increase accordingly. Therefore, it is essential to study the impact of the proposed MPC on the converter overall efficiency. On the one hand, as shown in Figure 3.14, activating the VSVs at t = 0.30 s has increased the switching loss of S_{a1} and S_{a2}. While Figure 3.14(a) presents that the switching loss of S_{a1} has been raised from 7 W to approximately 17 W as a result of using the VSVs, the switching loss of S_{a2} has also been increased from 2 W to around 5 W as shown in Figure 3.14(b). This increase in the switching losses is proportionally related to the increase in the average switching frequency of these devices as explained before.

On the other hand, the conduction loss has not been affected by the observed increase in the average switching frequency as Figure 3.15 demonstrates. Shown in Figures 3.15(a) and (b) are the conduction loss of S_{a1} and S_{a2}. It can be seen that the conduction loss of, S_{a1} and S_{a2}, have remained equal to 125 W and 175 W, respectively, even though the average switching frequency of these devices has been increased from 2 kHz to around 5 kHz. Now, from Figures 3.14 and 3.15, it can be concluded that the conduction losses are by far dominated by the overall switch loss. In spite of the notable increase in the average switching frequency, the conduction loss has remained unchanged for both power switches.

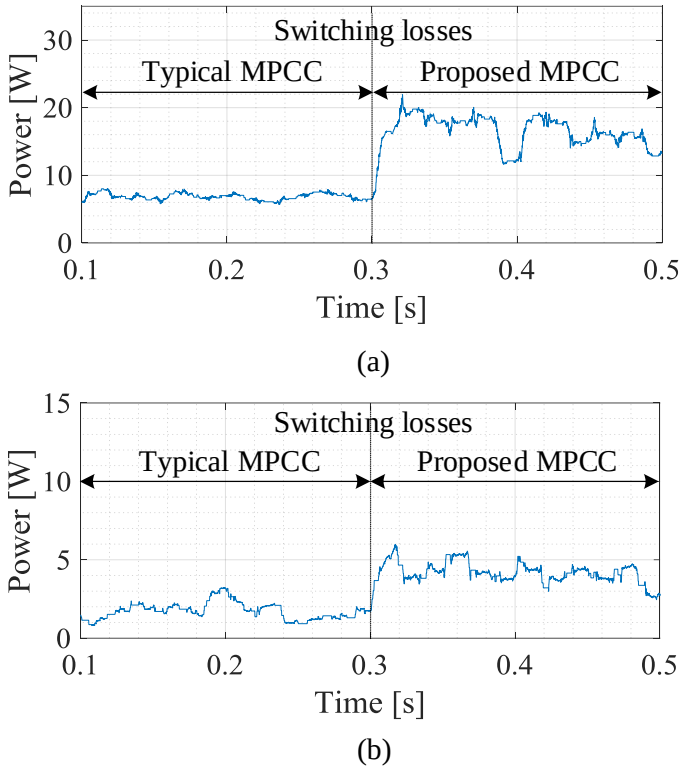


Figure 3.14: Switching loss of phase leg *a* (a) upper switch S_{a1} and (b) upper switch S_{a2}.

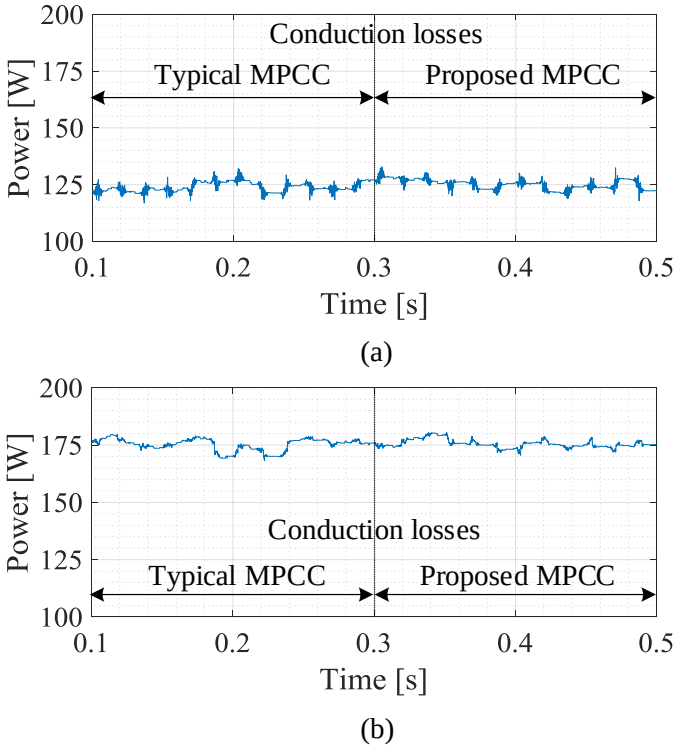


Figure 3.15: Conduction loss of phase leg *a* (a) upper switch S_{a1} and (b) upper switch S_{a2}.

Following the developed switching and conduction loss model in this chapter, the single- and three-phase switching and conduction losses are calculated using (3.6) and (3.7), respectively and summarized in Table 3.4. It is worth noting that only the conduction and switching losses were considered when the efficiency was calculated, and the power converter was assumed to operate at 100 KW rated power. Thus, for grid-connected MG applications, where the switching frequency is relatively not high, the increase of the switching frequency due to the use of VSVs should have minor impact on the 3-L NPC VSC overall efficiency. As shown in Table 3.4, the 3-L NPC VSC efficiency is only reduced by 0.045 % as a result of using the proposed MPCC strategy. Now, it has been demonstrated that, using the proposed MPC approach significantly improves the regulation of the NP-V oscillations, and high quality of the output waveforms can be achieved at the cost of slightly increased switching losses for grid connected applications.

Table 3.4
3-L NPC VSC Power Loss and Efficiency Analysis

Control Method	Three-Phase Switching Loss	Three-Phase Conduction Loss	Three-Phase Converter Loss	Converter Efficiency
Conventional MPVC	54 W	280 W	927 W	99.07 %
Proposed MPVC	132 W	324 W	972 W	99.03 %

- ***Dynamic Response Analysis of the Various MPC Strategies during Reference-Step Change***

The dynamic response of the proposed MPCC is also assessed and compared with that of the conventional MPCC to ensure adding the VSVs into the MPC control set does not affect the controller performance. A step change is applied to the solar inverter reference current, which is determined by the MPPT algorithm. Figures 3.16(a) and 3.16(b) show the solar inverter phase *a*

current, i.e., i_a^*, tracking performance of the conventional and proposed MPCC, respectively. The proposed MPCC shows particularly close dynamic tracking performance compared to the typical MPCC, which validates that the use of the additional six VSVs into the proposed MPCC design does not impact the fast-dynamic response of MPC.

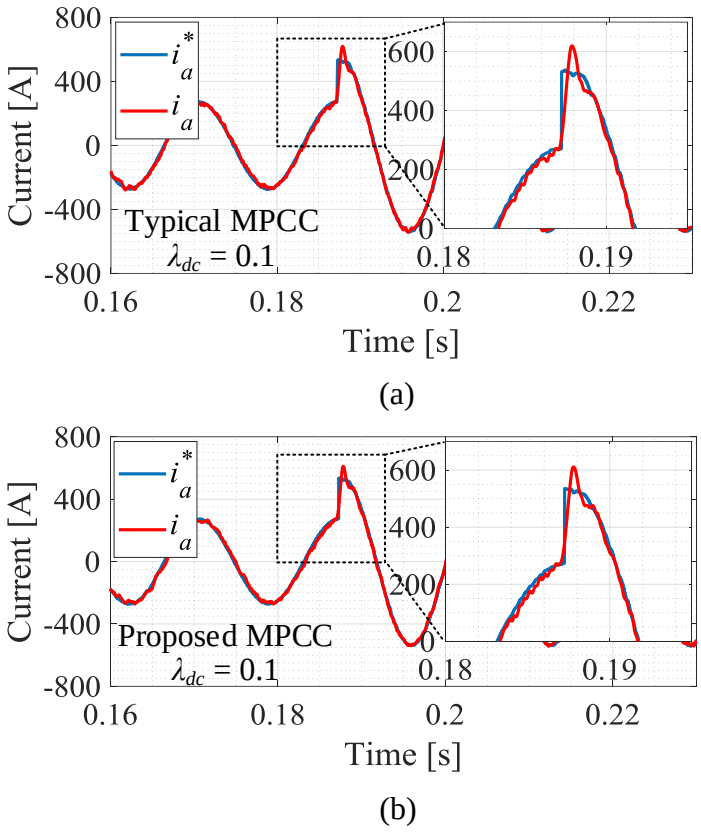


Figure 3.16: Current reference-step change using (a) typical MPCC and (b) proposed MPCC.

- ***Dynamic Response Analysis of the Proposed MPC Strategies During Load-Step Change***

The transient response of the MPCC and MPVC using VSVs methods have also been evaluated when the power generated by the solar inverter suddenly increased at t = 1.0 sec. Figure 3.17 shows the power supplied by both the ESS and the solar inverters as well as the total power consumed by the load of the PCC. Once the power generated by the grid-connected solar inverter rises from 60 kW to 180 kW, the grid-forming ESS inverter rapidly reduces its output power from 240 kW to

120 kW. However, it happens such that the three-phase output voltage and frequency at the PCC are not influenced. The three-phase voltage and frequency at the PCC, which are formed by the grid-forming ESS inverter, were not influenced when the grid-connected solar inverter doubled its generation as displayed in Figures 3.18(a) and (b).

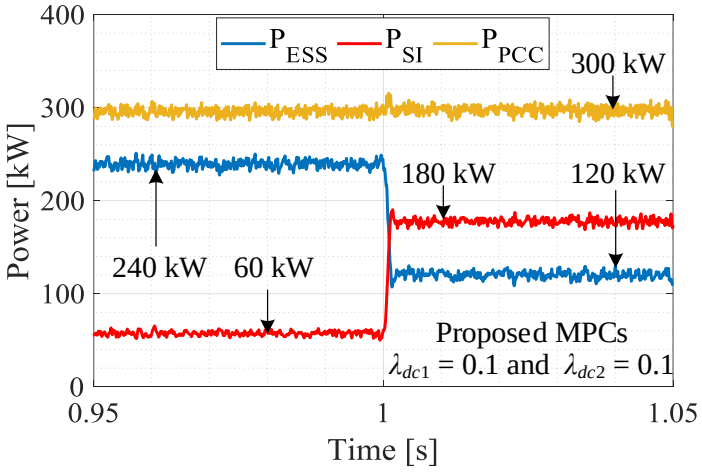


Figure 3.17: Active power generated by the ESS inverter, the solar inverter and the total power consumed by the load at PCC.

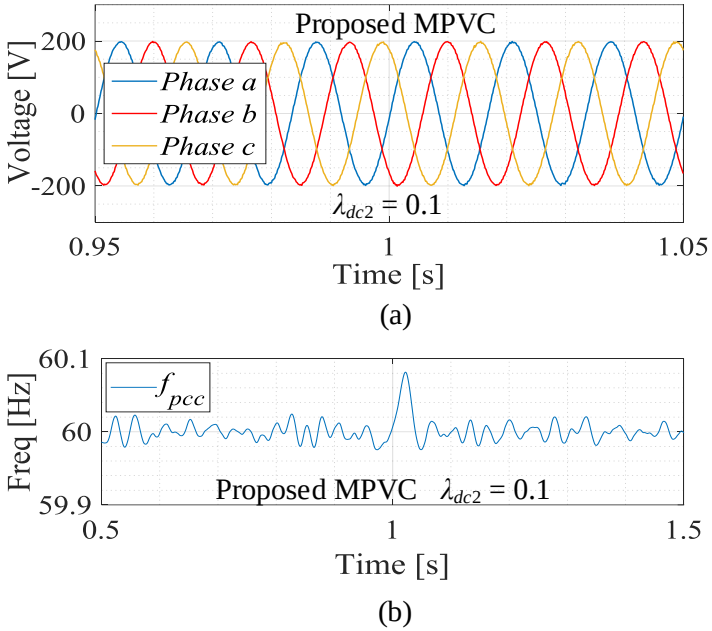


Figure 3.18: Waveforms at the PCC (a) three-phase output voltage and (b) frequency.

3.6 C-HIL Implementation for the Various MPC Strategies

In this work, in addition to the simulation studies, C-HIL studies are performed to validate the effectiveness and feasibility of the proposed MPC using VSVs. The proposed controller was implemented in a dSPACE MicroLabBox 1202 system while the notional MG system was modeled and implemented in Typhoon HIL 602+. As can be seen later in this section, the experimental results of the C-HIL test setup agree with the simulation results, which further verify the feasibility and effectiveness of the proposed MPC approaches.

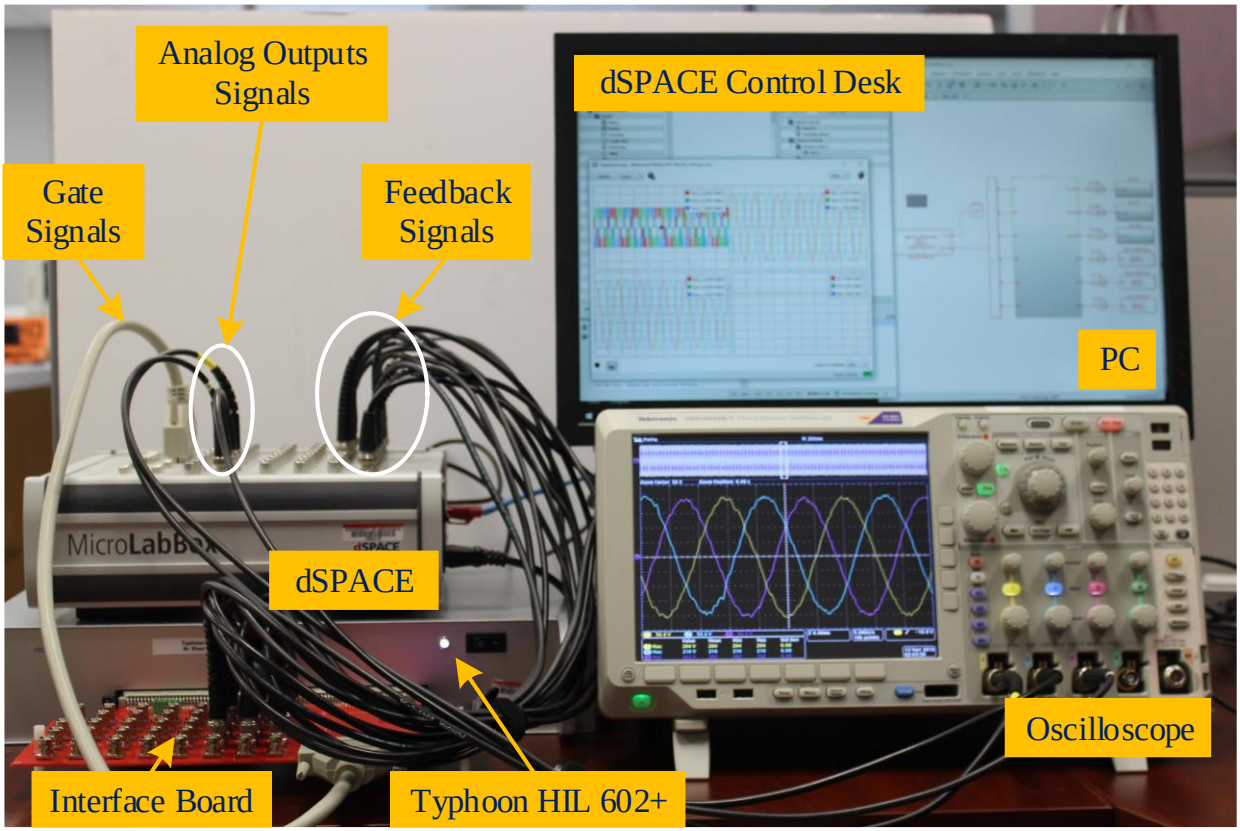


Figure 3.19: Controller hardware-in-the-loop test setup “photo by author”.

3.6.1 C-HIL Test Setup

A picture of the overall C-HIL test setup is shown in Figure 3.19. This C-HIL test setup is composed mainly of Typhoon HIL 602+ device and dSPACE MicroLabBox 1202. An interface board has been designed to interface the two equipment together. Then, using the analog output ports of the interface board, analog feedback signals are extracted, using BNC cables, from the Typhoon HIL 602+ platform. These analog signals have been connected to the dSPACE MicroLabBox 1202 through the analog input ports. The digital gate signals, which are generated using the dSPACE MicroLabBox 1202 have been connected to the Typhoon HIL 602+ using the digital input ports of the interface board. After that, by utilizing the analog output ports of the dSPACE MicroLabBox 1202, the C-HIL results were collected by connecting the BNC cables directly to the oscilloscope as demonstrated in Figure 3.19. The same investigated system parameters, which were used in the simulation studies, are used in C-HIL.

3.6.2 C-HIL Studies

In this subsection, different case scenarios were considered with the aim verifying that the proposed MPC techniques produces better results compared to the traditional MPC ones. The steady-state analysis of the presented MPCC approach is first studied and then compared to that of the typical MPCC method. The performance of the investigated traditional and proposed MPCC methods during current reference transient events were then evaluated. Finally, the performance of the MG, which includes the grid-forming ESS inverter and the grid-following solar inverter, were evaluated during load variations.

- ***Steady State Analysis of the Various MPC Strategies***

Figure 3.20 shows the waveforms of voltages across the dc-link capacitors and phase leg *a* current of the solar inverter as well as the corresponding THD_i when applying the traditional MPCC method. As shown in Figure 3.20, using the conventional MPCC technique with $\lambda_{dc1} = 10$ could achieve peak-to-peak voltage ripples across dc-link capacitors, $\Delta v_{C11,pp}$ and $\Delta v_{C12,pp}$, at 52 V. The THD_i of the solar inverter output current has also been calculated using the oscilloscope to be 3.51 %. Considering the typical MPCC approach where $\lambda_{dc1} = 1$, as shown in Figure 3.21, the THD_i was reduced to 2.38 %, yet $\Delta v_{C11,pp}$ and $\Delta v_{C12,pp}$ increased to 60 V. Unlike the previous case scenario when λ_{dc1} was equal to 10, having $\lambda_{dc1} = 1$ means equal efforts between the controller objectives are considered in this case. Therefore, the quality of the inverter current has been improved at the cost of more NP-V fluctuations. The case scenario, presented in Figure 3.22, also considers using the traditional MPCC method, but with λ_{dc1}, 100 times less than first case scenario. As shown in Figure 3.22, using $\lambda_{dc1} = 0.1$ has led to have more NP-V oscillations, which ultimately increased the THD_i of the solar inverter current. From Figure 3.22, it can be observed that the THD_i has the value of 2.98 % while $\Delta v_{C11,pp}$ and $\Delta v_{C12,pp}$ have become 72 V.

Finally, using $\lambda_{dc1} = 0.1$ with the proposed MPC method allows $\Delta v_{C11,pp}$ and $\Delta v_{C12,pp}$ to reduce from 72 V to 68 V. By using the proposed MPCC strategy, the THD_i of the solar inverter current declined from 2.98% to 2.22% when compared to the traditional MPCC technique with the same weighting factor value. This improvement in the solar inverter output current quality and the NP-V oscillations were achieved since more voltage space vectors have been used within the same 3-L NPC VSC SV diagram. The use of these VSVs also increased the average switching frequency which ultimately led to reduce the ripples of the solar inverter output current. The results of this case are demonstrated in Figure 3.23.

- ***Dynamic Response Analysis of the Various MPC Strategies During a Reference-Step Change***

The dynamic response of the conventional and proposed MPCC techniques are presented in Figures 3.24 and 3.25, respectively, when a change in the reference current, i_a^*, occurs suddenly from 450 A to 800 A. When a current reference-step change is applied, the actual current, i_a, of the classical MPC technique has tracked its reference in around 2.0 *m*s. Similarly, the proposed MPCC method has shown considerably close dynamic response compared to the conventional MPCC one as displayed in Figure 3.25. To further explain, i_a had tracked i_a^* in almost 2.0 *m*s when the proposed MPCC is tested. This comparison validates that the proposed MPCC method still retains the fast-dynamic response of MPC.

- ***Dynamic Response Analysis of the Various MPC Strategies During a Load-Step Change***

Similar to the simulation studies, the transient performance of the proposed MPCC and MPVC methods, when solar generation suddenly increased, was evaluated using the C-HIL. Waveforms of the active power during this transient condition are shown in Figure 3.26. The fast-transient response of the proposed MPCC and MPVC strategies can be clearly seen as the ESS inverter output power dropped immediately from 240 kW to 120 kW when there was a sudden increase in solar inverter output power. Finally, considering the reference rms voltage to be 141.2 V, Figure 3.27 shows that the output voltage, v_o, is 137 V_{rms}, which is within the maximum allowable limits, i.e., ±5 % of the rated voltage. This further validates the proposed MPC techniques have excellent current/voltage reference tracking, and they are robust against the solar power generation and the load variations.

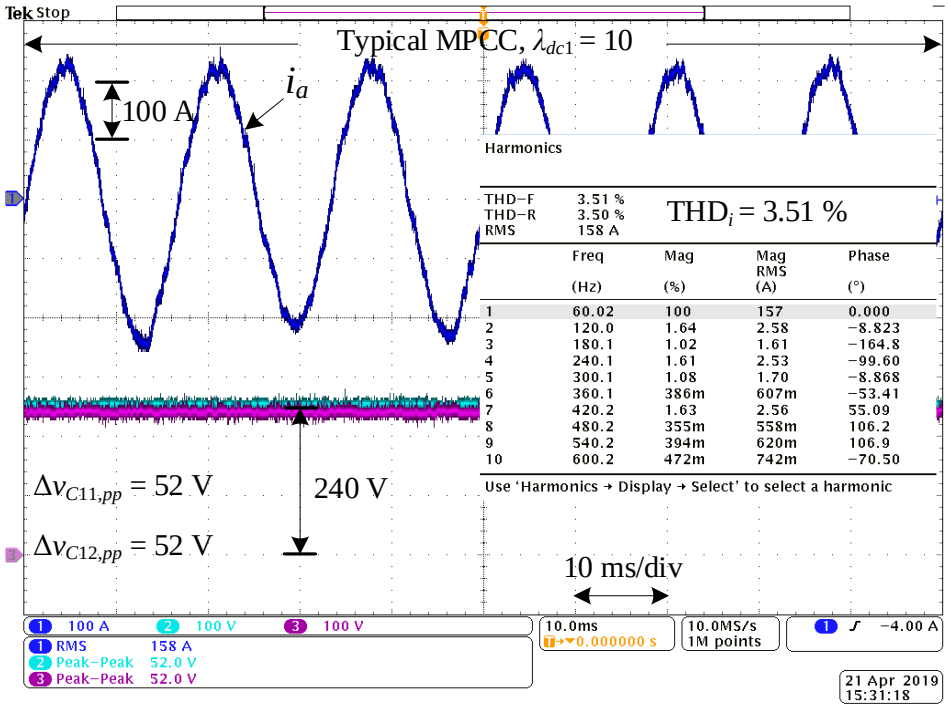


Figure 3.20: Solar inverter current and dc-link voltages using the typical MPCC with λ_{dc1} = 10.

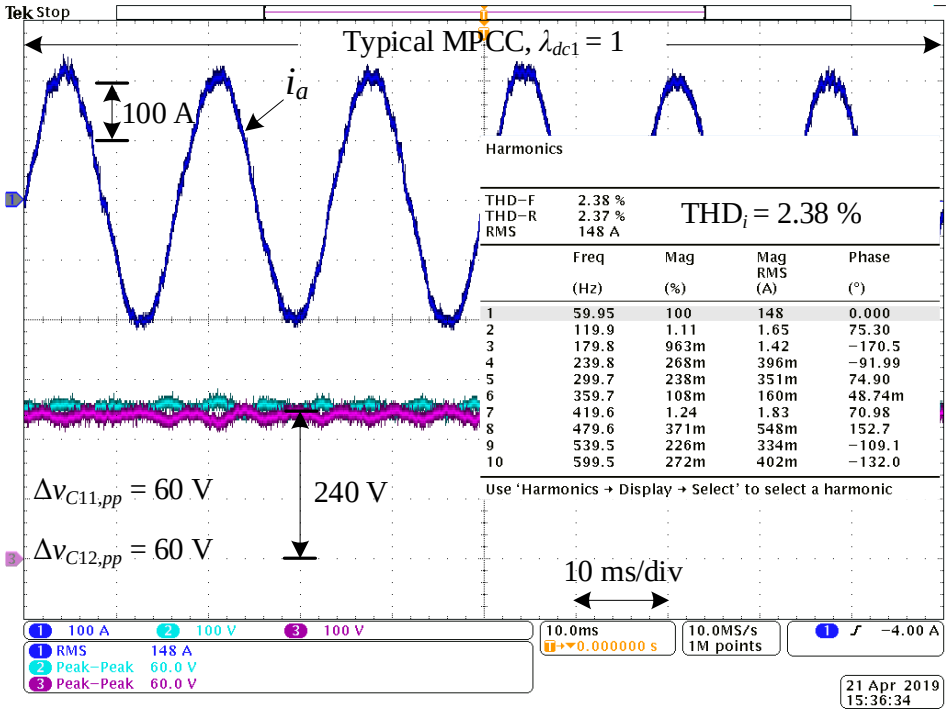


Figure 3.21: Solar inverter current and dc-link voltages using the typical MPCC with λ_{dc1} = 1.

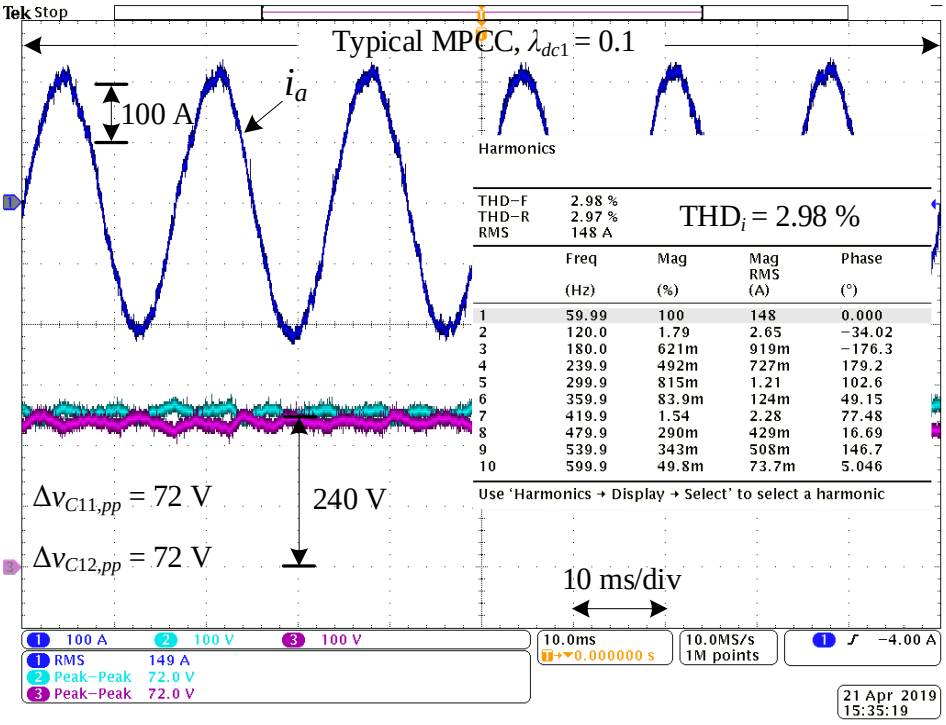


Figure 3.22: Solar inverter current and dc-link voltages using the typical MPCC with λ_{dc1} = 0.1.

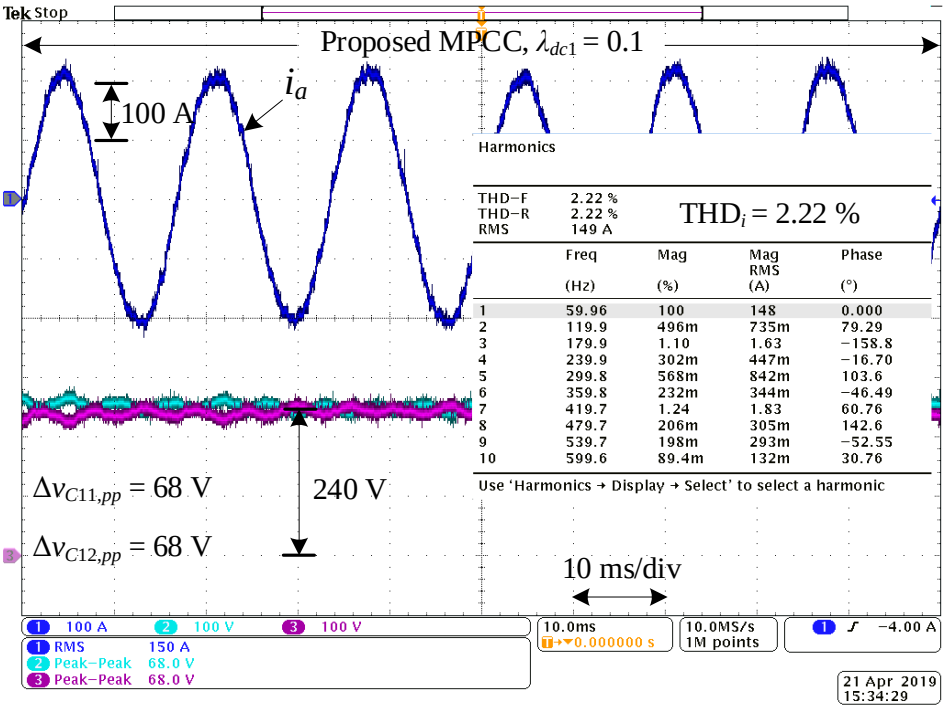


Figure 3.23: Solar inverter current and dc-link voltages using the proposed MPCC with λ_{dc1} = 0.1.

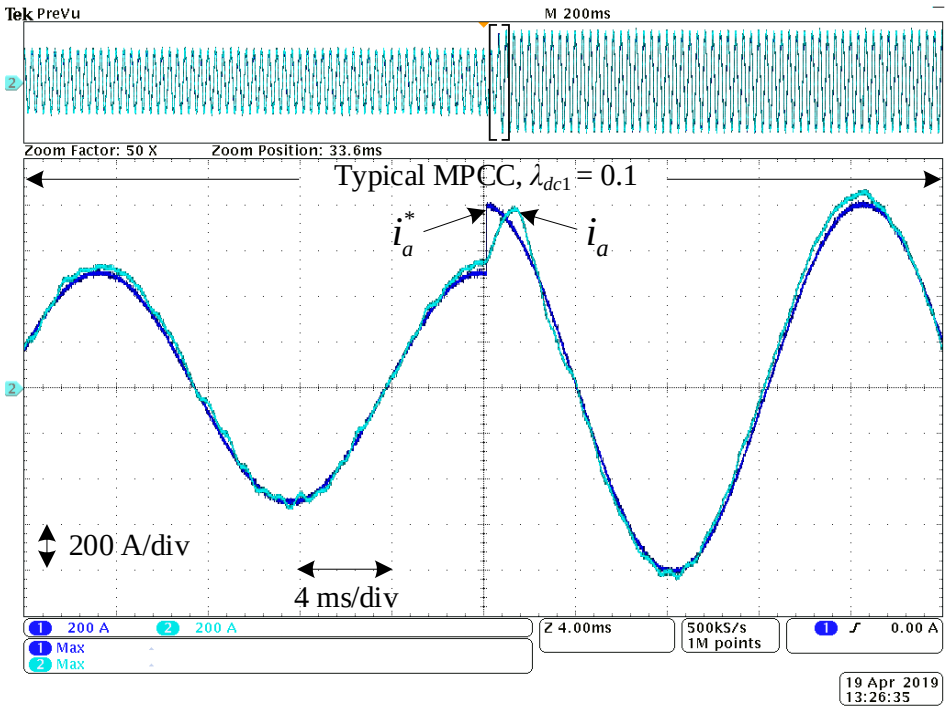


Figure 3.24: Current reference-step change using the typical MPCC.

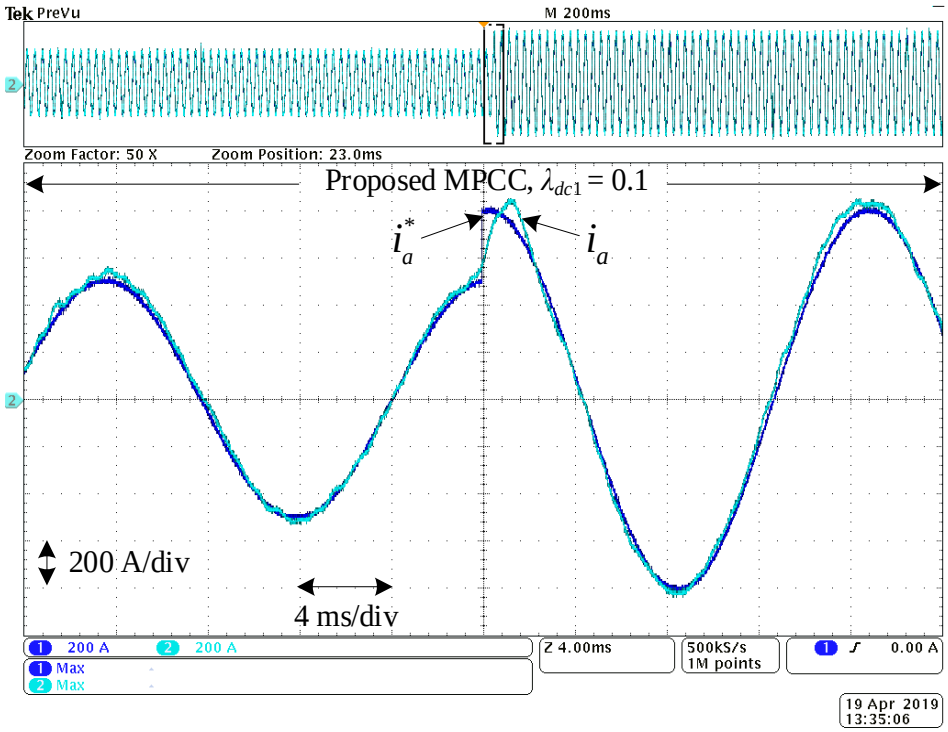


Figure 3.25: Current reference-step change using the proposed MPCC.

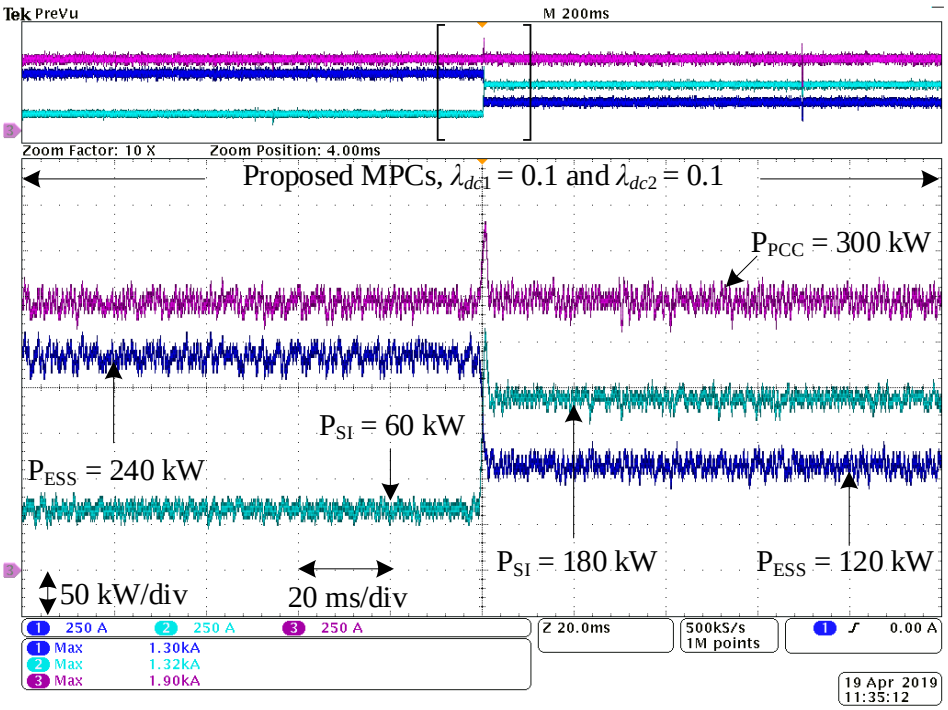


Figure 3.26: Power generated by the ESS inverter, the solar inverter and the total power consumed by the load.

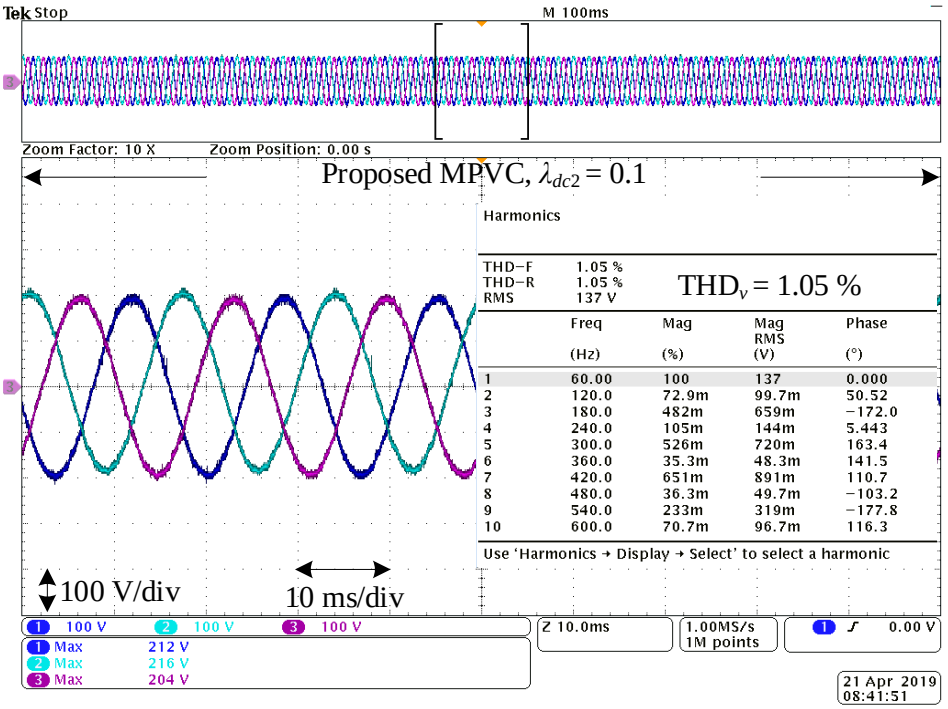


Figure 3.27: Three-phase voltage and THD_v analysis at the PCC.

3.7 Concluding Remarks

Proposed in this chapter is an improved MPC method for three-phase 3-L NPC VSCs operating in different modes. The various 3-L NPC VSCs are assumed to compose a notional MG. While one 3-L NPC VSC is energized using solar panels and connected to the PCC through an *LCL* filter, the other 3-L NPC VSC is powered using an ESS so that it can form the grid voltage and frequency when the main electric grid is disconnected. The improved MPCC and MPVC methods along with the gating signal generation method are explained in detail in this chapter. The switching and conduction power loss model, which is utilized to evaluate the impact of the proposed control strategies on the VSC efficiency was also added to this chapter. In order to evaluate the effectiveness of the proposed MPC approaches, simulation studies using Matlab/Simulink are carried out. It has been concluded from the simulation studies that MPC using the VSVs improves the quality of the VSC output current and voltage waveforms. Moreover, the NP-V fluctuations have been reduced when the VSVs are adopted in the controller design. Furthermore, the proposed MPC technique has led to select a relatively small dc-link capacitor voltages balancing weighting factor in the cost function while maintaining the improved NP-V. To verify the simulation results, the enhanced MPC approaches have been tested using the C-HIL. While the MG is modeled in Typhoon HIL 602+, the controller is applied using dSPACE MicroLabBox 1202. After describing the various component of the test setup, which is adopted in this work, the various C-HIL results have been demonstrated. It can be concluded that the C-HIL studies well match the simulation results, which further validates the contributions of the proposed MPCC and MPVC methods.

Despite the fact that the proposed MPC strategies have been verified to have multiple contributions over the typical ones as described before, it is worth mentioning that the proposed MPC methods still exhibit the drawbacks of the traditional MPC strategies. To illustrate, the

proposed MPC methods still suffer from the problem of having multiple objectives in the cost function. Even though the time needed to tune the weighting factors can be minimized, efforts are still mandatory to determine the optimal weighting factor value. Voltage and current sensors are also still mandatory at the VSC dc side to regulate the NP-V, which increases the cost of the hardware and reduce the system reliability. Furthermore, the digital controller execution time is a trade-off when implementing the VSVs' concept since the number of evaluations for the cost function is increased from 27 to 33 times. Therefore, a novel MPC method, which overcomes these challenges, is to be presented in the next chapter.

CHAPTER 4

A VIRTUAL SPACE VECTORS BASED MPC FOR INHERENT DC LINK VOLTAGE BALANCING OF 3-L T-TYPE CONVERTERS

4.1 Introduction

Adopting model predictive control (MPC) for three-phase three-level (3-L) T-type voltage source converters (VSCs) raises some challenges in the control design. First, for the 3-L T-type VSCs used in microgrid (MG) applications, a low controller sampling time is usually used since the switching frequency for such applications is normally not high. Therefore, implementing the MPC method in such systems generally leads to have a relatively low and variable average switching frequency. This can negatively impact the quality of the 3-L T-type VSC output waveforms [128] and complicate the controller design for the grid-following and grid-forming VSCs. Second, to achieve balanced dc-link capacitor voltages, a quality function, which has a dedicated term for the dc-link capacitor voltages balancing, is mandatory in the controller design such that balanced dc-link capacitor voltages are achieved [122], [123]. This extra term complicates the controller design as it has a weighting factor which requires careful tuning [158].

Therefore, a set of six virtual space vectors (VSVs) have been proposed previously in Chapter 3 to mitigate the aforementioned challenges and improve the controller performance. The addition of these VSVs in the controller design could achieve reduced total harmonic distortion (THD) in the 3-L VSC output voltage and current waveforms. This waveform quality improvement happens due to the fact that increased number of voltage space vectors have been used within the same control period, which increases the average switching frequency. In addition, more voltage space vectors in the space vector (SV) diagram have been used which improves the tracking of the reference signal. Other advantages of using the six VSVs is that the neutral-point voltage (NP-V)

oscillations have been minimized, which allows using a relatively small weighting factor for the balancing term of the dc-link capacitor voltages in the quality function [152].

However, although the use of the six VSVs, proposed in Chapter 4, has improved the control performance, and somehow simplified the quality function design, time and tuning effort are still required to select the optimal weighting factors. For a 3-L VSC topology, voltage and current sensors at the dc side are also unavoidable to ensure well-regulated NP-V oscillations. This drawback not only increases the hardware cost, but also reduces the system reliability as more hardware is needed. Moreover, as a result of the additional six VSVs, the total of the voltage space vectors to be evaluated by the controller is increased from 27 to 33 voltage space vectors, which increases the controller execution time.

Thus, this chapter proposes a new model predictive control (MPC) approach for 3-L VSCs [159]. The presented MPC method should have the following major contributions

- Inherited dc-link capacitor voltages balancing;
- Improved converter output waveform quality;
- Reduced hardware cost, size, weight and wiring complexity;
- Improved system reliability;
- Simplified cost function design;
- Reduced controller execution time.

In this chapter, the proposed MPC strategy has been demonstrated and validated on a three-phase 3-L T-type VSC working in a grid-forming operating mode, where the filter capacitor voltage is the control objective. In other words, the proposed MPC strategy is classified as model predictive voltage control (MPVC). Similar to the controllers proposed in the previous chapter,

the 3-L T-type VSC model, the dc-link capacitor models and the *LC*-filter model, which are derived in Chapter 2, have been used in this chapter. Since the conventional and proposed MPVC methods have been validated experimentally, it is essential to describe the one-step calculation delay in this chapter. The design of the conventional MPVC scheme has also been shown in this chapter. A detailed control description, which includes the proposed MPVC approach design, the gating signals generation and a comparison between various MPCs, have been presented and discussed. The VSC switching and conduction power losses have also been analyzed. Then, simulation results for both control methods are demonstrated in this chapter. The experimental test setup which is used for the work in this chapter has also been explained in detail. The experimental studies for the typical and proposed MPVC technique have been shown and discussed. Finally, some conclusions have been drawn regarding the work proposed in this chapter.

4.2 Typical and Proposed MPVC Strategies for Grid-forming VSCs

Figure 4.1 shows an uninterruptible power supply (UPS), which is designed to feed critical loads connected to the PCC when the ac mains are disconnected. In this system, the 3-L T-type VSC, with the *LC* filter, is operated in the grid-forming mode, where the main objective is to control the *LC*-filter capacitor voltage, which is the load voltage. Typically, robust control strategies, such as sliding mode control (SMC) [160], H_∞ control [161], adaptive control [162], multiple resonant control [163], disturbance rejection control [164], etc. have been used to attenuate harmonic distortion and ensure system stability. MPVC is also a robust control method which can be applied to control UPS systems [140], [165], [166]. Therefore, both conventional and proposed MPVC methods are explained in detail. To apply the MPVC algorithm in digital controllers, it is critical to consider the impact of the one sampling time delay, which is required to execute the control algorithm. Thus, the compensation for this one-step delay is firstly described.

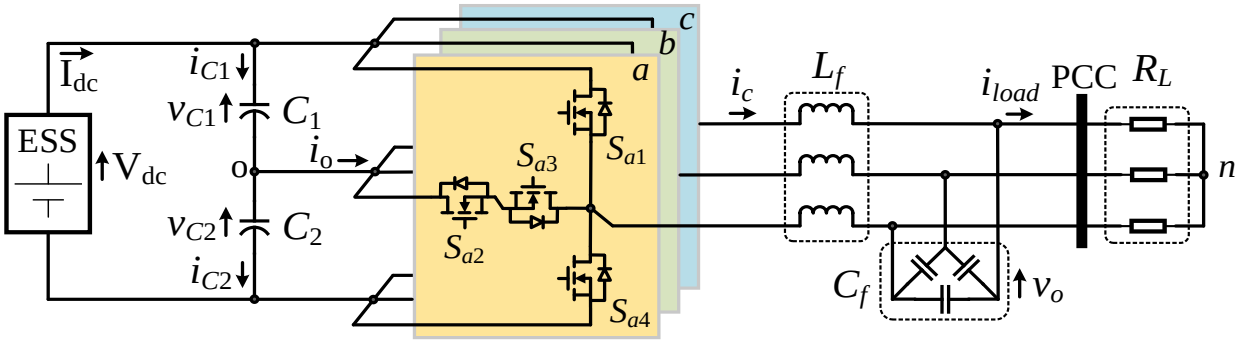


Figure 4.1: Schematic diagram of the system to be studied.

4.2.1 Compensation for the One-Step Calculation Delay

When implementing the MPVC algorithm in digital controllers, the time delay due to the execution of the algorithm should be considered. For instance, by using the information at the sampling instant k, the values of the controlled variables, which are the dc-link capacitor voltages v_{C1} and v_{C2}, and the load voltage, v_o, at the sampling instant $k + 1$ are predicted using (2.8), (2.9) and (2.13), respectively. However, these predicted variables, used in the predictive equations, have to be further shifted one-step forward at sampling instant $k + 2$ prior feeding them into the cost function, such that the one-step calculation delay is compensated. Since the controller sampling time, i.e., T_s, is considerably smaller than the fundamental period of the reference voltage, the reference voltage can be assumed as a constant over two consecutive sampling cycles. As a result, the reference voltage does not need to be extrapolated [123]. The discrete-time models of v_{C1}, v_{C2}, and v_o, expressed in (2.6), (2.7) and (2.11), are updated as follows

$$v_{C1}(k+2) = v_{C1}(k+1) + \frac{T_s}{C_1} i_{C1}(k+1) \tag{4.1}$$

$$v_{C2}(k+2) = v_{C2}(k+1) + \frac{T_s}{C_2} i_{C2}(k+1) \tag{4.2}$$

$$x(k+2) = Ax(k+1) + B_1 v_c(k+1) + B_2 i_{load}(k+1) \tag{4.3}$$

4.2.2 Conventional MPVC Algorithm

The control algorithm of the typical MPVC method is presented in Figure 4.2 while the control block diagram for the implementation of the conventional MPVC strategy is shown in Figure 4.3. To realize MPVC for a 3-L T-type VSC, measurements on both the dc and ac sides are required. On the one hand, the dc-source input current, I_{dc}, and the dc-link capacitor voltages, v_{C1} and/or v_{C2}, are measured at sampling instant k to predict v_{C1} and/or v_{C2} at sampling instant $k + 2$, using (4.1) and (4.2), for the dc-link capacitor voltages control purpose. On the other hand, the VSC-side current, i_c, the *LC*-filter capacitor voltage, v_o, and the load-side current, i_{load}, are sampled at sampling instant k to control the load voltage [140]. Now, v_o can also be predicted two-step ahead at sampling instant $k + 2$ by using (4.3). Then, using the 3-L T-type VSC model, which is described in detail in Chapter 2 and summarized in Figure 2.5, Table 2.1, Table 2.2, and equations (4.1)~(4.3), all the 27 switching states are evaluated in a pre-designed cost function, i.e., g expressed in (4.4), to select the optimal switching states to be applied in the next control iteration [167].

$$g = (v_\alpha^* - v_{o,\alpha}^p)^2 + (v_\beta^* - v_{o,\beta}^p)^2 + \lambda_{dc}(v_{C1}^p - v_{C2}^p) \tag{4.4}$$

where

v_α^* and v_β^*	real and imaginary parts of the load reference voltage;
$v_{o,\alpha}^p$ and $v_{o,\beta}^p$	real and imaginary parts of the load predicted voltage;
v_{C1}^p and v_{C2}^p	predicted dc-link capacitor voltages;
λ_{dc}	weighting factor for the dc-link voltages balancing term.

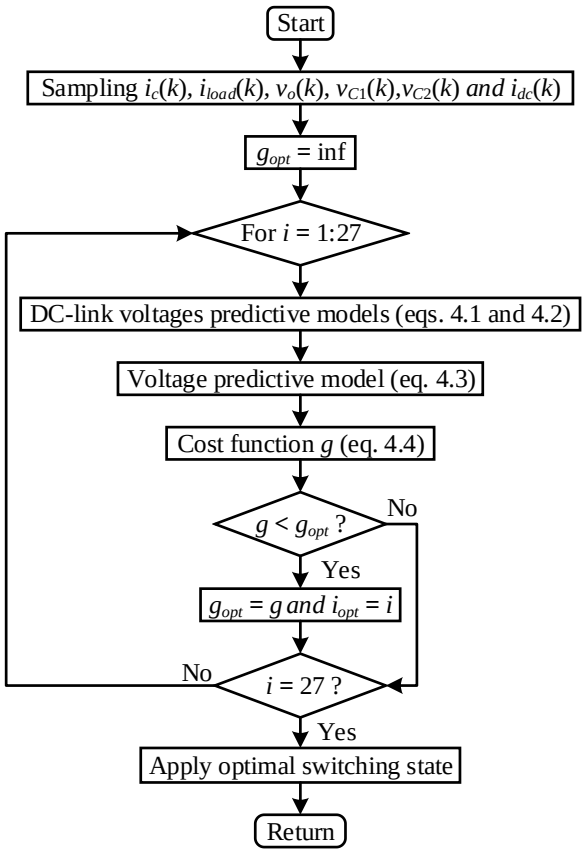


Figure 4.2: Control algorithm of the typical MPVC method.

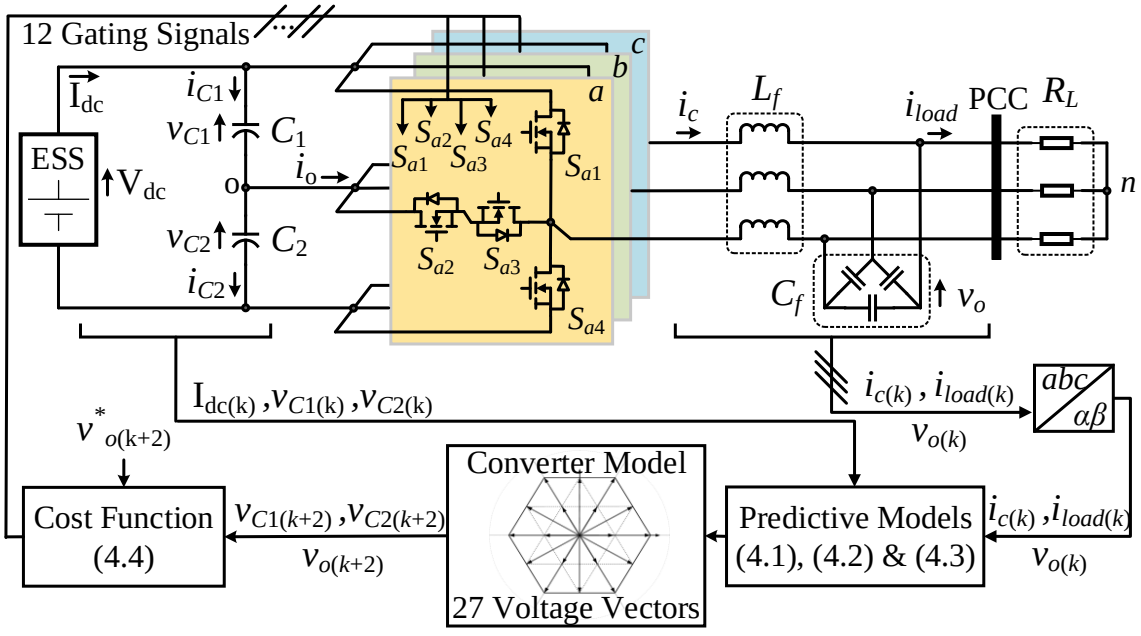


Figure 4.3: Control block diagram of the typical MPVC method for the 3-L T-type VSC.

4.2.3 Proposed MPVC Algorithm

Since S_a, S_b and S_c are the switching states for phase leg *a*, *b*, and *c*, respectively, the switching state of the overall inverter is denoted as (S_a S_b S_c). As shown in Table 2.1 of Chapter 2, in each phase, S_{x1} and S_{x3} are always complementary to each other, while S_{x2} and S_{x4} are also complementary to each other. Therefore, the switching state of phase leg *a*, e.g., S_a, can be represented by switching states of a pair of switch positions, e.g., (S_{a1} S_{a2}). In this work, an extended switching state, i.e., S^*, is defined as (S_{a1} S_{a2} S_{b1} S_{b2} S_{c1} S_{c2}), which will be critical to illustrate the concept and implementation of the VSVs later in this chapter.

Considering all the 27 possible switching states of a 3-L T-type VSC, a total of 19 non-redundant voltage space vectors can be produced. The corresponding SV diagram [127] is shown in Figure 2.3 of Chapter 2. Those 19 non-redundant voltage space vectors are classified into four different categories, which are the zero voltage vectors $\mathbf{V}_0$, the small voltage vectors $\mathbf{V}_{Si}$, the medium voltage vectors $\mathbf{V}_{Mi}$ and the large voltage vectors $\mathbf{V}_{Li}$, where i = 1, …, 6.

As shown in Figure 2.3, the zero voltage vector can be produced by applying three different switching states while each of the small voltage vectors is generated by two variant switching states. Every medium and large voltage vector has only one switching state. When different switching states are used, they can lead to different neutral-point current (NP-C) values. The NP-C associated with each switching state is presented in brackets next to the switching state, as shown in Figure 2.3.

In a 3-L T-type VSC, the instantaneous NP-C, i_o, is critical to the dc-link capacitor voltages balancing. Generally, the NP-V may oscillate or even drift if the average value of i_o is not zero over a sampling period, T_s, since it leads to unbalanced charging and discharging of the top and

bottom dc-link capacitors. Therefore, the NP-V oscillations can be inherently avoided if the average i_o over a sampling period T_s, i.e., I_o, is equal to zero [118]. Using this principle, the concept of the VSVs was proposed in [155] for space vector pulse width modulation (SV-PWM). The VSVs are a set of space vectors synthesized by using a linear combination of multiple original voltage space vectors, where the resulting I_o is zero. In [152], a set of six VSVs were included in the MPC design. This set of the VSVs not only improved the quality of the converter output voltage/current waveforms, but also mitigated the NP-V oscillations, yet a dedicated term in the cost function was still required to maintain balanced dc-link capacitor voltages.

4.2.3.1 VSVs and Extended Switching States Synthetization

Since the MPC method in general is a look-up table based control technique, it is possible to reform the look-up table, which is used in the traditional MPC method, so that it includes only voltage vectors with zero I_o. Therefore, in the work proposed in this chapter, all the voltage vectors, included in the finite control set (FCS), produce zero I_o so that the dc-link capacitor voltages are inherently balanced. To be more specific, all original voltage vectors, which lead to non-zero I_o, are replaced by equivalent VSVs which have the same magnitude and angle but generate zero I_o. This modification in the look-up table eliminates the need of using any dc-link capacitor voltages balancing term in the cost function.

In Figure 2.3, which was presented in Chapter 2, as specified in the brackets, the original voltage space vectors which contribute non-zero I_o are the small voltage vectors $\mathbf{V}_{Si}$ and the medium voltage vectors $\mathbf{V}_{Mi}$ whereas the zero voltage vectors $\mathbf{V}_0$ and the large voltage vectors $\mathbf{V}_{Li}$ generate zero I_o. By extending the methodology proposed in [152], the $\mathbf{V}_{Si}$ as well as the $\mathbf{V}_{Mi}$ can be synthesized in a way where I_o is zero. Hence, the new SV diagram, displayed in Figure 4.4, is proposed in this dissertation.

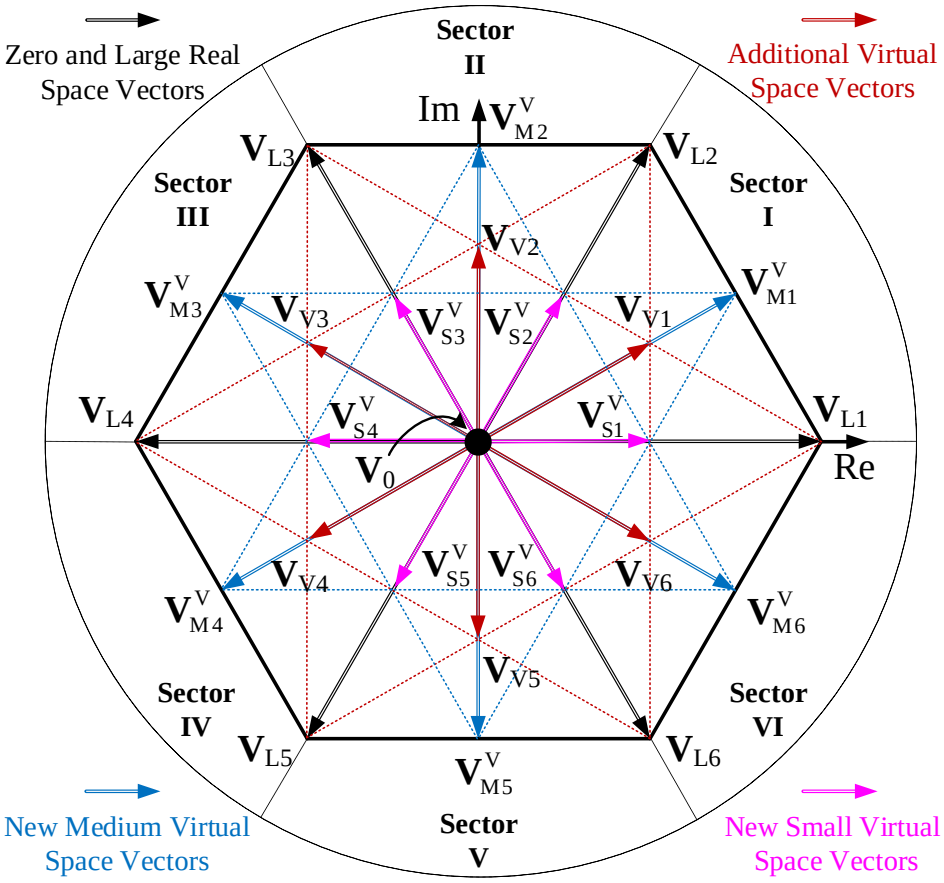


Figure 4.4: SV diagram of a three-phase 3-L T-type VSC with the extended VSVs.

Taking Sector I of the new SV diagram, as an example, the generation of the VSVs and their impact to the dc-link capacitor voltages balancing are analyzed as follows

1) $\mathbf{V}_0$ can be generated by using any of the switching states (–, –, –), (0, 0, 0) or (+, +, +). The corresponding I_o is always zero, which does not affect the NP-V.

2) The new small voltage vector, $\mathbf{v}_{S1}^{V}$, which is a VSV, can be synthesized as follows

$$\mathbf{V}_{S1}^{V} = \frac{\mathbf{V}_{S1}[i_a] + \mathbf{V}_{S2}[-i_a]}{2} \tag{4.5}$$

where $\mathbf{V}_{S1}[i_a]$ is the original small voltage vector with the switching state of (+, 0, 0), which contributes $+i_a$ to i_o when being applied; $\mathbf{V}_{S1}[-i_a]$ is also the original small voltage vector with the switch state of (0, –, –), which contributes $-i_a$ to i_o when being applied. As shown in (4.6),

if each voltage vector is applied for $0.5 \cdot T_s$, I_o shall be zero and the NP-V will not be affected by $\mathbf{v}_{S1}^{V}$. The extended switching state for the $\mathbf{v}_{S1}^{V}$ is determined as

$$\begin{aligned} S^*(\mathbf{V}_{S1}^{V}) &= \frac{S^*(\mathbf{V}_{S1}[i_a])}{2} + \frac{S^*(\mathbf{V}_{S1}[-i_a])}{2} \\ &= \left(\frac{1+0}{2} \quad \frac{1+1}{2} \quad \frac{0+0}{2} \quad \frac{1+0}{2} \quad \frac{0+0}{2} \quad \frac{1+0}{2} \right) \\ &= \left(\frac{1}{2} \quad 1 \quad 0 \quad \frac{1}{2} \quad 0 \quad \frac{1}{2} \right) \end{aligned} \tag{4.6}$$

3) The new medium VSV, $\mathbf{v}_{M1}^{V}$, is synthesized by the nearest two large voltage vectors, i.e., $\mathbf{V}_{L1}[0]$ and $\mathbf{V}_{L2}[0]$. To be specific, each of the $\mathbf{V}_{L1}$ with the switching state of (+, –, –) and the $\mathbf{V}_{L2}$ with the switching state of (+, +, –) are applied for $0.5 \cdot T_s$. This equitable combination results in a VSV, which is equivalent to the original $\mathbf{V}_{M1}$ but with zero I_o. The $\mathbf{v}_{M1}^{V}$ and its associated extended switching state are determined using (4.7) and (4.8), respectively.

$$\mathbf{V}_{M1}^{V} = \frac{\mathbf{V}_{L1}[0] + \mathbf{V}_{L2}[0]}{2} \tag{4.7}$$

$$\begin{aligned} S^*(\mathbf{V}_{M1}^{V}) &= \frac{S^*(\mathbf{V}_{L1}[0])}{2} + \frac{S^*(\mathbf{V}_{L2}[0])}{2} \\ &= \left(\frac{1+1}{2} \quad \frac{1+1}{2} \quad \frac{0+1}{2} \quad \frac{0+1}{2} \quad \frac{0+0}{2} \quad \frac{0+0}{2} \right) \\ &= \left(1 \quad 1 \quad \frac{1}{2} \quad \frac{1}{2} \quad 0 \quad 0 \right) \end{aligned} \tag{4.8}$$

4) The original large voltage vectors, $\mathbf{V}_{L1}[0]$ and $\mathbf{V}_{L2}[0]$, do not affect the NP-V since they produce zero I_o.

5) Finally, the additional six VSVs, $\mathbf{V}_{V1}$ to $\mathbf{V}_{V6}$, are included in FCS to improve the reference tracking and enhance the quality of the VSC output waveforms [152]. The VSV, $\mathbf{V}_{V1}$, along with its extended switching state are produced as follows

$$\mathbf{V}_{V1} = \frac{(\mathbf{V}_{S1}[i_a] + \mathbf{V}_{S2}[i_c] + \mathbf{V}_{M1}[i_b])}{3} \tag{4.9}$$

$$
\begin{aligned}
S^*(\mathbf{V}_{V1}) &= \frac{S^*(\mathbf{V}_{S1}[i_a])}{3} + \frac{S^*(\mathbf{V}_{S2}[i_c])}{3} + \frac{S^*(\mathbf{V}_{M1}[i_b])}{3} \\
&= \left(\frac{0+1+1}{3} \quad \frac{1+1+1}{3} \quad \frac{0+0+1}{3} \quad \frac{0+1+1}{3} \quad \frac{0+0+0}{3} \quad \frac{0+0+1}{3} \right) \\
&= \left(\frac{2}{3} \quad 1 \quad \frac{1}{3} \quad \frac{2}{3} \quad 0 \quad \frac{1}{3} \right)
\end{aligned}
\tag{4.10}
$$

Figure 4.4 shows the proposed SV diagram, including all the new small VSVs, $\mathbf{v}_{Si}^{v}$, the new medium VSVs, $\mathbf{v}_{Mi}^{v}$, and the additional six VSVs, $\mathbf{V}_{Vi}$. The generation of the extended switching states for $\mathbf{v}_{Si}^{v}$ and $\mathbf{v}_{Mi}^{v}$ are explained in Table 4.1 whereas Table 4.2 has the extended switching states for the additional six VSVs, $\mathbf{V}_{Vi}$.

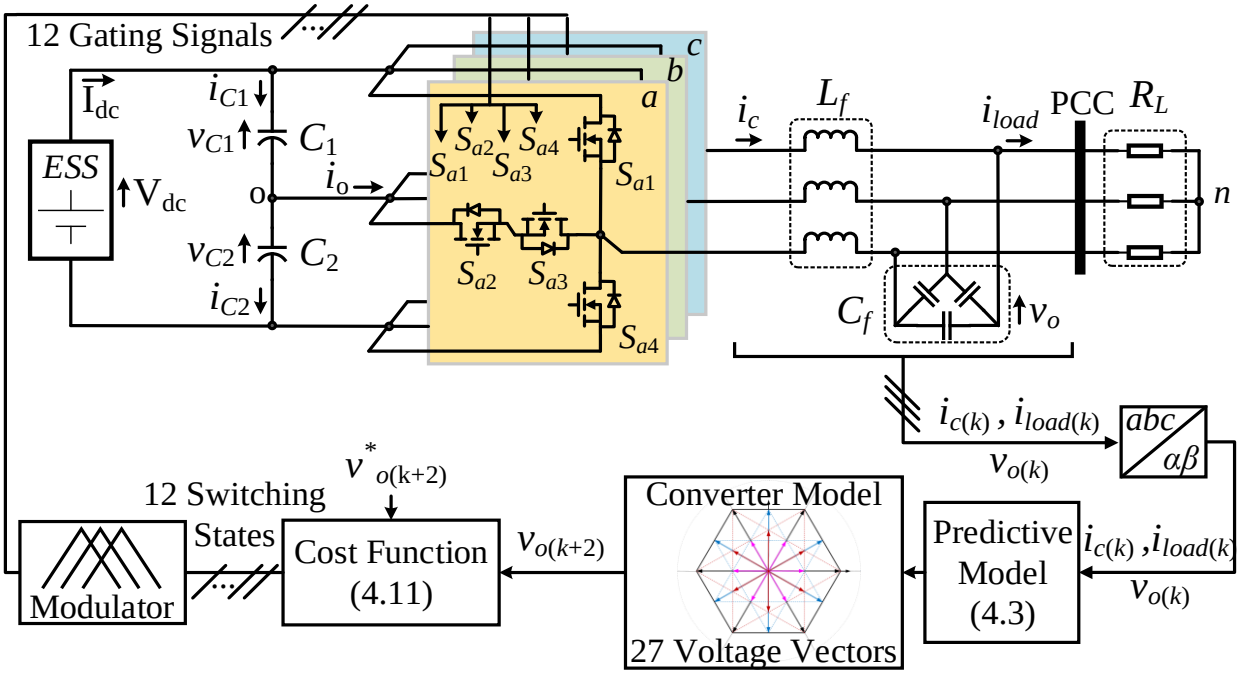


Figure 4.5: Control block diagram of the proposed MPVC method for the 3-L T-type VSC.

The control block diagram of the proposed MPVC technique using the VSVs concept, which has been implemented on the three-phase 3-L T-type VSC with an output *LC* filter, is shown in Figure 4.5. It is worth noting that the proposed controller requires measurements only from the load side, since the dc-link capacitor voltages balancing will be achieved inherently. Compared to the conventional MPVC method, the total number of voltage vectors to be evaluated by the

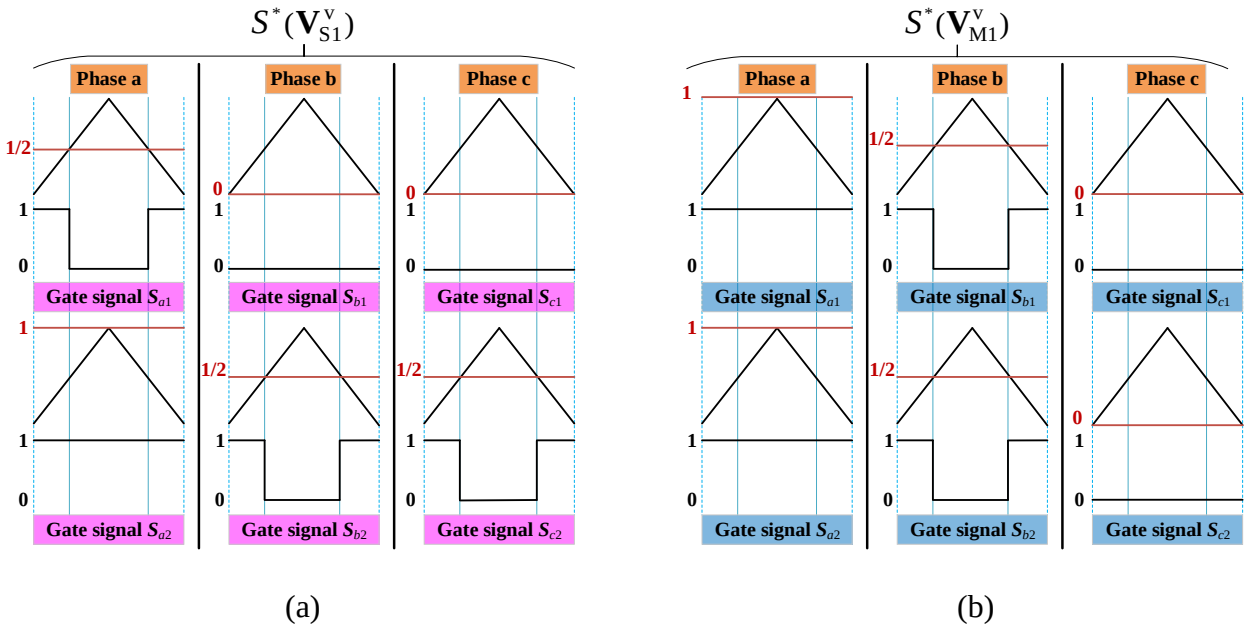
proposed MPVC strategy over one sampling period has remained unchanged, which is 27 voltage vectors. Finally, due to the inherently balanced dc-link capacitor voltages, the cost function, *g*, can be updated as in (4.11) to include only the load voltage.

$$g = (v_{\alpha}^{*} - v_{o,\alpha}^{p})^2 + (v_{\beta}^{*} - v_{o,\beta}^{p})^2 \tag{4.11}$$

4.2.3.2 Gate Signal Implementation

In the work proposed in this chapter, a PWM modulator, shown in Figure 4.5, has been used as an auxiliary tool to implement the extended switching states which have been already calculated and summarized in Table 4.1 and Table 4.2, and eventually generate the VSVs. Using the modulator, the extended switching state of the optimal VSV is compared to a carrier waveform which has a fixed period that is equal to the controller sampling time, T_s. An illustration of generating the gate signals of the new small and medium VSVs, $\mathbf{V}_{S1}^{V}$ and $\mathbf{V}_{M1}^{V}$, is presented in Figures 4.6(a) and (b), respectively. The gate signals generation of the $\mathbf{V}_{V1}$ is demonstrated in Figure 4.7.

It is important to mention that the MPVC algorithm, which is presented in Figure 4.2, has to be updated due to the fact that the proposed MPVC algorithm requires measurements from only the load side. Therefore, the new MPVC algorithm is depicted in Figure 4.8.



(a) (b)

Figure 4.6: An illustration of the gate signal generation for (a) small VSV, $\mathbf{v}_{S1}^{v}$ and (b) medium VSV, $\mathbf{v}_{M1}^{v}$.

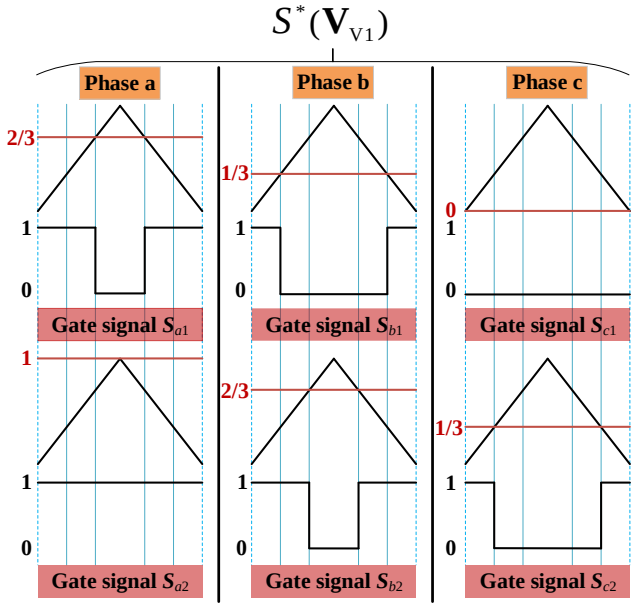


Figure 4.7: An illustration of the gate signal generation for the additional VSV, $\mathbf{V}_{V1}$.

Table 4.1
Summary for the New Small and Medium VSVs and Their Extended Switching States

VSV	$\mathbf{V}_x$	$S(\mathbf{V}_x)$	$\mathbf{V}_y$	$S(\mathbf{V}_y)$	Extended Switching States					
					S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}
$\mathbf{V}_{S1}^{V}$	$\mathbf{V}_{S1}[-i_a]$	(+, 0, 0)	$\mathbf{V}_{S1}[i_a]$	(0, –, –)	1/2	1	0	1/2	0	1/2
$\mathbf{V}_{S2}^{V}$	$\mathbf{V}_{S2}[-i_c]$	(0, 0, –)	$\mathbf{V}_{S1}[i_c]$	(+, +, 0)	1/2	1	1/2	1	0	1/2
$\mathbf{V}_{S3}^{V}$	$\mathbf{V}_{S3}[-i_b]$	(0, +, 0)	$\mathbf{V}_{S3}[i_b]$	(–, 0, –)	0	1/2	1/2	1	0	1/2
$\mathbf{V}_{S4}^{V}$	$\mathbf{V}_{S4}[-i_a]$	(–, 0, 0)	$\mathbf{V}_{S4}[i_a]$	(0, +, +)	0	1/2	1/2	1	1/2	1
$\mathbf{V}_{S5}^{V}$	$\mathbf{V}_{S5}[-i_c]$	(0, 0, +)	$\mathbf{V}_{S5}[i_c]$	(–, –, 0)	0	1/2	0	1/2	1/2	1
$\mathbf{V}_{S6}^{V}$	$\mathbf{V}_{S6}[-i_b]$	(0, –, 0)	$\mathbf{V}_{S6}[i_b]$	(+, 0, +)	1/2	1	0	1/2	1/2	1
$\mathbf{V}_{M1}^{V}$	$\mathbf{V}_{L1}[0]$	(+, –, –)	$\mathbf{V}_{L2}[0]$	(+, +, –)	1	1	1/2	1/2	0	0
$\mathbf{V}_{M2}^{V}$	$\mathbf{V}_{L2}[0]$	(+, +, –)	$\mathbf{V}_{L3}[0]$	(–, +, –)	1/2	1/2	1	1	0	0
$\mathbf{V}_{M3}^{V}$	$\mathbf{V}_{L3}[0]$	(–, +, –)	$\mathbf{V}_{L4}[0]$	(–, +, +)	0	0	1	1	1/2	1/2
$\mathbf{V}_{M4}^{V}$	$\mathbf{V}_{L4}[0]$	(–, +, +)	$\mathbf{V}_{L5}[0]$	(–, –, +)	0	0	1/2	1/2	1	1
$\mathbf{V}_{M5}^{V}$	$\mathbf{V}_{L5}[0]$	(–, –, +)	$\mathbf{V}_{L6}[0]$	(+, –, +)	1/2	1/2	0	0	1	1
$\mathbf{V}_{M6}^{V}$	$\mathbf{V}_{L6}[0]$	(+, –, +)	$\mathbf{V}_{L1}[0]$	(+, –, –)	1	1	0	0	1/2	1/2

Table 4.2
Summary for the Additional Six VSVs and Their Extended Switching States

VSV	$\mathbf{V_x}$	$S(\mathbf{V_x})$	$\mathbf{V_y}$	$S(\mathbf{V_y})$	$\mathbf{V_z}$	$S(\mathbf{V_z})$	Extended Switching States					
							S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}
$\mathbf{V}_{V1}$	$\mathbf{V}_{S1}[i_a]$	(0,–,–)	$\mathbf{V}_{S2}[i_c]$	(+,+,0)	$\mathbf{V}_{M1}[i_b]$	(+,0,–)	2/3	1	1/3	2/3	0	1/3
$\mathbf{V}_{V2}$	$\mathbf{V}_{S2}[i_c]$	(+,+,0)	$\mathbf{V}_{S3}[i_b]$	(–,0,–)	$\mathbf{V}_{M2}[i_a]$	(0,+,–)	1/3	2/3	2/3	1	0	1/3
$\mathbf{V}_{V3}$	$\mathbf{V}_{S3}[i_b]$	(–,0,–)	$\mathbf{V}_{S4}[i_a]$	(0,+,+)	$\mathbf{V}_{M3}[i_c]$	(–,+,0)	0	1/3	2/3	1	1/3	2/3
$\mathbf{V}_{V4}$	$\mathbf{V}_{S4}[i_a]$	(0,+,+)	$\mathbf{V}_{S5}[i_c]$	(–,–,0)	$\mathbf{V}_{M4}[i_b]$	(–,0,+)	0	1/3	1/3	2/3	2/3	1
$\mathbf{V}_{V5}$	$\mathbf{V}_{S5}[i_c]$	(–,–,0)	$\mathbf{V}_{S6}[i_b]$	(+,0,+)	$\mathbf{V}_{M5}[i_a]$	(0,–,+)	1/3	2/3	0	1/3	2/3	1
$\mathbf{V}_{V6}$	$\mathbf{V}_{S6}[i_b]$	(+,0,+)	$\mathbf{V}_{S1}[i_a]$	(0,–,–)	$\mathbf{V}_{M6}[i_c]$	(+,–,0)	2/3	1	0	1/3	1/3	2/3

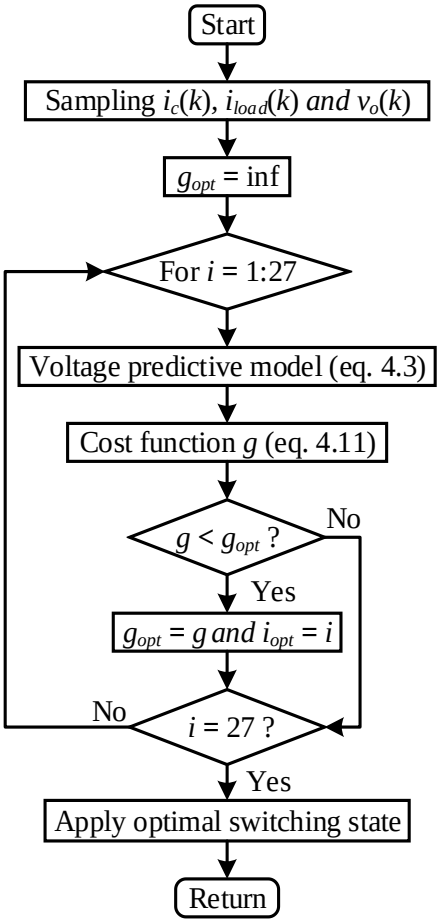


Figure 4.8: Control algorithm of the proposed MPVC.

4.2.3.3 SV Diagrams Comparisons of Different MPCs

As a comparison, Figure 4.9 describes the differences among the SV diagrams of the conventional MPC, enhanced MPC [152] and proposed MPC. A summary is also provided in Table 4.3 to show the voltage vectors that are used in the three different MPC methods and their effect on the NP-C, I_o. When comparing the enhanced MPC strategy [152] with the typical MPC one, a total of six additional VSVs, with zero NP-C, have been added to the FCS. However, the enhanced MPC still has 12 different voltage vectors which affect the NP-V. On the contrary, the proposed MPC strategy does not have any voltage vector which contributes non-zero I_o. This leads to have inherited balanced dc-link capacitor voltages.

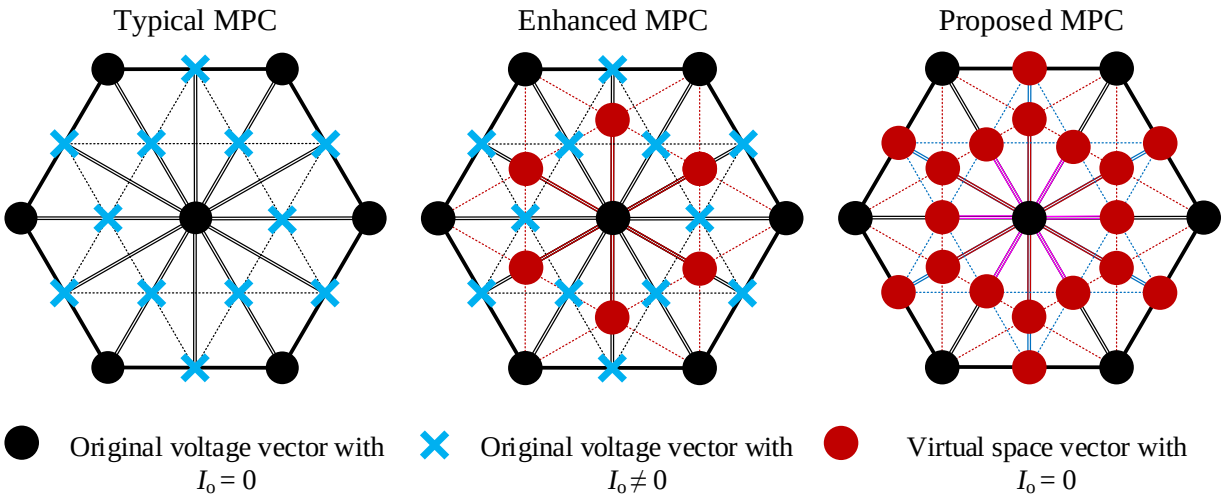


Figure 4.9: An illustration of the impact of different voltage space vectors on the VSC NP-C.

Table 4.3
Impact of Different Voltage Space Vectors on the NP-C of the 3-L T-type VSC

Impact of Voltage Vectors on NP-C	Typical MPC	Enhanced MPC [152]	Proposed MPC
Non-zero NP-C ($I_o \neq 0$)	$\mathbf{V}_{S1} \sim \mathbf{V}_{S6}$ $\mathbf{V}_{M1} \sim \mathbf{V}_{M6}$	$\mathbf{V}_{S1} \sim \mathbf{V}_{S6}$ $\mathbf{V}_{M1} \sim \mathbf{V}_{M6}$	None
Zero NP-C ($I_o = 0$)	$\mathbf{V}_0$ $\mathbf{V}_{L1} \sim \mathbf{V}_{L6}$	$\mathbf{V}_0$ $\mathbf{V}_{L1} \sim \mathbf{V}_{L6}$ $\mathbf{V}_{V1} \sim \mathbf{V}_{V6}$	$\mathbf{V}_0$ $\mathbf{V}^{V}_{S1} \sim \mathbf{V}^{V}_{S6}$ $\mathbf{V}^{V}_{M1} \sim \mathbf{V}^{V}_{M6}$ $\mathbf{V}_{L1} \sim \mathbf{V}_{L6}$ $\mathbf{V}_{V1} \sim \mathbf{V}_{V6}$

To summarize, compared to the typical MPVC method, the adoption of the proposed MPVC using the VSVs has resulted in multiple advantages. First, as expressed in (4.11), the cost function, used with the proposed MPVC method, has only one objective when compared with that of the traditional MPVC technique, which is a dual-objective cost function as expressed in (4.4). Having a sole-objective quality function simplifies the controller design because no weighting factors are required to be tuned. Since the proposed MPVC algorithm does not have any term related to the dc-link capacitors or their measured voltages, more reliable and robust control for the NP-V can

also be achieved. This is due to the fact that the proposed MPVC approach is independent of the dc-link capacitors' values. Therefore, having inconsistent values of dc-link capacitors due to aging does not deteriorate the controller performance. The number of voltage and current sensors, required by the proposed MPVC strategy, has also been reduced due to the inherent dc-link capacitor voltages balancing, which ultimately reduces the system overall cost. Additionally, having a simplified control algorithm in the proposed MPVC method has resulted in less computational burden for the digital controller. Using dSPACE MicroLabBox, the controller execution time, T_{MPC}, of the traditional and proposed MPVC methods are 14.8 μs and 11.2 μs, respectively. This can reduce the algorithm computational time of the proposed MPVC strategy, which allows the algorithm to be implemented in a less powerful digital controller. Moreover, the SV diagram of the proposed MPVC technique, depicted in Figure 4.4, has six more voltage vectors, referred to as additional six VSVs, compared to that of the traditional MPVC strategy, which is depicted in Figure 2.3 of Chapter 2. Having more voltage vectors in the SV diagram should improve the reference tracking as well as the VSC output waveform quality.

4.3 Power Loss Analysis

Similar to the enhanced MPC method presented in the previous chapter, the proposed MPVC strategy increases the equivalent switching frequency of the 3-L T-type VSC because more voltage space vectors are applied within the same control period, T_s. Therefore, it is critical to evaluate the power losses and ensure the 3-L T-type VSC efficiency is not severely affected when considering such approach. Therefore, in this work, the same power semiconductor device switching and conduction loss model which is explained in Section 3.4 of Chapter 3 has been used to evaluate the efficiency of the three-phase 3-L T-type VSC when the typical and proposed MPC methods are utilized [156]. The power loss analysis is performed for the switch positions S_{a1} and S_{a2} which

are demonstrated in Figure 4.1. Similar to the switching and conduction loss model, described in the previous chapter to calculate the losses for the 3-L NPC VSC, the other two power switches of phase leg *a*, i.e., S_{a3} and S_{a4}, are complementary, which means they should have similar results to the main power switches. Therefore, only the switching loss of S_{a1} and S_{a2} is simulated and presented in this chapter. Similarly, the conduction loss of the two primary power switches is demonstrated in this chapter since the other power switching devices, i.e., S_{a3} and S_{a4}, are complementary.

The 3-L T-type VSC single-phase power loss is calculated using the loss model presented in (3.6) of the previous chapter. The three-phase VSC power loss is also calculated by using the loss model which is expressed in (3.7).

4.4 Simulation Studies

The effectiveness and feasibility of the proposed MPVC method have been validated using simulation studies in the Matlab/Simulink. Presented in Table 4.4 are the investigated system simulation parameters. The main targets of the simulation studies are 1) demonstrating the issue of having unbalanced dc-link capacitor voltages; 2) showing the proposed MPVC using the VSVs has a steady-state performance which is better than that of the traditional MPVC method; 3) presenting the proposed MPVC approach has a similar dynamic response to that of the traditional MPVC one; 4) performing the parameter-sensitivity test to show both control strategies are robust against parameter uncertainties and 5) performing power loss analysis to ensure the efficiency of the 3-L T-type VSC is not sacrificed as a result of using the VSVs.

Table 4.4
Investigated System Simulation Parameters

Parameter	Description	Value
V_{dc}	ESS voltage	300 V
C_1 and C_2	DC-link capacitance	1700 μF
L_f	Filter inductance	0.15 mH
C_f	Filter capacitance	250 μF
R_L	Load resistance	0.43 Ω
v_o	Load voltage (rms)	120 V
f	Nominal frequency	60 Hz
T_s	Controller sampling time	50 μs

- ***The Impact of Weighting Factor Selection***

As presented in Figure 4.10, having a well-regulated NP-V requires adding a term with a weighting factor, i.e., λ_{dc}, in the cost function, g expressed in (4.4), specifically for the dc-link capacitor voltages balancing. In this test, first, the simulated system has been run when λ_{dc} is zero to show the impact of having unbalanced dc-link capacitor voltages on the system. Then, the value of λ_{dc} has been selected carefully to be 0.05 so that compromised results between the regulation of the NP-V fluctuations and other objective(s) which is the load voltage in this chapter can be achieved. As shown in Figure 4.10, selecting a value of zero for λ_{dc} has resulted in having unbalanced dc-link capacitor voltages. As soon as the value of λ_{dc} has become 0.05, the dc-link capacitor voltages have been perfectly balanced.

The quality of the T-type VSC line-to-line (L-to-L) voltage, i.e., $v_{c,ab}$, has been negatively affected by the voltage divergence of the dc-link upper and lower capacitors as demonstrated in Figure 4.11. However, as soon as the dc-link capacitor voltages are perfectly balanced, i.e., $v_{C1} = v_{C2}$, $v_{c,ab}$ has shown a three-level waveform shape, which validates having unbalanced dc-link capacitor voltages could deteriorate the VSC output waveforms quality.

Additionally, if the dc-link capacitor voltages, i.e., v_{C1} and v_{C2}, are unbalanced, the quality of the three-phase L-to-L load voltage, i.e., $v_{o,abc}$ presented in Figure 4.12, is deteriorated. To explain, when λ_{dc} is zero, the THD_v has been calculated to be 2.06 % as expressed in Figure 4.12. However, 0.70 % reduction in the THD_v of the load voltage has been observed once λ_{dc} has been selected to be 0.05.

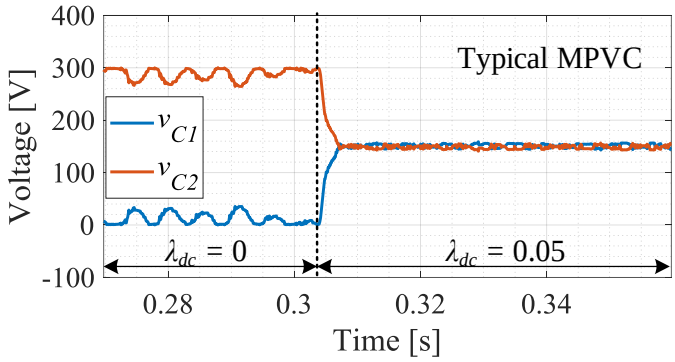


Figure 4.10: Dc-link capacitor voltages during a weighting factor step change.

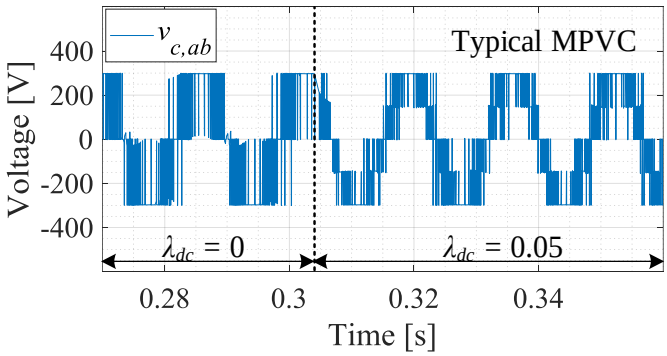


Figure 4.11: VSC voltage during a weighting factor step change.

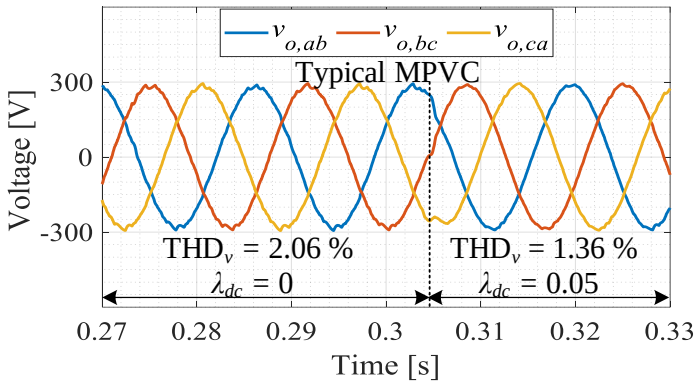


Figure 4.12: Load voltage during a weighting factor step change.

- ***Steady-State Analysis***

Figures 4.13 to 4.16 show various simulation results using the typical and proposed MPVC methods during the T-type VSC steady-state operation. As demonstrated in Figure 4.13, applying the typical MPVC strategy on the system results in having peak-to-peak voltage ripples, i.e., $\Delta v_{C,pp}$, across each dc-link capacitor, e.g., 15 V. However, when the proposed MPVC technique has been implemented, $\Delta v_{C,pp}$ has been determined to be only 5 V. This means that $\Delta v_{C,pp}$ of the classical MPVC is three times higher than that of the proposed MPVC using VSVs.

Another typical steady-state results to be evaluated is the L-to-L peak voltage which is generated by the VSC, i.e., $v_{c,ab}$ presented in Figure 4.14. Using the proposed MPVC strategy can cause significant increase in the switching frequency which can be observed in $v_{c,ab}$. The load three-phase L-to-L voltage, i.e., $v_{o,abc}$, and the THD$_v$ analysis are demonstrated in Figures 4.15 and 4.16, respectively. As shown in Figure 4.15, while the peak value of $v_{o,abc}$ using the traditional MPVC method has been determined to be 287.1 V, the proposed MPVC technique has improved voltage reference tracking relative to the traditional one. To explain, using the VSVs concept has resulted in having the peak value of $v_{o,abc}$ to be 290.6 V. This means the steady-state error of $v_{o,abc}$,

i.e., ε_v, has been decreased from 2.31 % to 1.12 % using the typical and proposed MPVC strategies, respectively. In addition, the quality of $v_{o,abc}$ has been enhanced when the MPVC using VSVs is used. Figure 4.16 shows the voltage spectra of $v_{o,abc}$ when both control methods are applied. It can be seen that using the proposed MPVC algorithm has reduced the THD_v of $v_{o,abc}$ to 0.90 % when compared to that of the traditional MPVC one which has the value of 1.36 %.

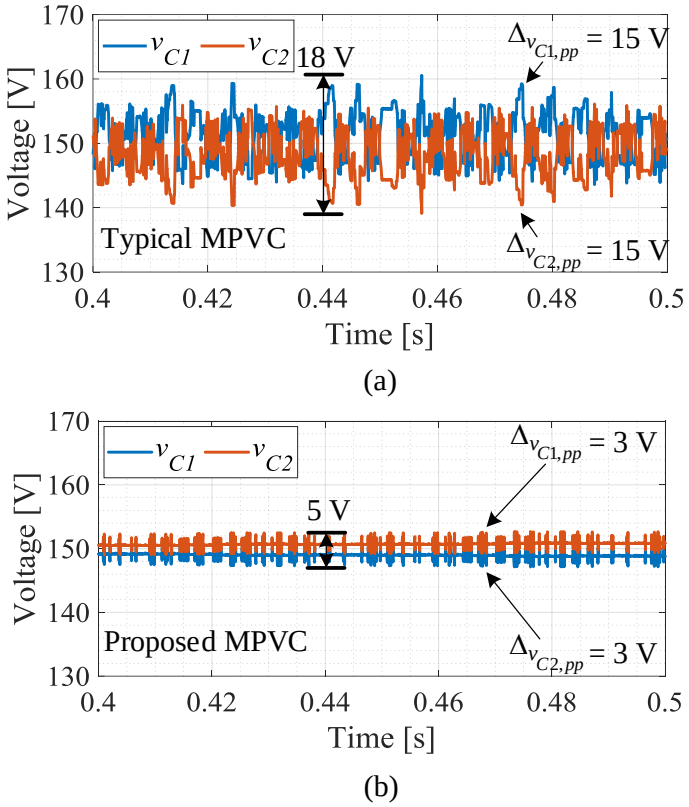


Figure 4.13: Dc-link voltages during steady-state conditions using (a) typical MPVC (b) proposed MPVC.

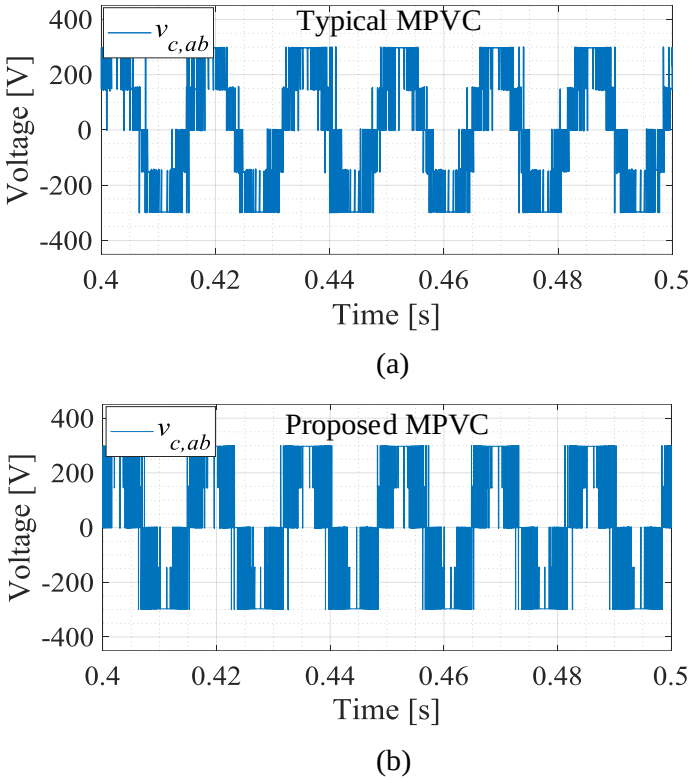


Figure 4.14: Converter voltage during steady-state conditions using (a) typical MPVC (b) proposed MPVC.

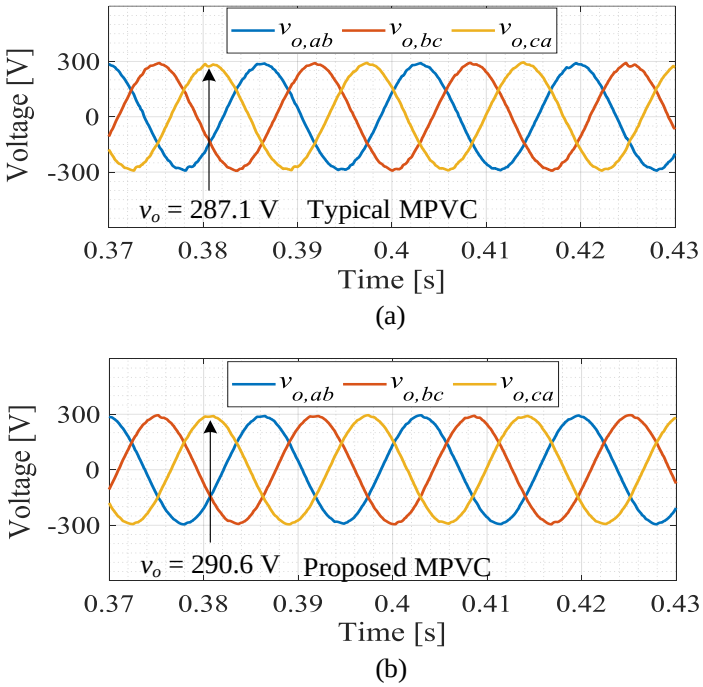


Figure 4.15: Load voltage during steady-state conditions using (a) typical MPVC (b) proposed MPVC.

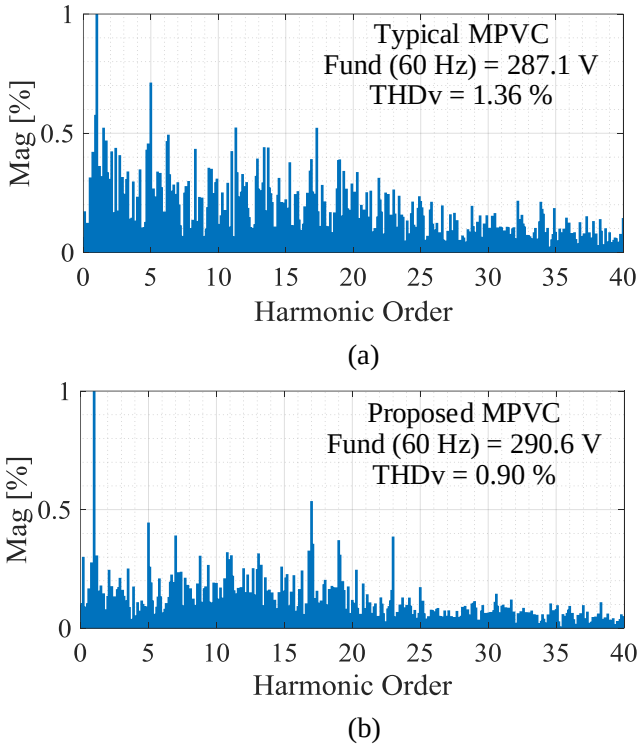


Figure 4.16: Load voltage spectra during-steady state conditions using (a) typical MPVC (b) proposed MPVC.

- ***Dynamic Response Analysis During a Load-Step Change***

The performance of the conventional and proposed MPVC methods during a load transient have been evaluated when a load-step change, from no load to full load, is applied at t = 0.304 s. The results are presented in Figures 4.17 to 4.20. The dc-link capacitor peak-to-peak voltage ripples, $\Delta v_{C,pp}$, the load voltage, $v_{o,abc}$, the load current, $i_{load,abc}$, and the power consumed by the load, P_{load} have been compared when either of the control strategies are implemented.

As presented in Figure 4.17, connecting the load at t = 0.304 s does not have significant influence on $\Delta v_{C,pp}$ when either control techniques are applied. By using the presented MPVC technique, $\Delta v_{C,pp}$ across the upper and lower dc-link capacitors have not been changed when the load-step change has been applied. In fact, considerably less $\Delta v_{C,pp}$ has been observed when testing the proposed MPVC method during no load and full load conditions. This further confirms the

capability of the proposed MPVC approach in maintaining not only balanced dc-link capacitor voltages but substantially minimized NP-V fluctuations regardless the load conditions. Furthermore, although a major load has been connected at t = 0.304 s, $v_{o,abc}$ has not been affected when either of the control methods are tested as shown in Figure 4.18 which shows the robustness of MPVC against parameter uncertainties in general. Moreover, similar dynamic response for $i_{load,abc}$ has been observed when the conventional and proposed MPVC techniques are implemented as depicted in Figure 4.19. The three-phase peak load current, $i_{load,abc}$, has increased from zero to nearly 400 A within a few microseconds. This sudden load current increase demonstrates the fast-dynamic response of MPVC. Finally, the power generated by the T-type VSC, P_{load}, when using the proposed MPVC approach has shown slightly less ripple compared to that when using the traditional MPVC technique as depicted in Figure 4.20.

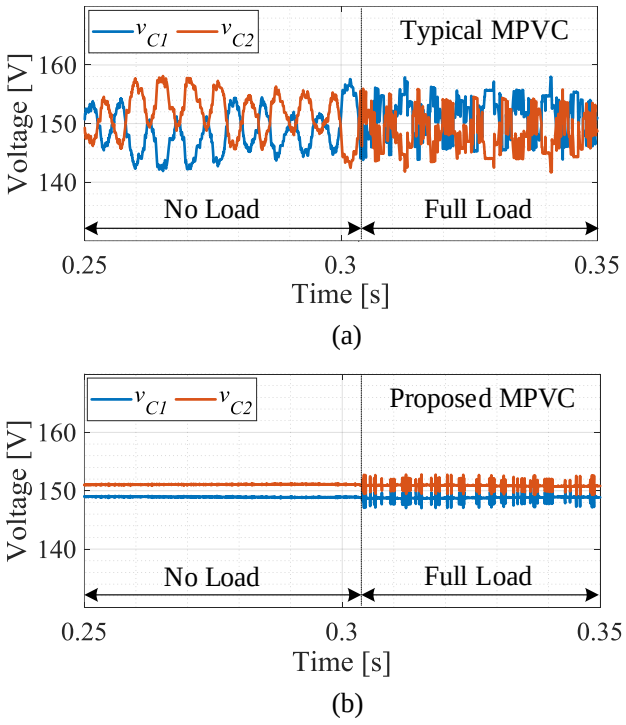


Figure 4.17: Dc-link voltages during a load-step change using (a) typical MPVC (b) proposed MPVC.

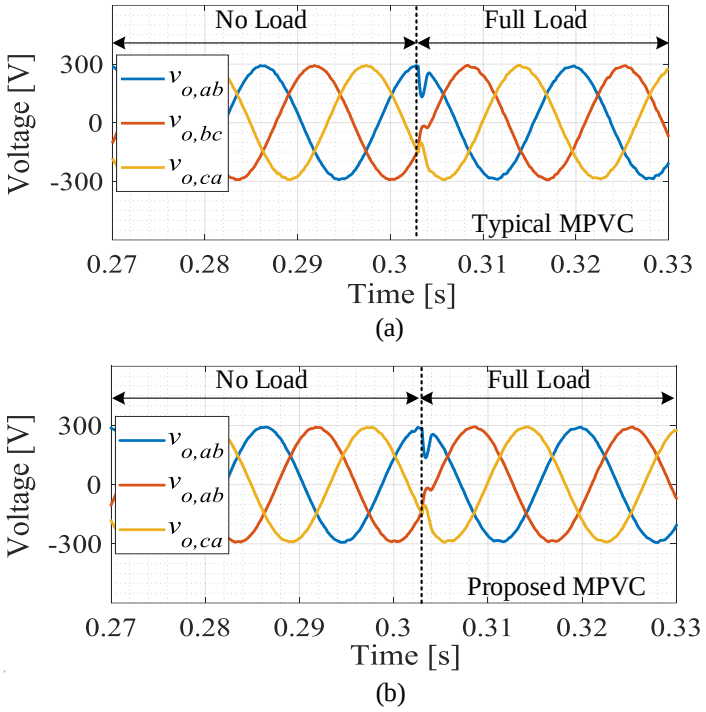


Figure 4.18: Load voltage during a load-step change using (a) typical MPVC (b) proposed MPVC.

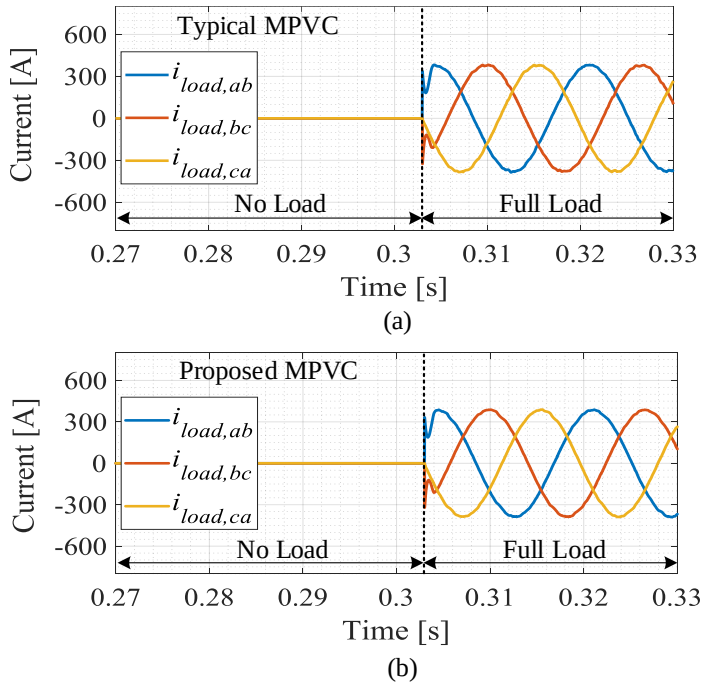


Figure 4.19: Load currents during a load-step change using (a) typical MPVC (b) proposed MPVC.

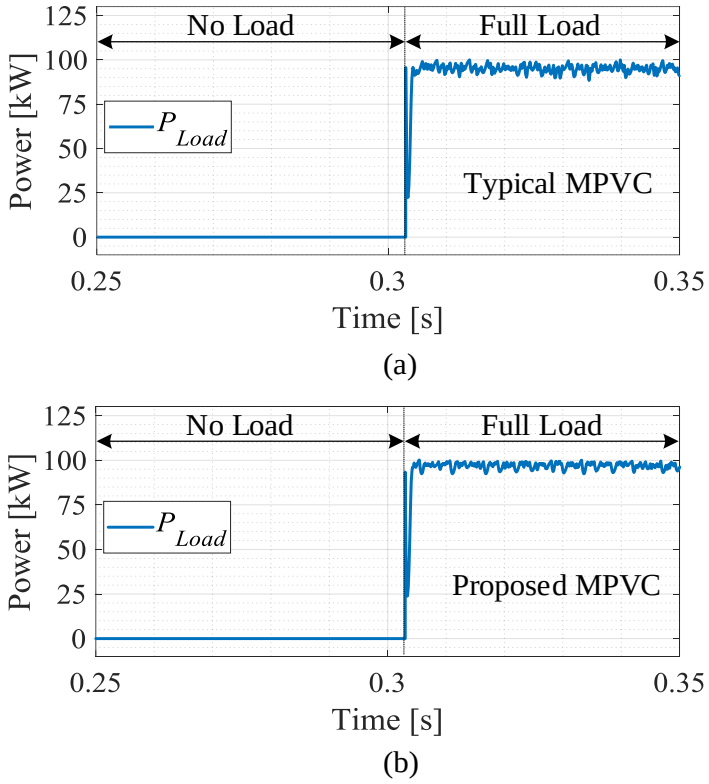


Figure 4.20: Injected power during a load-step change using (a) typical MPVC (b) proposed MPVC.

- ***Dynamic-Response Analysis During a Reference-Step Change***

The dynamic response of the conventional MPVC method as well as the proposed MPVC one has been obtained and compared in Figures 4.21(a) and 4.21(b), respectively, when a reference-step change is applied. Both control methods have presented identical dynamic response when the L-to-N voltage reference, v_{an}^{*}, has been changed from 100 V to nearly 170 V at t = 0.304 s. Figure 4.21(a) shows that the actual L-to-N voltage, v_{an}, has tracked v_{an}^{*} in 1 μs when the classical MPVC method is used. Similarly, using the proposed MPVC method has resulted in exactly the same voltage reference tracking time as v_{an} perfectly tracked its reference at t = 0.305 s. This observation validates that the proposed MPVC method can attain the fast-dynamic response of the traditional MPVC one.

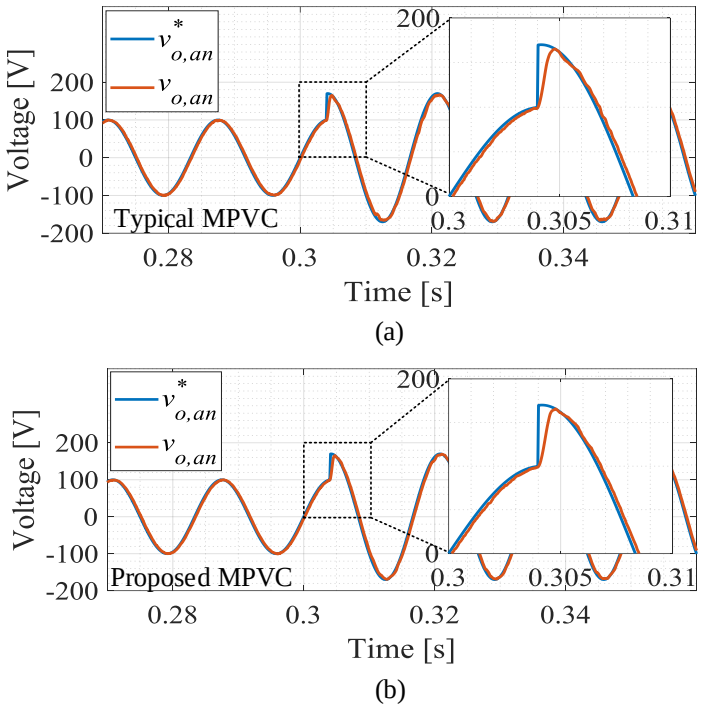


Figure 4.21: Voltage tracking during a reference-step change using (a) typical MPVC (b) proposed MPVC.

- ***Parameter-Sensitivity Analysis***

The simulation results, shown in Figures 4.22 and 4.23, are provided to further demonstrate the stability of the MPVC approach in general. The parameter-sensitivity test has been applied when ± 20 % and ± 40 % error, i.e., ΔL, is introduced to the inductor actual value, i.e., L_f. The **blue** stars in each of the figures below show all possible 27 voltage vectors to be evaluated by the controller in the predictive equation with exact *LC*-filter inductance value, L_f. The **green** stars represent all the possible 27 voltage vectors to be evaluated by the controller when ± 20 % and ± 40 % error has been introduced to the inductor value. The **black** stars which represent the error between using MPVC with exact inductance value and using MPVC with ± 20 % and ± 40 % error in the inductance value, are determined by subtracting the **green** stars from the **blue** ones. From both figures, it can be seen that having a ± 20 % error in the inductor value has resulted in less than 2.0 % voltage tracking error. Additionally, increasing the error in the inductor value to ± 40

% increases the voltage tracking error to around 5.0 %. These tests can demonstrate the robustness of the MPVC strategy against parameter uncertainty. Finally, Table 4.5 summarizes the results of the voltage reference tracking error when ΔL is 0 %, ± 20 % and ± 40 %.

Table 4.5
Load Voltage Reference Tracking Error Considering Different *LC*-Filter Inductor Values

Control Method	ΔL				
	−40 %	−20 %	0 %	+20 %	+40 %
MPVC Method	5.29 %	1.76 %	0.0 %	1.18 %	2.35 %

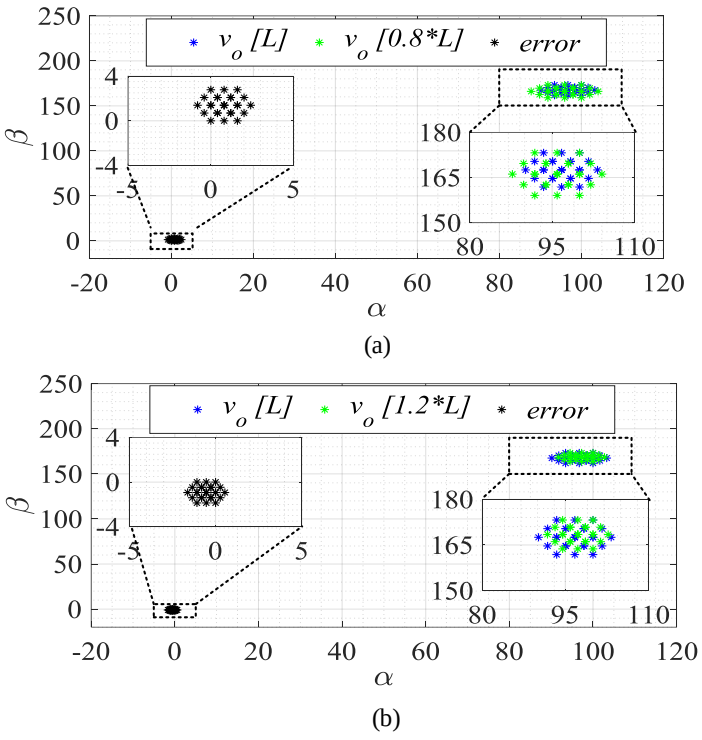
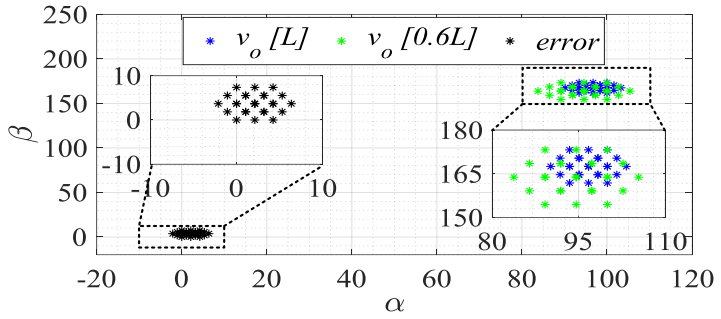
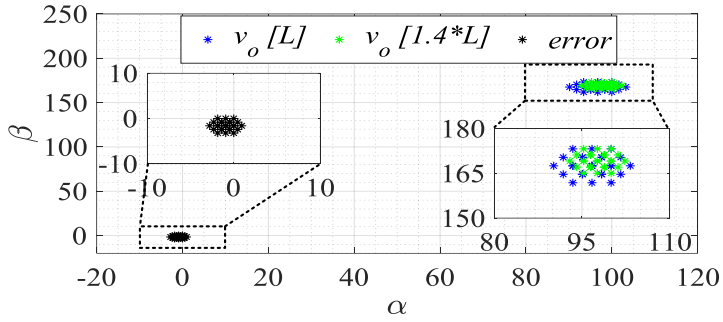


Figure 4.22: Load voltage tracking considering ΔL = ± 20 % using (a) typical MPVC (b) proposed MPVC.



(a)



(b)

Figure 4.23: Load voltage tracking considering ΔL = ± 40 % using (a) typical MPVC (b) proposed MPVC.

- ***Switching and Conduction Loss Analysis***

Based on data provided in the data sheet of CREE CAS325M12HM2 SiC power module [157], the switching and conduction power losses for the 3-L T-type VSC are simulated, analyzed and presented in this chapter. The converter overall efficiency has been calculated for both control techniques.

Since the proposed MPVC method increases the equivalent switching frequency of the T-type VSC, it is critical to evaluate the power losses and ensure the T-type VSC efficiency is not severely affected. In this work, by using the aforementioned data sheet of CREE CAS325M12HM2 SiC power module, the average switching frequency, i.e., f_{sw}, switching power loss, P_{sw}, conduction power loss, P_{cond}, and the T-type VSC three-phase switching and conduction power losses, P_{loss}, are simulated and presented in Figures 4.24 to 4.27. The power loss analysis model, presented in

[156] and was described in Chapter 3, is performed for the switch power positions S_{a1} and S_{a2}. Since the other two power switches of phase leg *a* are complementary, they should have similar results to the main power switches. As shown in Figure 4.24, the f_{sw} of both power switch positions have increased around three times when using the proposed MPVC approach compared to that of the typical MPVC technique. As a result, the P_{sw} has also tripled as shown in Figure 4.25. On the other hand, as presented in Figure 4.26, the P_{cond} of both switch positions, which are by far dominating, are particularly close to each other when both control methods are tested. Finally, shown in Figure 4.27 is the P_{loss} of the typical and proposed MPVC methods. As shown in Figure 4.27, although the f_{sw} has noticeably increased due to the use of the VSVs, the total power loss of the T-type VSC has increased only 35 W. Considering the converter power is rated at 100 kW, using the VSVs reduces the efficiency by only 0.035 % compared to the typical MPVC approach. Table 4.6 summarizes the three-phase switching power loss, three-phase conduction power loss and the three-phase T-type VSC loss. The VSC overall efficiency using both control strategies are calculated and depicted in Table 4.6.

Table 4.6
3-L T-type VSC Power Loss and Efficiency Analysis

Control Method	Single-Phase Switching Loss	Single-Phase Conduction Loss	Three-Phase Converter Loss	Converter Efficiency
Conventional MPVC	4 W	280 W	870 W	99.13 %
Proposed MPVC	11.5 W	288 W	905 W	99.10 %

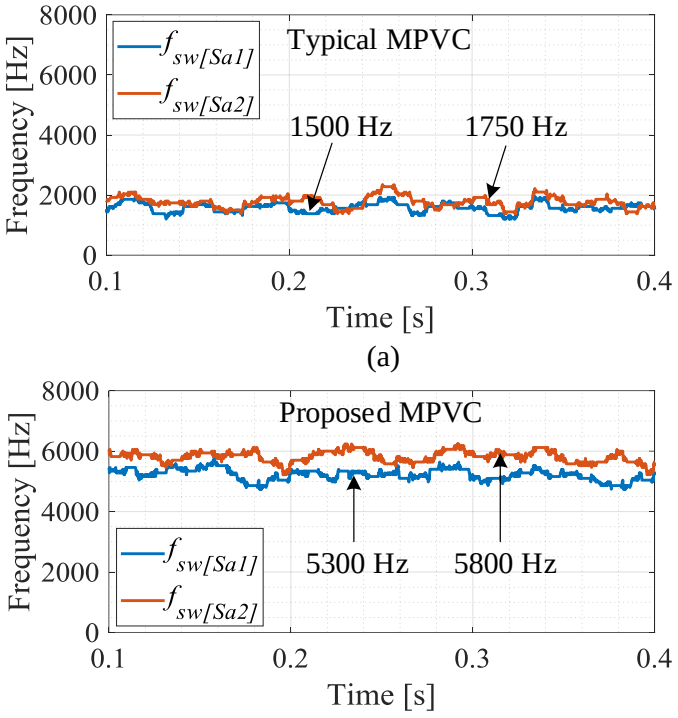


Figure 4.24: Switching frequencies of S_{a1} and S_{a2} using (b) typical MPVC (b) proposed MPVC.

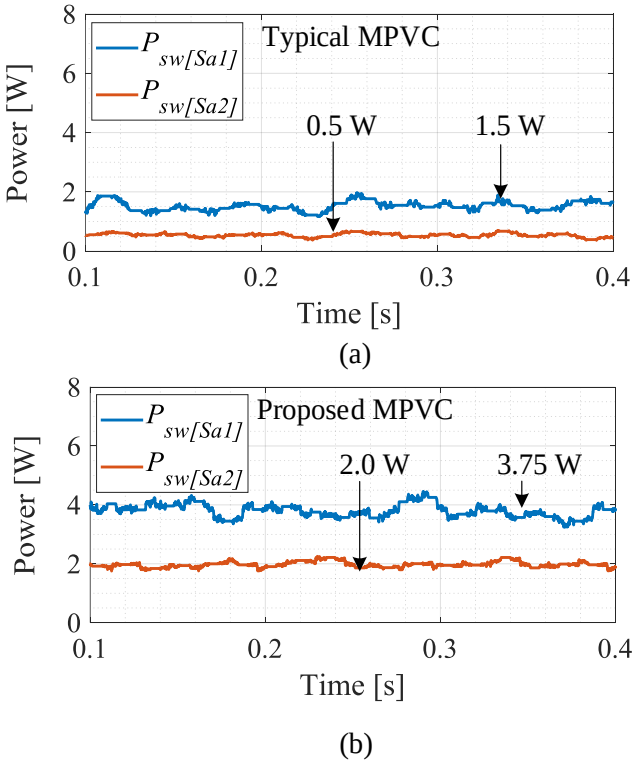


Figure 4.25: Switching loss of S_{a1} and S_{a2} using (a) typical MPVC (b) proposed MPVC.

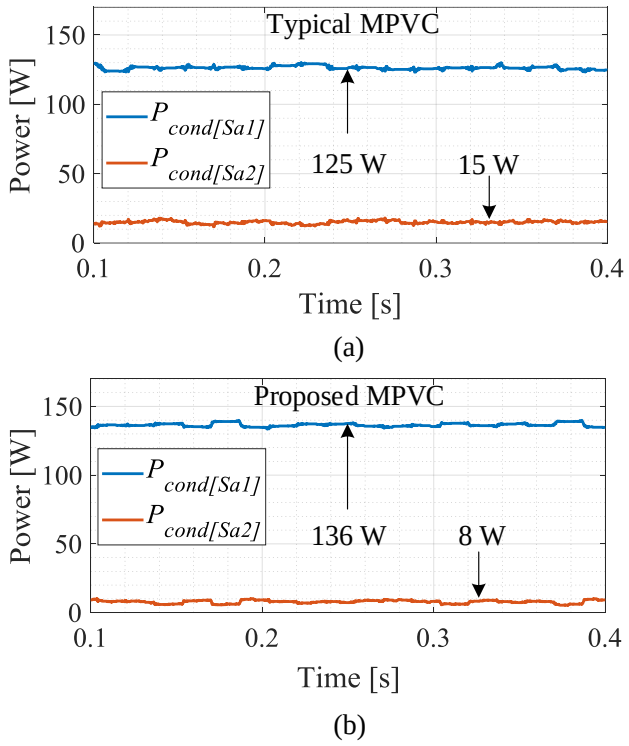


Figure 4.26: Conduction loss of S_{a1} and S_{a2} using (a) typical MPVC (b) proposed MPVC.

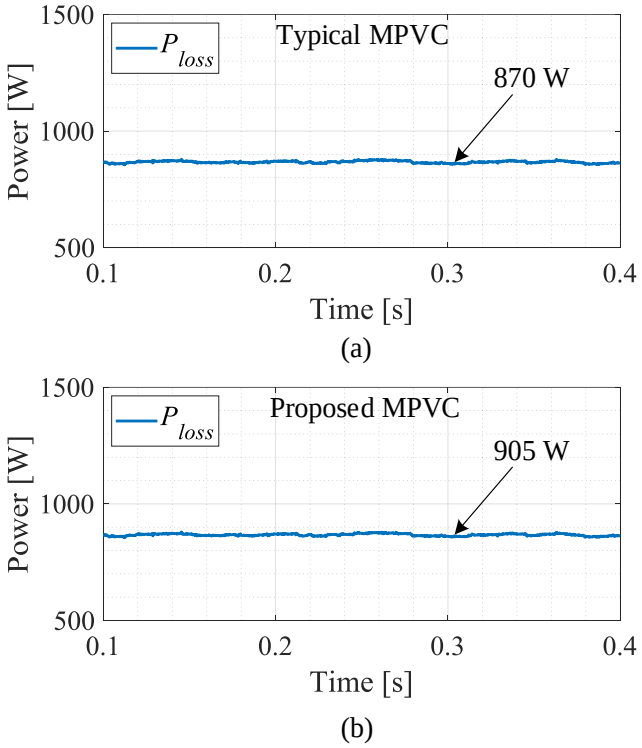


Figure 4.27: Three-phase switching and conduction losses using (a) typical MPVC (b) proposed MPVC.

4.5 Practical Implementation for Various MPVC Methods

As mentioned previously in the introduction of this chapter, the proposed MPVC method has been validated experimentally. Therefore, this section is used to explain the practical aspects of the performed tests in detail. After describing the experimental test setup which is used in this work, comprehensive experimental results are presented to verify the simulation studies.

4.5.1 Experimental Test Setup

In the work presented in this chapter, an experimental test setup was designed and built to validate and compare the performance of the proposed MPVC method with that of the typical one. The full picture of the experimental test setup is demonstrated in Figure 4.28. As shown in Figure 4.28, the main components of this test setup are listed as follows

- DC power supply;
- Two dc-link capacitors;
- Three-phase 3-L T-type converter;
- Three-phase *LC* filter;
- Three-phase resistive load;
- dSPACE MicroLabBox 1202.

In addition to the previous components, two sensor boards have been designed such that different feedback signals are obtained from the hardware setup and used in the controller. Three gate driver boards have also been structured in the lab to run the 12 power switching devices of the 3-L T-Type converter. The 3-L T-type VSC was also designed in the lab using discrete SiC MOSFETs from CREE (C2M0160120D) [157]. Finally, the control algorithms were implemented

using dSPACE MircroLabBox 1202. The parameters of the aforementioned components are listed in Table 4.7.

Table 4.7
Investigated System Experimental Parameters

Parameter	Description	Value
V_{dc}	ESS voltage	300 V
C_1 *and* C_2	DC-link capacitance	60 μF
L_f	Filter inductance	2.4 *m*H
C_f	Filter capacitance	15 μF
R_L	Load resistance	50 Ω
v_o	Load voltage (rms)	120 V
f	Nominal frequency	60 Hz
T_s	Controller sampling time	50 μs

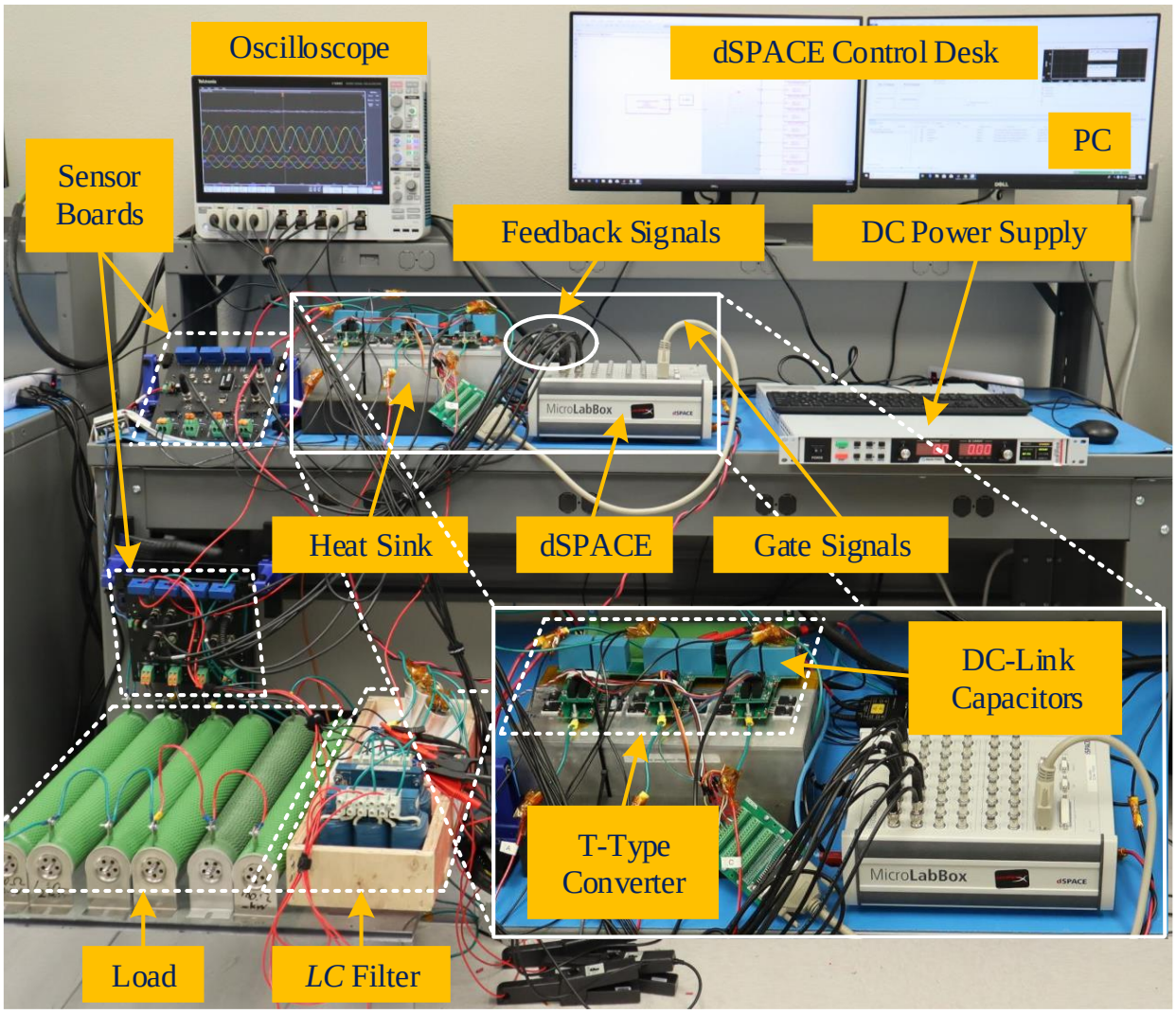


Figure 4.28: Experimental hardware test setup "photo by author".

4.5.2 Experimental Studies

Different tests have been carried out experimentally to demonstrate the superiority of the proposed MPVC technique over the traditional one. These tests include, 1) the steady-state operation which is used to compare the NP-V oscillations and the load voltage quality and reference tracking; 2) the dynamic response studies considering the load and the reference variations are demonstrated as well; 3) the parameter sensitivity test has also been applied to analyze the stability of different controllers; 4) finally, the typical and proposed controller's

execution times, T_{MPC}, have also been calculated and discussed in this section. The experimental observations have been summarized in Table 4.8 and Table 4.9.

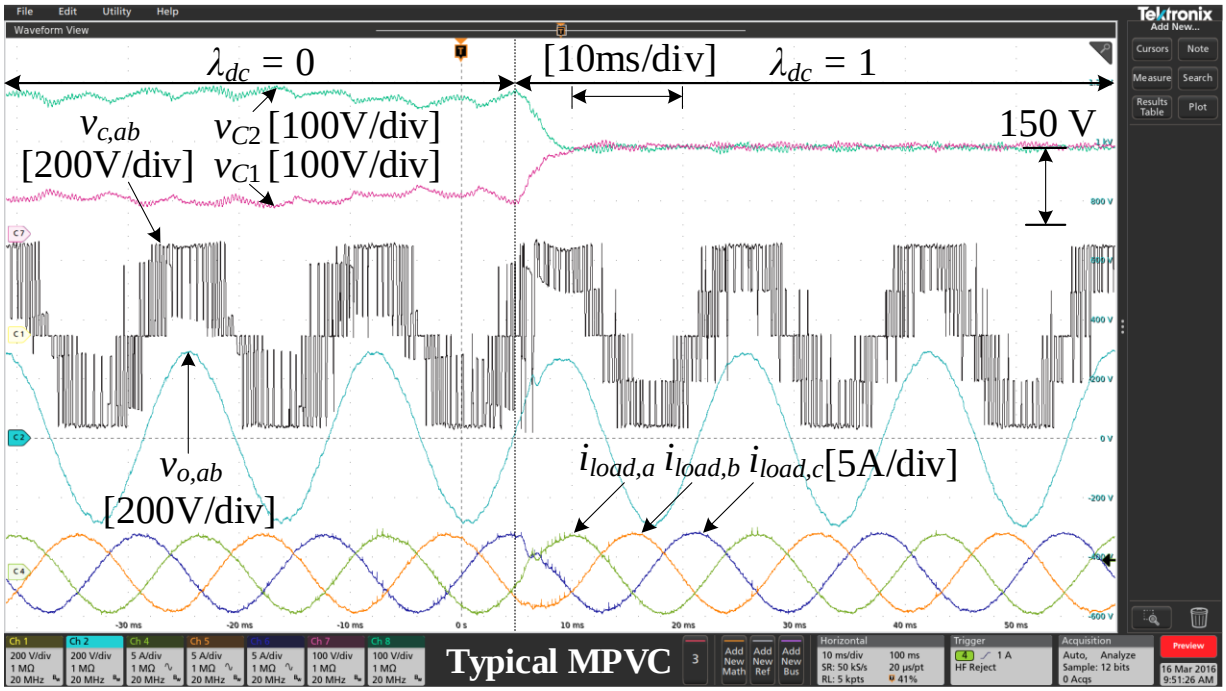


Figure 4.29: Typical MPVC experimental results during a weighting factor step change.

- ***The Impact of Weighting Factor Selection***

As shown in Figure 4.29, setting the value of the weighting factor, λ_{dc}, to zero causes a major divergence for the dc-link capacitor voltages. As soon as the value of λ_{dc} has been changed to one which has been determined to be the compromised value in the experiment, the voltages across the dc-link capacitors have been quickly recovered and equally shared the voltage of the dc-voltage source which is 300 V, between them. Then, they have started oscillating around their reference, i.e., 150 V. Therefore, in a traditional MPVC for a 3-L VSC topology, it is essential to add another term, related to the regulation of NP-V fluctuations, in the cost function, g expressed in (4.4), and select a proper value for λ_{dc} in order to achieve a well-regulated NP-V. Additionally, as shown in Figure 4.29, having an unbalanced dc-link capacitor voltages can impact the quality of the L-to-L

peak voltage generated by the T-type VSC, $v_{c,ab}$. This also results in a deterioration in the quality of the primary controlled objective of this work, i.e., load voltage $v_{o,abc}$, and accordingly affecting the quality of the load current, i.e., $i_{load,abc}$, presented in Figure 4.29. The L-to-L load voltage, $v_{o,ab}$, presented in Figure 4.29 has shown 0.30 % improvement in the THD_v once the voltages across the two dc-link capacitors have converged to their own reference which is 150 V.

- ***Steady-State Analysis***

Figures 4.30 and 4.31 show the steady-state results of the typical and proposed MPVC techniques, respectively. These results include the dc-link capacitor voltages, v_{C1} and v_{C2}, the converter output L-to-L voltage, $v_{c,ab}$, the *LC*-filter capacitor L-to-L voltages, $v_{o,ab}$ and $v_{o,bc}$, and the three-phase load current, $i_{load,abc}$. In these results, v_{C1} and v_{C2} of the proposed MPVC approach have shown less $\Delta v_{C,pp}$ across each dc-link capacitor. Compared to the typical MPVC strategy, where $\Delta v_{C,pp}$ = 20 V, the MPVC using the VSVs concept has $\Delta v_{C,pp}$ = 12 V. Additionally, the quality of v_o has been evaluated and compared as presented in Figure 4.32. While v_o using the traditional MPVC method has THD_v = 2.76 %, the proposed MPVC one has reduced the THD_v to 2.34 %. The voltage reference tracking has also been tested and compared using the typical and proposed MPVC methods. Considering the reference value of the load voltage to be 293.9 V, the traditional MPVC approach has achieved 286.8 V during the steady-state condition while the proposed one has accomplished 289.1 V. This means the steady-state error, ε_v, has been reduced from 2.42 % to 1.63 % as a result of using the VSVs concept. The THD_v as well as the voltage reference tracking accuracy of the load voltage during the steady-state operation are presented in Table 4.8 and Table 4.9, respectively.

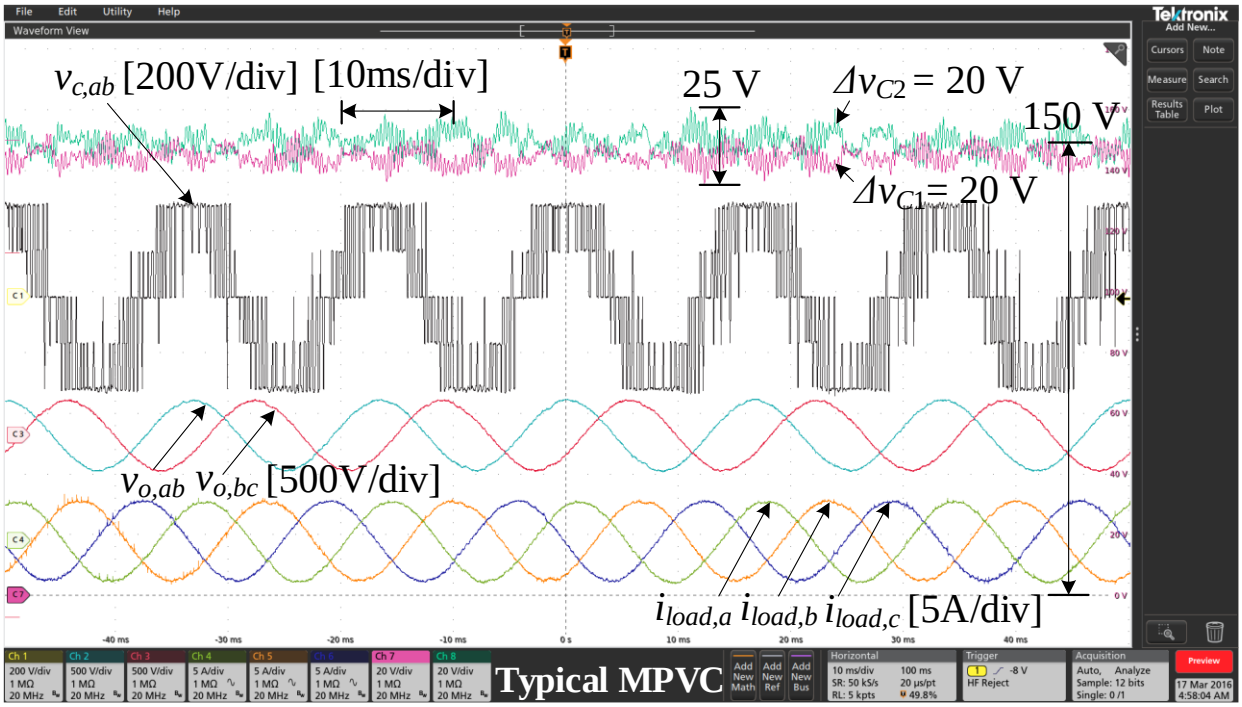


Figure 4.30: Typical MPVC experimental results during steady-state conditions.

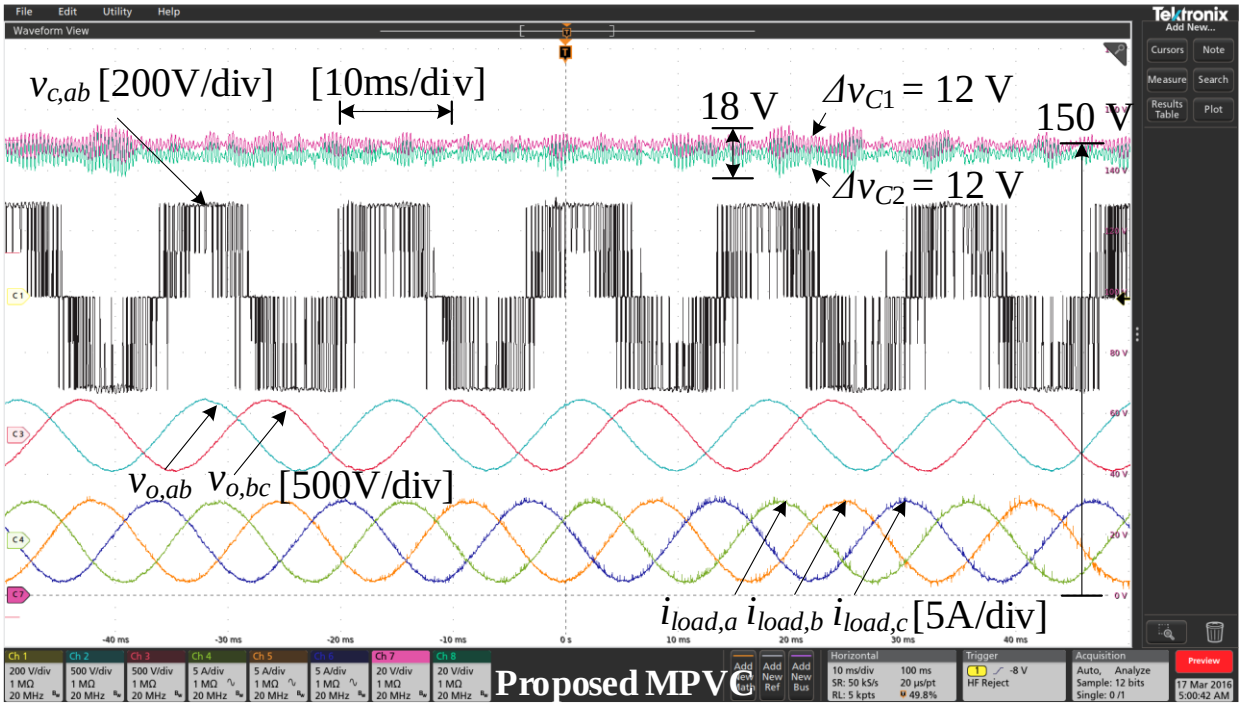


Figure 4.31: Proposed MPVC experimental results during steady-state conditions.

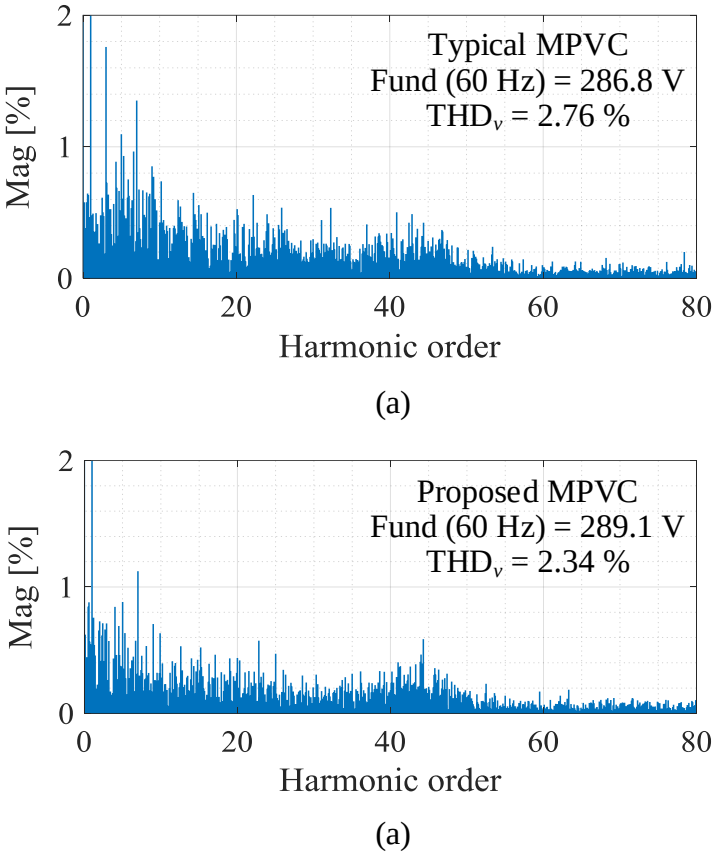


Figure 4.32: Experimental results of load voltage spectra using (a) typical MPVC (b) proposed MPVC.

- ***Dynamic Response Analysis***

In this section, the dynamic response of both MPVC strategies have been analyzed considering a load-step change as well as a reference-step change. The results of the typical and proposed MPVC techniques are displayed in Figures 4.33 to 4.36.

To start with, the results of the typical and proposed MPVC schemes when switching from no load to full load, are shown in Figures 4.33 and 4.34, respectively. Connecting the full load has caused an obvious dc-link voltage dip, but v_{C1} and v_{C2} have remained balanced and returned to their reference, i.e., 150 V, in less than 8 *m*s as shown in Figures 4.33 and 4.34. Figure 4.33 also shows $v_{o,ab}$ and $v_{o,bc}$ have not been affected due to the load transient. Similar to the traditional

MPVC strategy, Figure 4.34 presents that v_{C1} and v_{C2} have remained balanced regardless of the load step change, and they have recovered from the dc-bus voltage dip in less than 8 *m*s. Moreover, when both control techniques are tested, neither the load step change nor the dc-link voltage dip have affected the output voltage tracking, which further validates the robustness of the proposed MPVC method against the unpredicted load variations.

In addition, considering the fast-dynamic response as one of the most important advantages of MPC, it is essential to ensure that the use of the VSVs does not affect such superiority. Thus, Figures 4.35 and 4.36 show the results of the traditional and presented MPVC strategies, respectively, when a step change in the L-to-N voltage reference, v_{an}^{*}, is applied. In this test, the peak value of v_{an}^{*} is increased from 100 V to nearly 170 V. Both control methods, the typical and proposed MPVC methods, have been evaluated when such a test is applied. Figures 4.35 and 4.36 show that both control techniques have similar dynamic response as they both required around 1 *m*s to track their references. To illustrate, by selecting the classical MPVC scheme, the actual L-to-N voltage, i.e., v_{an}, has tracked the reference v_{an}^{*} in 987 μs as depicted in Figure 4.35. Similarly, as demonstrated in Figure 4.36, if the proposed MPVC using VSVs technique is the candidate control method, v_{an} can track its reference v_{an}^{*} in 992 μs. As a result, it can be concluded that using the concept of the VSVs with MPC does not impact the fast-transient response of the MPVC since the traditional and proposed MPVC strategies can perfectly track their references in almost 1 *m*s. It is worth noting that other variables such as the dc-link capacitor voltages, converter voltage, load currents are also shown in the same results, presented in Figures 4.35 and 4.36, to demonstrate the effect of the reference-tracking test on these waveforms.

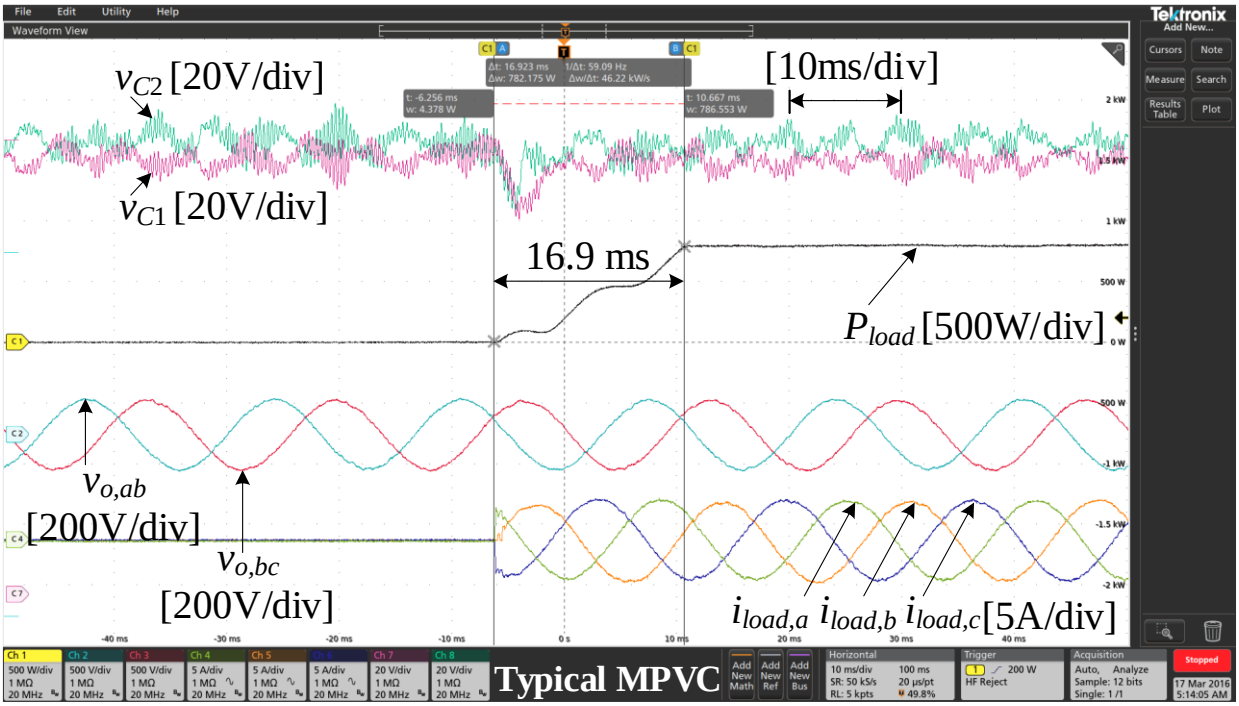


Figure 4.33: Typical MPVC experimental results during a load-step change.

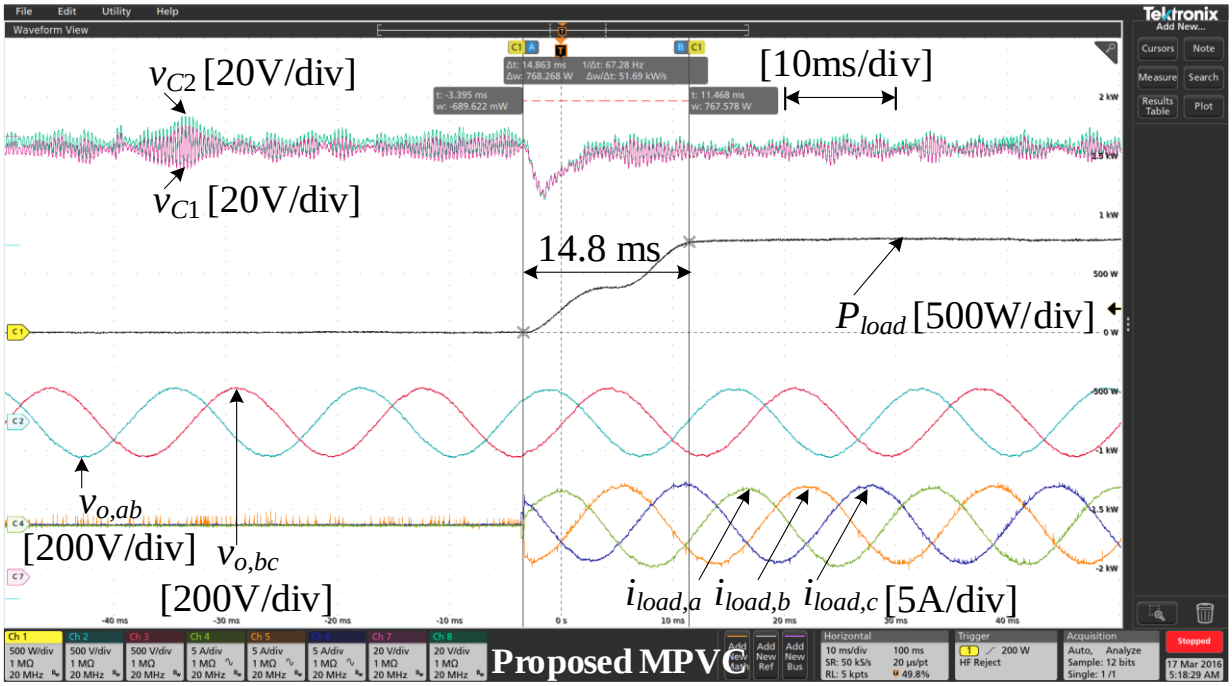


Figure 4.34: Proposed MPVC experimental results during a-load step change.

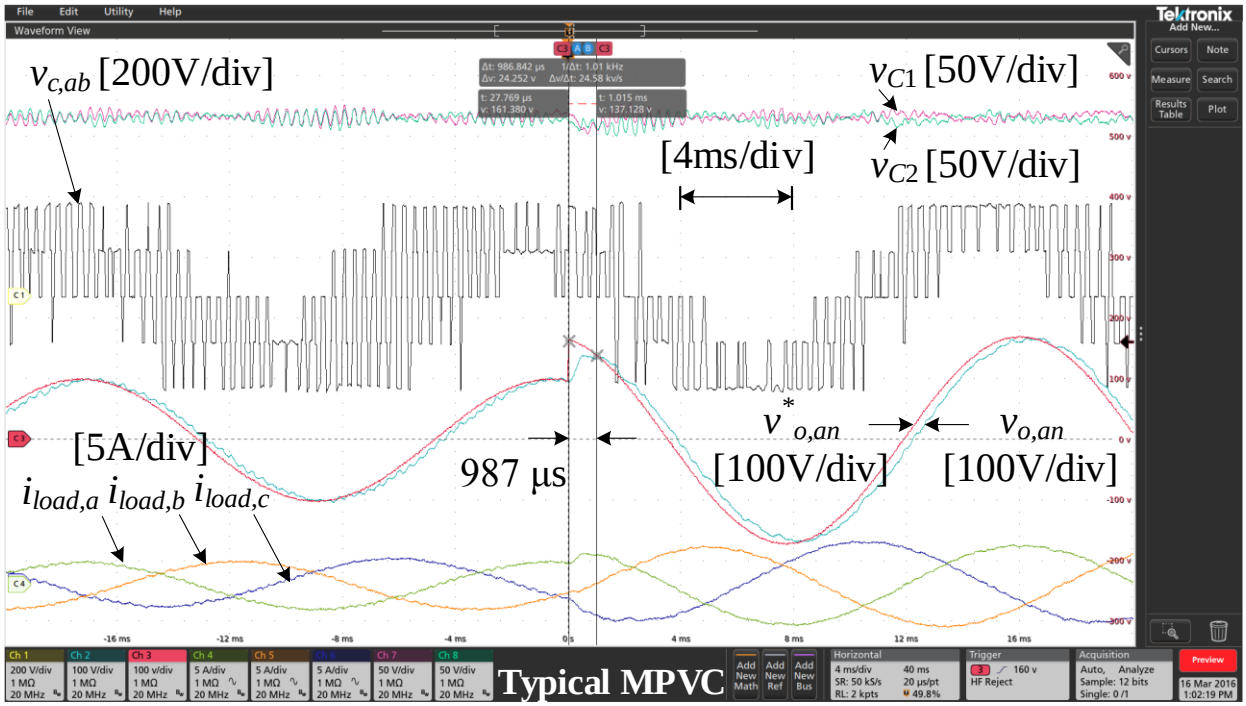


Figure 4.35: Typical MPVC experimental results during a reference-step change.

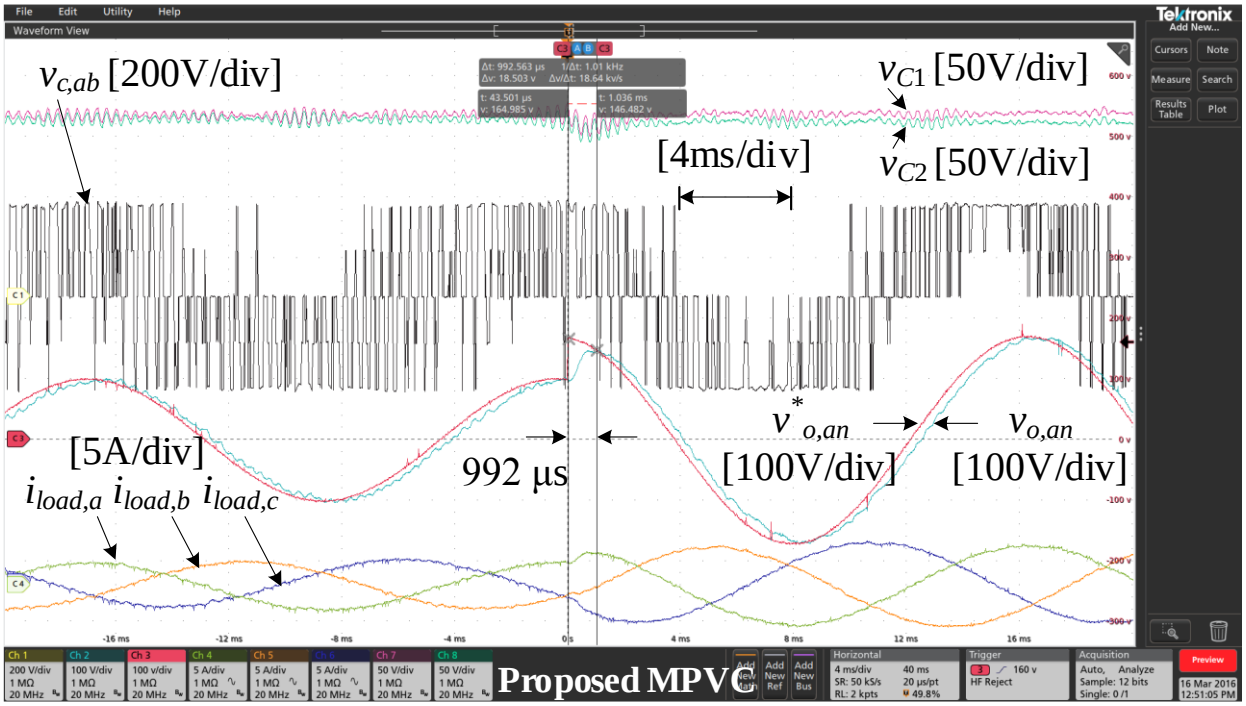


Figure 4.36: Proposed MPVC experimental results during a reference-step change.

- ***Parameters Sensitivity Analysis***

One important factor to evaluate the performance of the proposed MPVC is the controller response against parameter uncertainties. Therefore, the stability of both the typical and proposed MPVC methods has been evaluated experimentally by applying the parameter-sensitivity test. The inductor variations, ΔL, used for this test are ± 20 % and ± 60 % of the *LC*-filter inductor actual value, L_f. The inductor variations are calculated using (4.12) [150].

$$\Delta L = \frac{L - L_f}{L_f} \times 100 \tag{4.12}$$

where

L_f *LC*-filter inductor actual value, shown in Table VI;

L varied value used in the controller design.

While the results, presented in Figures 4.37 and 4.38, represent different converter output waveforms when $\Delta L = -20$ % using the conventional and proposed MPVC methods, Figures 4.39 and 4.40 show the results of the same waveforms using both control techniques considering ΔL = +20 %. Although +20 % error has been introduced in the results shown in the aforementioned Figures, the regulated NP-V fluctuations has not been affected when either of the control methods are applied. The increase in the THD_v of v_o is also less than 0.50 % in both cases. Similarly, having a –20 % error in L_f has not impacted the controlled NP-V oscillations of the typical and proposed MPVC strategies. Furthermore, only 0.20 % increase in the THD_v of v_o has been observed when the traditional and proposed MPVC methods are tested considering the –20 % inductor value error.

Similarly, the effect of having a ±60 % error in L_f has also been investigated in this work. Figures 4.41 to 4.44 demonstrate that the classical and presented MPVC strategies have shown

robustness against the sever parameter uncertainty. Although a major difference between the value of L_f and L has been introduced, the THD_v of the load voltage has not been severely increased. To explain, while applying the classical MPVC strategy with $\Delta L = -60$ % has increased the THD_v by around 0.32 %, adopting the proposed MPVC with $\Delta L = -60$ % has led to increase the THD_v by 0.43 %. On the other hand, having $\Delta L = +60$ % has reduced the quality of v_o by nearly 0.55 % if the traditional MPVC scheme is selected. Similarly, 0.62 % increase in the THD_v has been observed if the proposed MPVC method is the control candidate. Therefore, it can be concluded that the quality of v_o has been reduced by around 60 % when $\Delta L = +60$ %. In addition, the dc-link capacitor voltages have remained balanced regardless the sever parameter uncertainty in all cases. As a result, it can be concluded that both control techniques have shown robustness against the parameter mismatch between L_f and L.

Finally, Table 4.8 summarizes the THD_v results of the load voltage, v_o, when various parameter-uncertainty tests are performed. From Table 4.8 it can be seen that the proposed MPVC algorithm can always achieve less THD_v compared to the typical MPVC approach.

Table 4.8
THD Analysis of Load Voltage Considering Different *LC*-Filter Inductor Values

Control Method	ΔL				
	−60 %	−20 %	0 %	+20 %	+60 %
Conventional MPVC	3.08 %	2.96 %	2.76 %	3.23 %	3.31 %
Proposed MPVC	2.77 %	2.56 %	2.34 %	2.84 %	2.96 %

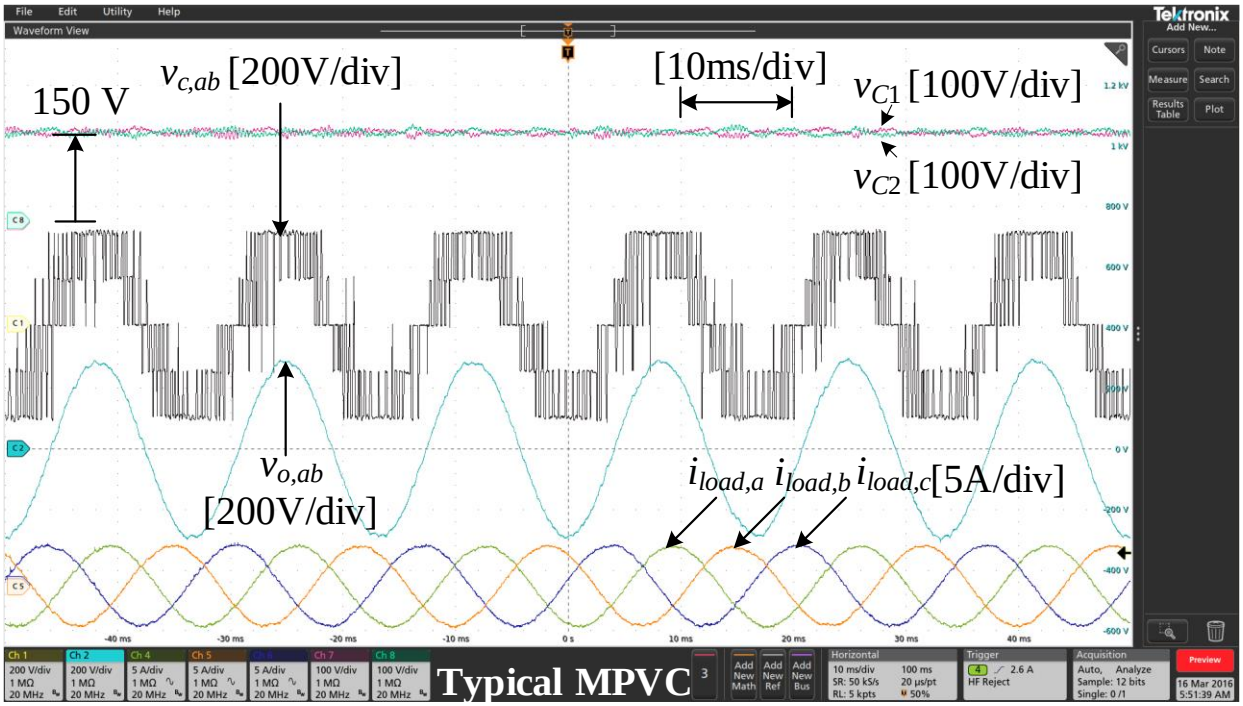


Figure 4.37: Typical MPVC experimental results with $\Delta L = -20$ %.

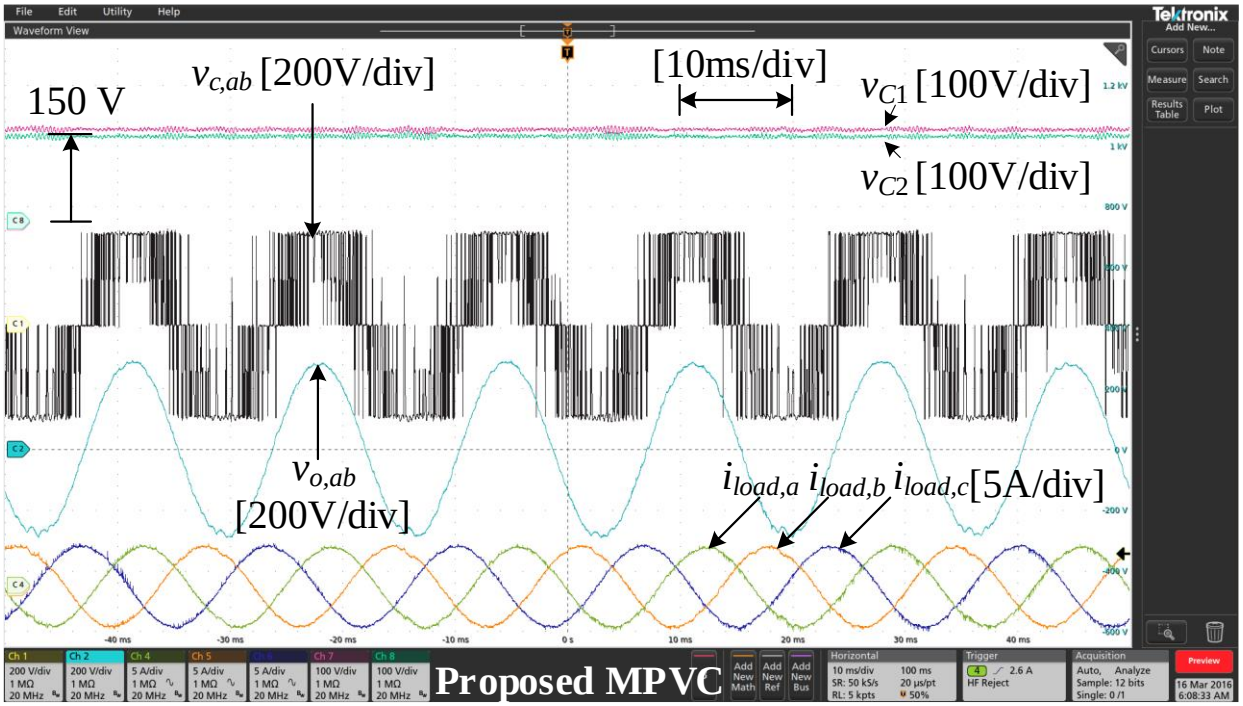


Figure 4.38: Proposed MPVC experimental results with $\Delta L = -20$ %.

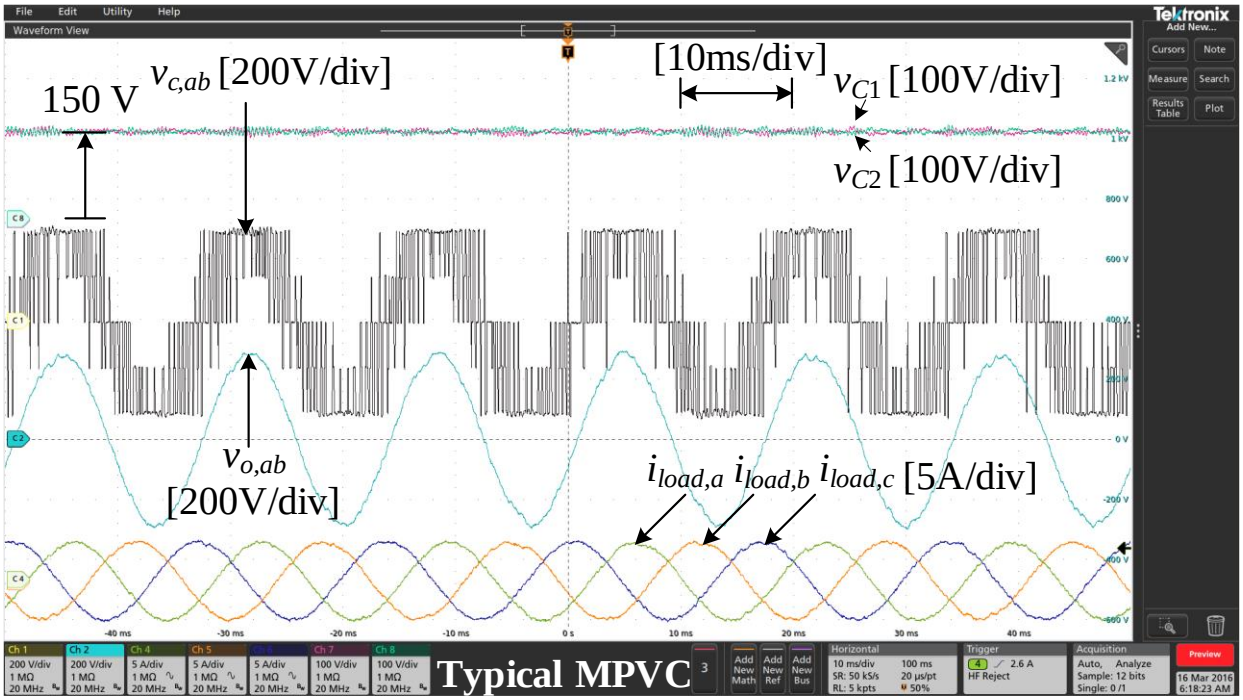


Figure 4.39: Typical MPVC experimental results with ΔL = +20 %.

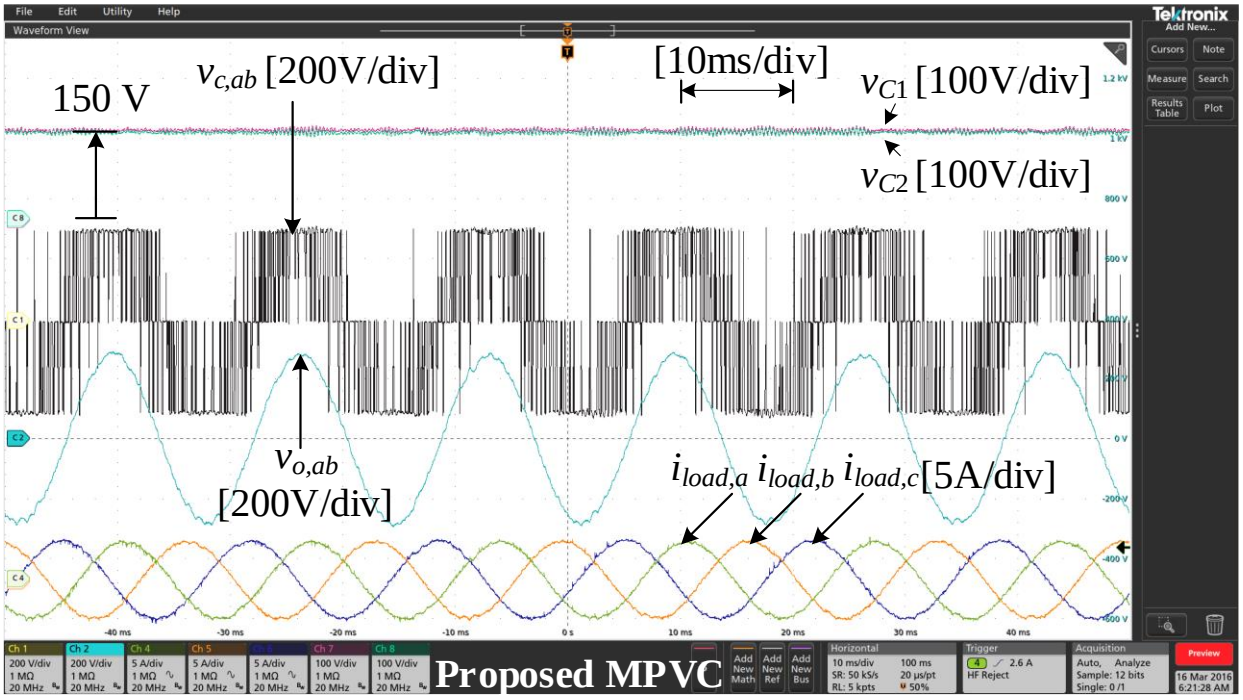


Figure 4.40: Proposed MPVC experimental results with ΔL = +20 %.

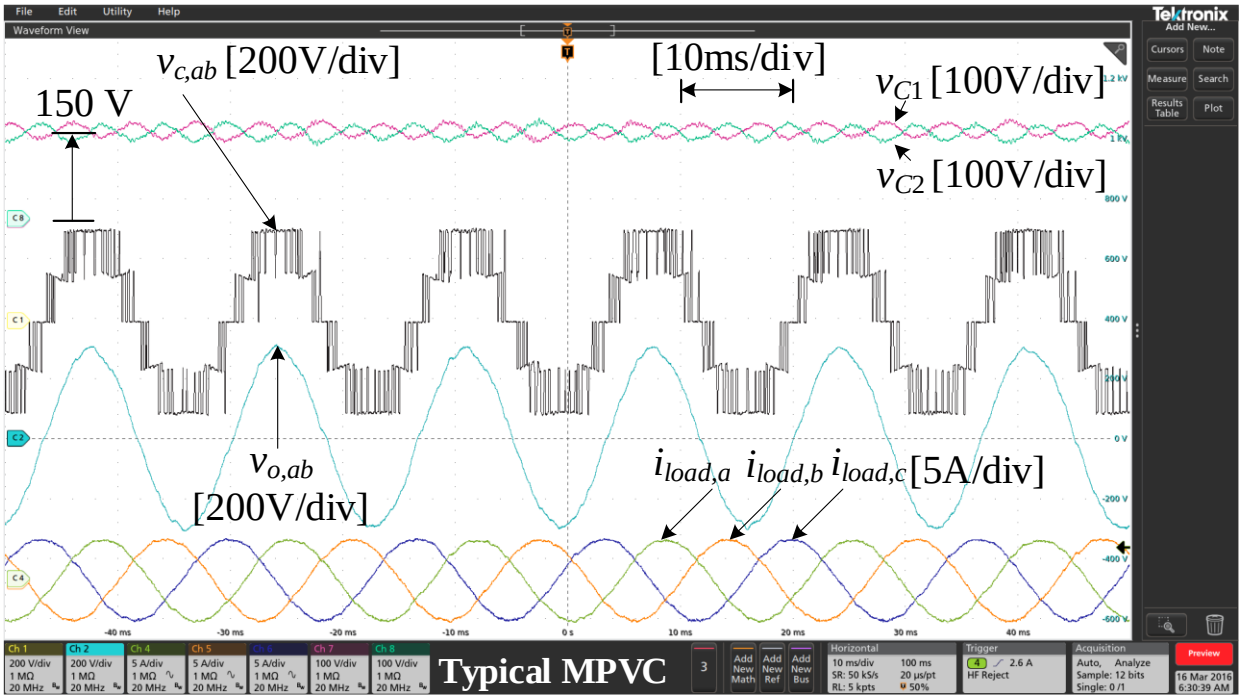


Figure 4.41: Typical MPVC experimental results with $\Delta L = -60$ %.

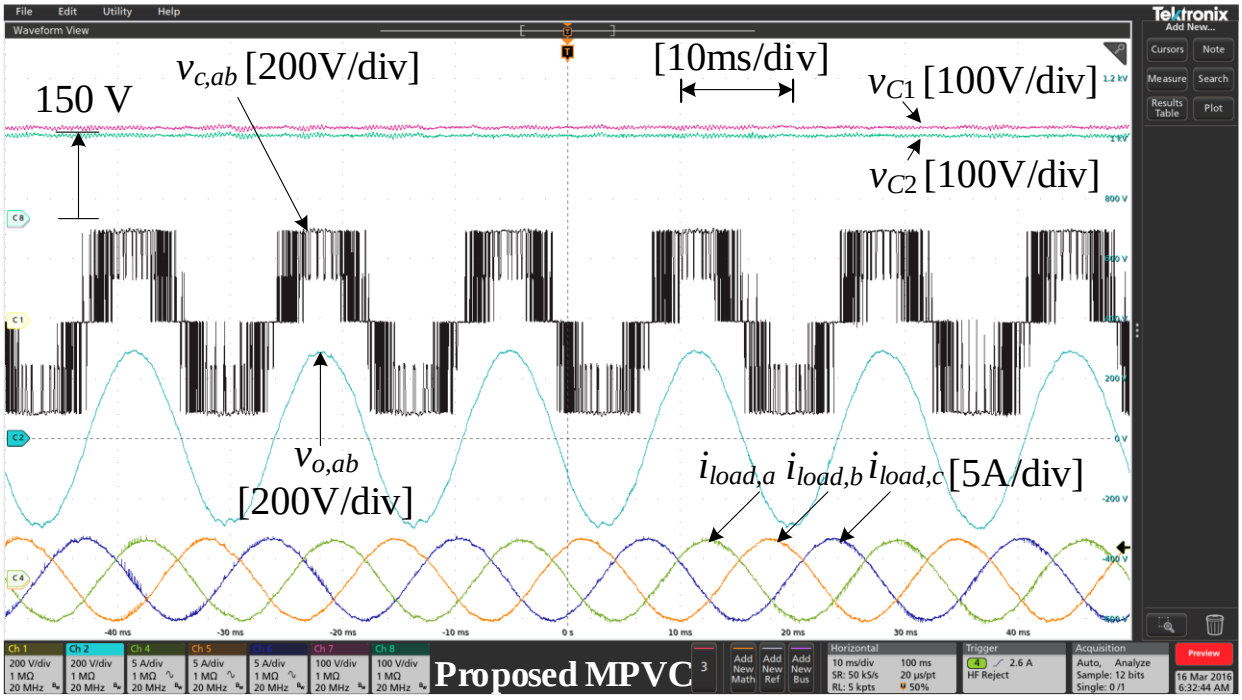


Figure 4.42: Proposed MPVC experimental results with $\Delta L = -60$ %.

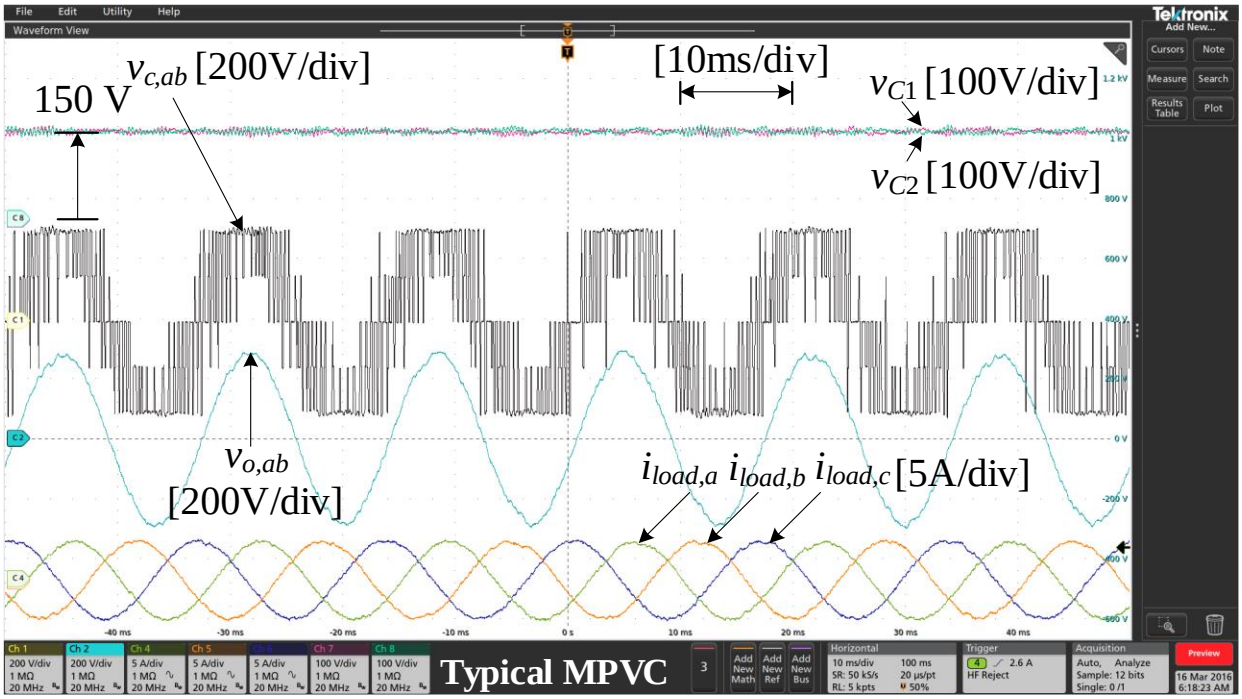


Figure 4.43: Typical MPVC experimental results with ΔL = +60 %.

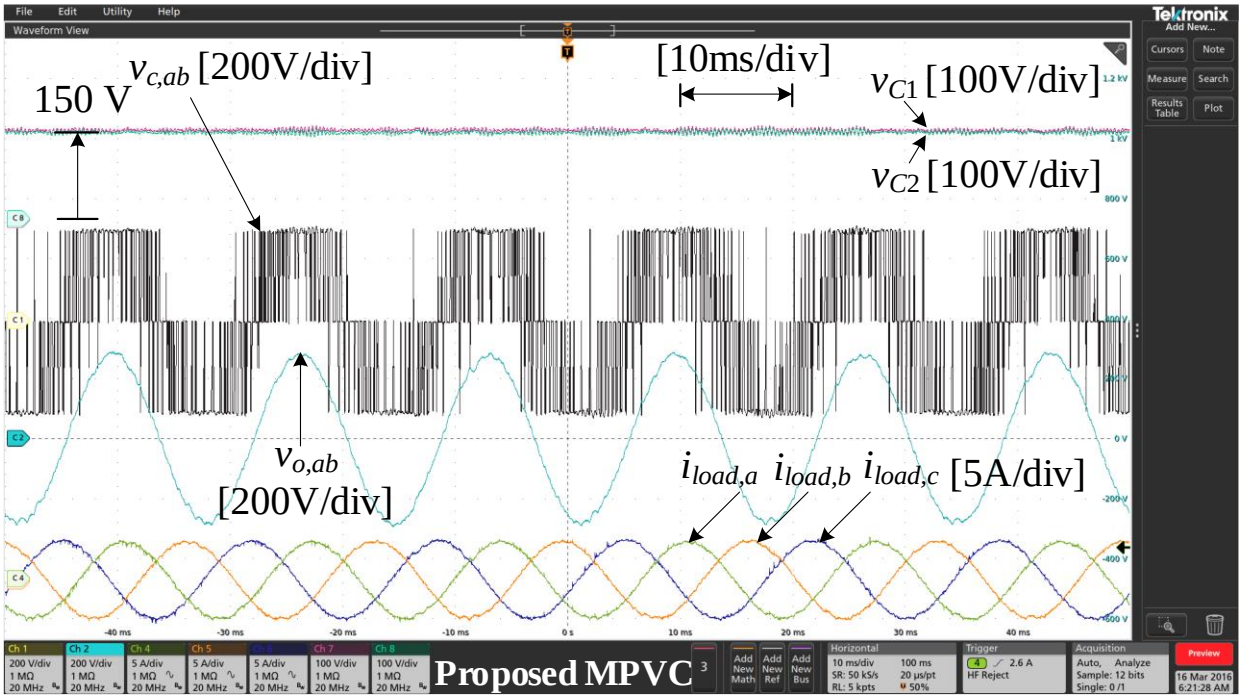


Figure 4.44: Proposed MPVC experimental results with ΔL = +60 %.

- ***Controller Execution Time Comparisons***

dSPACE MicroLabBox 1202 has been used to experimentally calculate the controller execution time, T_{MPC}, of the typical and proposed MPVC strategies to be 14.8 μs and 11.2 μs, respectively. This reduction in the calculation burden occurs mainly due to the fact that the proposed MPVC method has simpler controller algorithm as calculations related to the NP-V regulation have been eliminated from the applied presented MPVC strategy. A detailed step-by-step comparison between the typical and the proposed MPVC methods is presented in the Table 4.9 to show why the proposed MPC is more computationally efficient.

Table 4.9
Comparision of Different Control Algorithms Implementation

Typical MPVC	Proposed MPVC
Step 1: measure 10 signal feedbacks	Step 1: measure 7 signal feedbacks
Step 2: initiate cost function value, $g_{opt} = inf$	Step 2: initiate cost function value, $g_{inf} = inf$
Step 3: start a "for loop" with $i = 27$	Step 3: start a "for loop" with $i = 27$
Step 4: evaluate the following predictive equations $v_{C1}(k+2) = v_{C1}(k+1) + \frac{T_s}{C_1} i_{C1}(k+1)$ (eq. 4.1) $v_{C2}(k+2) = v_{C2}(k+1) + \frac{T_s}{C_2} i_{C2}(k+1)$ (eq. 4.2)	Step 4: None
Step 5: evaluate the following predictive equation $x(k+2) = Ax(k+1) + B_1 v_c(k+1) + B_2 i_{load}(k+1)$ (eq. 4.3)	Step 5: evaluate the following predictive equation $x(k+2) = Ax(k+1) + B_1 v_c(k+1) + B_2 i_{load}(k+1)$ (eq. 4.3)
Step 6: evaluate the following cost function $g = (v_\alpha^* - v_{o,\alpha}^p)^2 + (v_\beta^* - v_{o,\beta}^p)^2 + \lambda_{dc}(v_{C1}^p - v_{C2}^p)$ (eq. 4.4)	Step 6: evaluate the following cost function $g = (v_\alpha^* - v_{o,\alpha}^p)^2 + (v_\beta^* - v_{o,\beta}^p)^2$ (eq. 4.11)
Step 7: if $g_i < g_{opt}$ % make a comparison $g_i = g_{opt}$ % update g else if $i = 27$ exit the "for loop" % go to step 8 else go to "Step 3"	Step 7: if $g_i < g_{opt}$ % make a comparison $g_i = g_{opt}$ % update g else if $i = 27$ exit the "for loop" % go to step 8 else go to "Step 3"
Step 8: apply the switching state number "*i*"	Step 8: apply the switching state number "*i*"

4.6 Summary

Finally, Table 4.10 summarizes various results presented in this chapter, which include v_o steady-state error, ε_v, number of weighting factors to be designed, number of voltage and current sensors and the controller execution time, T_{MPC}. These results verify the superiority of the proposed MPVC technique over the traditional MPVC one.

Table 4.10
Load voltage, Number of Weighting Factors, Number of Voltage and Current Sensors, and Controller Execution Time

Control Method	Typical MPVC	Proposed MPVC
Steady-state error of v_o (ε_v) (simulation)	2.31 %	1.12 %
Steady-state error of v_o (ε_v) (experiment)	2.42 %	1.63 %
No. of weighting factors	2	1
No. of voltage sensors	5	3
No. of current sensors	5	4
Execution time (T_{MPC})	14.8 μs	11.2 μs

The bar charts depicted in Figures 4.45 to 4.49 provide various comparisons between the traditional MPVC method and the one proposed in this chapter. Considering the dc-link balancing as a major advantage of adopting the proposed MPVC scheme, the dc-link voltage ripples of both control strategies were compared and presented in Figure 4.45. The dc-link voltage ripples were reduced from 20 V, when applying the conventional MPVC approach, to only 12 V when the proposed MPVC strategy was implemented. The quality of the load voltage was also assessed. Figure 4.46 shows that the proposed MPVC algorithm reduced the THD_v of the load voltage from 2.76 % to 2.34 %. The proposed MPVC strategy not only decreased the THD_v of the load voltage,

but also improved the voltage reference tracking as displayed in Figure 4.47. While the typical MPVC technique resulted in 7.2 V voltage error when compared with the load voltage reference, the method presented in this chapter reduced the voltage error to 4.2 V. The controller execution time was also evaluated considering both control algorithms an demonstrated in Figure 4.48. The proposed MPVC algorithm required 11.2 μs to execute the proposed code whereas the classical MPVC one needed 14.8 μs to run one control iteration. Finally, the efficiency of the T-type VSC was evaluated and analyzed when either of the control schemes was selected. The results for this test are presented in Figures 4.49 and 4.50. As explained in Figure 4.49, the single-phase switching and conduction losses if the traditional MPVC method was applied were calculated to 284 W while these power losses were calculated to be around 299 W if the MPVC using the VSVs was the control candidate method. To clearly understand the effect of this slight increase in the power losses, the three-phase T-type VSC efficiency was determined considering the converter is operating at full power, i.e. 100 kW. As shown in Figure 4.50, when the proposed MPVC method was applied, the converter efficiency was calculated to 99.10 % compared to that of the conventional MPVC one which was determined to be 99.15 %. This slight and insignificant reduction in the efficiency is a drawback which results from the increased switching frequency.

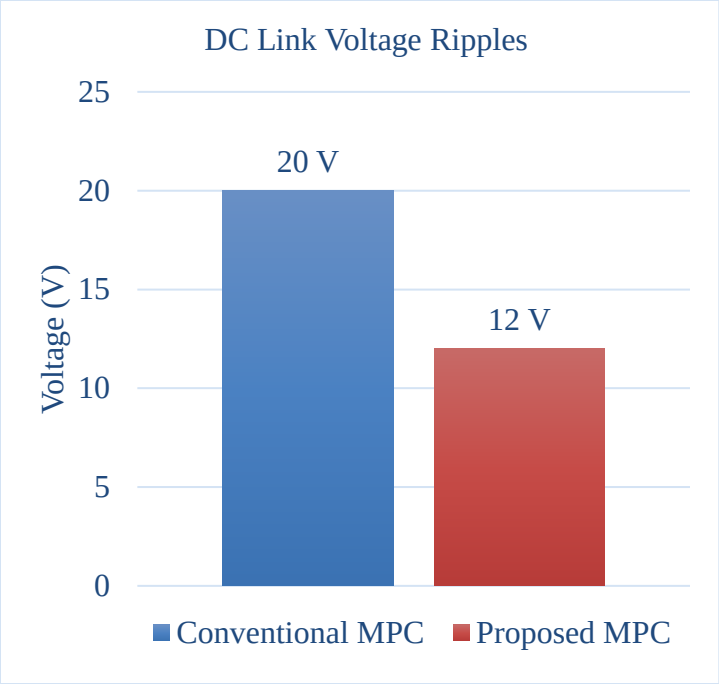


Figure 4.45: Comparison of the dc-link voltage ripples.

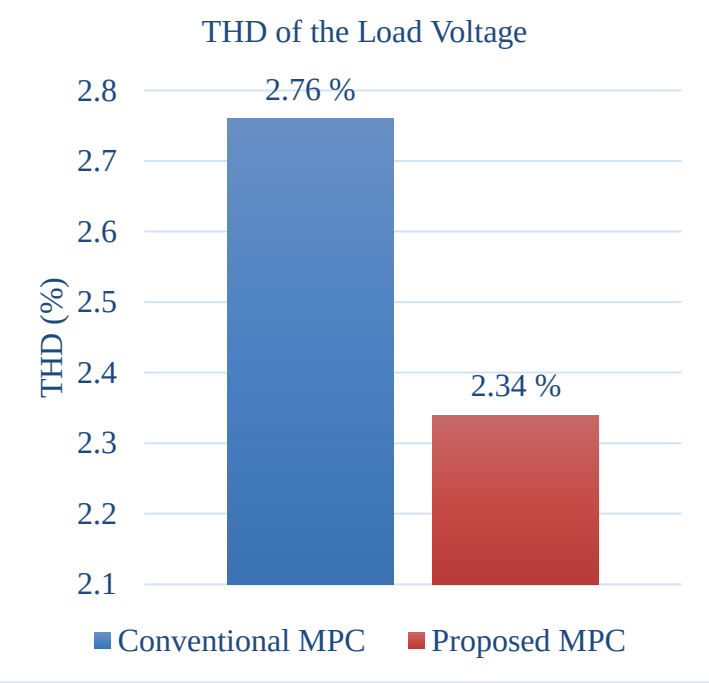


Figure 4.46: Comparison of the load voltage THD_v.

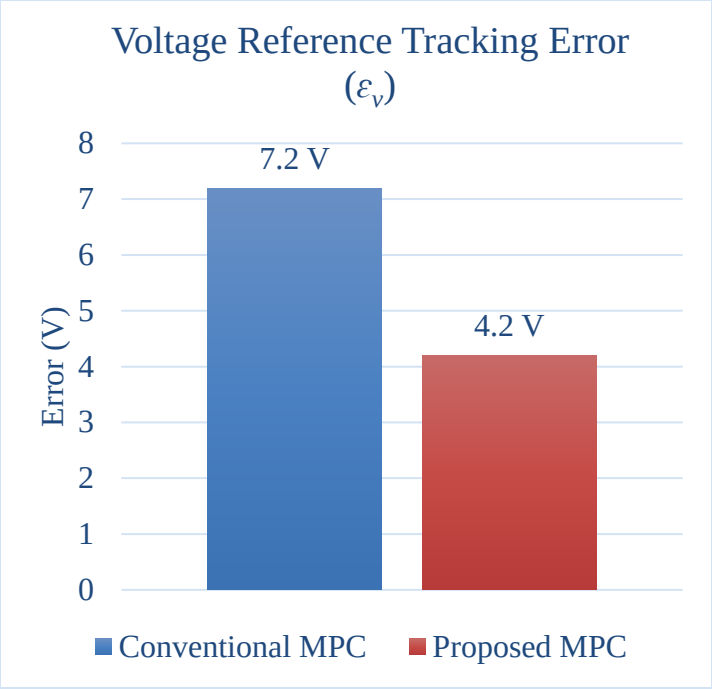


Figure 4.47: Comparison of the load voltage tracking accuracy.

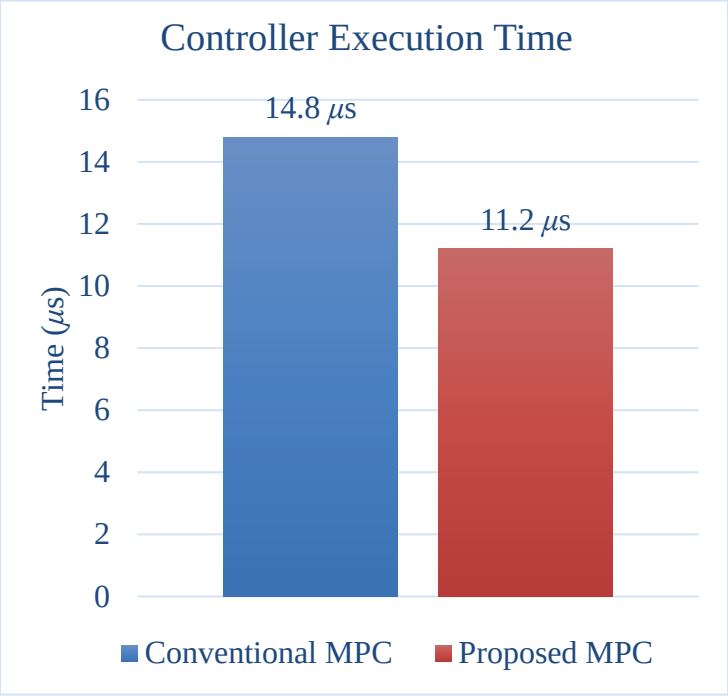


Figure 4.48: Comparison of the controller execution time.

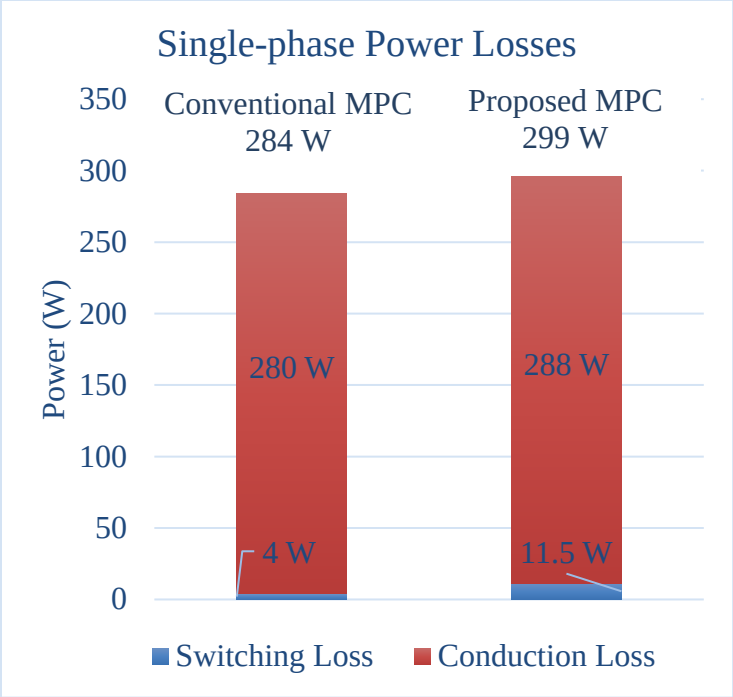


Figure 4.49: Comparison of the single-phase power losses.

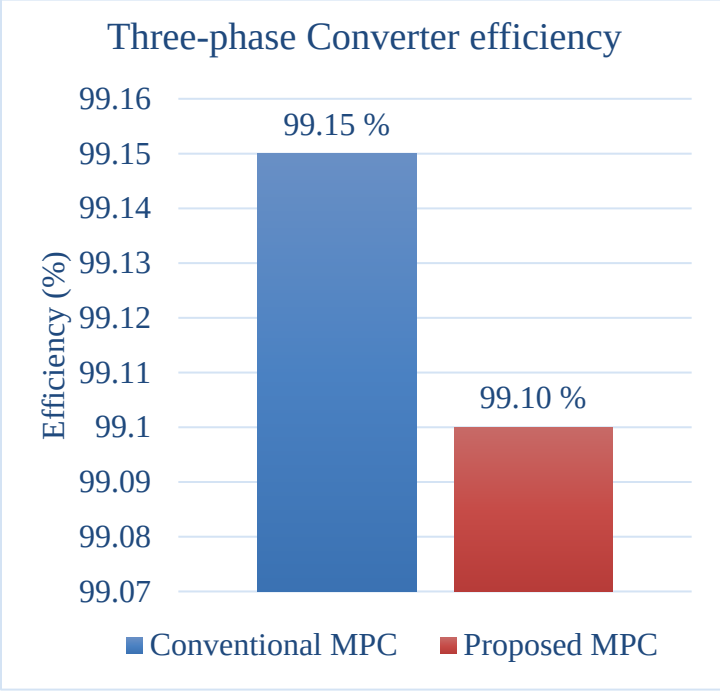


Figure 4.50: Comparison of the three-phase converter efficiency.

4.7 Concluding Remarks

By using the three-phase 3-L T-type VSC model, the dc-link model and the *LC*-filter model which were derived in Chapter 2, the implementation of the conventional MPVC scheme on a 3-L T-type VSC operating as an UPS has been presented in this chapter. The proposed MPVC using VSVs design has been explained in detail and compared with the design of the classical MPVC technique. Unlike the classical gating signals implementation of the typical MPVC method which can be performed without a modulator, a developed MPVC approach has to generate the gate signals using a modulator which has also been demonstrated in this chapter. A short comparisons for the different SV diagrams of the typical MPC, the enhanced MPC and the novel MPC, which clearly describe the influence of every voltage vector on the NP-V, were also shown in this chapter. After that, the converter switching and conduction power loss model was briefly mentioned. Comprehensive simulation studies which validate the concept of the proposed MPVC scheme, have been demonstrated in this chapter. To verify the simulations studies, the different control strategies have been tested experimentally. The various components of the hardware test setup which was used in this work were listed and described. Finally, it has been validated that compared to the traditional MPVC approach, the proposed control technique can simplify the design of such systems as the dc-link capacitor voltages are inherently balanced. As a result, the cost function can be formed considering only one objective, which eliminates the time and effort needed to select the proper weighting factors. The weighting factor elimination also improves the performance of the controller since only one target has to be controlled. Additionally, a noticeable enhancement in the converter output waveform quality has been observed as a result of the increase in the average switching frequency. Due to the inherently balanced dc-link capacitor voltages, the VSC dc-side voltage and current sensors are also avoided, which reduces the hardware cost and wiring

complexity. Furthermore, the proposed MPVC algorithm has been verified to have less computational burden compared to the typical one since the calculations used to predict the dc-link capacitors voltages are eliminated from the control algorithm.

CHAPTER 5

CONCLUSIONS, CONTRIBUTIONS AND FUTURE RESEARCH WORK

This chapter starts by revisiting the objectives of this dissertation so drawn conclusions regarding the multiple studies, contained herein, are well realized. Throughout this chapter, the accomplishments are emphasized. Finally, the dissertation concludes with recommendations for potential future research work.

5.1 Conclusions of This Dissertation

The legacy electric grid is going through substantial transformation from a passive unidirectional electric grid to a more active bidirectional electric network. Because microgrids (MGs) continue to undergo dramatic growth internationally, challenges related to the MG's reliability, stability, resiliency and sustainability continue to increase as well. Consequently, the attractions of power electronics topologies and advanced control schemes have persisted in recent research.

On the one hand, the inherent hard nonlinearities, model uncertainties, narrow operation range, complex design, slow-dynamic response, etc. together render linear control strategies incapable of extracting the highest possible performance out of the power converters. Thus, although linear control schemes are well-developed for many power electronics applications, the dependency on these control methods has been retracted, especially with the increase penetration level of the distributed energy resources (DERs) into the main electric grid. On the other hand, the intuitive control implementation, discrete-nature of power converters, multiple constraints, control platforms advancement, and other well-known nonlinear control characteristics have distinguished

the MPC method among the other nonlinear control strategies. As a consequence, the MPC method exhibits a promising alternative for traditional linear and non-linear control schemes.

Therefore, the primary objective of this dissertation was to develop novel model predictive control (MPC) strategies which attain all the well-known characteristics of the non-linear predictive control and solve the challenges related to implementing such a control technique on three-phase three-level (3-L) voltage source converters (VSCs) operating in an MG. The main issues with the existing MPC schemes when they are applied to 3-L VSC topologies include

- The need for a multi-objective quality function, which deteriorates the performance of the controller as control efforts are distributed;
- The need for a careful weighting factors design, which is time-consuming and laborious, and restricted to certain VSC operating conditions;
- The need for signal measurements from both the ac and dc sides of the 3-L VSC, which is costly and unreliable;
- Increased total harmonic distortion (THD) of the VSC output waveforms due to the relatively low and variable switching frequency as well as increased neutral-point voltage (NP-V) fluctuations;
- High controller computational time due to the complex control algorithms, which requires a powerful digital control platform.

In this dissertation, much research has been conducted and focused on the new MPC strategies using the virtual space vectors (VSVs) for three-phase 3-L VSCs operating in MGs. The obtained following conclusions are drawn based on the completion of this research work.

In Chapter 3 of this dissertation, research was conducted on an MPC strategy using six additional VSVs. The control technique could well serve in applications, which has intermittent nature of power generation, similar to renewable energy sources (RESs), which exist in the MG applications. Controller hardware-in-the-loop results validated that the enhanced MPC technique reduced the THD of the converter output waveforms from 2.98 % to 2.22 % when the same weighting factor of dc-link capacitor voltages balancing term was used in the cost function. In addition, it was verified that the NP-V oscillations were mitigated as a result of adopting the VSVs concept. The peak-to-peak voltage ripples across the dc-link capacitors were reduced from 72 V to 68 V. Although the enhanced MPC used more voltage vectors to be evaluated within the same sampling period, the fast-dynamic response was attained as the controlled current signal, when the classical and enhanced MPC methods were tested, tracked its reference within 2 *m*s as shown in the C-HIL studies. The work proposed in Chapter 3 was just the kernel of a novel MPC strategy.

Hence, extensive research was conducted to develop a simple-innovative MPC strategy. The novel MPC scheme took the advantages of the VSVs concept to completely replace the voltage vectors with non-zero NP-C by other voltage vectors, which have an average NP-C that is equal to zero. The proposed MPC technique had the advantages of being simple to be designed due to the simplified control algorithm compared to that of the conventional MPC method. Also, the dc-link capacitor voltages balancing had been inherently achieved, which reduced the sensing circuitries used with the classical MPC approach. Furthermore, a noticeably improved converter output waveforms was accomplished due to the increased average switching frequency as well as the well-regulated NP-V fluctuations. The calculation burden of the controller algorithm was substantially reduced when the proposed MPC scheme was the control candidate. This significant decrease in the controller execution time was the result of the proposed simple algorithm, which

neglect the dc-link capacitor voltages balancing term due to the accomplished inherent dc-link voltage balancing. All these merits were accomplished without using extra hardware, which is mandatory in the traditional MPC method. Extensive simulation and experimental studies verified that the proposed MPC using VSVs approach achieved better results than those of the classical MPC strategy. All the recognized features of predictive control like the fast-transient response and the robustness against parameter uncertainties were also attained. In short, the proposed MPC strategy considerably reduced the NP-V fluctuations from 20 V to only 12 V. Compared to the classical MPC approach, the presented MPC scheme improved the quality of the converter *LC*-filter output waveform by 0.42 % when compared with the conventional MPC one. Additionally, the voltage reference tracking was enhanced by 0.78 % as a result of adopting the proposed MPC scheme. The controller computational burden was significantly reduced from 14.8 μs to 11.2 μs due to the proposed simplified MPC algorithm. All the aforementioned accomplishments were obtained at the cost of a 0.035 % reduction in converter efficiency.

5.2 Contributions of This Dissertation

Several achievements have been accomplished throughout this dissertation. These contributions are summarized as follows

- Comprehensive review for the 3-L VSC model, the dc-link capacitor models and the different output passive filters models have been provided in this dissertation along with the complete description for one of the most popular synchronization techniques, i.e. SRF-PLL, which facilitates the implementation of the MPC on various MG applications.
- Enhanced MPC strategy was proposed to improve the performance of MPC when being implemented on 3-L neutral-point clamped (NPC) VSCs. Improved output waveforms quality and mitigated NP-V fluctuations were accomplished. A relatively small weighting

factor for the dc-link capacitor voltages balancing term in the quality function could be selected such that more considerations for the primary objective of the designed MPC were given. Ultimately, improved signal reference tracking was accomplished. The additional six VSVs were the key idea in the proposed MPC method. Thus, the synthetization of these voltage vectors and their extended switching states were presented.

- Gating signals implementation technique was proposed using an external modulator. The modulator eased achieving the required duty cycle of the proposed extended switching states using simple algebraic equations.
- Switching and conduction power loss model was proposed to evaluate the different power losses at the power semiconductor devices, which eventually ensured the proposed MPC strategies do not reduce the 3-L VSC efficiency.
- A simple-innovative MPC scheme was proposed to simplify the design process of classical MPC algorithms for the 3-L VSCs. An updated SV diagram, which fully occupied with zero NP-C voltage space vector was proposed by means of the VSVs. A guaranteed balanced dc-link capacitor voltages were a major outcome of the proposed MPC strategy. The substantial contribution simplified the hardware design and eliminated the unnecessary voltage and current sensor boards. This was a reality due to the fact that a single-objective cost function, which replaced the traditional dual-objective cost function for 3-L VSCs, was proposed resulting in a simple MPC algorithm. Ultimately, controller computational burden was significantly decreased. The VSC output waveforms with reduced ripples were obtained due to the increased average switching frequency as a result of utilizing of the VSVs as well as the well-regulated NP-V oscillations.

5.3 Future Research Work

Both MPC and grid-connected and stand-alone converter systems have been hot topics in recent years. Therefore, much research can be conducted to contribute to these subjects. Some of the recommendations for the future work are listed as follows

- When designing a model predictive voltage control (MPVC) for a 3-L VSC, a load-current observer can be developed since the load is usually unknown and a mathematical estimation for the load current is not reliable. This observer cannot only reduce the hardware cost and the THD, but also it can be further used to estimate the NP-C, which provides more support to the NP-V regulation.
- Utilize the concept VSVs to suppress the common mode (CM) noise. A common method to eliminate the common mode noise is to consider the zero and medium voltage vectors since these voltage vectors do not produce common mode voltage. However, a major drawback of this technique is that the utilization rate of the dc-bus voltage is decreased. Therefore, such an advanced technique can be further improved to wisely utilize the redundant switching states in order to reduce or even eliminate the common mode noise.
- Develop a more advanced MPC by significantly increasing the number of the VSVs in the finite control set (FCS). A significant improvement in the VSC output waveforms will be expected. An algorithm, which can wisely utilize the voltage vectors close to the reference, can also be designed so that the controller computation time will not be sacrificed.
- Investigate the possibility of using VSVs and the external modular to obtain a fixed switching frequency without increasing the controller computation time. This in particular is advantageous for the grid-connected and grid-forming VSCs since a fixed switching

frequency facilitates the VSC output *LCL*- and *LC*-filter design, and ultimately achieving high-quality waveforms.

- Investigate designing a hybrid MPC scheme, which combines the traditional and proposed MPC using the VSVs. During unbalance load conditions, the proposed additional six VSVs do not result in an average zero NP-C. Consequently, the harmonic components of the VSC output waveforms are increased due to the unbalance dc-link capacitor voltages. As thus, this suggested control strategy, the hybrid MPC, can secure a safe operation of the proposed MPC one even during unbalance system conditions.
- Utilize the developed switching and conduction power loss model to monitor the losses of the converter different switches so that thermal considerations can be included in the controller design to predict potential future failure in power semiconductor devices.

BIBLIOGRAPHY

[1] C. L. Sulzberger, "Triumph of AC - from Pearl Street to Niagara," *IEEE Power and Energy Magazine,* vol. 1, no. 3, pp. 64-67, 2003.

[2] R. W. Lobenstein, and C. Sulzberger, "Eyewitness to dc History," *IEEE Power and Energy Magazine,* vol. 6, no. 3, pp. 84-90, 2008.

[3] C. Sulzberger, "Pearl Street in Miniature: Models of the Electric Generating Station [History]," *IEEE Power and Energy Magazine,* vol. 11, no. 2, pp. 76-85, 2013.

[4] Q. Zhong, "Power-Electronics-Enabled Autonomous Power Systems: Architecture and Technical Routes," *IEEE Trans. Ind. Electron.,* vol. 64, no. 7, pp. 5907-5918, July 2017.

[5] G. Strbac, N. Hatziargyriou, J. P. Lopes, C. Moreira, A. Dimeas, and D. Papadaskalopoulos, "Microgrids: Enhancing the Resilience of the European Megagrid," *IEEE Power and Energy Magazine,* vol. 13, no. 3, pp. 35-43, 2015.

[6] D. Boroyevich, I. Cvetkovic, R. Burgos, and D. Dong, "Intergrid: A Future Electronic Energy Network?," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 1, no. 3, pp. 127-138, Sept. 2013.

[7] X. Yu, C. Cecati, T. Dillon, and M. G. Simões, "The New Frontier of Smart Grids," *IEEE Industrial Electronics Magazine,* vol. 5, no. 3, pp. 49-63, 2011.

[8] X. She, A. Q. Huang, and R. Burgos, "Review of Solid-State Transformer Technologies and Their Application in Power Distribution Systems," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 1, no. 3, pp. 186-198, Sept. 2013.

[9] C. Massimo, and P. Davide, *Fundamentals of Electric Power Engineering: From Electromagnetics to Power Systems*. Hoboken, NJ: John Wiley & Sons 2014.

[10] S. Bifaretti, P. Zanchetta, A. Watson, L. Tarisciotti, and J. C. Clare, "Advanced Power Electronic Conversion and Control System for Universal and Flexible Power Management," *IEEE Trans. Smart Grid,* vol. 2, no. 2, pp. 231-243, June 2011.

[11] Z. Wang, C. Shen, Y. Xu, F. Liu, X. Wu, and C. Liu, "Risk-Limiting Load Restoration for Resilience Enhancement With Intermittent Energy Resources," *IEEE Trans. Smart Grid,* vol. 10, no. 3, pp. 2507-2522, May 2019.

[12] B. Chen, Z. Ye, C. Chen, J. Wang, T. Ding, and Z. Bie, "Toward a Synthetic Model for Distribution System Restoration and Crew Dispatch," *IEEE Trans. Power Syst.,* vol. 34, no. 3, pp. 2228-2239, May 2019.

[13] S. Lee, and J. Park, "Selection of Optimal Location and Size of Multiple Distributed Generations by Using Kalman Filter Algorithm," *IEEE Trans. Power Syst.,* vol. 24, no. 3, pp. 1393-1400, Aug. 2009.

[14] S. M. M. Larimi, M. R. Haghifam, M. Zangiabadi, and P. Taylor, "Value Based Pricing of Distribution Generations Active Power in Distribution Networks," *IET Generation, Transmission & Distribution,* vol. 9, no. 15, pp. 2117-2125, Nov. 2015.

[15] F. Bouffard, and F. D. Galiana, "Stochastic Security for Operations Planning With Significant Wind Power Generation," *IEEE Trans. Power Syst.,* vol. 23, no. 2, pp. 306-316, May 2008.

[16] A. Y. Saber and G. K. Venayagamoorthy, "Plug-in Vehicles and Renewable Energy Sources for Cost and Emission Reductions," in *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1229-1238, April 2011.

[17] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *IEEE Trans. Ind. Electron.,* vol. 53, no. 5, pp. 1398-1409, Oct. 2006.

[18] M. Castilla, A. Camacho, P. Martí, M. Velasco, and M. M. Ghahderijani, "Impact of Clock Drifts on Communication-Free Secondary Control Schemes for Inverter-Based Islanded Microgrids," *IEEE Trans. Ind. Electron.,* vol. 65, no. 6, pp. 4739-4749, June 2018.

[19] H. Moussa, A. Shahin, J. Martin, B. Nahid-Mobarakeh, S. Pierfederici, and N. Moubayed, "Harmonic Power Sharing With Voltage Distortion Compensation of Droop Controlled Islanded Microgrids," *IEEE Trans. Smart Grid,* vol. 9, no. 5, pp. 5335-5347, Sept. 2018.

[20] P. Zhao, S. Suryanarayanan, and M. G. Simoes, "An Energy Management System for Building Structures Using a Multi-Agent Decision-Making Control Methodology," *IEEE Trans. Ind. Appl.,* vol. 49, no. 1, pp. 322-330, Jan.-Feb. 2013.

[21] J. Mitra, M. R. Vallem, and C. Singh, "Optimal Deployment of Distributed Generation Using a Reliability Criterion," *IEEE Trans. Ind. Appl.,* vol. 52, no. 3, pp. 1989-1997, May-June 2016.

[22] A. Ciocia *et al*., "Voltage Control in Low-Voltage Grids Using Distributed Photovoltaic Converters and Centralized Devices," *IEEE Trans. Ind. Appl.,* vol. 55, no. 1, pp. 225-237, Jan.-Feb. 2019.

[23] M.-G. Á, R. A. Mastromauro, T. García-Sánchez, S. Pugliese, M. Liserre, and S. Stasi, "Reactive Power Flow Control for PV Inverters Voltage Support in LV Distribution Networks," *IEEE Trans. Smart Grid,* vol. 8, no. 1, pp. 447-456, Jan. 2017.

[24] H. Mahmood, D. Michaelson, and J. Jiang, "A Power Management Strategy for PV/Battery Hybrid Systems in Islanded Microgrids," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 2, no. 4, pp. 870-882, Dec. 2014.

[25] F. Yang, Q. Sun, Q. Han, and Z. Wu, "Cooperative Model Predictive Control for Distributed Photovoltaic Power Generation Systems," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 4, no. 2, pp. 414-420, June 2016.

[26] J. Schiffer, C. A. Hans, T. Kral, R. Ortega, and J. Raisch, "Modeling, Analysis, and Experimental Validation of Clock Drift Effects in Low-Inertia Power Systems," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5942-5951, July 2017.

[27] H. V. Padullaparti, Q. Nguyen, and S. Santoso, "Optimal Placement and Dispatch of LV-SVCs to Improve Distribution Circuit Performance," *IEEE Trans. Power Syst.*, vol. 34, no. 4, pp. 2892-2900, July 2019.

[28] D. Divan, R. Moghe, and A. Prasai, "Power Electronics at the Grid Edge : The key to Unlocking Value from the Smart Grid," *IEEE Power Electronics Magazine*, vol. 1, no. 4, pp. 16-22, 2014.

[29] W. Caisheng, and M. H. Nehrir, "Analytical Approaches for Optimal Placement of Distributed Generation Sources in Power Systems," *IEEE Trans. Power Syst.*, vol. 19, no. 4, pp. 2068-2076, Nov. 2004.

[30] Y. Shan, J. Hu, and J. M. Guerrero, "A Model Predictive Power Control Method for PV and Energy Storage Systems With Voltage Support Capability," *IEEE Trans. Smart Grid*, vol. 11, no. 2, pp. 1018-1029, March 2020.

[31] S. H. Lee, and J. Park, "Optimal Placement and Sizing of Multiple DGs in a Practical Distribution System by Considering Power Loss," *IEEE Trans. Ind. Appl.*, vol. 49, no. 5, pp. 2262-2270, Sept-Oct. 2013.

[32] J. M. Carrasco *et al*., "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey," in *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002-1016, June 2006.

[33] C. N. Ho, H. Breuninger, S. Pettersson, G. Escobar, L. A. Serpa, and A. Coccia, "Practical Design and Implementation Procedure of an Interleaved Boost Converter Using SiC Diodes for PV Applications," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2835-2845, June 2012.

[34] A. Verma, R. Krishan, and S. Mishra, "A Novel PV Inverter Control for Maximization of Wind Power Penetration," *IEEE Trans. Ind. Appl.*, vol. 54, no. 6, pp. 6364-6373, Nov.-Dec. 2018.

[35] P. Mohammadi, and S. Mehraeen, "Challenges of PV Integration in Low-Voltage Secondary Networks," *IEEE Trans. Power Del.*, vol. 32, no. 1, pp. 525-535, Feb. 2017.

[36] F. Katiraei, and J. R. Agüero, "Solar PV Integration Challenges," *IEEE Power and Energy Magazine*, vol. 9, no. 3, pp. 62-71, 2011.

[37] R. A. Walling, R. Saint, R. C. Dugan, J. Burke, and L. A. Kojovic, "Summary of Distributed Resources Impact on Power Delivery Systems," *IEEE Trans. Power Del.*, vol. 23, no. 3, pp. 1636-1644, July 2008.

[38] Y. Riffonneau, S. Bacha, F. Barruel, and S. Ploix, "Optimal Power Flow Management for Grid Connected PV Systems With Batteries," *IEEE Trans. Sustain. Energy,* vol. 2, no. 3, pp. 309-320, July 2011.

[39] B. Mangu, S. Akshatha, D. Suryanarayana, and B. G. Fernandes, "Grid-Connected PV-Wind-Battery-Based Multi-Input Transformer-Coupled Bidirectional DC-DC Converter for Household Applications," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 4, no. 3, pp. 1086-1095, Sept. 2016.

[40] R. H. Lasseter, "MicroGrids," *2002 IEEE Power Engineering Society Winter Meeting. Conference Proceedings (Cat. No.02CH37309)*, New York, NY, USA, 2002, pp. 305-308 vol.1.

[41] F. Katiraei, and M. R. Iravani, "Power Management Strategies for a Microgrid With Multiple Distributed Generation Units," *IEEE Trans. Power Syst.,* vol. 21, no. 4, pp. 1821-1831, Nov. 2006.

[42] G. Diaz, C. Gonzalez-Moran, J. Gomez-Aleixandre, and A. Diez, "Composite Loads in Stand-Alone Inverter-Based Microgrids—Modeling Procedure and Effects on Load Margin," *IEEE Trans. Power Syst.,* vol. 25, no. 2, pp. 894-905, May 2010.

[43] P. Martí, J. Torres-Martínez, C. X. Rosero, M. Velasco, J. Miret, and M. Castilla, "Analysis of the Effect of Clock Drifts on Frequency Regulation and Power Sharing in Inverter-Based Islanded Microgrids," *IEEE Trans. Power Electron.,* vol. 33, no. 12, pp. 10363-10379, Dec. 2018.

[44] C. X. Rosero, M. Velasco, P. Martí, A. Camacho, J. Miret, and M. Castilla, "Analysis of Consensus-Based Islanded Microgrids Subject to Unexpected Electrical and Communication Partitions," *IEEE Trans. Smart Grid,* vol. 10, no. 5, pp. 5125-5135, Sept. 2019.

[45] V. Nasirian, Q. Shafiee, J. M. Guerrero, F. L. Lewis, and A. Davoudi, "Droop-Free Distributed Control for AC Microgrids," *IEEE Trans. Power Electron.,* vol. 31, no. 2, pp. 1600-1617, Feb. 2016.

[46] A. L. Bella, S. R. Cominesi, C. Sandroni, and R. Scattolini, "Hierarchical Predictive Control of Microgrids in Islanded Operation," *IEEE Trans. Auto. Sci. Eng.,* vol. 14, no. 2, pp. 536-546, April 2017.

[47] D. F. Teshome, W. Xu, P. Bagheri, A. Nassif, and Y. Zhou, "A Reactive Power Control Scheme for DER-Caused Voltage Rise Mitigation in Secondary Systems," *IEEE Trans. Sustain. Energy,* vol. 10, no. 4, pp. 1684-1695, Oct. 2019.

[48] F. Guo, C. Wen, J. Mao, and Y. Song, "Distributed Secondary Voltage and Frequency Restoration Control of Droop-Controlled Inverter-Based Microgrids," *IEEE Trans. Ind. Electron.,* vol. 62, no. 7, pp. 4355-4364, July 2015.

[49] J. Zhao, X. Lyu, Y. Fu, X. Hu, and F. Li, "Coordinated Microgrid Frequency Regulation Based on DFIG Variable Coefficient Using Virtual Inertia and Primary Frequency Control," *IEEE Trans. Energy Convers.*, vol. 31, no. 3, pp. 833-845, Sept. 2016.

[50] Y. Khayat *et al*., "Decentralized Optimal Frequency Control in Autonomous Microgrids," *IEEE Trans. Power Syst.*, vol. 34, no. 3, pp. 2345-2353, May 2019.

[51] C. Chen, J. Wang, F. Qiu, and D. Zhao, "Resilient Distribution System by Microgrids Formation After Natural Disasters," *IEEE Trans. Smart Grid,* vol. 7, no. 2, pp. 958-966, March 2016.

[52] H. Gao, Y. Chen, Y. Xu, and C. Liu, "Resilience-Oriented Critical Load Restoration Using Microgrids in Distribution Systems," *IEEE Trans. Smart Grid,* vol. 7, no. 6, pp. 2837-2848, Nov. 2016.

[53] Y. Xu, C. Liu, K. P. Schneider, F. K. Tuffner, and D. T. Ton, "Microgrids for Service Restoration to Critical Load in a Resilient Distribution System," *IEEE Trans. Smart Grid,* vol. 9, no. 1, pp. 426-437, Jan. 2018.

[54] S. Ma, L. Su, Z. Wang, F. Qiu, and G. Guo, "Resilience Enhancement of Distribution Grids Against Extreme Weather Events," *IEEE Trans. Power Syst.*, vol. 33, no. 5, pp. 4842-4853, Sept. 2018.

[55] J. A. P. Lopes, C. L. Moreira, and A. G. Madureira, "Defining Control Strategies for MicroGrids Islanded Operation," *IEEE Trans. Power Syst.*, vol. 21, no. 2, pp. 916-924, May 2006.

[56] J. Kim, J. M. Guerrero, P. Rodriguez, R. Teodorescu, and K. Nam, "Mode Adaptive Droop Control With Virtual Output Impedances for an Inverter-Based Flexible AC Microgrid," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 689-701, March 2011.

[57] H. Mahmood, D. Michaelson, and J. Jiang, "Decentralized Power Management of a PV/Battery Hybrid Unit in a Droop-Controlled Islanded Microgrid," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7215-7229, Dec. 2015.

[58] X. Quan, X. Dou, Z. Wu, M. Hu, H. Song, and A. Q. Huang, "A Novel Dominant Dynamic Elimination Control for Voltage-Controlled Inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6800-6812, Aug. 2018.

[59] S. P. Ribas, L. A. Maccari, H. Pinheiro, R. Coração de Leão Fontoura de Oliveira and V. Foletto Montagner, "Design and implementation of a discrete-time H-infinity controller for uninterruptible power supply systems," in *IET Power Electronics*, vol. 7, no. 9, pp. 2233-2241, Sept. 2014.

[60] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodríguez, "Control of Power Converters in AC Microgrids," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4734-4749, Nov. 2012.

[61] E. Afshari *et al*., "Control Strategy for Three-Phase Grid-Connected PV Inverters Enabling Current Limitation Under Unbalanced Faults," *IEEE Trans. Ind. Electron.,* vol. 64, no. 11, pp. 8908-8918, Nov. 2017.

[62] S. Alepuz *et al*., "Control Strategies Based on Symmetrical Components for Grid-Connected Converters Under Voltage Dips," *IEEE Trans. Ind. Electron.,* vol. 56, no. 6, pp. 2162-2173, June 2009.

[63] I. J. Balaguer, Q. Lei, S. Yang, U. Supatti, and F. Z. Peng, "Control for Grid-Connected and Intentional Islanding Operations of Distributed Power Generation," *IEEE Trans. Ind. Electron.,* vol. 58, no. 1, pp. 147-157, Jan. 2011.

[64] P. Rodriguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multiresonant Frequency-Locked Loop for Grid Synchronization of Power Converters Under Distorted Grid Conditions," *IEEE Trans. Ind. Electron.,* vol. 58, no. 1, pp. 127-138, June 2011.

[65] R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg, and C. L. Bak, "A Review of Passive Power Filters for Three-Phase Grid-Connected Voltage-Source Converters," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 4, no. 1, pp. 54-69, March 2016.

[66] M. Lindgren and J. Svensson, "Control of a Voltage-Source Converter Connected to the Grid Through an LCL-Filter-Application to Active Filtering," *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No.98CH36196),* Fukuoka, 1998, pp. 229-235 vol.1.

[67] P. Channegowda, and V. John, "Filter Optimization for Grid Interactive Voltage Source Inverters," *IEEE Trans. Ind. Electron.,* vol. 57, no. 12, pp. 4106-4114, Dec. 2010.

[68] R. Peña-Alzola, M. Liserre, F. Blaabjerg, R. Sebastián, J. Dannehl, and F. W. Fuchs, "Analysis of the Passive Damping Losses in LCL-Filter-Based Grid Converters," *IEEE Trans. Power Electron.,* vol. 28, no. 6, pp. 2642-2646, June 2013.

[69] V. Blasko, and V. Kaura, "A Novel Control to Actively Damp Resonance in Input LC Filter of a Three-Phase Voltage Source Converter," *IEEE Trans. Ind. Appl.,* vol. 33, no. 2, pp. 542-550, March-April 1997.

[70] Y. Tang, W. Yao, P. C. Loh, and F. Blaabjerg, "Design of LCL Filters With LCL Resonance Frequencies Beyond the Nyquist Frequency for Grid-Connected Converters," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 4, no. 1, pp. 3-14, March 2016.

[71] W. Wu *et al*., "A Robust Passive Damping Method for LLCL-Filter-Based Grid-Tied Inverters to Minimize the Effect of Grid Harmonic Voltages," *IEEE Trans. Power Electron.,* vol. 29, no. 7, pp. 3279-3289, July 2014.

[72] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and Control of an LCL-Filter-Based Three-Phase Active Rectifier," *IEEE Trans. Ind. Appl.,* vol. 41, no. 5, pp. 1281-1291, Sept.-Oct. 2005.

[73] M. B. Saïd-Romdhane, M. W. Naouar, I. Slama-Belkhodja, and E. Monmasson, "Robust Active Damping Methods for LCL Filter-Based Grid-Connected Converters," *IEEE Trans. Power Electron.,* vol. 32, no. 9, pp. 6739-6750, Sept. 2017.

[74] J. Dannehl, M. Liserre, and F. W. Fuchs, "Filter-Based Active Damping of Voltage Source Converters With *LCL* Filter," *IEEE Trans. Ind. Electron.,* vol. 58, no. 8, pp. 3623-3633, Aug. 2011.

[75] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang, "Capacitor-Current-Feedback Active Damping With Reduced Computation Delay for Improving Robustness of LCL-Type Grid-Connected Inverter," *IEEE Trans. Power Electron.,* vol. 29, no. 7, pp. 3414-3427, July 2014.

[76] M. Bragard, N. Soltau, S. Thomas, and R. W. D. Doncker, "The Balance of Renewable Sources and User Demands in Grids: Power Electronics for Modular Battery Energy Storage Systems," *IEEE Trans. Power Electron.,* vol. 25, no. 12, pp. 3049-3056, Dec. 2010.

[77] P. Mattavelli, F. Polo, F. D. Lago, and S. Saggini, "Analysis of Control-Delay Reduction for the Improvement of UPS Voltage-Loop Bandwidth," *IEEE Trans. Ind. Electron.,* vol. 55, no. 8, pp. 2903-2911, Aug. 2008.

[78] J. C. Vasquez, J. M. Guerrero, M. Savaghebi, J. Eloy-Garcia, and R. Teodorescu, "Modeling, Analysis, and Design of Stationary-Reference-Frame Droop-Controlled Parallel Three-Phase Voltage Source Inverters," *IEEE Trans. Ind. Electron.,* vol. 60, no. 4, pp. 1271-1280, April 2013.

[79] X. Wang, Y. W. Li, F. Blaabjerg, and P. C. Loh, "Virtual-Impedance-Based Control for Voltage-Source and Current-Source Converters," *IEEE Trans. Power Electron.,* vol. 30, no. 12, pp. 7019-7037, Dec. 2015.

[80] F. d. Bosio, L. A. d. S. Ribeiro, F. D. Freijedo, M. Pastorelli, and J. M. Guerrero, "Effect of State Feedback Coupling and System Delays on the Transient Performance of Stand-Alone VSI With LC Output Filter," *IEEE Trans. Ind. Electron.,* vol. 63, no. 8, pp. 4909-4918, Aug. 2016.

[81] Y. Geng, Y. Yun, R. Chen, K. Wang, H. Bai, and X. Wu, "Parameters Design and Optimization for LC-Type Off-Grid Inverters With Inductor-Current Feedback Active Damping," *IEEE Trans. Power Electron.,* vol. 33, no. 1, pp. 703-715, Jan. 2018.

[82] S. Tolani, S. Joshi, and P. Sensarma, "Dual-Loop Digital Control of a Three-Phase Power Supply Unit With Reduced Sensor Count," *IEEE Trans. Ind. Appl.,* vol. 54, no. 1, pp. 367-375, Jan.-Feb. 2018.

[83] Y. W. Li, "Control and Resonance Damping of Voltage-Source and Current-Source Converters With *LC* Filters," *IEEE Trans. Ind. Electron.,* vol. 56, no. 5, pp. 1511-1521, May 2009.

[84] Z. Li, Y. Li, P. Wang, H. Zhu, C. Liu, and F. Gao, "Single-Loop Digital Control of High-Power 400-Hz Ground Power Unit for Airplanes," *IEEE Trans. Ind. Electron.,* vol. 57, no. 2, pp. 532-543, Feb. 2010.

[85] X. Wang, P. C. Loh, and F. Blaabjerg, "Stability Analysis and Controller Synthesis for Single-Loop Voltage-Controlled VSIs," *IEEE Trans. Power Electron.,* vol. 32, no. 9, pp. 7394-7404, Sept. 2017.

[86] X. Li, P. Lin, Y. Tang, and K. Wang, "Stability Design of Single-Loop Voltage Control With Enhanced Dynamic for Voltage-Source Converters With a Low LC-Resonant-Frequency," *IEEE Trans. Power Electron.,* vol. 33, no. 11, pp. 9937-9951, Nov. 2018.

[87] H. Kim, H. Jung, and S. Sul, "Discrete-Time Voltage Controller for Voltage Source Converters With LC Filter Based on State-Space Models," *IEEE Trans. Ind. Appl.,* vol. 55, no. 1, pp. 529-540, Jan.-Feb. 2019.

[88] D. Pérez-Estévez, J. Doval-Gandoy, and J. M. Guerrero, "AC-Voltage Harmonic Control for Stand-Alone and Weak-Grid-Tied Converter," *IEEE Trans. Ind. Appl.,* vol. 56, no. 1, pp. 403-421, Jan.-Feb. 2020.

[89] J. M. Guerrero, L. Hang, and J. Uceda, "Control of Distributed Uninterruptible Power Supply Systems," *IEEE Trans. Ind. Electron.,* vol. 55, no. 8, pp. 2845-2859, Aug. 2008.

[90] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, "Decoupled Double Synchronous Reference Frame PLL for Power Converters Control," *IEEE Trans. Power Electron.,* vol. 22, no. 2, pp. 584-592, March 2007.

[91] D. Pérez-Estévez, and J. Doval-Gandoy, "Grid-Tied Inverter With AC Voltage Sensorless Synchronization and Soft Start," *IEEE Trans. Ind. Appl.,* vol. 55, no. 5, pp. 4920-4933, Sept.-Oct. 2019.

[92] H. Guan-Chyun, and J. C. Hung, "Phase-Locked Loop Techniques. A Survey," *IEEE Trans. Ind. Electron.,* vol. 43, no. 6, pp. 609-615, Dec. 1996.

[93] C. Se-Kyo, "A Phase Tracking System for Three Phase Utility Interface Inverters," *IEEE Trans. Power Electron.,* vol. 15, no. 3, pp. 431-438, May 2000.

[94] S. M. Ashabani, and Y. A. I. Mohamed, "A Flexible Control Strategy for Grid-Connected and Islanded Microgrids With Enhanced Stability Using Nonlinear Microgrid Stabilizer," *IEEE Trans. Smart Grid,* vol. 3, no. 3, pp. 1291-1301, Sept. 2012.

[95] D. Dong, B. Wen, P. Mattavelli, D. Boroyevich, and Y. Xue, "Modeling and Design of Islanding Detection Using Phase-Locked Loops in Three-Phase Grid-Interface Power Converters," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 2, no. 4, pp. 1032-1040, Dec. 2014.

[96] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and E. Acha, "Tuning of Phase-Locked Loops for Power Converters Under Distorted Utility Conditions," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2039-2047, Nov.-Dec. 2009.

[97] E. Kantar, and A. M. Hava, "Optimal Design of Grid-Connected Voltage-Source Converters Considering Cost and Operating Factors," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5336-5347, Sept. 2016.

[98] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219-2230, July 2010.

[99] J. Weidong, L. Wang, J. Wang, X. Zhang, and P. Wang, "A Carrier-Based Virtual Space Vector Modulation With Active Neutral-Point Voltage Control for a Neutral-Point-Clamped Three-Level Inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 11, pp. 8687-8696, Nov. 2018.

[100] J. Lyu, J. Wang, W. Hu, and Y. Yan, "A Neutral-Point Voltage Controller With Hybrid Parameters for NPC Three-Level Grid-Connected Inverters Under Unbalanced Grid Conditions," *IEEE J. Emerg. Sel. Topics Power Electron.*, to be published, doi: 10.1109/JESTPE.2019.2930570.

[101] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, and D. Boroyevich, "A Carrier-Based PWM Strategy With Zero-Sequence Voltage Injection for a Three-Level Neutral-Point-Clamped Converter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 642-651, Feb. 2012.

[102] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative Evaluation of Advanced Three-Phase Three-Level Inverter/Converter Topologies Against Two-Level Systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5515-5527, Dec. 2013.

[103] M. Schweizer, and J. W. Kolar, "Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899-907, Feb. 2013.

[104] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518-523, Sept. 1981.

[105] N. Celanovic, and D. Boroyevich, "A Comprehensive Study of Neutral-Point Voltage Balancing Problem in Three-Level Neutral-Point-Clamped Voltage Source PWM Inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242-249, March 2000.

[106] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2581-2596, Aug. 2010.

[107] R. Portillo, S. Vazquez, J. I. Leon, M. M. Prats, and L. G. Franquelo, "Model Based Adaptive Direct Power Control for Three-Level NPC Converters," *IEEE Trans. Ind. Inf.*, vol. 9, no. 2, pp. 1148-1157, May 2013.

[108] L. Yacoubi, K. Al-Haddad, L. Dessaint, and F. Fnaiech, "Linear and Nonlinear Control Techniques for a Three-Phase Three-Level NPC Boost Rectifier," *IEEE Trans. Ind. Electron.,* vol. 53, no. 6, pp. 1908-1918, Dec. 2006.

[109] R. Jose, and C. Patricio, *Predictive Control of Power Converters and Electrical Drives* Chichester. West Sussex: John Wiley & Sons, 2012.

[110] M. P. Kazmierkowski, and L. Malesani, "Current Control Techniques for Three-Phase Voltage-Source PWM Converters: a Survey," *IEEE Trans. Ind. Electron.,* vol. 45, no. 5, pp. 691-703, Oct. 1998.

[111] D. N. Zmood, and D. G. Holmes, "Stationary Frame Current Regulation of PWM Inverters With Zero Steady-State Error," *IEEE Trans. Power Electron.,* vol. 18, no. 3, pp. 814-822, May 2003.

[112] B. Bahrani, S. Kenzelmann, and A. Rufer, "Multivariable-PI-Based *dq* Current Control of Voltage Source Converters With Superior Axis Decoupling Capability," *IEEE Trans. Ind. Electron.,* vol. 58, no. 7, pp. 3016-3026, July 2011.

[113] R. Teodorescu, F. Blaabjerg, M. Liserre and P. C. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters," in *IEE Proceedings - Electric Power Applications*, vol. 153, no. 5, pp. 750-762, Sept. 2006.

[114] J. Rodriguez *et al*., "Predictive Current Control of a Voltage Source Inverter," *IEEE Trans. Ind. Electron.,* vol. 54, no. 1, pp. 495-503, Feb. 2007.

[115] S. Kouro, P. Cortes, R. Vargas, U. Ammann, and J. Rodriguez, "Model Predictive Control—A Simple and Powerful Method to Control Power Converters," *IEEE Trans. Ind. Electron.,* vol. 56, no. 6, pp. 1826-1838, June 2009.

[116] T. Geyer, G. Papafotiou, and M. Morari, "Model Predictive Direct Torque Control—Part I: Concept, Algorithm, and Analysis," *IEEE Trans. Ind. Electron.,* vol. 56, no. 6, pp. 1894-1905, June 2009.

[117] J. Rodriguez *et al*., "State of the Art of Finite Control Set Model Predictive Control in Power Electronics," *IEEE Trans. Ind. Inf.,* vol. 9, no. 2, pp. 1003-1016, May 2013.

[118] C. Hu *et al*., "An Improved Virtual Space Vector Modulation Scheme for Three-Level Active Neutral-Point-Clamped Inverter," *IEEE Trans. Power Electron.,* vol. 32, no. 10, pp. 7419-7434, Oct. 2017.

[119] S. Xu, J. Zhang, Y. Huang, and J. Jatskevich, "Dynamic Average-Value Modeling of Three-Level T-Type Grid-Connected Converter System," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 7, no. 4, pp. 2428-2442, Dec. 2019.

[120] Z. Liang, X. Lin, X. Qiao, Y. Kang, and B. Gao, "A Coordinated Strategy Providing Zero-Sequence Circulating Current Suppression and Neutral-Point Potential Balancing in Two

Parallel Three-Level Converters," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 6, no. 1, pp. 363-376, March 2018.

[121] R. Davoodnezhad, D. G. Holmes, and B. P. McGrath, "A Novel Three-Level Hysteresis Current Regulation Strategy for Three-Phase Three-Level Inverters," *IEEE Trans. Power Electron.,* vol. 29, no. 11, pp. 6100-6109, Nov. 2014.

[122] R. Vargas, P. Cortes, U. Ammann, J. Rodriguez, and J. Pontt, "Predictive Control of a Three-Phase Neutral-Point-Clamped Inverter," *IEEE Trans. Ind. Electron.,* vol. 54, no. 5, pp. 2697-2705, Oct. 2007.

[123] A. Calle-Prado, S. Alepuz, J. Bordonau, J. Nicolas-Apruzzese, P. Cortés, and J. Rodriguez, "Model Predictive Current Control of Grid-Connected Neutral-Point-Clamped Converters to Meet Low-Voltage Ride-Through Requirements," *IEEE Trans. Ind. Electron.,* vol. 62, no. 3, pp. 1503-1514, March 2015.

[124] S. A. Davari, D. A. Khaburi, and R. Kennel, "An Improved FCS–MPC Algorithm for an Induction Motor With an Imposed Optimized Weighting Factor," *IEEE Trans. Power Electron.,* vol. 27, no. 3, pp. 1540-1551, March 2012.

[125] C. A. Rojas, J. Rodriguez, F. Villarroel, J. R. Espinoza, C. A. Silva, and M. Trincado, "Predictive Torque and Flux Control Without Weighting Factors," *IEEE Trans. Ind. Electron.,* vol. 60, no. 2, pp. 681-690, Feb. 2013.

[126] P. Acuña, L. Morán, M. Rivera, R. Aguilera, R. Burgos, and V. G. Agelidis, "A Single-Objective Predictive Control Method for a Multivariable Single-Phase Three-Level NPC Converter-Based Active Power Filter," *IEEE Trans. Ind. Electron.,* vol. 62, no. 7, pp. 4598-4607, July 2015.

[127] J. Lee, H. Moon, and K. Lee, "An Improved Finite-Set Model Predictive Control Based on Discrete Space Vector Modulation Methods for Grid-Connected Three-Level Voltage Source Inverter," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 6, no. 4, pp. 1744-1760, Dec. 2018.

[128] F. Donoso, A. Mora, R. Cárdenas, A. Angulo, D. Sáez, and M. Rivera, "Finite-Set Model-Predictive Control Strategies for a 3L-NPC Inverter Operating With Fixed Switching Frequency," *IEEE Trans. Ind. Electron.,* vol. 65, no. 5, pp. 3954-3965, May 2018.

[129] Y. Yang, H. Wen, M. Fan, M. Xie, and R. Chen, "Fast Finite-Switching-State Model Predictive Control Method Without Weighting Factors for T-Type Three-Level Three-Phase Inverters," *IEEE Trans. Ind. Inf.,* vol. 15, no. 3, pp. 1298-1310, March 2019.

[130] D. Zhou, C. Jiang, Z. Quan, and Y. R. Li, "Vector Shifted Model Predictive Power Control of Three-Level Neutral-Point-Clamped Rectifiers," *IEEE Trans. Ind. Electron.,* to be published, doi: 10.1109/TIE.2019.2946549

[131] X. Xing, C. Zhang, J. He, A. Chen, and Z. Zhang, "Model Predictive Control for Parallel Three-Level T-Type Grid-Connected Inverters in Renewable Power Generations," *IET Renewable Power Generation,* vol. 11, no. 11, pp. 1353-1363, 13 9 2017.

[132] X. Wang, J. Zou, L. Ma, J. Zhao, C. Xie, K. Li, L. Meng, and J. M. Guerrero, "Model Predictive Control Methods of Leakage Current Elimination for a Three-Level T-Type Transformerless PV Inverter," *IET Power Electronics,* vol. 11, no. 8, pp. 1492-1498, 10 7 2018.

[133] R. Errouissi, and A. Al-Durra, "Design of PI Controller Together With Active Damping for Grid-Tied LCL-Filter Systems Using Disturbance-Observer-Based Control Approach," *IEEE Trans. Ind. Appl.,* vol. 54, no. 4, pp. 3820-3831, July-Aug. 2018.

[134] N. M. Abdel-Rahim, and J. E. Quaicoe, "Analysis and Design of a Multiple Feedback Loop Control Strategy for Single-Phase Voltage-Source UPS Inverters," *IEEE Trans. Power Electron.,* vol. 11, no. 4, pp. 532-541, July 1996.

[135] L. Poh Chiang, and D. G. Holmes, "Analysis of Multiloop Control Strategies for LC/CL/LCL-filtered Voltage-Source and Current-Source Inverters," *IEEE Trans. Ind. Appl.,* vol. 41, no. 2, pp. 644-654, March-April 2005.

[136] J. He, and Y. W. Li, "Generalized Closed-Loop Control Schemes with Embedded Virtual Impedances for Voltage Source Converters with LC or LCL Filters," *IEEE Trans. Power Electron.,* vol. 27, no. 4, pp. 1850-1861, April 2012.

[137] G. L. Calzo, A. Lidozzi, L. Solero, and F. Crescimbini, "LC Filter Design for On-Grid and Off-Grid Distributed Generating Units," *IEEE Trans. Ind. Appl.,* vol. 51, no. 2, pp. 1639-1650, March-April 2015.

[138] Z. Li, C. Zang, P. Zeng, H. Yu, S. Li, and J. Bian, "Control of a Grid-Forming Inverter Based on Sliding-Mode and Mixed H_2 / H_∞ Control," *IEEE Trans. Ind. Electron.,* vol. 64, no. 5, pp. 3862-3872, May 2017.

[139] P. A. Dahono, "A Control Method to Damp Oscillation in the Input LC Filter," *2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No.02CH37289),* Cairns, Qld., Australia, 2002, pp. 1630-1635 vol.4.

[140] P. Cortes, G. Ortiz, J. I. Yuz, J. Rodriguez, S. Vazquez, and L. G. Franquelo, "Model Predictive Control of an Inverter With Output *LC* Filter for UPS Applications," *IEEE Trans. Ind. Electron.,* vol. 56, no. 6, pp. 1875-1883, June 2009.

[141] W. Wu, Y. He, T. Tang, and F. Blaabjerg, "A New Design Method for the Passive Damped LCL and LLCL Filter-Based Single-Phase Grid-Tied Inverter," *IEEE Trans. Ind. Electron.,* vol. 60, no. 10, pp. 4339-4350, Oct. 2013.

[142] W. Wu, Y. Liu, Y. He, H. S. Chung, M. Liserre, and F. Blaabjerg, "Damping Methods for Resonances Caused by LCL-Filter-Based Current-Controlled Grid-Tied Power Inverters: An Overview," *IEEE Trans. Ind. Electron.,* vol. 64, no. 9, pp. 7402-7413, Sept. 2017.

[143] C. Bao, X. Ruan, X. Wang, W. Li, D. Pan, and K. Weng, "Step-by-Step Controller Design for LCL-Type Grid-Connected Inverter with Capacitor–Current-Feedback Active-Damping," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1239-1253, March 2014.

[144] Z. Qing-Chang, and H. Tomas, *Control of Power Inverters in Renewable Energy and Smart Grid Integration*. Chichester, West Sussex: John Wiley & Sons, 2012.

[145] S. Golestan, and J. M. Guerrero, "Conventional Synchronous Reference Frame Phase-Locked Loop is an Adaptive Complex Filter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1679-1682, March 2015.

[146] P. Rodríguez, R. Teodorescu, I. Candela, A. V. Timbus, M. Liserre and F. Blaabjerg, "New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions," *2006 37th IEEE Power Electronics Specialists Conference*, Jeju, 2006, pp. 1-7.

[147] T. Remus, L. Marco, and R. Pedro, *Grid Converters for Photovoltaic and Wind Power Systems*. Chichester, West Sussex: John Wiley & Sons, 2011.

[148] Escala Calame, E. A. (2019). *Local and central controllers for microgrids*. *Theses and Dissertations*, Retrieved from https://scholarworks.uark.edu/etd/3193.

[149] S. Vazquez *et al*., "Model Predictive Control for Single-Phase NPC Converters Based on Optimal Switching Sequences," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7533-7541, Dec. 2016.

[150] Y. Yang, H. Wen, M. Fan, M. Xie, R. Chen, and Y. Wang, "A Constant Switching Frequency Model Predictive Control Without Weighting Factors for T-Type Single-Phase Three-Level Inverters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5153-5164, July 2019.

[151] W. Alhosaini and Y. Zhao, "A Model Predictive Voltage Control using Virtual Space Vectors for Grid-Forming Energy Storage Converters," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019, pp. 1466-1471.

[152] W. Alhosaini, Y. Wu and Y. Zhao, "An Enhanced Model Predictive Control Using Virtual Space Vectors for Grid-Connected Three-Level Neutral-Point Clamped Inverters," in *IEEE Trans. Energy Convers.*, vol. 34, no. 4, pp. 1963-1972, Dec. 2019.

[153] W. Alhosaini, M. H. Mahmud and Y. Zhao, "Fast and Secure Operation of Voltage Source Inverter based DERs using Model Predictive Droop Control," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, 2018, pp. 1035-1042.

[154] J. Pou, R. Pindado, D. Boroyevich, and P. Rodriguez, "Evaluation of the Low-Frequency Neutral-Point Voltage Oscillations in the Three-Level Inverter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 6, pp. 1582-1588, Dec. 2005.

[155] S. Busquets-Monge, J. Bordonau, D. Boroyevich, and S. Somavilla, "The Nearest Three Virtual Space Vector PWM - A Modulation for the Comprehensive Neutral-Point Balancing in the Three-Level NPC Inverter," *IEEE Power Electron. Lett.,* vol. 2, no. 1, pp. 11-15, March 2004.

[156] Z. Wang, Y. Wu, M. H. Mahmud, Z. Zhao, Y. Zhao, and H. A. Mantooth, "Design and Validation of A 250-kW All-Silicon Carbide High-Density Three-Level T-Type Inverter," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 8, no. 1, pp. 578-588, March 2020.

[157] "Cree CAS325M12HM2 1.2 kV, 3.7 mΩ All-Silicon Carbide High-Performance, Half-Bridge Module C2M MOSFET and Z-RecTM Diode," https://www.wolfspeed.com/, Accessed: April, 19, 2020.

[158] L. M. A. Caseiro, A. M. S. Mendes, and S. M. A. Cruz, "Dynamically Weighted Optimal Switching Vector Model Predictive Control of Power Converters," *IEEE Trans. Ind. Electron.,* vol. 66, no. 2, pp. 1235-1245, Feb. 2019.

[159] W. Alhosaini, F. Diao, M. H. Mahmud, Y. Wu and Y. Zhao, "A Virtual Space Vectors based Model Predictive Control for Inherent DC Link Voltage Balancing of Three-Level T-Type Converters," *IEEE J. Emerg. Sel. Topics Power Electron*. "submitted for review".

[160] T. Tsang-Li, and C. Jian-Shiang, "UPS Inverter Design Using Discrete-Time Sliding-Mode Control Scheme," *IEEE Trans. Ind. Electron.,* vol. 49, no. 1, pp. 67-75, Feb. 2002.

[161] G. Willmann, D. F. Coutinho, L. F. A. Pereira, and F. B. Libano, "Multiple-Loop H-Infinity Control Design for Uninterruptible Power Supplies," *IEEE Trans. Ind. Electron.,* vol. 54, no. 3, pp. 1591-1602, June 2007.

[162] G. Escobar, P. Mattavelli, A. M. Stankovic, A. A. Valdez, and J. Leyva-Ramos, "An Adaptive Control for UPS to Compensate Unbalance and Harmonic Distortion Using a Combined Capacitor/Load Current Sensing," *IEEE Trans. Ind. Electron.,* vol. 54, no. 2, pp. 839-847, April 2007.

[163] L. F. A. Pereira, J. V. Flores, G. Bonan, D. F. Coutinho, and J. M. G. d. Silva, "Multiple Resonant Controllers for Uninterruptible Power Supplies—A Systematic Robust Control Design Approach," *IEEE Trans. Ind. Electron.,* vol. 61, no. 3, pp. 1528-1538, March 2014.

[164] Y. Wu, and Y. Ye, "Internal Model-Based Disturbance Observer With Application to CVCF PWM Inverter," *IEEE Trans. Ind. Electron.,* vol. 65, no. 7, pp. 5743-5753, July 2018.

[165] H. T. Nguyen, E. Kim, I. Kim, H. H. Choi, and J. Jung, "Model Predictive Control With Modulated Optimal Vector for a Three-Phase Inverter With an LC Filter," *IEEE Trans. Power Electron.,* vol. 33, no. 3, pp. 2690-2703, March 2018.

[166] B. Majmunović, T. Dragičević, and F. Blaabjerg, "Multi Objective Modulated Model Predictive Control of Stand-Alone Voltage Source Converters," *IEEE J. Emerg. Sel. Topics Power Electron.,* to be published, doi: 10.1109/JESTPE.2019.2925603.

[167] X. Li, H. Zhang, M. B. Shadmand, and R. S. Balog, “Model Predictive Control of a Voltage-Source Inverter With Seamless Transition Between Islanded and Grid-Connected Operations,” *IEEE Trans. Ind. Electron.,* vol. 64, no. 10, pp. 7906-7918, Oct. 2017.