FACULTY OF INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING

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MASTER'S THESIS

RF POWER AMPLIFIER DESIGN OPTIMIZATION USING MEASUREMENT DATA AND STATISTICAL METHODS

Author	Elina Autio
Supervisor	Risto Vuohtoniemi
Second Examiner	Aarno Pärssinen
Technical Advisor	Antti Heiskanen

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ABSTRACT

Constantly growing number of mobile data users, and thus the mobile data, creates challenges for spectral efficient data transmission. A high data throughput of a base station requires linear modulation methods and broadband signals. Radio frequency (RF) power amplifier (PA) as a part of base station has an important role making the output signal of the transceiver as linear and spectral efficient as possible. The key RF parameters such as peak power, efficiency, linearity and gain suffer from productional variety which needs to be taken into account in design process. In this thesis, the RF PA design is optimized to tolerate the productional variety of certain RF parameters.

The effects of productional variety are pre-analyzed by building the design using corner sample transistors. The build consists of seven different PA module versions where the RF transistor's internal matchings are modified. The best information of the PA performance is gathered from measurement results and therefore, the presented design optimization method is based on hardware measuring and tuning. Measurement results are compared to self-defined specification limits of each RF parameter and to the nominal version. Another method for analyzing a build which aims for illustrating large population of PA modules is statistical analysis. Along with the help of process capability index C_{pk}, the statistical behavior compared to the specification limits is evaluated.

Peak power proved to be the optimized parameter. Changing the biasing of the transistor and tuning the external input matching network, the peak power results increased. The measurement results proved that the RF PA design is optimized to tolerate the productional variety better with the design optimization method presented in this thesis.

Key words: Doherty, corner sample, productional variety, process capability index.

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TIIVISTELMÄ

Mobiilidatan käyttäjien, ja siten myös mobiilidatan määrä on jatkuvasti kasvussa, mikä luo haasteita spektritehokkaaseen datansiirtoon. Tukiaseman suuri datansyöttö vaatii laajakaistaisia signaaleja sekä lineaarisia modulointimenetelmiä. RF-tehovahvistimella on siis tärkeä rooli tukiaseman osana saada lähtösignaalista mahdollisimman lineaarinen ja spektritehokas. Tehovahvistimen RF-parametrit, kuten huipputeho, hyötysuhde, lineaarisuus sekä vahvistus kärsivät tuotannollisesta vaihtelusta, kun tehovahvistinmoduulia aletaan tuottaa suuria määriä. Tämän opinnäytetyön tarkoituksena on optimoida RF-tehovahvistimen suunnittelu sellaiseksi, että se on sietokykyinen tiettyjen RF-parametrien tuotannolliselle vaihtelulle.

Tuotannollisen vaihtelun vaikutuksia analysoidaan etukäteen käyttämällä tehovahvistimessa kulmanäytetransistoria. Kulmanäytteet koostuvat seitsemästä erilaisesta versiosta, jossa RF-transistorin sisäisiä sovituksia on muunneltu. Paras tieto tehovahvistimen käyttäytymisestä saadaan mittaustuloksista, minkä takia työssä käytetään mittauksiin ja laitteiston hienosäätämiseen perustuvaa optimointimetodia. Kulmanäytteiden mittaustuloksia verrataan itse määrittelemiin RF-parametrien spesifikaatioihin sekä nominaaliversioon. Toinen analyysimetodi suuren tehovahvistinmoduulimäärän havainnollistamiseen on tilastollinen analyysi. Prosessin kyvykkyysindeksin C_{pk} analysoinnin kanssa, RF-parametrien tilastollinen käyttäytyminen spesifikaatiorajoihin verrattuna voidaan arvioida.

Huipputeho osoittautui optimoitavaksi parametriksi. Transistorin biasoinnin muutoksella sekä tulon ulkoisen sovituspiirin muokkauksella huipputehoa saatiin kasvatettua. Mittaustulokset osoittavat, että työssä esitetyllä suunnittelun optimointimetodilla tehovahvistin saatiin sietämään tuotannollista vaihtelua paremmin.

Avainsanat: Doherty, kulmanäyte, tuotannollinen vaihtelu, prosessin kyvykkyysindeksi.

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FOREWORD

This Master's Thesis was conducted at Bittium Oyj in Oulu, Finland. The purpose was to find a way to optimize the PA design to tolerate the productional variety by measuring and analyzing the data of corner samples.

I express my gratitude to Lic.Sc. (Tech.) Antti Heiskanen, whose invaluable guidance through the process helped to achieve the goal. I also want to thank Seppo Rousu for coming up with this topic along with the RF team for help and encouraging finishing the process.

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Last but definitely not least, special thanks go to my family, friends and my boyfriend Veli-Matti for constant support and encouragement through the time in the university and in life.

Oulu, Finland, October 2019

Elina Autio

LIST OF ABBREVIATIONS AND SYMBOLS

3GPP	3rd Generation Partnership Project
ACP	Adjacent Channel Power
AM-AM	Amplitude-to-Amplitude Conversion
AM-PM	Amplitude-to-Phase Conversion
DPD	Digital Predistortion
DSP	Digital Signal Processing
DUT	Device Under Test
EVM	Error Vector Magnitude
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GSM	Global System for Mobile Communications
HCI	Hot Carrier Injection
IBW	Instantaneous Bandwidth
LDMOS	Laterally Diffused Metal-Oxide-Semiconductor
LSL	Lower Specification Limit
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NB-IoT	Narrow Band Internet of Things
OFDM	Orthogonal Frequency-Division Multiplexing
PA	Power Amplifier
PAE	Power-Added Efficiency
PAPR	Peak-to-Average Power Ratio
PDF	Probability Distribution Function
PEP	Peak Envelope Power
R&D	Research and Development
RF	Radio Frequency
RMS	Root Mean Square
SEM	Spectral Emission Mask
USL	Upper Specification Limit
VDMOS	Vertical Double-diffused Metal-Oxide-Semiconductor
VSWR	Voltage Standing Wave Ratio
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying

A	Amplitude of a Signal
C_{GD}	Feedback Capacitance
C_{GS}	Gate-Source Capacitance
C_{pk}	Process Capability Index
G	Gain
e	Euler's Number, approximately 2.71828
I_D	Drain Current
K	Voltage Gain
P_{DC}	Power of DC Supply

P_{IN}	Input Power Level
P_{main}	Peak Power of Main Branch Amplifier
$P_{peaking}$	Peak Power of Peaking Branch Amplifier
P_{RF}	RF Power at the output of PA
$P_{sat,\ main}$	Saturation Power of Main Branch Amplifier
$P_{sat,\ peaking}$	Saturation Power of Peaking Branch Amplifier
V_{GS}	Gate-Source Voltage
$V_{in}(t)$	Input Voltage at a Time t
V_{TH}	Threshold Voltage
$V_{out}(t)$	Output Voltage at a Time t
Z_1	Output Impedance
Z_L	Load Impedance
Z_M	Main Branch Impedance
Z_P	Peaking Branch Impedance
Z_T	Quarter Wave Transmission Line Impedance
Z_{TH}	Thermal Impedance
α	Power-Division Ratio
β	Saturated Power Ratio
η	Efficiency
ω	Angular Frequency
μ	Mean of Values
μ_L	Mean of Logarithmic Values
$\hat{\mu}$	Estimated Mean of a Process
θ_M	Offset Line of Main Branch
θ_P	Offset Line of Peaking Branch
σ	Standard Deviation of Values
σ_L	Standard Deviation of Logarithmic Values
$\hat{\sigma}$	Estimated Standard Deviation of a Process
π	Pi, Approximately 3.14159

dB	Decibel
dBc	Decibel Compared to Carrier Level
dBm	Decibel Relative to Milliwatt
MHz	Megahertz
V	Volt
W	Watt

1 INTRODUCTION

RF PA has an important role in modern communication systems. As any communication system consists of a transmitter and a receiver, the transmitted signal has to be linear and powerful enough to be detected by a receiver. RF PA is located at the front-end of transmitter side before a filter and an antenna having one of the most important tasks in signal transmission: amplify the transmitted signal with no errors in signal quality. Judging from the purpose of base station RF PA, it is the most power consuming part of a radio system. Therefore, the efficiency is a critical parameter to be taken into account when designing a good RF PA. Peak power is another critical parameter which has an effect to the efficiency and linearity.

These parameters along with the PA line-up gain and linearity direct the RF PA design process. Roughly, the RF PA design process can be divided into simulation-based process and measurement-based process. While these two processes improve each other together and is often used, the chosen design optimization method in this thesis is based on the feedback from measurement results of hardware and component tuning. The set of measured RF PA modules are called corner samples which are supposed to illustrate the expected productional variance of RF PA performance. Internal matchings of final stage transistor are tuned in order to achieve the expected productional variance. The most essential performance parameters are analyzed and compared to their specification requirements and the nominal RF PA version. Also, the statistical behavior of performance parameters is investigated. The device under test (DUT) operates in Long Term Evolution (LTE) system frequency band 7 (2600 MHz). LTE system support multiple input multiple output (MIMO) technique which is the basis of operative and upcoming network systems.

The reason for choosing the hardware tuning and measurement-based design process originates from many different parts which effects on the whole project. While the DUT is required to operate on 60 W and 40 W modes, the amount of testable combinations of supply voltage and output power is large. Datasheets and some components might be deficient research and development –versions (R&D) until the product is ready for production which means that there are no simulation models for immature components. The necessity of active collaboration with RF transistor manufacturers, for instance, is important. Scheduling of measuring different builds of the product comes up with importance, too. As a conclusion, the challenge in this design process is to ensure the PA module design changes further in achieving the goal of productional and long-living base station product in a tight project schedule.

2 RF POWER AMPLIFIER ROLE AND DESIGN CHALLENGES WITHIN HIGH POWER MULTISTANDARD BASE STATION

The amount of mobile equipment and users is constantly growing which naturally raises the amount of mobile data. Usually, the base station is sold to the operator with low power consumption and a high data throughput. The frequency allocation for a single operator is tight at the radio frequencies which means that the operator aims for a high data throughput per hertz. There are many different standards and technologies along with LTE, such as Global System for Mobile Communications (GSM) and Narrow Band Internet of Things (NB-IoT) which mean many ways of modulating and demodulating the signal. For example, NB-IoT is not able to transfer the same amount of bits per hertz than a signal with Quadrature Amplitude Modulation (QAM) method of 64 different symbols in LTE. Different equipment support different standards, and therefore, the base station should fulfill the 3rd generation partnership project (3GPP) standards in type approval in order to provide value for operators and their customers. Also, operators set their own requirements for the base station, for example in cell planning aspects.

There are many perspectives how the base station requirements define the PA requirements. A high data throughput requires broadband signals and linear modulation methods meaning a high signal peak-to-average power ratio (PAPR). 3GPP standardization sets requirements for the output signal at the antenna connector interface, which sets in turn the requirements for RF PA, in order to guarantee undisturbed operation in adjacent frequency bands of different operators as well as an adequate quality of service. Promised instantaneous bandwidth (IBW) of the base station is 70 MHz which means that the PA must be able to linearize multicarrier signal up to 70 MHz, not forgetting other LTE carriers with bandwidths of 5 MHz, 10 MHz and 20 MHz. As the base station is required to operate between the ambient temperature range of -40 °C to +55 °C, the RF PA with its components must tolerate extreme temperatures. The maximum supportable root mean square (RMS) output power is 60 W from the output of one antenna connector and hence the peak power is PAPR above that. System calculations take into account the performance of linearization and filtering and thus provide the specification for the PA module. The block before the PA in Figure 1 is digital pre-distortion (DPD) which is used to linearize the transmitted signal. The losses of filter and antenna are taken into account in defining the output power target for the PA in different use scenarios which means that 60 W output power is not binding for the PA module. [1][2]

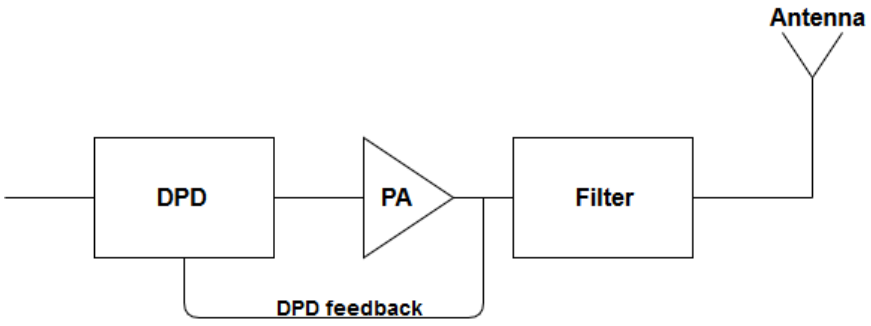

Figure 1. The block diagram of transmitter RF front-end.

The purpose of RF power amplifier is to amplify the signal for radio transmission aiming for linear operation. Essential performance parameters such as peak power, efficiency, gain and adjacent channel power (ACP) need to meet the target specification while the power amplifier can be linearized to the target spectral purity. PA design procedure usually means finding a balance between the most essential performance parameters. Design challenges with the PA are various since PA itself is a non-linear part in RF transmitter and the transmitter signal gets corrupted by non-linearities. The best efficiency and the worst linearity for the RF power transistor are typically achieved at peak power situation which is not constantly active. Due to high PAPR of the target signal, the overall power efficiency is challenging to achieve since the signal remains below the peak power situation most of the time. LTE uses a digital modulation method called Orthogonal Frequency-Division Multiplexing (OFDM). In OFDM, carrier signal consists of multiple subcarriers that are QAM-modulated. QAM combines linearly both phase and amplitude modulation. This requires linear transceiver. There is usually a number in front of abbreviation QAM which tells how many different values one symbol can have and of how many bits the symbol consists. The higher the QAM value is and the more subcarriers there is, the higher PAPR and tighter error vector magnitude (EVM) requirement power amplifier must be able to handle. Wide signal bandwidths are challenging for the PA, too. The wider the bandwidth is, the wider are the intermodulation distortion signals. Wideband signals are naturally sensitive to gain and phase variations which may cause problems in gain and phase ripples. Also, the delays in video signal processing and detection have become tougher as the signal bandwidths have increased.

2.1 Power amplifier operating classes and architectures

Since the requirements for the essential performance parameters need to be fulfilled, the power amplifier architecture must be suitable for providing the specified performance. Though, not any architecture can be used in base station operation. Together with optimal biasing and PA architecture the efficiency, gain and peak power can be achieved and optimized. In this chapter the optimal operation classes and architectures for the designed PA are described.

2.1.1 Operating classes

A linear power amplifier can be perceived as an ideal amplifier which does not create any amplitude and phase errors within the used frequency band to the signal at the output of PA. With equation (1) the linear output response $V_{out}(t)$ at a time can be defined as

$$V_{out}(t) = K \cdot V_{in}(t), \quad (1)$$

where K is the voltage gain of the amplifier and $V_{in}(t)$ is the input voltage as a function of time.

Class A amplifier can be defined as a linear amplifier in its classical manner. A device is linear in the region between cutoff and saturation, as Figure 2 shows input voltage-output current –curve [2]. Cutoff is a region where the input voltage has not crossed transistor's threshold voltage V_{TH}. Saturation is a region where the maximum current is achieved even though the gate bias voltage increases. The solid line represents an ideal nonlinear response whereas the dotted line represents a realistic nonlinear response. If the PA is designed to have

a bias point from the middle of the linear region, theoretically the linear operation is achieved. At the same time, the RF matching can make the PA nonlinear. If the load is too big, the drain voltage swing becomes too big causing the breaking the transistor's current due to drain-source voltage. [2]

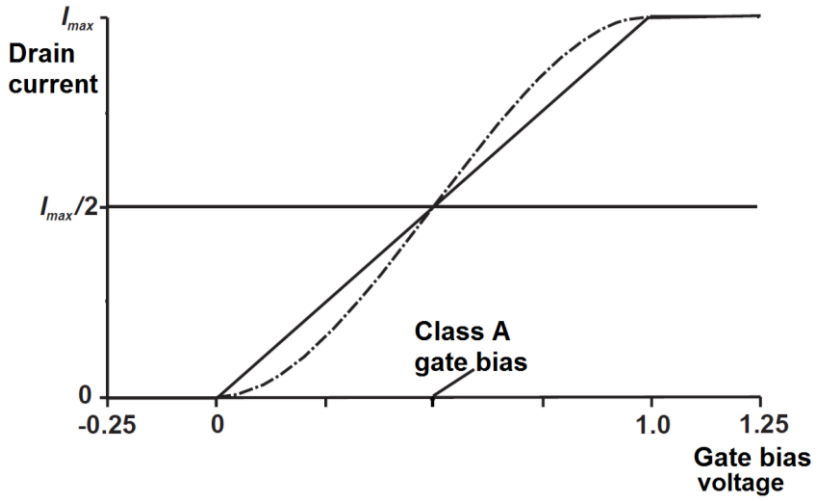

Figure 2. The linear operation can be found from ideal behavior of class A power amplifier.

However, non-linearity is the dominant nature for PA. Together with bias point, RF matching and suitable input drive the linearity is achieved. Bias point and conduction angle determines the operating class along with the RF matching and input drive. Bias point is an adjusted condition of gate voltage V_{GS} which as for adjusts drain current I_D. The conduction angle determines the part of the RF signal when the transistor is active and consumes power. RF power amplifiers can be divided in either current conducting or switching mode. Current conducting mode includes classes from A to C and all their variants whereas switching mode includes classes E, F and many variants. There are many different classes for bias point, but the classes A, B, AB and C are constitutive for the DUT.

The operation of class AB can be understood better by knowing the operation of classes A and B. Class A amplifier has the conduction angle of 360° and it is biased to operate in the linear region meaning that drain current flows all the time when input signal drives the output current. Therefore, the main disadvantage is that the transistor never turns off and consequently, theoretical maximum for peak power efficiency is 50 % [3]. The bias point of class B amplifier is set in a way that drain current is practically zero which means that transistor consumes power on the positive halves of the input signal. Since the power consumption happens on the input signal's positive halves, the conduction angle is 180°. In the case of class B amplifier, theoretical maximum for peak power efficiency reaches the value of 78.5 % [3]. Comparing to the class A amplifier, class B manages better with efficiency but with the cost of linearity. The output matching is needed in order to filter the distortion components out created by nonlinearity and achieve the linear output. [3]

Class AB amplifier is a compromise with classes A and B amplifiers trying to achieve good linearity with smaller power consumption. The operating point is set in a way that the current flows through a transistor in the DC-state but consumption is much less than with class A amplifier. With small input signal levels, class A amplifier acts as linear amplifier. When the input signal level is increased, the drain current begins to cut in the bottom of the sine wave due to the bias point of transistor as the Figure 3 presents. The conduction angle

varies between 180° and 360° while the theoretical maximum for peak power efficiency varying between 50 % and 78.5 % both depending on the biasing. [3]

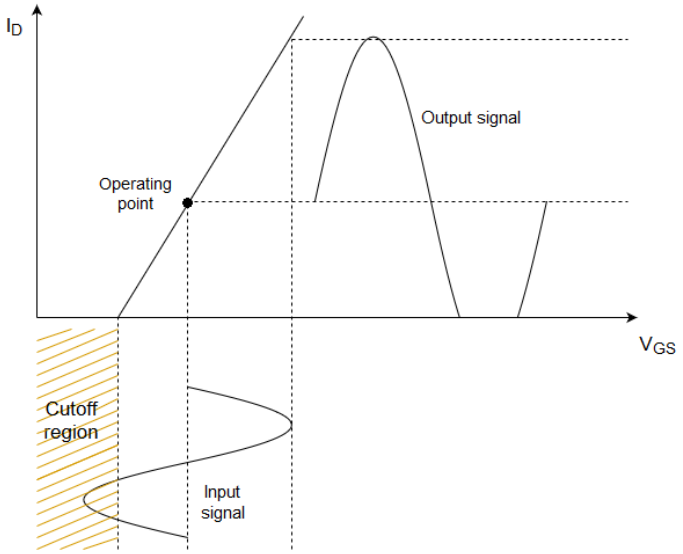

Figure 3. Operation of class AB amplifier.

The operation of class C amplifier is presented in Figure 4. The operation point is set below the threshold voltage of V_{GS}. In other words, class C amplifier starts operating when the amplifier has been driven to its cutoff region meaning that the amplifier does not operate in DC-state. The conduction angle is below 180°. The linearity is worse with class C amplifier when comparing it to class AB amplifier while efficiency remains good. This amplifier type is suitable for a peaking amplifier in the Doherty structure. [3]

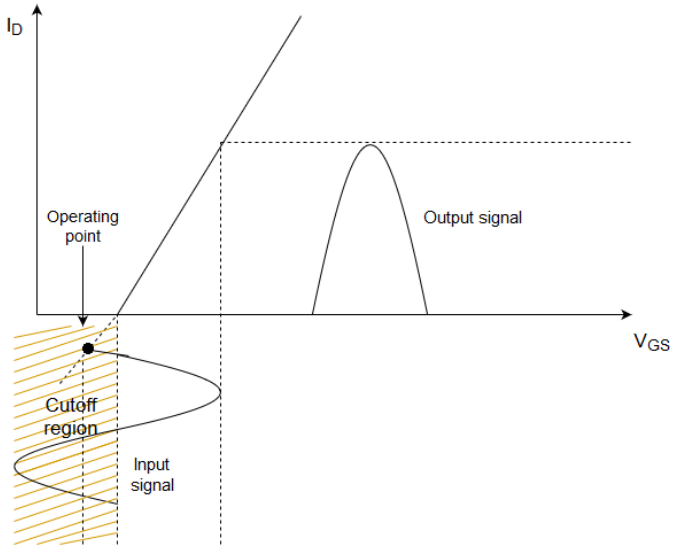

Figure 4. Operation of class C amplifier.

2.1.2 Power amplifier architectures

The most common amplifier topology is single-ended amplifier which amplifies only half of the input signal. Reference point with this amplifier type is normally ground and it acts as a return path for signal. If there is an error in the signal, ground will not be effected by the error and the error is forwarded. Therefore, single-ended architectures need complex error cancellation techniques to reject the signal variations. Single-ended signals are vulnerable to electromagnetic coupled interference and noise. Inspection of input and output voltages clarifies better the operation principle of single-ended amplifier. Equation (2) presents the input signal at a time t [4]

$$V_{in}(t) = A \cdot \cos \omega t, \tag{2}$$

where A is the amplitude of the signal and ω is the angular frequency. Equation (3) gives an output signal which is a sum of multiplication of voltage gain and input signal [4]

$$V_{out}(t) = \sum_{n=0}^{\infty} K_n \cdot V_{in}(t)^n,\ n = 0, 1, 2\ldots \tag{3}$$

where n is the order of nonlinearity and K_n is the voltage gain. When (2) is inserted to (3) and the sum is calculated, the output signal

$$V_{out}(t) = \left(K_0 + \frac{A^2 \cdot K_2}{2}\right) + \left(K_1 + \frac{3 \cdot A^3 \cdot K_3}{4}\right) \cos \omega t + \left(\frac{A^2 \cdot K_2}{2}\right) \cos 2\omega t + \left(\frac{A^3 \cdot K_3}{4}\right) \cos 3\omega t + \ldots \tag{4}$$

is achieved. Here the input signal is single-toned. Situation with multitoned signals is more complex. One can see that all nonlinearities have a constant which are dependent on the input signal amplitude and voltage gain. As the final stage gain is wanted to be as high as possible, this amplifier structure assures high nonlinearities.

Differential amplifier has two inputs and outputs and therefore, two operation modes. In common mode, the input signals change simultaneously in the same direction. In differential mode, the input signals have equal but opposite amplitudes around the reference point. The purpose of differential amplifier is to amplify the voltage difference between two input signals. Errors in differential signals will be cancelled out since the reference point is not constant. Compared to the single-ended structure, differential structure has an advantage of twice the composite signal swing on the same power supply which increases signal-to-noise ratio. In other words, amplifier has more headroom with the same power supply lowering distortion. The scrutiny of input and output signals helps understanding the operation principle of this amplifier structure. Equation (5) [4]

$$V_{in}^{+}(t) = A \cdot \cos \omega t \tag{5}$$

presents the input signal with positive amplitude. Oppositely, equation (6) [4]

$$V_{in}^{-}(t) = -A \cdot \cos \omega t \tag{6}$$

presents the input signal with negative amplitude. When it comes to the output signal [4]

$$V_{out}(t) = \sum_{n=0}^{\infty} [K_n \cdot V_{in}^{+}(t)^n - K_n \cdot V_{in}^{-}(t)^n]\ ,\ n = 0, 1, 2, \ldots \tag{7}$$

it is a sum of subtraction of positive and negative amplitude input signals multiplied by the voltage gain. Output signal of differential amplifier

$$V_{out}^{+}(t)\text{-}V_{out}^{-}(t)=(0)\text{-}\left(2\cdot A\cdot K_1+\frac{3\cdot A^3\cdot K_3}{2}\right)\cos\omega t+(0)\cos 2\omega t\text{-}\left(\frac{A^3\cdot K_3}{2}\right)\cos 3\omega t+\ldots \quad (8)$$

is achieved when input equations (5) and (6) are inserted to output sum equation (7). As the equation (8) shows, even order nonlinearities are cancelled out in differential structure.

Balanced structure is presented in Figure 5 and used in driver stage, which will be described later. The input signal is split into two different phased signals with quadrature 3 dB (90°) hybrid and then fed into two identical amplifiers. Then, amplifier outputs are recombined with a similar hybrid. An advantage of this structure is that reflections from the amplifiers are cancelled at the RF input and output ports. Also, the match seen at the input and output port is perfect as long as the amplifiers and paths through the amplifier are identical. Due to this, the structure enables designing gain "modules" which has imperfect and flat voltage standing wave ratio (VSWR) characteristics over a wide bandwidth. Balanced amplifiers work as a highly effective power combiner which means that the design needs twice the space compared to single-ended design. The cost is also higher, and the structure is usually noisier than single-ended structure due to twice the number of components. [1]

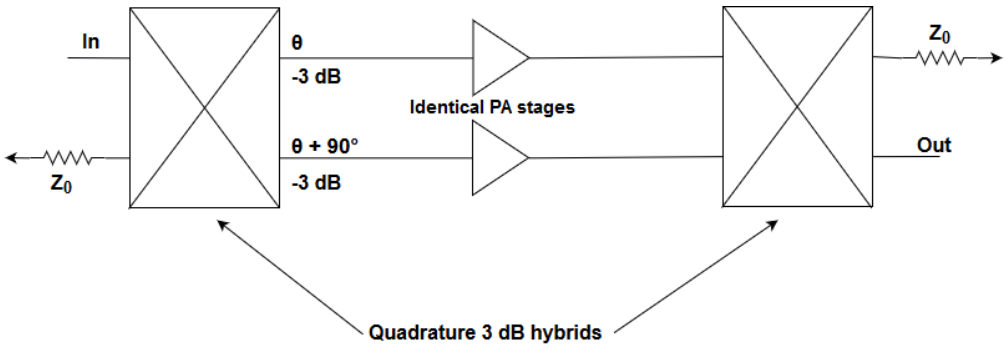

Figure 5. Balanced power amplifier structure.

2.2 Doherty topology

Doherty topology was introduced first in year 1936 by William H. Doherty and nowadays, this topology is widely used in base station power amplifiers. An active load-pull technique, sometimes also called load modulation technique, is the operational concept of Doherty amplifier. The conventional two-way symmetric Doherty has two amplifiers (transistors) in their own branches. The main amplifier, which usually holds the class AB, conducts on low power levels. As the power level is increased enough, class C or deep class AB peaking amplifier joins to the amplification while increasing the linear operation region and efficiency. Also, there are quarter wave transformers before the peaking amplifier and after the main amplifier before the combination of branches. Branches are combined at the end and fed to the 50 ohm load through a matching network. An active load-pull technique is made possible with the quarter wave transformer at the main amplifier branch. The load impedance the main and peaking amplifier sees changes with relation to the operational power level. In other words, when the peaking amplifier is turned on, both amplifiers experience the load

modulation. Therefore, the power efficiency can be expanded to the lower backoff power level. As mentioned earlier, the spectrum efficient modulation methods mean a high PAPR for the signal, which requires a large linear operation region from the amplifier. The main purpose of this power amplifier type is to improve the efficiency at backoff power levels by combining the outputs of *N* power amplifiers through an impedance-inverting network. [2]

The operation principle of two-stage symmetric Doherty topology is illustrated in Figure 6. By the symmetric topology it is meant that the power ratings of main and peaking amplifiers are equal. At the left hand side (a) the voltage over the load is observed as function of input voltage whereas on the middle (b) the current over the load is observed. At the right hand side (c) the operation is observed how the output power behaves as the function of input power. Generally, the threshold between low-drive and load-pull region is -6 dB from the maximum output power. This is called 6 dB backoff point. In voltage-level it means half of the maximum input power and in current-level a fourth of maximum device current. The latter is the maximum achievable current in the low-drive region. In the low-drive region, the peaking amplifier is turned off while main amplifier operates in its active region. As the threshold is crossed and load-pull region is reached while increasing the input voltage, the peaking amplifier activates while main amplifier attains its saturation region. In other words, the collector efficiency of main amplifier reaches its maximum value at the 6 dB backoff point, whereas peaking amplifier's collector efficiency reaches its maximum value at the peak-envelope power (PEP). Here, both amplifiers are saturated. In the graph c, the curves of main and peaking amplifiers are combined to see the linear operation of Doherty amplifier. [2][3]

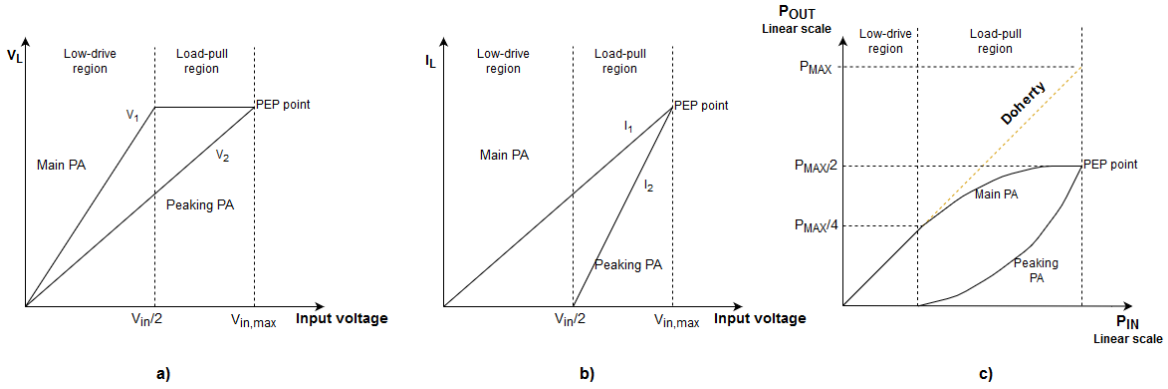

Figure 6. The operation principle of Doherty structure.

Efficiency is an interesting parameter to be observed in Doherty analysis. Figure 7 represents how it behaves as function of backoff power level. Comparison is done with efficiency of class B amplifier. Doherty amplifier reaches its first maximum efficiency at 6 dB backoff level whereas class B amplifier reaches it when there is no backoff.

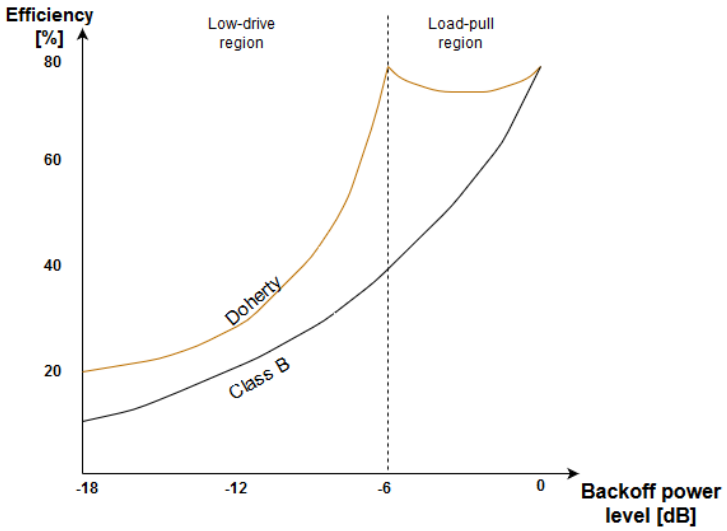

Figure 7. Efficiency comparison between Doherty and class B amplifier.

2.2.1 Inverted asymmetric Doherty structure

Since the theoretical 6 dB backoff of a conventional Doherty is not optimal for high signal PAPR, more backoff from the amplifier is needed which is achieved by an asymmetric Doherty structure. By the term "asymmetric" it is meant that main and peaking amplifiers have different power ratings. In other words, higher efficiency is achieved with smaller input power level. The backoff level is defined by a power-division ratio α described in equation (9)

$$\alpha = \frac{P_{\text{main}}}{P_{\text{peaking}}}, \tag{9}$$

where P_{main} is the peak power of main amplifier and P_{peaking} is the peak power of peaking amplifier. Even though the asymmetrical Doherty structure offers an improvement in efficiency, it comes with cost of redundancy of total power gain due to the insertion loss of input's N-way power divider. Also, there is inserted loss in the output matching network of main branch, which is reduced by the inverted Doherty structure. [3]

Therefore, the inverted asymmetric Doherty structure is a potential solution for improving the efficiency of the power amplifier. This structure is used in the measured PA modules due to the target signal nature where the root mean square (RMS) power of the signal is roughly the value of PAPR below the peak power. Most of the efficiency comes from the main branch and therefore, the loss of the main branch must be minimized. The loss minimization is made by shifting the load modulation to the peaking branch with the quarter wave transmission line. Figure 8 presents the structure of two-way inverted asymmetric Doherty amplifier with impedances. When comparing this structure to the conventional one, the electric length of output matching network of main branch has reduced in inverted asymmetric structure. [5]

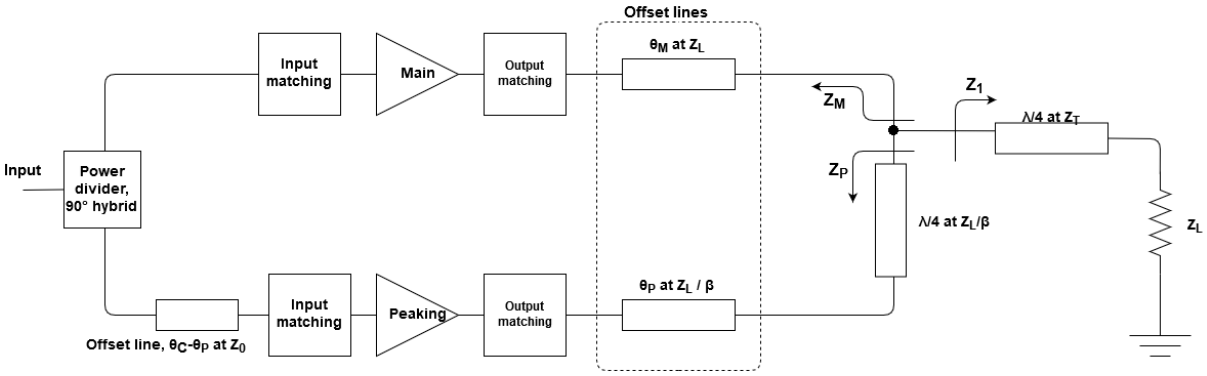

Figure 8. Structure of two-way inverted asymmetric Doherty amplifier.

The analysis of inverted asymmetric structure can be done with help of Figure 8. Equation (10) defines the saturated power ratio β

$$\beta = \frac{P_{\text{sat, peak}}}{P_{\text{sat, main}}}, \tag{10}$$

where $P_{\text{sat, peak}}$ is the saturation power of the peaking amplifier and $P_{\text{sat, main}}$ is the saturation power of the main amplifier. Z_1 is the output impedance at the junction of both branches when the input power is at its maximum. The output impedance is defined as

$$Z_1 = \frac{Z_{\text{L}}}{1+\beta}, \tag{11}$$

where Z_{L} is the load impedance. Therefore, the characteristic impedance of output quarter wave transmission

$$Z_{\text{T}} = \sqrt{Z_1 \cdot Z_{\text{L}}} \tag{12}$$

can be defined.

The output impedance of peaking branch Z_{P} is an open circuit at low power levels. In other words, the impedance before the quarter wave transmission line equals to zero ohms while Z_{P} equals to infinity. In theory, by tuning the offset line of peaking branch θ_{P} between the peaking amplifier and quarter wave transmission line the power leakage is prevented since the impedances sum coherently. Now, the output impedance of main branch Z_{M} equals to Z_1 which should be matched to the output impedance of the device by tuning the offset line θ_{M} which provides the optimum efficiency.

When the input power level is increased to the load-pull region and the peaking amplifier is turned on, the main amplifier is saturated to keep the efficiency as high as possible while peaking amplifier is providing the additional needed power. As the input power is being increased, the impedances are changing all the time and when the input power has reached its maximum value, the device is fully saturated and the impedances of main and peaking branches are defined with new values. The output impedance of the main branch is now the same as the load impedance Z_{L} while the output impedance of the peaking branch is Z_{L} divided by β. Output matching networks in both branches are meant to assure the optimum matching between the transistor's drain and offset line. The offset line in the beginning of

peaking branch has a function of compensating the phase difference between the main and peaking branches. It also maximizes the saturated power and compensates the phase difference between branches. The equation (13)

$$Z_M = \begin{cases} Z_1, \text{ when the peaking amplifier does not operate} \\ Z_L, \text{ when the peaking amplifier operates} \end{cases} \quad (13)$$

concludes the operation of main branch at the points when peaking amplifier is operating and when it is not. Equation (14)

$$Z_P = \begin{cases} \infty, \text{ when the peaking amplifier does not operate} \\ \frac{Z_L}{\beta}, \text{ when the peaking amplifier operates} \end{cases} \quad (14)$$

concludes the operation of peaking branch on its side. [5]

Main and peaking amplifiers are not fully isolated from each other in Doherty structure resulting a problem to design the optimum load impedance shift to both transistors for high efficiency, peak power or gain. It is impossible to achieve all these parameters simultaneously and therefore, a compromise in matching must be made for the most critical parameter. This supports the use of the hardware tuning and measurement method. Transistor determines the amount of impedance for each parameter which in turn determines the directions for impedance optimization. Typically, a big impedance produce better efficiency while smaller impedance produce better peak power. An inverted asymmetric Doherty structure is suitable solution in realizing the load impedance variation of main amplifier from lower impedance to higher impedance according to the increase of the input power level. In order to optimize the load impedance shift as a function of the input power level, external input and output matching circuits are necessary. [3]

2.3 Three-stage power amplifier

The power amplifier under testing consists of three stages and it is presented in Figure 9. The first, pre-driver stage is a class A amplifier. The second, driver stage is balanced asymmetric Doherty amplifier. The third, final stage is 2-way asymmetric inverted Doherty amplifier. The purpose of driver stages is providing enough power to drive the final stage, especially in the situations where DPD is used since final stage can operate close to its saturation point. Final stage is the most important of all since it has the greatest effect on PA performance. It consists of input and output matching circuits, RF power transistor and a DPD feedback coupler before an isolator. Each of these components effect on the essential performance parameters. Input and output matching networks have an effect on stability, gain, bandwidth and output power. The output matching networks dominate the energy efficiency. RF power transistor effects on maximum output power, bandwidth and energy efficiency. The complete PA has additional electronic components for gain control, bias stabilization and automatic shut down in order to ensure the safety and stable performance for the PA module and thus the entire base station. Bias control networks has the main task of selecting the absolute level of bias current and adjusting it according to the temperature. This ensures that each transistor works at their desired region. [1]

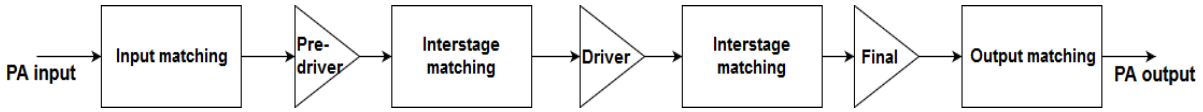

Figure 9. Line-up of three-stage power amplifier.

2.3.1 Key RF parameters

High power gain at the final stage and efficiency are the key parameters to approach in power amplifier design along with linearity. Power gain is a ratio between output and input power of the amplifier defining how much the signal level will increase. Gain is strongly related to the efficiency, as the following equations will show. The best efficiency can be achieved when the last amplifying stage has the highest possible gain. Then, the driver stages can operate with lower power levels. Reasons for approaching a high gain are good efficiency and cost. A high gain in high power final stage requires lower power and hence lower cost driver. Lineup might require fewer devices and therefore less space on printed circuit board. Designing of stable parts with a good isolation becomes challenging if the gain exceeds approximately 35 dB in multistage amplifiers. [1]

Since the power amplifier consumes a lot of power when the base station is running at the fullest, efficiency is an essential parameter along with power consumption. When the efficiency is high, power amplifier generates less heat creating a positive effect on thermal design. Also, the thermal memory effects are reduced. One way to define is power-added efficiency (PAE). It is a metric which considers the input power level and therefore, the gain. PAE is defined as [2]

$$\mathrm{PAE} = \frac{P_{\mathrm{RF}} - P_{\mathrm{IN}}}{P_{\mathrm{DC}}}, \tag{15}$$

where P_{RF} is the RF power at the output of power amplifier, P_{IN} is the input power level and P_{DC} is the power from the DC power supply. Total efficiency of three-stage amplifier is defined by equation (16) [2]

$$\eta_{\mathrm{T}} = \frac{1}{\left(\frac{1}{\eta_1 G_2 G_3} + \frac{1}{\eta_2 G_3} + \frac{1}{\eta_3}\right)}, \tag{16}$$

where η_n is the efficiency of n^{th} stage and G_n is the gain of n^{th} stage. It can be noticed that the final stage efficiency and gain has the most impact on total efficiency. Therefore, the careful design of the last stage becomes important. On the other hand, gain and efficiency tuning on the driver stages may help if the last stage gain is small.

Peak power means the maximum output power that the power amplifier can provide at a short time. Equation (16) holds mostly at the peak power situation. It is closely related to the average output power and PAPR, since the value of peak power can be estimated in decibels with a sum of PAPR and average output power. This means that the linear region must be large because of the maximum output power level requirement and PAPR and hence, peak power must stay within the linear region. Typically, the PA design is based on peak power requirements since the module is required to operate well in the toughest situation.

IBW measures how wide modulated spectrum the system can respond to. It includes the intermodulation products. Since the system uses wideband LTE signals, the analysis of them requires a wide IBW. For instance, spectral emission mask (SEM) test requires wider IBW than the interesting signal in order to perform the test more quickly. The situation with multicarrier signal, maximum IBW and high PAPR is the hardest from the linearization point of view. [6]

2.4 Nonlinearities of power amplifier

As explained on section 2.1.2, power amplifiers create nonlinearities caused by nonlinear elements. Thus, nonlinear behavior causes amplitude compression and high ACP ratio as the phenomena called spectral regrowth happens. The origin of nonlinearities arises from the current sources and parasitic capacitances of RF power transistor. Figure 10 illustrates how the nonlinear PA creates distortion components on the frequency domain. When all three stages are combined, the completeness defines the nature of nonlinearities. The interesting modulation scheme defines how the nonlinearity must be characterized. For instance, 16-QAM may suffer from the amplitude compression [7].

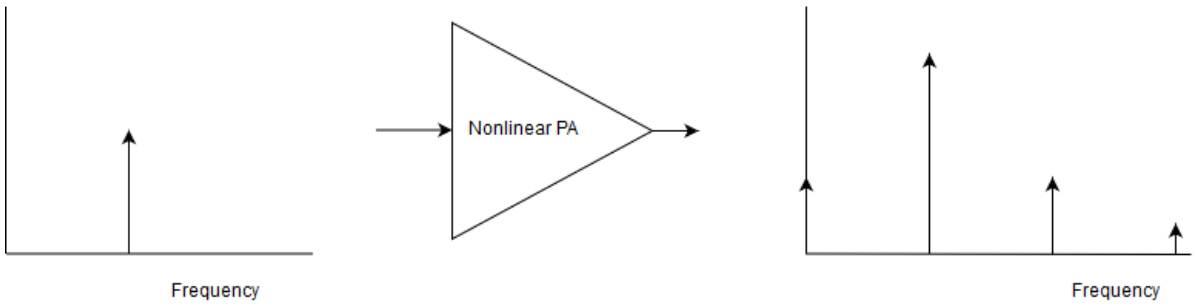

Figure 10. Nonlinearity causes distortion components on the frequency response of the amplified signal.

Testing of nonlinearity can be implemented with intermodulation IIP3 and 1-dB compression point tests which are usually based on unmodulated tones. For example, the specification for third generation mobile system requires intermodulation testing with unmodulated and modulated tones. Amplitude-to-amplitude (AM-AM) and amplitude-to-phase (AM-PM) conversions are another characterization of nonlinearity. In section 2.4.2, these topics are discussed more precisely.

2.4.1 LDMOS transistor technology

The transistor is the heart of RF power amplifier. There are many different transistor technologies which can be based on gallium arsenide (GaAs) or gallium nitride (GaN), for example. GaAs transistors can be utilized for high frequency, broadband and linear amplifiers but on the other hand, it is not suitable for high target output power amplifier. GaN transistors are able to deliver broadband, high frequency and high power but they are much more non-linear and expensive. Therefore, the optimal choice for this work is laterally diffused metal-oxide-semiconductor (LDMOS). Since the DUT is applied to base station which is an

environment for linear, high gain and cost-effective power amplifier, LDMOS transistor is a good option for qualifying the demands. LDMOS transistors are cheaper and linear and have high enough power efficiency.

Figure 11 represents both LDMOS (a) and vertically double-diffused metal-oxide-semiconductor (VDMOS) (b) transistor cross-section dies. There are three electrodes in both LDMOS and VDMOS transistor structures: drain, gate and source. Drain is connected to the supply voltage since the MOSFET is n-type. Source is connected to the ground whereas the purpose of gate is inducing a channel when gate voltage V_{GS} has risen above the threshold voltage which is adjusted by high voltage p region properties. As it can be concluded from the name "LDMOS", the current flows laterally from drain to source through a channel, a metal strap and p^+ sinker and substrate. The length and doping level of n-drift region depends on the magnitude of supply voltage. In order to preserve the integrity of the gate oxide, N-drift region creates a drop in voltage such that the drain region potential below the gate is less than the supply voltage. [1]

The advantages of LDMOS transistor are found with comparison between LDMOS and VDMOS transistors. As Figure 11 shows, LDMOS can be packaged in more compact way. Also, LDMOS has all the electrodes on the top side of surface meaning simpler integration with other components. The gate potential can reduce the resistance of n-drift region in low voltage applications by accumulating charge carriers close to the surface. As both structures have direct overlap onto the heavily n^+ doped areas, gate-source capacitance C_{GS} is contributed and it decreases the speed of transistors. Nevertheless, the feedback capacitance C_{GD} is minimized by minimal overlaps of gate and drain electrodes in LDMOS structure. Since the current flows laterally in LDMOS, the on-resistance is lower than VDMOS transistors. [1][8]

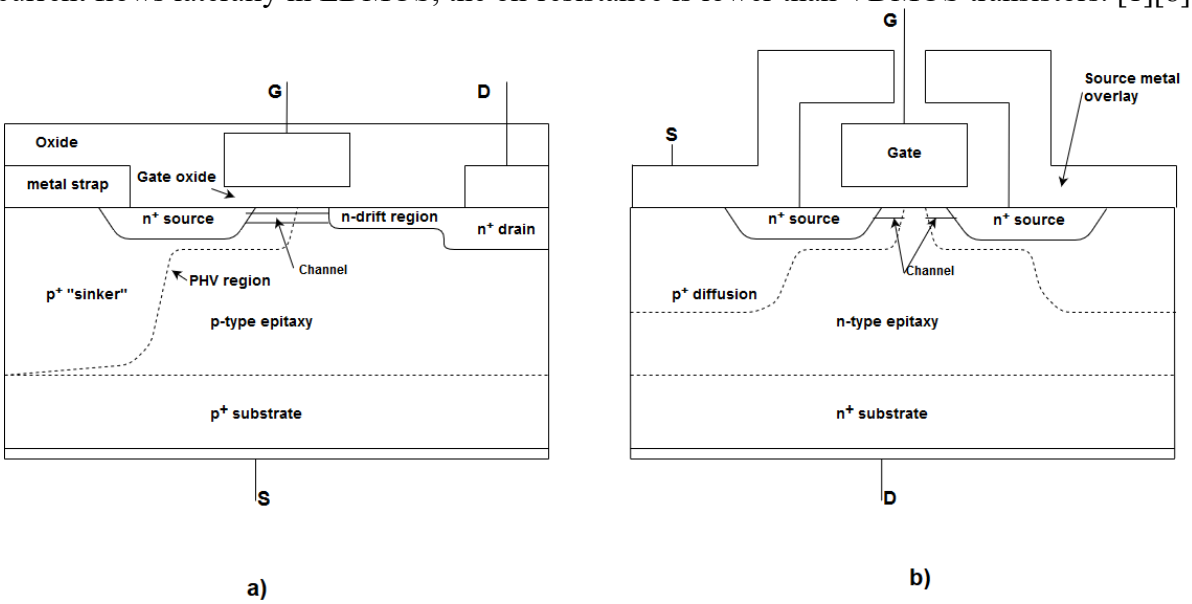

Figure 11. Cross sections of LDMOS (a) and VDMOS (b) transistors.

Though LDMOS has many advantages, it has its disadvantages, too. Hot carrier injection (HCI) is caused by electrons which are injected to into the gate oxide. This injection happens when there is a strong electric field which makes the electrons "hot". As the electron is injected into the oxide, it acts as a negative charge which induces a positive charge in the channel which causes loss of bias and therefore lower V_{TH} over the time. HCI is reduced by designing the n-drift region to sustain suitable breakdown voltage levels. [1]

Operational parameters of a transistor, such as efficiency and gain, are limited by parasitic elements which are represented in Figure 12. Often, nonlinear behavior of transistor is not

taken into account in discussion of operating classes, for example. Parasitic capacitances and resistances define the ultimate achievable performance limits. One common consequence of transistor's parasitic capacitance is degradation of transistor's frequency response. Other consequence results from the fact that parasitic capacitances are nonlinear functions of the junction voltage which causes distortion in the signal passing through the PA. Variation of these parasitic capacitances has a deteriorating effect on efficiency of input and output matching networks since the capacitances depend on the voltage used in the environment. Parasitic resistances limit the peak current of the transistor and hence the peak efficiency is degraded. Not forgetting the basic functionality of a resistor, the dissipation of energy is caused by the current flowing through the resistive elements. Degrade of overall performance is also a result of parasitic resistance in a way that certain regions, such as n-drift region, need to be optimized to meet the requirements for HCI reliability and breakdown voltage. In the case of target modulated signal, the biggest impact into heat generation and RF performance is defined by the dynamic broadband voltage and current at the input and output of the transistor. The biggest heat dissipation is caused by drain voltage and current power product having a high dissipated power. [1]

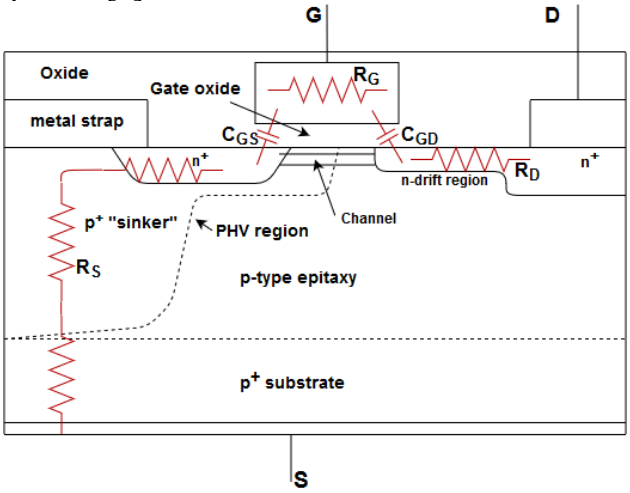

Figure 12. Parasitic resistances and capacitances of LDMOS transistor.

2.4.2 AM-AM and AM-PM

AM-AM and AM-PM conversions are graphical way to present the gain nonlinearities. These conversions are described as change in either amplitude or phase as a function of input power. Figure 13 illustrates both AM-AM (a) and AM-PM (b) conversion characteristics. On the left side, gain is visualized as a function of input power. The shape of the nonlinearity is common to Doherty PA structure presented in section 2.2.1 at the region where the peaking amplifier begin to turn on. First, the gain expands as the input power level is increased. The reason for gain expansion could result from beginning of transistor's self-biasing which is a cause of higher input drive. Also, peaking amplifier begin to turn on while main amplifier begins to saturate. Thus, the behavior of load modulation and the transistor is not ideal. The same effect could explain the shape of the AM-PM curve on the right side in Figure 13. These effects are nonlinear, thus the distortion makes the gain nonlinear. In practice, shapes of the AM-AM and AM-PM curves of the studied Doherty PA are more complicated. An amplifier with good linearity properties suffers less from phase distortion closer to the compression point. In modern communication systems, the phase distortion might be a real problem, especially with phase modulated signals. The reason what causes AM-PM distortion is a complex problem,

but in general, AM-PM effects can originate from signal-level dependency of key transistor model elements. For example, metal-oxide-semiconductor field-effect transistor's (MOSFET) nonlinear resistances, in presence of linear reactance, can cause AM-PM effects as much as nonlinear reactances. [2]

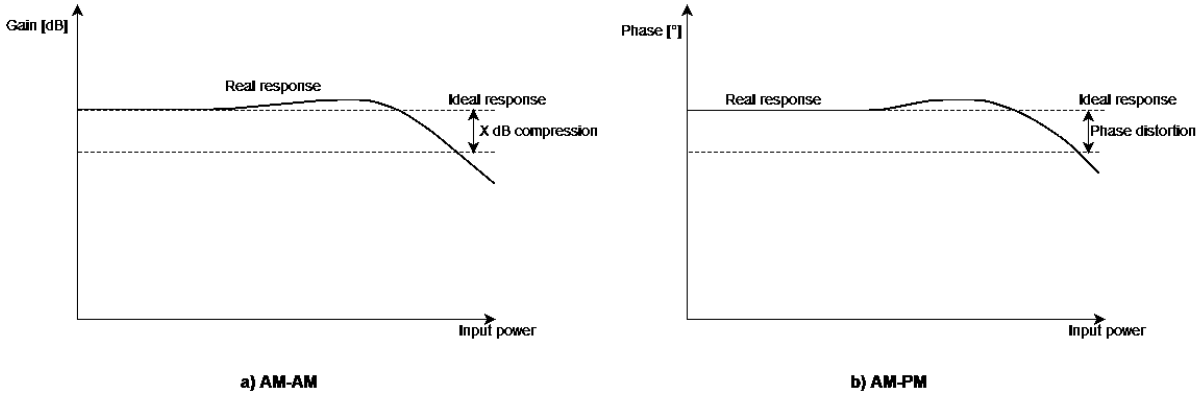

Figure 13. AM-AM and AM-PM conversion characteristics.

2.4.3 Memory effects

Distortion components vary as a function of signal bandwidth and amplitude. In other words, memory effects can be defined as bandwidth-dependent nonlinear effects which are divided into two categories: electrothermal and electrical effects. Memory effects are caused to the system by a mass with thermal or potential energy or active energy-saving devices such as a capacitor.

Electrothermal memory effects are results from electrothermal couplings which have an effect on frequencies up to the megahertz range. There is an assumption that a device that heats itself produces more memory effects than a component which get affected by the other sources generating heat. Transistor's external heat raises semiconductor's temperature slowly. This temperature raise is so slow that it does not change significantly during the downlink frame burst. When it comes to the heat that transistor generates, it modulates the semiconductor's temperature as a function of transmitted signal. This modulating temperature effects on the RF performance during the downlink frame burst. These effects have short time constants and they have an impact on the performance parameters of the transistor. Thermal impedance Z_{TH} describes mathematically how the modulating heat turns into "a control voltage" which changes the performance of the transistor. To overcome the heat dissipation which induces distortion and memory effects, the drain efficiency is tried to get as high as possible at the target RMS output power level. Also, the overall thermal resistance from transistor semiconductor junction to the mechanics is tried to make as low as possible by optimizing the thermal conductivity and cooling. [9]

Transistor generates distortion currents which are transformed to voltages by the impedance the currents see. Thus, the frequency-dependent envelope, fundamental or second or higher order harmonic node impedances have an effect on the created distortion voltages. The frequency dependency of distortion currents and impedances seen by the currents cause the electrical memory effects. These impedances operate in their own frequency bands. If the second harmonic band is wide and the impedance matching is constant, the harmonics are not trapped when the traps are not causing impedance variations which in turn may cause memory

effects. Narrow band resonances may cause difficult memory effects. Also, the fundamental impedance can be kept constant easily as the modulation frequency range is small commensurate with the center frequency. Nevertheless, the envelope impedances with transistor's internal connections and bias circuitry may play the biggest part in producing memory effects as the frequency band varies the most. The possible matchings inside the RF power transistor are usually optimized for a certain performance. Therefore, a designer cannot affect a lot on the overall performance of the PA from transistor level. If the system's center frequency changes, the situation is a bit different. Both the second harmonic and fundamental impedance change while the envelope impedance remains the same. It means that the second harmonic and fundamental bands produce a meaningful amount of memory. All in all, the electrical memory effects can be reduced with a careful design. [9]

Since the PA has to be linearizable, the analysis of generation of nonlinearities is a benefit. One way to represent dynamic nonlinearities is Volterra series where the nonlinearities are expressed as polynomials. Volterra analysis has its advantages. Recognition of dominant distortion mechanisms can be done as in normal AC noise analysis whereas recognition of multiple mixing mechanisms can be performed as in the nonlinear analysis helping in the optimization of harmonic terminal impedances. However, as power amplifiers contain many memory elements, the polynomial expression is not the simplest and quickest way to observe nonlinearities. Outside of the fitting range, the response of the polynomial model gets out of the hand towards infinity. Also, the noniterating Volterra calculations can only estimate the shifts in DC operating point which are caused by the large signal operation. To settle the latter shortcoming, the polynomial model can be fitted at the actual large signal operating point or the DC operating point shift can be proved not to be too significant. [9]

2.4.4 Digital pre-distortion

Digital pre-distortion is a linearization technique used in modern devices helping the PA to achieve linear behavior. Most linearization techniques use the input RF envelope's amplitude and phase as a reference to compare the output with and then generate the needed corrections. Figure 14 represents the principle of ideal predistorter and how it effects on amplifier's gain and output. Red curve represents the output of DPD and PA system, which is the sum of solid and dashed line around it. The blue curve represents the flat gain of DPD and PA system which is also the sum of dashed and solid curves around it. Since the digital techniques are utilized for signal generation in the most modern communication systems, the implementation of predistortion linearization is simplified at intermediate frequency or baseband while the signal is still in digital domain. [3]

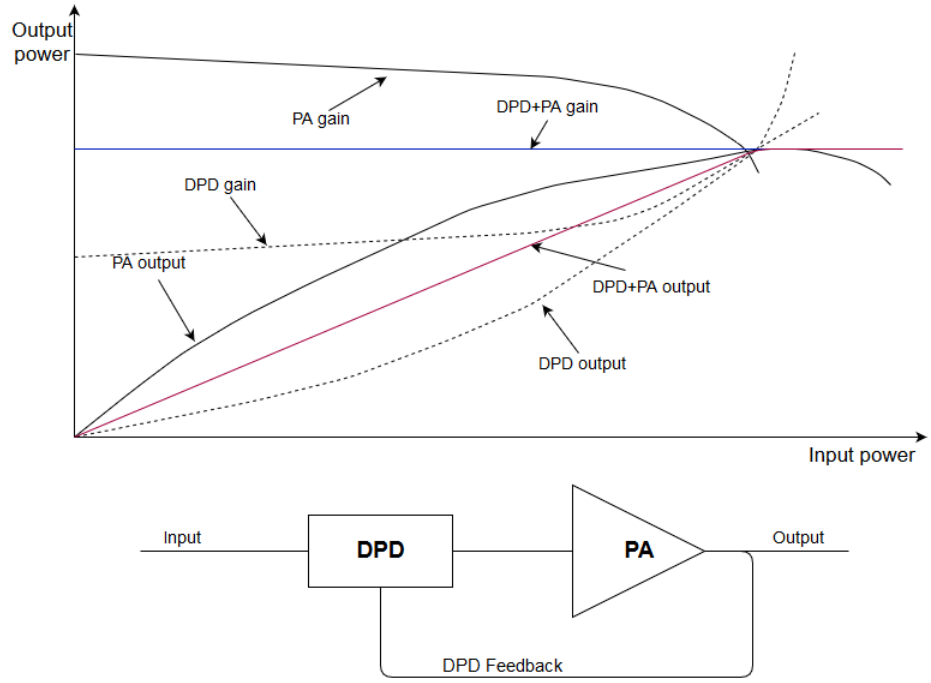

Figure 14. Operation of DPD and PA in terms of output and gain.

Simply, DPD creates an adaptive predistortion signal which goes through the PA making the output response linear. DPD models the PA behavior by a complex baseband model. Predistorter forms inverse nonlinear characteristics which can be implemented in several ways. The similarity with all of the characteristics is that the DPD output is calculated as an input magnitude-dependent function of the original input. Basically, DPD output is a predistortion signal which has the same amplitude as PA output but there is 180° phase shift. When the predistorted signal passes through the PA, the signal at the PA output become linear after the distortion effect of the PA. [1]

The advantage of DPD is that it can generate predistortion transfer characteristics that would be hard to implement with analog signals and discrete components. Also, memory effects are reduced when the PA design is done more carefully when taking DPD into account. Short-term memory effects are reduced in such a way that DPD algorithm includes the recent history of the signal. On the other hand, the sampling rate of the digital systems limits the IBW of the signal, which includes its intermodulation products. Overall, very non-linear power amplifiers with good efficiency can be put into operation with help of DPD. [2][3]

Inverted asymmetric Doherty PA scrutinized in this thesis demands specific properties from the DPD. Up to 70 MHz IBW and high PAPR signal is hard to be predistorted along with the nonlinearities the DUT creates. The goal is to get the identical shape of AM-AM and AM-PM curves at all channel frequencies. It would indicate that the PA has a small amount of short-term memory effects. AM-AM and AM-PM does not include intermodulation distortion components. Therefore, the final testing should be always done by using linearization.

3 CORNER SAMPLE DATA ANALYSIS METHODS

The main goal in RF PA design procedure is to optimize the PA design in a way that all the essential performance parameters are within their specification considering the aging and variance in quality of components' performance. Increase in production capability adds the variance in RF performance parameters meaning that this variance should be somehow illustrated in R&D phase. Also, there is productional variance in the RF power transistor and variations in components which gives a reason for investigating the components before their implementation. Since the simulation of amplifying stages separately and together cannot always be done due to incomplete datasheets and simulation models of different components, another way must be found. Corner sample build is one way for illustrating the productional variance of PA modules and it takes its place after the PA is designed by partial simulations and hardware tuning to a sufficient level.

3.1 Corner samples

Corner sample build is used in R&D in order to illustrate artificially the realistic productional variance of PA modules. Transistor manufacturer alters deliberately the internal matching network resonance frequencies below and above the known productional nominal matching resonance frequency. The tuning is executed by adjusting the bond wires inside the transistor. What comes to the input and output matching of the PA, usually it is a compromise between these three most monitored parameters: output power, efficiency or linearity. But in the end, the PA must be able to linearize in the system. The variations with this exact tested corner sample build are made to the final stage. The fact, that changes made in input matching changes the load the driver sees, should not be forgotten. Table 1 presents the definition for each corner sample version. As it can be noticed from Table 1, corner samples are forced to operate in certain resonance frequency. The transistor's manufacturer knows that these frequencies are statistically possible in production and need to be taken into account. Due to this fact, these samples represent the behavior only on the operational limits. Therefore, it is not commonly known whether these samples represent the operation of the whole population of this kind of power amplifiers. The amount of tested PA modules is 20: three per corner sample version. Version number V1, which is used as a reference version, makes an exception, because one module was assembled wrongly. With the test results the productional variance can be estimated and the PA design can be optimized to operate correctly within the specification.

Table 1. Definition for each corner sample version

Version number	Input matching resonance, main	Input matching resonance, peak	Output matching resonance, main	Output matching resonance, peak
V1	Nominal	Nominal	Nominal	Nominal
V2	Tuned down from nominal	Tuned down from nominal	Nominal	Nominal
V3	Tuned up from nominal	Tuned up from nominal	Nominal	Nominal
V4	Tuned down from nominal	Tuned up from nominal	Nominal	Nominal
V5	Tuned up from nominal	Tuned down from nominal	Nominal	Nominal
V6	Nominal	Nominal	Tuned down from nominal	Tuned down from nominal
V7	Nominal	Nominal	Tuned up from nominal	Tuned up from nominal

3.2 Performed tests and used test setup

At the R&D phase, PA modules are tested in many levels. The first test is performed right after the production to ensure that there are no broken components and the biasing is successful. Then, the performance of the power amplifier module is tested of the PA itself and in a sub-system with DPD. Also, PA modules are tested in the base station unit. The purpose of module level tests is to ensure the power amplifier design performance whereas the unit level tests are performed to ensure that the PA co-operates with other base station parts as it should fulfilling the requirements for base station. The behavior of the essential performance parameters is seen best from module level tests and therefore, the analysis is focused on module level test results. Effect of temperature in RF performance parameters and the PA module operation is ensured by implementing measurements in extreme temperatures. Substantive module level tests made with corner samples are presented in Table 2. Usually, there are many more tests to do. Tests presented in Table 2 are critical performance parameters with tight design specification. What comes to linearized ACP measurements, they are performed with four different carrier configurations: LTE5, LTE10, LTE20 and 2×LTE10.

Table 2. Performed tests in module level

Module level tests
DC Power consumption
Frequency response
Peak power
Non-linearized ACP
Linearized ACP

Proposed test setup is presented in Figure 15. It consists of the most common RF measurement equipment such as network and spectrum analyzers, couplers and attenuators. The used test setup is capable to perform all the tests in Table 2 systematically. In order to

minimize the user-based errors and ensure the quality of test results, test automation is one way for error minimization and ensuring the quality. Repeatability and the way how data is saved is always identical with test automation which saves also time.

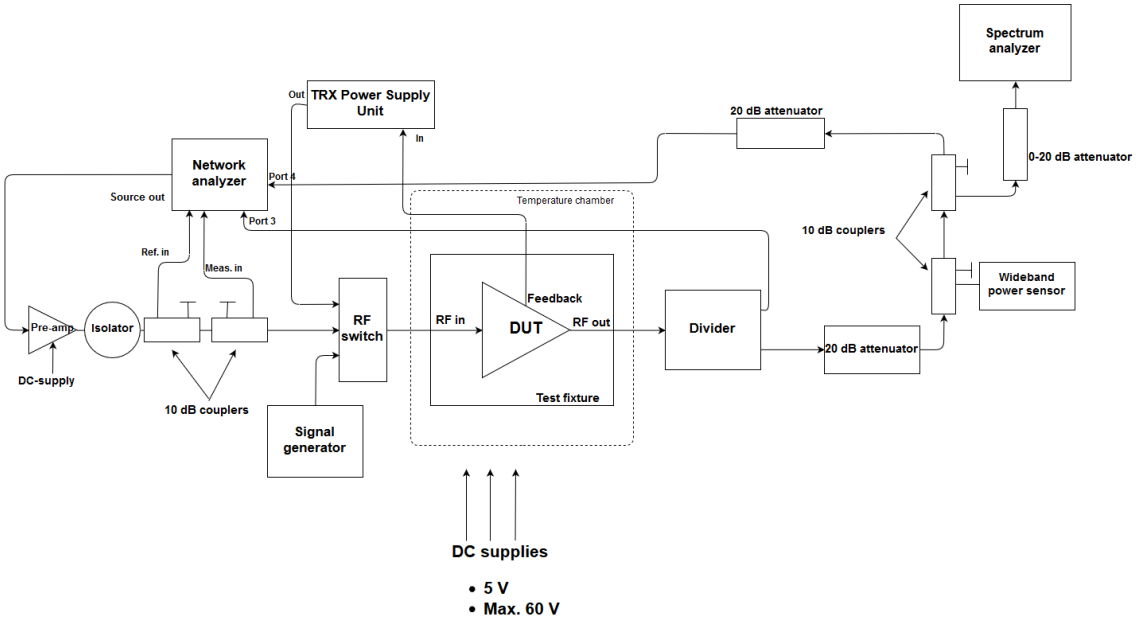

Figure 15. Proposed test setup for PA testing.

The information of the essential performance parameters is gathered from the performed tests. Analyzable parameters are peak power, power efficiency, ACP's and lineup gain. In addition, the process capability indices of the essential parameters will be analyzed. The reason for focusing on these parameters is the way how changes in one effects on another. High peak power means often poor efficiency which often leads to low gain. Low gain leads to higher power consumption. Therefore, the chosen corner sample version for modifications is the one with the worst peak power. Respectively, the version with the best peak power along with the nominal one should be chosen for the modification. Then, all three versions are verified.

3.3 Methods for measurement data analysis

The amount of gatherable data is huge and therefore, the careful planning of the tests is needed to be done before the beginning of testing. After performing the tests, the preparation of results may be done by filtering the unusable results out, ensuring the failed cases are not caused by a measurement mistake and testing the failed cases again, for example. If the failures are real, they are taken into the analysis. The next step is data analysis, which is a relevant part of any industrial process. The main purpose of data analysis is the PA design optimization. Generally, the process optimization increases the competitiveness of a company.

Basis of the measurement data analysis is based on the power amplifier theory and therefore, it is important to understand the phenomena behind the results. Depending on the process, there are many useful ways to analyze the process. In this design optimization case, the following methods are used. The raw data gathered from the measurements is unappealing to read and analyze in order to be able to make decisions about the design. Therefore,

visualizing the data into graphs helps the analysis process and the changes in performance are seen immediately. Comparing a certain performance parameter to the nominal, the best and the worst versions helps to see the variance and after the modification the growth of variation can be seen. Another analysis method concerns the way how the parameters change when comparing them to the behavior of the reference module and specification limits. In a statistical manner, process capability indices are the best way to study the behavior of parameters and based on the results the analysis of upcoming design changes can be done.

3.3.1 Lognormal distribution

The most common probability distribution used in statistical analysis of RF parameters is lognormal distribution. It is practically a version of normal distribution where logarithm of random variable is normally distributed. The reason for using lognormal distribution originates from the fact that most of the inspected RF parameters are expressed in logarithmic scale. [10]

Following equations are used in calculations for distribution graphs. Equation (17) presents the probability distribution function (PDF) of lognormal distribution [11]

$$f(x|\mu_L, \sigma_L) = \frac{1}{\sqrt{2\pi} \cdot \sigma_L \cdot x} e^{\frac{-(\ln(x)-\mu_L)^2}{2\cdot\sigma_L{}^2}}, 0 \leq x \leq \infty, \tag{17}$$

where μ_L is mean of logarithmic values, σ_L is standard deviation of logarithmic values, π is a constant pi and e is Euler's constant. Mean of the lognormal distribution can be defined with equation (18) [11]

$$\mu_L = e^{\mu + \frac{\sigma^2}{2}}, \tag{18}$$

where μ is mean of values and σ is standard deviation of values. The variance of lognormal distribution in equation (19)

$$\sigma_L = e^{2\cdot(\mu+\sigma^2)} - e^{2\cdot\mu+\sigma^2} \tag{19}$$

is defined. The measurement data is transferred to the logarithmic scale when it is expected that measurement data tend to be lognormally distributed. It is the basis of theories behind the parameter performance and analysis: for example, a process capability C_{pk} can not be calculated unless the data is not normally or lognormally distributed [12].

3.3.2 Process capability index and C_{pk}

Process capability is a unitless indicator which is defined as a range over which the process varies. The scrutiny of process capability is important in the process quality manner since the customers are requiring certain quality level on products. Most common process capability indices are related to the allowable process spread and the actual process spread. To clarify the concept of process capability index, let's consider a following example illustrated in

Figure 16. The process capability index is simply a division of actual and allowable process spread. If the index is one as in the left side (a) on the figure, the actual process spread is the same with allowable process spread. If the index is less than one as in the right side (b) on the figure, the actual process spread is greater than the allowable process spread meaning that the process is incapable. As a conclusion, process capability index should be greater than one in order to control the process statistically well. Electronics industry usually requires Six Sigma-level on process capability indices since the manufacturing is expensive. In other words, the process yield is higher with higher indices. Six Sigma simply means that the "distance" between process mean and upper or lower specification limit is six times the standard deviation of the process. [13]

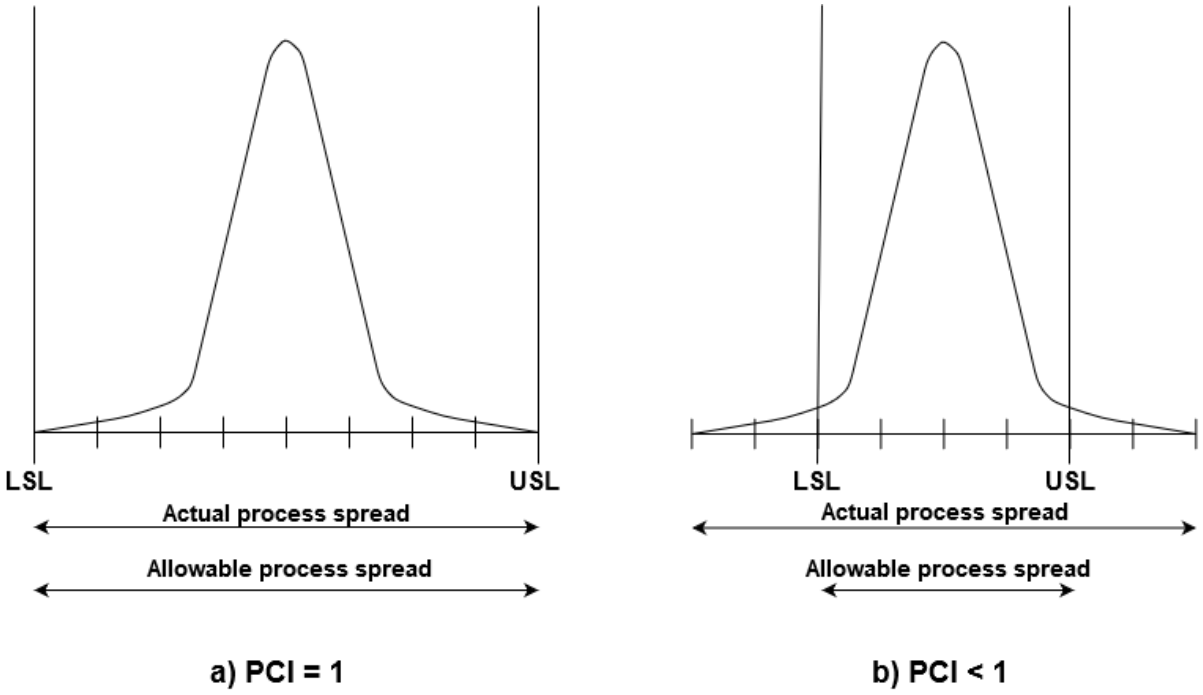

Figure 16. Illustration of process capability index.

Process capability C_{pk} estimates what the process is capable of producing while considering that the mean of the process is not centered between the specification limits. Simply, C_{pk} can be calculated as [13]

$$C_{pk} = \min\left[\frac{\hat{\mu} - \mathrm{LSL}}{3\hat{\sigma}}, \frac{\mathrm{USL} - \hat{\mu}}{3\hat{\sigma}}\right], \tag{20}$$

where LSL is the lower specification limit, USL is the upper specification limit, $\hat{\mu}$ is the estimated mean of the process and $\hat{\sigma}$ is the estimated variability of the process expressed as a standard deviation.

C_{pk} is a good index in analyzing the essential performance parameters of PA module from the quality point of view, especially with a build attempting to illustrate a large population of PA modules. Though, the amount of testable PA modules in R&D is small compared to the mass production and therefore, C_{pk} works better with larger number of testable modules. The productivity and design of PA modules can be monitored and directed with C_{pk} in such way that taking into account the productional variety, the PA will operate as expected. Also, C_{pk}

analysis can be attached to the customer satisfaction since the fulfillment of specification is necessary for customer. The way how each RF parameter is concentrated in relation with specification limits and direction for possible design optimization can be seen from bell shaped curves of each parameter. If a correction in PA design is made, a drawback arises when the design change should be verified with an adequate population of modules. If a bigger population of PA modules is produced, other possible changes in design must be added to the newer design in order to save the allocated resources of project. It means that the other changes can hide the effect of optimizing change from the C_{pk} analysis and therefore, the effect of this particular change cannot be ensured. Also, the optimization of a certain parameter might have a negative effect on another parameter.

Process yield is an important factor in the quality manner tied to C_{pk} and sigma level. The amount of successfully and unsuccessfully manufactured PA modules can be predicted with it. In R&D phase the amounts of modules are smaller compared to mass production. Therefore, the process yield is more suitable in analysis of mass production. However, the scrutiny of C_{pk} values and process yields in R&D has an important role in optimizing the design for better process yield. The relations between C_{pk} values, process yields and sigma values are presented in Table 3 [12]. As one can notice, the importance of Six Sigma requirement is emphasized. If one million PA modules are produced, only 3.4 modules are unsuccessful with C_{pk} of 2. If measured C_{pk} is 1, 67000 modules are unsuccessful of one million produced modules. Therefore, C_{pk} analysis suits well for estimating the true cost of manufacturing and replacing the broken modules.

Table 3. Relations between C_{pk} values, process yields and sigma levels

C_{pk}	Process Yield	Sigma level (short term)
2.0	99.99966 %	6
1.5	99.87 %	4.5
1.17	97.7 %	3.5
1	93.3 %	3

4 DESIGN OPTIMIZATION USING MEASUREMENT RESULTS

4.1 Electrical and functional test results

This chapter presents the module level test results of the essential parameters in all three temperatures which are compared to the specification limits presented in Table 4 and Table 5. Each PA module is measured as it is and with linearization. Usually, different supply voltages are used in order to optimize the power consumption in different situations. However, the supply voltage of 32 V and output power of 49.9 dBm are used in all following test cases making the comparison between parameters clearer.

Peak power specification takes into account the base station output power, signal PAPR and insertion loss with margin for performance variations and aging. The latter depends on the channel frequency: there is approximately 1 dB difference between the middle, the lowest and the highest channels. The output power decreases approximately 0.5 dB in hot temperature making a difference between temperatures. Gain is measured from the three stage PA module and specification for it comes from the system architecture specification. Thus, losses, input power and variations are taken into account. Non-linearized ACP specification comes from the experience of the non-linearized ACP level where DPD is expected to linearize the PA output. Requirement for linearized ACP is calculated backwards from antenna connector to the PA output with margin. Transmitter output power over the signal bandwidth is transformed to the output signal power per megahertz. The carrier signal bandwidth has an effect to the requirements: the narrower the bandwidth, the more stringent linearized ACP requirement is due to higher power density per megahertz. The SEM requirement per megahertz is subtracted from the output signal power per megahertz leading to the specification requirement for linearized ACP. Further, ACP requirements for PA module may include margins and knowledge of frequency responses after the PA output. Thus, the values below are examples used within this work. These factors also effect to the PA module peak power requirements.

Table 4. Specification limits for peak power and gain

	Peak power		Gain
Spec.	Lowest and highest	Middle	2620 - 2690 MHz
Room & Cold	57.5 dBm	56.5 dBm	40 - 50 dB
Hot	57.0 dBm	56.0 dBm	40 - 50 dB

Table 5. Specification for ACP measurements

	Non-linearized ACP	1xLTE20
Adj.	-26.5 dBc	-51.5 dBc
Alt.	-26.5 dBc	-53.0 dBc

4.1.1 Peak power

As mentioned in section 2.3.1, peak power is an essential parameter in a way that the PA module specification is defined in grounds of it. The maximum RMS output power target is 49.9 dBm when using the supply voltage of 32 V. The specification for peak power can be seen from Table 4. It should be remembered that the increase of peak power tends to worsen

the efficiency with modulated signals. On the other hand, too small peak power may have an effect on the linearity with the target output power and it lefts margin for performance variations and aging. Therefore, the corner sample version with average peak power values might linearize the best and achieve sufficient efficiency.

Peak power test results in room temperature with supply voltages of 32 V, 30 V and 28 V and output power of 49.9 dBm are presented in Figure 17, Figure 18 and Figure 19. The goal is to see how much and which direction the decrease of supply voltage effects on peak power values in different channel frequencies. As the figures show, the decrease of supply voltage decreases the peak power value with almost all board versions. Trend between the lowest, middle and highest channel frequencies are either decreasing or increasing: with versions 2, 5 and 6 the trend is decreasing whereas the trend is increasing with versions 3, 4 and 7. Corner sample versions as well as differences in transistor's internal matchings are described in Table 1. The greatest distribution within the board is seen in version 2 where the input of both main and peaking branches is tuned down from the nominal resonance frequency. The situation with such a high distribution is definitely not wanted since the specification cannot be met.

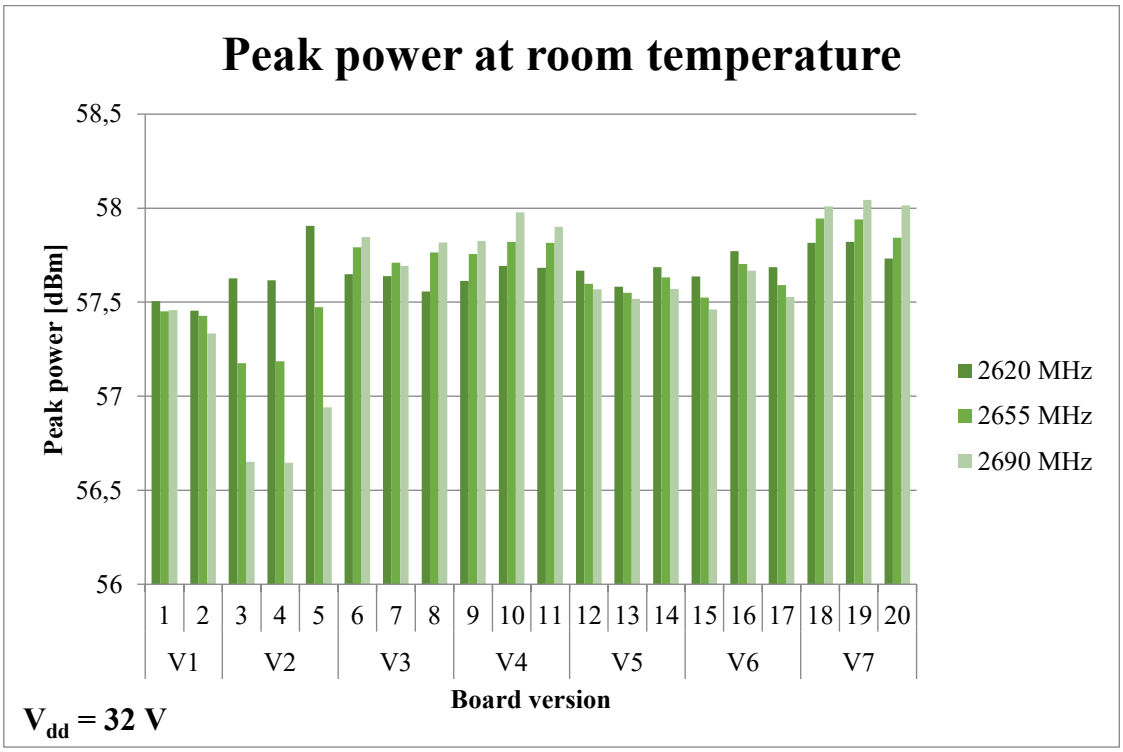

Figure 17. Peak power in room temperature when the supply voltage is 32 V.

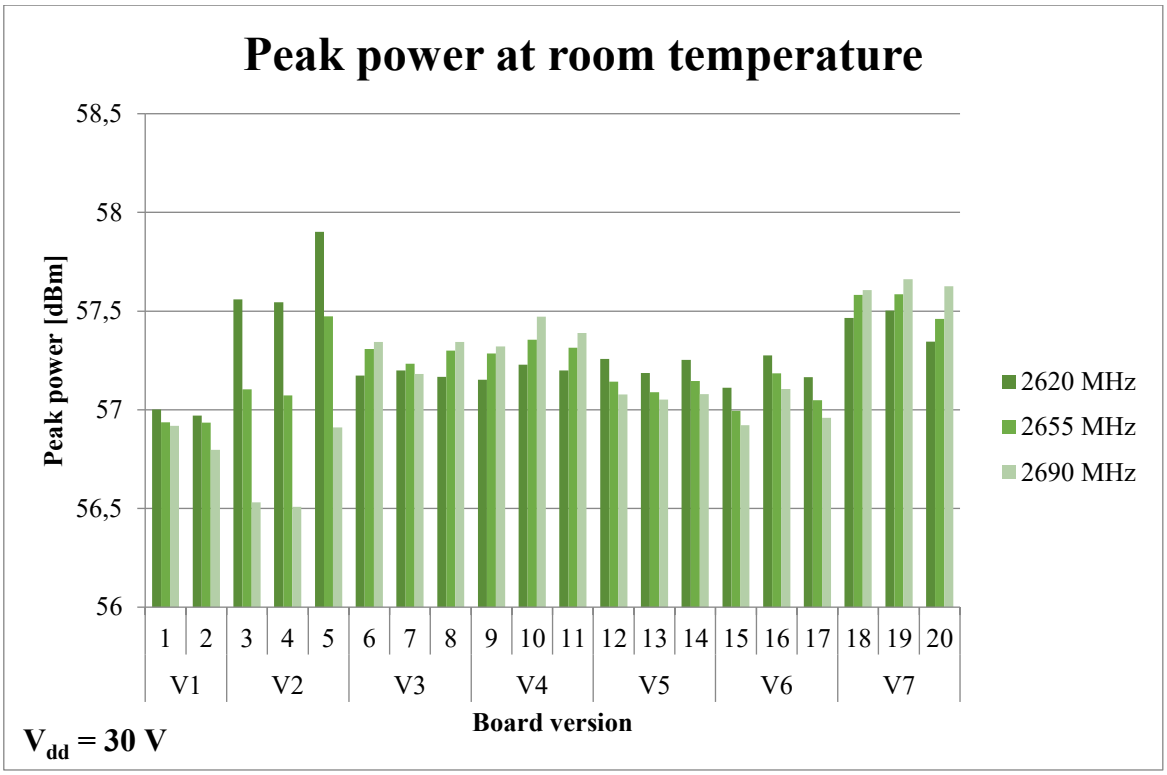

Figure 18. Peak power in room temperature when supply voltage is 30 V.

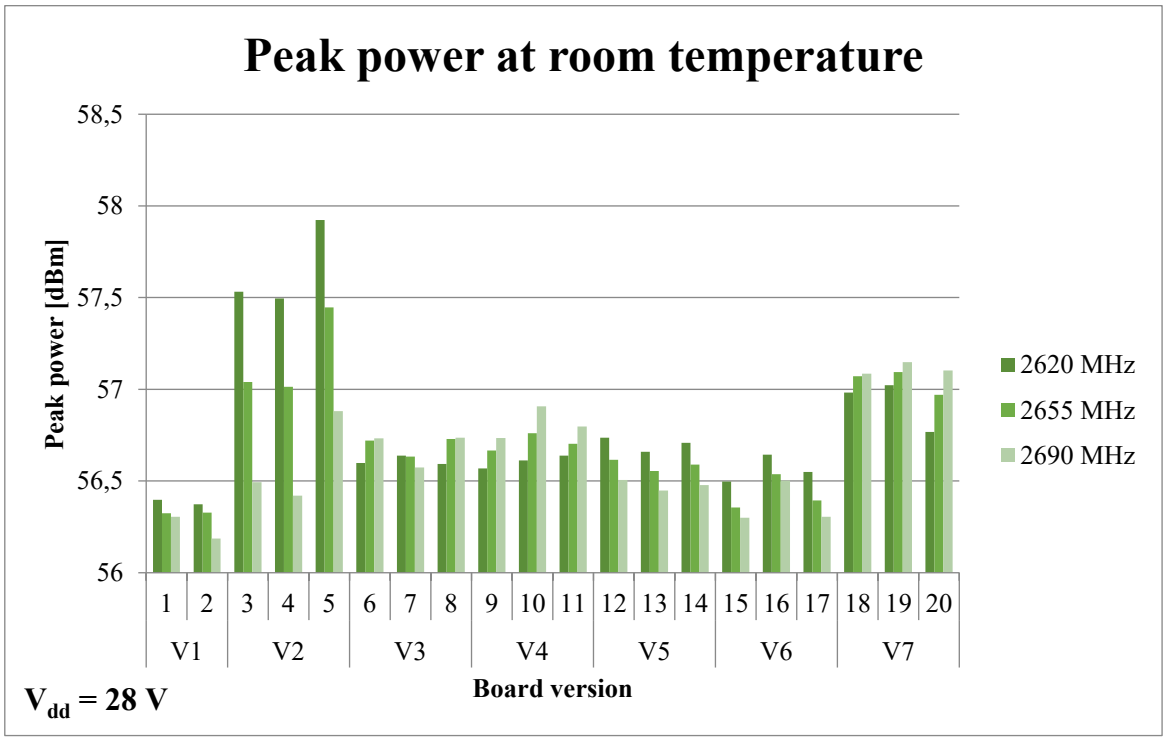

Figure 19. Peak power in room temperature when supply voltage is 28 V.

Figure 20, Figure 21 and Figure 22 present the peak power test results in cold temperature. The effect of temperature decreasing is seen by higher peak power values over all the corner sample versions. Versions 2, 5 and 6 had the decreasing trend in room temperature but now, peak power at the highest channel frequency has risen with most of the boards. Increasing trend is clearly seen only with version 7 now. With versions 3 and 4, peak power value has risen in the lowest channel frequency compared to room temperature results. All versions fulfill the specifications in all channel frequencies with 32 V supply voltage.

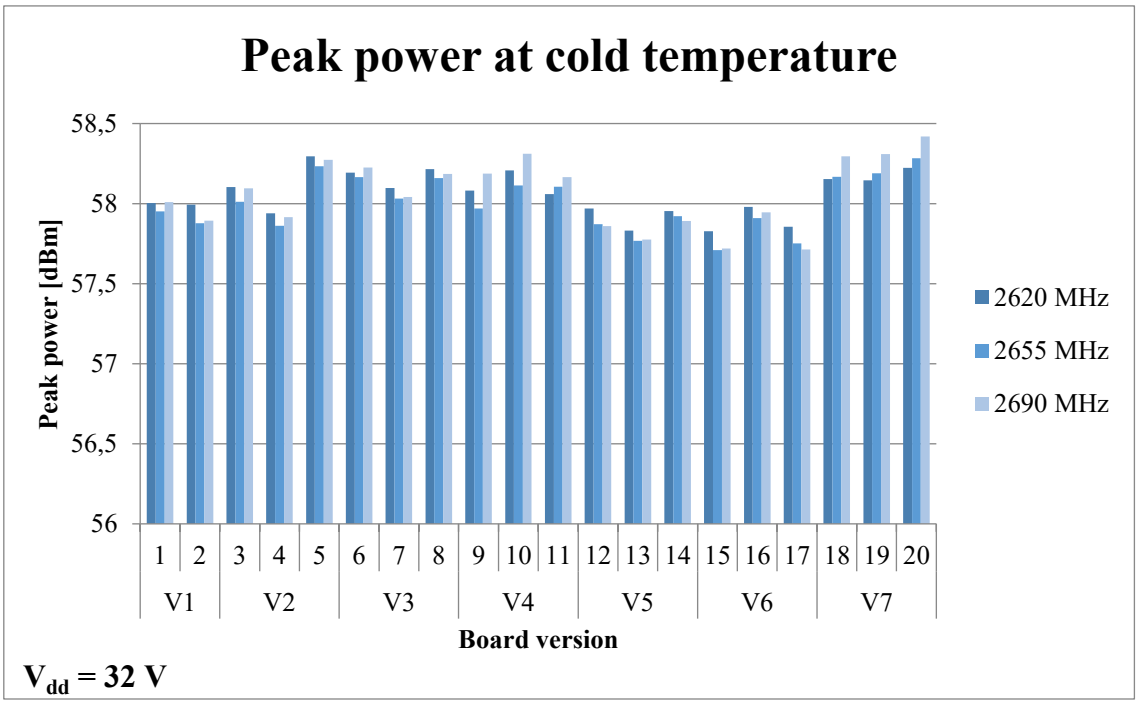

Figure 20. Peak power in cold temperature when supply voltage is 32 V.

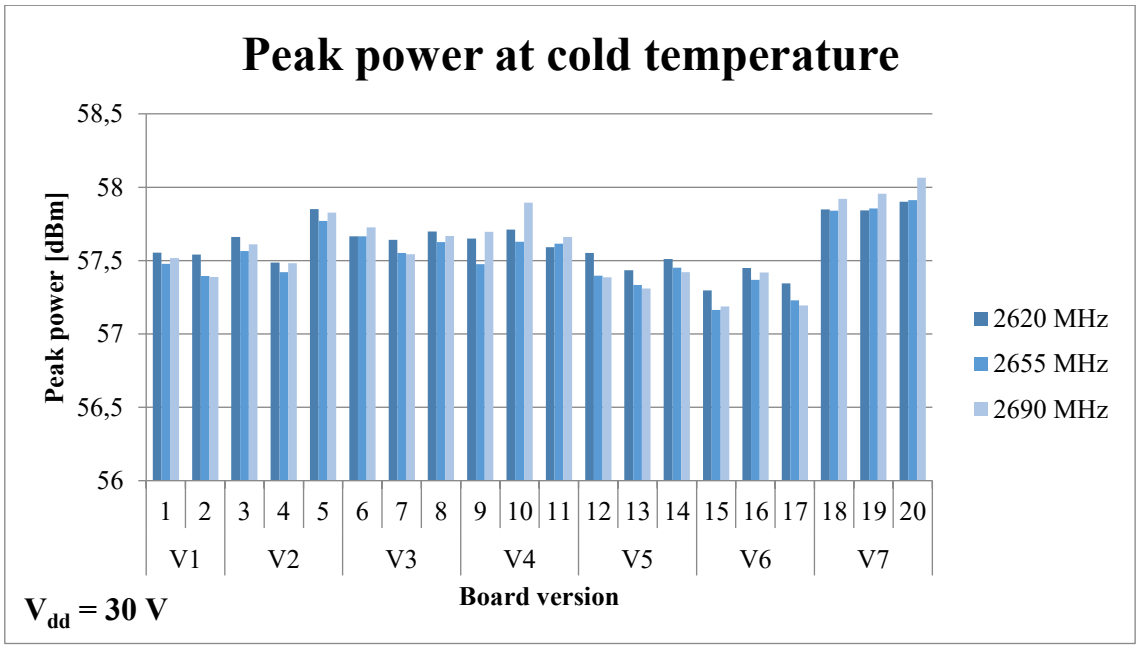

Figure 21. Peak power in cold temperature when supply voltage is 30 V.

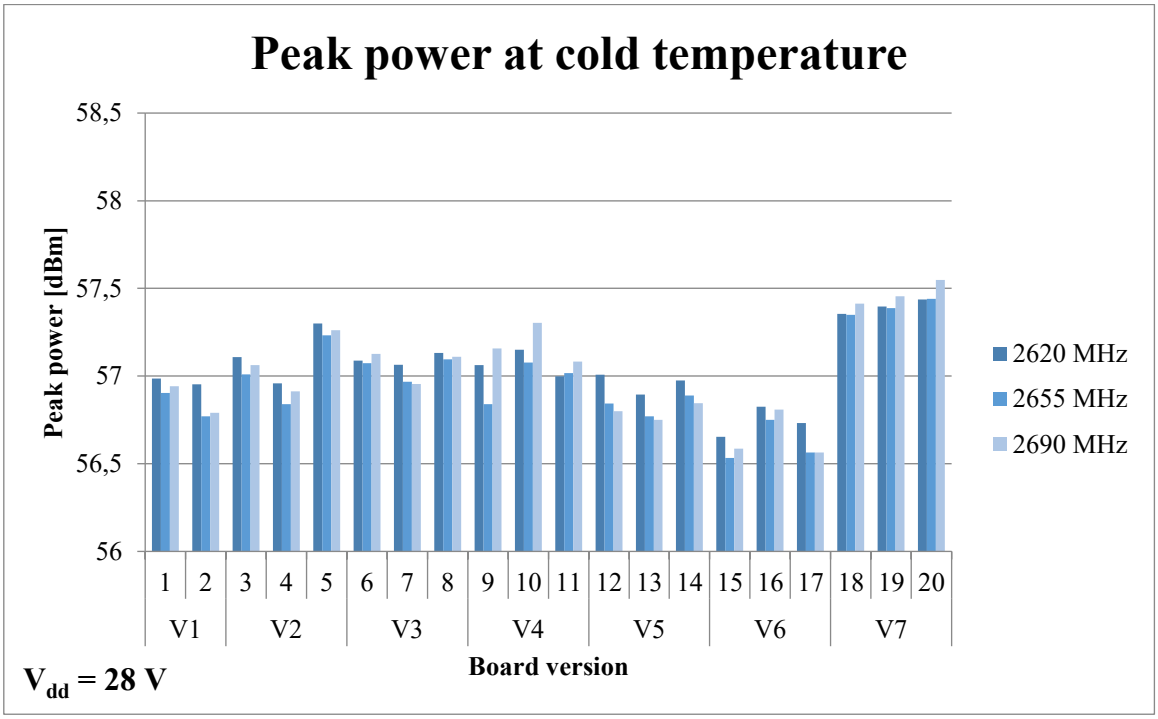

Figure 22. Peak power in cold temperature when supply voltage is 28 V.

In hot temperature, the peak power values are lower comparing to the situation in room temperature. Test results are presented in Figure 23, Figure 24 and Figure 25. The distribution between different channel frequencies inside a single board is higher with versions 3, 4 and 7 compared to room temperature situation. What comes to version 2, distribution between channel frequencies is much smaller than in room temperature. Specification is met with versions 1 and 2 only.

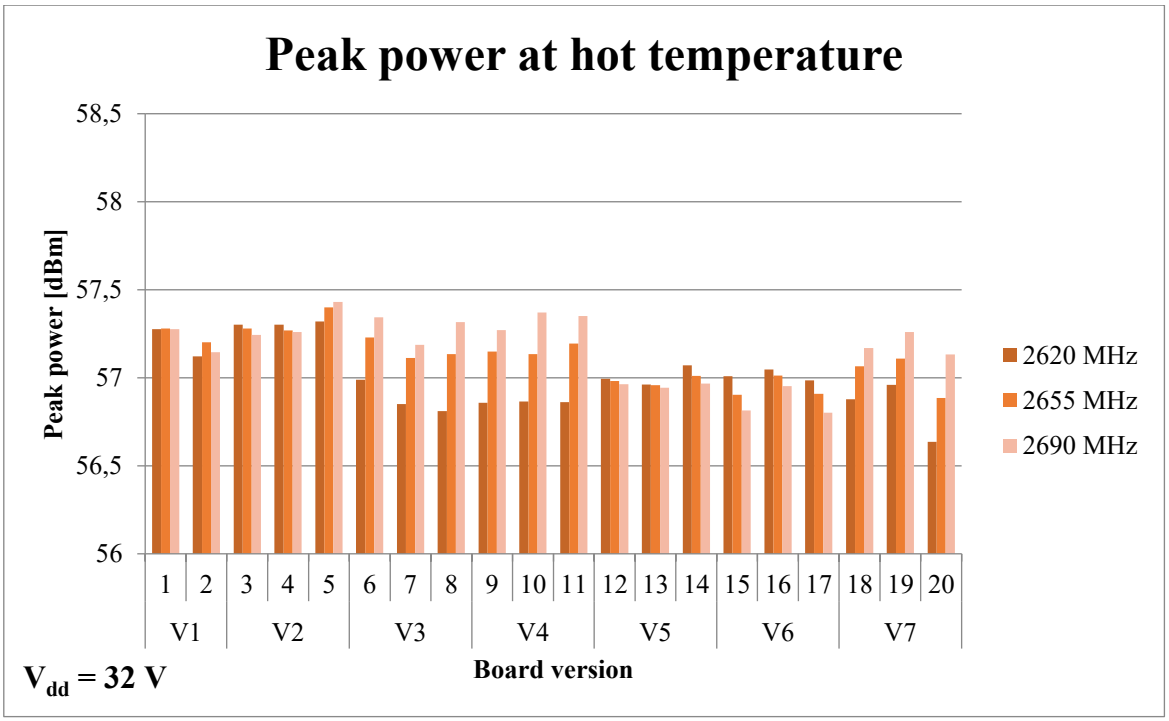

Figure 23. Peak power in hot temperature when supply voltage is 32 V.

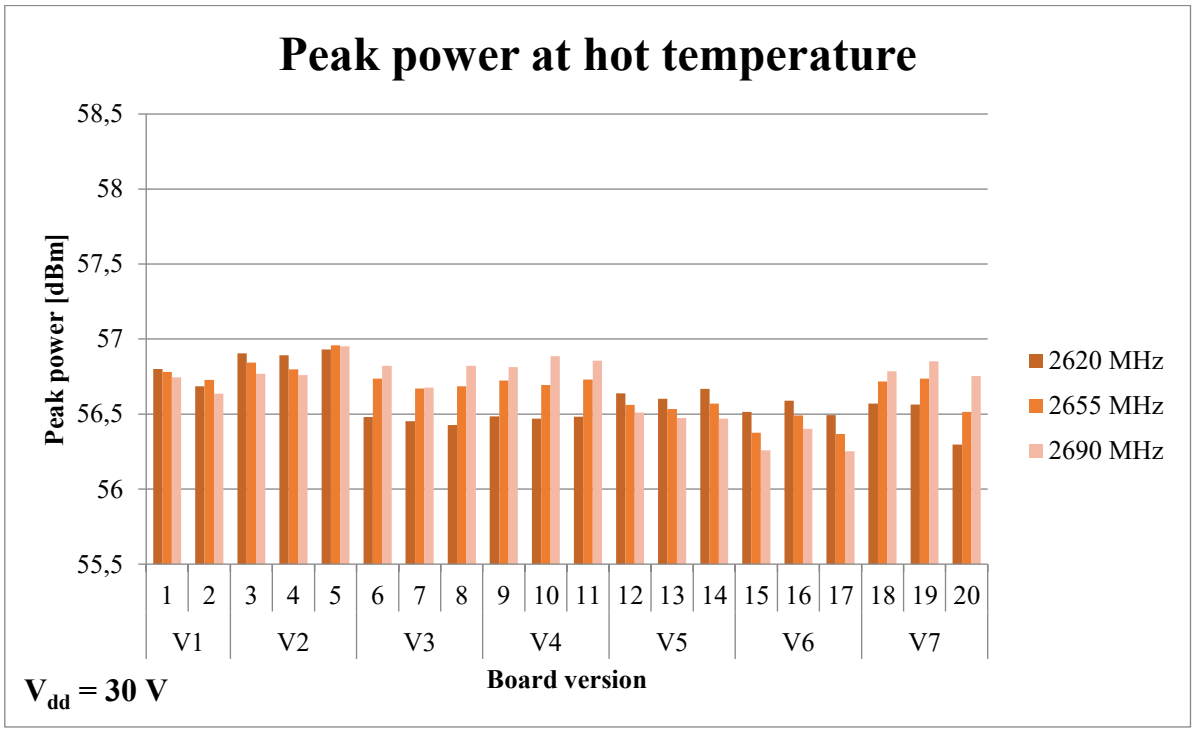

Figure 24. Peak power in hot temperature when supply voltage is 30 V.

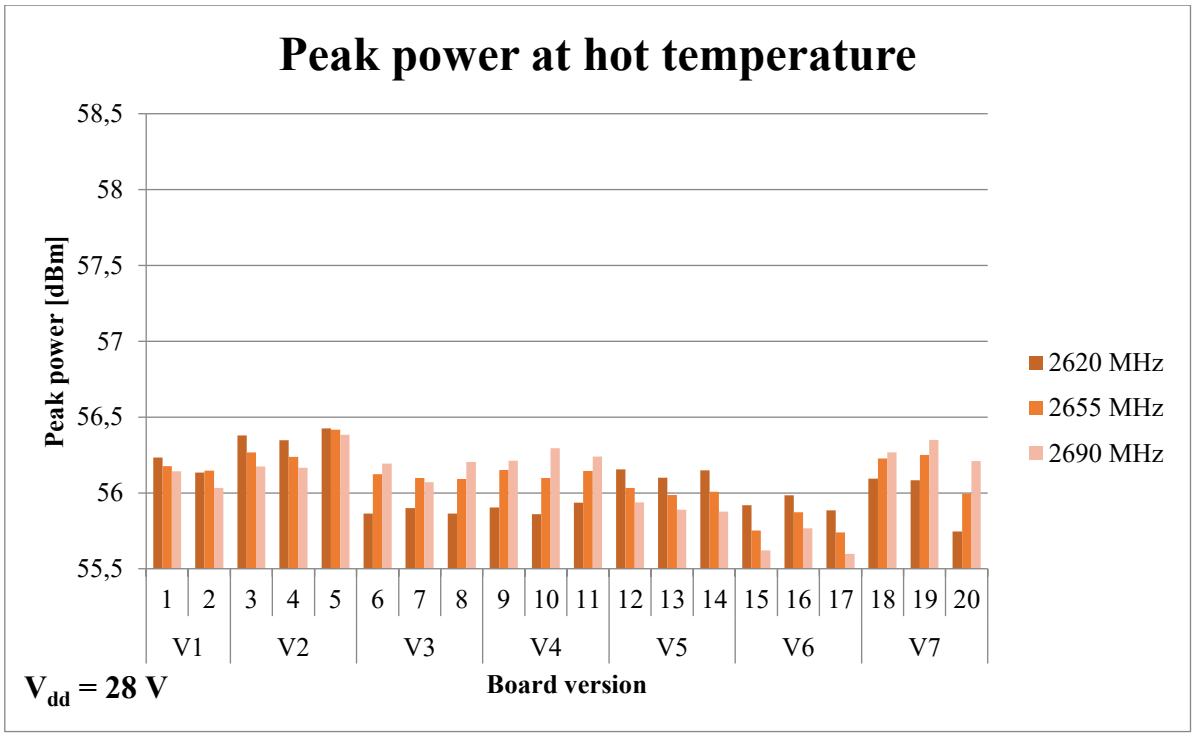

Figure 25. Peak power in hot temperature when supply voltage is 28 V.

Each corner sample version is ranked as the Table 6 presents. Ranking is made by choosing the minimum peak power value of each corner sample PA module. Then, the marginal to the specification is calculated and maximum marginal value is chosen for a specific version. Finally, the maximum marginal values are compared from the greatest to the smallest: the greatest is ranked the best (1) and the smallest the worst (7). As one can see, version 7 seems to be the best in room and cold temperatures but almost the worst in hot temperature. Version 3 seems to be also a good version over the temperatures. The peak power performance is the worst with version 6. Therefore, the conclusion can be reached that when the resonance frequency of transistor's internal matching in output of main and peaking branches varies low from the nominal; the peak power performance is too bad. Decreasing the supply voltage does not reveal any suspicious behavior in corner samples excluding version 2. In room temperature, peak powers in all frequency channels remain approximately the same.

Table 6. Ranking of the corner sample versions according to peak power

	V1			V2			V3			V4			V5			V6			V7		
	C	R	H	C	R	H	C	R	H	C	R	H	C	R	H	C	R	H	C	R	H
Ranking	4	7	3	3	5	2	2	3	1	6	2	4	5	4	5	7	6	7	1	1	6

4.1.2 Efficiency

This section covers the PAE results. Output and input power along with the DC power are measured in such way that output power is the same in all measurements. Equation (15) is used to calculate the PAE.

Results in all three temperatures are presented as a function of frequency in Figure 26, Figure 27 and Figure 28. The PAE value is achieved taking an average of each module's PAE

value in order to minimize the measurement inaccuracy. As expected, the efficiency has be the worst with version 7 in room temperature since it has the best peak power values compared to all other corner sample versions. This goes for the low channel frequency but reference version 1 is the worst at middle and the highest channel frequencies. Also, version 2 is worse than version 7 meaning that modifying the internal matchings of transistor down at the input of both main and peaking branches impairs the efficiency more than modifying the output of main and peaking branches up from the nominal.

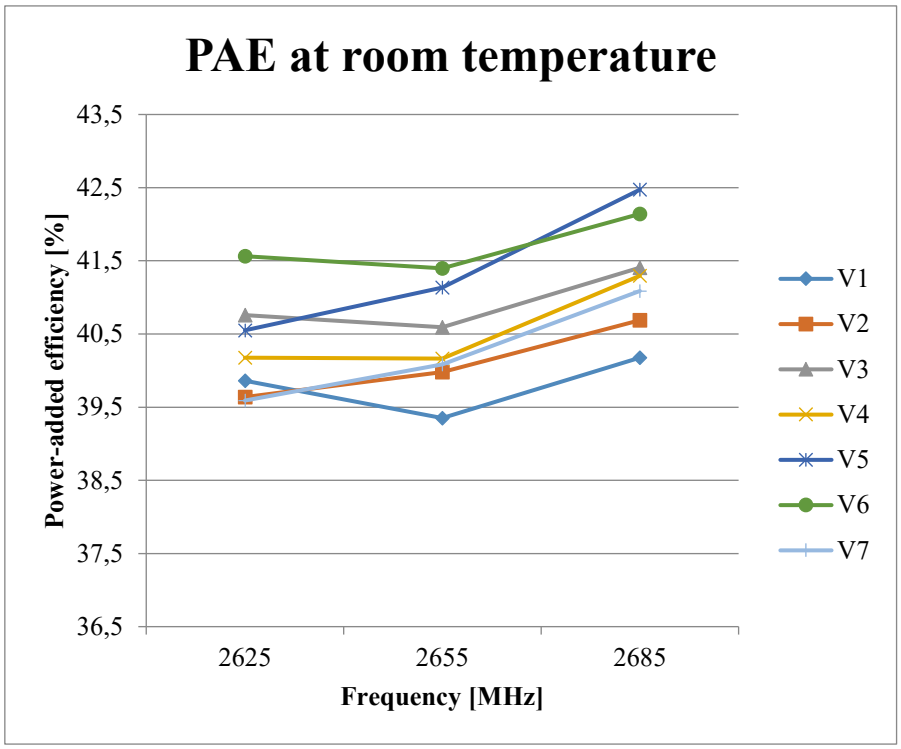

Figure 26. PAE in room temperature over the frequency band.

In cold temperature, overall efficiency is higher compared to the room temperature situation. Version 7 has the worst efficiency as expected from the peak power results whereas version 6 seems to be the best in the lowest and middle channel frequencies. Version 1 and 5 are slightly better in the highest channel frequency.

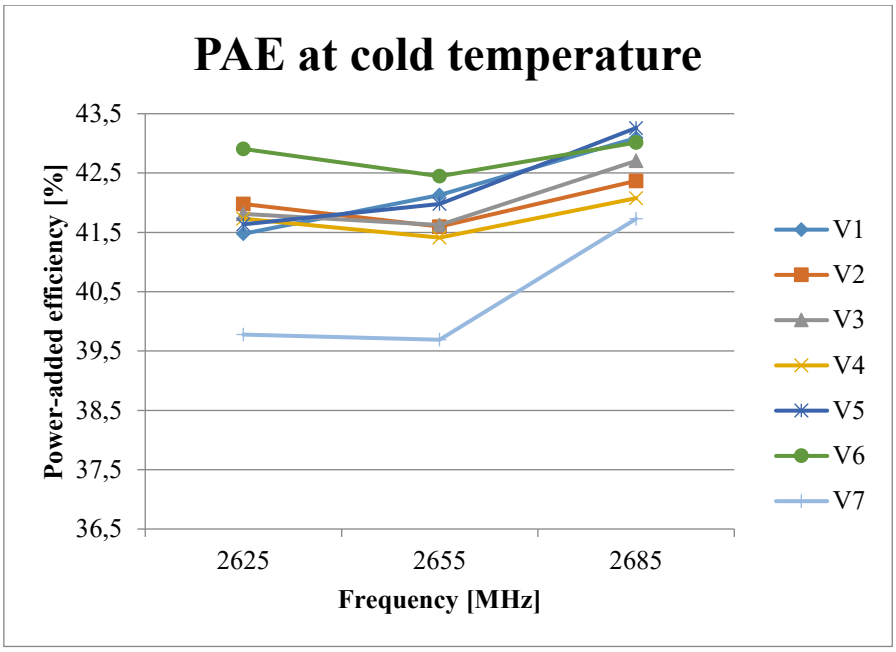

Figure 27. PAE in cold temperature over the frequency band.

Hotter temperature worsens the efficiency compared to room and cold temperatures. Once again, version 7 is the worst. Also, version 6 used to be good in room and cold temperatures but in hot, it does not stand out from average results and in the highest channel frequency its efficiency is quite bad.

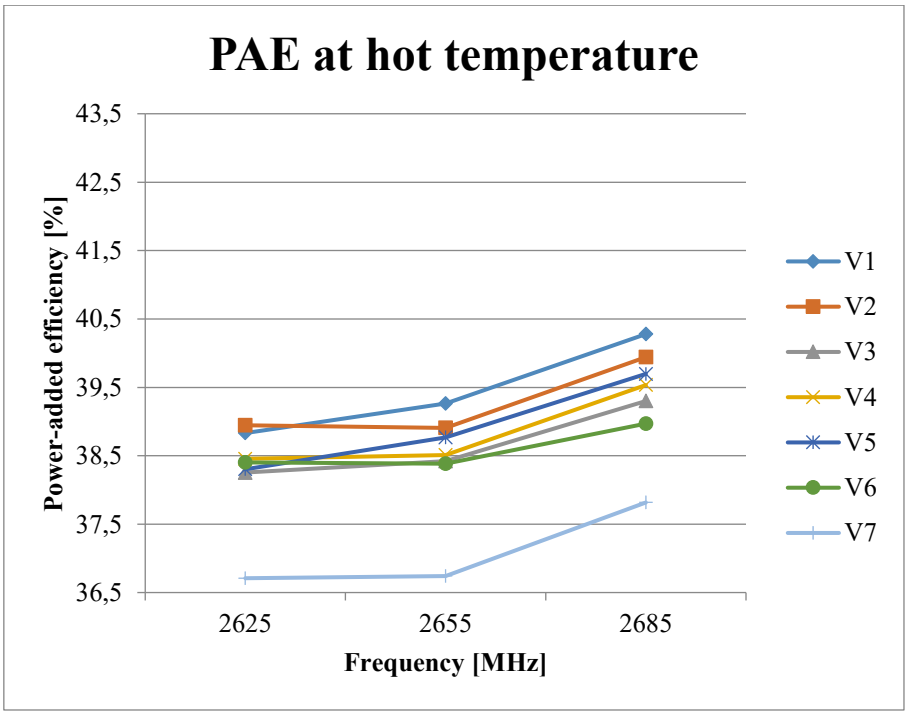

Figure 28. PAE in hot temperature over the frequency band.

Ranking according to the PAE is presented in Table 7. It is made by taking an average of each channel frequency value and choosing the highest to be the best. Version 6 seems to yield to the best efficiency in cold and room temperatures but almost the worst in hot temperature. There is a smaller variance in ranking of version 5 which means it is also a good version.

Table 7. Ranking of the corner sample versions according to PAE

	V1			V2			V3			V4			V5			V6			V7		
	C	R	H	C	R	H	C	R	H	C	R	H	C	R	H	C	R	H	C	R	H
Ranking	3	7	1	5	6	2	4	3	5	6	4	4	2	2	3	1	1	6	7	5	7

4.1.3 Linearization

The suitability of each corner sample PA versions is investigated with two different ACP measurements. These measurements differ from each other by the usage of DPD: non-linearized ACP measurement, which can be called also “raw-ACP”, does not use the DPD. Linearized ACP measurement uses the DPD and LTE20 signal. The reason for taking a look into both ACP measurements will provide wider understanding how each corner sample version behaves with and without DPD and how they will linearize. Asymmetry between higher and lower adjacent channels tells about the amount of distortion products. Also, the greater the asymmetry is, the harder the predistortion is to implement to the PA. Changes of asymmetry in function of temperature and frequency are an expression of memory effects.

Measurement results of non-linearized ACP in all temperatures are presented in Figure 29, Figure 30 and Figure 31. The supply voltage of 32 V and output power of 49.9 dBm is used. It can be easily seen that all versions fulfill the specification of -26.5 dBc and version 2 has the most marginal to the specification. Version 4 seems to have the smallest ACP values. As it can be noticed, the higher adjacent channel has better ACP values. The smallest asymmetry is owned by version 7 while version 6 has the biggest asymmetry in room temperature.

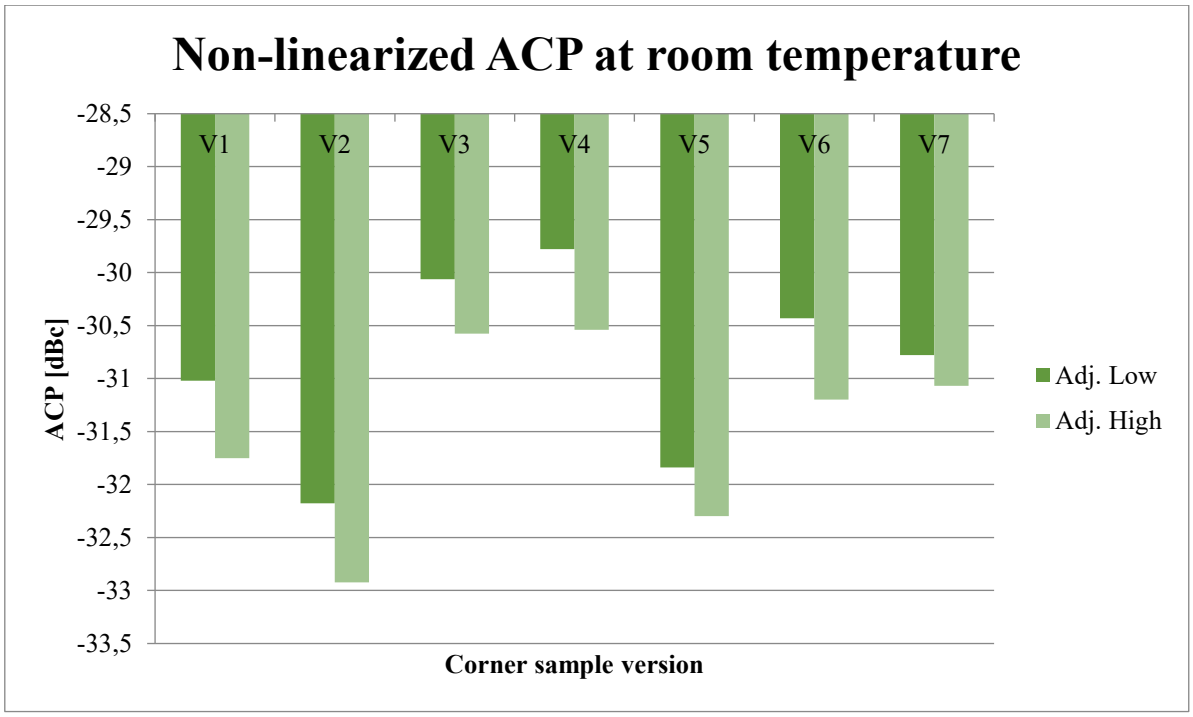

Figure 29. Non-linearized ACP of each corner sample version in room temperature.

The colder the temperature is, the smaller the ACP results are compared to the room temperature. The results of all versions fulfill the specification, though some differences can be noticed. Version 7 in cold temperature is worse than version 6 but in room temperature ACP of lower adjacent channel is better than in version 6. Asymmetries have decreased with almost all versions. Version 7 has again the smallest asymmetry between the lower and higher adjacent channels but version 2 has the biggest this time.

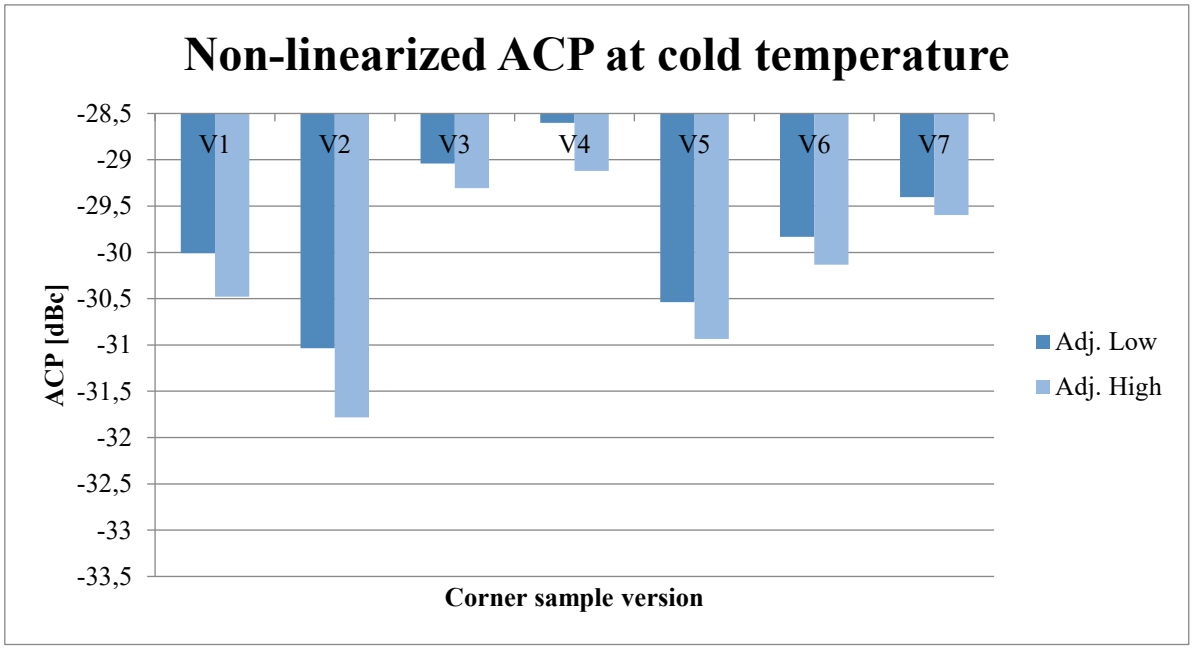

Figure 30. Non-linearized ACP of each corner sample version in cold temperature.

The hot temperature has an increasing effect to the ACP values but when looking for the differences between versions, nothing new is found. All the versions fulfill the specification. Higher adjacent channel ACP's of versions 6 and 7 have the same value while lower adjacent channel ACP is better in version 7. Version 1 has the smallest asymmetry while version 6 has the biggest.

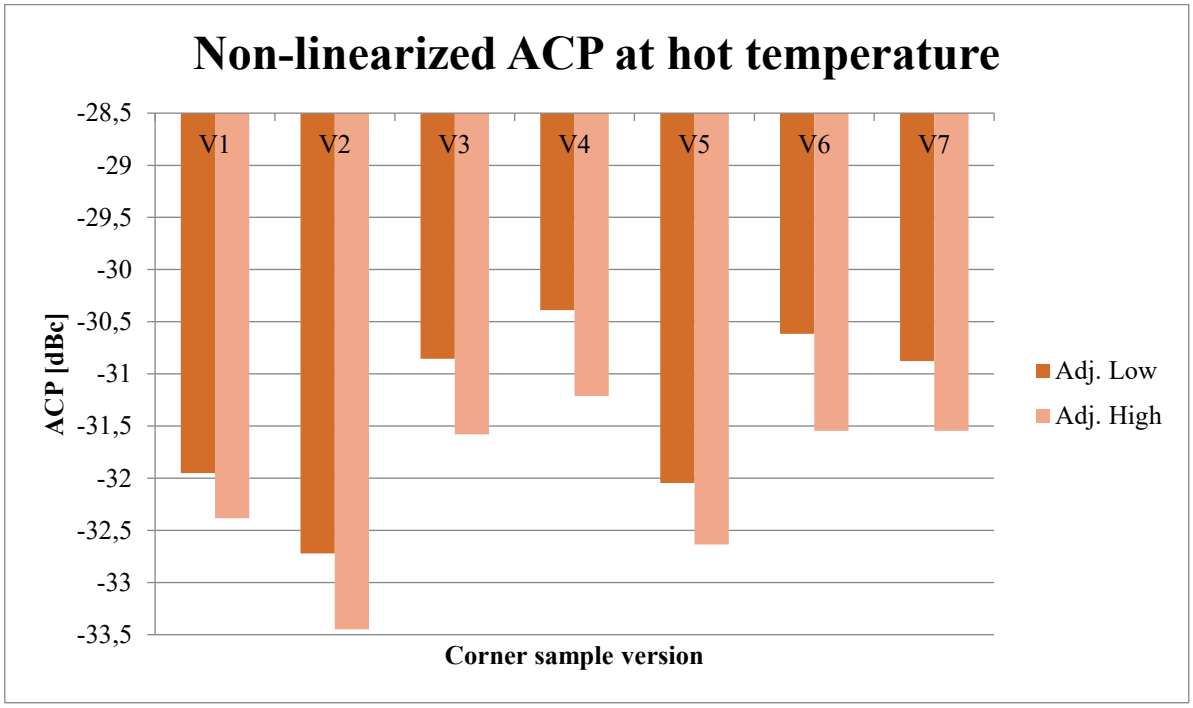

Figure 31. Non-linearized ACP of each corner sample version in hot temperature.

The ranking is achieved by taking an average of low and high ACP values and it is presented in Table 8. Rankings over the temperature are the most stable of all tested parameters. Now it can be seen that version 2 is the best of all versions whereas version 4 has the worst results. When it comes to asymmetry, the variation in ranking is bigger. The smallest asymmetry is owned by version 7. It is the version with highest peak power and the worst efficiency. Version 6 has the biggest asymmetry in room and hot temperatures.

Table 8. Ranking of all corner sample versions according to the non-linearized ACP

	V1			V2			V3			V4			V5			V6			V7		
	C	R	H	C	R	H	C	R	H	C	R	H	C	R	H	C	R	H	C	R	H
Ranking	3	3	3	1	1	1	6	6	4	7	7	7	2	2	2	5	5	6	4	4	5
Ranking according to the asymmetry	5	4	1	7	5	5	2	3	4	6	6	6	4	2	2	3	7	7	1	1	3

As the behavior of linearization of corner sample versions without DPD is known, the behavior with DPD is investigated next. The used signal configuration is LTE20 while supply voltage and output power are remaining the same. Test results are presented in Figure 32, Figure 33 and Figure 34. With DPD, the low and high adjacent results are contrary to non-linearized results except with the version 4 in room temperature. Version 4 seems to be the

worst in room temperature while version 3 reaches the best ACP result in lower adjacent channel. On the other hand, versions 2, 3 and 6 have over 1 dB difference between lower and higher adjacent channel ACP's while other versions have smaller than 1 dB difference. More accurately, the biggest asymmetry is seen with version 3 and the smallest with version 4. The specification is fulfilled with all corner sample versions.

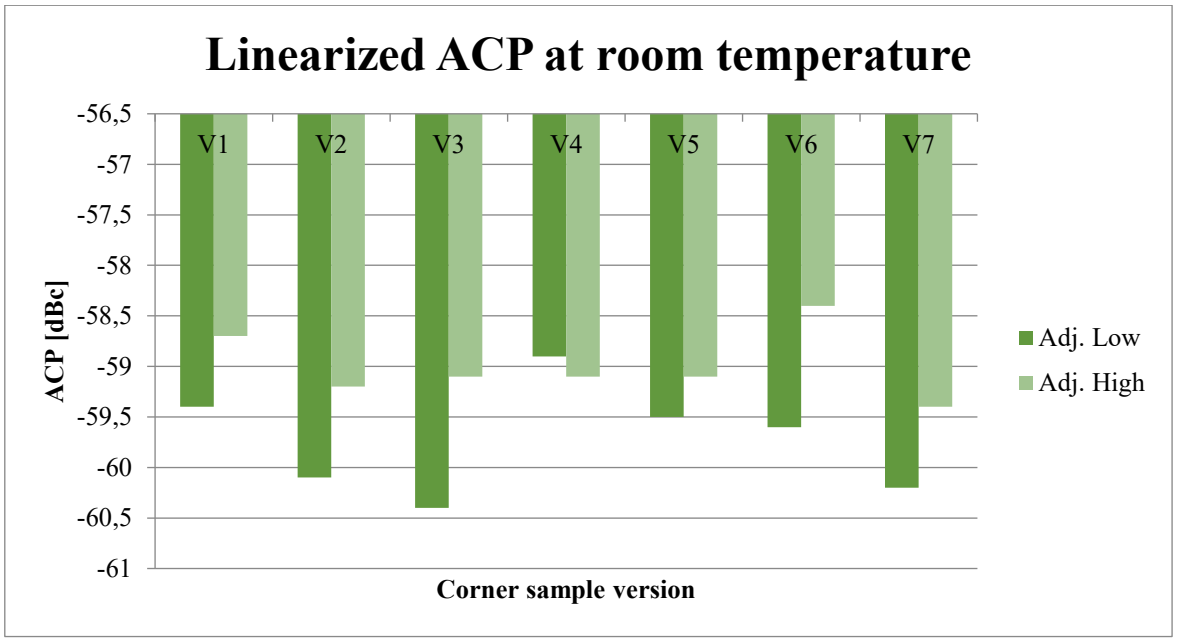

Figure 32. Linearized ACP of all corner sample versions in room temperature.

Test results in cold temperature are lower than in room temperature, as expected. Version 4 used to have deviating results in room temperature compared to other versions but now, the trend is the same with all versions. Differences between lower and higher adjacent channel results are smaller than in room temperature with versions 2 and 3. When taking a look in versions 6 and 7, the difference is approximately 0.5 dB bigger than in room temperature. Also, version 4 has a 1.5 dB difference between lower and higher adjacent channel results. To conclude, version 6 has the biggest asymmetry and version 2 has the smallest.

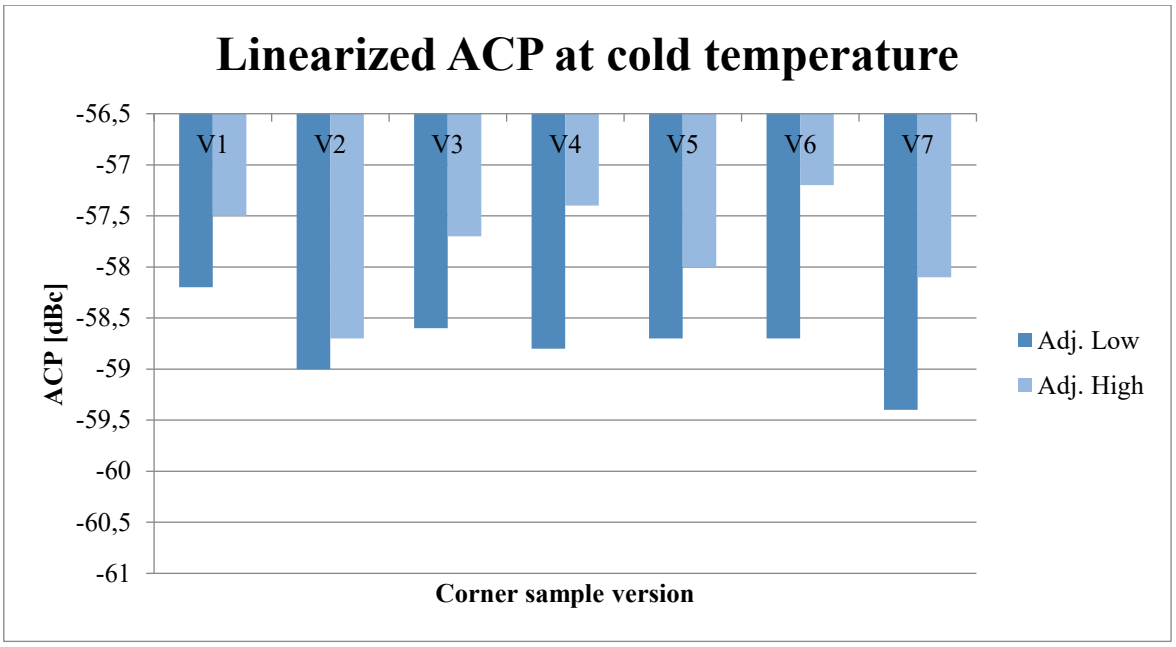

Figure 33. Linearized ACP of all corner sample versions in cold temperature.

In hot temperature, the ACP results have increased from the room temperature. As it can be noticed, there are no results for version 6. The reason for a blank cap is that it does not linearize in hot temperature. The measurement cannot be done close to our target power level while our comparison needs to be done with target output power level. The biggest difference between lower and higher adjacent channel ACP is seen with version 1. When it comes to version 2, the difference is the greatest in hot temperature compared to room and cold temperatures. Version 4 has a smaller difference than in cold temperature. All in all, the biggest asymmetry is seen with version 1 and the smallest is owned by version 4.

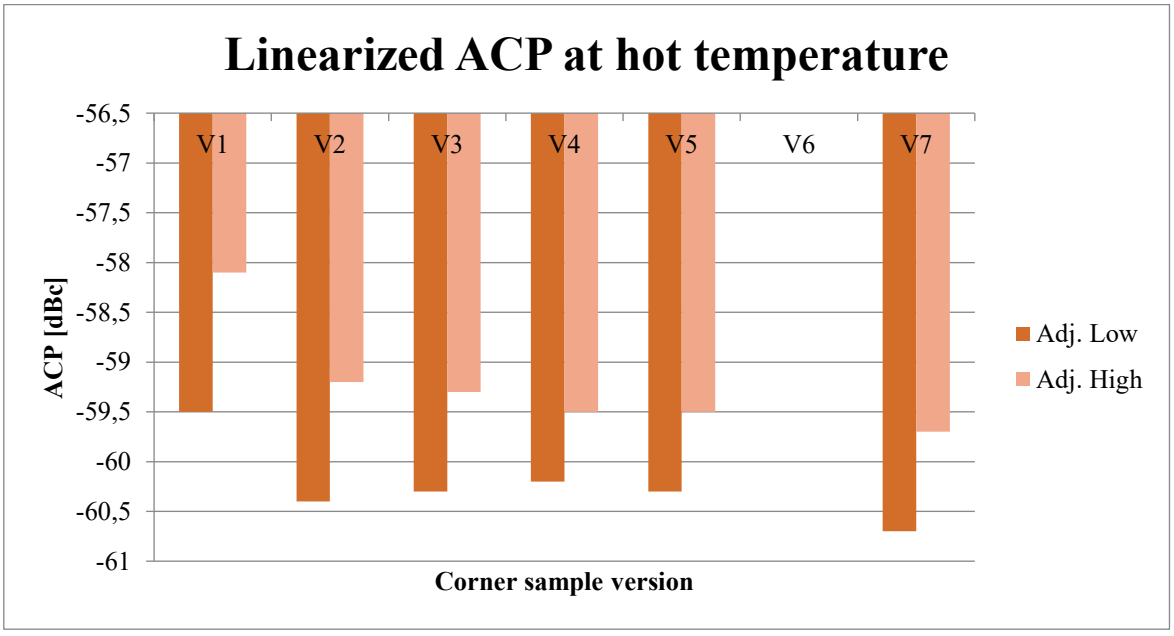

Figure 34. Linearized ACP of all corner sample versions in hot temperature.

The ranking is made the same way as with non-linearized ACP's and it is presented in Table 9. Compared to the ranking table of non-linearized ACP's, version 7 seems to linearize the best with DPD while version 2 linearized the best without DPD. However, the asymmetry presented in Table 8 was the smallest with version 7. It can be concluded that a corner sample version with the smallest asymmetry linearizes the best. A conclusion can be made that when the transistor's internal resonance frequency of output of main and peaking branches is tuned up from the nominal and DPD is used, the PA linearizes the best in all temperatures. When it comes to asymmetry ranking, version 4 manages the best in room and hot temperatures. In cold, the performance decreases a lot due to possible intolerance of distortion components. As for version 6, both rankings tell that the greater the asymmetry is, the worse the overall performance with linearization is.

Table 9. Ranking of all corner sample versions according to the linearized ACP

	V1			V2			V3			V4			V5			V6			V7		
	C	R	H	C	R	H	C	R	H	C	R	H	C	R	H	C	R	H	C	R	H
Ranking	7	5	6	1	3	5	4	2	4	5	6	3	3	4	2	6	7	7	2	1	1
Ranking according to the asymmetry	3	3	6	1	5	5	4	7	4	6	1	1	2	2	2	7	6	7	5	4	3

4.1.4 Gain

High gain at the final stage is a wanted feature of a PA due to the total efficiency as equation (16) shows. However, the total gain is wanted to be as low as possible since the background noise increases when the gain is higher. A stable gain over the temperatures and frequency band is ideal. Thus, the effect of temperature is approximately 3-5 dB upwards or downwards. Gain ripple is another important measurement. It is simply a subtraction of maximum and minimum gain. Failures in gain and ripple can be fixed by adjusting the bias values and temperature compensation and therefore, the ripple is not investigated as precisely as maximum and minimum values. The used supply voltage is 32 V and the output power is 49.9 dBm.

Measurement results of maximum and minimum in-band gain are presented in Figure 35, Figure 36 and Figure 37. As one can see, the highest gain is owned by version 2. On the other hand, version 3 has the worst maximum gain remaining below 45 dB compared to other versions. Gain ripple is the biggest with version 2 remaining more than 1 dB. This means that high gain is achieved by tuning the input resonance frequency down from the nominal in the cost of in-band gain ripple.

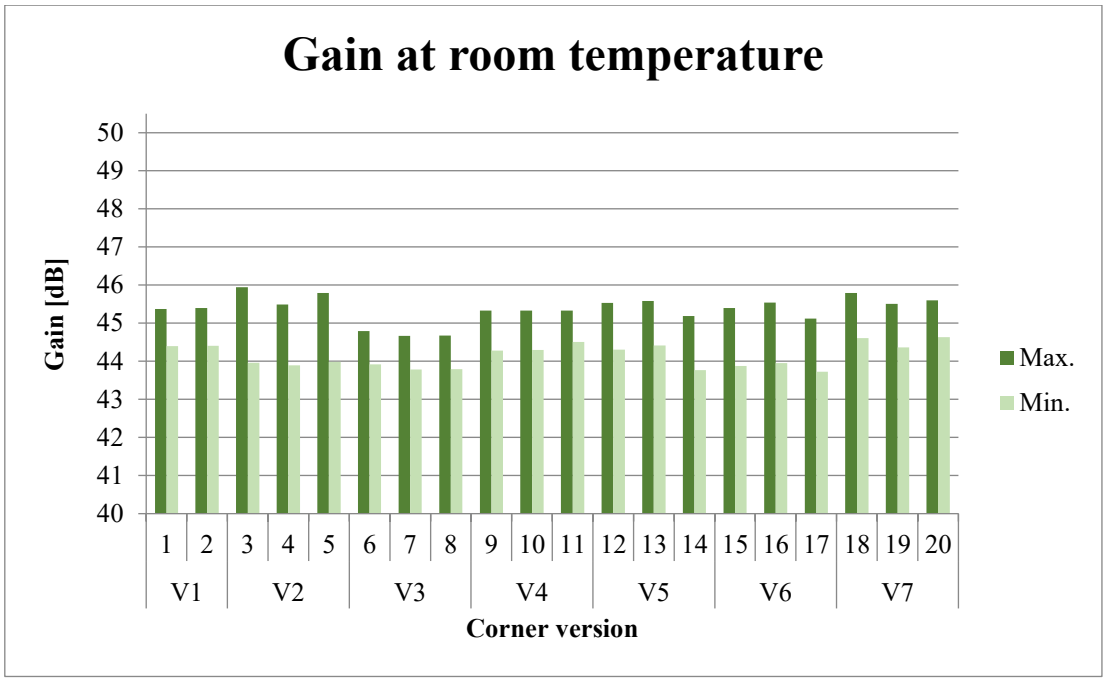

Figure 35. Maximum and minimum gain of all corner sample versions in room temperature.

In cold temperature, board number three exceeds the 50 dB upper limit specification. Boards four and five are clearly below the 50 dB limit which leads to the fact that variance is bigger in cold temperature with version 2. Cold temperature increases the gain.

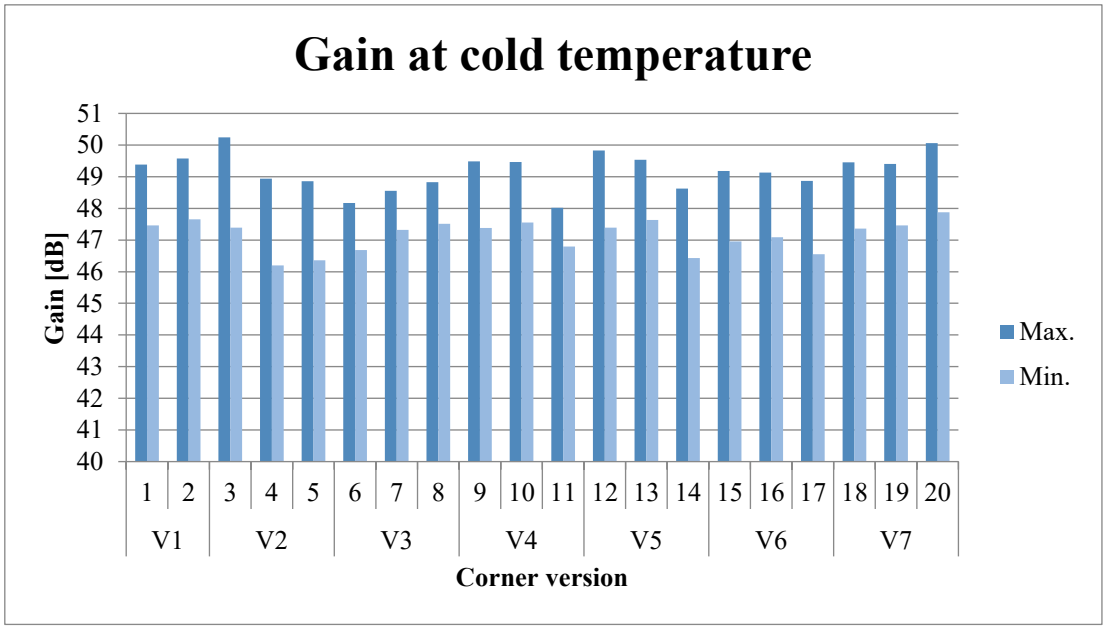

Figure 36. Maximum and minimum gain of all corner sample versions in cold temperature.

Gain ripple situation is a little better in hot temperature which decreases the gain compared to room temperature. Versions 2 and 7 have the highest maximum gain while version 6 has the lowest minimum gain.

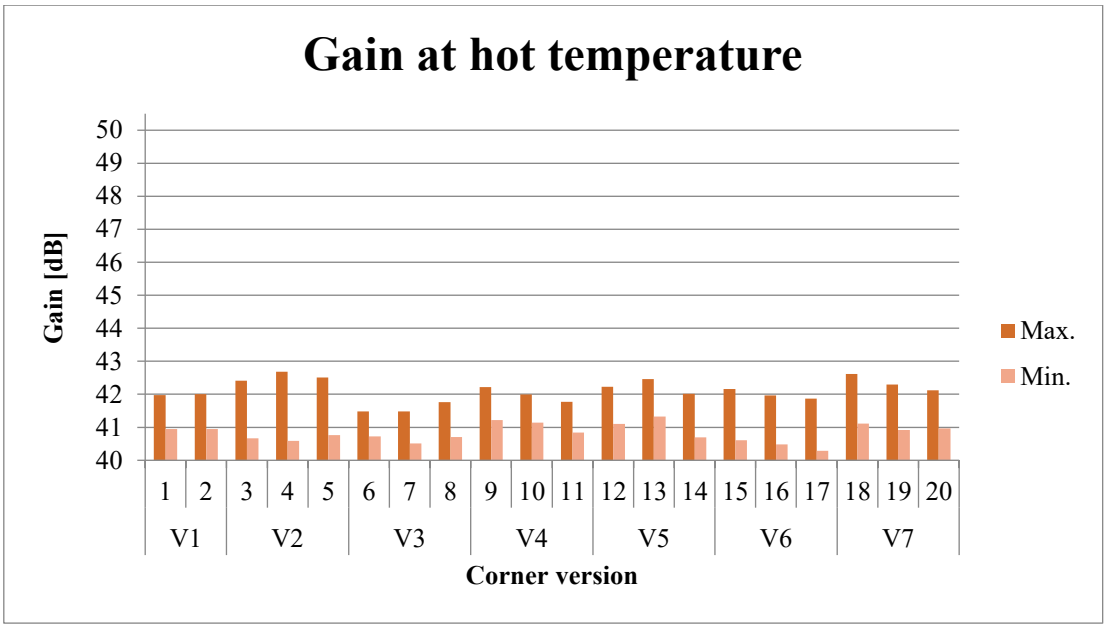

Figure 37. Maximum and minimum gain of all corner sample versions in hot temperature.

Ranking of the corner sample versions according to gain is presented in Table 10. The ranking is made by taking the average of maximum gain value and ordering the versions. Versions 2 and 7 seem to be the best over the change of temperature. When considering the effect of tuning the resonance frequency of output main and peaking branches down from the nominal, it provides high peak power and gain but the worst efficiency. The best efficiency is achieved with versions 5 and 6. Gain of these versions is on average level, version 5 approaching a better performance especially in room and hot temperature. Peak power of version 5 is also on average level whereas the peak power of version 6 is the worst of all versions. The lowest gain is held by version 3 where the input matching resonance frequency of both main and peaking branch is tuned up from the nominal. Version 3 has an average efficiency and quite good peak power values. From the efficiency point of view, version 5 has the best efficiency while the gain is approximately the third best.

Table 10. Ranking of the corner sample versions according to gain

	V1			V2			V3			V4			V5			V6			V7		
	C	R	H	C	R	H	C	R	H	C	R	H	C	R	H	C	R	H	C	R	H
Ranking	2	4	6	3	1	1	7	7	7	6	6	5	4	3	3	5	5	4	1	2	2

4.2 Statistical analysis and process capability indices

As the electrical functionality of corner sample modules is known, the way how the corner sample module population behaves statistically is investigated next. Measurement results of each parameter will be scrutinized with lognormal distributions and process capability indices. When it comes to C_{pk} values, equation (20) in section 3.3.2 will be used in cases of two specification limits as itself. Parameters such as peak power and ACP's have either upper or lower specification limit. In cases like this, C_{pk} is calculated as shown in the equation (20) but using only the division depending on the type of specification limit. C_{pk} suits well for this work when the value is one or greater. If the RF parameters are scrutinized in Six Sigma

manner, the C_{pk} value of two or greater is wanted. However, the number of tests is quite small in R&D and therefore the Six Sigma requirements suits better in analysis of production data. Table presented in [12] tells that the process yield of C_{pk} of one is 93.3 %. However, calculated C_{pk} values in following sections are approximates meaning that these values are not supposed to predict the final production outcome. The values are calculated to support the design optimization.

4.2.1 Peak power

Test conditions of this analysis are the following: supply voltage is 32 V, output power is 49.9 dBm and the used frequency channel is 2655 MHz. Figure 38 presents the lognormal distributions of measured peak power results in all temperatures in middle frequency channel. Dashed lines are the specification limits and thin solid lines are the peak power means of each temperature. The type of the specification is a lower limit: measurement result fails if it is under the limit. One can see that all bell curves concentrate above the specification limits which means that the measurement process in this particular case provides an adequate quality and the process is capable. The shapes and sizes of curves differ from each other. The curve of room temperature is the widest of all curves which means that the standard deviation is the largest. Standard deviation in hot temperature is the smallest of all temperatures. When taking a look into the mean lines and bell curves, the way how results are centered compared to the mean can be seen. In cold temperature, the results are uniformly distributed in the both sides of the mean. The situation at room temperature is a little different since most of the results locate below the mean whereas the situation in hot temperature is contrary.

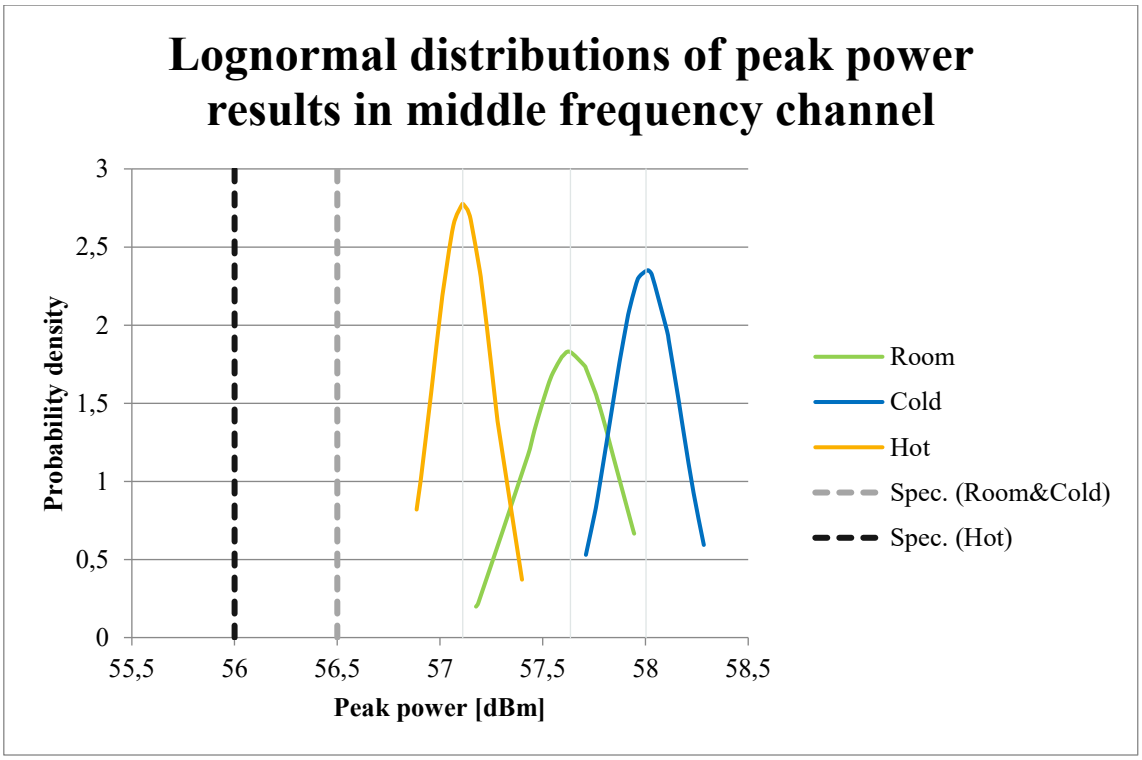

Figure 38. Peak power results of middle frequency channel presented in bell curves.

As measurement results presented in section 4.1.1 showed, failures are present in the highest frequency channel. Figure 39 presents the lognormal distributions of peak power in the highest frequency channel. Curves cross the specification limits in hot and room temperature. The greatest standard deviation is seen in room temperature, though all bell curves are wider compared to middle frequency channel in Figure 38.

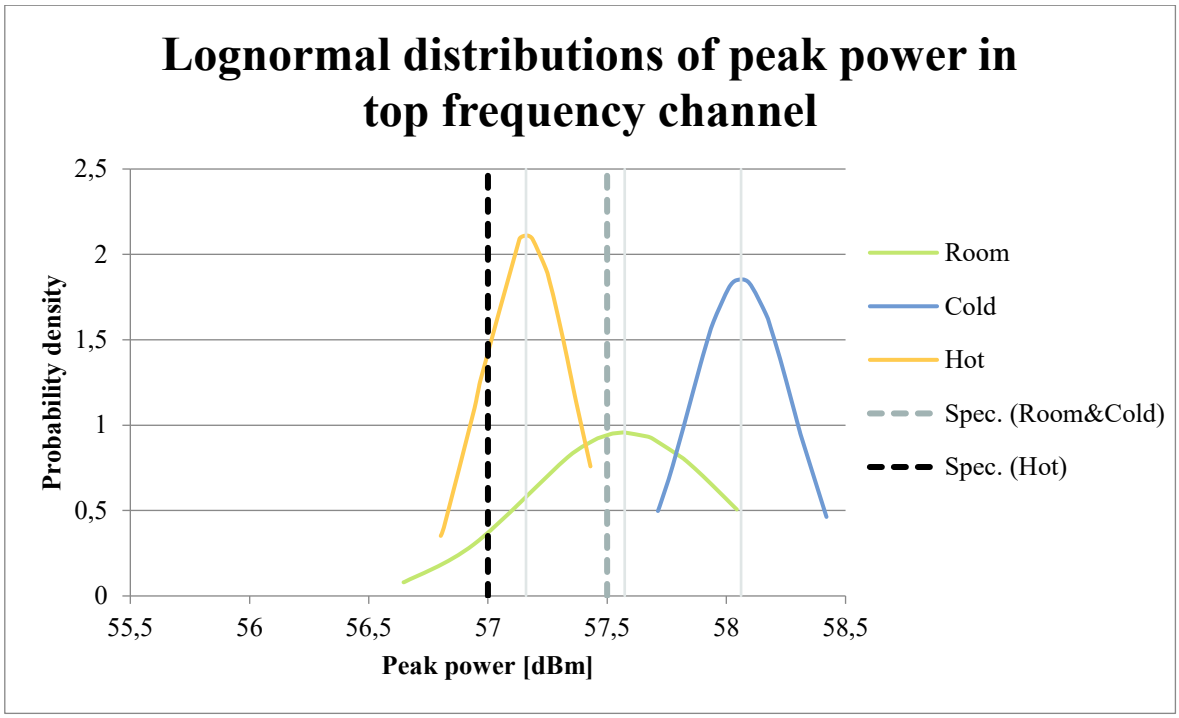

Figure 39. Peak power results in the highest frequency channel presented in bell curves.

C_{pk} values of all temperatures are presented in Table 11. Values support the bell curves in Figure 38 and Figure 39. Situation in middle frequency channel is much better than in the highest frequency channel meaning that peak power need to be optimized higher. While the bell curve of cold temperature does not cross the specification limit, the C_{pk} is still quite poor.

Table 11. Process capability indices of peak power values

	Room	Cold	Hot
C_{pk}, middle frequency channel	1.734	2.957	2.575
C_{pk}, highest frequency channel	0.059	0.871	0.282

4.2.2 Efficiency

The specification limit of 39 % is chosen particularly for this thesis and for this use case in room temperature. The analyzed results use the supply voltage of 32 V, output power of 49.9 dBm and middle channel frequency. Since PAE is a unitless metric, the normal distribution suits better for this analysis. The normal distributions of corner samples are presented in Figure 40. The type of specification is lower limit and immediately one can notice that all results are failing more or less. Standard deviations do not differ from each other much while cold temperature has the biggest and room temperature has the smallest. The results are

centered below the mean in hot and cold temperatures and in room temperature the results are centered above the mean.

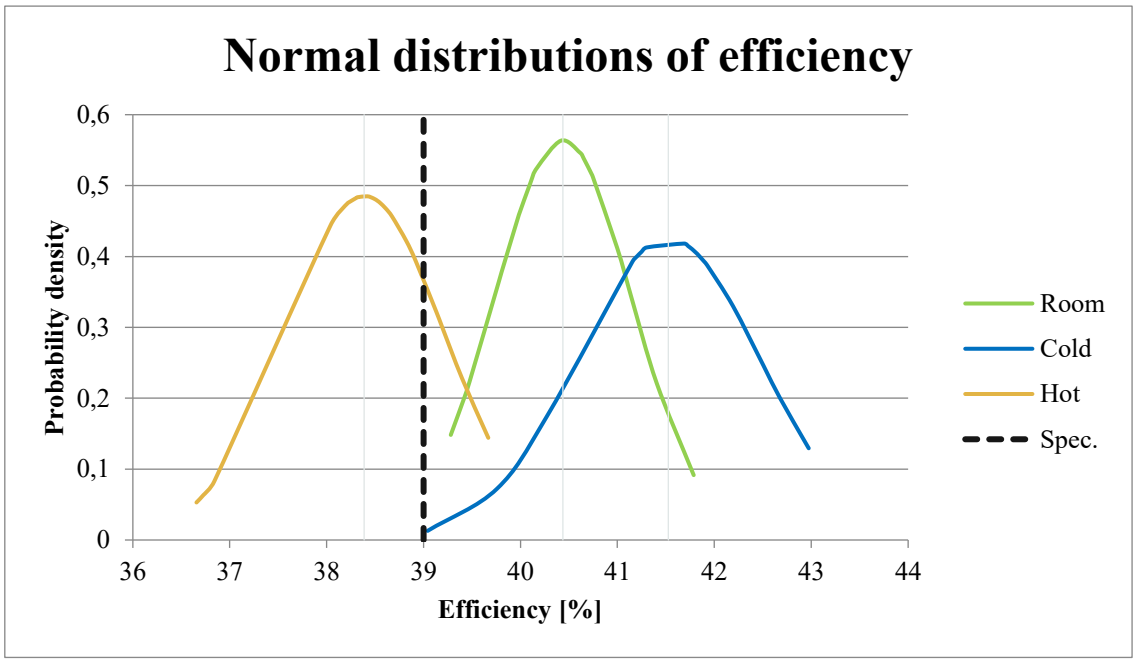

Figure 40. Efficiency bell curves of all corner samples.

Since the limit is set to 39 %, the process capability indices presented in Table 12 become interesting. The smaller the value of C_{pk} is, the worse the situation is compared to the limit. As one can conclude, the negative C_{pk} refers to the situation that the process is not capable with the specific limit.

Table 12. Process capability indices of efficiency

	Room	Cold	Hot
C_{pk}	0.677	0.896	-0.249

4.2.3 Non-linearized ACP

Only the non-linearized ACP is investigated since the amount of measured modules is too little in linearized ACP. Figure 41 presents the lognormal distributions of non-linearized ACP in all temperatures when the used supply voltage is 32 V and the output power 49.9 dBm. The average of low and high channel ACP has been taken of each module to simplify the figure. Standard deviation of each temperature does not differ much but it is the smallest in hot temperature and the largest in cold temperature. In all temperatures, the measured results have centered below the mean.

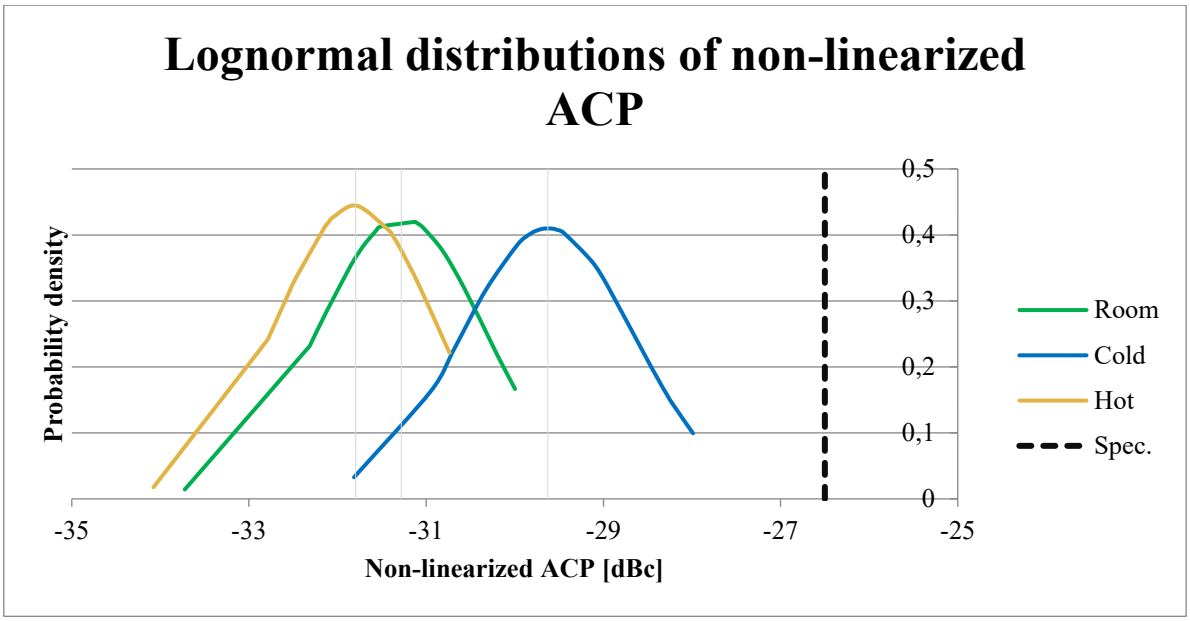

Figure 41. Non-linearized ACP bell curves of all corner samples.

The testing process of non-linearized ACP is capable since the process capability indices presented in Table 13 are more than one. As expected, the C_{pk} of cold temperature is closest to value one since the ACP is highest in cold. Also, the C_{pk} of hot temperature is furthest of one due to low ACP values.

Table 13. Process capability indices of non-linear ACP

	Room	Cold	Hot
C_{pk}	1.70	1.071	1.966

4.2.4 Gain

Maximum and minimum gain is investigated to see the behavior of both in relation to the upper and lower specification limit. The used supply voltage is 32 V and the output power is 49.9 dBm. Figure 42 presents the lognormal distributions of maximum gain. The standard deviation is the largest in cold temperature which crosses the upper specification limit. At room and hot temperature, the standard deviations are smaller than in cold.

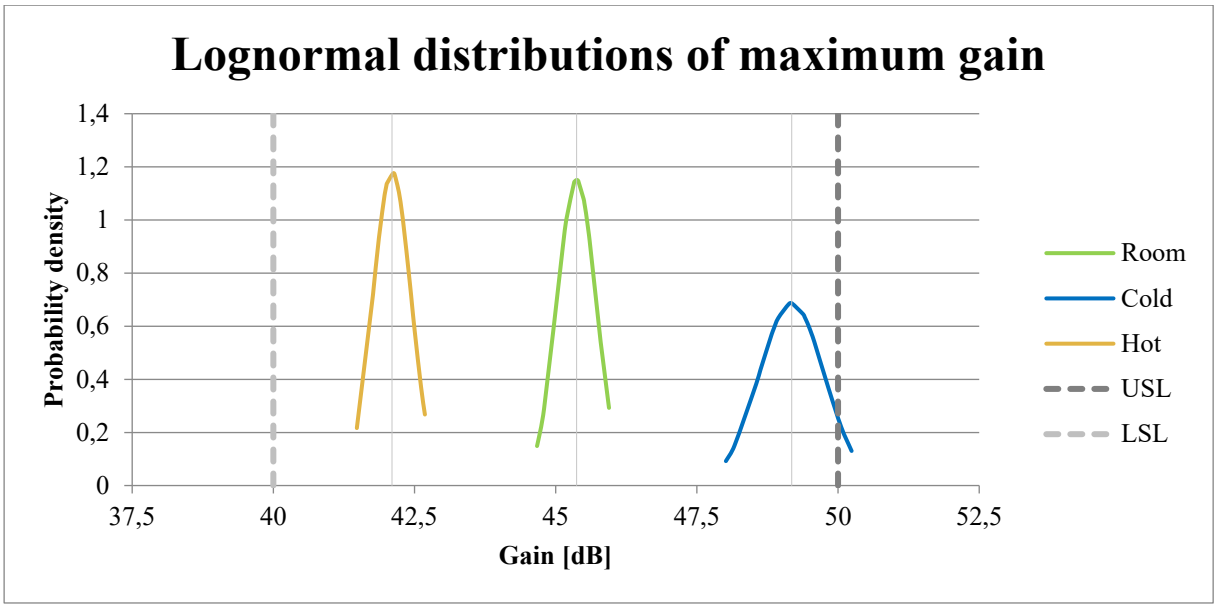

Figure 42. Maximum gain bell curves of all corner samples.

Lognormal distributions of minimum gain are presented in Figure 43. All the distributions are within the specification, hot temperature closest to the limit. As in the maximum gain situation, the standard deviation of cold temperature is the largest.

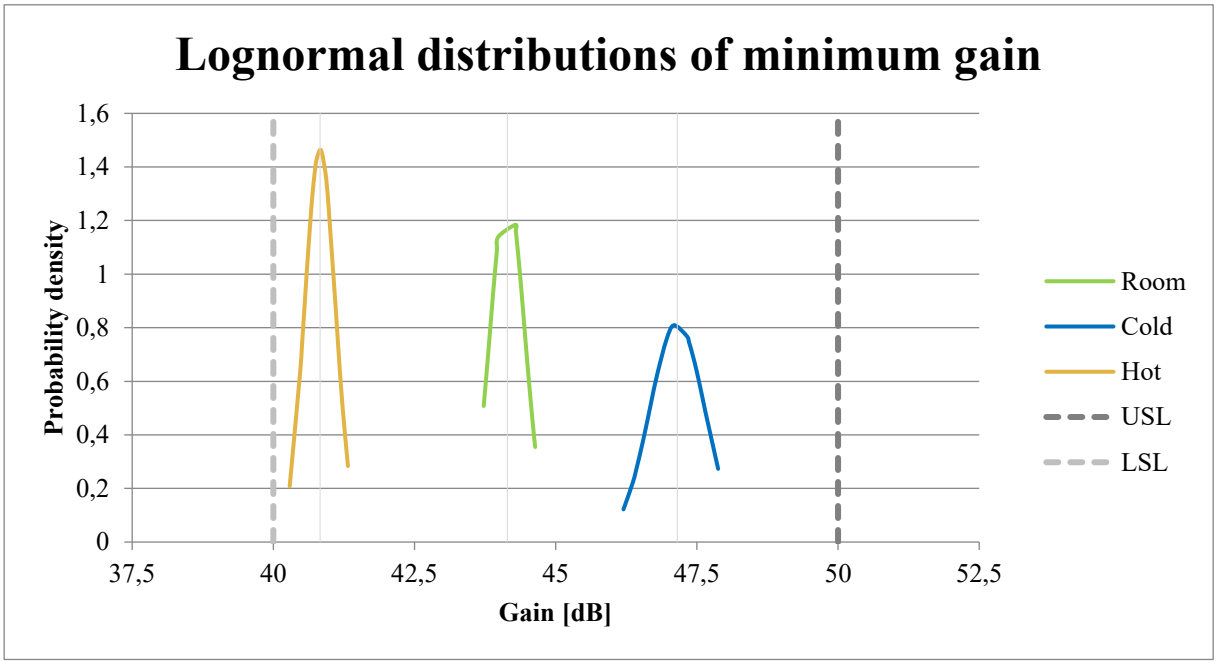

Figure 43. Minimum gain bell curves of all corner samples.

Process capability indices of both measured gains are presented in Table 14. The C_{pk} value of maximum gain in cold temperature is less than one as it should. Minimum gain in hot temperature is close to failure.

Table 14. Process capability indices of maximum and minimum gain

	Room	Cold	Hot
C_{pk}, max.	4.452	0.470	2.069
C_{pk}, min.	4.532	1.940	1.013

4.3 Conclusion of test results and decided design changes

The purpose of this chapter is to conclude the test results and make a decision of the design changes. As told in section 2.3.1, the most wanted features are high gain of the final stage, good efficiency, high peak power and that PA linearizes well. The ranking of test results is simplified by summing all the numbers over the temperature together to see better which version is the best in essential parameters. The final ranking is presented in Table 15 from which one can see that version 6 has the worst peak power. It means that it is chosen for tuning. Version 7 seems interesting choice for design optimization goal since it has high gain and peak power and it linearizes the best, but the efficiency is the worst. The earlier justified facts are proven when looking at the Table 15. Version 3 shows that high peak power actually leads to poor gain whereas version 5 shows that the efficiency and gain are good while peak power performance is not the best possible.

Table 15. The final ranking of corner sample versions

	V1	V2	V3	V4	V5	V6	V7
Peak power	4	3	1	5	6	7	2
Efficiency	3	5	4	6	1	2	7
Non-linearized ACP	3	1	5	7	2	5	4
Linearized ACP	6	3	4	5	2	7	1
Gain	4	1	7	6	3	5	1

As the final ranking is presented, the comparison between reference and other versions can be done. When the transistor's internal resonance frequency of input main and peaking branches is tuned down, peak power and gain increase while worsening the efficiency. It should not be forgotten that this version has a large variety between frequency channels in peak power as Figure 17 shows. Down-tuning seems to effect on the linearity in a positive way. Version 3, where the internal resonance frequency of input main and peaking branches is tuned up, shows that the gain outperforms contrary to the version 2. Peak power is the best of all versions. Version 3 linearizes better compared to the reference version, but non-linearized ACP is worse. Tuning the input of main branch down and input of peaking branch up worsens almost all parameters but linearized ACP. Up-tuning the input main branch and down-tuning the peaking branch leads to the best efficiency in the cost of peak power. Version 5 linearizes well and the gain is good also. In version 6, the matching in the output main and peaking branches is tuned down which causes decrease in peak power and linearized ACP. As expected, efficiency is good due to poor peak power which is unconventional since low gain at the final stage does not provide good efficiency usually. The gain might have worsened due to non-optimal input matching for this type of output matching. Up-tuning the resonance frequency of the same parts of the PA confirms this unusual gain-efficiency relation when looking the rankings of version 7. But then, version 7 linearizes well with DPD and the peak

power aims sufficient values. It can be concluded that when the matching changes in the output side, the unusual relation between gain and efficiency is created.

Statistically most of the results and their measurement processes have a good distribution. The process capability index of peak power results in room temperature tells that the mean of results could be focused a little higher or the deviation of results has to get smaller in order to guarantee a sufficient quality. When taking a look in Figure 40, the most notable affair is the large variety of efficiency results. The actual difference between the maximum and minimum efficiency in room temperature is 2.5 %, in cold temperature 3.9 % and in hot temperature 3 %. These differences are huge compared to the difference of reference version 1 which holds the difference of 0.2 %. However, it is positive that the results in room and cold temperature are concentrated over the 40 % limit. Non-linearized ACP's have no issues statistically: means are focused far enough from the specification limit providing good Cpk values. Maximum gain in cold temperature crosses the upper limit which can be also noticed from the process capability index which is less than one. Also, the minimum gain in hot temperature is close to the lower limit. In order to ensure the quality, fine-tuning of the distributions may be done to fit better between specification limits.

Adjustment of bias values was the most effecting change that can be made to the existing design and usually, it is always checked if the design change could be just adjustment of biasing. Also, places for two capacitors in the external input matching network of main branch were added to the schematic along with the delay line length increasing. Corner sample versions 1, 3 and 6 are selected for testing again with same modified bias values, elongated delay line and added capacitors due to their performance in peak power. Peak power is tested again at room and hot temperatures. The overall performance is better in cold temperature as can be seen from section 4.1.1 and therefore it is not tested. Figure 44 and Figure 45 help with comparison of the effect of bias change. Effect in nominal version is the biggest in both temperatures. The average increase is 0.5 dB which means that specification is fulfilled in all channels and peak power is statistically under control. In version 3, the variance between frequency channels is smaller with new biasing holding an average increase of 0.1 dB. The highest channel in version 6 does not seem to be impressed by bias change. The average increase is the same with version 3. To conclude, the bias change makes the peak power performance as required in room temperature with the best and the worst corner sample version leading for higher C_{pk}.

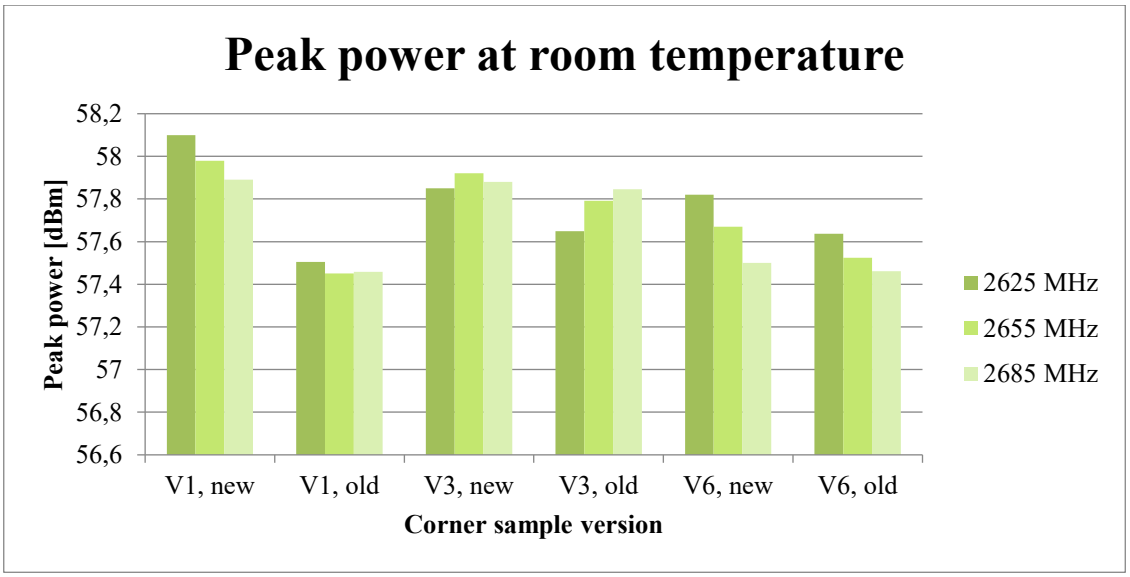

Figure 44. Comparison between corner sample versions with old and new bias values in room temperature.

Peak power results with version 1 in hot temperature have smaller variance between frequency channels than in room temperature. Results have increased approximately 0.4 dBm. When it comes to version 3, the balance between middle and the highest frequency channel is better with new biasing which increases the peak power performance approximately 0.2 dBm. The lowest channel is 0.2 dB worse than middle and the highest, but fulfills the specification requirement of 57 dBm. Version 6 has got much better from the old biasing: approximate increase is 0.5 dBm. Though, the variety between frequency channels is twice bigger compared to the old biasing. The lowest frequency channel in version 3 and all the frequency channels in version 6 failed before the new biasing. Therefore, the adjustment of biasing and adding capacitors is a correct design change since the mean of peak power results have to be concentrated higher from the present situation.

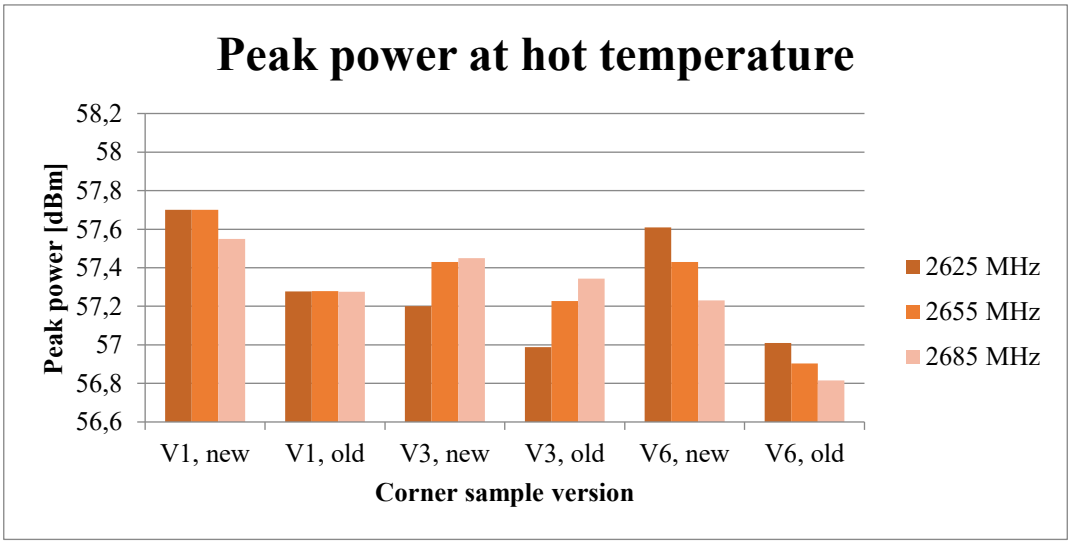

Figure 45. Comparison between corner sample versions with old and new bias values in hot temperature.

Statistical behavior is observed with six PA modules from the design with hardware fixes and new biasing. Due to much smaller amount of measured modules compared to the corner samples, following figures and a table are skewed and thus approximate proof of successful design optimization. Also, larger amount of PA modules also could give more accurate standard deviations. Lognormal distributions of peak power in middle channel frequency are presented in Figure 46. Compared to the specification limits, the lognormal distributions of these six modules are concentrated higher than in Figure 38. Otherwise, the peak power means have increased approximately 0.52 dB.

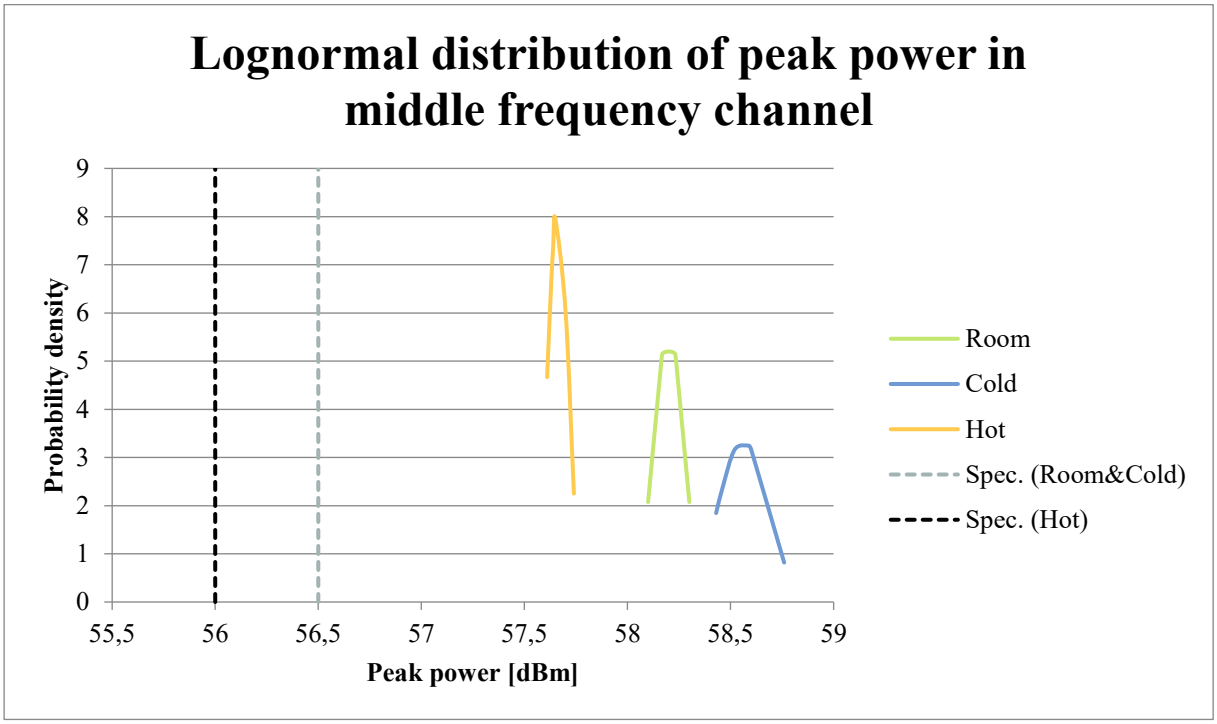

Figure 46. Bell curves of peak power results in middle frequency channel after modifications.

There were failures with corner samples in the highest frequency channel as Figure 39 shows. Though, situation is also much better after the modifications as Figure 47 presents. The parameter mean has increased approximately 0.58 dB in the highest channel frequency.

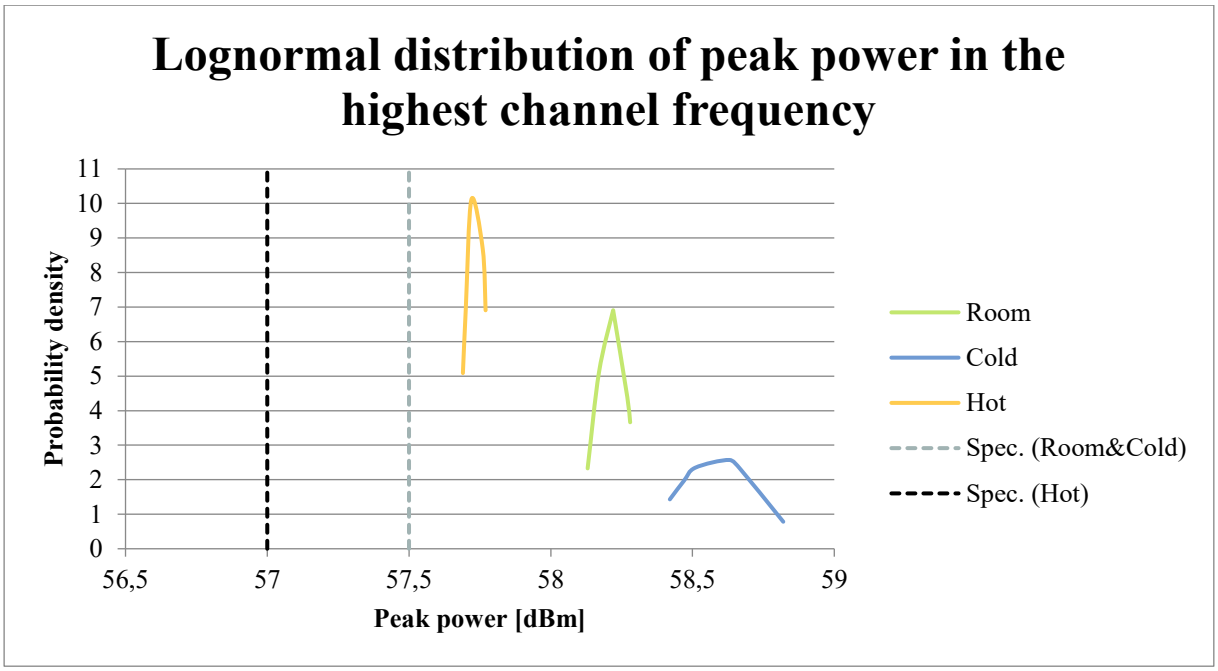

Figure 47. Bell curves of peak power results in the highest channel frequency after modifications.

Comparison of C_{pk} values can be done with help of Table 16. Even though the values are more realistic with larger number of measured modules, the values show that modifications have an increasing impact on process capability, especially in the highest frequency channel.

Table 16. Comparison of C_{pk} values before and after modifications

	Room, after	Room, before	Cold, after	Cold, before	Hot, after	Hot, before
C_{pk}, middle frequency channel	8.014	1.734	5.762	2.957	11.362	2.575
C_{pk}, highest frequency channel	4.143	0.059	2.436	0.871	2.164	0.282

5 DISCUSSION

The main goal of this thesis was to optimize the PA module design in a way it is able to tolerate the productional variance in RF parameters of peak power, gain, linearization and efficiency. Design procedure is based on measurement data analysis and hardware, temperature compensation table and bias tuning which gives more realistic results than simulation models. Thus, usually transistors are also in R&D phase along with the PA module since the co-functionality of both PA module and transistor is wanted to be the best. Moreover, no simulation models for transistor are available. Otherwise, the measurement and hardware tuning method enable the statistical data analysis due to large amount of PA modules. Measurements itself take more time than simulations since the reliability of measurement setup need to be ensured and instead of one simulated module, there are more modules to be measured. Furthermore, it is essential to measure the actual performance with linearization. As it can be concluded, the design optimization process was successful without any simulation models since the performance got better.

Inspection of statistical distributions and process capability indices of RF parameters broaden the dimensions of design analysis. Usually, only the measurement results are observed in R&D environment while statistical analysis with realistic production variety has less weight. Nevertheless, statistical analysis suits well in builds which are aiming for illustration of factors causing possible variety in overall performance of PA module. In addition to corner sample build, 2^{nd} source build is another chance to exploit statistical analysis methods. It is manufactured in order to see the impact of components by "2^{nd} choice" manufacturers in PA performance. Analysis of C_{pk} values is often used for production measurements since the value tells about the quality of production line and the manufacturing process. Also, the amount of tested PA modules in production is much larger than in R&D environment. The possibilities of using C_{pk} values in R&D environment as a part of design process should be taken into account since it creates the information about the measurement environment as well as reliability of RF parameter test specification. Six Sigma is a common tool for process and quality improvement which provides a certain value of C_{pk} in order to ensure the process fulfills the Six Sigma requirements. If the Six Sigma methods are implemented in R&D environment, it might create an irreplaceable value for the company. Overall, together the statistical and process capability index analysis shows the direction of optimizing the wanted RF parameter so that the design can tolerate the variability and perform as it is supposed.

Design optimization was carried out by adjusting the biasing of the transistor along with adding places for capacitors and increasing the delay line length in the external input matching circuit of main branch. The biggest improvement was seen with nominal version in Figure 44 which is the most probable version of all. Though the peak power values were ensured to be increased, the verification of other parameters was limited for this thesis. However, the PA modules with new biasing performed well in the base station unit without problems and therefore, the goal is achieved. The made design change is easy and quick to implement bringing up the benefits in project scheduling. Also, the resources can be used for driving the final design forward. The time in hardware modifications could have been used for testing the modification in many modules which might postpone the project deadlines in the worst case. As the way how each corner sample version linearizes, feedback for algorithm development can be given.

The most time-consuming part of this thesis process was measuring a big population of PA modules and processing the measurement results. The significance of test automation clarified during the thesis process and gave ideas for further development for test automation. What

comes to data processing, the big data technologies may be exploited in production, R&D and project management as a joint of cooperation in analysis between all data. Big data means collecting, storing and analyzing huge masses of information by solutions guaranteed by information technology [14]. Since the PA module design process from the very first module version to the last accumulates huge amount of data, the data could be analyzed from the beginning to the end and located on a timeline, for example. Finding a suitable way for aligning the data may help the design process during the project and in further projects with similar products. Also, possible harmful factors in development and thus the project can be noticed with data analysis. One modern technology for automatic data processing is called robotic process automation. It is a partial solution for automatization of data processing based on artificial intelligence or routine workflow [15].

6 SUMMARY

As the number of mobile data users and equipment is constantly growing, the importance of spectral efficient communications will be emphasized. Higher data throughput requires wideband signals along with the linear modulation methods. Therefore, the RF PA needs to be able to amplify the transmitted signal as linearly as possible. The large volume production increases the variety of RF parameters in a PA module, which has an important role in multi standard base station. In this thesis, the PA module design is optimized to tolerate the productional variety in the most important RF parameters for PA: linearity, gain, efficiency and peak power. In order to understand the structure of inverted asymmetric Doherty PA and requirements of its operation, the theory is introduced first.

The method for scrutinizing the productional variability is measuring and hardware tuning of corner sample build. Its purpose is to illustrate artificially the realistic productional variability of the final stage of PA. Building a simulation model of the whole design is complicated and simulations will not provide precise image of the real performance of the PA, not forgetting the cooperation with the other parts of the base station.

Seven different corner sample version are measured, and the measurement data is analyzed. Measurement results are compared to the specifications of each RF parameter, which are defined particularly for this thesis. Measurement results are compared also to the nominal version which is the most probable version to come out of the production line. Statistical behavior of parameters is presented also. Process capability indices are calculated from the measurement data in order to observe how each parameter behave with relation to specification limits.

Direction of design optimization can be seen from electrical and functional measurement data along with statistical analysis of measurement data. Simple graphical presentation of measurement results helps to see the behavior of each parameter in each corner sample version. Measurement results and statistical analysis showed that peak power needs to be tuned higher in order to design tolerates better the realistic productional variability. Biasing of the transistor is changed, and the capacitors are added to the external input matching network along with increasing the length of delay line which altogether increases the peak power. Thus, design was optimized with the measurement and hardware tuning based design process and RF parameters tolerate the productional variety better.

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