
FACULTY OF INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING
DEGREE PROGRAMME IN ELECTRONICS AND COMMUNICATIONS ENGINEERING

# MASTER'S THESIS

# REGISTER-TRANSFER-LEVEL POWER PROFILING FOR SYSTEM-ON-CHIP POWER DISTRIBUTION NETWORK DESIGN AND SIGNOFF

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# ABSTRACT

**This thesis is a study of how register-transfer-level (RTL) power profiling can help the design and signoff of power distribution network in digital integrated circuits. RTL power profiling is a method which collects RTL power estimation results to a single power profile which then can be analysed in order to find interesting time windows for specifying power distribution network design and signoff.**

**The thesis starts with theory part. Complementary metal-oxide semiconductor (CMOS) inverter power dissipation is studied at first. Next, power distribution network structure and voltage drop problems are introduced. Voltage drop is demonstrated by using power distribution network impedance figures. Common on-chip power distribution network structure is introduced, and power distribution network design flow is outlined. Finally, decoupling capacitors function and impact on power distribution network impedance are thoroughly explained.**

**The practical part of the thesis contains RTL power profiling flow details and power profiling flow results for one simulation case in one design block. Also, some methods of improving RTL power estimation accuracy are discussed and calibration with extracted parasitic is then used to get new set of power profiling time windows. After the results are presented, overall RTL power estimation accuracy is analysed and resulted time windows are compared to reference gate-level time windows. RTL power profiling result analysis shows that resulted time windows match the theory and RTL power profiling seems to be a promising method for finding time windows for power distribution network design and signoff.**

**Key words: power estimation, switching activity, decoupling capacitor, power distribution network impedance.**

**Hämäläinen J. (2019) Rekisterisiirtotason tehoprofilointi järjestelmäpiirin tehonsiirtoverkon suunnittelussa ja verifioinnissa.** Oulun yliopisto, elektroniikan ja tietoliikennetekniikan tutkinto-ohjelma. Diplomityö, 50 s.

# TIIVISTELMÄ

**Tässä työssä tutkitaan, miten rekisterisiirtotason (RTL) tehoprofilointi voi auttaa digitaalisten integroitujen piirien tehonsiirtoverkon suunnittelussa ja verifioinnissa. RTL-tehoprofilointi on menetelmä, joka analysoi RTL-tehoestimoinnista saadusta tehokäyrästä hyödyllisiä aikaikkunoita tehonsiirtoverkon suunnitteluun ja verifiointiin.**

**Työ alkaa teoriaosuudella, jonka aluksi selitetään, miten CMOS-invertteri kuluttaa tehoa. Seuravaksi esitellään tehonsiirtoverkon rakenne ja pahimmat tehonsiirtoverkon jännitehäviön aiheuttajat. Jännitehäviötä havainnollistetaan myös piirikaavioiden ja impedanssikäyrien avustuksella. Lisäksi integroidun piirin tehonsiirtoverkon suunnitteluvuo ja yleisin rakenne on esitelty. Lopuksi teoriaosuus käsittelee yksityiskohtaisesti ohituskondensaattoreiden toiminnan ja vaikutuksen tehonsiirtoverkon kokonaisimpedanssiin.**

**Työn kokeellisessa osuudessa esitellään ensin tehoprofiloinnin vuo ja sen jälkeen vuon tulokset yhdelle esimerkkilohkolle yhdessä simulaatioajossa. Lisäksi tässä osiossa käsitellään RTL-tehoestimoinnin tarkkuutta ja tehdään RTL-tehoprofilointi loisimpedansseilla kalibroidulle RTL-mallille. Lopuksi RTL-tehoestimoinnin tuloksia ja saatuja RTL-tehoprofiloinnin aikaikkunoita analysoidaan ja verrataan porttitason mallin tuloksiin. RTL-tehoprofiloinnin tulosten analysointi osoittaa, että saatavat aikaikkunat vastaavat teoriaa ja että RTL-tehoprofilointi näyttää lupaavalta menetelmältä tehosiirtoverkon analysoinnin ja verifioinnin aikaikkunoiden löytämiseen.**

**Avainsanat: tehoestimointi, kytkentäaktiivisuus, ohituskondensaattori, tehonsiirtoverkon impedanssi.**

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# FOREWORD

The purpose of this thesis was to study register-transfer-level power profiling flow. Big part of the thesis covers theoretical background of power distribution network and is supposed to give a brief introduction to a very wide topic. Thesis is made at Nokia Networks during 2018.

I would like to thank my manager Juha Yrjänäinen for offering me this position and making this thesis possible. Also, I would like to thank my colleague and technical advisor Miikka Haataja. He was a priceless source for help and technical knowledge. Also, I want to thank the whole University of Oulu staff for all the help during my master's studies with extra mention to Professor Timo Rahkonen and Dr. Jukka Lahti for the help during thesis.

Oulu, December 28th, 2018

Joona Hämäläinen

# LIST OF ABBREVIATIONS AND SYMBOLS

| | |
|---|---|
| ASIC | Application-Specific Integrated Circuit |
| CMOS | Complementary Metal-Oxide-Semiconductor |
| ESL | Effective Series Inductance |
| ESR | Effective Series Resistance |
| FET | Field-Effect Transistor |
| HP | High-Performance Transistor |
| IC | Integrated Circuit |
| LOP | Low-Operating Power Transistor |
| LSTP | Low Stand-by Power Transistor |
| LUT | Lookup Table |
| MOS | Metal-Oxide-Semiconductor |
| MOSFET | Metal-Oxide-Semiconductor Field-Effect Transistor |
| nMOS | N-type Metal-Oxide-Semiconductor |
| PCB | Printed Circuit Board |
| PDN | Power Distribution Network |
| PLL | Phase-Locked Loop |
| pMOS | P-type Metal-Oxide-Semiconductor |
| RTL | Register-Transfer-Level |
| VCD | Value Change Dumb |
| VRM | Voltage Regulator Module |
| WLM | Wire Load Model |

| | |
|---|---|
| $C$ | Capacitance |
| $\frac{di}{dt}$ | Current transient |
| $f$ | Clock frequency |
| $I$ | Current |
| $I(f)$ | Current spectrum |
| $I(t)$ | Time varying current |
| $L$ | Inductance |
| $L_g$ | Ground line parasitic inductance |
| $L_p$ | Power line parasitic inductance |
| $P_{dyn}$ | Dynamic power dissipation |
| $P_{leak}$ | Leakage power dissipation |
| $P_{short}$ | Short-circuit power dissipation |
| $P_{stat}$ | Static power dissipation |
| $P_{total}$ | Total power dissipation |
| $Q$ | Charge |
| $Q$ | Quality factor |
| $R$ | Resistance |
| $R_g$ | Ground line parasitic resistance |

| | |
|---|---|
| $R_p$ | Power line parasitic resistance |
| $V$ | Voltage |
| $\Delta V_L$ | Inductive voltage drop |
| $\Delta V_R$ | Resistive voltage drop |
| $V_{ripple}(f)$ | Maximum ripple spectrum in supply voltage |
| $V_{T_n}$ | nMOS transistor threshold voltage |
| $V_{T_p}$ | pMOS transistor threshold voltage |
| $V_T$ | Threshold voltage |
| $V_{dd}$ | Supply voltage |
| $V_{dd}^{load}$ | Supply voltage at load |
| $V_{in}$ | Input voltage |
| $V_{out}$ | Output voltage |
| $V_{ss}$ | Ground voltage |
| $V_{gnd}$ | Ground voltage |
| $V_{gnd}^{load}$ | Ground voltage at load |
| $Z$ | Impedance |
| $Z_{PDN}(f)$ | PDN impedance profile |
| $Z_{target}$ | Target impedance |
| | |
| $\alpha$ | Activity factor |
| $\beta$ | Transistor gain |
| $\omega$ | Angular frequency |
| $\omega_{res}$ | Resonant frequency |
| $\tau$ | Transistor delay |

# 1. INTRODUCTION

The design of a digital integrated circuit's power distribution network needs accurate power information. Accurate power information has traditionally not been available when a power distribution network has been characterised, so the power distribution network tends to be conservatively designed to ensure power integrity. A power distribution network could take up to 40% of a chip's metal resources and any late change to a power distribution network could lead to very costly signal rerouting. In addition to all that, power consumption has become the most important limiting factor in semiconductor industry and that in its turn has led to creation of innovative and advanced power features. These power features could include things like dynamically adjusted supply voltages and power gating. Also, lithography is shrinking and a huge number of transistors can be manufactured in a very small area and supply voltages and noise margins are dropping. These all cause increasing difficulties in power distribution network design. As if that were not bad enough, companies try to push time to market as short as possible. This has raised a need for accurate power information in early stages of chip design.

This thesis studies one methodology to get early and sufficiently accurate power information easily. That methodology is called register-transfer-level (RTL) power profiling. In RTL power profiling, the power information is collected in register-transfer-level with realistic test vectors. The thesis describes (1) what information RTL power profiling needs, (2) how it works, (3) what the results are it provides, (4) and how the results can be used in the power distribution network design.

Chapter 2 gives a short introduction to complementary metal-oxide semiconductor (CMOS) circuits and their power dissipation as background information for the whole chip's power consumption. Chapter 3 explains basics of a power distribution network and most important reasons for power distribution network voltage drop. It also briefly explains a multitude of other topics related to power distribution network structure and action. Chapter 4 describes how RTL power profiling flow works, what information it needs and what results it provides. Chapter 5 analyses RTL power profiling result's accuracy. Chapter 6 discusses the thesis and its topic. Finally, Chapter 7 summarises the contents of the thesis and the results gained therein.

# 2. CMOS CIRCUITS AND THEIR POWER DISSIPATION

Chapter 2 gives introduction to CMOS circuits and their power dissipation. Section 2.1 gives short introduction and brief history of MOS transistors and CMOS circuits. Section 2.2 describes the simplest CMOS circuit, the CMOS inverter and its operation. Finally, Section 2.3 explains CMOS circuits power dissipation methods.

## 2.1. Introduction to CMOS

Fundamental basics of metal-oxide-semiconductor (MOS) transistor's operation is the field-effect principle which occurs in publications already at the 1930s [1 p. 1]. At the time, material technology was insufficient for fabricating working devices [1 p. 1] [2 p. 1-4]. Usable MOS transistors could be manufactured in the 1960s, after advances in planar silicon and semiconductor material technology [1 p. 3] [2 p. 1-6]. Field-effect transistors are generally called FET and therefore MOS transistors are also called as MOSFET in some sources.

CMOS uses both p-type and n-type MOS transistors (pMOS, nMOS). The difference between pMOS and nMOS is that pMOS uses holes as majority carries, whereas nMOS uses electrons as majority carries. The mobility of holes is less than that of electrons (modern strained silicon methods can largely equalize the mobility difference [1 p. 144]). That makes pure pMOS circuits slower than pure nMOS circuits with equal chip area and CMOS circuits are more complex to manufacture than pure nMOS circuits. These reasons led to nMOS domination on early years of the MOS transistors. Demand for higher density and performance led nMOS manufacturing process complexity to rise at the CMOS manufacturing process level. CMOS circuits also consume less than one tenth of the power dissipated by pure nMOS equivalent circuit and CMOS circuits have better noise margins. These advantages in their turn led to a rise of the CMOS use in the mid-1980s. Use of the CMOS has only been rising after that and the CMOS integrated circuits (IC) take about 80% of total semiconductor revenue in 2016 and 14% of those ICs are analogue and 86% is digital. [1 p. vii-viii, 161-162] [2 p. 1-6]

## 2.2. CMOS inverter

The simplest CMOS circuit is a CMOS inverter which consists of an nMOS and pMOS transistors connected, as shown in Figure 1 [1 p.173-174]. Inverter input voltage ($V_{in}$) is connected to gates of both pMOS and nMOS transistors. Depending on $V_{in}$ and threshold voltage ($V_T$) of both n- and p-type transistors ($V_{T_n}, V_{T_p}$), current either runs or doesn't run through a transistor. $V_T$ is the limit when a transistor becomes highly conductive and a short circuit path is created between transistors drain and source [3 p. 14]. When only one of the transistors is conducting, CMOS is said to be in stable operating point. The stable operating point happens either when

$$V_{in} < V_{T_n}, \tag{1}$$

or

$$V_{in} > V_{dd} + V_{T_p}, \tag{2}$$

where $V_{dd}$ is supply voltage and $V_{T_n} > 0$ and $V_{T_p} < 0$. In equation (1) situation, nMOS is off and pMOS is on and output voltage ($V_{out}$) is in $V_{dd}$, while in equation (2), nMOS is on and pMOS is off and $V_{out}$ is in ground voltage ($V_{ss}$). Figure 2 explains $V_{out}$ dependency of $V_{in}$ and illustrates the limits of the previous equations. The symmetric shape in the Figure 2 is caused by a symmetrical inverter where amplifications and threshold voltages are equal for both sides of the inverter. It's important to understand that one of the transistors is always off at stable operating point and that means that there is no DC current going from supply to ground. The current only goes through both transistors during inverter $V_{out}$ state transitions. This absence of DC current makes CMOS circuits much less power hungry than pure nMOS circuits. Figure 2 also partly explains why CMOS has good noise margins. $V_{out}$ is very flat when $V_{in}$ is close to $V_{ss}$ and $V_{dd}$. In this flat region, any small change (noise) in $V_{in}$ doesn't have an effect on $V_{out}$. [1 p. 176, 186-187]

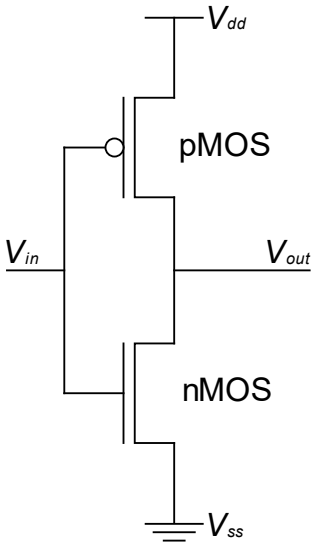


Figure 1. Circuit diagram of a CMOS inverter.

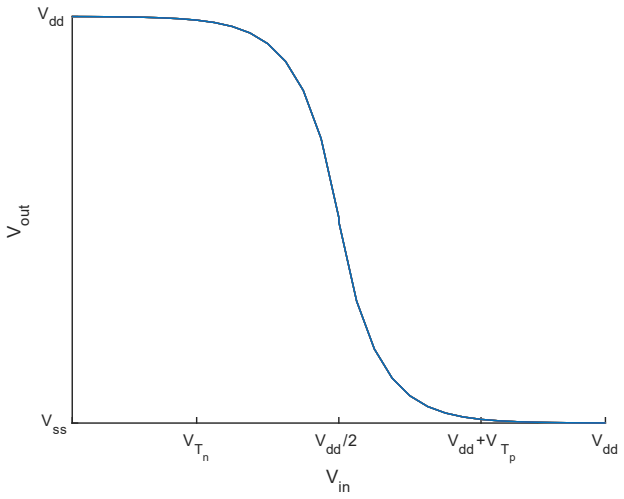


Figure 2. Symmetrical CMOS inverter transfer characteristics.

### 2.3. CMOS power dissipation

When the CMOS circuits are operating, they consume power. Some of the power is constantly consumed and some is only consumed when circuit output is changing a state. Total power dissipation $P_{total}$ can be divided in to components, so that

$$P_{total} = P_{dyn} + P_{stat} + P_{short} + P_{leak}, \quad (3)$$

where $P_{dyn}$ is dynamic dissipation, $P_{stat}$ is static dissipation, $P_{short}$ is short-circuit dissipation and $P_{leak}$ is leakage dissipation. $P_{dyn}$ and $P_{short}$ occur only when the circuit is changing its state and they're collectively known as switching power. $P_{stat}$ and $P_{leak}$ dissipate power constantly as the circuit is powered up. Figure 3 shows the power dissipation components in the CMOS inverter circuit [3 p. 12]. Figure 3 has one update from Figure 1 circuit, CMOS output total capacitance $C$. $C$ represents CMOS output load capacitance which consists of interconnection capacitance, driven transistors gate capacitances and parasitic capacitances in driving logic itself [1 p. 389]. [1 p. 384]

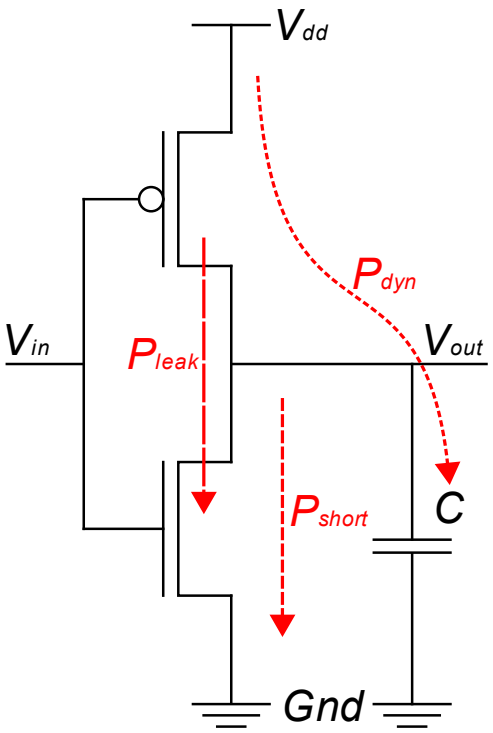


Figure 3. CMOS power dissipation components.

#### *2.3.1. Leakage power dissipation*

$P_{leak}$ represents subthreshold, gate and substrate non-zero leakage currents. These currents cause CMOS circuit to have a power leakage when power is on even if the circuit has no activity [3 p. 15]. As circuit power usage has been dropping though years, $P_{leak}$ has risen a more and more significant contributor in circuit's total power usage [3 p. 18, 31]. [1 p. 384-385]

Because of manufacturing process (lithography) progress, channel lengths inside a transistor are becoming so small that supply voltage must be limited to reduce the electric field inside the MOS transistors. From 0.8 µm to 120 nm CMOS technology node, the supply voltage has been lowered from 5 V to 1.2 V. Reducing supply voltage makes transistors slower. Threshold voltages have been reduced to compensate this slowness. But when threshold voltage is reduced, the leakage current is increased and noise margin is decreased. It is application-specific whether low threshold high-performance (HP, fast and high leakage) or high threshold low stand-by power (LSTP, slow and low leakage) transistors are better [2 p. 2-2]. [1 p. 385-386, 391-392] [3 p. 18]

### *2.3.2. Dynamic power dissipation*

$P_{dyn}$ represents the dynamic dissipation. $P_{dyn}$ happens when the CMOS charges and discharges the output node and all the capacitances related to that. Figure 3 displays output node's capacitance charging path. Every time the output state changes, the node is either charged from $V_{dd}$ or discharged to ground (*Gnd*). $P_{dyn}$ can be calculated by

$$P_{dyn} = C \cdot V_{dd}^2 \cdot \alpha \cdot f, \tag{4}$$

where $\alpha$ is activity factor and $f$ is switching frequency. $\alpha$ represents average gate switch activity in one clock period. $\alpha$ is application-specific and it can even be more than 1, because glitches and hazards can cause unnecessary transitions during a single clock period [1 p. 418]. [1 p. 384]

$P_{dyn}$ used to be the largest cause of the power consumption down to 120 nm technology. At smaller technologies, $P_{leak}$ started to rise to a significant role in the CMOS power consumption. That raised a demand to balance total power usage between $P_{dyn}$ and $P_{leak}$. Low-operating power (LOP) transistors are those balanced transistors and their properties are between HP and LSTP. Balancing is done as a compromise by adjusting $P_{leak}$ to be roughly equal to $P_{dyn}$ or in equation form:

$$P_{leak} = I_{off} \cdot V_{dd} = C \cdot V_{dd}^2 \cdot \alpha \cdot f = P_{dyn}, \tag{5}$$

where $I_{off}$ describes leakage currents. This equation leads to minimum power for required performance. [1 p. 391-392]

It's important to notice that $P_{leak}$ is directly proportional to $V_{dd}$, while $P_{dyn}$ is proportional to square of $V_{dd}$. Total power dissipation can be reduced in many ways, but the large power savings can be achieved by reducing the supply voltage. Other actions to reduce the power dissipation could be: reducing leakage currents, parasitic capacitances or switching activity. [1 p. 424-425]

### *2.3.3. Static power dissipation*

$P_{stat}$ represents power dissipation of temporary or continuous static DC currents [1 p. 384]. Sometimes, pseudo-nMOS (e.g. wired OR) solution can be beneficial. In pseudo-nMOS circuit, gate of pull-up pMOS is permanently connected to ground. That causes pMOS to conduct constantly. And when the nMOS is also conducting, that causes current to flow from $V_{dd}$ to $Gnd$ because both transistors are conducting at the same time. $P_{stat}$ represents this current flowing through transistors. $P_{stat}$ is not present in pure CMOS circuits. That is the reason why $P_{stat}$ is not present in Figure 3. A pure CMOS circuit is more power efficient than pseudo-nMOS circuits. [1 p. 394-395]

### *2.3.4. Short-circuit power dissipation*

$P_{short}$ represents power dissipation by current flowing though both transistors when the CMOS output is changing a state. $P_{short}$ is present when $V_{in}$ is between $V_{T_n}$ and $V_{dd} + V_{T_p}$ during state change in Figure 2. $P_{short}$ is similar to $P_{stat}$ but in this case, current is only temporary when both transistors are changing a state and conducting at the same time. $P_{short}$ is also present in CMOS circuits. The amount of $P_{short}$ can be calculated by

$$P_{short} = \frac{\beta}{12} \cdot (V_{dd} - 2V_T)^3 \cdot \tau \cdot f, \tag{6}$$

where $\beta$ is transistor gain, $\tau$ is transistor delay and $f$ is clock frequency. Transistor delay includes both rise and fall delays and they are assumed to be equal in equation (6). Also $\beta$ and $V_T$ are assumed to be equal for nMOS and pMOS in equation (6). More generally, $P_{short}$ can be minimised by minimising transistor rise and fall times and adjusting transistor rise and fall time to be equal. In most modern CMOS circuits, rise and fall times are so small that $P_{short}$ is negligible. $P_{short}$ could be a significant factor if transistor's input fall or rise time is much larger than output rise and fall time allowing output to be between 0 and 1 state longer. This is possible, e.g. if consecutive similar transistors in the circuit are driving large capacitance nets and low capacitance nets. [1 p. 384, 393-394] [3 p.14, 30-31]

# 3. POWER DISTRIBUTION NETWORK

Chapter 3 explains basics of structure, action and voltage drop in power of PDN. Section 3.1 contains a brief introduction to PDN structure and describes an early design problem for PDN. Section 3.2 introduces PDN voltage drop and noise margin. Section 3.3 explains what kinds of problems PDN noise could cause. Section 3.4 introduces decoupling capacitors and their impedance characteristics and importance to PDN. Section 3.5 describes difficulties with defining PDN target impedance. Section 3.6 explains PDN's impedance profile. Section 3.7 shows how decoupling capacitors affect PDN impedance profile. Section 3.8 gives some basics about on-chip PDN, flip-chip package and die-package interface. Section 3.9 explains PDN design flow and design steps. Finally, Section 3.10 shows some simple methods of how to calculate needed decoupling capacitance.

## 3.1. Introduction

Supplying reliable power to a high performance integrated circuit (IC) has become a challenge. The entire power supplying system is referred to as the power distribution system. The power distribution system consists of a switching voltage regulator module (VRM) and the power distribution network (PDN). The VRM converts DC voltage to an IC operating voltage $V_{dd}$. The VRM serves as a power source, effectively decoupling the IC's PDN from the system level power supply. [4 p. 87-88]

A power distribution network is a collection of everything at conductive path between power source (VRM) and power load (transistor). PDN consists of interconnects, vias and possible planes in printed circuit board (PCB), package and chip. Also, all the different kinds of decoupling capacitors, possible solder balls and wire bonds and returning current (ground) paths are part of the PDN. Figure 4 shows a simplified PDN structure with some decoupling capacitors. The main thing to notice from Figure 4 is that the PDN has a hierarchical structure and that decoupling capacitors have a similar hierarchical structure as the PDN. The hierarchical structure of the PDN allows impedance characterisation for each structural step at a time. On-chip PDN design and impedance characterisation are most difficult task in PDN design. [4 p. 87-89] [5 p. 615]

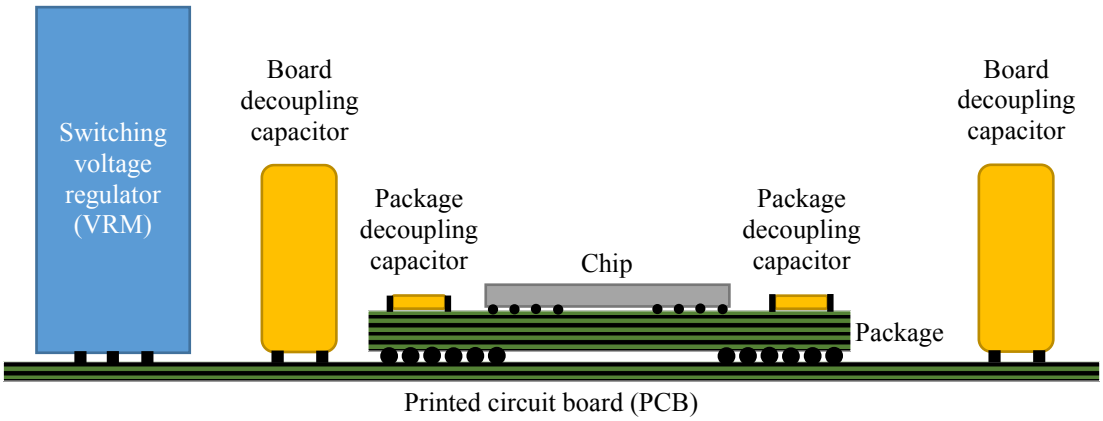


Figure 4. Simplified cross-sectional view of PDN with decoupling capacitors.

A significant fraction of the on-chip metal and area resources is committed to the PDN power integrity. The global on-chip PDN is typically characterised at early stages of the design process, when little is known about the power demands in different locations in IC. Allocating more metal resources for the PDN at the later stages of the design to improve power integrity could mean complete redesign of the surrounding signal lines, which is very expensive and time consuming. For all these reasons, PDN tends to be conservatively designed. On the other hand, overengineered and too hefty PDNs can be costly for modern interconnect limited and complex ICs as well. [4 p. 14-15] [6 p. 276]

### 3.2. Voltage drop in power distribution network

Two main issues that cause voltage drop in the PDN are called: resistive voltage drop or IR-drop and inductive voltage drop or Ldi/dt drop. [7 p. 157]. Figure 5 has a simple PDN circuit model to help visualize how IR-drop and Ldi/dt drop cause voltage drop in the PDN. In Figure 5, the circuit consists of a power supply (VRM), a power load (transistor) and interconnections between the supply and the load. The power supply is assumed to be an ideal voltage source providing a supply voltage $V_{dd}$ and a ground voltage $V_{gnd}$. The power load is modelled as a time varying current source $I(t)$, because transistor's power consumption is not constant. The important part of Figure 5 is that interconnects between the supply and the load are not ideal. Both the power and the ground net have parasitic resistances $R_p$ and $R_g$ and parasitic inductances $L_p$ and $L_g$. Every wire, net or interconnection has parasitic resistance and inductance. [4 p. 10-11]

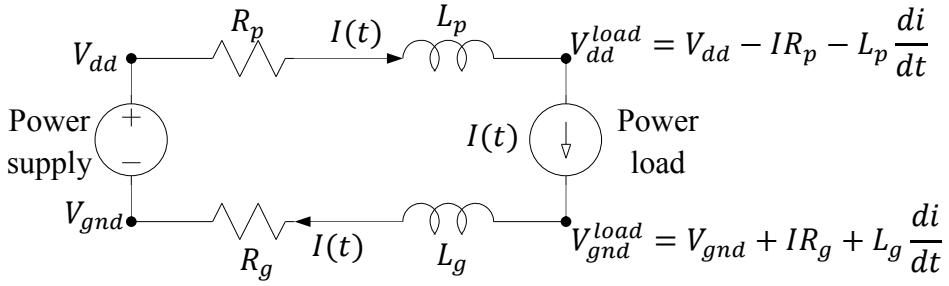


Figure 5. Simplified PDN circuit model without decoupling capacitors.

Parasitic resistance causes resistive voltage drop $\Delta V_R$ to interconnects when load draws current $I(t)$. The resistive voltage drop

$$\Delta V_R = IR \tag{7}$$

is directly proportional to current $I$ flowing through interconnection and interconnection parasitic resistance $R$. [4 p. 10-11]

The parasitic inductance causes inductive voltage drop $\Delta V_L$ to interconnects when load current $I(t)$ has change in level. Inductive voltage drop

$$\Delta V_L = L\frac{di}{dt} \tag{8}$$

is directly proportional to current transients $\frac{di}{dt}$ flowing through interconnection and interconnection parasitic inductance $L$. [4 p. 10-11]

Voltage at load differs from nominal voltage at power supply. Supply voltage at load is

$$V_{dd}^{load} = V_{dd} - IR_p - L_p\frac{di}{dt} \tag{9}$$

and ground voltage at load is

$$V_{gnd}^{load} = V_{gnd} + IR_g + L_g\frac{di}{dt}. \tag{10}$$

This change from nominal voltages is referred to as PDN noise or ripple. Supply voltage in load is different than in power supply. Even if the power supply sees a stable voltage, that doesn't mean that supply voltage in the load is within a specification [5 p. 618]. Load circuit operates correctly only when the voltage levels are maintained within a certain range near nominal voltages. This voltage range is called as noise margin. The main objective of PDN is to supply sufficient current to each transistor in IC, while similarly ensuring that the voltage level stays within a noise margin. [4 p. 10-11]

Reduced supply voltages have also lead to reduced noise margins, as shown in Figure 6. When the total voltage range is reduced, also the noise margin is reduced: Lower supply voltage has less room for voltage fluctuation before circuit performance is compromised. [4 p. 12-13]

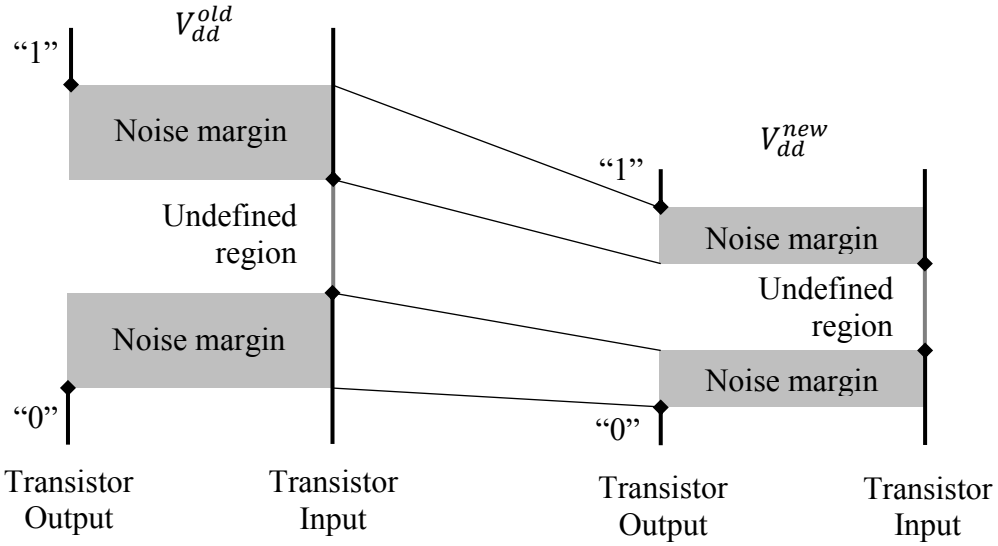


Figure 6. Reduction in noise margin with technology scaling.

Continuous progress in lithography creates significant challenges for PDN. IC densities and transistor count are rising as transistors are becoming smaller and smaller. At the same time, dropping IC supply voltage causes ICs to have higher current for the same power usage. This all leads to increased current densities and total currents. ICs are also using higher and higher clock speeds. Higher clock speeds lead to fasters transitions in transistors which shows as steeper (faster) current transients [8 p. 53]. [4 p. 11-13]

All this has led to tightening requirements for PDN. According equations from (7) to (10), PDN parasitic resistance and inductance must be as small as possible to keep voltage drops within noise margins. Usually, PDN resistance and inductance are combined to PDN impedance $Z$ and PDN impedance is described as impedance profile as function of frequency $Z_{PDN}(f)$. Maximum PDN impedance as a function of frequency is limited by

$$Z_{PDN}(f) < \frac{V_{ripple}(f)}{I(f)}, \tag{11}$$

where $V_{ripple}(f)$ is maximum ripple spectrum in supply voltage or noise margin and $I(f)$ is current spectrum [5 p. 618-619]. As equation (11) shows, reducing noise margins and increasing currents cause significant pressures to push PDN impedance as low as possible. [4 p. 11-15]

### 3.3. Effects of noise in power distribution network

Propagation delay of on-chip signals depends on the supply voltage levels during transistor transitions. CMOS transistor output current is reduced when the CMOS supply to ground voltage difference is reduced. Signal delay is also increased because lower current takes longer to charge output signal net. Conversely, a higher supply to ground voltage difference will shorten the propagation delay. Therefore, PDN noise cause propagation delay uncertainty in clock and data signals. Propagation delay uncertainties cause limitations to the circuit's maximum frequency. So, PDN noise could limit circuits maximum operating frequency [9 p. 141-142]. [4 p. 17]

The supply and the ground networks also serve as a voltage reference for the on-chip signals in digital logic. If a transistor outputs a low voltage state (0), the output of the transistor is connected to the ground network. Alternatively, the output is connected to the supply network to transfer the high voltage state (1). The receiver compares received voltage to the receiver's local reference supply and ground voltages. Signal sender and receiver can have a significant difference in voltage levels. PDN noise between signal and receiver's reference voltages reduces noise margin or could even cause metastability or false state identification at the receiver. [4 p. 20]

Supply voltage drops aren't the only problem. Supply voltage overshoot is also a problem. As mentioned in Section 2.3.1 supply voltages have been lowered in a modern IC's in order to reduce the electric field inside transistors. Overshoot and voltage variations in both power and ground lines could increase the voltages inside transistor over safe limits. Overshoots must be limited to avoid transistor reliability degradation. [4 p. 20]

PDN noise can also disturb other circuit elements like phase-locked loop (PLL) operations. PLL is often used to generate on-chip clock signals by multiplying the system clock signal. Power supply level variations affect the phase of the PLL. Disturbances of shorter than PLL feedback response time result in deviation of the on-chip clock phase from ideal timing. These deviations in phase are referred to as clock jitter. High frequency, comparable or shorter than clock period PDN noise causes cycle-to-cycle clock jitter. Similarly, as previously, clock jitter could limit the maximum operating frequency. Prolonged power supply variations can also cause systematic variations in clock phase. The clock phase can begin to roam and the phase difference could rise between system and on-chip clock before PLL feedback adjust becomes effective. This kind of difference would cause significant issues in clock domain synchronization. PLL feedback response time could also be highly dependent on power supply voltage. [4 p. 17-19] [10 p. 73-76]

## 3.4. Decoupling capacitors

Decoupling capacitors are used to reduce the impedance of PDN and to provide charge to the fast switching circuit, smoothing the variable currents. Both lower the PDN noise. As decoupling capacitors lower noise in PDN, they also lower electromagnetic interference noise radiated by the PDN. Decoupling capacitors are shunting capacitors which terminate the high frequency current loop by permitting the high frequency current to bypass the inductive interconnects. The high frequency impedance of PDN as seen from load is thereby reduced. In other words, the capacitor decouples the high impedance paths of PDN from the load at high frequency. That is the reason why these capacitors are called as decoupling capacitors. [4 p. 16, 126, 136]

### *3.4.1. Decoupling capacitor's impedance*

An ideal decoupling capacitor is effective over the entire frequency range, but a practical decoupling capacitor is effective only in a certain frequency range. This is caused by parasitic properties of practical capacitor, as Figure 7 shows. A practical capacitor also has effective series resistance (ESR) and effective series inductance (ESL) in addition to capacitance. ESR and ESL have a huge effect on decoupling capacitor's impedance profile [11 p. 216]. [4 p. 129-130]

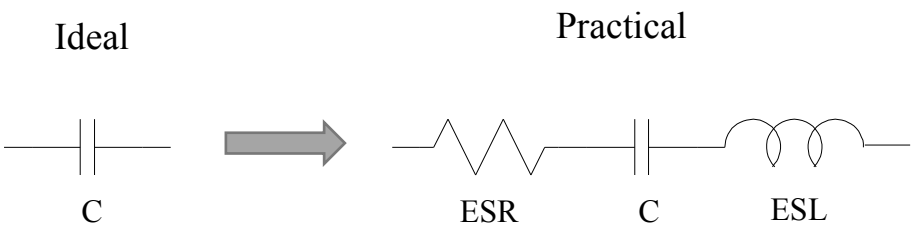


Figure 7. Capacitors ideal and simplified practical circuit models.

Ideal decoupling capacitors impedance ($Z_C$) is determined by

$$Z_C = \frac{1}{j\omega C}, \tag{12}$$

where $\omega$ is angular frequency and $C$ is capacitance. As equation (12) shows, capacitor's impedance decreases as frequency increases. An ideal capacitor's impedance profile is plotted in Figure 8. As Figure 8 shows, ideal capacitor's impedance decreases linearly -20 dB/decade on a log-log plot. [4 p. 130-131]

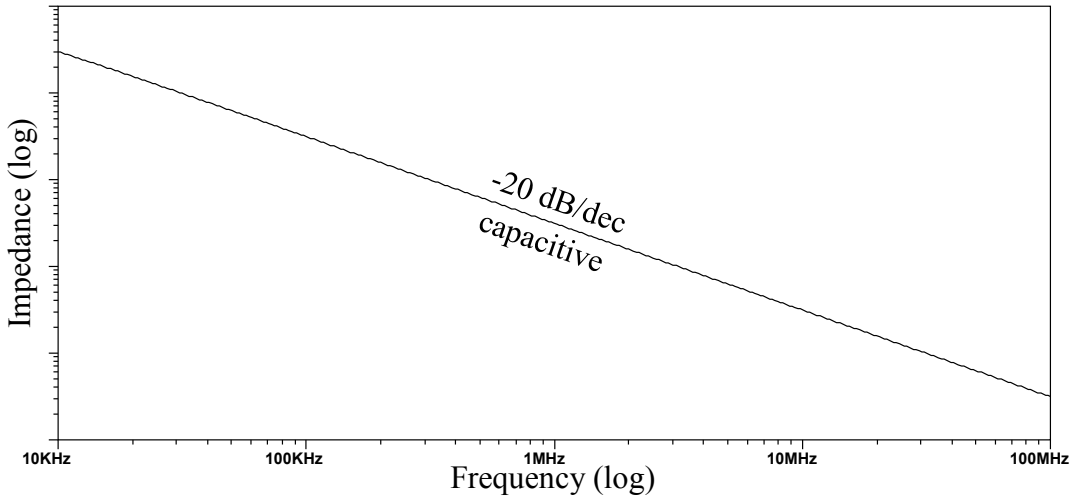


Figure 8. Ideal capacitor's impedance as a function of frequency.

In a practical decoupling capacitor, ESR and ESL have also an effect on impedance profile. Inductor impedance $Z_L$ is determined by

$$Z_L = j\omega L, \tag{13}$$

where $\omega$ is angular frequency and $L$ is inductance. In contrast to a capacitor, inductor impedance increases as frequency increases. As frequency increases and capacitor's impedance decreases, inductor impedance is rising. At some point, capacitor and inductor impedances match and after that point inductor impedance is dominant. The point where capacitor's and inductor's impedances match is called as resonant frequency $\omega_{res}$ and it can be calculated by

$$\omega_{res} = \frac{1}{\sqrt{LC}}. \tag{14}$$

Impedance minimum is in resonant frequency because capacitor and inductor voltage's phases are 180 degrees apart (value is oppositely signed) so they cancel each other out. Impedance minimum is then determined by ESR value [11 p. 213]. Resistor impedance is not affected by frequency. Figure 9 shows this graphically. Impedance is decreasing -20 dB/decade until the impedance reaches resonant frequency ($\omega_{res}$) and impedance starts to rise 20 dB/decade because inductance starts to dominate.

Impedance minimum is reached at resonant frequency and value is limited by ESR. [4 p. 130-131]

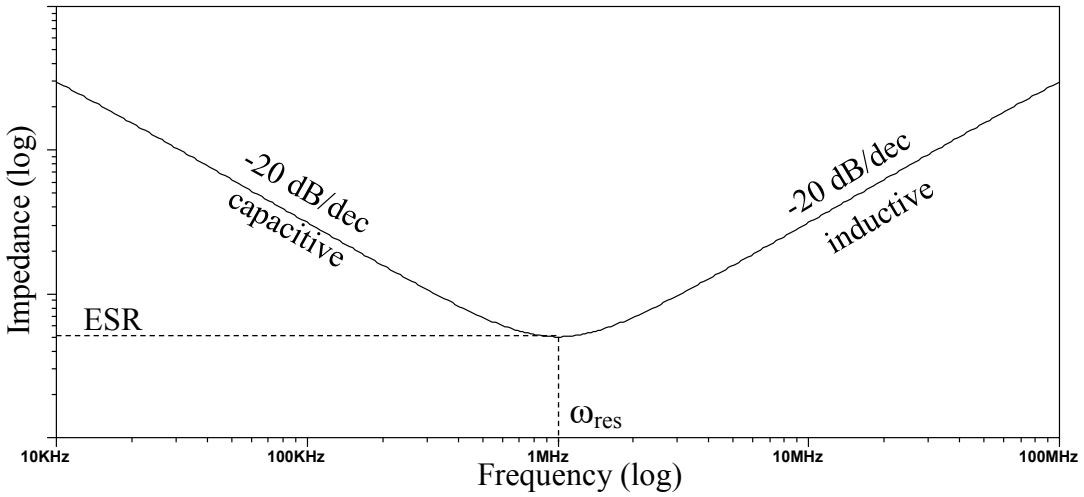


Figure 9. Practical capacitor's impedance as a function of frequency.

The impedance of decoupling capacitors depends on the values of all the components: capacitor's capacitance, ESR parasitic resistance and ESL parasitic inductance. Parasitic inductance for the same capacitor type is close to fixed for different capacitance capacitors. This means that the inductive part of the impedance curve stays almost unchanged when a similar capacitor with different capacitance is used. Capacitor selection mainly affects the capacitive part of the impedance curve. Figure 10 shows how doubling a capacitor's capacitance affects the capacitor impedance. Black line in Figure 10 shows how the capacitive part of the impedance is halved but the inductive part stays the same. [4 p. 131]

One way to move the inductive part of the impedance curve down is to connect decoupling capacitors in parallel. Identical decoupling capacitors reduces impedance by a factor of two for every doubled parallel of decoupling capacitors. It's important to notice that each additional capacitor has less impact on impedance [4 p. 137]. Figure 10 shows how doubling identical capacitors halves the impedance. Impedance drops also in the inductive part of the curve, which makes this better than just increasing capacitance and the resonant frequency stays the same in parallel configuration. [4 p. 131]

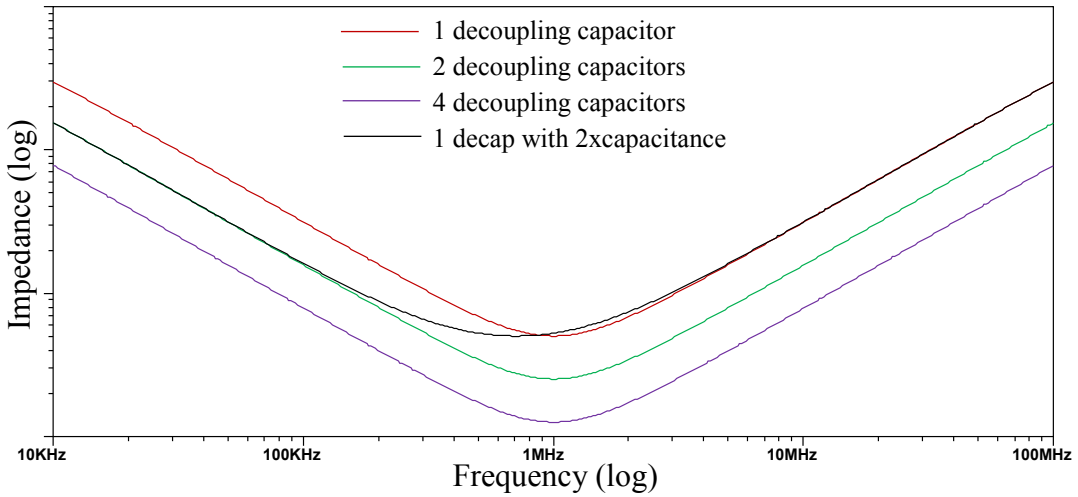


Figure 10. Parallel decoupling capacitors impedance as a function of frequency.

Typically, several parallel decoupling capacitors with different magnitudes are used to maintain low impedance over a wider frequency range. Figure 11 shows how a parallel identical capacitor with different capacitance widens low impedance area. Different capacitance capacitors also get lower impedance benefit at the inductive part of the impedance curve. If the impedance should be lowered at higher frequencies, then a capacitor's parasitic inductance should be as low as possible. But connecting different capacitance capacitors in parallel can create a new problem, antiresonance. Antiresonance is caused by LC-circuit which is created when a lower resonant frequency capacitor has become inductive and that inductance causes a resonant spike with a higher frequency capacitor which is still capacitive. Magnitude of the resonant spike is determined by capacitor's parasitic properties. A high resonant peak is caused by high quality factor $Q$. $Q$ can be roughly calculated by

$$Q = \frac{L}{R}, \tag{15}$$

where $L$ and $R$ represent capacitor's parasitic properties. A high Q leads to a high resonance spike, so the capacitor should have as low ESL as possible and high ESR only if necessary. Antiresonance could also be dampened with adding capacitors in antiresonance frequency. Additional capacitors create new notch in antiresonance frequency. Figure 12 shows an example antiresonance curve in red. Antiresonance curve has very sharp peaks. Peaks can be softened by adding additional ESR. Additional ESR softens both, high and low peaks. Peaks can be also softened by choosing capacitor with lower ESL value and higher capacitance in order to keep resonance frequency unchanged. Lower ESL valued capacitor softens peaks similarly as high ESR, but it also lowers impedance in all frequencies. Lower ESL and higher ESR have same effect on impedance curves as equation (15) implies. Antiresonance can break PDN impedance target and can cause an excessive voltage drop. [4 p. 137-139] [12 p. 284, 289-290]

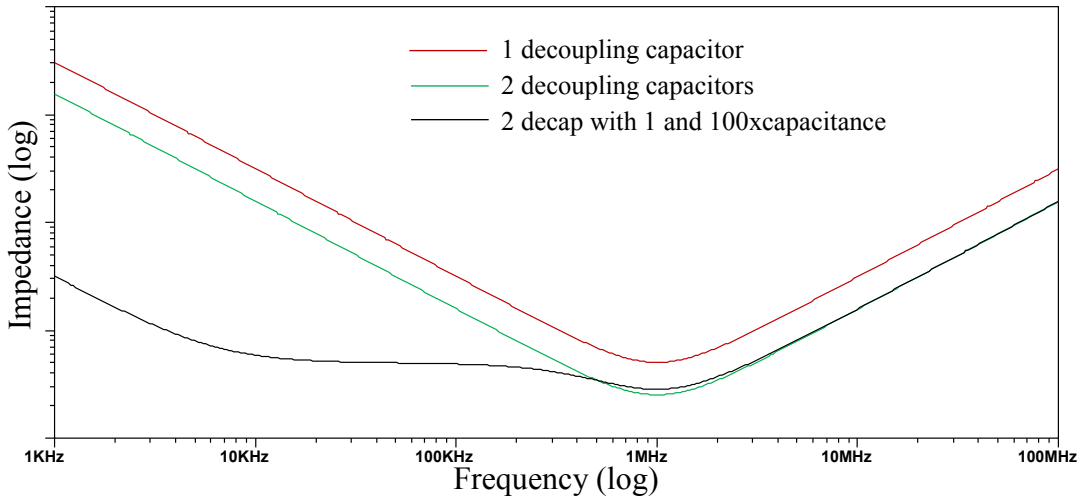


Figure 11. Parallel decoupling capacitors with different capacitance.

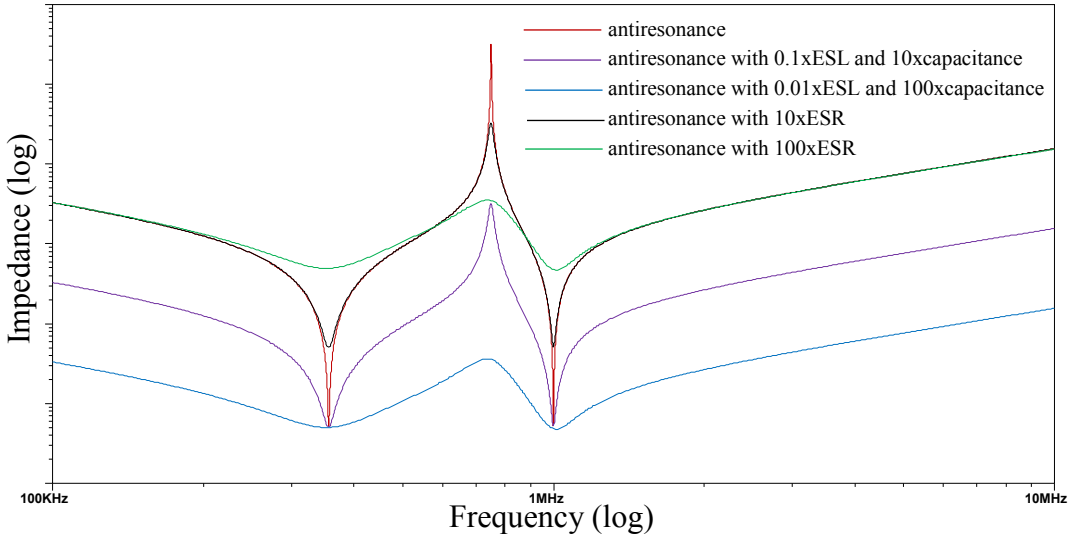


Figure 12. Parallel decoupling capacitors antiresonance with varied parasitic values.

### *3.4.2. Decoupling capacitor as a reservoir of charge*

An ideal decoupling capacitor should provide fast and high capacity energy storage, in addition to impedance reduction. It's expensive to satisfy both these requirements. Typically, in most practical applications, these requirements are contradictory. The physical realisation of a large capacitance requires the use of a discrete capacitor with a large capacity and large form factor. The large form factor of the capacitor has two drawbacks, however. The parasitic series inductance of a physically large capacitor is high due to an increased area of current loop within a large capacitor. In addition, technology limits placing physically large capacitors close to the load (on a chip). An increased distance increases inductance of the current path between load and capacitor. A trade-off must therefore be made between high capacity and low parasitic impedance of a decoupling capacitor. [4 p. 140-142]

Few tens of picoseconds gate switching times are common in modern ICs, creating fast and high transient currents in the PDN. Only decoupling capacitors with low ESL and ESR can effectively maintain low impedance at high frequencies. The lowest ESL and ESR can be achieved when decoupling capacitors are placed on-chip, as close to the load as possible. Placing large decoupling capacitors on-chip, requires many times more chip area than a typical circuit itself. A large on-chip decoupling capacitor is therefore typically built as a cluster of parallel connected small decoupling capacitors. [4 p. 142]

An efficient solution to this problem is to place multiple stages of decoupling capacitors, getting progressively smaller and closer to the load. Hierarchically placed decoupling capacitors produce a low impedance and high frequency power distribution system in a cost-effective way. This explains the different decoupling capacitor stages at Figure 4. The decoupling capacitors are placed hierarchically to the board, package and on-chip. Arranging the decoupling capacitors in several different stages eliminates the need to satisfy both high capacitance and low impedance requirements in the same stage. Power supply (VRM) timing constrains are relaxed because faster and lower impedance decoupling capacitors provide charge to fast current transients. [4 p. 142-143]

### 3.5. Target impedance of power distribution network

Power distribution network's impedance is measured directly at the load terminals. Impedance of a PDN should be maintained below upper bound, target impedance $Z_{target}$ from DC to the maximum operating frequency of the network. It's important to notice that the PDN's maximum operating frequency is determined by the switching times of transistors and on-chip signal transients rather than circuit clock frequency. Typically, the quickest switching times are an order of magnitude smaller than the clock period. That makes PDN maximum operating frequency significantly higher than the clock frequency. [4 p. 133]

Equation (11) provided a simple equation for target impedance calculation. But in real life, establishing the target impedance is hard. As equation (11) shows, the maximum allowed impedance depends on current's amplitude at that frequency. Unfortunately, a PDN designer has very little control over or accurate information about current profile and bandwidth. Usually, only some information about peak current is provided and that is used to estimate high frequency maximum transient current. Without accurate information about the worst-case current spectrum, conservative design must assume worst-case current that could happen in any frequency in band. This kind of flat worst-case $Z_{target}$ is present in the following impedance figures. Usually, problems with impedance happen in the high part of the bandwidth as the following section shows. [5 p. 621-625]

### 3.6. Power distribution network impedance

One of the power distribution network design objective is to ensure impedance characteristics at the operating frequency range. It's then important to understand how

the PDN circuit elements affect PDN's output impedance. In Figure 5, PDN consists of resistors and inductors. The magnitude of impedance of this network is

$$|Z_{tot}(\omega)| = |R_{tot} + j\omega L_{tot}|, \tag{16}$$

where the total resistance $R_{tot}$ and total inductance $L_{tot}$ are:

$$R_{tot} = R_p + R_g \tag{17}$$
$$L_{tot} = L_p + L_g. \tag{18}$$

Figure 5 circuit's impedance profile is plotted in Figure 13 with some component values. The impedance profile has some similarities with those in Section 3.4.1. Total resistance limits impedance's lowest value, and inductor's total impedance rises with frequency and becomes dominant at a certain frequency. In Figure 13, impedance stays below the target impedance only to 130 kHz. Impedance should stay below the target also in higher frequencies. Opportunities for reducing inductance of the whole power distribution network structure are very limited. [4 p. 93-94]

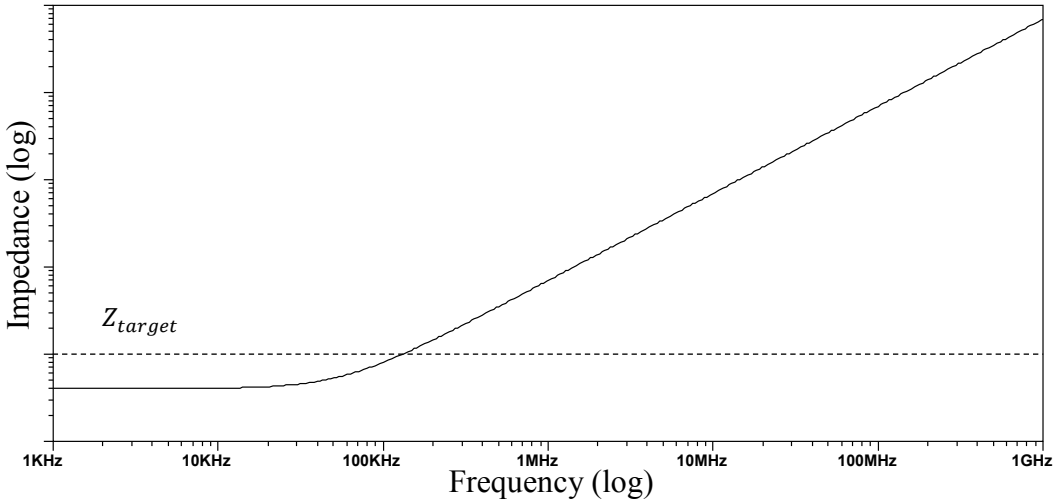


Figure 13. PDN impedance profile without decoupling capacitors.

### 3.7. Power distribution network with decoupling capacitors

The high frequency impedance is effectively reduced by placing decoupling capacitors across the power and ground conductors. These decoupling capacitors provide a new route for high frequency currents which bypasses highly inductive board and package interconnects, lowering high frequency impedance. Figure 14 shows a PDN with one decoupling capacitor and Figure 15 shows an impedance profile for that same PDN. Parasitic components in Figure 14 are divided from Figure 5 components as:

$$R_P = R_1^p + R_2^p \quad (19)$$
$$R_g = R_1^g + R_2^g \quad (20)$$
$$L_p = L_1^p + L_2^p \quad (21)$$
$$L_g = L_1^g + L_2^g \quad (22)$$

and impedance for Figure 14 circuit's load is calculated as

$$Z(\omega) = R_2 + j\omega L_2 + (R_1 + j\omega L_1)||(R^C + j(\omega L^C - \frac{1}{\omega C})), \quad (23)$$

where

$$R_1 = R_1^p + R_1^g \quad (24)$$
$$R_2 = R_2^p + R_2^g \quad (25)$$
$$L_1 = L_1^p + L_1^g \quad (26)$$
$$L_2 = L_2^p + L_2^g. \quad (27)$$

The idea behind equations and decoupling capacitor is shortly explained as follows: The decoupling capacitor divides the connector's parasitics to subscripts 1 (VRM side) and 2 (load side) in equations (19) - (22) and those in their turn form new parasitics in equations (24) to (27). Then, equation (23) explains how the capacitor creates a current path for subscript 2 circuit. The decoupling capacitor decouples subscript 1 circuit for high frequency currents, in a way that $L_1$ and $R_1$ don't affect high frequency impedance. Figure 15 clarify the situation further. Decoupling capacitors provide a lower impedance path after the decoupling capacitor's dashed impedance line cuts the actual line, lowering impedance on high frequencies, and a new impedance line is shifted as $L_1$ and $R_1$ are eliminated from the circuit. Figure 15 shows clearly how $L_1$ elimination shifts the impedance profile but impedance's lowest value shifting from $R_1$ elimination isn't clearly shown at these component values. The impedance profile is of course highly depending on selected components values. The decoupling capacitor increases the highest useful frequency of this PDN from 130 kHz to 1.3 MHz. [4 p. 95-99]

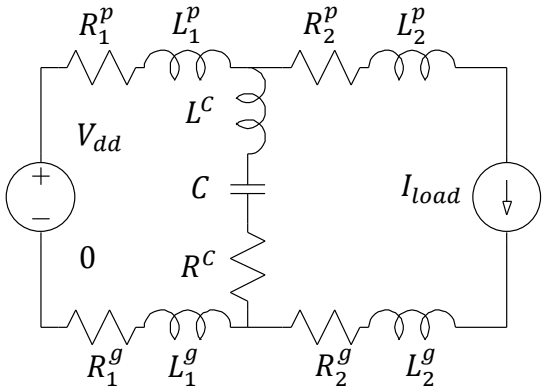


Figure 14. PDN circuit model with one decoupling capacitor.

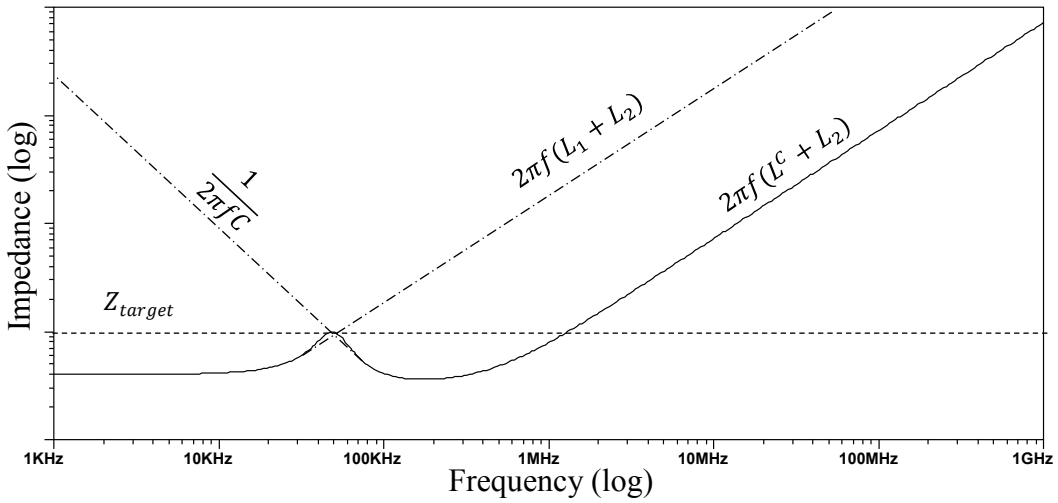


Figure 15. PDN impedance profile with one decoupling capacitor.

As Section 3.4.2 explained, a single tier decoupling is not practical and a better result can be achieved by placing decoupling capacitors in multiple different hierarchies across the power distribution network. Figure 16 shows the circuit model with hierarchical decoupling capacitors, hierarchies and parasitics divided in those hierarchies. The circuit's impedance profile is in Figure 17, which shows how hierarchical and overlapping placement of decoupling capacitors widens power distribution network's useful range frequency region significantly [4 p. 106]. Dashed lines in Figure 17 represent approximation of different hierarchy decoupling capacitor's impedance. The power distribution network's highest useful frequency is increased from original 130 kHz to 1.0 GHz. Hierarchical decoupling capacitors have massive impact on power distribution network impedance on high frequency, which can be seen by comparing Figure 13 impedance profile without decoupling capacitors and Figure 17 impedance profile with hierarchical decoupling capacitors.

Figure 17 has significantly high "bumps" between decoupling capacitors impedance minimums. On those frequencies, current goes also through the previous decoupling capacitor. The lower frequency decoupling capacitor is inductive at those frequencies making an RLC-resonator circuit with power distribution network and higher frequency decoupling capacitor. The theory behind resonance is similar to anti-resonance mentioned in the end the Section 3.4.1. Maintaining a low impedance profile in a power distribution network, leads to minimizing the quality factor in all resonant modes at a power distribution network. A power distribution network's resonances quality factors are commonly relatively low valued. The decoupling capacitor's ESR is an important damping factor in resonance control. [4 p. 108, 124]

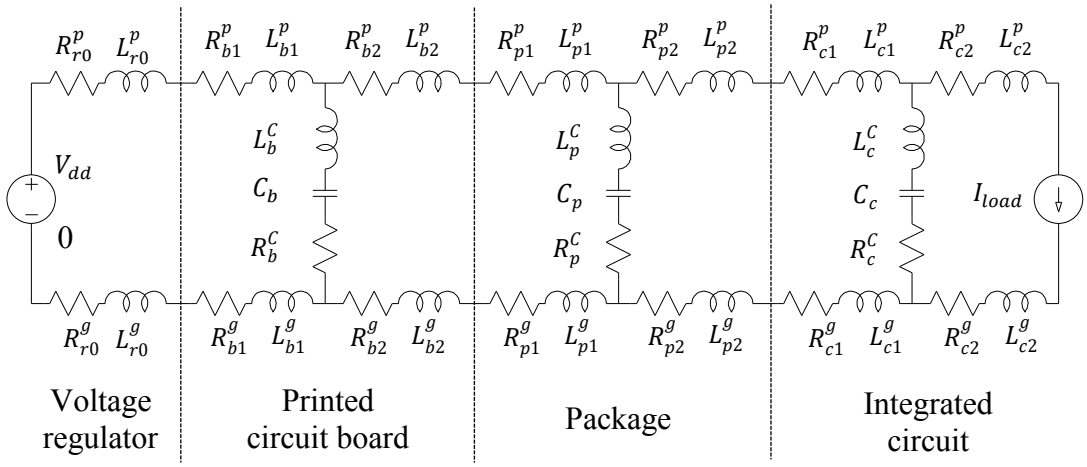


Figure 16. PDN circuit model with hierarchical decoupling capacitors.

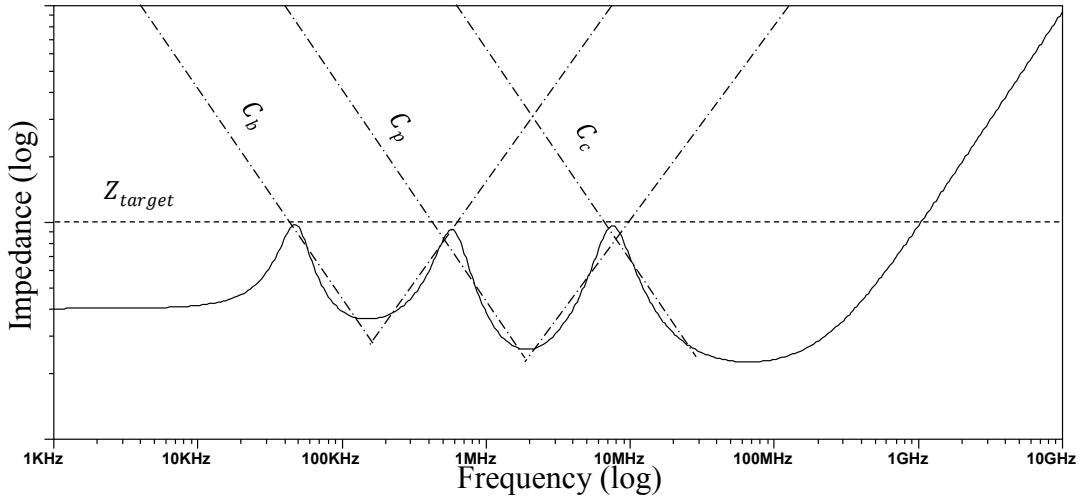


Figure 17. PDN impedance profile with hierarchical decoupling capacitors.

Figure 18 shows graphically how hierarchical decoupling capacitors decouple parts of the power distribution network as current frequency increases. When parts of power distribution network are decoupled, the current loop is shrinking, reducing parasitics in the loop. Especially, reduced inductance in the high frequency loop, reduces a network's impedance at load in high frequencies. [4 p. 106-108]

A PDN with decoupling capacitors "should therefore be carefully designed to provide a low impedance, resonant-free power distribution network over the entire range of operating frequencies, while delivering sufficient charge to the switching circuits to maintain the local power supply voltages within target noise margins." [4 p. 16]

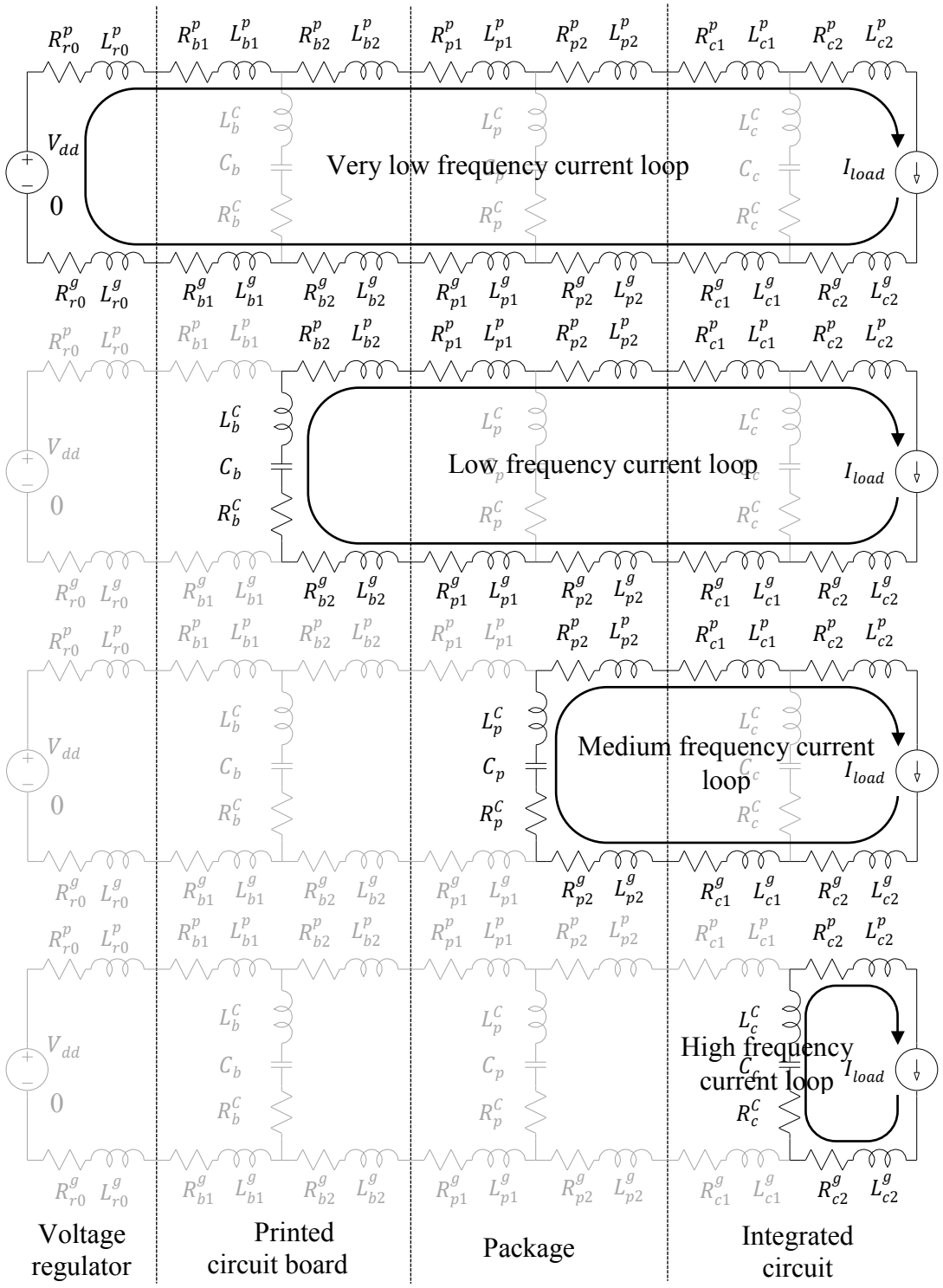


Figure 18. PDN current loops and decoupling with hierarchical decoupling capacitors.

### 3.8. On-chip Power distribution network

Previous PDN circuit models are based on very simplified one-dimensional circuit models. One-dimensional models are useful for understanding the principles of the

power distribution system, but they aren't useful in describing power and ground network across circuit die. Power consumption of on-chip circuitry varies across die area and that leads to different current characteristics in different parts of the PDN. The voltage across the on-chip PDN is therefore non-uniform. It's therefore necessary to consider two- and three-dimensional models of the on-chip PDNs to ensure more accurate characterisation. [4 p. 175]

As mentioned in Section 3.1, on-chip PDN design and impedance characterisation are the most difficult task in PDN design. This is caused by the plain complexity of on-chip PDN. Figure 19 has a simplified example of on-chip PDN. The on-chip PDN given in Figure 19 is a grid structured network. Grid structured PDNs are commonly used in high complexity and high-performance ICs. Each layer of the grid consists of many equally spaced power and ground lines with equal width. The direction of the lines within each layer is orthogonal to lines in the adjacent layers and adjacent layer lines are connected by vias at the overlapping sites. Typically, the lower the metal layer, the smaller the width and space between the lines. The upper layer lines spacing and with are adjusted to match the package's power solder balls, while lowest layer lines are divided to standard cell width. [4 p. 177-179]

Power distribution grids are a very robust way of providing current because multiple redundant current paths exist between load and power supply pads. Power integrity is less sensitive to current changes of individual circuit blocks and grid's single segment failures due to these, redundant current paths. Orthogonal structure of the grid also provides capacitive and inductive shielding for on-chip data signals. Large grid structure doesn't come without disadvantages, however, as the power distribution grid can take up to 20%-40% of chip metal resources. [4 p. 178-179]

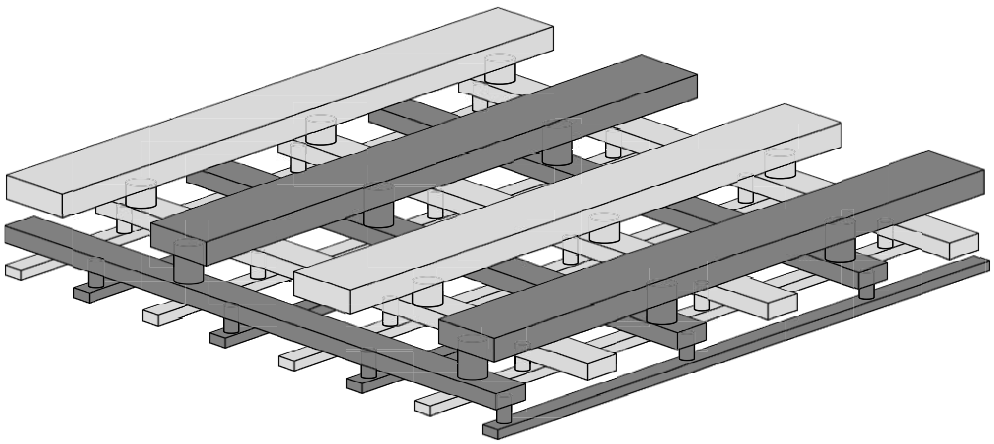

Figure 19. Multi-layered, grid structured on-chip PDN.

### *3.8.1. Die-package interface*

A power distribution network's high frequency impedance is determined by the impedance characteristics of the on-chip and package PDN. On-chip decoupling capacitors are used to ensure low impedance at the frequencies higher than the package decoupling capacitors can handle. That frequency is determined by the inductive impedance of the current path between package decoupling capacitors and IC. Minimizing this parasitic inductance achieves PDN target impedance with the smallest

on-chip decoupling capacitance relaxing requirements for on-chip PDN and on-chip decoupling capacitors [4 p. 188]. [4 p. 184]

Achieving a low impedance connection between the package capacitors and an integrated circuit is, however, difficult, as the IC package has also several other functions than providing the PDN current path: it needs to pass I/O signals and heat and provide mechanical support for chip. Trade-offs between these requirements often prevent the realization of a resonance-free die-to-package interface. [4 p. 185]

Flip-chip packaging is the most common die-package interface in modern and complex ICs. Flip-chip packaging refers to a bonding technique where a die is attached to a package with an array of solder balls. Flip-chip bonding provides a larger number of die to package connections and bonding pads are at the bottom of the chip (chip is "flipped") as compared to traditional wire-bonding. In cost sensitive circuits, the ball connections can be restricted to the edge of the die to reduce package complexity. But high speed and complex ICs have solder balls connections in the entire area of the die. The inductance of a solder ball connection is much smaller than with a bonding wire. A large number of low inductance power and ground connectors allows a high number of parallel connections which decreases inductance even more. It's possible that more than 80% of the thousands of flip-chip connectors are allocated to power to ensure low impedance power connection [13]. Flip-chip packaging significantly decreases the overall inductance of the die to package connection. [4 p. 186-187]

One factor is also that, in edge connected die-packages, the worst-case currents need to travel from edge to die's centre. In full area array, flip-chip packaging power connections are distributed over the whole die area, so currents don't need to travel so long distances. This reduced distance in its turn significantly reduces both resistance and inductance of the on-chip PDN. Flip-chip packaging improves power supply integrity, while also reducing the die area [4 p. 188]. [4 p. 187]

### 3.9. On-chip power distribution network design flow

The high-level design of global PDN typically begins before physical design for high performance circuits. The structure and other main parameters of PDN are decided early. That ensures advanced allocation of metal resources for PDN needs and that will also simplify the following design process. These early decisions are made when little is known about specific power requirements. Early design is therefore very conservative, and design is gradually refined during the subsequent design process steps. Figure 20 shows main on-chip PDN design steps and design flow. Figure 20 also shows how the on-chip PDN design flow relates to IC design flow. Main power grid design steps are: preliminary pre-floorplan design, floorplan-based refinement and layout-based verification [14 p. 738]. Figure 20 describes how a PDN becomes more precise as the circuit design becomes better specified and provides more information for the power grid design process. [4 p. 193-195]

Figure 20 also mentions worst-case current waveforms at layout-based verification. The main idea behind power profiling is to provide these worst case current waveforms during earlier design steps. That way PDN can be designed more precisely earlier.

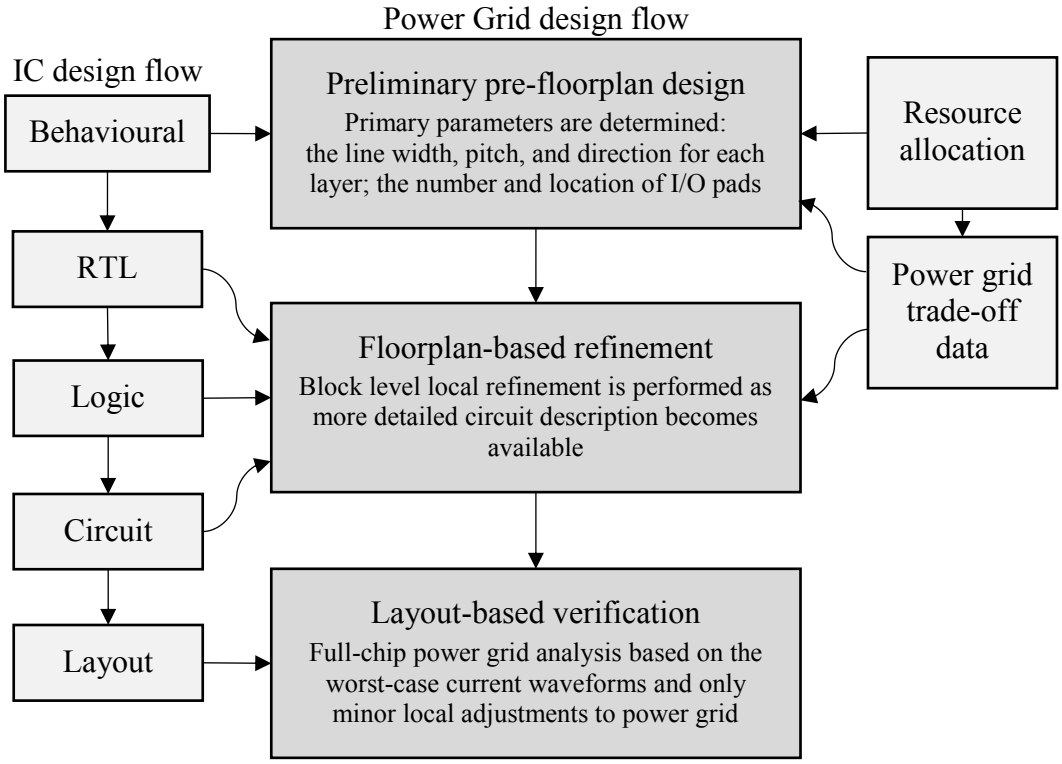


Figure 20. Design flow for on-chip power distribution network.

### *3.9.1. Floorplan-based refinement*

After the floorplan of the circuit is determined, an initial power grid is refined to match better power and current requirements of the individual circuit blocks. The maximum and average power and current of each circuit block is determined based on the type and function of an individual block. Power and current requirements inside a block are still assumed to be uniform but because power and current estimates are now made in block level, that provide non-uniform power requirements across the die. A power grid can now be refined according DC analysis of non-uniform power distribution to fix large scale deficiencies in capacity and many of the primary problems. Computational models are still in this stage moderately simple, so it's possible to make iterative analysis of the power grid. [4 p. 196]

As the IC design continues and the circuit blocks become better specified, the local power consumption in the die can be characterized with more detail and accuracy. After the logic structure of the blocks are known, the current requirements are enhanced based on the number of gates and clocked components on the block. Gate-level simulations can also provide a per cycle estimate of the dc power for a chosen simulation case. Cycle-to-cycle variations of the average power permits a preliminary dynamic AC analysis of the PDN. Dynamic analysis accuracy can be improved if gate-level simulation provides more detailed current waveforms. The worst-case current waveform of each type of gate is pre-characterized in library. Timing information obtained in the simulation can be used to add different gate's current waveforms to current waveform for an entire circuit block. The power grid can be refined according

to these current waveforms to provide sufficient integrity of the on-chip power supply while also minimizing routing resources. As the actual locations of the gates are still unknown, the floorplan-based model's spatial resolution stays relatively rough. The model becomes more complex computationally, as more information of the whole circuit is obtained. However, the number of nodes still remains relatively small, permitting analysis with conventional nonlinear circuit simulation tools such as SPICE. [4 p. 196-197]

### *3.9.2. Layout-based verification*

After the physical design of the circuit is largely completed, a PDN can be analysed and verified to ensure that noise margins are satisfied at every circuit components power and ground terminals. A detailed analysis can be started from individual blocks before moving to whole chip analysis. Individual block noise violations are identified and fixed until specifications are met. Fixing could include things like widening existing power lines, making more power lines or adding additional decoupling capacitance. After blocks are fixed, it's time to verify the whole chip. Whole chip analysis is necessary because neighbouring blocks affect current flow in the power grid. Power hungry neighbouring blocks cause additional currents in power lines and can cause additional voltage drop to the block. [4 p. 197-198]

The difficulty in the whole chip verification is the high complexity and sheer magnitude of the problem. The on-chip PDN of a modern IC can contain millions of interconnects line segments in multi-layer power grid and network loading circuit also consists of millions of transistors and interconnects. At transistor level, whole circuit simulations are therefore infeasible due massive memory and CPU time requirements. Final verification is therefore one of the most challenging task in on-chip PDN design. [4 p. 198-199]

Whole chip verification is successful if the noise margin violations are minor and can be corrected with available resources. However, if the changes in PDN require significant changes in signal routing, signal timing can be critically impaired. That in its turn would cause re-doing routing and timing verification and ultimately cause delays and increased costs. Thus, change limitations in the power grid cause earlier power grid design phases to be very conservative. The resulting PDN is therefore typically overdesigned and over resourced, ultimately increasing the die area (costs) in modern interconnect limited circuits. [4 p. 199]

## 3.10. Calculating required on-chip decoupling capacitance

The placing of the on-chip decoupling capacitors is usually performed iteratively. Each iteration step consists of two steps: analysis and capacitors size/location/amount modification. Magnitude of power supply noise is determined in the analysis step and after that capacitors are modified according to the analysis results in parts of the circuit which don't meet specifications. Then, the circuit goes back to analysis. Iterative process continues until the PDN noise target is reached. Occasionally, some parts of the circuit are unable to meet the power supply noise specifications. If that happens, then, the layout should be changed so that there is more room for decoupling capacitors

or room to place decoupling closer to the circuit that doesn't meet specifications. [4 p. 217]

Interconnect limited circuits typically contain blank areas where decoupling capacitors can be placed without increasing die size. After that, every on-chip decoupling capacitor increases the die area. Although a large amount of on-chip decoupling capacitance increases power supply integrity, they won't come without a cost. Every decoupling capacitor leaks current, increases complexity and possibly increases the die area as well. For those reasons, the amount of decoupling capacitance is kept reasonable low. [4 p. 217]

Different calculations strategies exist to lower the amount of needed iterations and three of those are described in in following three sub sections: charge-, excessive noise amplitude- and excessive noise charge-based.

### *3.10.1. Charge-based*

One of the simplest ways to calculate required decoupling capacitance is based on average power current $I_{avg}$ at a certain point. Decoupling capacitance $C_{dec}$ is calculated by

$$C_{dec} = \frac{\Delta Q}{\Delta V_{dd}} = \frac{I_{avg}}{f_{clk}\Delta V_{dd}}, \tag{28}$$

where $\Delta Q$ is amount of charge needed at a certain point during one clock cycle, $\Delta V_{dd}$ is noise margin and $f_{clk}$ is the clock frequency. The main idea behind equation (28) is that all the currents are provided by on-chip decoupling capacitors during the one-cycle. This is true if other decoupling capacitors are decoupled (impedance is much higher) by on chip decoupling capacitors and that capacitors are re-charged during one clock cycle before the next clock cycle begins. [4 p. 218-219]

Both assumptions cannot, however, be simultaneously satisfied with high accuracy. If the impedance of the package-to-die interface is low, a significant portion of the current is provided by package decoupling capacitors, overestimating capacitance requirements. And vice versa, if the impedance is high, on-chip capacitors can't be loaded during one clock cycle. Required capacitance can be calculated more accurately if package and package-die impedances are known. With these considerations, charge-based calculation is robust but a conservative way to calculate necessary decoupling capacitance. [4 p. 219-220]

### *3.10.2. Excessive noise amplitude-based*

More aggressive capacitance budgeting is possible. One of those is to use excessive noise amplitude as a metrics in capacitance calculation. The circuit is first simulated without on-chip decoupling capacitors, so that the noise violations can be measured. Capacitance is then calculated as

$$C_{dec} = \frac{(V_{noise} - \Delta V_{dd})}{V_{noise}} \frac{\Delta Q}{\Delta V_{dd}}, \quad (29)$$

where $V_{noise}$ is maximum noise amplitude, $\Delta V_{dd}$ is noise margin and $\Delta Q$ is amount of charge needed at a certain point during one clock cycle. Noise amplitude is measured at a certain accuracy at certain points, like at block boundaries. Equation (29) implies that those parts of the circuit where the noise margin is not violated doesn't need decoupling capacitors. In other parts, capacitance is determined by the excessive noise amplitude. Excessive noise amplitude-based on equation (29) leads to lower capacitance requirements than charge-based on equation (28). [4 p. 220-221]

### *3.10.3. Excessive noise charge-based*

The previous excessive amplitude-based equation could be improved by taking time integral from excessive voltage, so that also the duration of noise violation is taken into account by excessive noise charge rather than just violation's maximum amplitude. Longer excessive voltages cause bigger problems for power integrity. Calculating excessive noise charge-based capacitance is much more challenging than previous ones and calculation also needs voltage waveforms from every measure point not just maximum deviation at those points. [4 p. 221-222]

# 4. POWER PROFILING

Chapter 4 describes how a power profile is created with a power profiling tool and why a power profile is useful. Section 4.1 explains how power profiling is practical. Section 4.2 describes power profiling flow and what files, information and steps power profiling needs. Section 4.3 shows one example power profile figure and section 4.4 deals with interesting time windows in that power profile figure. Finally, Section 4.5 describes how and where resulted time windows are utilized.

## 4.1. Power profiling introduction

Accurate time-based power simulations are slow for complex ICs making long simulation cases and large simulation activity files unpractical. Power profiling is high performance power estimation which can be used to generate a cycle-based power profile from large simulation activity files. Power profiling trades off accuracy for performance and that is why it doesn't report absolute power numbers. Power profiling generates a power profile, which can be used to identify interesting time windows from large activity files for power and thermal analysis. These short time windows can be used for PDN design, simulation and sign-off, where large and unpractical activity files are unusable. Because power profiling uses activity files from different use case simulations as an input during power profiling, power profiler results should correspond to realistic usage scenarios. Power profiling can be done in both register-transfer-level (RTL) and gate-level.

## 4.2. Power profiling flow

Preparations are needed before power profiling can be performed. Power profiling needs multiple input files. Figure 21 shows a power profiling flow diagram. The flow diagram describes main steps for power profiling and input files for those steps. Steps are blue boxes and files are in green or yellow document boxes in Figure 21. Also, there is a grey document box which is a collection of all the rest files and parameters which could vary a lot case by case.

The first step of the power profile flow is design import. This step imports RTL source code and chosen standard cell libraries. The tool compiles and maps design source code to a functional standard cell circuit. There are also some parameters which affect this process. Parts of the design can be left unsynthetized (black boxed) or macros can be ignored, for example. After that, the tool creates the proprietary netlist file from the imported design.

The second step is the power profiling itself. First, the power profiler imports the proprietary netlist which was made in the previous step. Then, it maps each cell power consumption numbers to standard cell library and net parasitic resistance and capacitance values to technology library wire load model (WLM) or from some other format parasitics file, to the used netlist. Finally, the tool reads nets simulation waveforms from the activity file and calculates net activities from those waveforms. Now, the tool can calculate power usage using activities for the cells and the nets and their power characteristics. The tool can also create an estimate for a clock tree if one

doesn't exist in design and calculate a clock tree power estimate using estimated clock tree and WLM for clock tree cells. Power profiling flow produces power profile figure.

Yellow boxes in Figure 21 describe the differences in the flow for gate-level power profiling. Steps are the same, but the first step takes the gate-level netlist as input and power profiling needs a new activity file to match gate-level netlist or file that maps changed netlist names from RTL to gate-level. Gate-level power profiling should be more accurate than RTL power profiling, depending on how much more information the tool has available during power profiling. Additional information in gate-level could be for example activity file waveforms with glitches, net parasitics and more realistic standard cell distribution. It is also possible to mix RTL and gate-level blocks if necessary.

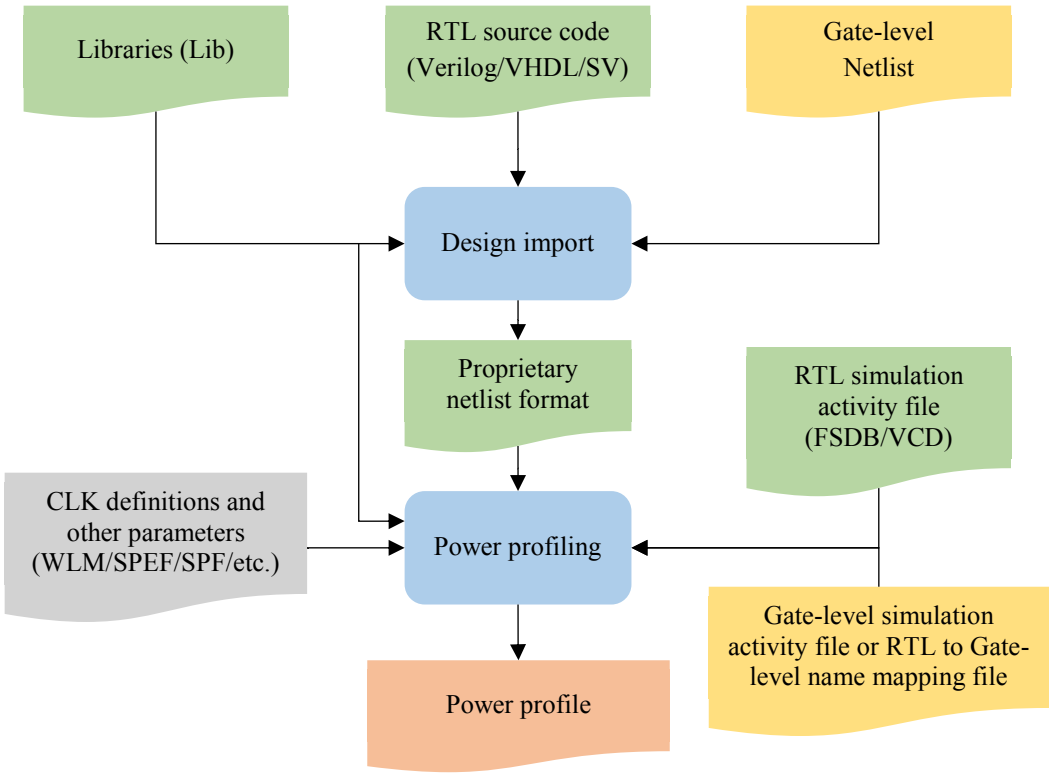


Figure 21. Power profiling flow diagram.

### *4.2.1. Libraries*

Libraries include two main types of libraries used in application-specific integrated circuit (ASIC) design: technology file/library and standard cell libraries. Technology file contains information and parameters to design targeted to specified process technology [15 p. 38]. The technology file describes physical properties and limits of targeted process technology.

The standard cell library contains pre-established layouts and pre-defined electrical characteristics for universal ASIC building blocks, standard cells [16 p. 10-11]. RTL synthesis tools read available gate-level components from the standard cell library and

synthesizes RTL design to those gate-level components during synthesis. The standard cell library contains physical standard cell designs for each gate-level component [15 p. 2]. The standard cell library includes lookup tables (LUT) with electrical and timing specification and accurate behavioural model for simulation and timing analysis for each standard cell [16 p. 29]. The power profiling tool extracts available gate-level components LUT and models from the standard cell library to calculate power estimates for power profiling.

Standard cell libraries could also include multiple different standard cell variants (corners) for each gate-level component. A standard cell corner could differ from each other by threshold voltage, operation temperature, supply voltage and/or speed [15 p. 31-33].

### *4.2.2. Netlist*

A netlist is a file which contains information about what components make up the circuit and how those components are connected to each other [16 p. 40, 42]. Component connections make up circuits wires/net. Netlists could be describing design in different phases of flow. It's usually used with a description like gate-level netlist, which means that it describes gate-level components and their interconnections. A netlist doesn't have more information about a circuit. Tools refer the netlist to the standard cell libraries and other information to make a working circuit.

### *4.2.3. Simulation activity file*

A simulation activity file contains netlist's nets waveforms in the time domain. Net activity is pre-recorded, so the power profiling tool can use that information as it extracts every net's activity which it uses to estimate power consumption during power profiling. The power profiling tool doesn't need to care about actual operation of a circuit because the activity file tells the tool what is happening during simulation case.

### *4.2.4. Net parasitic resistance and capacitance models*

The power profiling tool uses some net parasitic model to estimate net power usage for power profiling. Wire load model (WLM) is the roughest estimate. WLM uses statistical models from a library to estimate net parasitics without any knowledge on interconnect's physical dimensions. After the synthesis or layout is done, net parasitics could be extracted from design to increase power profiling accuracy. Post- and pre-layout parasitics could be extracted from design which then defines gate-level netlists interconnect parasitics. Pre-layout parasitics are estimated but post-layout parasitics could be extracted more accurately from the design's physical layout. [15 p. 84-85, 138] [16 p. 586]

### 4.3. Power profiler flow results

The power profiling flow produces a power profile figure. One RTL block with 28 million gates and one of its simulation activity file is chosen as an example. Figure 22 shows a normalized power profile figure and its running average as a function of clock cycles for RTL block with a corresponding simulation case. A power profile immediately visualises interesting information about a block's behaviour during simulation. The power profile given in Figure 22 has three distinguishable zones.

The first zone of Figure 22 has a rising power profile until the profile settles. The first zone most likely includes block initialization and configuration and it lasts from 0 to about 60,000 cycles. Beginning of power profile doesn't seem all that significant, but there is a spike right at start-up which could be interesting.

The second zone has a massive increase in the power profile and the profile stays up for about 50,000 cycles until it decreases back to idle level. This is the most interesting interval from the whole power profile, simply because the power profile is highest during this zone. The block is working at full throughput during this window. The power profiles average stays stagnant, but the power profile has quick variations in level.

The third zone is the rest of the power profile. The power profile is very flat, after the profile decreases at 110,000 cycles. Most likely simulation data has ended, and the block is in idle mode. This interval can be used to run simulations in idle mode for idle power optimization. Other than that, the end of Figure 22 is unnecessary.

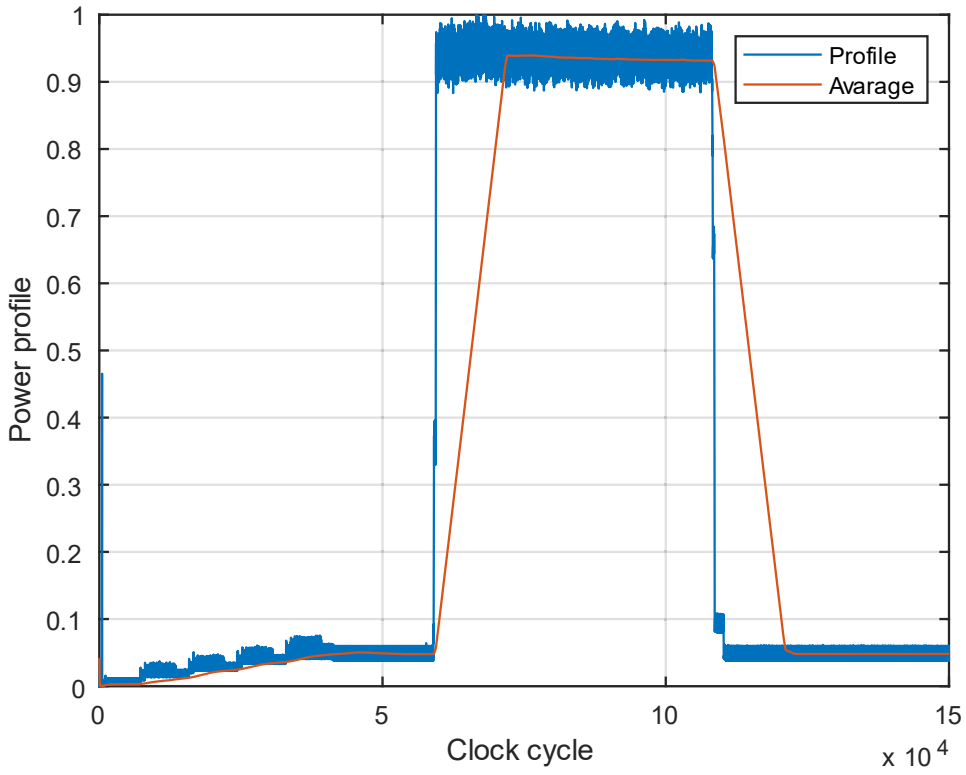


Figure 22. RTL power profile and profiles running average.

## 4.4. Interesting time windows in power profile

The power profile figure given in Figure 22 is informative, but there is a problem: how to find those interesting power profile windows. Figure 22 is simple enough to enable power profile window extraction by hand. What if a power profile is more complex? The power profiling tool reads a power profile and analyses it clock by clock. After analysis, the power profiling tool reports locations of interesting power profile windows. Reported interesting power profile windows are: highest average power, high peak power profile and largest di/dt or largest current change in power profile.

### *4.4.1. Highest average power in power profile*

As the name indicates, this result shows the location of the highest average value in a power profile. The highest point in average power can be seen in Figure 22. The highest point in average power is right when average, red figure, reaches top. The highest average point in a power profile could be used to estimate the worst-case average power usage and heat dissipation. The amount of clock cycles, which are used to calculate a running average of power profile, can be changed. In this case, averaging window size seems to be quite high as it reacts really slow to a steep change in power profile. Averaging window seems to calculate only previous clock cycles, so the average figure marks high average power window endpoint and it also causes strange delay in average figure when power profile drops.

### *4.4.2. High peak power profile*

As the name implies, this power profile window contains a high peak power profile window. The window is more precisely called a high power profile peak during high power usage. It's not necessarily the highest point in a power profile, but, in this case, it happens to be the highest point of the power profile. The power profile is also normalized to this value. Figure 23 shows this highest peak in the power profile in the middle of the figure. The peak can also be seen in Figure 22 at about 70,000 clock cycles. This power profile window can be used to test if a PDN could carry enough peak current without issues, e.g. how IR-drop behaves with worst-case peak currents. Possible issues revealed by this could be for example: power rails are not wide enough to carry high current or a PDN doesn't have enough decoupling capacitors to supply high peak current during high power usage.

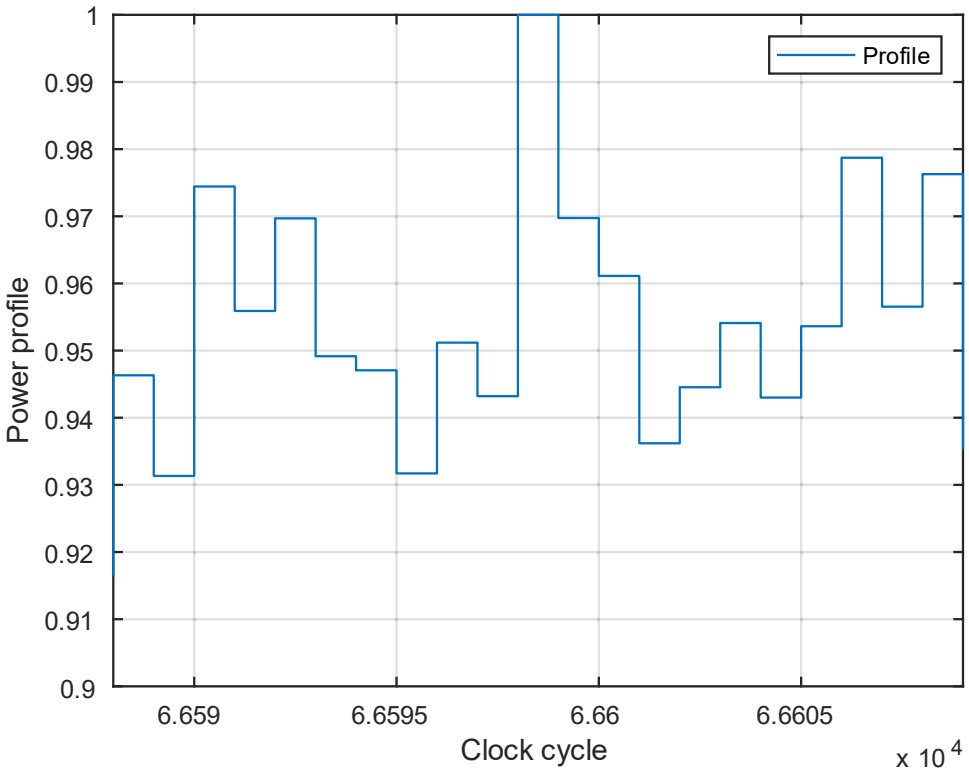


Figure 23. High peak power profile.

### *4.4.3. Largest current change*

The largest current change happens when the power profile has the largest difference in magnitude at adjacent clock cycles. Figure 24 shows the tool's chosen time window for the largest current change and the largest current change is in the middle of that time window. The power profile window is from Figure 22 profile's raising edge. The largest current change can be used to test if a PDN can cope with quick current changes and it's especially useful while testing how PDN parasitic inductance resists fast current changes by adjusting voltage over inductance (Ldi/dt drop).

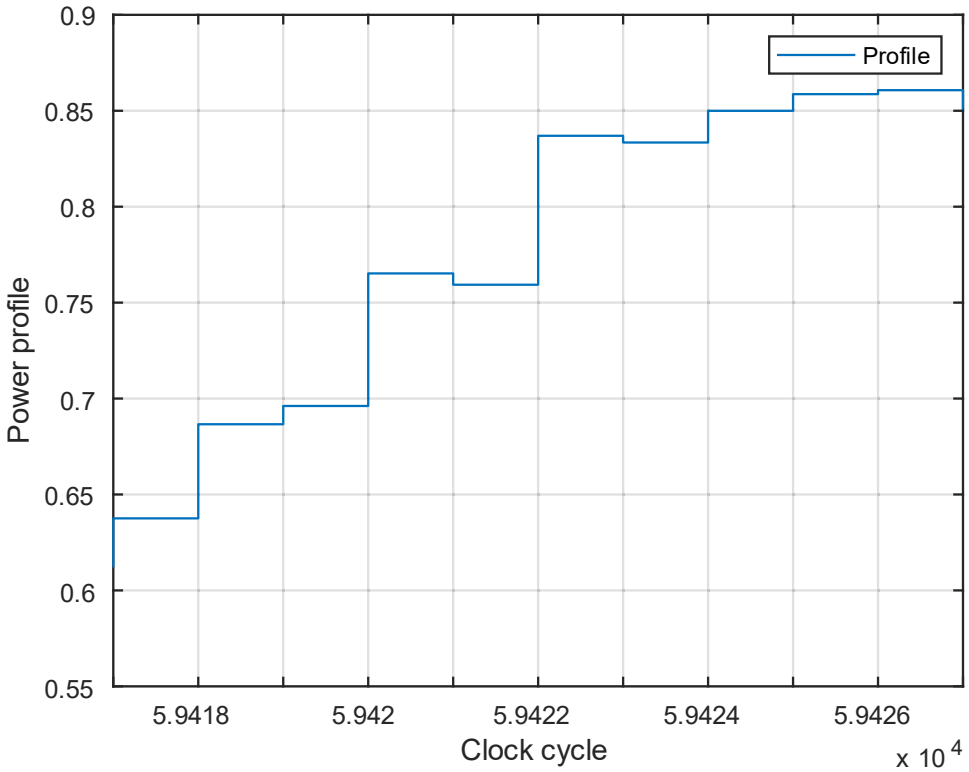


Figure 24. Largest current change in power profile.

### 4.5. Power profiling time windows utilization

PDN simulation is impossible with long simulation cases by the sheer complexity of the layout simulations. Thus, PDN design and signoff usually relies on some vectorless simulation like simulation with average net activity numbers. That leads to an inaccurate simulation result which in its turn leads to increased margins. A PDN becomes too hefty and conservative.

The problem with PDN simulation can be solved with resulting time windows. Time windows are used to locate and collect relevant input vectors for each of the time window. Input vectors can then be used during PDN design and signoff to simulate accurate test scenarios. Accurate simulation is possible because simulation is needed only for these pre-defined short time windows. There is no need to run the whole test cases because time windows should include most challenging parts of the whole simulation case. Simulation with time windows should result in more accurate simulation results which enable the design of more accurate, cheaper and smaller PDN.

Power profiling results enable accurate on-chip PDN simulations which could also be utilised in chip-package co-simulations enabling more accurate package design.

Power windows locations could be also utilized in normal RTL power estimation to show each blocks power consumption in that case. High peak power window could be used to identify high power blocks so that they can be placed closest to the power pads or in wider power rails. Largest current change power window could be used to identify blocks that caused large current change and thus need plenty of decoupling capacitors to provide charge for big current transients.

# 5. RTL POWER PROFILING RESULT ANALYSIS

Chapter 5 analyses how accurate early power profiles are and how good chosen time windows are. Section 5.1 shows absolute RTL power estimation accuracy and RTL power estimation accuracy with calibration. Section 5.2 analyses time windows by comparing power profiles to gate-level power simulation results.

## 5.1. RTL power estimation accuracy

Power profiling uses conventional RTL power estimation methods as it creates power profiles. RTL power estimation has known limitations with its accuracy. RTL power estimation can never be 100% accurate since it can't know what happens during synthesis and place and route. Also, designs differ a lot and RTL power estimation settings could affect accuracy differently case by case.

Table 1 shows used setups RTL power estimation accuracy related to gate-level design. The simulated 28 million gates block is only part of the system-on-chip and it has no I/O pads, so that I/O category is missing from the table. Estimated RTL power consumption is about half of the gate-level estimated power consumption. Two categories vastly differ from each other which are clock and memory powers. Estimated memory power consumption is about the same in RTL and gate-level and estimated clock tree power consumption is about the fourth of the gate-level power consumption. Big differences between categories could lead to inaccuracies in a power profile because it could emphasize some category too much, as seen in later simulations.

Some of the RTL power estimation inaccuracies can be corrected with calibration. The next section explains what methods calibration can contain. Estimated calibrated RTL power is very close to gate-level estimated power in Table 1. But this result is too good because it uses same designs gate-level as source for extracted parasitic calibration which is practically impossible in "real" cases. There rarely is a ready gate-level design when RTL power estimations are run. In this case, the simulated block was purposely chosen in a way that it had a synthesised gate-level design available because gate-level design was used as the benchmark.

Table 1. Average power consumption

| **Design phase** / **Category** | **RTL** | **Calibrated RTL** | **Gate-level** |
|---|---|---|---|
| Register | 0.62 | 0.85 | 1 |
| Logic | 0.70 | 1.20 | 1 |
| Memory | 1.06 | 1.07 | 1 |
| Clock | 0.25 | 1.01 | 1 |
| Total | 0.48 | 1.07 | 1 |

### *5.1.1. Calibration in RTL power estimation*

In addition to WLM, power profiling can use also other net parasitics models from existing designs, during power profiling. Existing design must be for the same technology and as similar as possible to get best possible results. The tool reads the existing design's parasitics and makes a more accurate statistical parasitics model for power profiling. Power profiling then uses the acquired statistical parasitics model instead of WLM to improve RTL power estimation accuracy. The power profiling tool can also read post-synthesis cell distribution and used cell versions (corners) and use that information when the tool estimates what cells RTL is synthesised to during RTL power estimation. The power profiling tool could also extract a clock mesh/tree model from existing design and use that to estimate a clock's power consumption in RTL designs.

All these calibrations improve RTL power estimation accuracy. The power profiling tool can use methods separately or collectively. If RTL power estimation is accurate enough, it will make gate-level simulations pointless. The problem with gate-level simulations is that gate-level simulations are complex, and the results will come too late anyway to have any significant impact on design.

## 5.2. Power profiler result windows analysis

Power profiler absolute power estimation accuracy isn't the most important issue. The most important thing is that power profiler accuracy is close enough so that those power windows could be decided accurately.

Section 4.4 power windows are widened and some comparison figures are collected to Figure 25 and Figure 26. Figure 25 and Figure 26 contain the original RTL power profile on top and calibrated RTL power profile and time-based gate-level power figure in the middle and bottom. Time-based gate-level power simulation is the benchmark. It is as close to the real circuit as a cycle-based simulation result can get in this case. The gate-level power figure is normalized to average power on the whole high activity region in the power profile as power profiles are normalized to corresponding peak power. The calibrated RTL figure is for comparison purposes to show how much the calibrated RTL power profile differs from the plain RTL power profile.

Figure 25 power profiles are very similar. Both show a high power profile during the window as was expected. Peaks and notches seem to match between figures, but the calibrated RTL has less fluctuation and it doesn't have the same profile peak as the plain RTL has. Fluctuation seems to decay as RTL design nets are calibrated with more realistic parasitics and clock three power is better matched. Same can be seen in the gate-level power waveform as its relative flat. The gate-level power waveform doesn't match as good as power profiles, but it also shows high power usage as the figure is above the normalized average value. The gate-level power simulation figure matches power profiles. Power usage is high during the high peak power window.

Figure 26 shows the largest current change profile windows. All the three curves are similar. The only difference is that some of those figures are steeper than others. Gate-level power simulation drops least during the time window. The gate-level power

simulation figure shows that the time window matches with rising power consumption. The largest current changes very likely within the chosen power window.

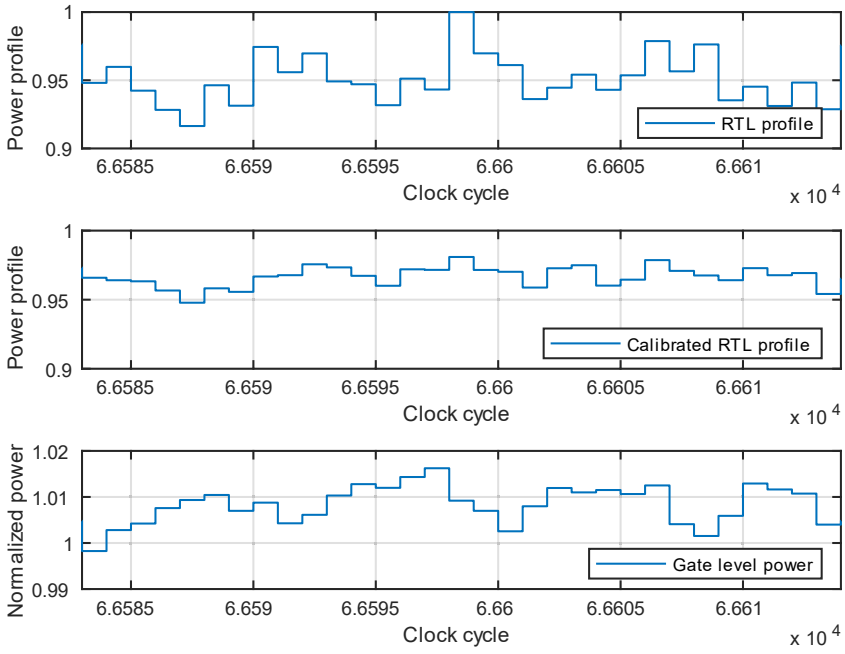


Figure 25. RTL high peak power profile, calibrated RTL power profile and time-based gate-level simulated power on the same time window from top to bottom.

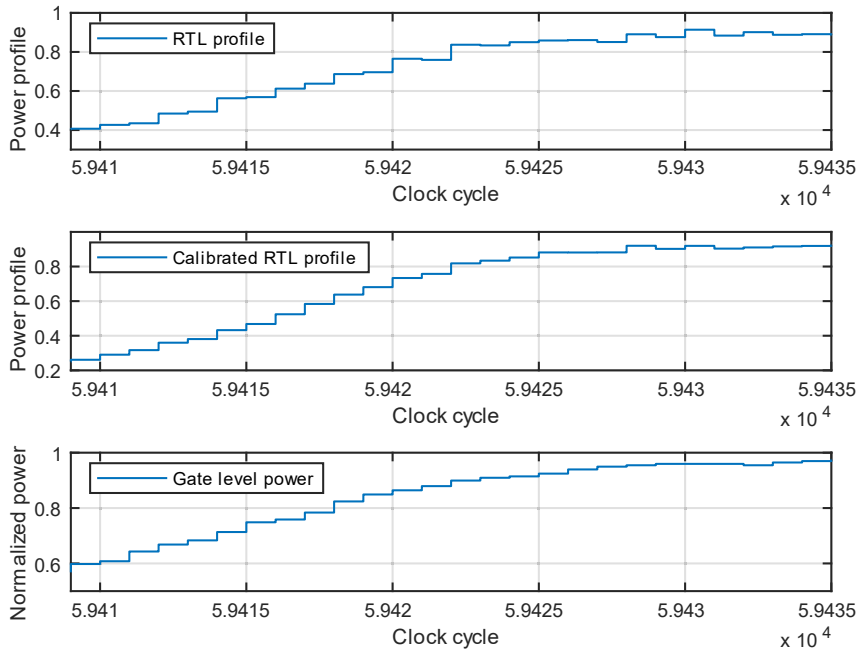


Figure 26. RTL largest current change power profile, calibrated RTL power profile and time-based gate-level simulated power on the same time window from top to bottom.

### *5.2.1. Calibrated RTL power profile windows*

Calibrated RTL will lead to a new power profile. This means that also the power profile windows could be new for the calibrated RTL. In this case, the largest current change window is the same as in the plain RTL's case, but the high peak power profile chooses a new window. The new window is in Figure 27 with the same reference figures. The new window is chosen so that it includes the calibrated RTL power profile peak. A similar peak can also be seen in the plain RTL's power profile. Generally, Figure 27 and the other high peak power profile given in Figure 25 are very similar to each other. Neither of the figures seems to have a better high peak power window. The conclusion drawn here is that calibration does improve power estimation accuracy, but it didn't affect time window selection, at least not with this block and test case.

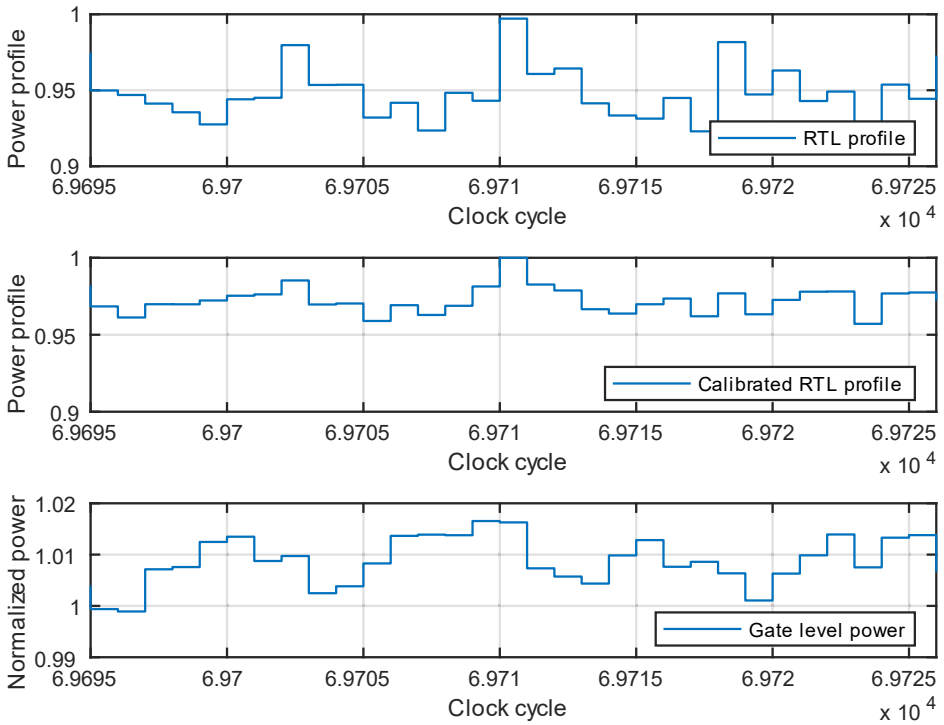


Figure 27. Calibrated RTL high peak power profile, RTL with power profile and time-based gate-level simulated power on the same time window from middle to top to bottom.

# 6. DISCUSSION

The objective of this thesis was to study how RTL power profiling can help the design and signoff of a power distribution network in digital integrated circuits. A power distribution network was studied theoretically and valuable information for power distribution network design and signoff from power profiling was gained. Then, power profiling flow was explained and the flow's results accuracy and usefulness were analysed.

The theoretical part of the thesis starts with a chapter about CMOS circuit and their power dissipation. That was not topic of the thesis as such, but it is included in order to give some background information about CMOS circuit's power dissipation. The theoretical study of the power distribution network makes most of the pages. A wide variety of topics related to a power distribution network is mentioned. Decoupling capacitors play a surprisingly big role in the thesis, but decoupling capacitors are a very important part of the power distribution network as well. Decoupling capacitors ease requirements for other parts of the power distribution network. The thesis provides a basic information package about a power distribution network for interested engineers. The thesis also tries to identify and explain what kind of information is useful to power distribution network design and signoff.

The practical part of the thesis explains power profiling flow thoroughly and explains how results can be utilised in power distribution network design and signoff. It also provides power profiling results from one sample design block and simulation case. Power profiling results are compared to gate-level power simulation figures. In this case, power profiling results match the gate-level reference figures and power profiling results seems to be what they theoretically should be. That conclusion might not be true for a different design blocks or even for a different simulation cases on the same block. Cases were limited to just one in order to limit the scope of the thesis. Future work could run power profiling for multiple blocks and simulation cases in order to validate the conclusion on wider scale. It was surprising that power profile matches the reference figure that well even when RTL power estimation shows several inaccuracies between RTL and gate-level models. Planned RTL model calibration were nonetheless run and even RTL calibration improved RTL power estimation accuracy it didn't have big impact on power profiling result figures. Power profiling results are promising, and even plain RTL power profiling seems to be a useful method to provide desired power information for power distribution network design and signoff.

Figure 20 summarises on-chip power distribution network design flow and it mentions worst-case currents as part of the verification step. Power profiling idea is to identify these worst-case currents earlier in design flow, so that the worst-case current can be utilized in early design steps. Figure connects power profiling to the power distribution network theory and show that power profiling could be used in traditional design flow to just identify worst-case currents for verification. It is up to a power distribution network designer where in design flow he or she wants to utilize power profiling.

"Real" design would utilise simulation/verification tools which use real current waveform after power profiling. Current waveform changes a lot inside a clock cycle. The highest current is needed at clock edges, but transistors clock delays can be different inside a chip. This makes power distribution network current waveforms very

complicated. Accurate current waveforms were left outside of this thesis. Probably, they would provide useful information for power profiling accuracy analysis if that is analysed in further studies. It is possible that some future work could continue the topic by analysing a power profile's time windows with a tool that can analyse current waveforms. That would confirm if power profiling time windows are actually useful in real use cases.

I hope that the objective of the thesis was met, nevertheless. Power profiling was studied with example case results and power profiling was connected to power distribution network theory.

# 7. SUMMARY

The objective of this thesis was to study RTL power profiling flow and how power profiling flow result time windows could help in power distribution network design and signoff.

Thesis is started by explaining CMOS power dissipation in Chapter 2 in order to give an understanding where how modern CMOS circuit consumes power. Chapter 3 contains theory behind the power distribution network and it explains the main voltage drop sources in a power distribution network and how power profiling time windows link up to these voltage drops. There is also a wide variety of different topics which refer to a power distribution network like decoupling capacitors, impedance profile and on-chip power distribution network design flow. Chapter 4 explains power profiling flow and Chapter 5 contains time window and RTL power estimation accuracy analysis and comparison to reference gate-level design.

RTL power profiling result time windows match the theory. Time windows seem to show highest current transient and peak current from the whole simulation case. Power profiling would then provide help in power distribution network design and signoff because these time windows could be used in analysis instead of the whole simulation case. This would reduce power distribution network simulation times dramatically.

Although RTL power estimation result seems to have significant inaccuracies, the resulted RTL power profiling time windows shape match gate-level power profile which is used as reference. The RTL model is also calibrated and, while the RTL power estimation accuracy is increased significantly, it doesn't change resulting time windows dramatically. It seems that plain RTL power profiling is adequate enough to result in useful time windows for PDN design and signoff, for this design block and simulation case at least. As such, RTL power profiling flow looks very promising based on the results gained in this thesis.

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