Parallel Association of Power Semiconductors: An Experimental Evaluation with IGBTs and MOSFETs

Tiago J. C. Sousa
ALGORITMI Research Centre
University of Minho
Guimarães, Portugal
tsousa@dei.uminho.pt

Vítor Monteiro
ALGORITMI Research Centre
University of Minho
Guimarães, Portugal
vmonteiro@dei.uminho.pt

Bruno Nova
ALGORITMI Research Centre
University of Minho
Guimarães, Portugal
a71314@alunos.uminho.pt

Frederico Passos
ALGORITMI Research Centre
University of Minho
Guimarães, Portugal
a62031@alunos.uminho.pt

José Cunha
ALGORITMI Research Centre
University of Minho
Guimarães, Portugal
jcunha@dei.uminho.pt

João L. Afonso
ALGORITMI Research Centre
University of Minho
Guimarães, Portugal
jla@dei.uminho.pt

***Abstract*— This paper presents a study on the parallel association of power semiconductors. The main purpose of this paper is to demonstrate that the parallel association of lower rated power semiconductors can be more advantageous than the use of a single higher rated power semiconductor, both economically and in terms of dynamic performance, i.e., switching behavior and semiconductor temperature. In this context, two different power semiconductor technologies were tested: (1) Insulated gate bipolar transistors (IGBTs); and (2) Metal oxide semiconductor field effect transistors (MOSFETs). For each technology, the adopted methodology consisted of verifying the dynamic performance of a single higher rated power semiconductor, comparing it with the dynamic performance of a set of five parallel-connected lower rated power semiconductors, focusing on the current sharing between the devices. The obtained experimental results demonstrate that the parallel connection of lower rated power semiconductors can be advantageous over the use of a single higher rated power semiconductor above certain power levels, offering better switching characteristics and lower cost.**

Keywords—Power Semiconductors, Parallel Association, Insulated Gate Bipolar Transistors (IGBTs), Metal Oxide Semiconductor Field Effect Transistors (MOSFETs).

I. Introduction

Power semiconductors are used in a variety of applications, ranging from small electrical appliances, such as battery chargers of mobile phones and laptops, to more power demanding applications, such as uninterruptible power supplies, traction drive systems for electric motors and battery chargers of electric vehicles. Several studies can be found in the literature regarding the paralleling of insulated gate bipolar transistors (IGBTs) [1]-[7] and metal oxide semiconductor field effect transistors (MOSFETs) [8]-[12].

Although this approach is unavoidable for very large currents (thousands of amperes), it can be advantageous even when single semiconductors are available for the desired currents. Typically, as the power rating of a semiconductor increases, its cost also increases. In fact, for current ratings of hundreds of amperes, the cost of the semiconductors tends to increase in a nonlinear fashion; besides, their dynamic performance tends to decrease (e.g., higher switching times and higher capacitances), limiting their operation to low switching frequencies, even because it demands a higher capability from the gate driver. Both the cost and performance issues can be solved by the implementation of lower rated devices connected in parallel instead of using a single higher rated device. Besides, this approach allows distributing the temperature hot spots along the heatsink instead of focusing the heat in a single spot. An additional advantage of this approach is the improved reliability of the power system, since it can maintain its operation (although with a lower power rating) if a device succumbs, which is not possible with a single higher rated device. However, the paralleling approach requires additional volume and proper handling, i.e., the current sharing along the different devices must be kept as balanced as possible in order not to cause damage and malfunction of the desired circuit [13]-[17]. In this context, this paper presents a study on the parallel association of power semiconductors, namely IGBTs and MOSFETs, focusing especially on the dynamic performance of a single higher rated device and its comparison with five lower rated devices connected in parallel for the same operating conditions. A cost analysis is also performed in order to emphasize the benefits of the parallel association of power semiconductors.

The paper is structured as follows: Section II presents the experimental setup especially developed for this study, mainly the gate drive circuit and the test circuit; Section III presents the experimental results, firstly for the IGBTs and then for the MOSFETs; Section IV presents a comparison in terms of dynamic performance and cost for the IGBTs and MOSFETs implemented in this paper; finally, Section V presents the conclusions of the work carried out.

II. Experimental Setup

A. Gate Driver Circuit

This section presents the designed circuit to perform the experimental validation, as well as the driver circuit of the paralleled power semiconductors. Three main approaches can be used for the driver circuit of parallel devices, namely: (1) One gate driver for each device; (2) A single gate driver for all devices, using a single gate resistor; and (3) A single gate driver for all devices, with a gate resistor for each device. The first approach can lead to switching mismatches due to different propagation times of the gate drivers, which is not desirable. Using a single gate driver for all devices eliminates this issue, making the mismatching depend mainly on the gate impedance. It should be referred, however, that the differences in the gate-threshold voltages of the switches are always an

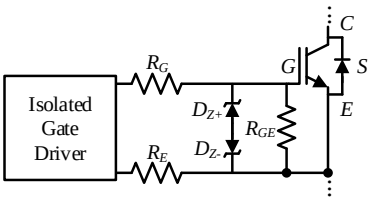


Fig. 1. Driver circuit and gate protections implemented for each power semiconductor (IGBTs in the figure).

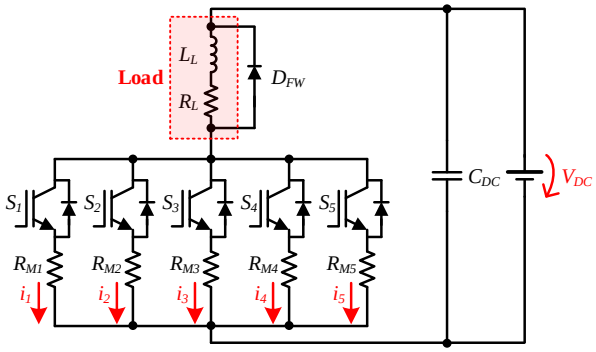


Fig. 2. Implemented test circuit for the parallel association of five power semiconductors (IGBTs in the figure).

issue regardless the number of used drivers. By using a single gate resistor, the resistive component of the gate path impedance is equal for all the devices, but oscillation can occur due to differences in the inductive component of the gate path impedance. On the other hand, by using a gate resistor for each device, oscillation problems are minimized, but the switching times are higher. Hence, approach (2) requires a careful layout, while approach (3) sacrifices part of the driver performance in order to prevent significant oscillations. In the scope of this paper, approach (3) was chosen. Additionally, instead of a single gate resistor, the desired resistance value was split in the gate and in the emitter (or source) in order to prevent loops due to the connection of multiple devices to the same point, besides the fact that each emitter (source) terminal presents parasitic voltages induced by each device current.

Fig. 1 shows the implemented circuit for each power semiconductor, apart from the isolated gate driver that is the same for all devices. Besides the gate (R_G) and emitter (R_E) resistors, this figure shows two types of protections connected between gate and emitter: (1) Two-level peak limiter with two zener diodes (D_{Z+} and D_{Z-}), which prevents both positive and negative voltage spikes in the gate-emitter voltage; and (2) A resistor acting as a pull-down for the gate (R_{GE}) to prevent parasitic turn-on of the device.

B. Test Circuit

The implemented test circuit for the parallel association of the five power semiconductors (IGBTs as example) can be seen in Fig. 2. Basically, this circuit is the setup commonly employed by semiconductor manufacturers to test the switching behavior of IGBTs and MOSFETs. In series with each device (S_1 to S_5), a 0.1 Ω shunt resistor (R_{M1} to R_{M5}) was used in order to measure the individual currents of the devices. The type of used load was resistive-inductive (R_L and L_L), thus the connection of a freewheeling diode in antiparallel (D_{FW}) was needed. This figure also shows a dc power supply (V_{DC}) and a decoupling capacitor (C_{DC}).

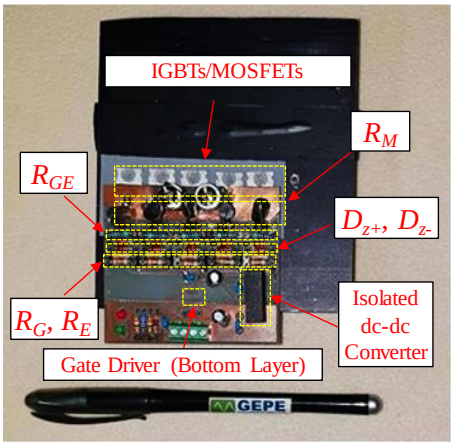


Fig. 3. Developed prototype for the parallel association of five IGBTs or MOSFETs with integrated driver circuit.

TABLE I. PARAMETERS OF THE IMPLEMENTED LOAD

LOAD	#1	#2
R_L	9.0 Ω	4.6 Ω
L_L @dc	41 µH	23 µH
L_L @50 kHz	9.9 µH	5.5 µH
L_L @100 kHz	8.4 µH	4.7 µH
L_L @200 kHz	6.7 µH	3.7 µH

C. Developed Prototype

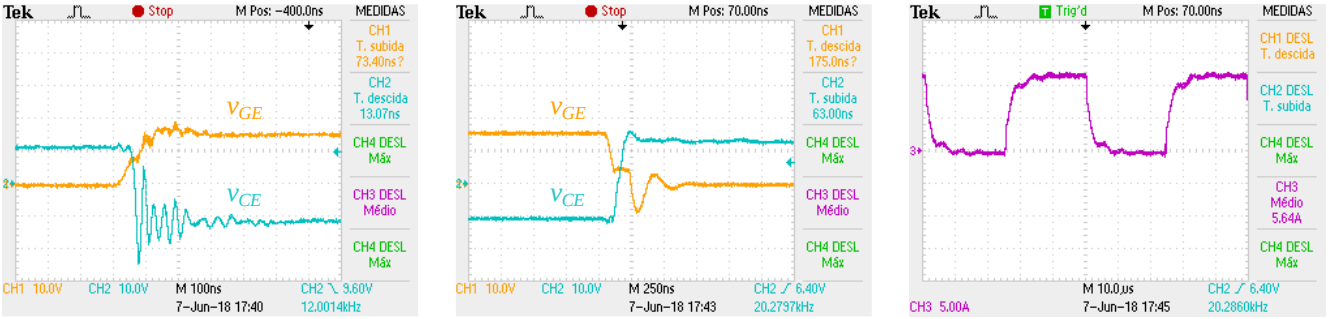
The laboratorial prototype, specially developed for the parallel association of five IGBTs or MOSFETs analyzed in this study, can be seen in Fig. 3. The developed printed circuit board (PCB), which is attached to a passively cooled heatsink, comprises both the gate driver and the power semiconductors. The implemented gate driver was Analog Devices model ADUM3123, an isolated single-channel gate driver capable of delivering peak currents of 4 A and a maximum switching frequency of 1 MHz. In order to supply the output side of the gate driver, an isolated dc-dc converter, Traco Power model TMA0515S, was used, providing gate-emitter/gate-source voltages of 15 V and 0 V to turn-on and turn-off, respectively, the devices. The gate, emitter (or source) and gate-emitter (or gate-source) resistors are also visible, as well as the zener diodes and the measuring shunt resistors, the latter being placed vertically.

III. EXPERIMENTAL RESULTS

This section presents the obtained experimental results of the parallel association of lower rated IGBTs and MOSFETs and a comparison with a single higher rated device. For this purpose, a set of five parallel power semiconductors was employed, with a total current rating similar to one single power semiconductor. The switching times are analyzed for the two cases and, for the parallel association, the current sharing is evaluated in order to attest the suitability of this approach under several conditions. Table I shows the parameters of the two resistive-inductive loads used (#1 and #2). In addition, a preliminary test with different values of gate resistance was performed in order to select a proper tradeoff between switching times and voltage/current oscillation.

A. IGBTs

This section presents the IGBTs used for the analysis, as well as the respective obtained results. Table II shows the main parameters of the selected IGBTs for the analysis carried out, namely the maximum collector-emitter voltage (V_{CE}), the



(a) (b) (c)

Fig. 4. Experimental results obtained with the single higher rated IGBT: Gate-emitter (v_{GE}) and collector-emitter (v_{CE}) voltages during (a) turn-on and (b) turn-off; (c) collector current for a peak current of 12 A and a switching frequency of 20 kHz.

maximum collector current (I_C) and the maximum power dissipation (P_D) for an operating case temperature of 25 ºC, the junction-case thermal resistance ($R_{th(jc)}$), the input capacitance (C_{ies}) and the reverse transfer capacitance (C_{res}). The first column lists the single higher rated IGBT (IXYS model IXXR110N65B4H1 in a TO-247 package), while the second column lists one of the lower rated IGBTs for the paralleling (Infineon model IKP15N65H5 in a TO-220 package). In order to establish a comparison between the single higher rated IGBT and the five lower rated IGBTs connected in parallel, a third column lists the resulting parameters of the five IGBTs connected in parallel. It can be seen that these parameters are similar to those of the single higher rated IGBT, as intended for the comparison.

TABLE II. PARAMETERS OF THE IMPLEMENTED IGBTS

IGBT	IXXR110N65B4H1	IKP15N65H5	5 x IKP15N65H5
V_{CE}	650 V	650 V	650 V
I_C @25 º	165 A	30 A	150 A
P_D @25 º	455 W	105 W	525 W
$R_{th(jc)}$	0.33 ºC/W	1.4 ºC/W	0.28 ºC/W
C_{ies}	5500 pF	930 pF	4650 pF
C_{res}	80 pF	4 pF	20 pF

1) Single Semiconductor

This section depicts the results obtained for the single higher rated IGBT (IXXR110N65B4H1). Fig. 4 (a) shows the switching behavior of this IGBT during turn-on with a 3 Ω gate resistor, where the gate-emitter (v_{GE}) and the collector-emitter (v_{CE}) voltages can be seen. The oscillation is significant in the latter, which can be a consequence of the low value for the gate resistance. This voltage only gets stable after roughly 400 ns. Regarding the voltage v_{GE}, it takes around 150 ns to reach the constant value of 15 V, presenting a slight overshoot. The turn-off situation is depicted in Fig. 4 (b), where no oscillation can be seen in the voltage v_{CE}. However, the voltage v_{GE} presents a significant overshoot when v_{CE} reaches its peak, reaching the value of -10 V before stabilizing in 0 V after approximately 500 ns. The voltage v_{CE} takes circa 200 ns to stabilize.

Fig. 4 (c) shows the collector current (i_C) for this IGBT with a collector-emitter voltage of 60 V, operating at 20 kHz and using load #2, resulting in a 12 A peak current. During the turn-on transition, it can be seen that the IGBT takes around 4 µs to reach 10 A and more 4 µs to reach 12 A. Regarding the turn-off transition, it takes 4 µs for the current to decrease from 12 A to 1 A and more 4 µs to be completely extinguished.

2) Parallel Semiconductors

This section shows the results obtained for the five IGBTs associated in parallel for the same operating conditions of the previous results. Fig. 5 (a) depicts the turn-on of the five lower rated parallel connected IGBTs, each one with a total gate resistor of 3 Ω (2 Ω in the gate and 1 Ω in the emitter). Once again, the figure shows the voltages v_{GE} and v_{CE} and, in this case, the oscillation in v_{CE} is inexistent, stabilizing in just 6.7 ns. The voltage v_{GE} takes approximately 80 ns to reach 15 V and, once again, has a slight overshoot. Fig. 5 (b) shows the turn-off of the five parallel IGBTs, where v_{GE} reaches a value no less than -2 V and takes around 150 ns to stabilize in 0 V. The voltage v_{CE} takes around 100 ns to fully stabilize.

As aforementioned, the current sharing must be analyzed in order to assure a proper operation of the paralleled devices. Fig. 5 (c) shows the individual collector currents of four of the five paralleled IGBTs for a collector-emitter voltage of 60 V with load #1, resulting in a 7 A peak current. In this case, the IGBTs are switched at 50 kHz. It can be seen that the devices present a current unbalance of less than 0.5 A. Besides, in comparison to the single higher rated IGBT, the current rise and fall times are significantly lower, as expected. Fig. 5 (d) shows a similar result but with load #2, resulting in a 12 A peak current. It can be seen that the current unbalance is less noticeable due to the increased current, which is a desired characteristic, since the current balancing is more critical for higher currents. Fig. 5 (e) shows the results obtained with the same conditions of the previous result except for the switching frequency, which in this case was doubled (100 kHz) in order to attest the current sharing for higher power losses. It can be seen that the current unbalance is practically the same as the previous result (circa 0.5 A), despite the increased oscillation in the switching instants.

After increasing the load current and the switching frequency, the temperature in the surroundings of the prototype was increased through an electric air blower in order to test the switching behavior for higher operating temperatures. Additionally, the switching frequency was increased again. Fig. 5 (f) shows the obtained result for the severest conditions used in the present study, namely using a load current of 12 A, a switching frequency increased to 200 kHz and a surrounding temperature increased to 67 ºC. The increase in the oscillation is significant, but the current sharing remains approximately the same, with a maximum difference of 0.8 A. Complementarily to this result, Fig. 6 shows a thermal image of the prototype. It can be seen that the IGBTs are not the hottest devices registered in the figure, whereby the good performance of the parallel association can be validated.

B. MOSFETs

This section presents the MOSFETs used for the analysis, as well as the respective obtained results. Table III shows the

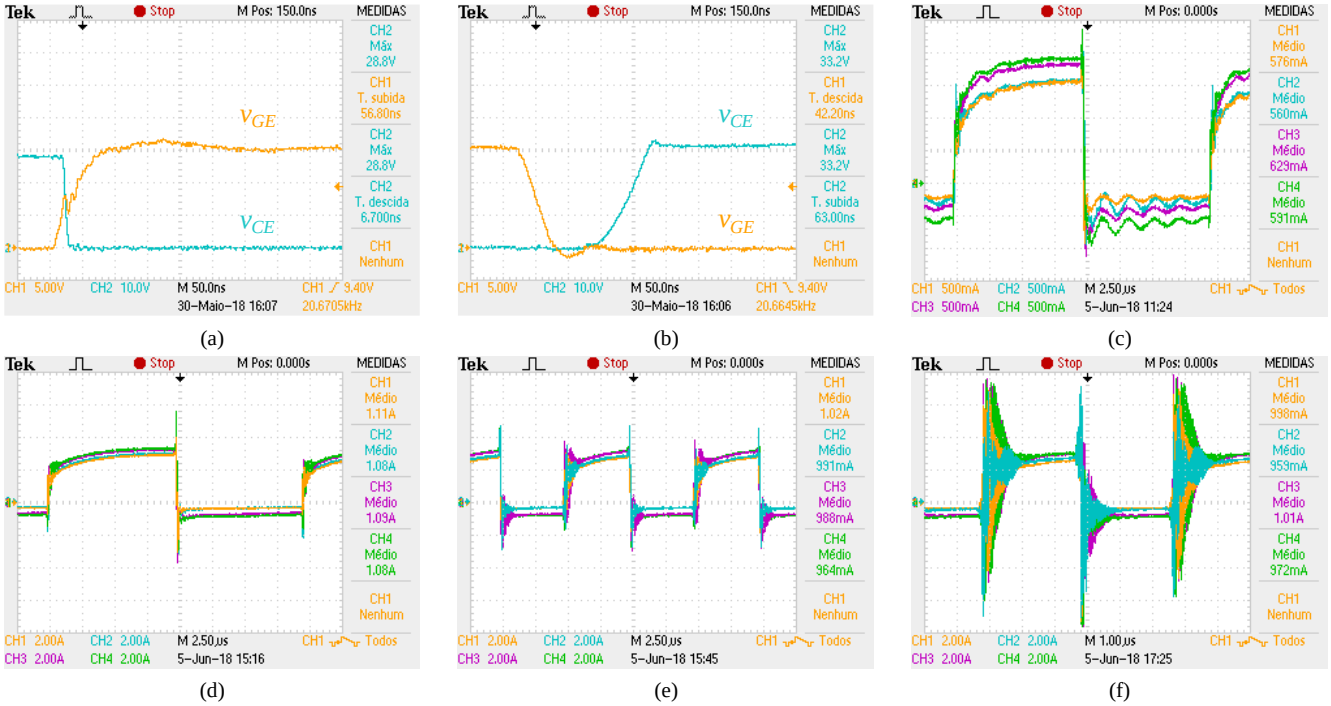


Fig. 5. Experimental results obtained with the five lower rated IGBTs connected in parallel: Gate-emitter (v_{GE}) and collector-emitter (v_{CE}) voltages during (a) turn-on and (b) turn-off; collector currents of four of the five IGBTs for a load peak current and a switching frequency, respectively, of (c) 7 A, 50 kHz; (d) 12 A, 50 kHz; (e) 12 A, 100 kHz; (f) 12 A, 200 kHz and a surrounding temperature increased to 67 ºC.

main parameters of the selected MOSFETs for the analysis carried out, namely the maximum drain-source voltage (V_{DS}), the maximum drain current (I_D) and the maximum power dissipation (P_D) for an operating case temperature of 25 ºC, the junction-case thermal resistance ($R_{th(jc)}$), the input capacitance (C_{ies}) and the reverse transfer capacitance (C_{res}). The first column lists the single higher rated MOSFET (International Rectifier model IRFP90N20D in a TO-247 package), while the second column lists one of the lower rated MOSFETs to be connected in parallel (Fairchild model FDP18N20F in a TO-220 package). Additionally, a third column lists the resulting parameters of the five MOSFETs connected in parallel, where these parameters are similar to those of the single higher rated MOSFET.

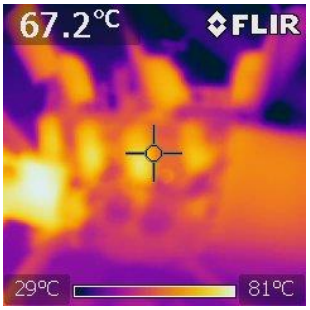


Fig. 6. Thermal image of the five lower rated IGBTs connected in parallel for a load peak current of 12 A with a switching frequency of 200 kHz and with a surrounding temperature of 67 ºC.

TABLE III. PARAMETERS OF THE IMPLEMENTED MOSFETS.

MOSFET	IRFP90N20D	FDP18N20F	5 x FDP18N20F
V_{DS}	200 V	200 V	200 V
I_D @25 º	94 A	18 A	90 A
P_D @25 º	580 W	100 W	500 W
$R_{th(jc)}$	0.26 ºC/W	1.2 ºC/W	0.24 ºC/W
C_{iss}	6040 pF	885 pF	4425 pF
C_{res}	170 pF	24 pF	120 pF

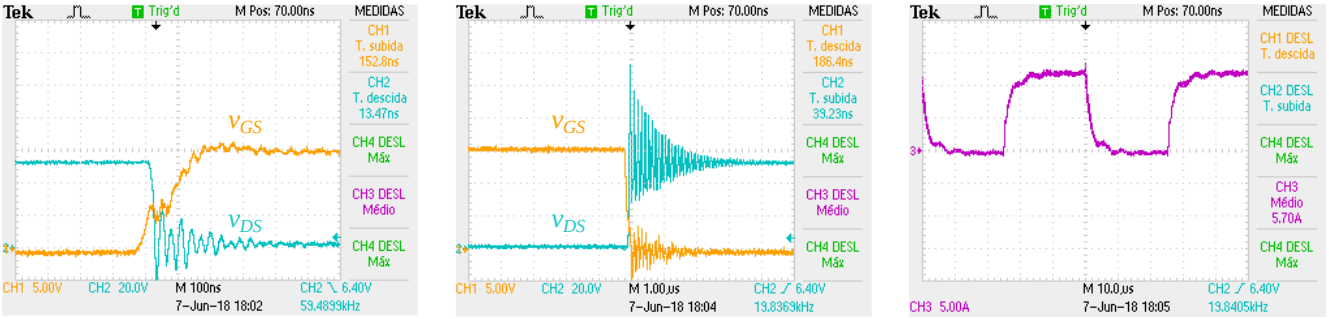
1) Single Semiconductor

This section depicts the results obtained for the single higher rated MOSFET (IRFP90N20D). Fig. 7 (a) shows the switching behavior of this MOSFET during turn-on with a 5.6 Ω gate resistor, where the gate-source (v_{GS}) and the drain-source (v_{DS}) voltages can be seen. The oscillation is even higher for this case than what it was for the IGBTs, even with a higher value of gate resistance. The voltage v_{DS} only gets stable after roughly less than 400 ns. Regarding the voltage v_{GS}, it takes almost 200 ns to stabilize. Fig. 7 (b) shows the turn-off behavior of this MOSFET, where the oscillation is even more severe, i.e., v_{DS} presents an overshoot of 100% that gets stabilized only after nearly 3.5 µs. The voltage v_{GS} reaches the value of -5 V and stabilizes after circa 2 µs.

Fig. 7 (c) shows the drain current (i_D) for this MOSFET with a drain-source voltage of 60 V and with load #2, resulting in a 12 A peak current. This result is very similar to the analogous result obtained for the single higher rated IGBT. During the turn-on transition, it can be seen that the MOSFET takes around 4 µs to reach 10 A and more 4 µs to reach 12 A. Regarding the turn-off transition, it takes slightly less than 4 µs for the current to decrease from 12 A to 1 A and more 4 µs to be completely extinguished.

2) Parallel Semiconductors

This section presents the results obtained for the five paralleled MOSFETs for the same operating conditions of the previous results. The oscillation is considerably reduced when compared to the single higher rated MOSFET, but not as much as verified for the IGBTs. Fig. 8 (a) depicts the turn-on of the five lower rated parallel connected MOSFETs, each one with a total gate resistor of 5.6 Ω (4.3 Ω in the gate and 1.3 Ω in the emitter). Once again, the figure shows the voltages v_{GS} and v_{DS}, where it can be seen that both voltages oscillate during nearly 200 ns. Fig. 8 (b) shows the turn-off of the five parallel MOSFETs, where the voltage v_{DS} takes around 70 ns to reach its peak and v_{GS} stabilizes in approximately 100 ns.



(a) (b) (c)

Fig. 7. Experimental results obtained with the single higher rated MOSFET: Gate-source (v_{GS}) and drain-source (v_{DS}) voltages during (a) turn-on and (b) turn-off; (c) Drain current for a peak current of 12 A and a switching frequency of 20 kHz.

As performed with the IGBTs, the current sharing was analyzed. Fig. 8 (c) shows the individual drain currents of four of the five paralleled MOSFETs for a drain-source voltage of 60 V with load #1, resulting in a 7 A peak current. In this case, the MOSFETs are switched at 50 kHz. It can be seen that the devices present a current unbalance of less than 0.5 A. Besides, in comparison to the single higher rated MOSFET, the current rise and fall times are significantly lower, as expected and verified with the IGBTs. Fig. 8 (d) shows a similar result but with load #2, resulting in a 12 A peak current. Contrarily to what was verified with the IGBTs, the current unbalance increased with the total current, with the maximum difference being almost 1 A. Fig. 8 (e) shows the results obtained with the switching frequency increased to 100 kHz, where it can be seen that a severe oscillation appeared. On the other hand, the current unbalance decreased to approximately 0.5 A, which is practically the same as verified with the IGBTs. Thus, despite the strong oscillation in the switching instants, the current sharing became more even with the temperature rise, which is convenient for the paralleling of power semiconductors. However, due to the magnitude of the oscillation registered in this result, further tests were not performed, i.e., increasing the switching frequency and the surrounding temperature.

IV. Dynamic Performance and Cost Comparison

This section presents a discussion of the obtained results, focusing on the comparison, for the IGBTs and MOSFETs, of the single higher rated device with the five lower rated devices connected in parallel. The comparison is based on the switching times and the cost, as it can be seen in Table IV for the IGBTs and in Table V for the MOSFETs. The switching times were measured with the gate resistor values previously referred in this paper, i.e., 3 Ω for the IGBTs and 5.6 Ω for the MOSFETs. It should be noted that the cost values used in this paper were gathered from an electronics components retailer in July 2018 for small quantities.

Table IV. Dynamic Performance and Cost Comparison of the Implemented IGBTs.

IGBT	IXXR110N65B4H1	IKP15N65H5	5 x IKP15N65H5
t_{on}	59 ns	24 ns	46 ns
t_{off}	140 ns	21 ns	34 ns
Cost	7 €	2.32 €	11.6 €

Table V. Dynamic Performance and Cost Comparison of the Implemented MOSFETs.

MOSFET	IRFP90N20D	FDP18N20F	5 x FDP18N20F
t_{on}	122 ns	21 ns	6 ns
t_{off}	149 ns	20 ns	26 ns
Cost	4.86 €	1.27 €	6.35 €

As it can be seen for both cases, the parallel association of the five lower rated devices provides shorter turn-on (t_{on}) and turn-off (t_{off}) times, therefore reducing the switching losses and allowing the use of higher switching frequencies. On the other hand, the parallel association did not bring economical savings in the studied cases; however, for higher power levels, the benefits of the parallel association include not only the dynamic performance but also the economical point of view. In order to support this idea, Table VI and Table VII were assembled, where a cost comparison was performed for higher rated IGBTs and MOSFETs, respectively. For these cases, the economical factor favors the parallel association of lower rated devices, especially for the IGBTs case, where the single higher rated device costs more than twice the set of five lower rated devices. Taking into consideration that the cost values correspond to small quantities of the products, the parallel association is even more pertinent, since the unitary costs are lower for larger quantities.

Table VI. Cost Comparison of Higher Rated IGBTs.

IGBT	VS-GT175DA120U	IRG4PH50SPBF	5 x IRG4PH50SPBF
V_{CE}	1200 V	1200 V	1200 V
I_C @25 °	288 A	57 A	285 A
Cost	75.36 €	6.09 €	30.45 €

Table VII. Cost Comparison of Higher Rated MOSFETs.

MOSFET	IXFB132N50P3	SiHP25N50E	5 x SiHP25N50E
V_{DS}	500 V	500 V	500 V
I_D @25 °	132 A	26 A	130 A
Cost	14.26€	2.65 €	13.25 €

V. Conclusions

This paper presented a study on the parallel association of power semiconductors, namely insulated gate bipolar transistors (IGBTs) and metal oxide semiconductor field effect transistors (MOSFETs). The aim of this study was to prove that the implementation of lower rated devices connected in parallel can be advantageous over the utilization of a single higher rated device, both in terms of dynamic performance and cost. The experimental results showed that the current sharing among a set of five parallel devices was ensured for different operating conditions. It was also verified that the implementation of lower rated devices connected in parallel is advantageous over the use of a single higher rated device in terms of dynamic performance, offering shorter switching times, which in turn reduces the switching losses. For the devices used in this study, an economical gain was not verified; however, another example, for higher power levels, was presented, in which the cost benefits are substantial. Thus, it can be concluded that the parallel

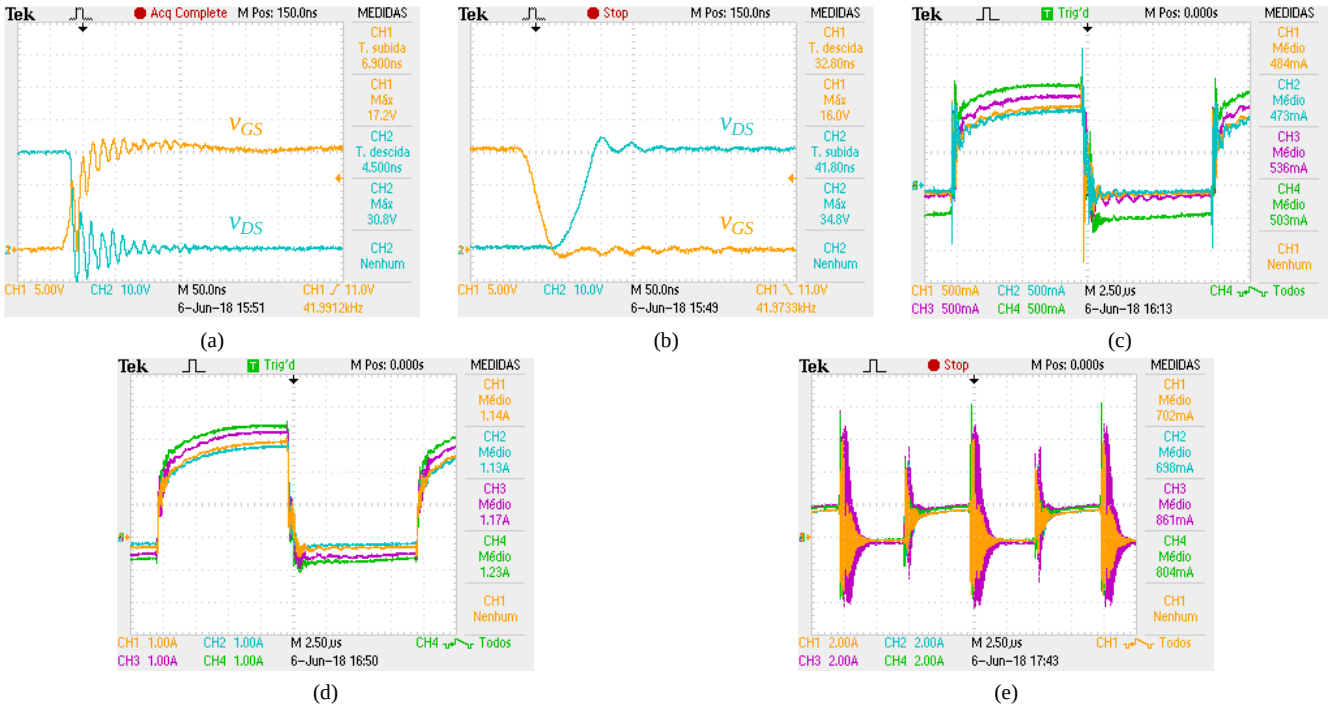


Fig. 8. Experimental results obtained with the five lower rated MOSFETs connected in parallel: Gate-source (v_{GS}) and drain-source (v_{DS}) voltages during (a) turn-on and (b) turn-off; drain currents of four of the five MOSFETs for a load peak current and a switching frequency, respectively, of (c) 7 A, 50 kHz; (d) 12 A, 50 kHz; (e) 12 A, 100 kHz.

association of power semiconductors is advantageous in terms of dynamic performance for a wide range of power levels, and, above a certain power level, it is additionally advantageous in terms of cost.

ACKNOWLEDGMENTS

This work has been supported by FCT – Fundação para a Ciência e Tecnologia within the Project Scope: UID/CEC/00319/2019. This work has been supported by FCT within the Project Scope DAIPESEV – Development of Advanced Integrated Power Electronic Systems for Electric Vehicles: PTDC/EEI-EEE/30382/2017. Mr. Tiago Sousa is supported by the doctoral scholarship SFRH/BD/134353/2017 granted by the Portuguese FCT agency.

REFERENCES

[1] D. Medaule, "Parallel operation of high power IGBTs," in *IEE Colloquium on `IGBT Propulsion Drives'*, 1995, no. 2, pp. 2–2.

[2] Hua Yang, Wen Xuhui, Gu Lingyun, Wang Li, and Zhao Feng, "Investigation of parallel connection of IGBTs," in *2005 International Conference on Electrical Machines and Systems*, 2005, p. 833–835.

[3] Wen Huiqin, Liu Jun, Zhang Xuhui, and Wen Xuhui, "Design of high power electronic building block based on parallel of IGBTs for electric vehicle," in *2008 13th International Power Electronics and Motion Control Conference*, 2008, pp. 1518–1522.

[4] J. Bohmer, J. Schumann, K. Fleisch, and H.-G. Eckel, "Current mismatch during switching due to the self-turn-off effect in paralleled IGBT," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–9.

[5] Chen Huawei, Liu Jun, Zhang Jian, and Wang Youlong, "Investigation of parallel connection of 1700V IGBTs in 400kW inverter," in *2014 IEEE Conference and Expo Transportation Electrification Asia-Pacific (ITEC Asia-Pacific)*, 2014, vol. 2, pp. 1–4.

[6] N. Chen, F. Chimento, M. Nawaz, and L. Wang, "Dynamic Characterization of Parallel-Connected High-Power IGBT Modules," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 539–546, Jan. 2015.

[7] Y. Chen, F. Zhuo, W. Pan, F. Zhang, and L. Feng, "A novel active gate driver for static and dynamic current balancing of parallel-connected IGBTs," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 795–799.

[8] G. Wang, J. Mookken, J. Rice, and M. Schupbach, "Dynamic and static behavior of packaged silicon carbide MOSFETs in paralleled applications," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 1478–1483.

[9] H. Li *et al.*, "Influences of Device and Circuit Mismatches on Paralleling Silicon Carbide MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 621–634, Jan. 2016.

[10] Y. Mao, Z. Miao, C.-M. Wang, and K. D. T. Ngo, "Balancing of Peak Currents Between Paralleled SiC MOSFETs by Drive-Source Resistors and Coupled Power-Source Inductors," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8334–8343, Oct. 2017.

[11] A. Hussein, B. Mouawad, and A. Castellazzi, "Dynamic performance analysis of a 3.3 kV SiC MOSFET half-bridge module with parallel chips and body-diode freewheeling," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2018, vol. 2018–May, pp. 463–466.

[12] J. Muting, N. Schneider, T. Ziemann, R. Stark, and U. Grossner, "Exploring the behavior of parallel connected SiC power MOSFETs influenced by performance spread in circuit simulations," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, vol. 2018–March, pp. 280–286.

[13] Infineon Technologies, "Design reference on IGBT paralleling," *Application Note AP99007*, pp. 1–19, 2008.

[14] ON Semiconductor, "Paralleling of IGBTs," *Application Note AND9100/D*, no. 1, pp. 1–7, 2014.

[15] Semikron, "IGBT Modules in Parallel Operation with Central and Individual Driver Board," *Application Note AN 17-001*, 2017.

[16] Texas Instruments, "IGBT Gate Driver Reference Design for Parallel IGBTs With Short-Circuit Protection and External BJT Buffer," *Application Note TIDUC70A*, no. December 2016, pp. 1–33, 2017.

[17] P.-O. Jeannin, J.-L. Schanen, and E. Clavel, "Original cabling conditions to insure balanced current during switching transitions between paralleled semiconductors," *IEEE Trans. Ind. Appl.*, vol. 38, no. 1, pp. 181–188, 2002.