Proceedings of the 8th European Microwave Integrated Circuits Conference

Harmonic-injection divider based on feedback through a nonlinear transmission line

Franco Ramírez
Dpto. Ingeniería de Comunicaciones
Universidad de Cantabria
Spain
ramirezf@unican.es

Almudena Suárez
Dpto. Ingeniería de Comunicaciones
Universidad de Cantabria
Spain
suareza@unican.es

***Abstract*—An application of nonlinear transmission lines (NLTLs) to the design of harmonic-injection frequency dividers by high division order is presented. The NLTL, composed by inductance-varactor cells, is used as a feedback block of an active-device circuit, which gives rise to a free-running oscillation. Due to its highly nonlinear behavior, the NLTL can be optimized to enhance the harmonic components required for high order division through mixing with the input signal. The frequency bandwidth is further increased through a combination of phase-locking and frequency-locking effects. This is done extracting an error baseband signal from the active-device output, which, after suitable amplification, is applied to the varactor diodes of the NLTL. A design procedure is also presented to enable the switching of the division order between N and N-1 through control of the bias voltage. The novel configuration can have the advantage of a low complexity, low dc power consumption, and scalability. The new concept has been applied for the design a dual-order frequency divider by 10 and 9 with about 2% bandwidth.**

Keywords—Frequency divider, nonlinear transmission line, injection-locking phase-locking

I. Introduction

Nonlinear transmission lines (NLTL), usually composed by a high number of inductance-varactor cells [1–2], can be used for harmonic generation, based on soliton-like propagation [3]. Solitons are pulsed waveforms that propagate along the line without distortion due to the combined effect of the dispersion inherent to the lumped-element line and the nonlinear capacitances C(v) [3], the latter giving rise to a shorter propagation delay for higher voltage amplitude. The effect of losses increases with the number of inductor-varactor cells, so it is convenient to limit the number of stages, often below 10 to 15 [3], this requiring sufficient amplitude of the excitation signal. Although most of the pulse-shaping circuits are based on the use of an independent source, exciting the NLTL, the works [4–6] demonstrate the possibility to design a self-sustained pulsed-waveform generator. Two main topologies have been proposed: pulsed-waveform oscillators with the NLTL in a feedback configuration [4–6] and reflection soliton oscillators [5]. The goal of all these previous works has been to achieve an output signal consisting of a narrow periodic pulsed waveform. Here a different application of the NLTL plus active device configuration is devised. In similar manner to the works [5–6], the NLTL is used as a feedback loop of the active device to enable the self-sustained oscillation. However, unlike these previous works, the aim is not to obtain a pulsed output signal, but to take advantage of the harmonic generation capability of the NLTL to implement a feedback frequency multiplier. Assuming that the output fundamental frequency is f_o, the mixing of the feedback signal at $(N–1)f_o$ with the input signal at $f_{in} = Nf_o$ should increase the sensitivity [7] to the input signal and, thus, facilitate the frequency harmonic-injection division by high order N. The mixing is carried out in the device(s) used to generate the self-sustained oscillation. This new configuration can enable design flexibility and scalability and low dc-power consumption. Additionally, the operation bandwidth can be increased combining the effects of harmonic injection locking and phase locking [8]. Advantage is taken of the dc bias input of the varactor diodes of the NLTL to introduce a baseband error signal extracted from the transistor output with a lowpass filter and amplified along the low-frequency loop. A design procedure enabling the switching between division orders N and N–1 will also be presented. To the best of our knowledge, it is the first time that the use of an NLTL as feedback element of high-order harmonic-injection dividers is proposed. The concept will be illustrated through the implementation of a divider by 9 and 10, based on the use of the transistor ATF33143 and varactor diodes SMV1247.

II. Optimization of the NLTL for Frequency Division by N=10

In the analog divider by N based on the NLTL, the aim is to achieve injection locking through the mixing of the input signal with the NLTL output. Due to the high harmonic generation capability of the NLTL, the mixing will generate various intermodulation terms, including the oscillation frequency f_o, which will injection-lock the oscillator circuit. In particular, the mixing of the input signal at f_{in} with the feedback signal at $(N–1)f_o$ will give rise to a lower intermodulation product in the order of the oscillation frequency. In the design carried out here, the drain-current nonlinearity of the PHEMT transistor should mix the input and feedback signals entering the gate port. With this aim, the transistor must be biased near pinchoff and still be able to sustain the oscillation at f_o. Unlike previous works, the NLTL, excited by the oscillator output signal, is used internally to achieve frequency multiplication by the high order N–1 (Fig. 1). This function will require a suitable choice of the NLTL components, inductor and varactor diodes, taking into account the desired input frequency $f_{in} = 7.25$ GHz. The NLTL Bragg frequency $f_B = 1/(\pi\sqrt{LC_{eff}})$ [1–2] with C_{eff} the average capacitance and L the line inductor, should be higher than the maximum desired harmonic term [3]. On the other hand, the line characteristic impedance $Z_c = \sqrt{L/C_{eff}}$ should be suitably chosen not to degrade the matching of the input signal. Considering both f_B and Z_c, the chosen varactor diode is the SMV1247 and the initial value of the line inductor is L = 2 nH, providing $Z_c \cong 145$ Ohm.

In order to determine the NLTL input amplitude required for a proper frequency multiplication, in a first stage, the line is simulated separately from the overall oscillator structure. The line is excited with a periodic generator at $f_o = 0.75$ GHz, expected to correspond approximately with the centre of the output division band. The line termination impedance is also relevant and, as shown in previous works [9], inductive terminations enhance the pulse-forming capabilities of relatively short transmission lines. In fact, different numbers of L–varactor cells have been tested here, obtaining optimum behaviour for n = 9 cells. With the analysis of the NLTL isolated form the complete oscillator circuit, it has been found that an input amplitude A = 2 V provides sufficient voltage amplitude at the output harmonic components N–1 = 9 and N+1 = 11. The line terminated in a parallel inductor enhances the harmonic generation and should also be convenient for input matching.

In the full oscillator configuration, with the NLTL acting as a feedback loop, the amplitude at the fundamental frequency f_o required at the transistor output should agree with A = 2 V. This amplitude is fixed with the aid of an auxiliary generator (AG), playing the role of the oscillation [10]. The voltage AG must fulfill a non-perturbation condition given by the zero value of the ratio between the current through this generator and the voltage delivered $Y_{AG} = 0$ [10]. This condition is solved through optimization. The AG frequency is set constant to the desired free-running oscillation frequency (agreeing with the center of the division band). Then the circuit elements are optimized in order two fulfil two goals, $Y_{AG} = 0$ and a maximum value of the magnitude of harmonic voltage V_9 at the NLTL output. Note that, once the NLTL is inserted into the circuit, the operation conditions are different from those of the isolated NLTL, due to loading effects. To maximize the amplitude V_9, the minimum allowed value of this amplitude is gradually increased with an optimization goal added to the non-perturbation condition $Y_{AG} = 0$. To achieve the mixed goals, both the NLTL inductor L and the circuit input network are optimized. The great harmonic-generation capability of the line and the parallel feedback enable an undemanding convergence process. Fig. 2(a) shows the spectrum at the output of the NLTL in the free-running oscillator circuit before and after the procedure for maximization of the harmonic (N–1)f_o. In both cases, the circuit fulfils the steady-state oscillation condition at $f_{AG} = f_o$ for a voltage amplitude at the input of the NLTL given by A = 2V (at f_o). The final spectrum can be compared with the measured one, presented in Fig. 2(b).

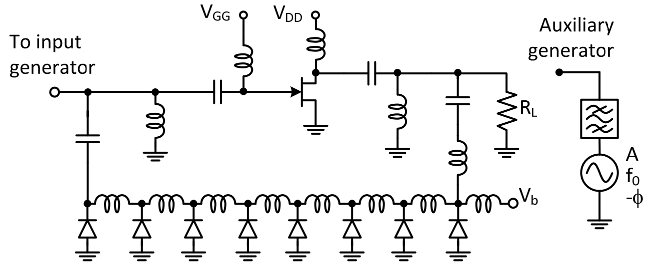


Fig.1 Schematic of the new frequency divider using an NLTL to implement a feedback frequency multiplier. The auxiliary generator represented separately from the circuit is connected to the output node only for design purposes. The fabricated circuit used an ATF33143 transistor and SMV1247 varactor diodes on RO4003C substrate.

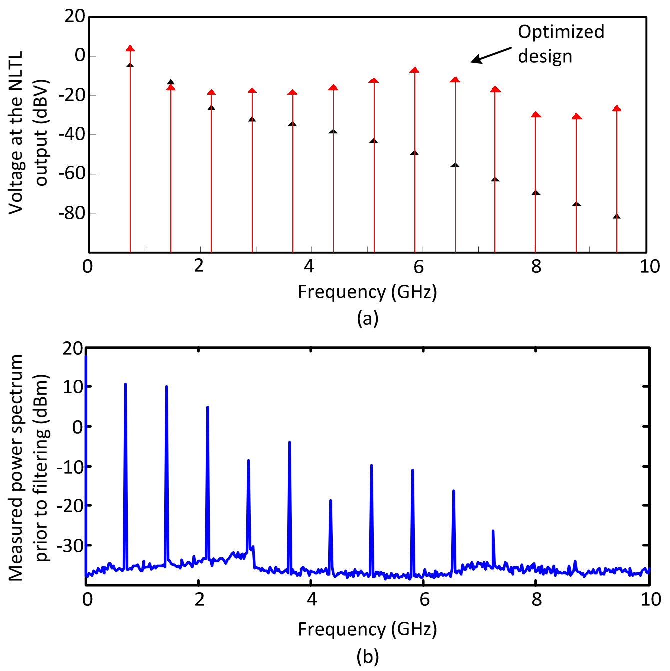


Fig. 2 Optimization of the free-running oscillator with device output voltage A = 2V. (a) Enhancement of the voltage amplitude of the harmonic component (N–1) = 9f_o at the NLTL output. (b) Measured spectrum before output filtering.

The frequency division band is analysed with the same AG used for the oscillator design. Because it is a divider by N = 10, the input frequency should be N times the oscillation frequency, that is $f_{in} = Nf_{AG}$. Due to the synchronized behaviour there must be a phase relationship between the oscillation and the input source. The AG phase is arbitrarily set to zero (system phase origin) and the input source phase ϕ is swept between zero and 2π [10], solving for the AG amplitude and frequency at each phase step. The constant input power considered is $P_{in} = 10$ dBm. For the varactor bias voltage $V_b = 1.5$ V, the described analysis provides the first closed curve shown in Fig. 3. The synchronization bandwidth is about 2% of the central frequency, which is in the order of previous works with division order 4 and 5 [7]. In this proof-of-concept prototype, insufficient effort has been devoted to input matching and we believe that a broader bandwidth could have been obtained with a more accurate matching network. For other varactor bias voltages, the closed synchronization curve shifts in frequency as shown in the same figure. It is to be noted that the output division bandwidth by $N = 10$ obtained replacing the NLTL with an ordinary linear distributed transmission line (providing approximately the same delay) turns out to be negligible, since there is no frequency multiplication. In comparison with the use of a multiplier based on transistor devices, this topology has the advantage of design simplicity and low power consumption. Furthermore, the low number of L-varactor cells enables a small circuit size.

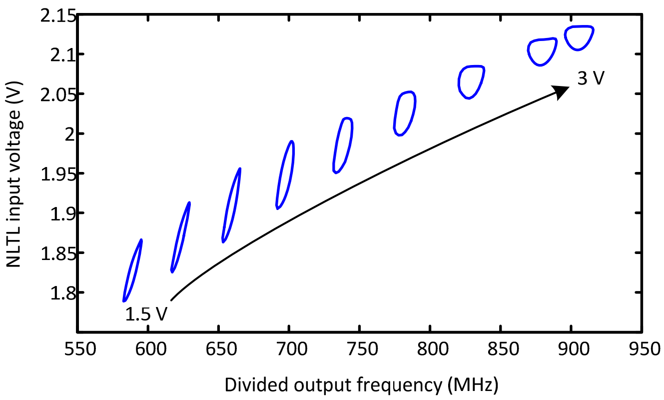


Fig. 3 Division bandwidth by $N = 10$. Closed synchronization curves providing the division bandwidth for different values of the NLTL varactor-bias voltage.

III. COMBINATION OF HARMONIC-INJECTION AND PHASE-LOCKING

The capability to shift the frequency division band by changing the bias voltage of the varactor diode (Fig. 3) suggests the possibility to combine harmonic injection and phase locking [8] in order to increase the frequency division band. This is based on the use of a low-frequency control signal to change the circuit self-oscillation frequency. The transistor nonlinear transconductance $i_{DS}(v_{GS})$ gives rise to the low-frequency error signal $v_D(t)$ at the intermodulation term $|f_{in} - Nf_o|$ [11]. This signal is extracted through a choke and amplified in the feedback loop, as in [11]. The differential amplifier compares the low frequency-signal extracted from the transistor drain terminal with a dc reference voltage. Here the amplifier output is connected to the cathode of the varactor diodes (V_b in Fig. 1) and this modifies the self-oscillation frequency so as to decrease the frequency error, as in a phase-locked oscillator [8]. The enlargement of the synchronization bandwidth depends on the voltage gain G_a of the low-frequency amplifier. Assuming synchronized behavior, when the input frequency changes, the effect low-frequency loop can be modeled as a shift of the free-running oscillation frequency, $f_o(\phi)$, depending on the phase shift between this oscillation and the input signal [8]. To illustrate, assuming low input amplitude E_{in} at f_{in}, the current-to-voltage ratio Y_s at the divided frequency can be linearized about the free-running solution (V_o, $f_o(\phi)$, E_{in}=0) at the same node [11]:

$$\frac{\partial Y_o}{\partial V_o}(V_s - V_o) + \frac{\partial Y_o}{\partial f_o}\left(\frac{f_{in}}{N} - f_o(\phi)\right) = -\frac{\partial Y_o}{\partial E_{inr}} E_{in}\cos\phi - \frac{\partial Y_o}{\partial E_{ini}} E_{in}\sin\phi \qquad (1)$$

where V_s is the voltage amplitude in synchronized operation. The double dependence on the phase shift ϕ is due to the combined effect of phase-locking (changing the oscillation frequency so as to reduce the frequency difference) and injection locking. Due to this double action, one should expect an increase of the operation bandwidth. This is evidenced in Fig. 4, where the bandwidth before and after the introduction of the low-frequency feedback loop is compared. Using this feedback loop, the input power requirement is P_{in} = -10 dBm. Measured results (with the low-frequency loop) are also presented. Without this loop, the measured bandwidth decreases to about 3 MHz. Deviations from the simulated results are believed to be mostly due to inaccuracies in the transistor modeling.

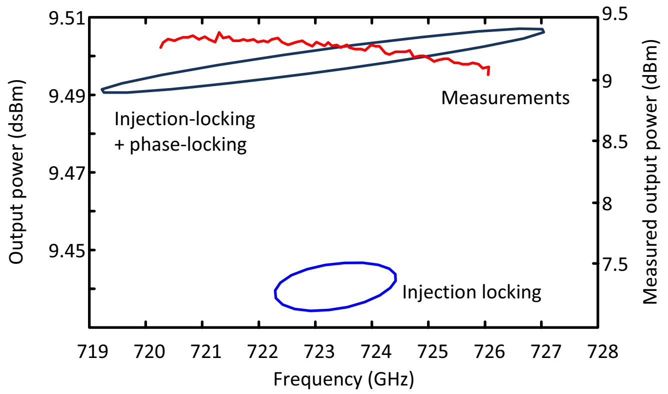


Fig. 4 Combined action of injection and phase locking for $P_{in} = -10$ dBm. The division bandwidths with and without the low-frequency feedback loop are compared. Measurements with the low-frequency loop are superimposed.

IV. DIVISION-ORDER SWITCHING

An interesting function would be the capability to switch the division order between N and N-1, while keeping constant the input frequency. This will be done through a change of the varactor bias voltage. The analysis of this possible application requires fixing the input frequency and obtaining the division bandwidths by 10 and 9 versus the varactor-bias voltage. The input-generator frequency is set constant to the desired center value of the operation bandwidth $f_{in} = N \cdot f_o = 10 f_o$ and the input power is set constant to $P_{in} = 0$ dBm. Then, the input source phase is swept, calculating the AG amplitude and varactor bias voltage at each phase step, which is done for the two division orders $N = 9$ and $N = 10$, at the same input frequency value. This means that in the former case the input source is at the 9^{th}

harmonic component of the AG frequency, whereas in the second case it is at the 10th harmonic component of AG frequency. The results are shown in Fig. 5. With the same divider topology, it is possible to switch between the two division orders by simply changing the varactor bias voltage V_b. Next, the two varactor-bias voltages were judiciously chosen (with the aid of this synchronization analysis) so as to have the same total frequency bandwidth when dividing by N = 9 and N = 10. The results are shown in Fig. 6(a). For validation, the spectra at constant input frequency f_{in}=7.25 GHz, calculated with a time-domain analysis, for the two division orders, are shown in Fig. 6(b).

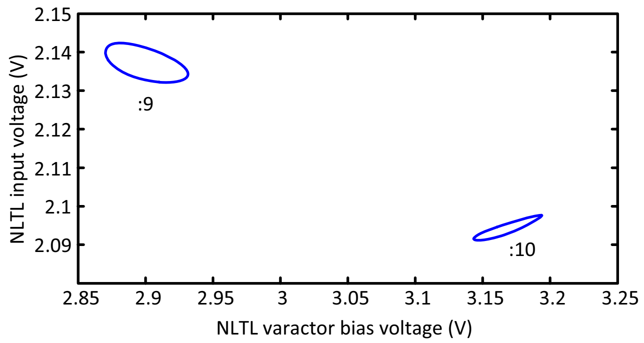
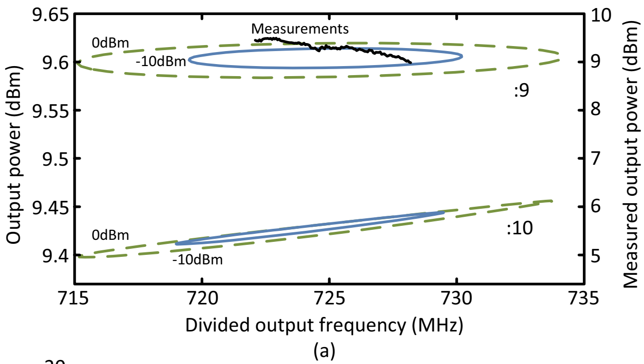


Fig. 5 Synchronization analysis versus the varactor-bias voltage with constant input frequency f_{in} = 7.25 GHz The closed synchronization curves corresponding to division by N = 9 and N = 10 are presented.



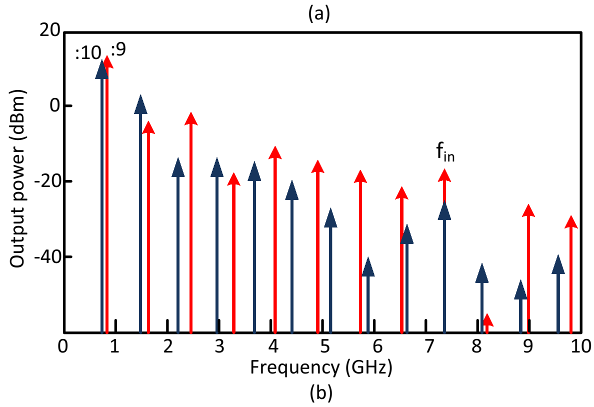


Fig. 6 Frequency bandwidth when dividing by N = 9 and N = 10. The change in the division order is obtained by switching the varactor-bias voltage from V_b = 2.28 V (N = 9) to V_b = 3.16 V (N = 10). (a) Closed synchronization curves showing approximately the same synchronization bandwidth for the two division orders. (b) Spectra at the constant input frequency f_{in} = 7.25 GHz, calculated, for validation, with a time-domain analysis, for the two division orders.

V. Conclusions

A proof of concept of the possible application of nonlinear transmission lines (NLTLs) for the design of harmonic-injection frequency dividers by high division order has been presented. The NLTL is used for harmonic generation in the divider feedback loop, whereas the active device(s) sustains the self-oscillation and provides mixing between the input and feedback signals. A technique is presented to enhance the harmonic generation capabilities of the NLTL at the required harmonic terms once inside the oscillator circuit. For a further increase of the division bandwidth, advantage is taken of the NLTL varactor-bias input to combine the effects of injection locking and phase locking through the introduction of a low-frequency feedback loop. This is done extracting an error baseband signal from the active-device output, which, after suitable amplification, is applied to the varactor diodes of the NLTL. The control of the bias voltage enables a switching between the division orders N and N–1. Although this first divide-by-10 and divide-by-9 prototype is not totally optimized, we believe that this topology can be useful for a low complexity design, with low dc power consumption.

References

[1] E. Afshari, A. Hajimiri, “Nonlinear Transmission Lines for Pulse Shaping in Silicon”, IEEE J. Solid-State Circ., vol. 40, no.3, pp. 744-752 , Mar., 2005.

[2] M. Remoissenet, Waves Called Solitons: Concepts and Experiments, New York: Springer, 1999.

[3] F. Martín, , X. Oriols, J. A. Gil, J. García-García, Optimization of Nonlinear Transmission Lines for Harmonic Generation: The Role of the Capacitance-Voltage Characteristic and the Area Effect, International Journal of Infrared and Millimeter Waves, Vol. 23, Issue 1, pp 95-103, Jan. 2002.

[4] D.S. Ricketts, X.Li, N. Sun, K.Woo,D.Ham, “On the Self-Generation of Electrical solitón Pulses”, IEEE J. Solid-State Circuits, vol. 42, no.8 , pp. 1657-1668 , Aug., 2007.

[5] O. Yildirim, D. Ricketts, D. Ham, “Reflection Soliton Oscillator”, IEEE Trans. Microw. Theory Techn., vol. 57, no.10, pp. 2344-2353, Oct., 2009.

[6] M. Pontón, F. Ramírez, A. Suárez, JP. Pascual, "Applications of Pulsed-Waveform Oscillators in Different Operation Regimes”, IEEE Trans. Microw. Theory Techn., vol.57, no. 12, Dec., 2009.

[7] J. Jinho Jeong, K. Youngwoo Kwon, "V-band high-order harmonic injection-locked frequency-divider MMICs with wide bandwidth and low-power dissipation," IEEE Trans. On. *Microwave Theory and Techniques,* vol.53, no.6, pp. 1891- 1898, June 2005

[8] H. C. Chang, A. P. Yeh, R. A. York, "Analysis of oscillators with external feedback loop for improved locking range and noise reduction", *IEEE Trans. Microwave Theory and Techniques,* vol. 47, no. 8, August 1999, pp. 1535-1543.

[9] M. Pontón, F.Ramírez, A.Suárez, “Design of pulsed waveform oscillators with a short nonlinear transmission line”, IEEE Int. Micro. Symp. Dig., Anaheim, CA, 2010, pp.560-563.

[10] A. Suárez, Analysis and Design of Autonomous Microwave Circuits, Hoboken, New Jersey: Wiley - IEEE Press, 2009.

[11] F. Ramírez, E. de Cos, A. Suárez, “Nonlinear analysis tools for the optimized design of harmonic-injection frequency dividers”, *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 6, Jun. 2003, pp. 1752-1762