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The role of the dc-bus in voltage sags experienced by three-phase adjustable-speed drives

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Abstract. This research work is devoted to the critical evaluation of the role of the dc-bus in the behavior of three-phase adjustable-speed drives with voltage sags. In particular, the dc-link voltage variation under voltage sag and its dependence on bus capacity, dc-link resistance and inductance and source impedance.

The analysis can be used to introduce additional capacitance in the dc-link in order to increase the ride-through capability of the ASD.

Both an electromagnetic transient model and a set-up facility have been introduced. This test platform can be used in order to study the sensitivity of ASD to different disturbances.

Keywords. power quality, sags, PWM drives, ASD

1. Introduction

A voltage sag or dip can be defined as a reduction of the voltage related to the nominal value with a duration that can go from one cycle to some few seconds. It is well known that voltage sags are produced by short circuits, motor starting, maniobres in breakers, electrical welding machines and other loads with sudden and intermittent power demand. The effects of voltage sags on adjustable-speed drives (ASD) has been studied from different points of view [1–10]. In Bollen [3] it is possible to find conclusions about the economic cost of sags in several types of industrial applications. Duran-Gomez et all. [11] proposes a critical evaluation of the effect of voltage sags on ASD's, underlying the dc-link voltage variation under voltage sags and its dependence on source impedance, dc-link inductance and output load. In a complementary way Collins et all. [5] reviews the behavior of ac motor drives during sags. Zyl et all. [12] introduces a methodology for incorporating voltage sag ride-through in the design of ASD's with active rectifiers.

2. Electric Circuit Model

The simplified equivalent electric circuit model of the ASD is shown in fig. 2. The average value of the dc-link under steady state operating conditions is given by Mohan et all. [13],

$$V_{dc,i} = \frac{3\sqrt{2}}{\pi} V_{LL} \tag{1}$$

where,

- $V_{dc,i}$ Steady-state mean value at the output of the rectifier converter.
- V_{LL} rms value of the line-to-line voltage of the utility input supply.

In order to reduce the complexity of the study, only balanced three-phase sags are considered. Fig. 1 shows a typical case A [3] sag. A simple sag can be characterized using the residual voltage $V_{dc,r}$ and the duration t_{sag}.

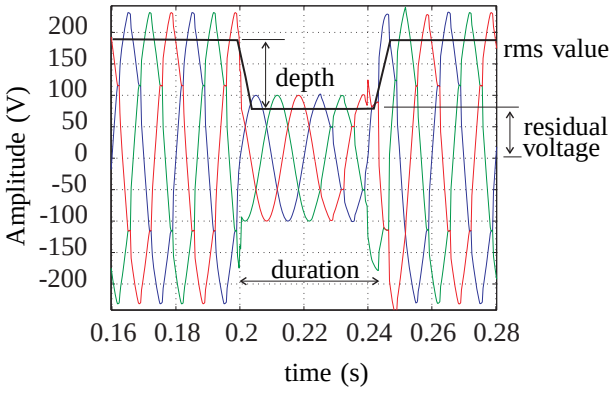

Figure 1. Typical parameters of a voltage sag.

The instantaneous dc-bus voltage at output $v_{dc,o}$ is computed by the instantaneous current i_C through the link capacitor C,

$$C\frac{dv_{dc,o}(t)}{dt} = i_C(t) = i_{dc,i}(t) - i_{dc,o}(t) \qquad (2)$$

Cano et all [4] propose an equation that can be used to compute the time needed (t_{max}) to discharge the capacity C at dc-bus

$$t_{max} = \frac{C(V_{dc,o}^2 - V_{dc,t}^2)}{2P} \qquad (3)$$

where,

- t_{max} Maximum time before the undervoltage protection at ASD trips.
- C dc-bus capacity.
- $V_{dc,o}$ rms dc-bus voltage at inverter input.
- $V_{dc,t}$ rms dc-bus voltage that produces an undervoltage trip at ASD.
- P Active power demanded by the ASD.

Fig. 3 shows the computed value of t_{max} as a function of C/P and $V_{dc,t}$.

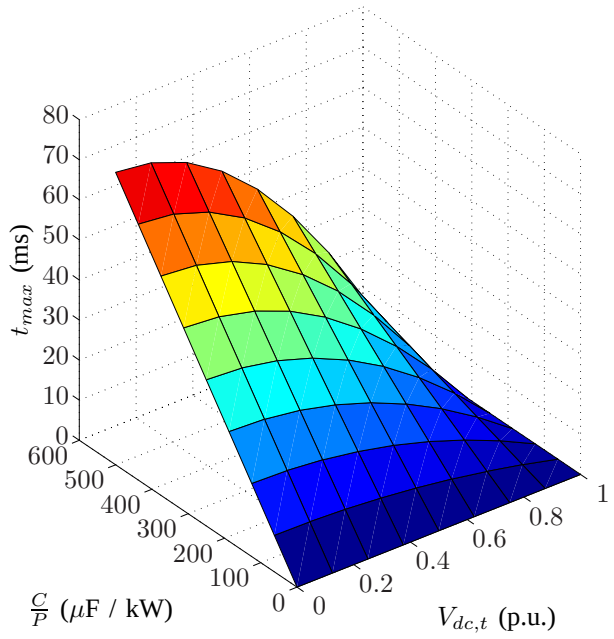

Figure 3. Maximum voltage sag duration for and ASD as a function of $V_{dc,t}$ and the ratio C/P.

The basic model of Fig. 2 has been implemented using PSCAD [14]. This model can be considered a basic approach for analyzing the behavior of the residual voltage at dc-bus as a function of L_{dc}, C, R_g, L_g and the voltage sag depth and duration.

3. Set-up facility

A Set-up facility suitable for testing the behavior of the ASD to voltage sags has been developed. The facility has a programmable power supply with the ability to generate three-phase arbitrary waveforms. Fig. 4 summarizes the structure of the proposed test system. The facility also includes a programmable mechanical load that can be used to simulate typical loads.

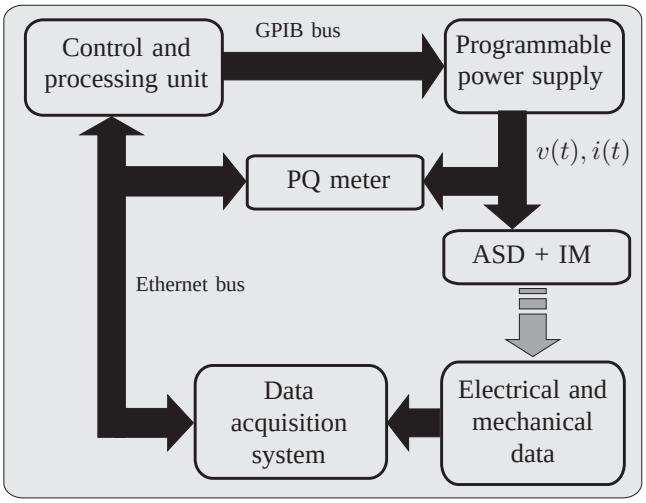

Figure 4. Set-up facility for sags testing.

4. Results

The basic equivalent circuit of fig. 2 has been simulated using PSCAD/EMTDC [14] for a 1.5 kW equivalent machine. The model is shown in Fig. 7. This software has a powerful multiple run module that can be used to study the sensitivity of electrical parameters.

Among other factors, the ratio between the power of the driver and the short-circuit power at common coupling point will define the effects of voltage dips on the dc-link. Fig. 5 shows the impact of voltage dips over the dc-bus as a function of the ratio between the short-circuit power and the nominal power of the ASD considering a dc-link capacity C of 300 μF.

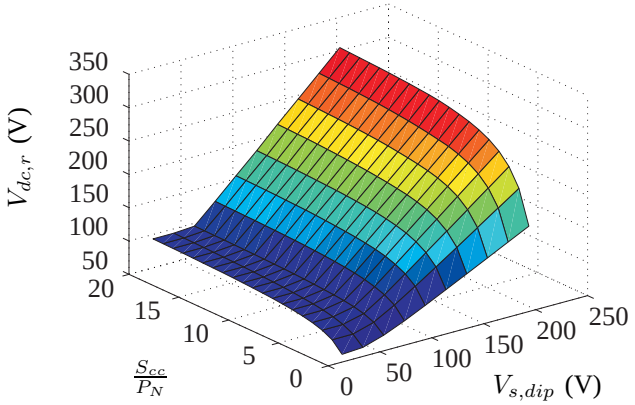

Figure 5. Residual voltage at dc-bus during a sag as a function of the $\frac{S_{cc}}{P_N}$ ratio and the residual voltage at source.

Fig. 5 shows that, from a general point of view, the residual value of the voltage sag is almost similar to the residual value of the voltage supply when the ratio between the short-circuit power at common coupling point and the nominal power of the driver is greater or equal to 15.

Fig. 6 shows that dc-bus capacity C plays the most important role in the behavior of the overall system regarding voltage dips.

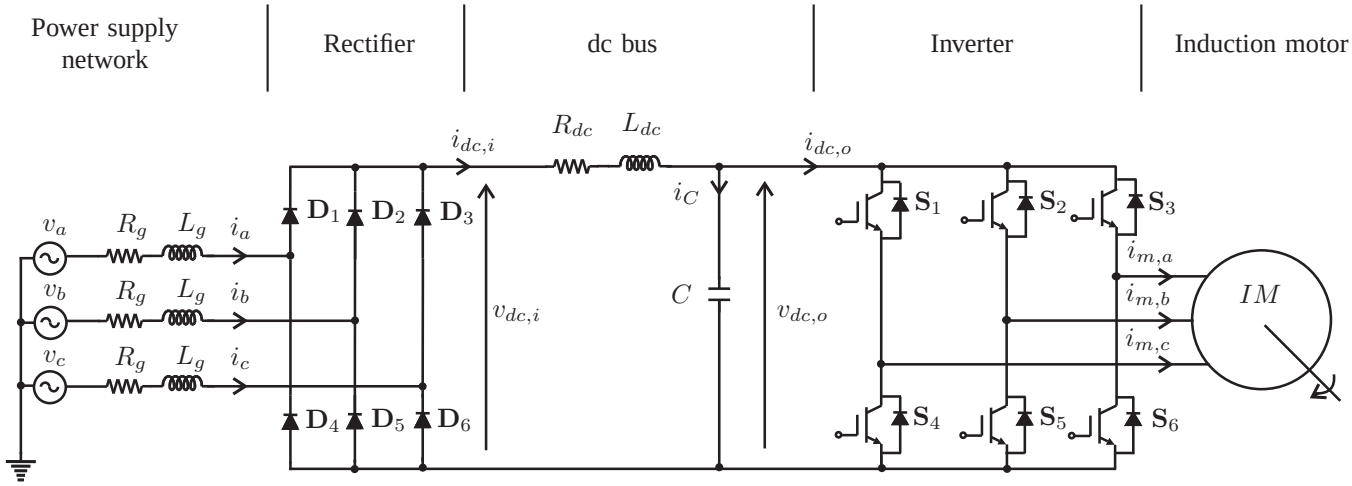

Figure 2. Equivalent circuit model of the ASD power stage.

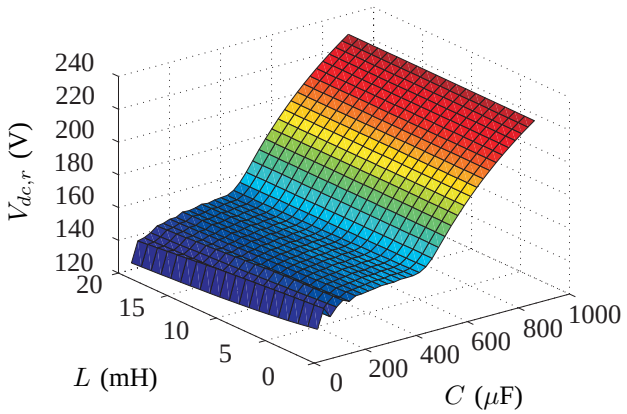

Figure 6. Residual voltage at dc-bus during a sag as a function of the dc-link C and L_{dc}

5. Conclusions

The survival of the ASD to voltage sags depends on the trip-point settings of the drive protections and the way the control is implemented. Undervoltage protection with a trip point set close to the nominal voltage will cause high sensitivity to sags. An increase in the capacity at dc-bus will increase their immunity to voltage sags.

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Appendix
PSCAD/EMTDC Basic Model

Fig. 7 shows the PSCAD basic model used for sensitivity analysis. It is important to underline the *multirun* component. This module can be used to control a multiple run simulation. Up to six variables can be controlled and the component can record up to six channels each run.

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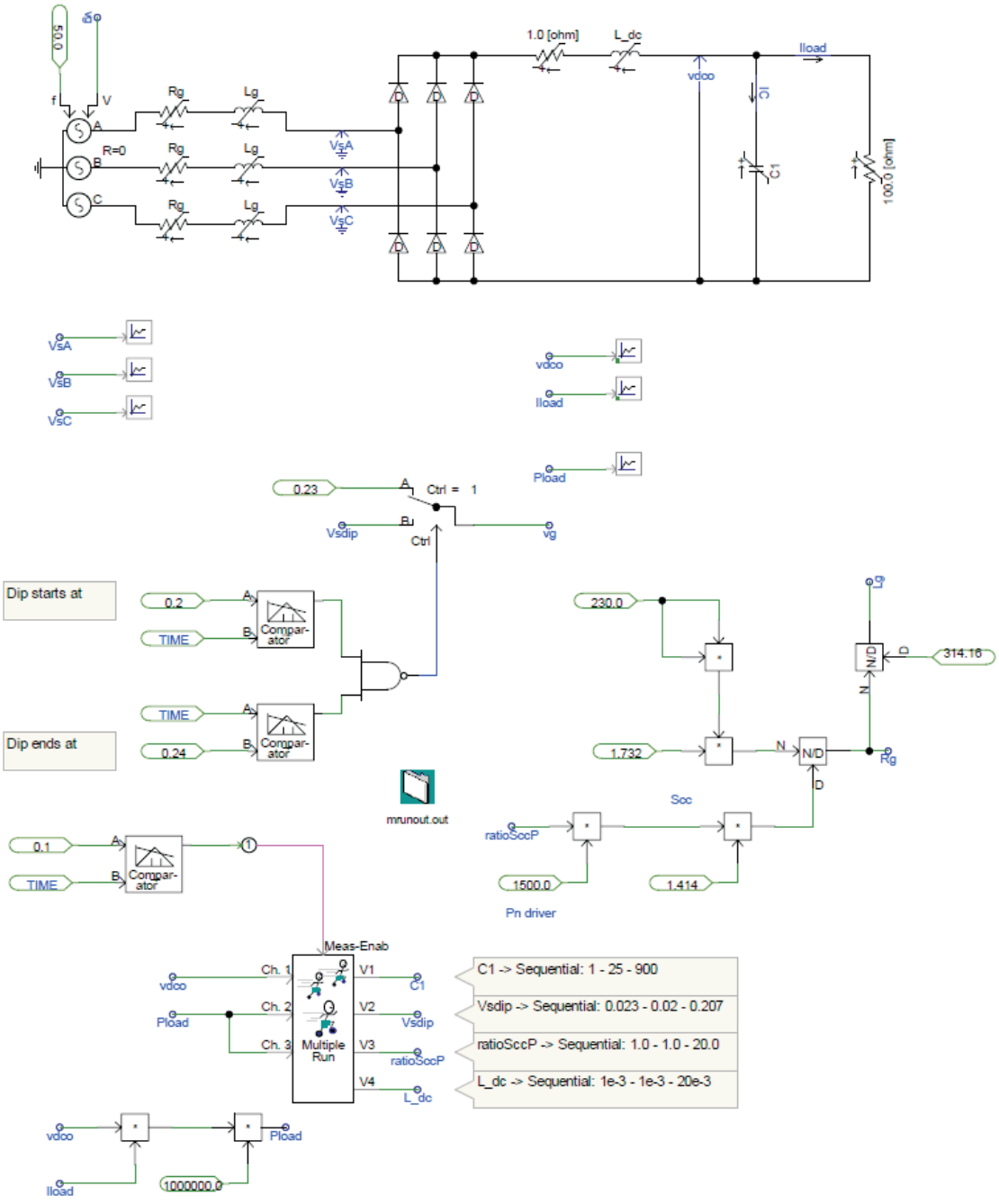

Figure 7. Basic PSCAD model used for sensitivity analysis.