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NONLINEAR MODELING OF TRAPPING AND THERMAL EFFECTS ON GaAs AND GaN MESFET/HEMT DEVICES

M. Chaibi, T. Fernández*, A. Mimouni, J. Rodriguez-Tellez, A. Tazón, and A. Mediavilla

Departamento de Ingeniería de Comunicaciones, Universidad de Cantabria, Laboratorios I+D+i de Telecomunicaciones, Plaza de la Ciencia s/n, Santander 39005, Spain

Abstract—A novel nonlinear model for MESFET/HEMT devices is presented. The model can be applied to low power (GaAs) and high power (GaN) devices with equal success. The model provides accurate simulation of the static (DC) and dynamic (Pulsed) I-V characteristics of the device over a wide bias and ambient temperature range (from $-70°$C to $+70°$C) without the need of an additional electro-thermal sub-circuit. This is an important issue in high power GaN HEMT devices where self-heating and current collapse due to traps is a more serious problem. The parameter extraction strategy of the new model is simple to implement. The robustness of the model when performing harmonic balance simulation makes it suitable for RF and microwave designers. Experimental results presented demonstrate the accuracy of the model when simulating both the small-signal and large-signal behavior of the device over a wide range of frequency, bias and ambient temperature operating points. The model described has been implemented in the Advanced Design System (ADS) simulator to validate the proposed approach without convergence problems.

1. INTRODUCTION

The simulation of the DC and dynamic characteristics of MESFET and HEMT devices as a function of bias (whether they be static and/or dynamic), temperature and frequency has received much attention over recent years [1–11]. Addressing these three areas with a

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* Corresponding author: Tomas Fernandez (tomas.fernandez@unican.es).

nonlinear model which provides a good compromise between accuracy, model complexity, and ease of parameter extraction has proved to be troublesome. There is no doubt that the significant dependence of the MESFET and HEMT I-V characteristics on frequency has played a major role in this situation. The inter-dependence between trapping effects and the thermal conditions of the device (whether they be through self-heating or ambient) has also added to the simulation difficulties [12–14].

With the arrival of GaN HEMT, the combination of higher operating potentials and higher operating currents lead to higher power dissipation levels which worsen the effects of self-heating and traps. The latter leads to current collapse due to the gate- and drain-lag phenomena [15–19]. For such devices the need for a more accurate simulation model which accounts for such effects in a relatively simple manner is imperative.

In this paper we present a novel nonlinear model, along with the model topology, which simulates accurately the static and/or dynamic I-V characteristics of MESFETs and HEMTs over a wide bias and temperature region without the need of an additional electro-thermal sub-circuit. In the new model, thermal and trapping effects are simulated by modifying the parameters which define the nonlinear current source I_{ds}. The method employed to modify these parameters so that such effects are taken into account represents the novelty of this work. This approach also accounts for the inter-dependence between trapping effect, the bias and thermal conditions of the device. This approach reduces the model complexity considerably and leads to a model that can be implemented in circuit simulators relatively easily. The model described here has, for example, been implemented in the Advanced Design System (ADS) simulator and its application has not led to convergence problems.

Experimental results to be presented also show the model accuracy when simulating the small- and large-signal behavior of low and high power devices over a wide range of frequency, bias and ambient temperature conditions. For one of the devices, the accuracy of the model under large-signal conditions (output versus input power) is also demonstrated.

We believe that the new approach described here can be, suitably modified, applied to other models [20–23] to increase their accuracy and area of operation without unduly increasing their complexity.

2. *I-V* PULSED MEASUREMENTS AND NONLINEAR MODELING

The measurement of the device *I-V* characteristics under pulsed conditions offers significant advantages. For example, by adjusting the pulse width and duty cycle the amount of self-heating can be controlled or eliminated. The measurement frequency also enables the characteristics to be observed once the frequency dispersion effect has taken place. Performing the measurements from different static bias points also enable the self-heating due to the power dissipated, the current collapse and the interaction between the two be observed. To demonstrate some of these points a high power $8 \times 75\,\mu$m AlGaN/GaN HEMT manufactured by *III-V* LAB will be employed as a test vehicle. This device was selected due to its high current handling capability which enables the self-heating and effects of traps to be more clearly observed. Later in the paper a lower power GaAs MESFET will also be used to demonstrate the accuracy and generality of the modeling approach described.

The experimental results presented in this paper were performed with a pulse width of 1 µs and a duty cycle of 0.001.

2.1. Trapping Effects: Current Collapse

The pulse measurement technique enables the phenomena of current collapse (gate-lag and drain-lag) to be observed simply by measuring the pulsed *I-V* characteristics of the device from different static bias points. This should be clear since the state-occupancy of the traps is dependent on the static operating point as well as the sudden change in the electric field due to the change in the dynamic bias.

To observe the current collapse due to gate-lag it is only necessary to measure the dynamic *I-V* characteristics from different DC bias points with the drain-source at the static point of $V_{dscc} = 0\,$V. Since it is only the static gate-source potential that is varied this, and the pulse test conditions, ensures that no self-heating takes place. The resulting data, therefore, shows the effect of changes to the electric field on the traps. This is demonstrated in Fig. 1.

The behavior of the data shown in Fig. 1 is normally attributed to surface traps situated primarily between the gate and drain terminals [24–27]. For large negative gate potentials the energy states situated in the buffer region can, however, capture free charges and augment the gate-lag effect [27, 28].

In the case of current collapse due to drain-lag, the pulsed *I-V* measurements are performed in the same manner. This time it is the static potential on the drain-source (V_{dscc}) which is varied with

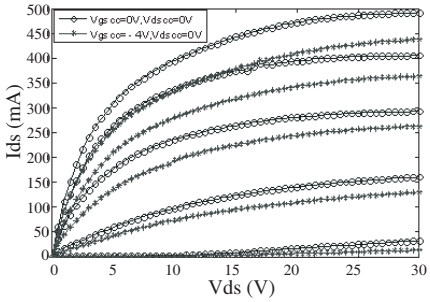

Figure 1. Pulsed I-V curves at various static gate-source potentials showing gate-lag effect for the GaN device. V_{gs} range from -4 V to 0 V.

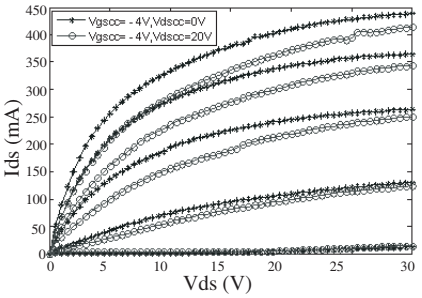

Figure 2. Pulsed I-V curves at various static drain-source potentials showing drain-lag effect for the GaN device. V_{gs} range from -4 V to 0 V.

the gate-source set near to pinch-off thereby ensuring no self-heating. Fig. 2 shows the pulsed I-V characteristics of the same device under these conditions.

While the effects of gate-lag are normally attributed to surface traps, the effects of drain-lag are mainly due to traps present in the buffer and the substrate region [29, 30]. The problems that arise from gate-lag can be reduced by improved passivation. Unfortunately, this approach can not be used to reduce the effects of drain-lag [31–33].

2.2. Self-heating

The effect of self-heating is particularly important in devices able to handle high power. The GaN device considered previously is a good example of this. The effect of self-heating is quite noticeable in the DC I-V characteristics. These normally show a pronounced negative slope in the saturation region as the current and hence power dissipation level increases. In Fig. 3 for example, we show the DC and dynamic I-V characteristics of the device. The pulsed I-V characteristics were measured from the static bias points of $V_{gscc} = 0$ V, $V_{dscc} = 0$ V. The negative slope in the drain current for the DC case, where there is considerable self-heating, is quite marked against the pulsed I-V case where there is no self-heating. For the $V_{gs} = 0$ V curve at a V_{ds} value of 30 V, for example, the percentage difference between the DC and dynamic current values is 33%.

2.3. Ambient Temperature

In order to observe the effects of changing the ambient temperature a number of pulsed I-V measurements of the GaN device were

performed, from the static bias points of ($V_{gscc} = -4V$, $V_{dscc} = 20\,\mathrm{V}$) and ($V_{gscc} = 0\,\mathrm{V}$, $V_{dscc} = 0\,\mathrm{V}$), using a temperature controlled chamber. Fig. 4 shows the behavior of the device at +27°C. For this case the maximum drain-current (at $V_{gs} = 0\,\mathrm{V}$) is degraded by 78 mA. Fig. 5 shows the corresponding results at +70°C. For the $V_{gs} = 0\,\mathrm{V}$ curves, at the saturation region, the difference in the drain current at the two bias points is 66 mA.

For both cases, it can be seen that a change in the ambient temperature not only changes the value of the drain current but also the distribution of the traps. These results indicate the importance of the interaction between thermal effects and the bias conditions, and hence trapping states, of the device in determining the drain-current degradation.

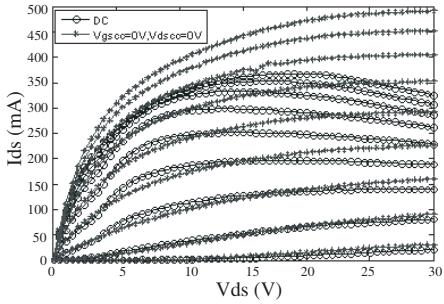

Figure 3. DC and pulsed *I-V* characteristics for the GaN device. V_{gs} range from −4 V to 0 V with a voltage step size of 0.5 V.

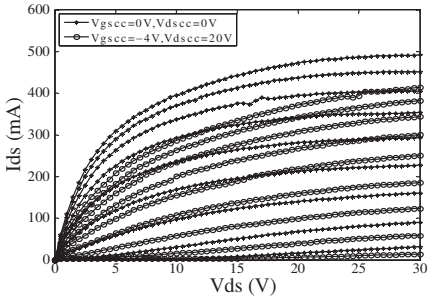

Figure 4. Pulsed *I-V* curves for the GaN device at +27°C from two different bias points. V_{gs} range from −4 V to 0 V with a voltage step size of 0.5 V.

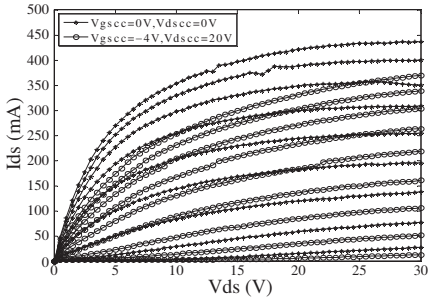

Figure 5. Pulsed *I-V* curves for the GaN device at +70°C from two different bias points. V_{gs} range from −4 V to 0 V with a voltage step size of 0.5 V.

2.4. Summary

The above results clearly shows the usefulness of the pulsed measurement idea as a means of developing a nonlinear model able to simulate the DC and dynamic I-V characteristics of the device over a wide bias and ambient temperature region. The results also illustrate the need to account for the inter-dependence between bias, thermal and trapping effects. In the following sections a modeling approach which satisfies these conditions is described.

3. DC AND DYNAMIC NONLINEAR MODEL

3.1. Drain-source Current Source

The nonlinear dependence of the drain-source current of the device on the intrinsic gate-source and drain-source potentials is usually expressed as:

$$I_{ds} = f(V_{gsi}, V_{dsi}) \tag{1}$$

In this expression f is a nonlinear function which describes the dependence of the drain-source current I_{ds} on the internal gate-source V_{gsi} and internal drain-source V_{dsi} junction voltages. The limitation of this approach is that the defining junction potentials can either represent the DC or the dynamic (after the frequency dispersion effect has taken place) junction potentials but not both. While a number of suggestions have been proposed to overcome this problem [34–40] the procedure illustrated below produces excellent results and is simple to implement.

As described in reference [41], our initial approach was to modify the general expression I_{ds} as defined in (1) as:

$$I_{ds} = f\left(V_{gsicc}, V_{dsicc}, V_{gsi}(t), V_{dsi}(t)\right) \tag{2}$$

where V_{gsicc} and V_{dsicc} represent the intrinsic static potentials and $V_{gsi}\,(t)$ and $V_{dsi}\,(t)$ represent the intrinsic dynamic potentials applied to the device.

While the above approach worked well with low power devices, for high power GaN HEMT structures the accuracy in reproducing the dynamic I-V characteristics of the device was not good. This was especially so for those cases where the potentials and current levels were high. Following many measurements and modeling attempts on a variety of GaN HEMT devices it was observed that the modeling emphasis should be placed on the parameters which control the drain-source current source rather than on the potentials which control the current source.

In view of the above, a new approach has been developed so that a model able to accurately simulate the DC and dynamic *I-V* characteristics at any operating bias point of the DC characteristics and ambient temperature was achieved. This was performed simply by making each parameter which defines the behavior of the nonlinear, I_{ds}, current source dependent on the static and dynamic bias points. In this way each parameter of the model, which would normally be a constant, vary as the DC bias (V_{gsicc} and V_{dsicc}) and the dynamic bias (V_{gsid} and V_{dsid}) vary. The expression developed to perform this for each parameter takes the form:

$$p_i = p_{i\_\mathrm{DC}} \cdot (1 + \lambda_i \cdot V_{gsid} + \beta_i \cdot V_{dsid}) \tag{3}$$

where p_i represents parameter "i" of the nonlinear equation for I_{ds}, p_{i_DC} represents the value of parameter "i" acquired under DC conditions and λ_i and β_i simulate the dependence of parameter "i" on the dynamic potentials V_{gsid} and V_{dsid}. The dynamic potentials are defined as:

$$V_{gsid} = V_{gsi}(t) - V_{gsicc}; \quad V_{dsid} = V_{dsi}(t) - V_{dsicc} \tag{4}$$

where V_{gsicc} and V_{dsicc} represent the static intrinsic potentials and $V_{gsi}(t)$ and $V_{dsi}(t)$ represent the total intrinsic junction potentials applied to the gate-source and drain-source junctions respectively. V_{gsid} and V_{dsid} represent the difference between the static and dynamic intrinsic potentials.

Expressions (3) and (4) have been carefully developed to ensure that the DC and dynamic behavior of the device are accurately reproduced. Notice that when no dynamic potential is applied ($V_{gsid} = 0\,\mathrm{V}$, $V_{dsid} = 0\,\mathrm{V}$) the parameter "i" of the model reduces to its DC value p_{i_DC}.

The need to keep the expressions as simple as possible while at the same time providing good accuracy over as wide an operating range as possible figured highly. Developing an approach which reduces convergence problems was also an important issue.

The above approach was implemented with the model topology shown in Fig. 6. Notice the incorporation of the series RC networks (R_{gg}-C_{gg}, R_{dd}-C_{dd}) in parallel with the intrinsic gate-source and drain-source junctions [42]. These enable the extraction of the DC component (V_{gsicc} and V_{dsicc}) and the dynamic component (V_{gsid} and V_{dsid}) which appear in Equations (3) and (4).

While the parameter estimation process is described in more detail later on, here we briefly describe some of the general points that should be borne in mind. Firstly the most appropriate model to represent the nonlinear current source I_{ds} should be decided on. This will largely depend on the application. Once this issue has been

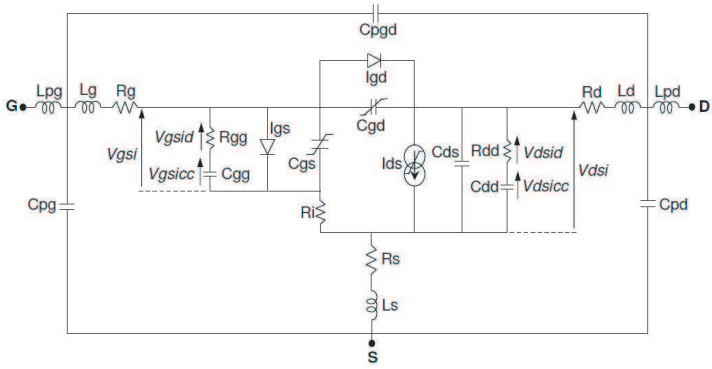

Figure 6. The nonlinear model topology employed.

decided on, the DC parameters of the model selected for I_{ds} should be determined from DC I-V measurements at the reference ambient temperature T_0 of +27°C (300 K). The temperature dependency of these DC parameters should then be determined (and the relevant ambient temperature modeling parameters extracted) from DC I-V measurements at different ambient temperatures. Finally, the parameters that simulate the dynamic behavior of the device should be determined from pulsed I-V measurements. These are performed from different and carefully selected static bias points (referred to as key points later on) at the reference ambient temperature point. Each of the parameters of the model "p_i" for I_{ds} will, therefore, contain components which simulate their dependency on the DC, dynamic and ambient temperature conditions. Their form is:

$$p_i = p_{i\_\mathrm{DCT}} \cdot (1 + \lambda_i \cdot V_{gsid} + \beta_i \cdot V_{dsid}) \tag{5}$$

where

$$p_{i\_\mathrm{DCT}} = p_{i\_\mathrm{DCTo}} + k_{i\_\mathrm{DC}} \cdot (T - T_0) \tag{6}$$

where p_{i_DCT} is parameter "i" of the DC model for I_{ds} at the ambient temperature of interest T. p_{i_DCTo} is the value of the same parameter at the reference temperature T_0 and k_{i_DC} defines the temperature dependence of the parameter.

As a test vehicle for the above idea, the nonlinear expression employed to represent the drain-source current source of the device is [43]:

$$I_{ds} = I_{dss} \cdot \exp\left(-\left(V_{giflch}^{\delta}/\mu\right)\right) \cdot (V_{giteff})^{(E+K_E \cdot V_{gsi})} \cdot \left(1 + \frac{S_s v_{dsi}}{I_{dss}}\right) \cdot \tanh\left(\frac{S_L \cdot v_{dsi}}{I_{dss} \cdot (1 - K_G \cdot v_{gsi})}\right) \tag{7}$$

where

$$v_{giteff} = \frac{1}{2 \cdot \eta} \cdot (\chi \cdot v_{git} + v_{gitlch}) \tag{8}$$

$$v_{gitlch} = \ln\left(2 \cdot \cosh\left(\chi \cdot v_{git}\right)\right) \tag{9}$$

$$v_{giflch} = \ln\left(2 \cdot \cosh\left(v_{gif}\right)\right) \tag{10}$$

$$v_{git} = v_{gsi} - \left(V_p + \gamma \cdot v_{dsi}\right); \quad v_{gif} = v_{gsi} - V_{\mathrm{PF}} \tag{11}$$

In its present form this is a standard nonlinear DC model for the device and a fuller description of this DC model together with experimental results and the parameter extraction process can be found in the quoted reference. It is used here since it provides good accuracy from a DC point of view and is particularly suited to applications where the accurate simulation of intermodulation distortion is important. It also illustrates the remarks made earlier that the proposed new simulation approach can be applied to many of the existing expressions for I_{ds}.

To convert this standard DC model to a model able to simulate the DC and dynamic behavior of the device, including therefore self-heating and trapping effects, it is only necessary to replace the model parameters in the above equations by the new dynamic parameters through expressions (3) and (4) (p_i parameter would be: I_{dss}, V_P, V_{PF}, γ, χ, η, K_G, S_L, S_S, $K_E\,E$, μ, and δ). For the purposes of this paper it can be assumed that this process has been performed.

3.2. Gate-Source and Gate-Drain Junctions

For completeness, the expressions employed to model the nonlinear gate-source and gate-drain current sources ($I_{gs}\left(V_{gs}\right)$, $I_{gd}\left(V_{gd}\right)$) and capacitances ($C_{gs}\left(V_{gs}\right)$, $C_{gd}\left(V_{gd}\right)$) [44] are stated below.

$$I_{gx} = I_{nss} \cdot (\exp(\alpha \cdot V_{gx}) - 1) \tag{12}$$

$$C_{gx} = C_{gx0} + \frac{A_{Cgx}}{2} \cdot (1 + \tanh\left[K_{Cgx} \cdot (V_{gx} - V_{Cgx})\right]) \tag{13}$$

where "x" refers to "s" or "d".

4. THERMAL EFFECTS MODELING

4.1. Incorporation of Thermal Effects into I_{ds} Current Source

As mentioned above, the effects of ambient temperature are introduced into the DC model for I_{ds} using expression (6). The effects of self-heating are incorporated in the model in an implicit manner. It should be remembered that the parameters of the model implicitly includes the

effects of the power dissipated in the device as the operating conditions are varied.

The λ_i and β_i parameters, which define the dynamic conditions, are assumed to be temperature-independent. This assumption does not degrade the model accuracy unduly. It should be noted that the dynamic I-V characteristics are measured using a pulse system which enables full control of the measurement frequency, rise time and width of the pulses. The conditions employed ensure that the dynamic potentials applied to the device do not cause self-heating. The parameters which model thermal effects in I_{ds} are determined uniquely from the DC I-V characteristics of the device measured at different ambient temperatures.

Although the above thermal equation could be introduced for each parameter of the basic DC model, in many cases it is sufficient to only consider those parameters which have a primary role in defining the DC value of I_{ds}. To a large extent this will depend on the model in use and the application. For the purposes of this paper, all the parameters defining the DC behavior of the device in the expression for I_{ds} were included from a thermal point of view.

4.2. Incorporation of Thermal Effects into Gate-source and Gate-drain Junctions

In order to model the effects of ambient temperature on the gate-source and gate-drain capacitance it has been assumed that parameters C_{gx0}, A_{Cgx}, K_{Cgx}, and V_{Cgx} associated with each junction capacitance C_{gs} and C_{gd} (13) vary with temperature in the linear fashion:

$$C_{gx0} = C_{gx0T0} + C_{gx0T} \cdot (T - T_0) \tag{14}$$

$$A_{Cgx} = A_{CgxT0} + A_{CgxT} \cdot (T - T_0) \tag{15}$$

$$K_{Cgx} = K_{CgxT0} + K_{CgxT} \cdot (T - T_0) \tag{16}$$

$$V_{Cgx} = V_{CgxT0} + V_{CgxT} \cdot (T - T_0) \tag{17}$$

where C_{gx0T0}, A_{CgxT0}, K_{CgxT0}, and V_{CgxT0} are the value of the parameters C_{gx0}, A_{Cgx}, K_{Cgx}, and V_{Cgx} at the reference temperature T_0 and C_{gx0T}, A_{CgxT}, K_{CgxT}, and V_{CgxT} define the temperature dependence of these parameters.

All the parameters defining I_{gs} and I_{gd} (12) were considered to be ambient temperature-dependent. For this case their temperature dependence was assumed to be of the form:

$$I_{nss} = I_{nss0} \cdot \exp\left(I_{nssT} \cdot \left(\frac{T}{T_0} - 1\right)\right) \tag{18}$$

$$\alpha = \alpha_0 \cdot \exp\left(\alpha_T \cdot \left(\frac{T}{T_0} - 1\right)\right) \tag{19}$$

where I_{nss0} and α_0 are the parameter values of I_{nss} and α at the reference temperature T_0. I_{nssT} and α_T simulate the temperature dependency of the previously described parameters.

5. MODEL TOPOLOGY AND PARAMETERS ESTIMATION STRATEGY

The topology of the nonlinear model employed is shown in Fig. 6. Notice the inclusion of the elements associated with the package of the device which are relevant for the test MESFET considered in this paper. For those cases where an on-wafer device is under consideration, the relevant elements should be removed from the model topology.

The complete model parameters extraction process could be summarized as follows:

Step 1) Using cold S-parameters measurements [45, 46] at the reference temperature T_0 (+27°C), the parasitic and extrinsic elements of the model are extracted and optimized over the frequency range of interest.

Step 2 Once the parasitic and extrinsic elements have been de-embedded, the bias and temperature-dependent intrinsic elements are extracted using multi-bias S-parameters measurements over the temperature range of interest (−70°C to +70°C).

Step 3) The parameters of the I_{gs} and I_{gd} current sources are extracted from forward current (I_{gs}-V_{gs}, I_{gd}-V_{gd}) measurements over the temperature range of interest.

Step 4) The DC I-V output characteristics of the device are measured over the bias range of interest at the reference temperature T_0. The parameters of the nonlinear DC model are extracted and optimized to provide the best possible fit to the measured data. Once this process is completed, these DC parameters are treated as constant and referenced to T_0.

Step 5) The process described in step 4 is repeated at different ambient temperatures and the parameters that model thermal effects are extracted and optimized against the measured data at all temperature points.

Step 6) Using the pulsed output I-V characteristics of the device, measured at T_0, from five different static bias points (*key operating points*) (($V_{gs} = 0$, $V_{ds} = 0$); (V_{gs} (pinch-off), $V_{ds} = 0$); ($V_{gs} = 0$, $V_{ds\,\max}$); (V_{gs} (pinch-off), $V_{ds\,\max}$); (V_{gs} (50%I_{dss}), $V_{ds\,\max}/2$)), the λ_i and β_i parameters of (3) are estimated and optimized to yield the best accuracy to all five output characteristics. Clearly, this process requires the use of the parameters (step 4) which simulate the DC I-V behavior of the device.

6. SIMULATION AND EXPERIMENTAL RESULTS

6.1. Test Devices

To demonstrate the accuracy of the approach presented, the MGF1923 GaAs MESFET from Mitsubishi Semiconductors and the $8 \times 75\,\mu m$ AlGaN/GaN HEMT from *III-V* LAB were used as test vehicles. Similarly good results have, however, been achieved with devices (of varying gate-widths and number of fingers) from other manufacturers.

6.2. GaN HEMT Experimental Results

In order to demonstrate the validity of the model topology as well as the accuracy of the expressions and methodology described in simulating high power devices, the parameters of I_{ds} for the GaN device were measured. The parameters extraction process ensured that the DC and dynamic characteristics as a function of ambient temperature could be assessed. The parameters associated with the I_{ds} current source are shown in Table 1.

Figure 7 shows the measured and simulated DC *I-V* characteristics for the device at two ambient temperatures. The excellent fit near pinch-off and deep in saturation is worthy of note. The fact that this accuracy is maintained over a relatively wide temperature range is also worthy of note.

Figure 8 shows the measured and simulated pulsed *I-V* curves for the device at three different temperature points. For the $-70°C$ case the starting DC bias conditions correspond to $V_{gscc} = -3\,V$, $V_{dscc} = 5\,V$. For the $+27°C$ case the starting DC bias conditions were $V_{gscc} = -4\,V$, $V_{dscc} = 20\,V$ and, finally, for the $+70°C$ case the starting DC bias conditions were $V_{gscc} = -1\,V$, $V_{dscc} = 10\,V$.

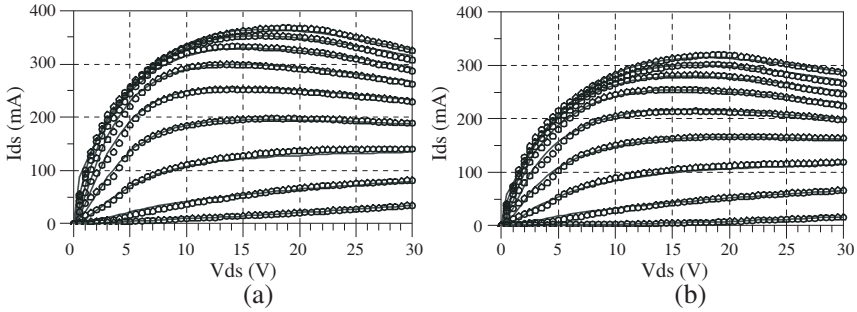

Figure 7. GaN HEMT measured (circles) and simulated (solid lines) DC *I-V* characteristics at (a) $-70°C$ and (b) $+70°C$. V_{gs} range from $-4\,V$ to $0\,V$ with a voltage step size of $0.5\,V$.

Table 1. GaN HEMT Drain-Source current source model parameters.

DC and their correspondent thermal parameters				
Parameter		DC value @ *To* (P_{i_DCTo})	Thermal parameter	Value
p_1:	I_{dss}	443.26 (mA)	k_1	$-1.0061 \cdot 10^{-3}$ (A/K)
p_2:	V_P	−2.2467 (V)	k_2	$-1.95 \cdot 10^{-3}$ (V/K)
p_3:	V_{PF}	0.7012 (V)	k_3	$2.4568 \cdot 10^{-4}$ (V/K)
p_4:	γ	−0.0657	k_4	$9.9949 \cdot 10^{-5}$ (K^{-1})
p_5:	χ	0.962	k_5	$-1.6190 \cdot 10^{-3}$ (K^{-1})
p_6:	η	3.612	k_6	$-6.6054 \cdot 10^{-3}$ (K^{-1})
p_7:	K_G	73.223 (V^{-1})	k_7	$6.8329 \cdot 10^{-1}$ (V^{-1}/K)
p_8:	S_L	24.8032	k_8	$2.3443 \cdot 10^{-1}$ (K^{-1})
p_9:	S_S	423.844 (mA/V)	k_9	$9.9356 \cdot 10^{-4}$ (A/(V·K))
p_{10}:	K_E	−0.7593 (V^{-1})	k_{10}	$-7.6036 \cdot 10^{-4}$ (V^{-1}/K)
p_{11}:	E	-2.8967	k_{11}	$-3.7347 \cdot 10^{-3}$ (K^{-1})
p_{12}:	μ	0.2892	k_{12}	$-4.1814 \cdot 10^{-4}$ (K^{-1})
p_{13}:	δ	0.3102	k_{13}	$6.4947 \cdot 10^{-5}$ (K^{-1})
Dynamic parameters				
Parameter		Value (V^{-1})	Parameter	Value (V^{-1})
λ_1		$2.3899 \cdot 10^{-1}$	β_1	$1.0257 \cdot 10^{-2}$
λ_2		$-1.3725 \cdot 10^{-1}$	β_2	$-1.3897 \cdot 10^{-2}$
λ_3		$-8.5789 \cdot 10^{-3}$	β_3	$2.1935 \cdot 10^{-2}$
λ_4		$-2.3580 \cdot 10^{-2}$	β_4	$-2.3788 \cdot 10^{-3}$
λ_5		$1.1425 \cdot 10^{-1}$	β_5	$-1.2729 \cdot 10^{-2}$
λ_6		$1.4924 \cdot 10^{-2}$	β_6	$-1.2687 \cdot 10^{-2}$
λ_7		$-1.9131 \cdot 10^{-1}$	β_7	$-8.6126 \cdot 10^{-3}$
λ_8		$-2.4482 \cdot 10^{-1}$	β_8	$3.3526 \cdot 10^{-4}$
λ_9		$-1.6628 \cdot 10^{-1}$	β_9	$8.1041 \cdot 10^{-3}$
λ_{10}		$-6.3628 \cdot 10^{-2}$	β_{10}	$-7.9717 \cdot 10^{-3}$
λ_{11}		$-1.5226 \cdot 10^{-1}$	β_{11}	$-8.6968 \cdot 10^{-3}$
λ_{12}		$7.7157 \cdot 10^{-2}$	β_{12}	$-2.0771 \cdot 10^{-3}$
λ_{13}		$1.5324 \cdot 10^{-2}$	β_{13}	$-7.4605 \cdot 10^{-3}$
Parasitic resistances				
$R_g = 0.8\,\Omega$; $R_d = 1.2\,\Omega$; $R_s = 0.6\,\Omega$				

As with the DC case previously, the accuracy of the model in representing the dynamic characteristics is high. The precision near pinch-off and saturation across the three temperature point is, for

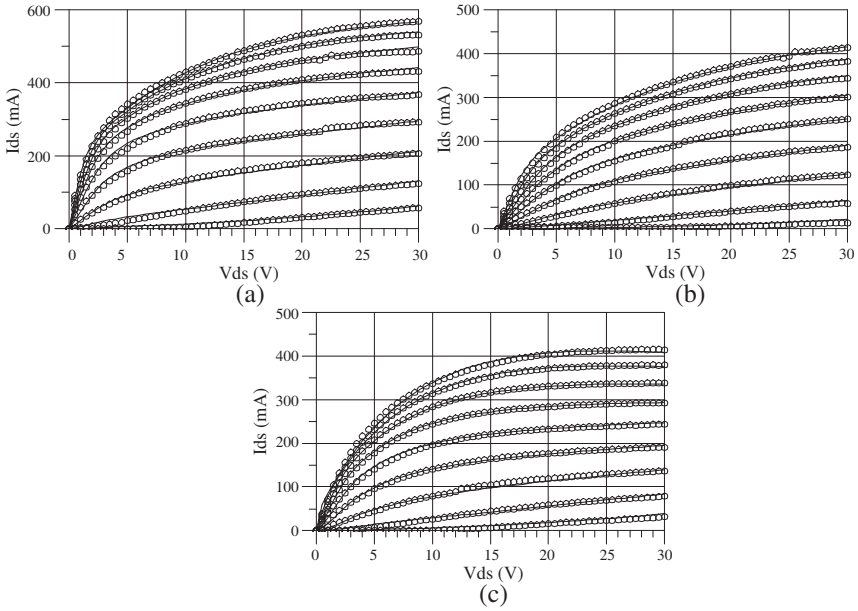

Figure 8. GaN HEMT measured (circles) and simulated (solid lines) pulsed I-V characteristics at (a) $-70°$C, (b) $+27°$C and (c) $+70°$C. V_{gs} range from -4 V to 0 V with a voltage step size of 0.5 V.

example, excellent. As can be seen this particular device is quite dispersive but the accuracy of the results highlights the effectiveness of the λi and βi parameters in simulating the trapping effects.

Similarly good results were obtained at other bias and temperature points. It is also worth noting that the test conditions demonstrated here were different to those used in the parameters estimation/optimization process.

6.3. MGF1923 GaAs MESFET Experimental Results

As with the previous case, in this section we demonstrate the accuracy of the modeling approach with a lower power GaAs MESFET. In Table 2, the parameters associated with the I_{ds} current source are shown.

Table 3 shows the extrinsic, packaging-related and intrinsic parameter values. Finally, Table 4 shows the parameters associated with the gate-source and gate-drain junctions, including the thermal modeling parameters.

Figure 9 shows the experimental and simulated DC I-V curves for the device at two different ambient temperatures. As can be seen,

Table 2. MGF1923 drain-source current source model parameters.

DC and their correspondent thermal parameters				
Parameter		DC value @ To (P_{i_DCTo})	Thermal parameter	Value
p_1:	I_{dss}	80.703 (mA)	k_1	$3.0863{\cdot}10^{-4}$ (A/K)
p_2:	V_P	−1.0006 (V)	k_2	$-4.9478 \cdot 10^{-3}$ (V/K)
p_3:	$V_{\rm PF}$	1.5865 (V)	k_3	$4.0932{\cdot}10^{-3}$ (V/K)
p_4:	γ	−0.2204	k_4	$1.554{\cdot}10^{-4}$ ($\rm K^{-1}$)
p_5:	χ	2.5268	k_5	$1.2362{\cdot}10^{-2}$ ($\rm K^{-1}$)
p_6:	η	10.6678	k_6	$7.0145{\cdot}10^{-2}$($\rm K^{-1}$)
p_7:	K_G	−0.0285 ($\rm V^{-1}$)	k_7	$5.0438 \cdot 10^{-4}$ ($\rm V^{-1}$/K)
p_8:	S_L	0.226	k_8	$7.7293{\cdot}10^{-4}$ ($\rm K^{-1}$)
p_9:	S_S	17.95 (mA/V)	k_9	$-4.8846{\cdot}10^{-5}$ (A/(V· K))
p_{10}:	K_E	−0.9899 ($\rm V^{-1}$)	k_{10}	$8.3934 \cdot 10^{-4}$ ($\rm V^{-1}$/K)
p_{11}:	E	−0.9181	k_{11}	$1.7394{\cdot}10^{-4}$ ($\rm K^{-1}$)
p_{12}:	μ	0.8186	k_{12}	$-1.7036 \cdot 10^{-3}$ ($\rm K^{-1}$)
p_{13}:	δ	0.3714	k_{13}	$-1.7808 \cdot 10^{-3}$ ($\rm K^{-1}$)
Dynamic parameters				
Parameter		Value ($\rm V^{-1}$)	Parameter	Value ($\rm V^{-1}$)
λ_1		$6.3759 \cdot 10^{-3}$	β_1	$-1.6558 \cdot 10^{-1}$
λ_2		$-4.2069 \cdot 10^{-2}$	β_2	$-3.8408{\cdot}10^{-2}$
λ_3		$3.0674 \cdot 10^{-1}$	β_3	$-9.1495 \cdot 10^{-2}$
λ_4		$-2.3610 \cdot 10^{-1}$	β_4	$6.2167 \cdot 10^{-2}$
λ_5		$-6.6742 \cdot 10^{-2}$	β_5	$-5.9005 \cdot 10^{-2}$
λ_6		$3.2157{\cdot}10^{-3}$	β_6	$-2.5832{\cdot}10^{-2}$
λ_7		-2.1194	β_7	−1.7585
λ_8		$-1.2333{\cdot}10^{-2}$	β_8	$-1.6711{\cdot}10^{-1}$
λ_9		$-2.6897{\cdot}10^{-1}$	β_9	$2.2419{\cdot}10^{-2}$
λ_{10}		$-9.0582{\cdot}10^{-2}$	β_{10}	$1.3147{\cdot}10^{-2}$
λ_{11}		$-2.1508{\cdot}10^{-1}$	β_{11}	$1.0517{\cdot}10^{-1}$
λ_{12}		$1.0966{\cdot}10^{-1}$	β_{12}	$-3.4334{\cdot}10^{-2}$
λ_{13}		$-3.7102{\cdot}10^{-1}$	β_{13}	$-8.5548{\cdot}10^{-4}$

the accuracy of the model in simulating the DC characteristics of the GaAs device as a function of bias and ambient temperature is as good as for the GaN transistor.

In Fig. 10, we show the measured and computed dynamic characteristics of the device at three different static bias and ambient

Table 3. MGF1923 drain-source current source model parameters.

Packaging and extrinsic elements		
Inductances	Capacitances	Resistances
$L_{pg} = 99.67\,\text{pH}$; $L_{pd} = 0.2\,\text{nH}$ $L_g = 0.58\,\text{nH}$; $L_d = 0.62\,\text{nH}$ $L_s = 62.42\,\text{pH}$	$C_{pg} = 0.14\,\text{pF}$ $C_{pd} = 0.156\,\text{pF}$ $C_{pgd} = 17.42\,\text{fF}$ $C_{gg} = C_{dd} = 1\,\text{pF}$	$R_g = 1.82\,\Omega$ $R_d = 1.58\,\Omega$ $R_s = 1.52\,\Omega$ $R_{gg} = R_{dd} = 10\,\text{M}\Omega$
Intrinsic elements		
$R_i = 5.8\,\Omega$; $\tau = 4.42\,\text{ps}$; $C_{ds} = 0.13\,\text{pF}$		

Table 4. MGF1923 gate-source and gate-drain rectifying junctions parameters.

Gate-Source Junction Capacitance
$C_{gs0T0} = 0.12$ (pF); $A_{CgsT0} = 0.303$ (pF); $K_{CgsT0} = 0.94$ (V^{-1}); $V_{CgsT0} = -1.42$ (V); $C_{gs0T} = 1.4031{\cdot}10^{-3}$ (pF/K); $A_{CgsT} = -1.96 \cdot 10^{-3}$ (pF/K) $K_{CgsT} = 1.031 \cdot 10^{-3}$ (V^{-1}/K); $V_{CgsT} = 4.017 \cdot 10^{-3}$ (V/K)
Gate-Drain Junction Capacitance
$C_{gd0T0} = 23.387$ (fF); $A_{CgdT0} = 98.361$ (fF); $K_{CgdT0} = 1.58$ (V^{-1}); $V_{CgdT0} = -0.89$ (V) $C_{gd0T} = -4.7803 \cdot 10^{-2}$ (fF/K); $A_{cgdT} = -1.6865 \cdot 10^{-1}$ (fF/K) $K_{CgdT} = -2.8071 \cdot 10^{-3}$ (V^{-1}/K); $V_{CgdT} = 1.2583 \cdot 10^{-3}$ (V/K)
Gate-Source and Gate-Drain nonlinear current sources
$I_{nss0} = 3.52 \cdot 10^{-11}$ (A); $\alpha_0 = 28$ (V^{-1}) $I_{nssT} = 21.684$; $\alpha_T = -0.675$

temperature points. For the $-70°$C case the starting DC bias conditions correspond to $V_{gscc} = -0.4\,\text{V}$, $V_{dscc} = 2\,\text{V}$. For the $+27°$C case the starting DC bias conditions were $V_{gscc} = -1.6\,\text{V}$, $V_{dscc} = 1\,\text{V}$. For the $+70°$C case the starting DC bias conditions were $V_{gscc} = -0.8\,\text{V}$, $V_{dscc} = 4\,\text{V}$. As with the DC case previously, the accuracy of the model in representing the dynamic characteristics is very good.

In Fig. 11, we show the measured and simulated scattering parameters of the device over the 0.4 to 15 GHz frequency range at three different ambient temperature points. For the $-70°$C case the DC bias conditions correspond to $V_{gscc} = -1.2\,\text{V}$, $V_{dscc} = 4\,\text{V}$. For the

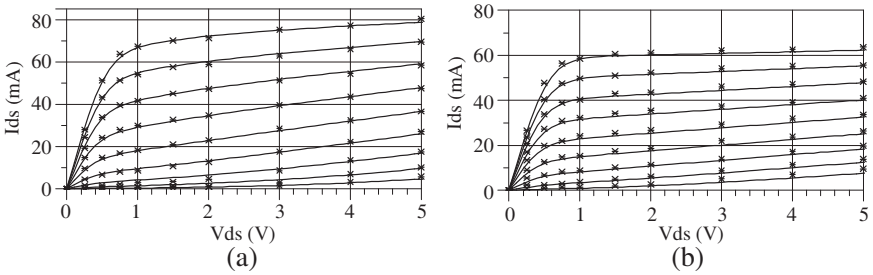

Figure 9. MGF1923 measured (stars) and simulated (solid lines) DC I-V characteristics at (a) $-70°$C, and (b) $+70°$C. V_{gs} range from -1.6 V to 0 V with a voltage step size of 0.2 V.

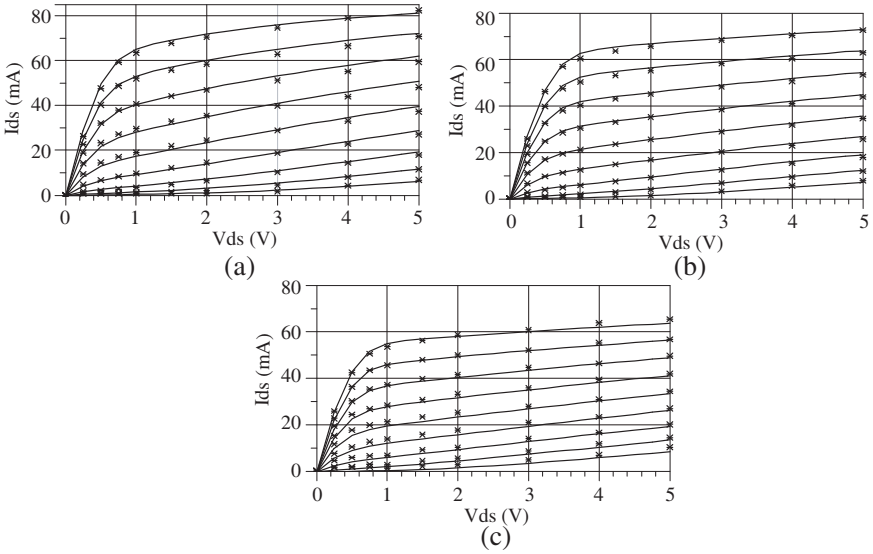

Figure 10. MGF1923 measured (stars) and simulated (solid lines) pulsed I-V characteristics at (a) $-70°$C, (b) $+27°$C, and (c) $+70°$C. V_{gs} range from -1.6 V to 0 V with a voltage step size of 0.2 V.

$+27°$C case the DC bias conditions were $V_{gscc} = -0.6$ V, $V_{dscc} = 3$ V. For the $+70°$C case the DC bias conditions were $V_{gscc} = -1$ V, $V_{dscc} = 2$ V. The results show good agreement between the model and the measured data and this was found to be the case over a wide bias area.

Figures 12 and 13 show the measured and simulated single-tone output power, at the fundamental frequency (fo) and at the higher

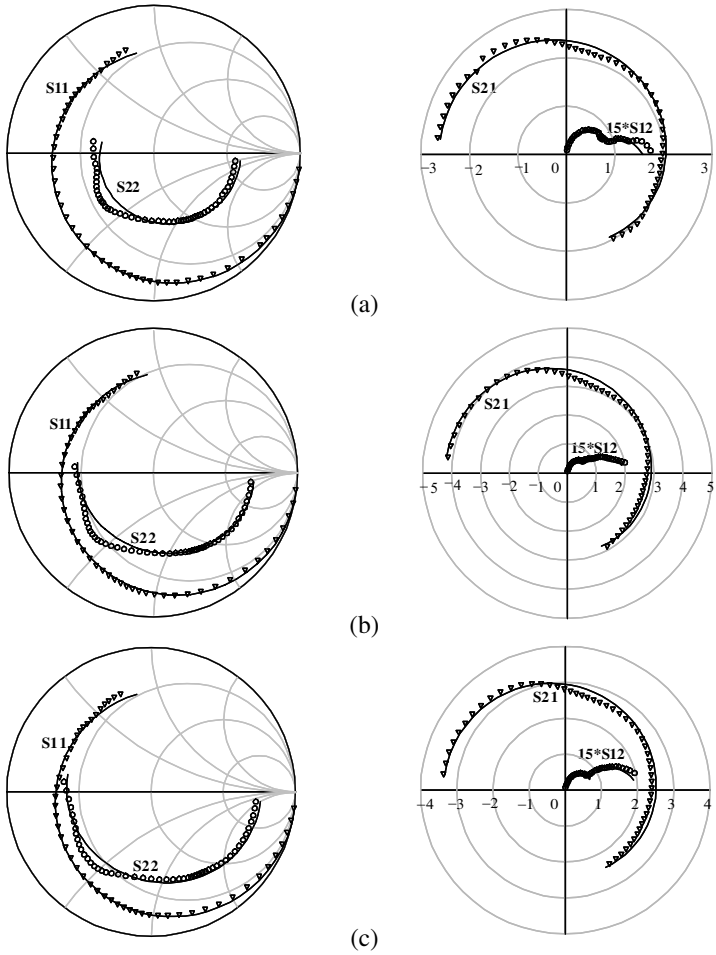

Figure 11. MGF1923 measured (symbols) and simulated (solid lines) scattering parameters over the 0.4 to 15 GHz frequency range at (a) −70°C, (b) +27°C, and (c) +70°C.

harmonic components (second (*2fo*) and third order (*3fo*) harmonic), and gain at three different bias and temperature points. For the −70°C case the DC bias conditions correspond to $V_{gscc} = -1.6\,\mathrm{V}$, $V_{dscc} = 5\,\mathrm{V}$ and the frequency corresponds to 1 GHz. For the +27°C case the DC bias conditions were $V_{gscc} = -0.6\,\mathrm{V}$, $V_{dscc} = 3\,\mathrm{V}$ and the frequency was 5.8 GHz. For the +70°C case the DC bias conditions were $V_{gscc} = 0\,\mathrm{V}$, $V_{dscc} = 3\,\mathrm{V}$ and the frequency was 8 GHz. These results show excellent agreement between the model and the measured data. The results demonstrate the suitability of the model for large-signal applications.

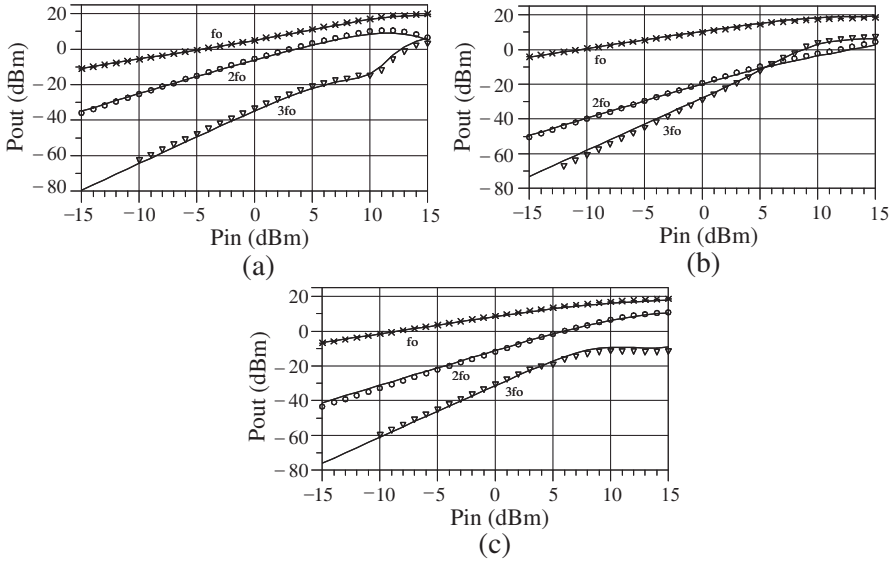

Figure 12. MGF1923 measured (symbols) and simulated (solid lines) output versus input power at (a) −70°C, (b) +27°C, and (c) +70°C.

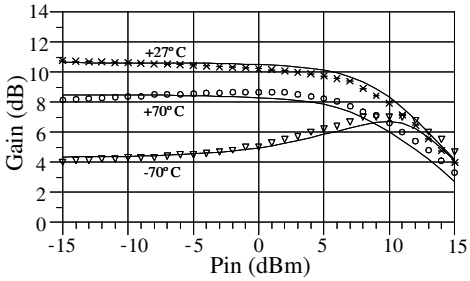

Figure 13. MGF1923 measured (symbols) and simulated (solid lines) gain versus input power at different ambient temperatures.

7. CONCLUSION

A new nonlinear model for low and high power GaAs and GaN devices (MESFETs, HEMTs) which accurately simulates the *I-V* characteristics of the device under static and pulsed conditions over a wide ambient temperature range has been presented. These claims are supported with extensive experimental data acquired under static and dynamic conditions over a broad ambient temperature range.

The results presented demonstrate the ability of the model to simulate thermal and trapping effect on the *I-V* characteristics. The

data presented shows how the model can track the dependence between traps, self-heating and ambient temperature in a relatively simple but accurate manner.

The accuracy of the model when simulating the RF and/or microwave performance of the device at any operating bias and temperature point has also been validated under small-signal and large-signal conditions. Scattering parameters and output versus input power tests, for example, demonstrate the accuracy of the model under these conditions.

The proposed approach combines high accuracy with relatively few model parameters and a simple parameter estimation process. The approach presented can be applied to existing DC models to improve their range of application and accuracy.

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