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QFN-Packaged Highly-Linear Cascode GaN LNA MMIC from 0.5 to 3 GHz

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***Abstract*—A GaN high electron mobility transistor technology with a gate length of 0.25 µm has been used to design and fabricate a cascode broadband low noise amplifier (LNA). The two-stage monolithic microwave integrated circuit (MMIC) with feedback topology yields a bandwidth of 0.5-3 GHz at a constant gain of 35 dB and noise figures of less than 1.5 dB. A third order intercept point (OIP3) of up to 42.5 dBm was measured at 0.8 GHz, with a linear output power of 24 dBm over the full bandwidth. The MMIC was further assembled and measured in a low-cost plastic QFN package on an evaluation board with optimized thermal design and passive cooling. At a power dissipation of ~3 W the packaged LNA yields an OIP3 of 35-38 dBm over the full bandwidth at a noise figure of < 1.9 dB.**

Keywords—GaN; LNA; MMIC;broadband; cascode; linearity; feedback amplifier; mobile communications

I. Introduction

Increasing data rates in mobile communications and high-speed wireless networks require improved spectrum efficiency by a parallel and software defined operation of the wireless infrastructure. This development requires high-performance transceiver hardware capable of flexible and reconfigurable multi-band and multi-standard operation. Highly-linear broadband receivers covering all mobile communication frequency bands are key components of this architecture. Based on Gallium Nitride (GaN) technology, low-noise amplifiers (LNAs) with additional advantages such as high input-power survivability can be used to simplify the architecture of receiver front-ends. The resulting absence of limiters and filters reduces the system complexity and improves the overall noise figure. GaN LNAs offer high linearity in terms of intermodulation and linear output power [1], [2], while low noise figures as low as 0.5 dB [3], and high gain can be realized over a decade bandwidth [4] at mobile communication frequencies. First commercial products are already available today [5]. However, the high linearity of GaN technology is achieved at the cost of power consumption, which needs a design trade-off for both parameters [2], [6].

Nevertheless, the resulting high power dissipation confronts receiver front-end designers with unusual thermal issues and power consumption with noticeable impact on the overall efficiency of a transceiver system. Therefore, the aim of this work was to evaluate the trade-offs between noise figure, linearity, and associated power consumption of a broadband GaN LNA monolithic microwave integrated circuit (MMIC) for applications in mobile communication transceivers. This paper focuses on the performance of a GaN LNA assembled in package environment with emphasis on the realization by using low-cost plastic packages and low-grade substrate materials performed at the restriction of purely passive cooling.

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II. GaN MMIC Technology

The applied GaN-based semiconductor technology uses 3-inch semi-insulating SiC substrates with AlGaN/GaN heterostructure epitaxy grown by metal-organic chemical vapor deposition. The processing is based on a high electron mobility transistor (HEMT) device technology with a gate length of a 0.25 µm designed to operate at a typical drain voltage of 30 V [7]. These devices yield a transconductance of 330 mS/mm and a maximum drain current of about 1 A/mm with cut-off frequencies of higher than 30 GHz (f_T) and 42 GHz (f_{max}), a minimum noise figure (NF) as low as 0.85 dB at 10 GHz and a typical output power of 5 W/mm at 10 GHz and 55% power added efficiency. The GaN process includes full MMIC capability, comprising thin film resistors, MIM capacitances, substrate via-holes and wafer thinning to a thickness of 100 µm. The presented amplifier circuit is designed in microstrip transmission line technology.

III. LNA MMIC Design

The LNA was designed for applications in mobile communication receivers in the frequency range of 0.5-2.7 GHz with an objective of high gain (> 30 dB), high linearity (OIP3 of 38 dBm), input and output matching of better than 10 dB, and lowest possible noise figure. The MMIC consists of two amplifier stages with resistive feedback topology both using cascode transistors. Each cascode consists of a pair of HEMTs with a gate width of 0.48 mm (0.96 mm total MMIC gate periphery). The cascode configuration provides a high gain per stage as well as high reverse isolation and high output impedance. The schematic diagram of the two-stage amplifier is shown in Fig. 1.

The design strategy has been to optimize the first stage of the amplifier for a trade-off between minimum noise figure and good input matching to 50 Ohm, and the second stage for gain, high linearity and maximum output power compression. Both

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stages use parallel feedback, which provides the advantage of increasing the stability factor, improving input and output return losses and a flat gain behavior over a wide bandwidth. A pair of 1700 Ohm thin-film resistors and 19 pF capacitors are used in the layout-symmetric feedback loop of the first stage, while a pair of 880 Ohm thin-film resistors and 2.5 pF capacitors in the second stage. Additionally, the first stage uses inductive source degradation for simultaneous low-noise and impedance matching. The interstage network was designed to convert the input of the second stage directly to the required load impedance of the first. The output matching network provides matching for high linearity and output power compression from 50 Ohm environment. All DC-bias and matching networks are realized fully on-chip to allow an easy practical use of the chip with minimized external passive RF components. However, this requires large area RF de-coupling capacitors and high-density spiral inductors (up to 11 turns) due to the low operation frequency of the circuit. In order to simplify transceiver systems using this LNA the cascode voltage is generated on-chip by a DC voltage divider, however, with the possibility to apply also and an external cascode bias. Furthermore, the gate and drain bias voltages for both stages are intentionally identical to reduce the required bias circuit complexity. Note that an individual gate and drain bias per stage will significantly improve the overall power consumption without any trade-off in linearity. Fig. 2 shows a photograph of the compact GaN MMIC LNA.

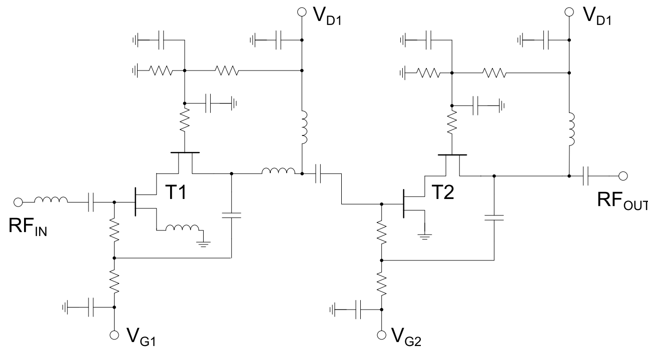

Fig. 1. Simplified schematic of the cascode GaN MMIC LNA.

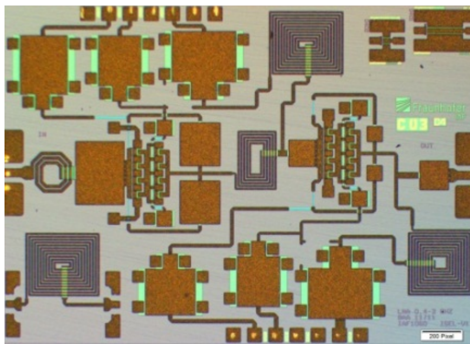

Fig. 2. Die photograph of the LNA MMIC (size: 3.5x2.5 mm^2).

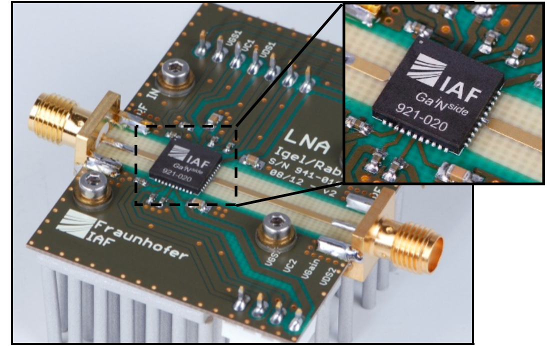

Fig. 3. Plastic QFN packaged GaN LNA MMIC in low-cost evaluation board using FR4 PCB material (4x5 cm^2).

IV. Plastic Package Integration and LNA Evaluation Board

The goal of this work is to demonstrate the feasibility of GaN LNA performance with high linearity by using low-cost packaging and assembly materials. The MMIC was packaged in a standard quad flat no-lead (QFN) plastic package (7x7 mm^2) with copper lead frame. The die was soldered to the thermal ground pad and additional in-package decoupling capacitors of 150 pF per bias line were included in the package. Based on a fully in-house assembly a ceramic lid instead of plastic overmolding has been used. The LNA evaluation board was designed using standard low-grade FR4 printed circuit board (PCB) material and was thermally optimized in order to allow an operation at various power consumption levels with the restriction to use solely passive heat sinking. Additionally, the PCB comprised a simple external decoupling network using only a small number of low-frequency surface mount device (SMD) capacitors. A photo of the packaged chip and the full board are shown in Fig. 3.

V. Simulation and Measurement Results

Measurements of the LNA were performed both on-wafer and on evaluation board level with packaged MMIC. For the module all data are taken at the coaxial connector reference plane without any further de-embedding to the chip and without any additional cooling measures.

A. S-Parameters and Noise Figure

A good agreement of measured and simulated S-parameters was achieved with minor influence due to the packaging (Fig. 4). An input and output matching of better than 10 dB and a flat gain of ~35 dB was realized over an operation bandwidth from 0.5 to 3 GHz. A noise figure (NF) smaller than 1.5 dB was measured on-wafer through this bandwidth, with a minimum value as low as 1.25 dB at 1.8 GHz (Fig. 5). However, an increased NF of < 1.9 dB, with a minimum of 1.6 dB, and an 1-2 dB lower gain were measured for the packaged LNA in the evaluation board at the same bias of 30 V and 150 mA (4.5 W dissipated power).

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To identify the root course of the measured influence on performance, infrared scope investigations of the packaged MMIC on the evaluation board and on-wafer temperature-dependent noise figure measurements have been performed under the above mentioned bias conditions. Based on this measurement data (Fig. 5), we identified a temperature increase of the chip of about +50°C from on-wafer to packaged chip on the evaluation board as the main origin. The importance of these constrains for the practical implementation of GaN LNAs will be further discussed in the end of this paper.

B. *Linear Output Power and Input Power Survivability*

To determine the output power characteristics on-wafer large signal measurements of the MMIC have been performed. The frequency dependence of the linear output power (P_{1dB} compression point) extracted from power sweep measurements is shown in Fig. 6. At 30 V drain bias a flat P_{1dB} as high as 24 dBm was achieved over the bandwidth, which slightly reduces to about 22 dBm for 15 V bias. A representative power sweep measurement at 3 GHz and 30 V including the gain compression behavior is shown in Fig. 7. The measurement was performed up to an input power of 0 dBm, where a slight increase of the gate current appears indicating a first limit of a safe operating area of the applied HFET devices.

In the presented design, the specific gain compression behavior of GaN cascode transistors [8] is used to realize an extended input power survivability without causing any gate current. With this technique, the cascode LNA achieves a satisfactory trade-off between gain, P_{1dB} and input power survivability. The presented LNA MMIC shows an input power survivability (0 dBm), which is at least 10 dB above the input power where P_{1dB} was found. Further survivability tests may extend these power limits, depending on destructive and degradation mechanisms due to gate-source and gate-drain diode currents under higher gain compression.

C. *Two-Tone Linearity Characterization*

Furthermore, two-tone linearity measurements have been performed on-wafer (tone spacing of 5 MHz). Fig. 8 and Fig. 9 illustrate the bias-dependent third-order intercept point (OIP3) at two mobile communication bands of 0.8 GHz and 2.1 GHz. It is important to notice that for a defined current, an increase in drain voltage does not increase the OIP3 beyond a specific value, and vice versa. Therefore each target value in OIP3 results in a minimum associated power consumption. At 0.8 GHz an OIP3 of up to 42.5 dBm was measured, which decreases to 40 dBm at 2.1 GHz, both at a bias of > 25 V and a drain current of 300 mA.

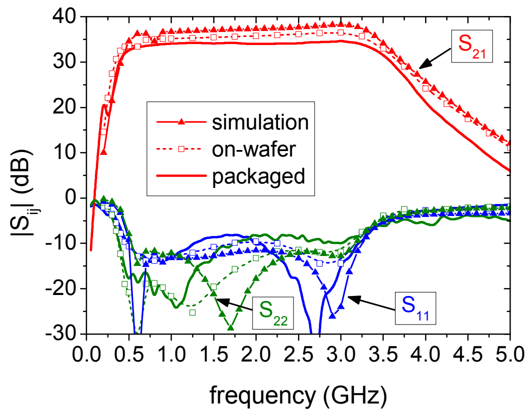

Fig. 4. S-parameter performance simulated and measured on-wafer and in package at a bias of 30 V and 150 mA.

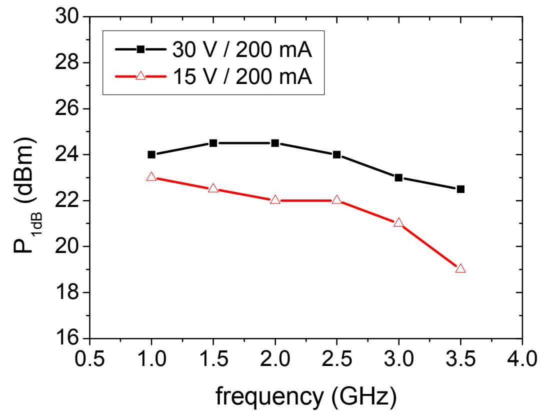

Fig. 6. On-wafer measured linear output power (P_{1dB}) versus frequency for a drain bias of 30 V and 15 V at 200 mA drain current.

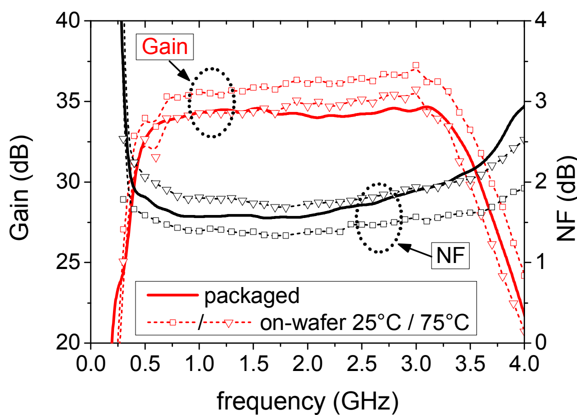

Fig. 5. Gain and noise figure (NF) measured in-package and on-wafer at 25°C and 75°C backside temperature (30 V, 150 mA).

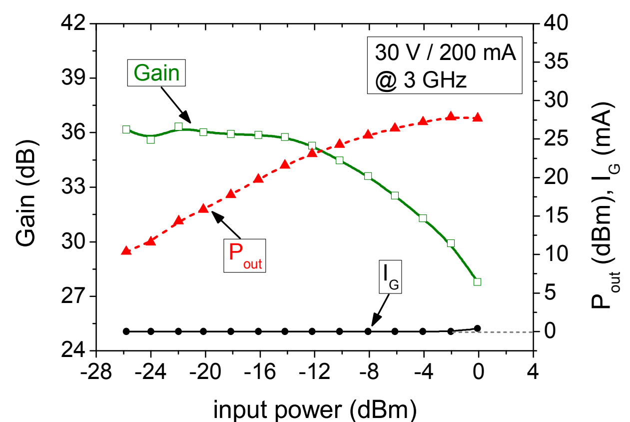

Fig. 7. On-wafer measured gain, output power (P_{out}) and gate current (I_G) for a input power sweep up to 0 dBm input power at 3 GHz and 30 V bias.

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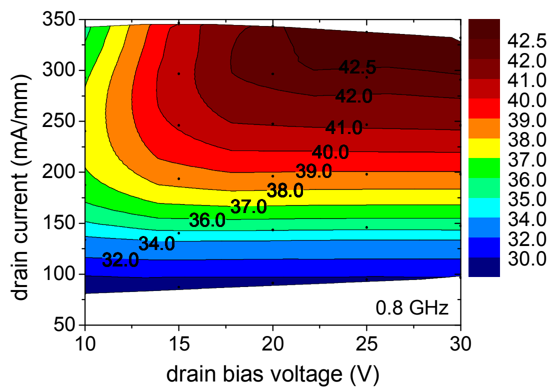

Fig. 8. Third-order intercept points (OIP3) extracted under various bias conditions from on-wafer measurements at 0.8 GHz.

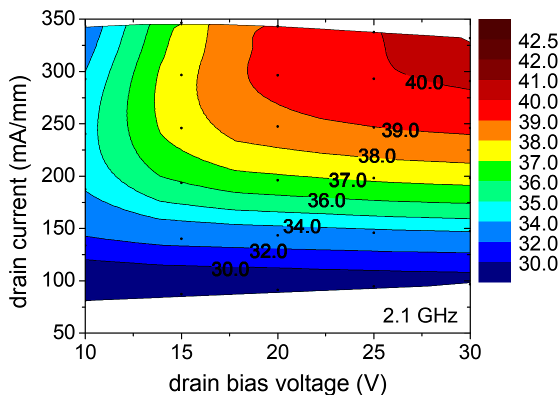

Fig. 9. Third-order intercept points (OIP3) extracted under various bias conditions from on-wafer measurements at 2.1 GHz.

Fig. 10 shows the behavior of OIP3 versus frequency for different bias conditions and the influence of packaging. It can be seen, that a high power dissipation increases the difference in linearity from on-wafer to packaged MMIC, due to higher channel temperature, however, with low impact at the high frequency band performance. An OIP3 in-package of 35-38 dBm over a bandwidth from 0.5-3 GHz was measured at a trade-off bias of 15 V and 200 mA. Finally, Table I compares all discussed results with recently published works.

VI. Conclusions

A plastic QFN-packaged two-stage cascode LNA MMIC in a low-cost evaluation board without additional passive RF components demonstrates the feasibility and challenges of GaN for high-linearity broadband LNAs for wireless mobile communication receivers. The module yields a NF of < 1.9 dB and OIP3 of 35-38 dBm over a bandwidth of 0.5-3 GHz. We showed that the packaged MMIC is mainly thermally limited due to a degraded NF and OIP3 at increased chip temperatures, caused by power dissipation in the assembled receiver module. The high power consumption is an inherent challenge for GaN low noise circuits with high linearity. Consequently, a trade-off for high linearity with minimized power dissipation, noise figure, as well as an optimized thermal design and is essential for a practical use of highly-linear GaN-based LNAs.

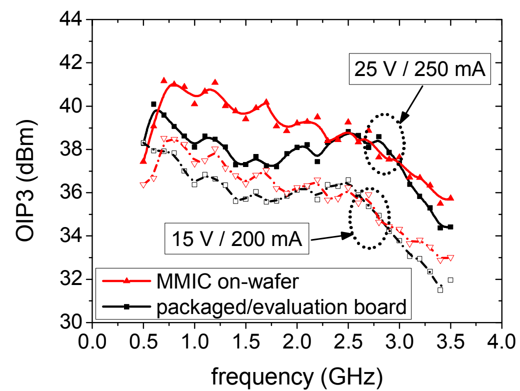

Fig. 10. Third-order intercept points (OIP3) versus frequency measured on-wafer and in-package at different bias points.

TABLE I
Comparison of State-of-the-Art Highly Linear GaN and GaAs LNAs.
*Requires External Passive RF Components

Ref	freq [GHz]	NF [dB]	Gain [dB]	OIP3 [dBm]	P_{1dB} [dBm]	P_{DC} [W]	Type
[2]	0.3-3.0	< 1.3	20.0±1.0	37-43	30.5	2.0	MMIC*
[2]	0.3-3.0	< 2.8	20.0±1.0	49-52	37-39	20	MMIC*
[4]	1.0-4.0	< 2	17.5±0.5	/	20	1.2	MMIC
[5]	2.5-4.5	< 2	27.0±3.0	39-41	/	/	MMIC
[9]	1.7-2.7	< 1.2	31.0±2.5	36-40	24	0.8	Package*
This work	0.5-3.0	< 1.5	34.5±1.5	39-42	24	6.3	MMIC
This work	0.5-3.0	< 1.9	33.0±1.0	35-38	22	3.0	Package

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