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Buck-Plus-Unfolder as the Superior Active Power Decoupling Solution for 400 Vdc/kW-Level Applications

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ABSTRACT In single-phase ac/dc applications where reliability and/or power-density are critical, active power decoupling (APD) circuits can be employed to reduce the required capacitance on the dc-link. Various APD circuits have been proposed so far, all with their advantages and disadvantages. However, many confusions still exist in the literature on this topic which is mainly attributed to a lack of unified and comprehensive assessment criteria. In this paper, first the decisive criteria for a modern APD circuit are established, and the buck APD is identified as the current state-of-the-art, based on them. Then the buck-plus-unfolder topology with triangular current mode (TCM) modulation is proposed as an improvement, and a simple, yet solid foundation is introduced to choose the superior decoupling solution at different specifications. The operation equations for the APD with TCM modulation are derived next, and the operation of the proposed solution is demonstrated using a hardware prototype.

INDEX TERMS Active power decoupling, double line frequency ripple, power density, single-phase PFC, single-phase inverter, triangular current mode (TCM).

I. INTRODUCTION

It is well known that in single-phase ac/dc converters that achieve unity power factor at the ac-side, the power waveform contains a large component pulsating at the double-line-frequency (DLF). This DLF ripple power can have adverse effects on the load in different applications, including battery chargers, fuel cell systems, PV inverters, and LED drivers.

In order to prevent it from flowing into the load, the DLF ripple power can be mitigated by directly connecting bulk capacitors to the dc-link. However, in this method, called passive power decoupling (PPD), the voltage across the capacitor is the same as the dc-link voltage which contains a large average value with very small variations. Consequently, there is always a large amount of redundant energy stored in the capacitor, and only a small portion of its energy storage capability is utilized to deal with the DLF ripple. As a result, passive power decoupling requires large values of capacitance to be used. For 400 Vdc/kW-level applications, it can be only realized using large values of electrolytic capacitors, resulting in low power-density and low reliability.

For instance, a 6.6 kW modern ac/dc converter using PPD can be found in [1]. Although several efforts have been made to reduce the volume of the main converter, the large capacitor bank still occupies around 25% of the whole converter's volume, making it worthy of notice as one of the major remaining bottle-necks for further power-density improvements.

For applications in which power-density and reliability are more critical and the hold-up time is unnecessary, an alternative solution is using active power decoupling (APD) [2]. In APD, as shown in Fig. 1, the capacitor is separated from the dc-link by means of a power electronic converter. Consequently, the voltage across the capacitor can have large variations while the dc-link voltage remains constant. Larger capacitor voltage variations imply that a larger portion of the capacitor's storage capability is utilized to deal with the DLF ripple. As a result, a smaller capacitance value can be used for the same amount of power being processed.

As explained in [3], the underlying condition to realize APD is

$$C_b v_{cb}(t) \frac{d v_{cb}(t)}{dt} = P_o \sin(2\omega_0 t), \tag{1}$$

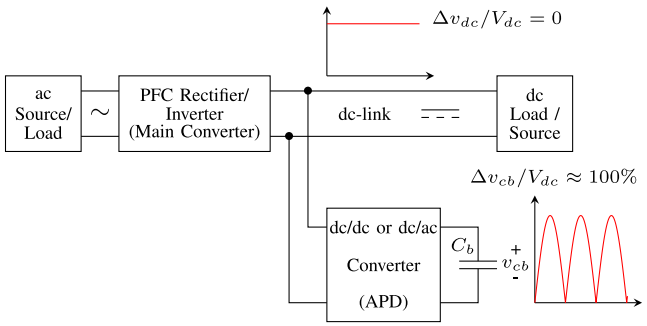

FIGURE 1. Schematic view of active power decoupling.

which equates the power drawn by the buffer capacitor, on the left-hand side, to the DLF ripple power that needs to be absorbed, on the right-hand side. In this equation, C_b and $v_{cb}(t)$ are the buffer capacitor value and the voltage across it, and P_o and ω_0 are the main converter's output power and ac-line angular frequency, respectively.

One set of the answers for (1) can be obtained as

$$C_b = \frac{(K+1)P_o}{\omega_0 V_{cb(\max)}^2} \triangleq \frac{K+1}{2} C_{b(\min)}, \quad K \geq 1 \tag{2a}$$

$$v_{cb}(t) = \sqrt{\frac{V_{cb(\max)}^2}{K+1}(K - \cos(2\omega_0 t))} \tag{2b}$$

$$i_{cb}(t) = \frac{P_o \sin(2\omega_0 t)}{\sqrt{\frac{V_{cb(\max)}^2}{K+1}(K - \cos(2\omega_0 t))}}, \tag{2c}$$

in which $V_{cb(\max)}$ is the determined maximum value of the voltage across the capacitor. These equations state that in order to achieve APD, it would be enough to choose the buffer capacitor as given in (2a), and use the APD converter to form its voltage according to (2b) (or equally form its current as (2c)). Since the capacitor voltage is a dc waveform—hence the name dc-decoupling—a dc/dc converter can be employed for this purpose. The synchronous buck topology shown in Fig. 2(a) is the simplest converter that can be used for dc-decoupling [3]–[9].

In (2a)-(2c), there is one degree of freedom provided by the parameter K, which exists in the equations as a result of the integration constant. As can be seen in Fig. 2(b), when K = 1, the capacitor's voltage charges up to its maximum allowable value and then drops back all the way to zero, implying full utilization of the capacitor's energy storage capability to deal with the DLF ripple. However, as K gets larger, the capacitor's voltage only drops back to larger values, implying there is always some redundant energy remaining in it. Although K is commonly known as the "energy storage margin," it is preferred in this paper to call it "energy redundancy index" to emphasize on its negative aspect. As is expected, having a higher energy redundancy index requires using larger capacitors for the same amount of power being processed—which is also evident in (2a). The theoretical minimum possible value of

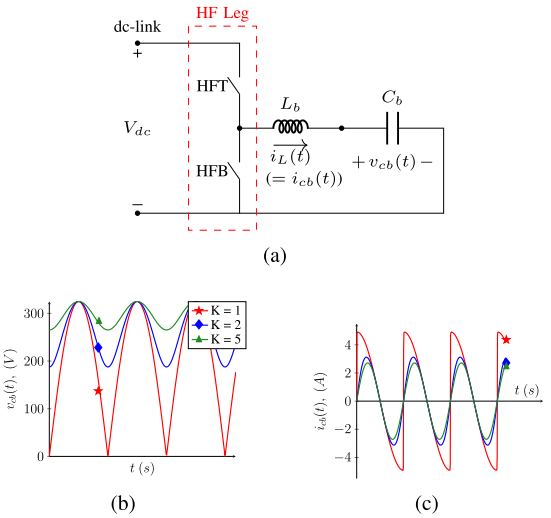

FIGURE 2. DC-Decoupling using buck converter: (a) topology and buffer capacitor (b) voltage and (c) current waveforms.

capacitance, $C_{b(\min)}$, can then be used when K has its smallest allowable value, K = 1.

However, a major problem with buck APD is that for the case of full capacitor utilization, K = 1, the capacitor's current waveform contains sharp edges, as can be observed in Fig. 2(c). These sharp edges contain infinite higher-order harmonics, introducing challenges from control point-of-view [10]–[15]. Therefore, to use the simple buck APD, there is no way but to settle for using larger-than-optimum capacitor values with K > 1.

In addition to (2), Equation (1) has another unique solution as

$$K = 1 \Rightarrow C_b = C_{b(\min)} \tag{3a}$$

$$v_{cb}(t) = V_{cb(\max)} \sin(\omega_0 t) \tag{3b}$$

$$i_{cb}(t) = \frac{2P_o}{V_{cb(\max)}} \cos(\omega_0 t). \tag{3c}$$

This solution is called ac-decoupling because of the ac capacitor waveform. Since the capacitor's voltage is bipolar in this case, it cannot be realized using a dc/dc converter such as buck, and an inverter is needed to convert the dc-link voltage to the required ac waveform across the capacitor. A full-bridge inverter using sinusoidal pulse-width modulation (SPWM), shown in Fig. 3(a), is the simplest converter that can be used for this purpose [16].

As can be observed in Fig. 3(b) and (c), in ac-decoupling, full capacitor utilization can be achieved while having smooth sinusoidal current waveform, enabling closed-loop implementation of this solution while maintaining K = 1.

The problem with using the full-bridge topology for ac-decoupling is that the additionally required switching leg almost doubles the losses and increases the overall cost and volume. Therefore, it does not provide a reasonable alternative for the buck APD.

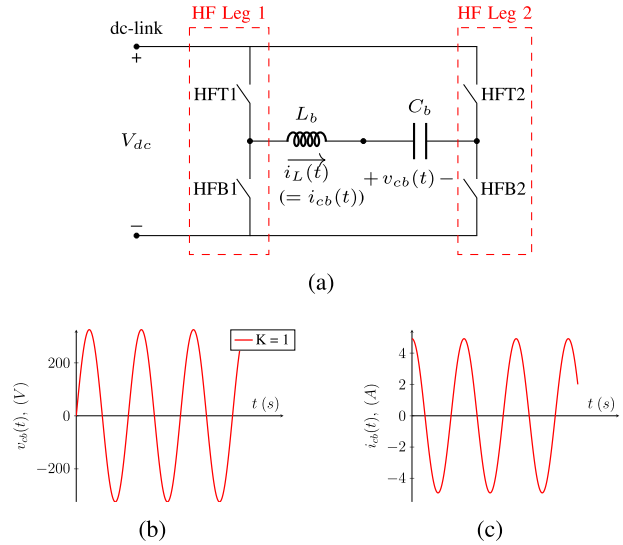

FIGURE 3. AC-Decoupling using full-bridge converter: (a) topology and buffer capacitor (b) voltage and (c) current waveforms.

As will be discussed in Section II, several other solutions have been introduced in the literature so far. In spite of having a number of review papers in this area [2], [17], [18], still some contradictory arguments can be found among some of the different literature. A major intended contribution of this paper is to establish a simple and solid criteria and use it to classify the previous literature, in order to reduce the confusion that could be previously found among them. It will be argued that despite having all of these solutions, the buck APD can still be considered as the current state-of-the-art. Buck-plus-unfolder using triangular current mode (TCM) modulation will then be proposed as a superior improvement. In Section III, this proposed solution will be compared to the buck APD from the efficiency and power density perspectives, and a procedure for choosing the best APD solution will be introduced. As the TCM modulation has been never elaborated for APD circuits in any of the previous literature, Section IV includes some of the important control design details for the proposed solution, including explanations on deriving the equations for TCM soft-switching operation. In Section V, the experimental results used to verify the operation of a hardware prototype developed based on this solution are included. Finally, Section VI draws the conclusion by summarizing the main contributions of this work.

II. STATE-OF-THE-ART AND THE PROPOSED SOLUTION

A. ESTABLISHING THE DECISIVE CRITERIA

Before reviewing the other APD solutions introduced in the literature, a criteria is established based on the three requirements that are believed to be of critical importance, given the recent advances in power electronics.

First, the APD is preferred to be controlled independently from the main converter (PFC or inverter). As will be discussed in Subsection II-B, there are a group of APD solutions, called dependently-controlled topologies, that allow gaining benefits by sharing switches between the main converter and the APD. However, their problem is that they apply the restriction of using a certain topology and control strategy for each combined main converter+APD solution. With the advent of wide bandgap (WBG) devices, many topologies have gained more desirability, including the totem-pole rectifier topology [19], [20]. Additionally, as switching frequency limits are getting increased, soft-switching control methods are gaining more importance. Using dependently-controlled APDs, these modern topologies and modulation methods cannot be used in the main converter, and hence they are not preferred for modern, practical applications.

Second, it is preferred that the maximum allowable voltage across the buffer capacitor, $V_{cb(\max)}$, is smaller than the dc-link voltage, V_{dc}. This requirement is established assuming the application adopts the commonly used 400 V nominal dc-link voltage. The commercially available GaN switches are rated at 650 V at maximum, which are designed to ensure enough voltage margin for 400 V applications. If the voltage across the buffer capacitor is expected to regularly exceed $V_{dc} = 400\ V$, these superior GaN switches [21] cannot be used anymore, and the choice will be limited to other types of switching devices such as Si and SiC MOSFETs or IGBTs.

Additionally, among the solutions that satisfy both of the above-mentioned requirements, it is preferred to use the minimum possible value of buffer capacitance, and preferably achieve the optimum capacitance requirement. This preference will obviously result in a higher overall converter power-density and reliability.

In summary, there are three qualities that are important in APD converters used in 400 Vdc/kW-level applications:

- Requirement (I): Be controlled independently from the main converter
- Requirement (II): The maximum voltage in the APD be less than the dc-link voltage
- Preference (III): Among the solutions that satisfy requirements (I) and (II), it is preferred to achieve the minimum possible required buffer capacitance.

B. IDENTIFICATION OF THE STATE-OF-THE-ART

Buck topology is not the only converter that can be used for dc-decoupling. If the buck converter discussed in Section I is replaced with a boost or buck-boost converter, Equation (2) still holds. Based on (2a), using boost-based [22]–[25] or buck-boost-based [26] APD solutions, the capacitance requirement can then be reduced further as the maximum allowable voltage across the capacitor, $V_{cb(\max)}$, can be increased beyond the dc-link voltage. This case, however, is not preferred as it fails to meet requirement (II).

A unique family of solutions found in the literature includes the split-capacitor solutions [13], [14], [27], [28] which use a split configuration of two capacitors connected to the dc-link to absorb both of the high-frequency and low-frequency ripples. However, as can be found in [13] and [14], the required capacitance value for each of the two capacitors in

this topology is $C_f = \frac{4P_o}{\omega_o V_{dc}^2}$, which is twice the minimum capacitance requirement shown in Equation (2a), given that $V_{cb(\max)}$ is allowed to get close enough to V_{dc}. Therefore, the total required capacitance in this solution is 4 times larger than the minimum capacitance requirement in single-capacitor solutions, and hence they fail to satisfy preference (III).

Another group of solutions, as explained previously, try to offer attractive alternatives by sharing some of the switches between the main converter and the APD, such as the example shown in Fig. 4(c). However, these dependently-controlled solutions [10]–[12], [29]–[33] are also not preferred in here as they reject requirement (I).

Additionally, besides the solutions that use capacitors to store the DLF ripple, there is another group of APD solutions in which an inductor is used for this purpose [15], [29], [34], [35], as shown in Fig. 4(d). Since inductors have large sizes and losses when they are used to store low-frequency power, these solutions can end up being bulkier and heavier than the capacitor-based counterparts.

By ruling out the other alternatives according to the above-mentioned arguments, the two remaining solutions are the basic buck and SPWM full-bridge introduced in Section I. On one hand, there is the simple dc-decoupled buck APD that has small losses but cannot achieve the minimum capacitance requirement; on the other hand, there is the ac-decoupled full-bridge solution that achieves the optimum capacitance requirement, but at the expense of much higher losses. Since the capacitance required by the buck is not significantly larger than the theoretically minimum value, it can be assumed that the buck APD also meets all of the three requirements. As these requirements are met without significant losses—as opposed to the SPWM-full-bridge—the buck APD is identified as the state-of-the-art APD solution, based on the criteria established in this paper.

These arguments can be attested by the results of the recent Google's Little Box Challenge, as a practical application, in which 4 out of the 7 finalist teams that used APD, including the contest winner, were using synchronous buck for this purpose [36].

C. PREVIOUS ATTEMPTS TO IMPROVE THE BUCK APD

It was shown in the previous subsection that buck can be considered as the current state-of-the-art APD solution. However, it still has the problem of not being able to meet the theoretical minimum capacitance requirement; any attempt to solve this problem may potentially improve its power-density. In addition to this reduction of component values, reduction of the components count is another possibility that can be considered. Besides the generally possible improvements such as enhanced layout design that can be applied to every converter, these are the only two (at least readily) imaginable ways to improve this state-of-the-art, from the circuit topology point of view.

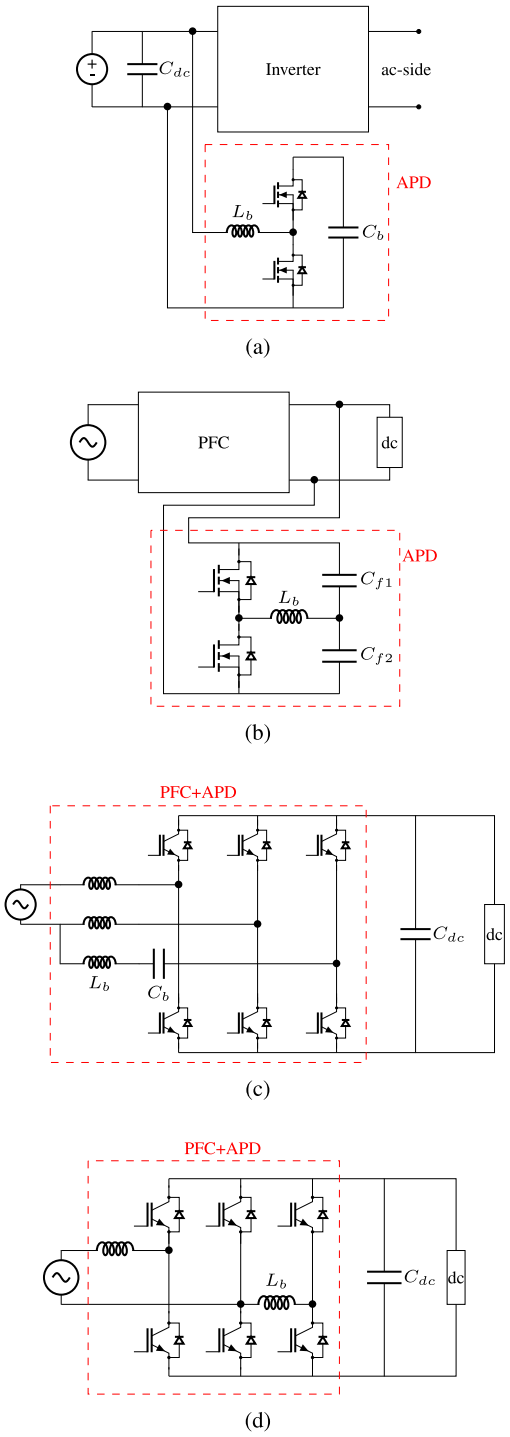

FIGURE 4. Examples for the different mentioned APD categories: (a) boost-based [22], [23], [25], (b) split-capacitor [13], [14], (c) dependently-controlled [10], [11], and (d) Inductive [29], [34].

In fact, both of these two possibilities have been already considered in the literature. To investigate how the mentioned literature have addressed the buck APD and potential improvements for it, they are re-organized into the following four categories.

In the first group, without having the buck being mentioned, other solutions are used, including inductive [29], [34],

dependently-controlled [29], [30], boost-based [22], [23], split-capacitor-based [27], [28], or full-bridge [16] solutions. Based on the previous explanations, these solutions are not preferred according to the proposed evaluation metrics.

In the second group, the buck APD is mentioned and alternatives are proposed by addressing problems other than its inability to achieve full capacitor utilization. For instance, in [31]–[33], it is tried to reduce its component count. However, as expected, the only way to achieve this purpose is to use dependently-controlled switch-sharing methods, because of the buck's simple topology. In a number of other publications, other problems are cited and either inductive [35] or boost-based [24], [25] solutions are proposed.

The third group of the literature suggest solutions by addressing the inability of buck APD to achieve the minimum capacitance requirement. However, the split-capacitor solution [13], [14] ends up requiring even larger capacitance than the buck does, and the other solutions of this group are dependently-controlled [10]–[12] or inductive [15].

Consequently, in the fourth group of the literature [3]–[9], it is accepted to settle for the buck APD, in order to avoid the disadvantages of the other alternatives.

In summary, based on the three criteria suggested by this paper, buck APD is identified as the current state-of-the-art, in spite of its inability to use the minimum capacitance requirement. Even though many interesting alternatives have been proposed so far, they are not considered to be preferable in this paper, as they point back to the same previously-rejected solutions. These arguments are summarized in Fig. 5.

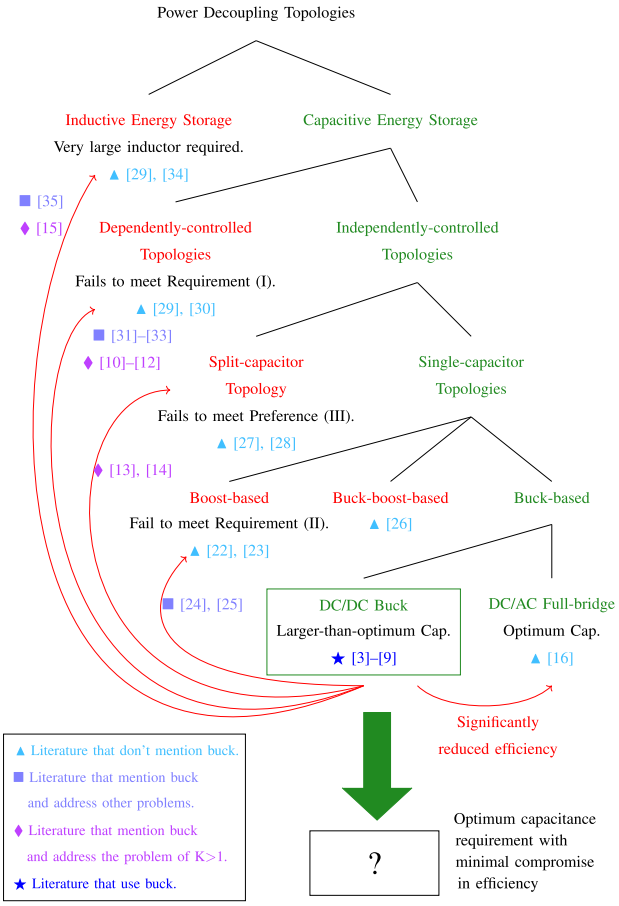

FIGURE 5. Summary of different active power decoupling solutions and identification of the state-of-the-art.

D. THE PROPOSED SOLUTION

In this paper, the buck-plus-unfolder topology [37] with TCM modulation [38]–[40] is proposed as a superior alternative to the buck APD. Although this topology has been known for many years, it has never been used in APD applications. The underlying idea is to use a low-frequency (LF) unfolder leg to extend the operation of the two-quadrant buck APD to four-quadrant operation.

The two operation modes of this topology can be seen in Fig. 6. The unfolder leg is switched at the line frequency. During the positive capacitor voltage half-cycles, the LF bottom switch (LFB) is ON, while negative values of capacitor voltage are enabled by turning the LF top switch (LFT) ON.

Since the capacitor's voltage can be bipolar in this case, unlike the buck APD, ac-decoupling can be achieved, which allows using the theoretical minimum capacitance requirement (preference (III)). Additionally, both of the requirements (I) and (II) are satisfied as well.

In contrast to the SPWM full-bridge, these three requirements are met with insignificant compromise in efficiency. Since the high-frequency (HF) leg is switched independently from the LF-leg, it can still be controlled using the soft-switched TCM modulation, keeping the HF-leg's switching losses low. Also, as the LF-leg is only switched at the line frequency, the added switching losses are negligible. Low-$R_{ds(on)}$

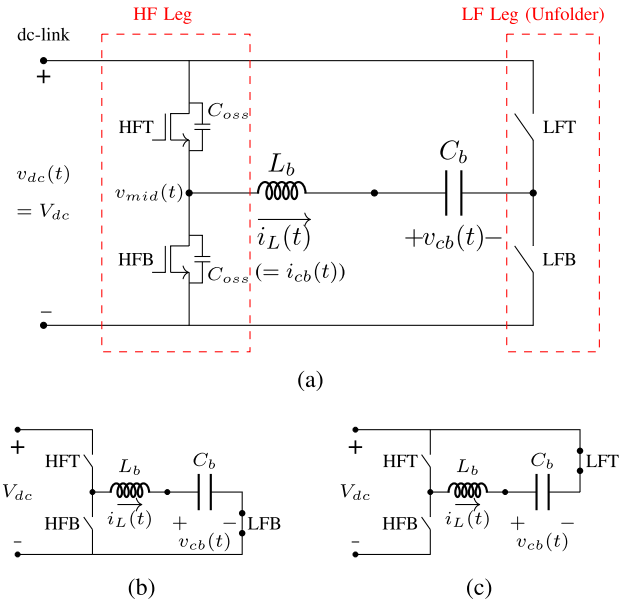

FIGURE 6. The proposed APD solution: (a) topology and the operation modes during (b) positive and (c) negative $v_{cb}(t)$ half-cycles.

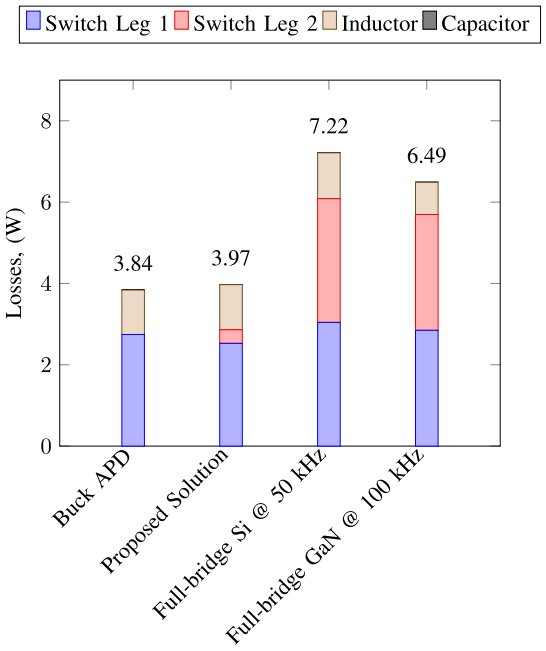

FIGURE 7. Comparison of the breakdown of the calculated losses between the buck, the proposed, and the SPWM-full-bridge APD solutions (capacitor losses are invisibly small).

TABLE 1. Assumed Converter Specifications

Main converter rated power	P_o	800 W
Amplitude of the ripple power	$\hat{P}_r(=P_o)$	800 W
Line frequency	f_0	60 Hz
DC-link voltage	V_{dc}	400 V
Nominal maximum capacitor voltage	$V_{cb(max)(nom)}$	325 V
Mean capacitor voltage for buck	$V_{cb(mean)}$	280 V

switches can be used for the LF-leg, additionally, to ensure that its conduction losses are insignificantly small as well.

III. BENEFITS ASSESSMENT

A. EFFICIENCY POINT OF VIEW

To investigate the claims made at the end of the previous section in a quantitative manner, the efficiencies of the buck, SPWM full-bridge and the proposed solution are calculated and compared in Fig. 7. Other solutions have been ruled out from the comparison as they fail to meet some of the previously-discussed three requirements (among the compared ones, full-bridge and the proposed solution meet all of the requirements, and buck nearly satisfies preference (III)).

These calculations are carried out assuming the specifications shown in Table 1 and using the components listed in Table 2, which are currently available high-performance components with moderate prices. The custom inductor is designed using the K_g method [41]. Also, the switching frequencies chosen for the two full-bridge cases are determined optimally using simulations at different switching frequencies.

TABLE 2. Components Used in the Converter Designs

HF switching leg	LMG3410-HB-EVM
LF switching leg	STY105NM50N+UCC27712DR+auxiliary components
Inductor	N49, PQ40/40 Core, 58 turns of AWG14 copper wire
Capacitor	C5750X6S2W225K250KA capacitors in parallel

It is emphasized that these calculations are performed using some components as benchmark components and their equivalent models. In practice, values of losses will obviously vary slightly depending on multiple design factors. However, these calculations can still provide a good insight on how the mentioned solutions compare to each other in terms of efficiency.

It is verified that while the losses in the full-bridge topology are almost twice that of the buck APD, the added LF-leg in the proposed solution introduces negligibly small additional losses.

B. POWER-DENSITY POINT OF VIEW

It was shown that unlike the full-bridge topology, the proposed solution can be a potential alternative for the buck APD, as it is almost the same as the buck in terms of efficiency. However, another major converter-level index of interest is the power-density. The proposed solution saves up some volume as a result of achieving the minimum capacitance requirement. However, this benefit is gained at the expense of the additionally required volume to accommodate the LF-leg. Therefore, it becomes necessary to evaluate whether this reduction in capacitance requirement would translate into a higher power-density in overall, or not.

For the same specifications, the only two modules that are different between the buck APD and the proposed solution are the capacitor-bank and the LF-leg circuitry (including the switches and their required sensing and driving circuitry). Consequently, the other parts of the two converters can be considered as two black-boxes with similar sizes:

$$V_{buck} = V_{bbox} + V_{C,buck} \tag{4a}$$

$$V_{proposed} = V_{bbox} + V_{C,proposed} + V_{LF,proposed}, \tag{4b}$$

in which V_{bbox}, the volume of the common black box, incorporates all of the common modules among the two of them:

$$V_{bbox} = V_{HF} + V_L + V_{control} + V_{protection} + \cdots. \tag{5}$$

In this case, the power-density comparison will be reduced to a simple trade-off between the volume saved by the reduced capacitor requirement and the lost volume as a result of the LF-leg:

$$V_{buck} - V_{proposed} = (V_{C,buck} - V_{C,proposed}) - V_{LF,proposed}. \tag{6}$$

The capacitance requirements for the buck APD and the proposed solution were shown in (2a) and (3a), respectively.

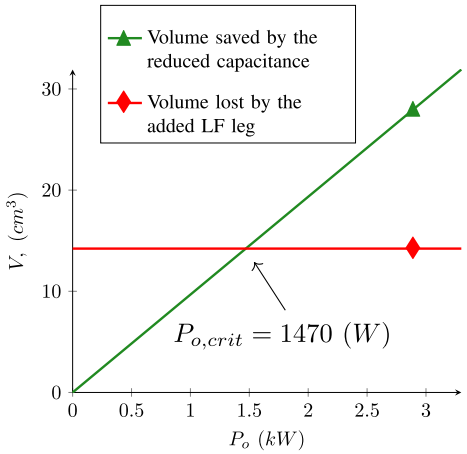

FIGURE 8. Identification of the beneficial range of power for the specific "design" of the proposed solution.

By subtracting these two equations, it can be realized that the reduction in the capacitance requirement is linearly proportional to the output power:

$$C_{buck} - C_{proposed} = \alpha P_o. \tag{7}$$

Assuming that the capacitor-bank is built up by connecting capacitors in parallel, its volume would be a staircase function ascending as each capacitor is added to the capacitor-bank. By employing small ceramic capacitors to build up the capacitor-bank, the explained staircase volume function is increased by tiny increments, which can be approximated as being linearly proportional to the output power:

$$V_{buck} - V_{proposed} \approx \beta C_{buck} - \beta C_{proposed} = \gamma P_o. \tag{8}$$

The circuitry added for the LF-leg, on the other hand, occupies the same volume as long as the output power is smaller than 17.9 kW, according to Equation (3c), as the employed STY105NM50 N switches are rated for 110 A:

$$V_{LF,proposed} \approx \lambda. \tag{9}$$

The proportionality constants α, β, γ, and λ used in (7)-(9) vary for every certain converter "design". For instance, equations (8) and (9) are plotted in Fig. 8 for the same specifications and components of Tables 1 and 2, and a moderate layout design for the capacitor-bank and the LF-leg, as elaborated in [42]. In the considered moderate layout design, the capacitors in the capacitor bank have a clearance of 6 mm with each other, and the LF leg circuitry has a boxed volume of 14.22 cm^3.

By comparing the saved and lost volume curves, it is realized that for the certain "design" used in this example, the proposed solution will result in a higher power-density for rated output powers larger than the critical value of $P_{o,crit} = 1470\ W$.

C. CHOOSING THE SUPERIOR DLF RIPPLE DECOUPLING SOLUTION

In the previous subsection, the critical output power was obtained based on a certain "design". Here, the term design is referring to three elements:

- Converter specifications: Table 1
- Component selection: Table 2
- Layout design: a moderate design (elaborated in [42])

Obviously, changes in any of these three elements would result in another value of critical output power. For instance, if the LF-leg is realized using switches with smaller packages, or a more compact layout design is employed, the proposed solution would yield into a higher power-density compared to the buck APD, at a lower output power rating. However, the general trend will still be valid.

In fact, a similar discussion can be made when comparing PPD to APD. Regardless of the employed APD method, it always results in a smaller capacitance requirement compared to PPD. This reduced capacitance requirement, however, does not necessarily imply a higher power-density. Based on the "design" of the two circuits, there would be a certain critical value of allowable dc-link voltage ripple, ΔV_{crit}, which can be obtained by comprehensive studies, such as the one carried out in [4]. APD would result in a higher power density only if the voltage ripple regulations are stricter than ΔV_{crit}.

Fig. 9 summarizes the arguments of this section. For any specific "design," there exists a corresponding critical value of allowable voltage ripple, ΔV_{crit}, and a critical value of output power, $P_{o,crit}$. If the dc-link regulations are more lenient than ΔV_{crit}, PPD would still result in a higher power-density; otherwise, APD methods should be employed. When choosing the APD method, if the output power is lower than $P_{o,crit}$, buck APD would be the best choice; for output powers beyond $P_{o,crit}$, the solution proposed in this paper would be superior.

IV. CONTROL DESIGN DETAILS

A. TCM MODULATION (INNER CONTROL LOOP)

As was previously explained, in order to achieve ac-decoupling, the inductor's current is shaped by means of the HF-leg to have a sinusoidal average, so that the capacitor's voltage becomes sinusoidal, as well. To achieve soft-switching, TCM modulation is chosen to control the HF-leg. In TCM, as shown in Fig. 10(a), each switching cycle is comprised of four distinct intervals: T_{on}, T_{off}, T_{ext}, and T_{res}. By knowing these four durations, it can be identified when and for how long each of the two switches on the HF-leg needs to be turned ON.

Although the use of TCM has already been demonstrated for both PFC and APD circuits, the details of calculations for these intervals has only been published for PFCs [38]–[40]. In this subsection, the equations for the required durations of these four intervals are derived for the APD circuit of Fig. 6(a). These equations are obtained for a typical switching cycle at which both of the inductor current reference, $i_{L(ref)}$, and the capacitor voltage, $v_{cb}(t)$, are positive, so that the

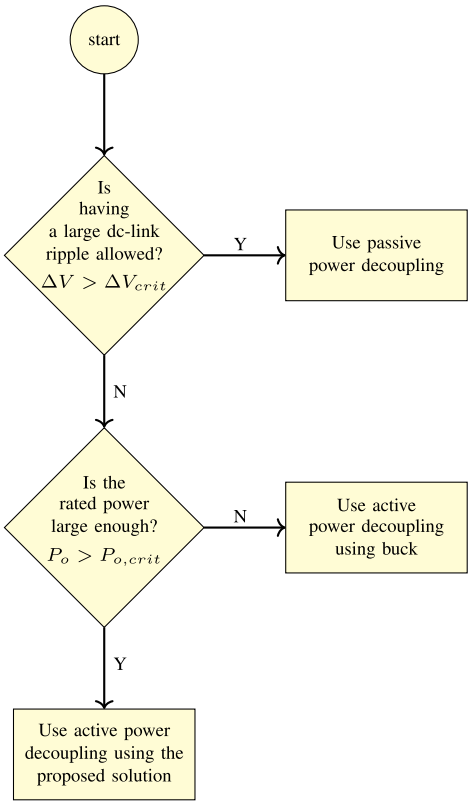

FIGURE 9. Proposed flowchart for choosing the best power decoupling solution.

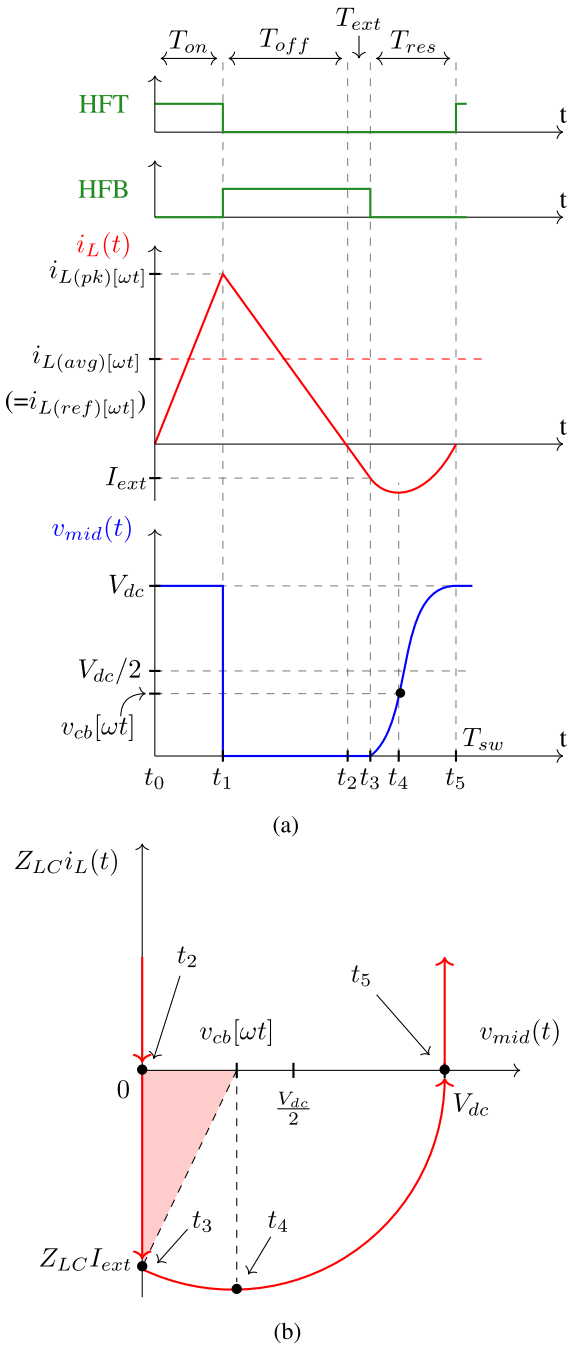

FIGURE 10. Waveforms during a typical switching cycle at which soft switching extension is achieved (assuming that $v_{cb[\omega t]} < \frac{V_{dc}}{2}$): (a) time plots and (b) V/I resonance diagram.

circuit is in the operation mode of Fig. 6(b). The equations for the other operating regions can be obtained in a similar manner [42].

1) T_{on}

In the first interval, (t_0-t_1), HFT and HFB are ON and OFF, respectively, for the duration of T_{on}. In this case, the midpoint of the HF-leg is connected to V_{dc} ($v_{mid}(t) = V_{dc}$). As a result, assuming the capacitor's voltage to be constant at each switching cycle, the constant positive voltage of $V_{dc} - v_{cb}[\omega t]$ is applied across the inductor. Consequently, the inductor's current increases linearly according to

$$L_b \frac{i_{L(pk)}[\omega t]}{T_{on}[\omega t]} = V_{dc} - V_{cb(\max)} \sin[\omega t], \tag{10}$$

which assumes that the capacitor's voltage is the required sinusoidal waveform of (3b).

Also, the required average current waveform, which was previously shown in (3c), can be represented in an alternative form as

$$i_{L(ref)}[\omega t] = C_b \frac{dv_{cb}(t)}{dt} = C_b \omega_0 V_{cb(\max)} \cos[\omega t]. \tag{11}$$

Noting that the peak curent is twice its average value in TCM, the required duration of T_{on} can then be obtained based on (10) and (11) as

$$T_{on}[\omega t] = \frac{2L_b C_b \omega_0 V_{cb(\max)} \cos[\omega t]}{V_{dc} - V_{cb(\max)} \sin[\omega t]}. \tag{12}$$

It can be observed that in contrast to the PFC circuits, the commonly-used constant-T_{on} method is not applicable to the APDs, as T_{on} varies throughout the line-cycle.

2) T_{off}

At instant t_1, HFT is opened and HFB is turned ON instead. As the constant negative voltage $-v_{cb}[\omega t]$ is applied to the inductor, its current decreases linearly. After a duration of T_{off}, the inductor's current drops to zero at instant t_2. T_{off} can be calculated as

$$T_{off}[\omega t] = \frac{2L_bC_b\omega_0\cos[\omega t]}{\sin[\omega t]}, \tag{13}$$

in a similar way as T_{on} was calculated.

3) T_{ext}

To avoid valley-switching when $v_{cb}[\omega t] < \frac{V_{dc}}{2}$, ZVS-extension is applied. In this case, HFB is kept ON for an extended period of T_{ext}, so that the inductor's current can drop to the appropriate negative value of I_{ext}. This negative current should be large enough to be able to charge and discharge HFT and HFB's parasitic capacitances, respectively, during the upcoming resonance period. If this extended period is shorter than the appropriate duration, valley-switching happens which results in switching losses; on the other hand, if this state takes longer than required, unnecessary conduction losses will be generated. It is reminded that the ZVS-extension would not be required ($T_{ext} = 0$) when $v_{cb}[\omega t] > \frac{V_{dc}}{2}$, as soft-switching can be achieved in this situation by starting the resonance period right after the inductor's current drops to zero.

The required negative extension current, I_{ext}, can be derived by applying the Pythagorean theorem to the colored triangle of Fig. 10(b). It should be noted that the vertical axis of this figure represents $Z_{LC}i_L(t)$, which has a dimension of voltage (to be consistent with the horizontal axis $v_{mid}(t)$).

$$Z_{LC}I_{ext}[\omega t] = \sqrt{(V_{dc} - v_{cb}[\omega t])^2 - v_{cb}^2[\omega t]} \tag{14}$$

$$\Rightarrow I_{ext}[\omega t] = \frac{\sqrt{V_{dc}(V_{dc} - 2v_{cb}[\omega t])}}{\sqrt{\frac{L_b}{2C_{oss}}}} \tag{15}$$

Since the inductor's current is still decreasing linearly during this period with the negative voltage of $-v_{cb}[\omega t]$,

$$T_{ext}[\omega t] = \sqrt{2L_bC_{oss}}\frac{\sqrt{V_{dc}(V_{dc} - 2v_{cb}[\omega t])}}{v_{cb}[\omega t]}. \tag{16}$$

4) T_{res}

At instant t_3, the HFB is also turned OFF to start the resonance period, T_{res}. Since both of the switches are open, an LC resonant circuit forms between the inductor and the parasitic capacitors of the two HF switches. The inductor's negative current charges $C_{oss(HFT)}$, while discharging $C_{oss(HFB)}$ simultaneously. As a result, the voltage of the HF-leg's midpoint, $v_{mid}(t)$, starts to increase. At t_5, when the midpoint voltage has increased to V_{dc} as a result of $C_{oss(HFT)}$ being fully discharged, HFT can be turned ON under ZVS condition.

Because of the LC resonance, $v_{mid}(t)$ and $i_L(t)$ change in a sinusoidal manner, with an angular frequency of $\omega_{res} = 1/\sqrt{L_b(2C_{oss})}$. Also, when $v_{mid}(t) = v_{cb}[\omega t]$, the voltage across the inductor becomes zero; consequently, at this point, the minimum point and inflection point will be observed in $i_L(t)$ and $v_{mid}(t)$, respectively. According to the two mentioned points, the midpoint voltage can be represented as

$$v_{mid}(t) = -(V_{dc} - v_{cb})\cos\left(\frac{1}{\sqrt{2L_bC_{oss}}}t\right) + v_{cb}. \tag{17}$$

Since $v_{mid}(t_3) = 0$ and $v_{mid}(t_5) = V_{dc}$, the required resonance period $T_{res} = t_5 - t_3$ can then be obtained as

$$T_{res}[\omega t] = \sqrt{2L_bC_{oss}}\left(\pi - \cos^{-1}\left(\frac{v_{cb}[\omega t]}{V_{dc} - v_{cb}[\omega t]}\right)\right). \tag{18}$$

The explained sequence can be implemented using a finite state machine, as shown in Fig. 11(a), going through the four intervals one-by-one.

B. OUTER CONTROL LOOP

As the converter's load increases, the DLF ripple also increases. In this case, a larger power needs to be handled by the capacitor, requiring $V_{cb(\max)}$ to get larger. An outer-loop controller is used to adjust $V^*_{cb(\max)}$—which is then used by the inner-loop in (12), (13), (16), and (18). The purpose of this outer-loop controller is therefore to generate a dc signal, $V^*_{cb(\max)}$, changing proportionally to the ripple at twice the line frequency.

By ignoring the higher-order harmonics, the sensed dc-link voltage can be approximately represented as

$$v_{dc}(t) = V_{dc} + V_{dc,2}\sin(2\omega_0 t). \tag{19}$$

While the dc component of the dc-link voltage is regulated by the PFC stage, the goal of the APD controller is to regulate the amplitude of the DLF voltage ripple, $V_{dc,2}$, to be zero. This component is extracted using a band-pass filter around $2f_0$:

$$x_1(t) = V_{dc,2}\sin(2\omega_0 t). \tag{20}$$

By multiplying the DLF ripple signal by $V_{dc,2}sin(2\omega_0 t)$, a dc component proportional to $V_{dc,2}$ is generated, in addition to a component at $4f_0$. The reason why x_1 is multiplied by $V_{dc,2}sin(2\omega_0 t)$ rather than being squared is to maintain its phase information.

$$x_2(t) = \frac{V_{dc,2}^2}{2} - \frac{V_{dc,2}^2}{2}\cos(4\omega_0 t). \tag{21}$$

A low-pass filter is then used to extract the dc component:

$$x_3(t) = \frac{V_{dc,2}^2}{2}. \tag{22}$$

A proportional-integral (PI) controller can then be employed to modify the control signal, $V^*_{cb(\max)}$, in a way that the amplitude of the DLF voltage ripple, $V_{dc,2}$, is regulated to be zero (which can be equally achieved by regulating $x_3(t) = V_{dc,2}^2/2$ to be zero).

The control-to-voltage-ripple transfer function of the system can be obtained using the injected current approach [43]

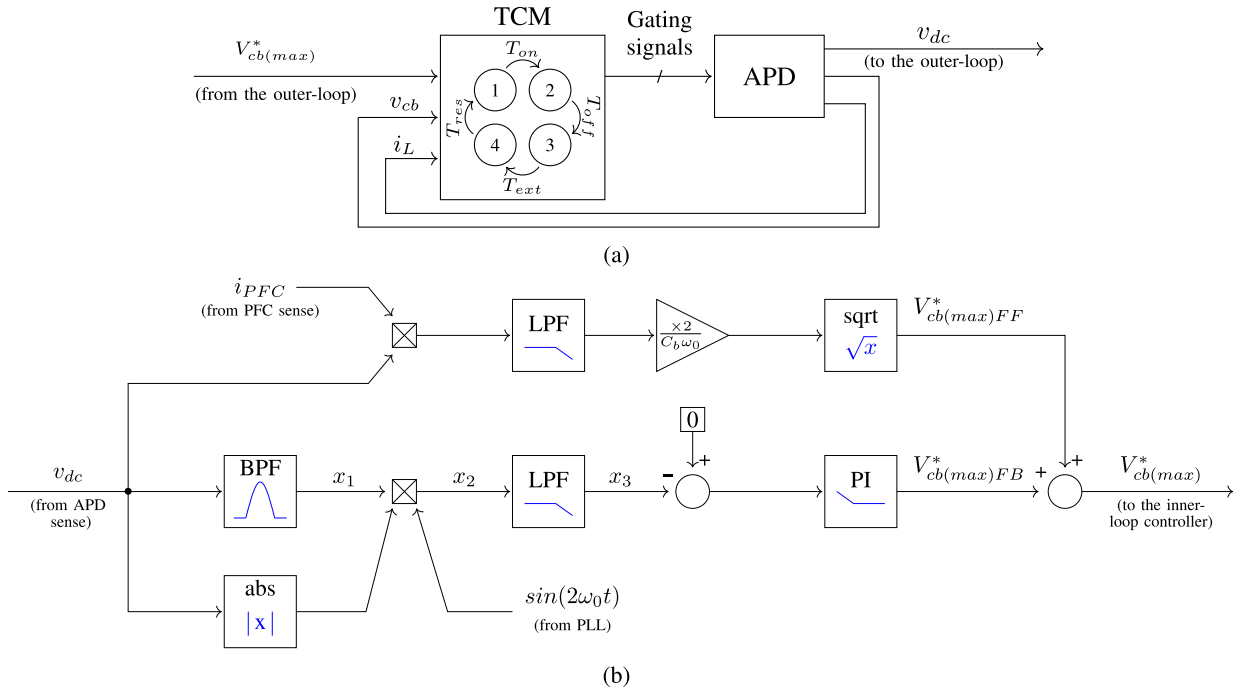

FIGURE 11. Block diagram view of the employed control design: (a) inner-loop and (b) outer-loop.

as

$$\frac{\hat{V}_{dc,2}}{\hat{V}_{cb(\max)}}(s) = \frac{C_b\omega_0 V_{dc} V_{cb(\max)}}{P_o} \frac{1}{\frac{C_{dc}V_{dc}^2}{P_o}s + 1}, \tag{23}$$

which is a single-pole response with a dc-gain of 8.77 dB and crossover frequency of 21.9 Hz, using the parameters of Table 1.

It should be noted that since this transfer function has been obtained through averaging the instantaneous DLF ripple, it is only accurate at frequencies below $2f_o$. However, since the chosen control signal, the desired amplitude of the buffer capacitor, should be constant during each buffer capacitor voltage cycle, the compensated transfer function should not have a high bandwidth, as well. Therefore, the range of frequencies at which the obtained transfer function, (23), is accurate is sufficient for our control purpose in here.

The open-loop crossover frequency of 21.9 Hz is appropriately small for this case. The following PI controller can be used to provide infinite closed-loop dc-gain while maintaining the same crossover frequency:

$$G_{c(PI)}(s) = 1 + \frac{31.42}{s}. \tag{24}$$

In addition to the explained feedback loop which mainly regulates the steady-state performance of the converter, a feedforward loop is employed to improve its transient response [4]. This loop attempts to equate the amplitude of the power absorbed by the APD with the amplitude of the sensed

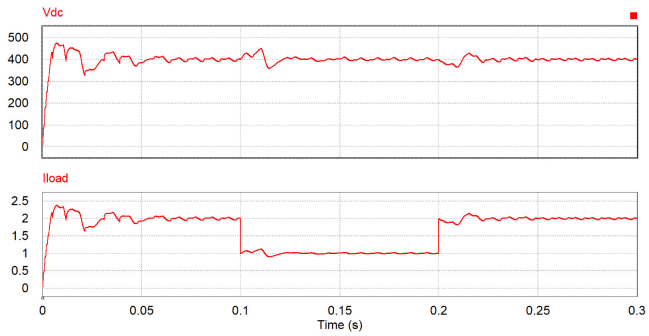

FIGURE 12. Simulation results for the proposed control scheme, under load step-down and step-up: (top) dc-link voltage and (bottom) load current.

DLF ripple power, based on (1), (3b), and (3c):

$$V^*_{cb(\max)FF} = \sqrt{\frac{2P_o}{C_b\omega_0}}. \tag{25}$$

The dynamic operation of the converter using the proposed control scheme is simulated as illustrated in Fig. 12, in which the initial start-up of the converter is followed by step-down and step-up of the output load, from full-load to half-load and vice versa.

V. EXPERIMENTAL VERIFICATION

The steady-state operation of the proposed solution is demonstrated using an experimental setup. For this purpose, an APD circuit based on the proposed solution is developed, mainly using the same specifications and components of Tables 1 and

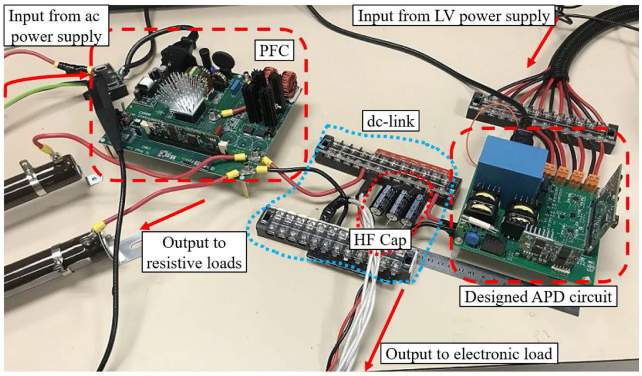

FIGURE 13. Photo of the prepared experimental setup.

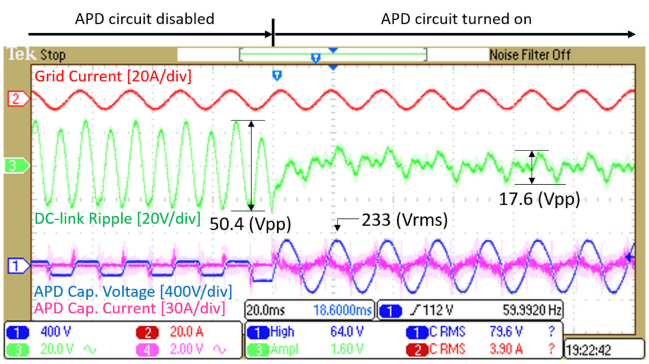

FIGURE 14. Oscilloscope screenshot demonstrating dc-link ripple reduction as the APD circuit is turned ON.

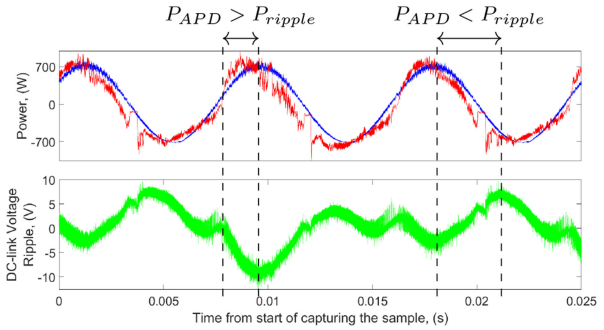

FIGURE 15. Power mismatch as the reason for the remaining ripple on the dc-link voltage.

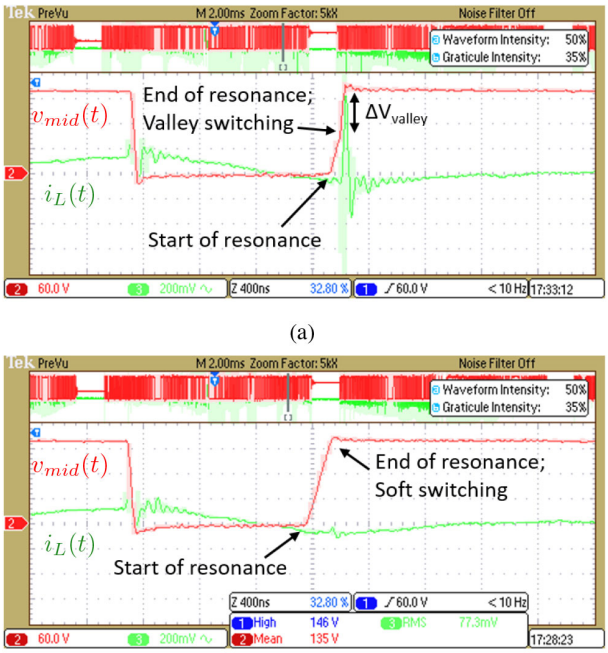

FIGURE 16. Waveforms of the inductor's current (green) and voltage of the HF leg's midpoint (red): (a) without applying soft-switching and (b) with applying soft-switching.

2. The only differences are related to the inductor and capacitor banks, for which 019890300R and B32758G3406K000 have been used, respectively. In choosing these two components, the availability and convenience of use are also considered, rather than mere power-density optimization. The developed APD circuit is then connected to the output of the 380 V/700 W TMDSILPFCKIT PFC evaluation module from Texas Instruments, with all of its output electrolytic capacitors having been removed.

The operation waveforms can be observed in Fig. 14. Initially, the APD circuit is disabled. As expected, a large DLF ripple appears on the dc-link voltage. After some time, the APD circuit is activated. In this situation, the inductor's current is controlled to have a sinusoidal average, which shapes the capacitor's voltage to be a sinusoidal waveform as well, with 90° phase lag. Consequently, the capacitor absorbs the DLF ripple from the dc-link, leaving a small voltage ripple with a typically-accepted peak-to-peak value of less than $\pm$2.5%.

Ideally, an APD circuit is expected to leave no ripple on the dc-link voltage by exactly absorbing the DLF ripple power. In practice, however, there always remains some ripple as a result of the mismatch between the DLF ripple power that needs to be absorbed and the (non-perfect) power that the APD actually absorbs. As can be observed in Fig. 15, at intervals when the power absorbed by the APD is less than the DLF ripple power, dc-link voltage increases as the PFC is pouring more power into the dc-link than the APD absorbs. Conversely, when the APD draws more power than what the PFC injects into the dc-link, the instantaneous dc-link voltage drops. Therefore, an HF capacitor would still be needed to be installed on the dc-link to limit the amplitude of this remaining ripple. By controlling the APD capacitor's voltage to have a lower THD, its absorbed power would have less mismatch with the DLF power required to be absorbed, resulting in smaller remaining ripple for the same HF capacitor being used.

Additionally, the effect of soft-switching can be seen in Fig. 16. In Fig. 16(a), the resonance period required to achieve ZVS is skipped by turning the investigated switch ON shortly after the other switch on the leg is turned OFF. In this case, valley-switching happens as the parasitic capacitance of the

switch does not have enough time to be fully discharged. Switching losses and current ringings occur as a result of the dissipation of this remaining charge in the $R_{ds(on)}$ of the switch. These negative effects, in contrast, are not observed in Fig. 16(b) where the required T_{ext} and T_{res} intervals are not skipped, so that ZVS is realized.

VI. CONCLUSION

This paper was focused on improving the current state-of-the-art for the active power decoupling circuits in 400 Vdc/kW-level single-phase ac/dc applications. The three main contributions of this paper are summarized as follows:

- Establishing the principal criteria for modern APD circuits, categorizing the previous literature, and identifying the current state-of-the-art based on these criteria. It was realized that although many alternatives have been already introduced in the literature, the simple buck APD can still be considered as the state-of-the-art. These results were summarized in Fig. 5.
- Proposing the buck-plus-unfolder topology as an improvement for the buck APD, and establishing a simple, yet solid foundation to choose the superior decoupling solution for different ΔV and P_o specifications. It was realized that the proposed solution becomes more attractive as the dc-link voltage regulations become more stringent and the rated power is increased. These results were summarized in Fig. 9.
- Deriving the TCM operation equations for APD circuits. It was realized that as opposed to the PFCs, the required T_{on} duration is not constant for APD circuits.

Finally, the operation of the proposed solution was demonstrated using the developed hardware prototype.

REFERENCES

[1] Z. Liu, B. Li, F. C. Lee, and Q. Li, "Design of CRM AC/DC converter for very high-frequency high-density wbg-based 6.6kw bidirectional on-board battery charger," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2016, pp. 1–8.

[2] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4778–4794, Jul. 2016.

[3] R. Wang *et al.*, "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1430–1443, May 2011.

[4] D. Neumayr, D. Bortis, and J. W. Kolar, "Ultra-compact power pulsation buffer for single-phase DC/AC converter systems," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf. (IPEMC-ECCE Asia)*, May 2016, pp. 2732–2741.

[5] Y. Panov, M. M. Jovanovic, and B. T. Irving, "Single-loop control of buck power-pulsation buffer for AC-DC converter system," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2018, pp. 1577–1584.

[6] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690–4698, Nov. 2012.

[7] F. Frebel, P. Bleus, O. Bomboir, and D. Rixhon, "Transformer-less 2 kw non isolated 400 VDC/230 VAC single stage micro inverter," in *Proc. IEEE Int. Telecommun. Energy Conf.*, Oct. 2016, pp. 1–6.

[8] M. Chen *et al.*, "High power density and high efficiency inverter with ripple decoupler circuit," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf. (IPEMC-ECCE Asia)*, May 2016, pp. 546–549.

[9] X. Zhao, L. Zhang, R. Born, and J. Lai, "Solution of input double-line frequency ripple rejection for high-efficiency high-power density string inverter in photovoltaic application," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2016, pp. 1148–1154.

[10] A. S. Morsy and P. N. Enjeti, "Comparison of active power decoupling methods for high-power-density single-phase inverters using wide-bandgap fets for google little box challenge," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 790–798, Sep. 2016.

[11] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active power decoupling for high-power single-phase PWM rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1308–1319, Mar. 2013.

[12] R. Chen, Y. Liu, and F. Z. Peng, "DC capacitor-less inverter for single-phase power conversion with minimum voltage and current stress," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5499–5507, Oct. 2015.

[13] Y. Tang, F. Blaabjerg, and P. C. Loh, "Decoupling of fluctuating power in single-phase systems through a symmetrical half-bridge circuit," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2014, pp. 96–102.

[14] Y. Tang, F. Blaabjerg, P. C. Loh, C. Jin, and P. Wang, "Decoupling of fluctuating power in single-phase systems through a symmetrical half-bridge circuit," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1855–1865, Apr. 2015.

[15] M. Saito and N. Matsui, "Modeling and control strategy for a single-phase PWM rectifier using a single-phase instantaneous active/reactive power theory," in *Proc. 25th Int. Telecommun. Energy Conf.*, Oct. 2003, pp. 573–578.

[16] S. Harb, M. Mirjafari, and R. S. Balog, "Ripple-port module-integrated inverter for grid-connected PV applications," *IEEE Trans. Industry Appl.*, vol. 49, no. 6, pp. 2692–2698, Nov. 2013.

[17] M. A. Vitorino, L. F. S. Alves, R. Wang, and M. B. de Rossiter Corrêa, "Low-frequency power decoupling in single-phase applications: A comprehensive overview," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2892–2912, Apr. 2017.

[18] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, Jun. 2013.

[19] Q. Huang and A. Q. Huang, "Review of GaN totem-pole bridgeless PFC," *CPSS Trans. Power Electron. Appl.*, vol. 2, pp. 187–196, Sep. 2017.

[20] L. Huber, Y. Jang, and M. M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 23, pp. 1381–1390, May 2008.

[21] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016.

[22] A. C. Kyritsis, N. P. Papanikolaou, and E. C. Tatakis, "Enhanced current pulsation smoothing parallel active filter for single stage grid-connected AC/PV modules," in *Proc. 13th Int. Power Electron. Motion Control Conf.*, Sep. 2008, pp. 1287–1292.

[23] H. Watanabe, J. Itoh, and Q. Roudier, "Single-phase power decoupling technique utilizing hybrid method with passive and active power decoupling," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo.*, Nov. 2018, pp. 1–6.

[24] Z. Qin, Y. Tang, P. C. Loh, and F. Blaabjerg, "Benchmark of AC and DC active power decoupling circuits for second-order harmonic mitigation in kilowatt-scale single-phase inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 15–25, Mar. 2016.

[25] G. Kafanas, M. R. Jeffrey, and X. Yuan, "Variable structure control for active power decoupling topologies," in *Proc. 8th IET Int. Conf. Power Electron., Mach. Drives*, Apr. 2016, pp. 1–6.

[26] S. Yamaguchi and T. Shimizu, "A single-phase power conditioner with a buck-boost-type power decoupling circuit," in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 3771–3777.

[27] X. Li, S. Xiao, H. Zhang, R. S. Balog, and B. Ge, "Dual buck based power decoupling circuit for single phase inverter/rectifier," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2016, pp. 1–6.

[28] S. Xiao, X. Li, H. Zhang, and R. S. Balog, "Active power decoupling method based on dual buck circuit with model predictive control," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2018, pp. 3089–3094.

[29] K. Tsuno, T. Shimizu, K. Wada, and K. Ishii, "Optimization of the DC ripple energy compensating circuit on a single-phase voltage source PWM rectifier," in *Proc. IEEE 35th Annu. Power Electron. Specialists Conf. (IEEE Cat. No.04CH37551)*, Jun. 2004, vol. 1, pp. 316–321.
[30] T. Shimizu, T. Fujita, G. Kimura, and J. Hirose, "A unity power factor PWM rectifier with DC ripple compensation," *IEEE Trans. Ind. Electron.*, vol. 44, no. 4, pp. 447–455, Aug. 1997.
[31] Y. Ohnuma and J. Itoh, "A novel single-phase buck PFC AC-DC converter with power decoupling capability using an active buffer," *IEEE Trans. Industry Appl.*, vol. 50no. 3, pp. 1905–1914, May 2014.
[32] W. Qi, H. Wang, X. Tan, G. Wang, and K. D. T. Ngo, "A novel active power decoupling single-phase PWM rectifier topology," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2014, pp. 89–95.
[33] I. Serban, "Power decoupling method for single-phase H-bridge inverters with no additional power electronics," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4805–4813, Aug. 2015.
[34] T. Shimizu, Y. Jin, and G. Kimura, "DC ripple current reduction on a single-phase PWM voltage-source rectifier," *IEEE Trans. Industry Appl.*, vol. 36, no. 5, pp. 1419–1429, Sep. 2000.
[35] M. Su, P. Pan, X. Long, Y. Sun, and J. Yang, "An active power-decoupling method for single-phase AC-DC converters," *IEEE Trans. Ind. Informat.*, vol. 10, no. 1, pp. 461–468, Feb. 2014.
[36] K. A. Kim, Y. Liu, M. Chen, and H. Chiu, "Opening the box: Survey of high power density inverter techniques from the little box challenge," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 2, pp. 131–139, 2017.
[37] R. W. Erickson and A. P. Rogers, "A microinverter for building-integrated photovoltaics," in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2009, pp. 911–917.
[38] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, Feb. 2014.
[39] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-based MHz totem-pole PFC rectifier," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 799–807, Sep. 2016.
[40] B. Su, J. Zhang, and Z. Lu, "Totem-pole boost bridgeless PFC rectifier with simple zero-current detection and full-range ZVS operating at the boundary of DCM/CCM," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 427–435, Feb. 2011.
[41] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2ed., ch. 14. Berlin, Germany: Springer, 2001, pp. 539–564.
[42] S. Sadrian, "Active power decoupling achieving optimum capacitance requirement with minimal compromise in efficiency," Master's thesis, Simon Fraser Univ., Burnaby, BC, Canada, Apr. 2019.
[43] S. Yang, S. Chen, and C. Huang, "Analysis, modeling and controller design of CRM PFC boost AC/DC converter with constant on-time control ic fan7530," in *Proc. 9th IEEE Conf. Ind. Electron. Appl.*, Jun. 2014, pp. 354–359.

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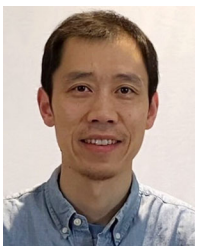

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