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Modélisation distribuée et évolutive du GaN HEMT

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Résumé

Mots-clés: GaN, HEMT, modélisation évolutive, résistance de grille distribuée

L'industrie de télécommunication et les satellites se base majoritairement sur les technologies Si et GaAs. La demande croissante des hauts débits de données entraine une facture élevée en énergie. En outre, la saturation de la bande des basses fréquences, le besoin des débits élevés et les exigences de la haute puissance imposait l'utilisation de la bande hautes fréquences. Dans le but de résoudre les problèmes cités auparavant, la technologie GaN est introduite comme un candidat prometteur qui peut offrir de la haute puissance, taille du circuit plus faible avec une meilleure stabilité mécanique aux environnements hostiles/milieux agressifs. À titre d'exemple, l'agence spatiale européenne sont en cours de développement d'un circuit à base du GaN sur substrat en Si pour faible cout, une hautes performance et une grande fiabilité.

La technologie GaN est assez mature pour proposer de nouveaux systèmes intégrés utilisés pour les puissances microonde ce qui permet une réduction considérable de la taille du système. Étant un semiconducteur à grande bande interdite, GaN peut offrir une haute puissance sous hautes températures (>225^{o}C) avec une bonne stabilité mécanique. Elle présente un facteur de bruit faible, qui est intéressant notamment pour les circuits intégrés aux ondes millimétriques. À noter que la mobilité du GaN par rapport à la température est assez élevée pour proposer des amplificateurs dans la bande W.

Avec le progrès du procédé de fabrication du GaN, notre objectif est l'introduction de cette technologie dans des applications industrielles. À cette fin, on désire avoir un modèle du dispositif qui correspond à la meilleure performance. Ensuite, on veut le valider dans une modélisation du circuit. Cette thèse, basée sur la technologie GaN unique développée au 3IT, a pour objectif l'amélioration de l'outil de conception en réduisant son erreur avec une validation de son utilisation dans la conception du circuit. Ce travail est réalisé pour la première fois au 3IT avec des résultats de simulation pour une conception idéale d'un circuit MMIC ainsi que sa démonstration.

Une caractérisation des échantillons a été réalisée avec objectif d'extraction de données qui vont servir à l'alimentation de modélisation des transistors sur l'outil ADS. Une fois complétée, la modélisation a été validée par une modélisation des petits et grands signaux et a été testée par une mesure load-pull. Enfin, ce modèle a été utilisé lors de la conception d'un amplificateur pour les applications RF.

L'innovation de ce travail réside dans la modélisation de la résistance d'une grille large sous forme de quadripôles parallèles à structure 3D (ou à résistances de grille distribuées) du transistor MOSHEMT GaN. La conception et la fabrication de l'amplificateur à haute puissance (HPA) aux fréquences microondes (≤4GHz) sont réalisés au LNN du 3IT et inclus une couche d'oxyde de grille afin de réduire le courant de fuite notamment pour les tensions Vgs élevées, la grille du transistor forme un serpentin pour fournir une puissance de sortie élevée avec un encombrement spatial minimal et une grille présentant une électrode de champ pour permettre d'augmenter la tension de claquage.

Abstract

Keywords: GaN, HEMT, Scalable modeling, distributed gate resistance

The telecommunication and satellite industry is mainly relying on Si and GaAs technologies as the demand for a high data rate is continuously growing, leading to higher power consumption. Moreover, the lower frequency band's saturation, the need for high data rate, and high-power force to utilize the high-frequency band. In pursuit of solving the issues mentioned earlier, GaN technology has been introduced as a promising candidate that can offer high power at a smaller circuit footprint and higher mechanical stability in harsh environments. For example, currently, the European space agency (ESA) is developing an integrated circuit with GaN on Si substrate for low cost, high performance, and high reliability.

GaN technology is sufficiently mature to propose integrated new systems which are needed for microwave power range. This technology reduces the size of the system considerably. GaN is a wide bandgap semiconductor which can offer remarkably high power at high temperature ($> 225℃$), and it is very stable mechanically. It presents a low noise factor, very interesting for a millimeter-wave integrated circuit. Finally, the mobility of GaN vs. temperature is sufficiently elevated to propose a power amplifier in W-Band.

With the improvement of the GaN process, our objective is to introduce this technology for industrial applications. For this purpose, we wish to have a better model of the device that corresponds to the best performance and then validate it by using this model in a circuit. Based on the 3IT's GaN process, which is unique in its context, this thesis aims to improve the design kit by reducing the design model's error and validating it by using it in circuit design. This work is the first to realize in 3IT with simulation results to design an MMIC circuit for demonstration.

I first characterized the new samples by performing different measurements than using these measurement data; transistor is modeled in ADS software. Once the model was completed, it is validated by small-signal modeling, and then the large-signal model is tested with non-linear capacitances, current source, and transconductance modeling. Finally, we used this model to design a power amplifier for RF application.

The innovation comes from modeling large gate resistance as distributed gate resistance for GaN MOSHEMT transistor and then designing high-power amplifier (HPA) in the frequency range ($\leq$ 4GHz) while using 3IT GaN process which includes first oxide layer to have low gate current and more voltage of V_{gs}, the second transistor is meander to have high power and third, field plate - gate for high breakdown voltage.

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I also want to thank my parents here for their permanent support and especially my brothers; with their help, I reach this far in life and be able to visit and experience the wonderful multicultural world.

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List of Abbreviations and Acronyms

AlGaN	Aluminum Gallium Nitride
AlN	Aluminum Nitride
InAlN	Indium Aluminum Nitride
NSERC	Natural Sciences and Engineering Research Council of Canada
GaN	Gallium Nitride
GaAs	Gallium Arsenide
Si	Silicon
SiC	Silicon Carbide
SiGe	Silicon Germanium
InP	Indium Phosphide
IGBT	Insulated-gate bipolar transistor
FET	Field-effect transistor
HEMTs	High electron mobility transistors
MMICs	Monolithic microwave integrated circuits
RF	Radio Frequency
3IT	Institut interdisciplinaire d'innovation technologique
LDMOS	Laterally diffused metal oxide semiconductor
MESFET	Metal–semiconductor field-effect transistor
MOSHEMT	Metal-oxide-semiconductor high electron mobility transistor
MOCVD	Metalorganic chemical vapor deposition
ADS	Advance design system
DGRM	Distributed gate resistance model
SSM	Small-signal modeling
SSSM	Scalable small-signal modeling

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Chapter 1: Introduction

1.1 Background

The telecommunication industry is growing day by day, and the demand of the end-user for more data rate transfer and receive with high speed is increasing rapidly. The demand for more data is expected to increase in the next ten years by 2020. Each user needs about ten simultaneously connections of a mobile network because of the proliferation of electronic devices in our daily lives, which will need gigabytes per second data rate by the network providers [1]. Second, future technology or network has to be more intelligent and efficient with respect to its energy consumption and cost. For example, the Japan energy consumption of the IP routers will increase exponentially from less than 1TWh to about 100TWh between 2000-2020 and goes above 100,000TWh (100,000,000 million kWh) in 2050. Meanwhile, the date rate shows a similar behavior from 0.1Tbs to about 80Tbs till 2020. It will rise to above 10,000 Tbps in 2050 [2], as shown in Figure 1-1.

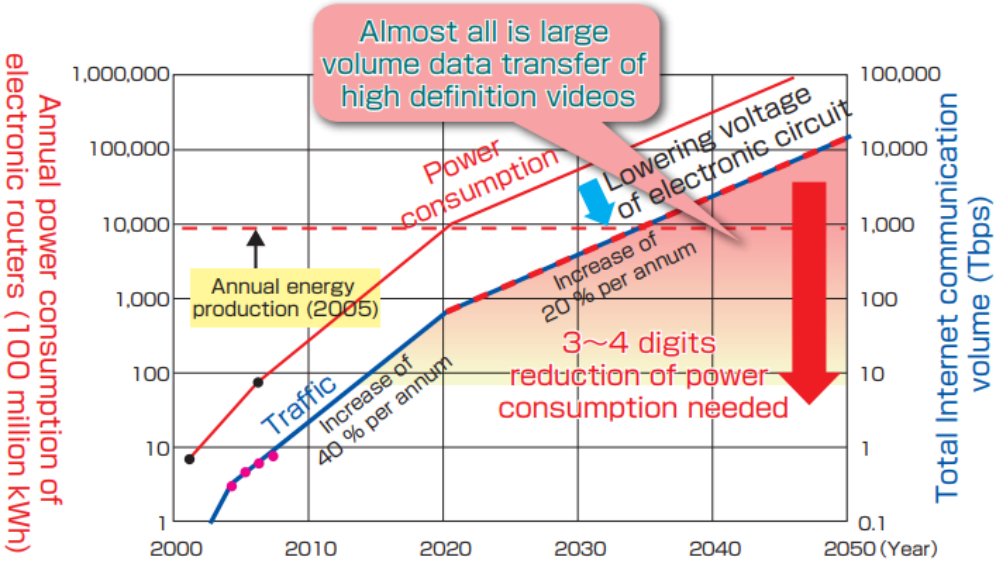


Figure 1-1: The Internet communication volume vs. power consumption of the routers [2].

Approximately 20% increase in traffic each year requires 3 to 4 digit power reduction. As a result, we need devices for RF application which can handle high power with minimum consumption & losses and provide high data rate also reduce the latency (time between transmitting and receiving data) from currently 40ms-60ms to 1ms-10ms to enable the 5G technology. It is not possible by the existing network technology to handle such big data. As a result, we cannot afford such a power consumption by the existing devices, requiring continuous technological research to improve the system's transmission/reception chain.

Above estimated amount of power, the increase can be justified with another estimate growth in the internet of things per year given in Figure 1-2. It shows an estimation of about a 50% increase between 2017 and 2019, and devices number could reach 50.1 billion in total. That means we need a smaller size high power device with better power efficiency.

Another problem we are facing due to an increase in the data demand is that we need more equipment to handle massive power, so the equipment and power consumption are increasing. Besides that, the lower band of frequencies is becoming saturated, leaving us no option besides going to the high-frequency band. The telecommunication and satellite industry has been mainly on silicon and GaAs technology. However, now it is looking for a technology that can provide high power at high frequency, lead to a small size of the circuit, work at high temperature, have a high level of hardness and mechanical stability. For all the above demands, GaN technology is the solution [3].

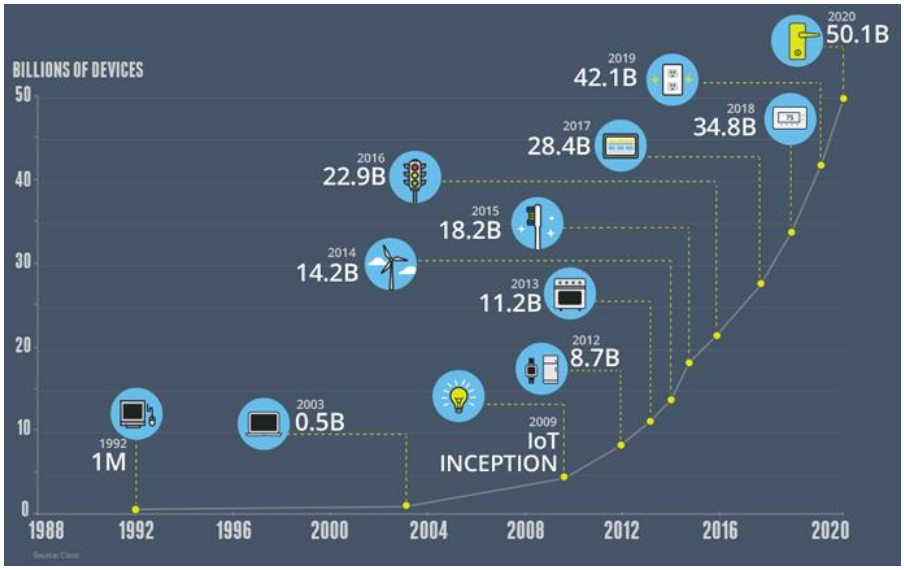


Figure 1-2: Growth in the Internet of things [4]

RF Subsystem architectures are used in all radio communication and Radar products. RF tests, measurement equipment, and scientific instrumentation also make use of RF subsystems. In any subsystem, we are always constrained by the dynamic range of signal powers that can be processed and the power consumed to do the processing. The dynamic range is limited by the thermal noise on the weak signal end and by the subsystem linearity or voltage/current swing on the strong signal end. The power consumption constraint manifests itself as either a power efficiency or a thermal dissipation limit.

A wide bandgap semiconductor GaN HEMT process has advanced subsystem performance by providing a relatively low noise process with higher drain voltage swings than Si, GaAs, or SiGe. GaN devices also have better thermal conductivity and can support much higher channel temperatures than other processes.

Historically GaN HEMTS devices are being used for higher frequency band applications due to its ability to deliver high power at those frequencies. The available market for GaN-related products for different applications based on different power and frequency is given in Figure 1-3.

Satellite technology is proliferating and has a wide area of applications, increasing every day, such as broadband internet, satellite-HDTV, live video, telemedicine, interactive gaming, and video conferencing. It is also used for astronomy, weather forecasting, broadcasting, mapping, and many more applications.

To transmit the signal at the base station, it requires very high power. Currently, LDMOS or GaAs PA are being used for such an application. Still, GaN, due to its ability to deliver high power even at high temperatures, makes it as a potential competitor for the application in L-band (1-2GHz) and S-band (2-4GHz) of frequency.

3IT GaN process is available at a lower frequency (1-4GHz). However, most GaN devices development work today are focused on higher frequencies >15 GHz and higher powers >50W so it is interesting to look at amplification by improving medium power linearity (Less transconductance variation with RF Power) to have a high dynamic range and low noise amplifier devices in this band of frequency. Those characteristics are especially important for military, space, high-reliability applications, which are required an amplitude limiter to protect the receiver chain. Any efforts to research and develop GaN devices, which can enable the higher dynamic range performance (even at lower frequencies), will be well received by device manufacturers and their customers.

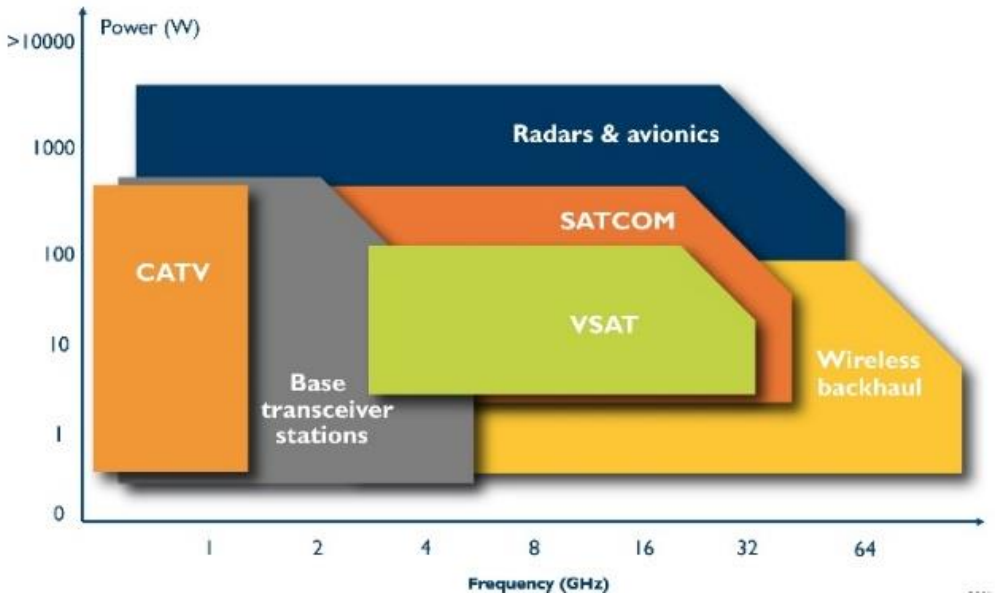


Figure 1-3: Available market for GaN-related products [5] such as CATV (Community Antenna Televisions), VSAT(Very Small Aperture Terminal), and SATCOM(Satellite Communication), etc.

To take the benefits and advantages mentioned above, we need an accurate description of the High-Electron-Mobility-Transistor (HEMT) in the form of a reliable and accurate large-signal model, which requires a small-signal model to develop it. Hence, a precise and stable small-signal model is critical to design an MMIC and optimize the circuits fabrication process. The focus of this thesis is to model AlGaN/GaN HEMT transistor with large gate width for S-Band frequencies application.

1.2 Main Objectives of the research work

The thesis's main objective is to improve the transistor model to better design power amplifiers operating in the device's saturation region for frequency until 4GHz and improve both linearity and efficiency. The research question is to improve the gate resistance model to have a better transistor model for PA design based on the hypothesis that as gate length increases, the classical model does not give accurate fit and is not adopted for equivalent circuits.

Typically, the assertions are:

- The intrinsic region is the same all along with the gate
- The gate resistance “seen” close to the gate contact pad is null while it is equal to R_g^{tot} at the finger edge

The currently available model of GaN HEMT transistor for RF application is for smaller gate width. However, as we increase the gate width, the traditional models are no longer valid because gate resistance is not fully included; that’s what we have studied in this thesis.

1.3 Outline of the thesis

Chapter 1 introduces the reader to the research field, provides a guideline to the thesis's general problem, and gives a clear picture of the research work's objectives.

Chapter 2 gives the background of GaN in detail and shows its importance compared to other technologies based on five different parameters: material physical properties, electrical parameters, power and frequency application, performance and cost, and analysis as a full product (system level), indicating it’s application.

Chapter 3 is about state-of-art. It provides information about the structure of AlGaN/GaN HEMT, state-of-art GaN HEMT process, process information, detailing every step involved in modeling from extrinsic to intrinsic components, and non-linear components modeling.

Chapter 4 describes the distributed gate resistance model, model development, and extraction procedure and compares the classical model with a distributed model.

Chapter 5 Provides scalability of the distributed gate resistance model from extrinsic to intrinsic lever such scalability of the access resistances and intrinsic parameters, then validation of it by S-parameters comparison.

Chapter 6 shows model validation at the transistor for large-signal modeling and a circuit-level with a PCB based power amplifier design. In the end, the conclusions of this thesis are presented and an outlook of future work.

Chapter 2: Why GaN

Microelectronics industries are encouraged and motivated to develop a market-oriented technological process to fulfill the end-user requirement (low cost, small size devices) and meet the industry's demand for an integrated circuit based on a lesser level complexity, better performance, and low cost. The competition among companies in the semiconductor industry is tough, and they are fighting each day to protect and expand their business to gain more market shares. For example, when it comes to implementing the radio frequency integrated circuits, microwave monolithic integrated circuits (MMIC), a system in package (SiP) or system on chip (SoC), whatever the circuits or system type are low cost, high performance, and high integration are vital parameters which each designer pay attention and for which companies always try to compete.

For doing analyses between GaN vs. other technologies, including Si and III-V technologies, it is essential to see their properties, characterizations, advantages, and limitations for comparison at material physical properties level, performance level, and analyzing them a full product. Each level of comparison provides us information for specific requirements or goals. Still, it's hard to judge which technology is better unless we make a comparison based on a specific application. However, we need to pay attention that only some semiconductor material is far better than others in physical material properties. Still, there are not mature in technology or other getting mature in technology. Still, there is no industrial process that exists so far; thus, these materials are out of the competition in both cases when it comes to application. The detail of each comparison is given the following:

2.1 Comparison based on the material's physical properties and electrical parameters

2.1.1 Comparison based on material's physical properties

The detailed comparison of GaN with other technologies such as Ge, Si, GaAs, InP, SiC, and diamond is given in Table 2-1 for several material properties.

These technologies have proved their value for RF and millimeter-meter integrated products because the circuit design and implementation of it on the substrate is more feasible with III-V technologies than the silicon-based process. Silicon and Silicon-Germanium are catching upmarket due to increased performance and high integration capabilities. Still, they have competition with already market player GaAs technology. The GaN technology has been improved by reducing substrate thickness to have low thermal dissipation and smaller parasitic series resistors for high power and high-frequency circuit application. In comparison, InP has high mobility, which leads to high frequency practically greater than 100GHz but theoretically above 200GHz. However, it yields low power density because of the smaller bandgap.

SiC is better in case of thermal conductivity and high breakdown voltage, but the problem comes from its high cost and difficulty in the grown of other III-V material because of high lattice mismatch; thus, it does not offer 2DEG. Diamond is way better than all other technologies at the material properties level. Still, it is not mature at the technology level, and no process exists for it yet, so it is out of competition for MMIC design.

GaN is better in various physical parameters, which are very feasible for RF and millimeter-wave high power circuits [6]. It offers two-dimensional electron gas (2DEG), which offers a mature system

of very high mobility electrons even at low temperatures. It has several advantages over GaAs and Si in the power and RF application due to its superior physical material properties. This analysis is given in the radar chart Figure 2-1 according to five main physical properties of materials that define the technology limit.

Table 2-1: Material characteristic comparison between GaN and competitors [7]–[9]

Materials	Ge	Si	GaAs	InP	SiC	GaN
Bandgap (eV)	0.67	1.12	1.43	1.34	3.2	3.4
Dielectric constant	16	11.8	13.1	12.5	10	9.5
Intrinsic resistivity	47	2.3×10^{5}	1×10^{8}	8.6×10^{5}	10^{12}	10^{10}
Electron mobility ($cm^2V^{-1}s^{-1}$)	3900	1350	8500	4600	1140	1000(Bulk) 2200(2DEG)
Hole mobility ($cm^2V^{-1}s^{-1}$)	1900	480	400	150	50	850
Thermal conductivity ($Wcm^{-1}K^{-1}$)	0.6	1.5	0.46	0.68	3.7	1.3
Breakdown field (E_c)	1×10^{5}	3×10^{5}	6×10^{5}	5×10^{5}	3.5×10^{6}	2×10^{6}
Power density (Wmm-1)	N/A	1.5	0.67	0.54	4	5-12
Saturation Velocity of electron at 300k (cms^{-1})	0.7×10^{7}	1.0×10^{7}	0.72×10^{7}	0.67×10^{7}	–	1.4×10^{7}

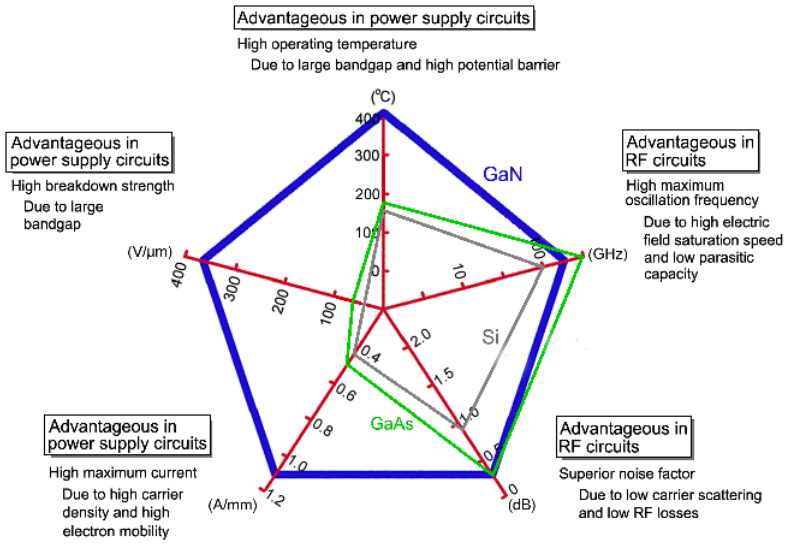


Figure 2-1: Advantages of GaN in RF and Power supply circuits over GaAs and Si [10]

As a result, it has advantages over competitive material such as GaAs and Si, similarly the competitive technology such as LDMOS and GaAs technology. Both LDMOS and GaAs are useful in

a specific range of frequency and power level [11], [12]. For example, GaAs products are suitable for high frequency but medium power up to 25W-50W applications [12]. GaAs does not behave well at high power due to low thermal conductivity. Second, LDMOS is useful for high power applications based on Si technology, but it only goes up to a maximum 3GHz-5GHz frequency [12]. However, GaN is an alternative of both because it is suitable for high power and frequency application.

2.1.2 Comparison based on electrical parameters

After making this comparison based on the material physical properties, the next electrical parameters are essential to see differences among different technologies. The comparison is among GaAs, GaN, SiGe, and Si technologies, which are mature enough and have industrial processes given in Table 2-2. based on electrical parameters: cutoff frequency (f_T), maximum oscillation frequency (f_{max}), noise figure, phase noise, IP3/PDC, breakdown voltage, and power handling capability.

SiGe HBTs are useful to provide the highest cutoff frequency but not competitive to GaN HEMT and HBT GaAs, which are better in high efficiency, low noise figure, better power handling capability, and a high ration of linearity over dissipated DC power. Because of fully developed technology and existing platform Si (RF-CMOS) is perfect for large scale integration. On the other hand, it is not good competitive in other parameters and comes at the end among its competitor's technologies for typical electrical figures of comparison.

Table 2-2: Comparision of typical electrical figures of several semiconductor technologies [6]

Technology Devices	**GaAs**			**GaN**	**SiGe**	**Si**
	MESFET	**PHEMT**	**HBT**	**HEMT**	**HBT**	**RF-CMOS**
f_T	L	M	H	M	H	L
f_{max}	M	H	H	M	H	L
Noise figure	M	L	M	L	M	H
Phase Noise	M	H	L	L	L	H
IP3/PDC	H	M	H	H	M	L
Breakdown voltage	M	H	M	H	L	L
Power Handling	M	H	H	H	M	L

H=High, M=Medium, L=Low

2.1.3 Comparison based on power and frequency application

Some specific applications and performance of the devices made from different semiconductor technologies need specific output power and frequency. The following Figure 2-2 gives an idea about specific technology's power and frequency [13].

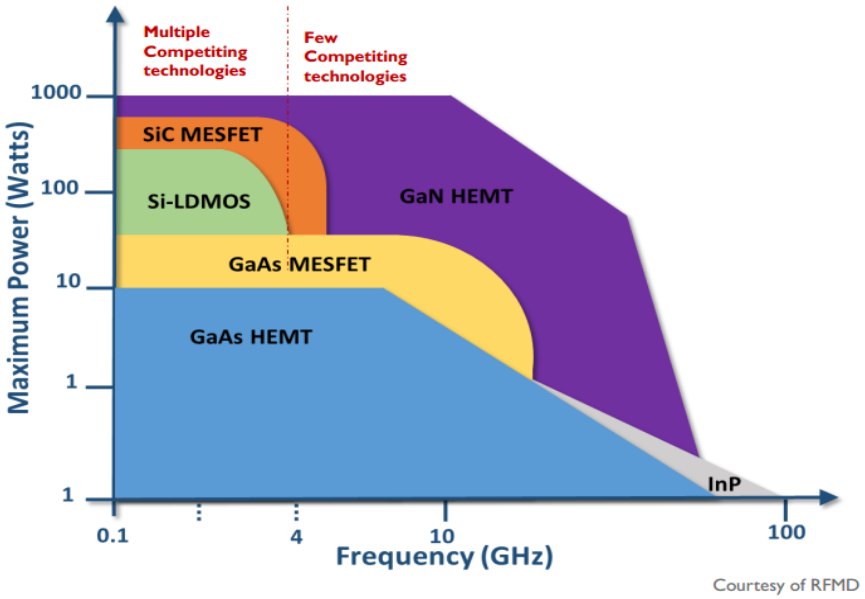


Figure 2-2: Power and frequency region for different semiconductors [13]

Currently, the GaAs Power amplifier is widely used for the base station because of its capability to handle high power at high frequency. Silicon carbide also exists for this application but is limited with frequency. However, for the broadcasting station, communication satellites, and radar applications, we need high power at high frequency, for example, 125W at the 10-12GHz for communication satellites [14], so GaN enables new possibilities for both high-power and high-frequency.

Silicon or Gallium arsenide power amplifier is used for the cell phones because the required power is about 0.9W around 1GHz. Multiple technologies are competing below 3GHz. The choice of technology for a particular application is based on either cost or high-performance. For a low cost, Si is dominating, but for high-performance, SiC is mostly used. However, with the advancement in GaN technology, such as 6 inches wafer size (OMMIC) [15] and MACOM claimed that GaN on silicon transistor outperforms premium-priced GaN-on-SiC transistor [16], It shall gradually gain the market below 3GHz application.

2.1.4 Comparison based on performance and Cost

Material physical properties and electrical parameters give the initial difference among technology, but we have to consider the relative performance and limitation of those technologies for better understanding. A figure of merit which is commonly used for active components is given by the following equation [17]–[19]:

$$FoM = f_T \times BV_{CBO} \qquad (2\text{-}1)$$

where BV_{CBO} is the breakdown voltage is given in Voltage [V], and f_T is in giga-hertz [GHz]. In most cases, we need high power along with the high-frequency application. In those cases, Si RF-CMOS and SiGe BiCMOS have low breakdown voltage, limiting the voltage swing. Another problem comes from the low bandgap of silicon, which results in a critical electrical field compared to its competitor's III-V technologies.

GaAs and other III-V technologies, particularly GaN, provide high breakdown voltage and high frequency, which is advantageous in a significant trade-off between f_T and BV_{CBO} for millimeter-wave applications. It is better to have high power by having high voltage than having high current for good efficiency, so GaN suits well in this scenario.

There are other figures of merit depending on the application such as Johson figure of merit (JFOM) [20] which is for low-voltage transistors, Keyes [21] KFOM used to see thermal limitation to the switching behavior of transistor, Baliga [22] BFOM for determining conductive losses in low-frequency and most exciting figure of merit in our case is Baliga high-frequency FoM (BHFFOM) [23]. The detailed comparison for high power RF transistors is given in Figure 2-3 between GaN and other semiconductor technologies, which indicate that GaN is better for high power RF applications.

A performance comparison is fair but not enough unless we consider cost and the particular application from manufacturing to all development costs. Again here is another trade-off in Table 2-3. There is a comparison given about capabilities and manufacturing costs related to some parameters for different technologies.

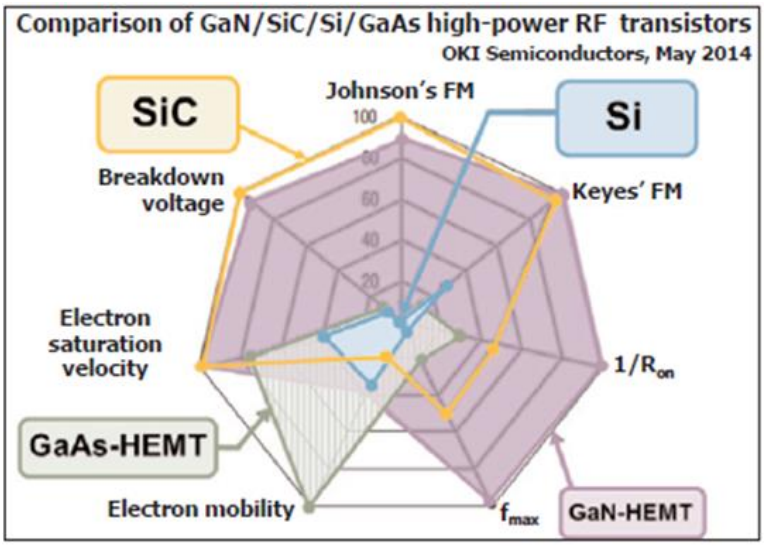


Figure 2-3: Comparison of GaN/SiC/Si/GaAs high-power RF transistors [24]

The wafer size and wafer cost for GaN technology are large as compare to others. However, it's hard to judge which technology is better based on cost because we choose technology according to the application, such as designing a mixer or power amplifier. Nevertheless, cost and performance comparison gives us an estimate of what we can have or design in the available budget for the particular application.

There is another recent comparison about wide band-gap (WBG) material cost, and wafer size is done by Yole development with an 8-inch Si wafer as reference shown in Figure 2-4. Diamond and Ga_2O_3 are future technology, don't exist yet. We can see that GaN-on-Si is the most exciting WBG technology in terms of cost and wafer size.

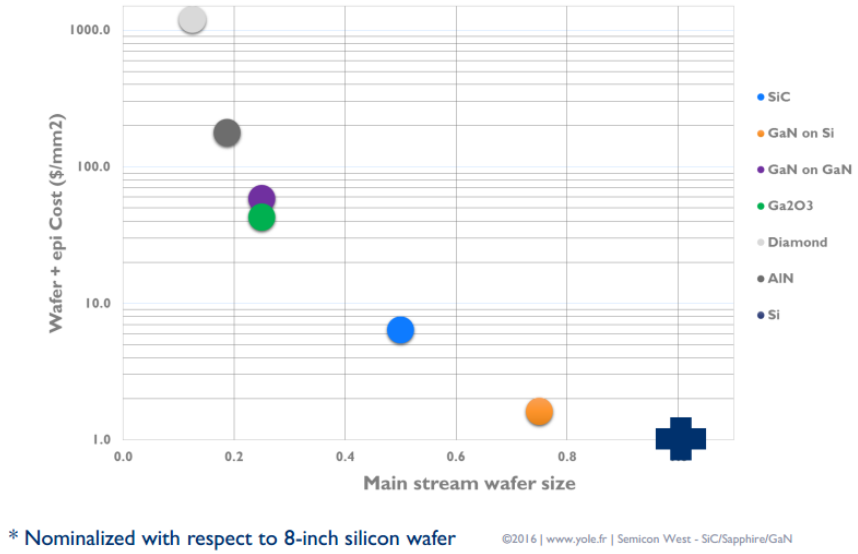


Figure 2-4: WBG material cost and wafer size comparison [25]

Table 2-3: Manufacturing Cost and Capabilities for Different Technologies [6]

Materials	GaN	GaAs	SiGe	Si
Technology Process	0.15 - 0.1 µm	0.25 - 0.1 µm	180 – 55 nm	65 – 20 nm
Devices	HEMT	HEMT	HBT	RF-CMOS
Wafer size (inches)	3 - 6	4 - 6	6 - 8	8 - 12
Mask set cost (K$)	75 - 150	25 - 50	250 - 400	400 - 1000
Wafer cost(k$)	10 - 15	4 - 10	2 - 3	1 - 2
CAD cost(k$)	10 - 50	10 - 50	500 - 1000	500 - 1000
Triple well process	NO	NO	YES	YES
Backside process	YES	YES	NO*	NO*
Metal layers	2 - 3	2	4 - 6	8 - 12
Metal material	Au	Au	Al-Cu	Al-Cu
Integration level	Low	Low	High	High

*= Through Silicon Via (TSV)

2.1.5 Comparison based on analysis as part of a full product

The last level of comparison for different technologies is done by analyzing them at the full product level. It's most difficult because trade-off involves technological process, design rule, cost, and performance. It should also consider the cost of chemicals, gases, labor, process tool maintenance, number of processes, and technology process yield. Estimation of all the above costs is given in an index [18]; thus, we can better compare different technologies. However, it still does not cover everything. We need to consider a broader area in case of planning for a particular application, so it is difficult to define one function which can give us an estimate because of performance trade-off at each stage of each stage such as device level, at circuit level (topologies, biases control), at the interface level (filters, matching-network) or the product level (interconnections, packages).

The function called product-wise comparison parameter PcP is used for this purpose:

$$PcP = f\left\{\frac{Die\ per\ wafer, Num.of\ wafers}{Wafer\ cost\ [K\$], Mask\ Cost\ [K\$]}\right\} \cdot \frac{FoM}{Process\ Yiel} \cdot \frac{Num.of\ functions}{CAD\ Costs\ [K\$]} \qquad (2\text{-}2)$$

The equation includes several parameters the die size, process yield, possible implemented number of functions also include FoM, even CAD cost. It is a complex function but can be very handy for industrial purpose use for any particular application.

For the challenges mentioned above, the GaN HEMT FET transistor offers to promise an alternative technology for highly competitive MMICs. There are some products in the markets due to the already vital research that has been done on this technology. However, this technology is not mature and far away from giving full potential due to specific issues, for example, the traping effect [26], which hinder the performance of the device, so research efforts are continuously required to overcome such issues and to optimize the cycle of technology from manufacturing to final modeling and design steps.

The summary of all the benefits or values added by GaN's technology and possible applications which it can offer at the system level are given in Figure 2-5.

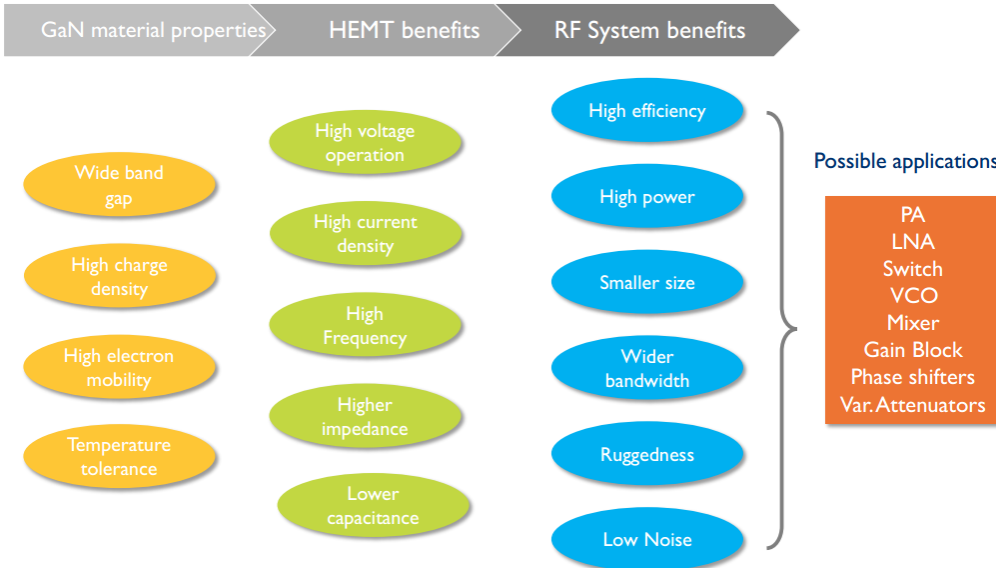


Figure 2-5: GaN's added values at system level [27]

2.2 Applications of GaN technology:

Application for GaN devices, particularly for RF electronics systems, with respect to the frequency band and available other technologies, are given in Figure 2-7. Power amplifiers are the main area of GaN adoption for these applications.

There are several applications of GaN-on-Silicon in the micro-nano electronics and optoelectronics are given in Figure 2-6 below because of low cost, the thermal conductivity of silicon is almost the same as GaN, high electrical resistivity, large area available (> 8 "), Different crystalline orientations (111), (110), (001), MOS compatible technology and, finally easy to transfer/change exotic substrate (diamond, flexible, ...).

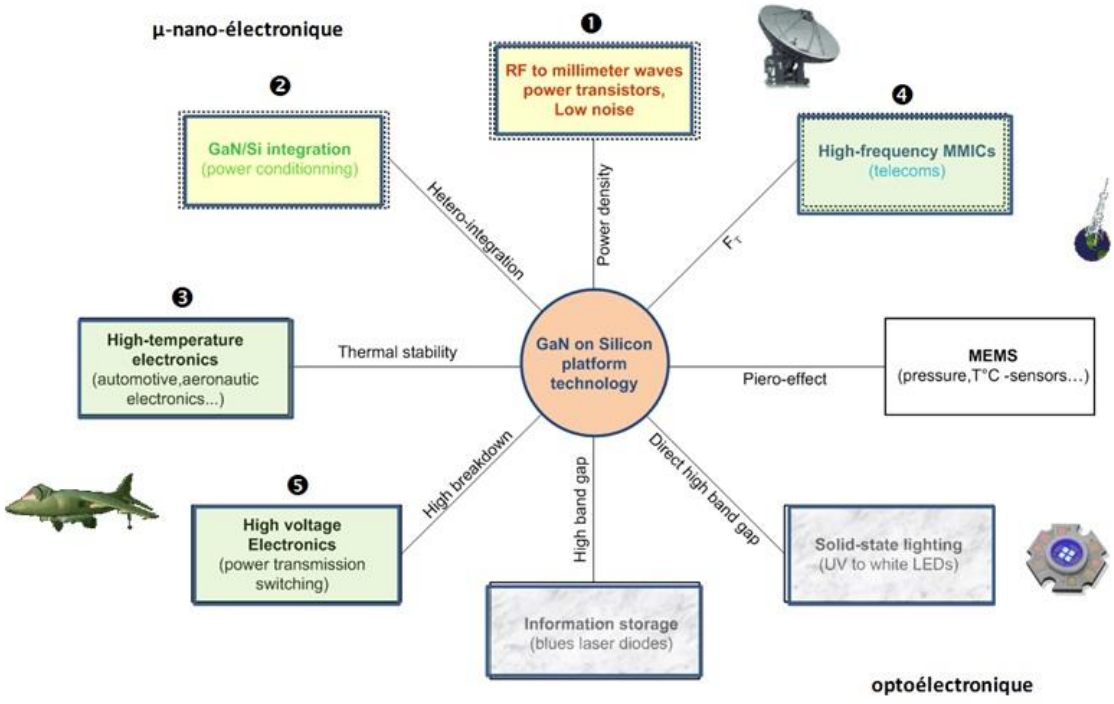


Figure 2-6: Applications of GaN on Si

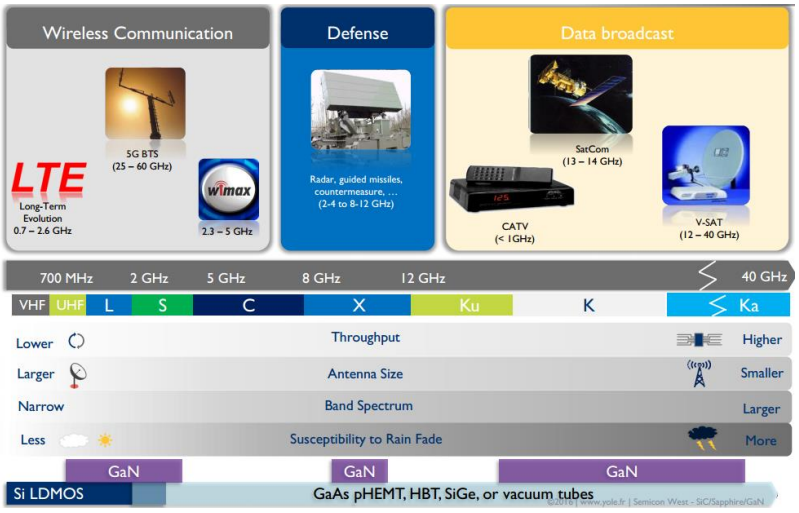


Figure 2-7: Applications of GaN devices in RF Electronics Systems

Chapter 3: State-of-the-art

This chapter explains device structure and operations layer by layer, presents state-of-art technologies based on GaN-on-SiC and GaN-on-Si (111, 100, 110) for comparison purposes. Once technologies are presented, afterward, challenges for modeling of GaN devices are mentioned. Several methods are explained for small and large signal modeling of such devices at an intrinsic and extrinsic level.

3.1 Physical structure and operation of AlGaN/GaN HEMTs

HEMT (High Electron Mobility Transistors) has two wide bandgap semiconductors (Large bandgap such as Al(Ga)N-In(Ga)AlN on lower band gap-GaN), which are not doped. In this technique, electrons come from the wide-bandgap barrier layer's surface, composed the two-dimensional electron gas (2DEG) thanks to the polarization effect (spontaneous and piezoelectric polarization). It is crucial to know that in all HEMT structure layers, there is no doping. The transport properties show improved electron mobility and higher saturation velocity in the well. This effect implies a higher f_T, a better gain, and a noise figure (NF) than MESFET. HEMT based on heterojunction AlGaN/GaN was reported for the first time in 1994 in Khan's pioneering work [28].

The typical layer structure of the AlGaN/GaN HEMT structure is shown below in figure Figure 3-1.

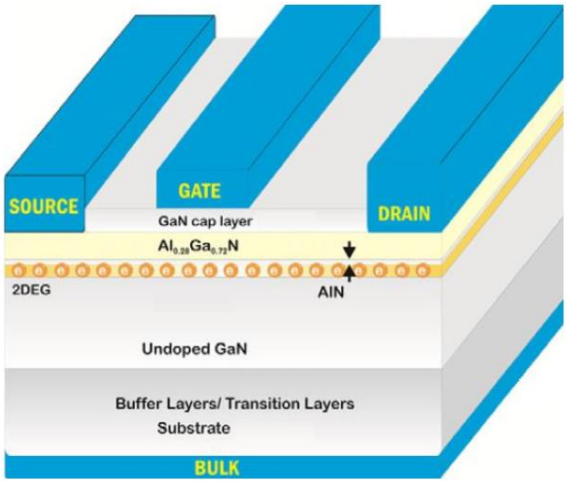


Figure 3-1: Typical HEMT structure [29]

The structure is composed of the following layer:

Cap layer: It is an optional layer (typically GaN, SiN) that allows the protection of the barrier layer (typically AlGaN), limits the currents. However, it decreases the height of the Schottky barrier [Liu et al., 2011]. We need this layer mostly when the heterostructure has many defects. Its thickness varies between a few nm to 50 nm.

The barrier layer: This is the layer with a high bandgap (In, Ga)AlN, which allows the formation of well at the interface with the GaN channel.

The Spacer Layer: This is an optional layer (typically AlN), which is the lower part of the barrier layer whose thickness is generally less than 2nm. It allows having good confinement of the electrons in

the 2DEG and increasing the electron mobility, reducing the interactions between the electrons of the 2DEG and the aluminum atoms present in the barrier layer.

Channel Layer: It is composed of undoped GaN and totally relaxed. The thickness varies between a few 10nm to a few 100nm. This layer has a lower bandgap in comparison with the barrier layer, and the 2DEG is formed in this layer.

Buffer Layer: It can be composed of a GaN layer, but it is preferred to use a back-barrier layer with a higher bandgap (typically, AlGaN, the aluminum is the function of application). Its thickness is generally greater than a few µm. Because of its high thickness, the buffer layer is fully or partially relaxed. If this layer is fully relaxed, it does not present a piezoelectric polarization. This layer's quality is very important for electronic application: It must act as an electrical insulator and have good thermal conductivity.

Stress Engineering Layers: These layers are composed of different layers between the nucleation and buffer layers. Their role is to reduce stress and dislocation rate. The thickness varies between a few 100nm to few μm.

The nucleation layer: It is the first layer to accommodate the substrate's lattice parameter with wide band-gap nitrides deposed by epitaxy. On the silicon substrate, this layer is typically aluminum nitride (AlN). Its thickness is 20-60nm.

Substrate: This is the support layer on which the growth of the different layers takes place. The substrates generally used for the growth of GaN are sapphire (Al_2O_3), silicon (Si), silicon carbide (SiC), and GaN. Table 3-1 shows a comparison between the different substrates used for the growth of GaN, depending on cost, thermal conductivity, mesh mismatch, coefficient of thermal expansion, resistivity, and size availability.

Table 3-1: Comparison between different substrates available for GaN technology

Attribute	HR-Si (111)	Sapphire	SiC	GaN (Bulk)
Thermal Conductivity (W/cm. K)	1.5	0.42	4.9	3.3
Lattice mismatch with GaN (%)	~ -17	~ -16	~ +3.5	0
Currently available wafer size (inch)	12	6	4	6
Cost (compared to Si)	Low	Very low	High	Very high
Resistivity (Ohms.cm)	Max $1\times e^{4}$	$>1\times e^{6}$	$1\times e^{5}$-$1\times e^{8}$	Max $1\times e^{13}$
Difference in heat expansion ($x10^{-6}$-K^{-1}) (300-1000K)	2.6	7.5	4.2	5.6

Silicon: It is one of the most attractive substrates for the growth of GaN, thanks to its price very competitive, its availability of large diameters, its good thermal conductivity (1.5 $Wcm^{-1}K^{-1}$), and its processing in standard silicon fabs (high productivity). The major disadvantage is that the GaN layers

elaborated on Si generally have a concentration of defects due to the mismatch in lattice parameters (17%) and a very large coefficient of thermal expansion(CTE).

Sapphire (Al_2O_3): It is a semi-insulating material that can withstand high growth temperatures and relatively cheap. On the other hand, it has very low thermal conductivity (0.5 $Wcm^{-1}K^{-1}$), large lattice mismatch (13%), and large CTE mismatch. Low thermal conductivity means it has a problem in heat dissipation as a result, not a good choice for high power applications.

Silicon carbide (SiC): Silicon carbide has very high thermal conductivity (4 $Wcm^{-1}K^{-1}$), low lattice mismatch (3%), and relatively low CTE mismatch. However, the problem is the high cost, and the technological process is more complicated.

3.2 State-of-the-art GaN technology

For the state-of-the-art GaN technology comparison, it is important to relate it with the substrate. Depending on the substrate, we have different performance because of certain advantages and disadvantages of each substrate. As mentioned in Table 3-1, SiC and Si are the most suitable substrate for GaN technology because of the advantages mentioned in chapter 2.

For GaN-on-SiC, the state-of-the-art is given in Table 3-2 at 4, 10, 18, 40, and 94GHz frequencies. These results are best obtained with the SiC substrate by having a low rate of mismatch with GaN and keeping excellent thermal conductivity. At 4GHz, the saturation output power 41.4 Wmm^{-1} was achieved with PAE at 60% [30]. Similarly, at 94GHz, 1.51 Wmm^{-1}, and 8.5% were measured P_{sat} and PAE, respectively [31]. However, OMMIC claimed that they reached 4.5 Wmm^{-1} at 94GHz with GaN-on-SiC.

Table 3-2: State-of-the-art for GaN-on-SiC at different frequencies

Frequency	Gp(dB)	Psat (W/mm)	PAE (%)	Gate length (nm)	Drain voltage (V)
@ 4GHz [30]	16	41.4	60	250	135
@10GHz [32]	24	17.5	61	250	55
@18GHz [33]	8.6	12	33	150	50
@ 40GHz [34]	-	10.5	34	160	30
@ 94GHz [31], OMMIC	9	1.51	8.5	50	9
	-	4.5	-	-	-

For more details, we can see the plot of power density as a function of frequency given in Figure 3-2. There is a clear shrinking in power as we go to high frequency.

There are three Si substrates possible depending on plane orientation, such as Si(111), Si(100), and Si(110). In the (111) plane, the crystalline silicon has a hexagonal triple symmetry surface suitable for GaN growth by epitaxy. Thus, it is commonly used as a substrate for the growth of

heterostructures dedicated to HEMT transistors and have given significant performance in terms of microwave power density. For GaN-on-Si(111), the state-of-the-art is given in Table 3-3 at 2.14, 10, 40, and 94GHz frequencies. At 2.14GHz, the saturation output power 12 Wmm^{-1} was achieved with PAE at 52.7% [35]. Similarly, at 94GHz, 1.35 Wmm^{-1}, and 12% was measured Psat and PAE, respectively [36]. However, OMMIC claimed that they reached 4.5 Wmm^{-1} at 94GHz with GaN-on-SiC.

Table 3-3: State-of-the-art for GaN on Si (111) at different frequencies

HEMT	Frequency	Gp (dB)	Psat (W/mm)	PAE (%)	W(µm)	Meas. Condition
On Si(111)	@2.14GHz [35]	15.3	12	52.7	-	-
	@10GHz [37]	-	7	52	-	-
	@18GHz [38]	9.1	5.1	20	2×50	-
	@40GHz [39]	9	2.7	18	2×25	-
	@ 94GHz [OMMIC]	-	2.1	-	-	Pout max

In the case of Si(100 and Si(110) substrates, there are also proven results given in Table 3-4. But the defect density of the heterostructures produced in these orientations is greater as compared to Si (111). However, the advantage lies in co-integration with CMOS technology.

Table 3-4: State-of-the-art for GaN on Si (100) and Si (110) at different frequencies

HEMT	Frequency	G_p (dB)	P_{sat} (dBm)	P_{sat} (W/mm)	PAE (%)	W (µm)	Measurement condition
On Si(100)	@4GHz [40]	19.3	25.3	3.4	14.3	2×150	Pout max
	@10GHz [40]	7.5	29.4	2.9	20.4	2×150	Pout max
On Si(110)	@18GHz [40]	15.6	23.4	3.76	33	2×30	Pout max
	@ 40GHz [40]	10.6	23	3.3	20.1	2×30	-

Figure 3-2 gives the best results of GaN transistors on SiC, Si (111), Si (110), Si (100), and GaN substrates in terms of power density as a function of the measurement frequency.

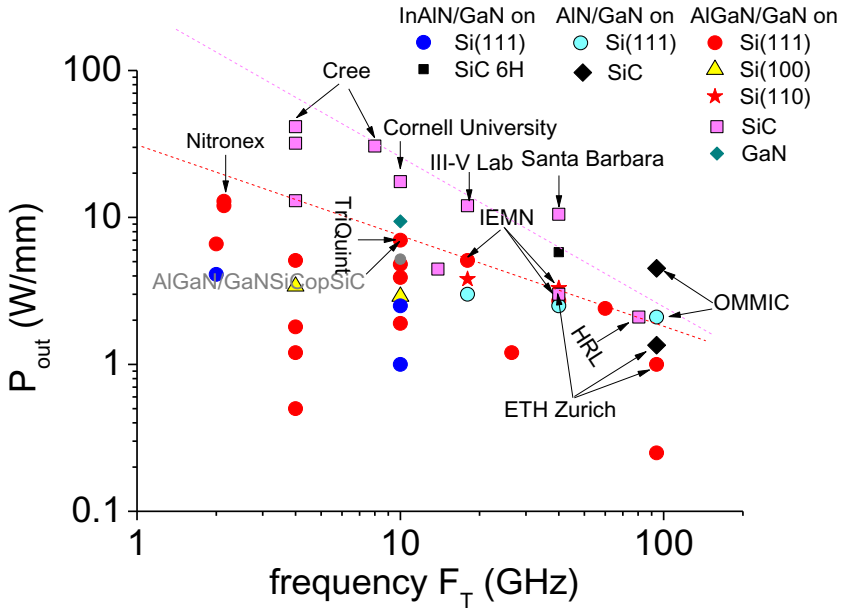


Figure 3-2: State of the art of GaN HEMT technology on Si and SiC (Power density in saturation as a function frequency) [30]–[39], [41]–[49]

3.2.1 Our process:

In the 3IT process, we have two types of devices, normally-on and normally-off transistors based on AlGaN/GaN thickness and different Aluminum (Al) concentrations in the barrier layer. In both cases, the AlGaN/GaN MOSHEMT structures were fabricated on a Si substrate and commercial HEMT wafer (supplied by EpiGaN) by using the Metal-Organic Chemical Vapor Deposition technique (MOCVD). The gate length is 1.5µm.

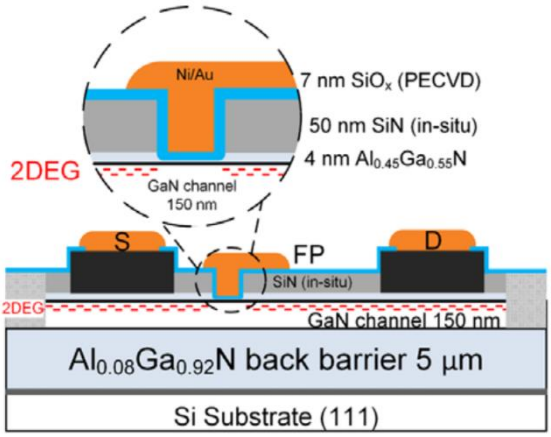
The epitaxial structure consists of a 150nm thick un-doped GaN channel layer and a thin 4nm $Al_{0.45}Ga_{0.55}N$ top barrier layer. The epitaxial structure is capped with a 50nm thick in-situ SiN layer. However, the difference between normally-on and normally-off is that the structure consists of a 1.8µm thick $Al_{0.18}Ga_{0.82}N$ back-barrier layer and 5µm $Al_{0.08}Ga_{0.92}N$ back-barrier layer, respectively, as shown in Figure 3-3 [50], [51]:

Oxide layer – MOSHEMT: In our process, we have SiOx deposited by PECVD, which acts as a gate insulator; consequently, it gives a very small gate leakage current in reverse and forwards bias condition. The thickness of the oxide layer is 5nm for normally-on MOSHEMT and 7-10nm for normally-off. It is very important to choose the oxide layer's proper thickness because it is a trade-off between better isolation to achieve low leakage current and high transconductance. To have more voltage on V_{gs} also depends on the thickness of the oxide layer. For example, for 10nm, we can go up to 10V in case of forwarding bias.

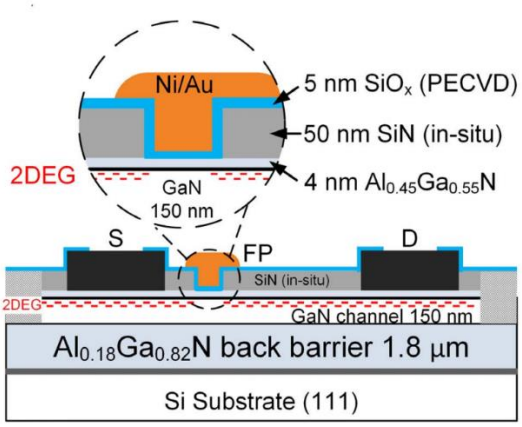
Meander shape: We are using a meander shape for the transistor. Because of this shape, we can have a longer gate length in a small space; ultimately, it leads to high power density.

Field-plate Gate: We have a field-plate gate in our process. The purpose of using a field plate gate is to increase breakdown voltage by distributing the electric field at the wider area as reported in [22] the reduction of peak electric field 40% to 50% depending on the length of the plate towards the drain side.

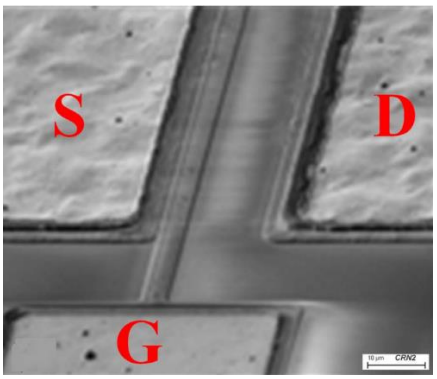
Recess gate: In the case of a recessed gate, the gate metal deposited close to 2DEG to allow improved transconductance, linearity and to shift threshold voltage from negative to positive V_{gs} voltage. The control of the etch thickness obtained by digital etching (few cycles composed of two-step: dry oxidation followed by wet etching).



a) Normally-off AlGaN/GaN



b) Normally-on, AlGaN/GaN



c) SEM image of fabricated MOS-HEMT

Figure 3-3: Schematic of the fabricated MOSHEMT [50], [51]

3.2.2 The principle of GaN HEMT Operation

A HEMT is a three-terminal device with a source, gate, and drain in which the gate electrode controls the current flow between drain and source (ohmic contacts). Its operation principle is based on the presence of 2DEG at the AlGaN/GaN heterostructure interface. By applied voltage at the gate electrode, it is possible to control the transistor channel's electron density, thus controlling the drain current (I_{DS}).

Normally-on Transistor: This transistor has four regions of operation as shown in Figure 3-4 (Vth is negative)

$$Region\ of\ Operation = \begin{cases} Cut-off & V_{gs} \le V_{th} \\ Ohmic & V_{th} < V_{gs}\ \&\ V_{Ds} \ll V_K \\ Saturation & V_{th} < V_{gs}\ \&\ V_{Ds} \ge V_K \\ Breakdown & V_{th} < V_{gs}\ \&\ V_{Ds} = V_{br} \end{cases} \quad (3\text{-}1)$$

where $V_K = V_{gs} - V_{th}$

Looking at the I_{DS} vs. V_{gs} transfer curve (Figure) for a fixed V_{DS} voltage, the I_{DS} current increases with increasing gate bias. When a negative voltage is applied to the gate, the current I_{DS} decreases, thus depleting the channel under the gate. The value of V_{gs} for which the channel is cut-off is called the threshold voltage (V_{th}).

Cut-off region: It is a region of operation in which the device channel is close means there is no conduction of electrons and no current. It occurs when the gate-source applied voltage is less than the threshold voltage.

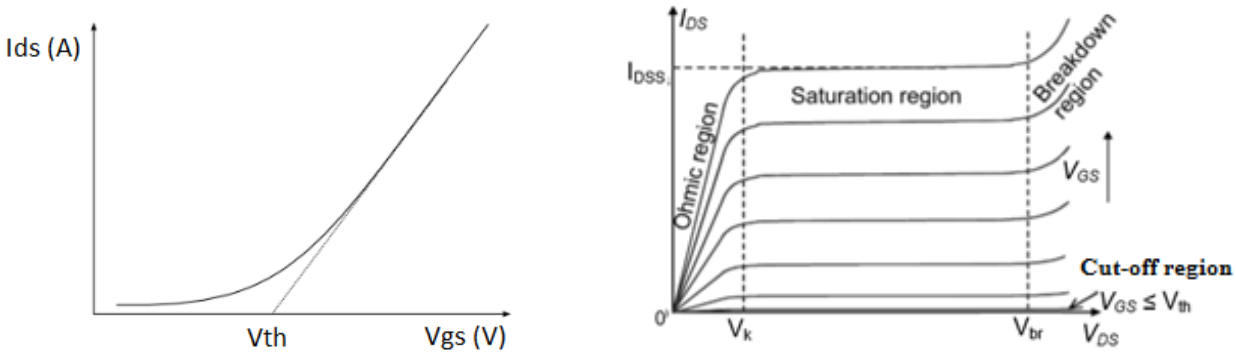
Ohmic/linear region: The drain-source current varies linearly when drain-source voltage is low. In this case, the electric field is constant along the 2DEG, and electrons move in parallelepiped bar's shape homogenously. The current can be calculated by:

$$I_{DS} \approx V_{DS} \frac{q.\mu.n_s.W}{1+q.\mu.n_s.W(R_D+R_S)} \qquad (3\text{-}2)$$

Saturation region: Current is saturated because the channel is cut-off at the drain end and V_{DS} does not affect the channel any longer.

$$I_{DS} = q.v_{SAT}.n_s.W \qquad (3\text{-}3)$$

Breakdown region: breakdown voltage is Vds' value to generate hot carriers by impact ionization, leading to an avalanche phenomenon and destroying the lattice.



a) Threshold Voltage *b) Device region of operation*

Figure 3-4: Determine threshold voltage and region of operation of the device

Depending on the application, we use the transistor to operate in different regions, depending on the quiescent point's position.

3.3 Modeling challenges of GaN HEMTs

There are different literature models, which we can broadly divide into three main categories: physical model, compact model, and behavioral model. The physical model is based on the physic of the device. For this reason, these models are limited only to the device. The advantage of these models is the large operating range. However, these are time-consuming because of the complex equation used to model physical behavior.

The second category is compact models, which are based on I-V and S-parameters measurements. These models contain a smaller number of parameters as compared to physical models and allow the designer to do model according to the desire application. These models include the thermal effect and trapping effects associated particularly with GaN technology. These models are good for die-level applications.

The last category is the behavior model, which is based on frequency domain measurement. These models are easy, quick, and can model die-level even packaged transistors, but they are like black-box. We don't know what is inside, and their accuracy is highly dependent on the measurement conditions. Each model has its advantages and disadvantages. The comparison between these is given in Figure 3-5 [52]

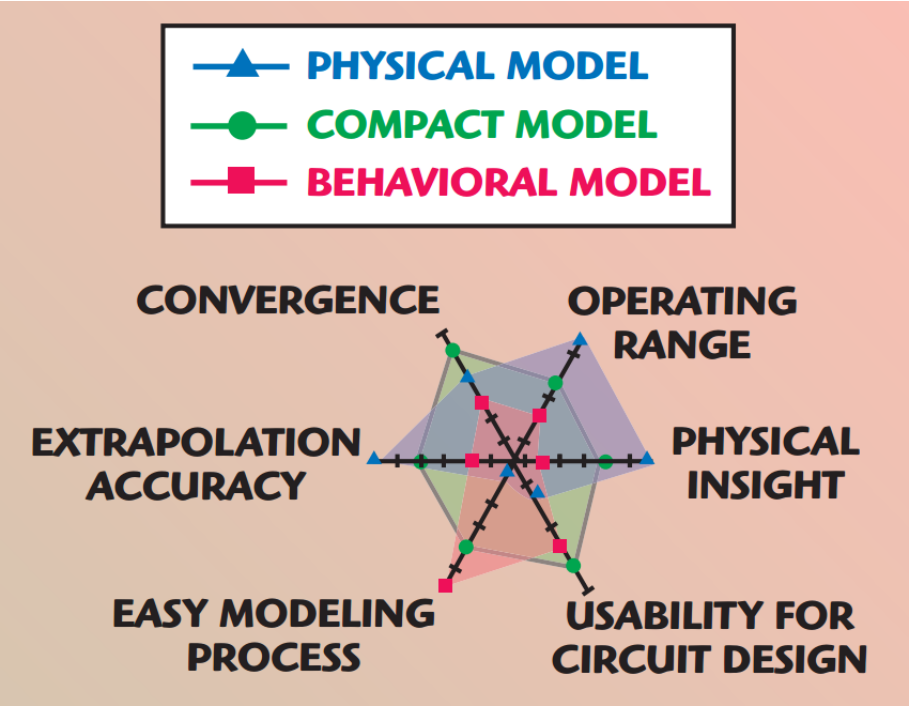


Figure 3-5: Type of large-signal models [52]

3.3.1 HEMT compact models

We can see that the best models are compact models based on different comparison parameters. To further investigate the compact models in the literature, we can find five well-known compact models given in Table 3-5.

In general, having a large number of parameters does not mean that model is accurate or gives a better fit in all conditions. In some cases, they just tried to model physical process effects or AC and DC aspects of device behavior. A large number of parameters lead to a lot of time for extraction of those parameters, trend to be more empirical and less physical, and last but not least is there is a high certainty of error in the extraction of a large number of parameters [53].

Table 3-5: Comparison of five main models [53]

FET Model	Approx. Number of Parameters	Electrothermal Model	Geometry Scalability Built-In	Original Device Context
CFET [54]	48	Yes	Yes	HEMT
EEHEMT [55]	71	No	Yes	HEMT
Angelov [56]	80	Yes	No	HEMT/MESFET
Angelov GaN [57]	90	Yes	No	HEMT
Auriga [58]	100	Yes	Yes	HEMT

There are other large-signal models exist in literature with less number of parameters such as [59]–[61] some of these require optimization procedure based on error function.

3.3.2 Transistor equivalent model

A simplified version of the equivalent model in relation to the geometrical structure is given below in Figure 3-6 [62]. In the literature, the small signal of the device has been studied extensively [63]–[69].

Pad capacitances (C_{pgs}, C_{pds}, C_{pgd}), parasitic inductances (L_g, L_s, L_d), and access resistances (R_g, R_s, R_d) are called an extrinsic parameter.

Capacitances C_{gs}, C_{ds}, C_{gd}, resistances R_{gs}, R_{ds}, R_{gd}, transconductance $g_{m,}$ and transconductance delay time or constant- τ are called intrinsic components. These all are related under the gate region, as shown in figure 3.6, with pink color. Intrinsic parameters are very important and difficult to extract.

Access Resistances ($R_g, R_{s,} R_d$): R_s and R_d are coming from the finite resistant of 2DEG and ohmic contact between metal and semiconductor, while R_g is coming from the metallization resistance of gate Schottky contact. R_s and R_d are more important in case of power gain cut-off frequency f_{max}.

Pad capacitances (C_{pgs}, C_{pds}, C_{pgd}): These are the parasitic capacitance due to the pad connection, measurement equipment, probes, and probe tip to device contact transition.

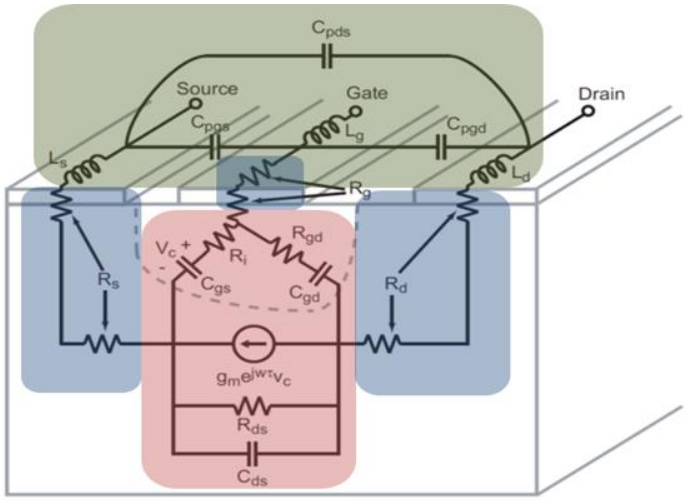


Figure 3-6: AlGaN/GaN HEMT equivalent model in relation to the geometrical structure [62]

Transconductance (g_m) is a parameter that reflects the efficiency of the I_{DS} current modulation in the channel from the voltage applied to the gate (for a constant Vds voltage).

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \qquad (3\text{-}4)$$

It can also be approximated by:

$$g_m = \frac{v_{sat}\, C_{gs}}{L_g} \qquad (3\text{-}5)$$

This expression shows the electron saturation velocity (v_{sat}) has a direct relation with transconductance. In the case of power amplifier design to get higher gain and linearity, it is usually preferred high and constant transconductance.

Capacitances (C_{gs}, C_{ds}, C_{gd}): The capacitances C_{gs} and C_{gd} reflect the change in the depletion charge with changes in V_{gs} and V_{gd}, respectively. C_{ds} accounts for the geometric capacitance effects between the source and drain electrodes; normally, it is very small. Typically C_{gs} is about 10 times the size of C_{gd} and C_{ds}. These capacitances define the unity gain frequency of the device and have an inverse relationship with the operation's maximum frequency.

Charging resistances (R_i, R_{gd}, R_{ds}): These resistances are associated with capacitances C_{gs}, C_{ds}, and C_{gd} respectively. If we want faster devices, then we need to have smaller values. Because smaller values lead to smaller charging time delay of the capacitors. As a result, we can have faster devices.

Output Transconductance (g_{ds}): It is a parameter that reflects the efficiency of the I_{DS} current modulation in the channel from the voltage applied to the gate (for a constant V_{gs} voltage). It is preferred to be small as high output resistance is required for high output power, and second, it has an inverse relation with unity gain frequency, which means its high value can cause a reduction of unity gain frequency.

$$g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} \qquad (3\text{-}6)$$

Transconductance delay τ: The drain current cannot change instantaneously and needs some time to respond to the gate voltage changes. This time is called transconductance delay or time delay τ. It also has an inverse relation with the unity gain frequency.

The physical description of each parameter is given in the following Table 3-6, Table 3-7 below:

Table 3-6: Physical description of extrinsic components

Extrinsic Elements	Physical Description
Gate inductance L_g	Inductance due to the contact of gate
Drain inductance L_d	Inductance due to the contact of drain
Source inductance L_s	Inductance due to the contact of source
Gate resistance R_g	The resistance of the gate metal strip along with the gate current flow
Drain resistance R_d	The resistance of drain access region and drain Ohmic contact
Source resistance R_s	The resistance of source access region and source Ohmic contact
Gate-source pad capacitance C_{pgs}	The capacitance between gate and source pad associated with the measurement
Drain-source pad capacitance C_{pds}	The capacitance between the drain and source pad associated with the measurement
Gate-drain pad capacitance C_{pgd}	The capacitance between gate and drain pad associated with the measurement

Extrinsic parameters independent of bias and frequency:

R_g
L_g
C_{pgs}
L_s
R_s
C_{pds}
L_d
R_d
C_{pgd}

→ **Bias and Frequency Independent**

The access resistance for drain and source also has some variation with respect to temperature:

$$\left.\begin{matrix} R_s \\ R_d \end{matrix}\right\} \longrightarrow \quad R_s = f(T)$$

Table 3-7: Physical description of intrinsic components

Intrinsic Elements	Physical Description
Gate-source fringe capacitance C_{gs}	Gate charge modulation by changing V_{GS}
Gate-drain fringe capacitance C_{gd}	Gate charge modulation by changing V_{DS}
Drain-source fringe capacitance C_{ds}	The capacitance between drain and source (e.g., substrate capacitance)
Input resistance R_i	Lumped representation of distributed channel resistances
Gate-drain resistance R_{ds}	Complement of R_i, to reflect the symmetrical nature of the device
Transconductance g_m	Drain current gain with respect to the change of gate voltage
Transconductance delay τ	Time delay between the change of gate voltage and drain current
Output Transconductance g_{ds}	Variation of drain current by the change of drain voltage

Another parameter is the gate's width, and extrinsic parameters such as inductances and parasitic capacitances increase with the increase in gate width(W. While R_g has direct relation, however, R_s and R_d are inversely proportional and decrease as W increase are given below:

$$\left.\begin{matrix} L_s \\ L_d \\ L_g \\ C_{pgs} \\ C_{pds} \\ C_{pgd} \end{matrix}\right\} \text{ increase with } \mathbf{W}$$

$$R_g\} \propto W \quad \text{and} \quad \left.\begin{matrix} R_s \\ R_d \end{matrix}\right\} \propto \frac{1}{W}$$

The intrinsic parameters are independent of frequency, so their curves should be flat during extraction with respect to frequency. Second, they are dependent on the bias, particularly C_{gs}, $C_{gd,}$ and current source. However, the current source depends on temperature also.

$$\left.\begin{matrix} C_{gs} \\ C_{gd} \end{matrix}\right\} \longrightarrow \begin{matrix} C_{gs} = f(V_{gs}, Vds) \\ C_{gd} = f(V_{gd}) \end{matrix}$$

Where

$$V_{gd} = V_{gs} - V_{ds}$$

C_{gs} has more dependency on V_{gs} as compare to $V_{ds,}$ and V_{gd} has more dependency on V_{ds} as compare to $V_{gs;}$ as a result, we can consider only C_{gs} (V_{gs}) and C_{gd} (V_{ds}) [14].

Intrinsic parameters are directly related to the gate length of the device. All capacitances and transconductance have direct proportional relation with respect to the gate length. However, the resistances have inverse proportional relation as given in the equations below:

$$\left.\begin{matrix} R_i \\ R_{gs} \\ R_{gd} \end{matrix}\right\} \propto \frac{1}{W}$$

$$\left.\begin{matrix} C_{gs} \\ C_{gd} \\ g_{m_{ins}} \end{matrix}\right\} \propto W$$

3.3.3 Small-signal modeling

3.3.3.1 Extraction methods for extrinsic parameters:

It is important to properly de-embed the extrinsic parameters of the device for proper modeling. Pad capacitances (C_{pgs}, C_{pds}, C_{pgd}), parasitic inductances (L_g, L_s, L_d), and access resistances (R_g, R_s, R_d) extraction methods are explained in this section separately.

3.3.3.1.1 Parasitic capacitance:

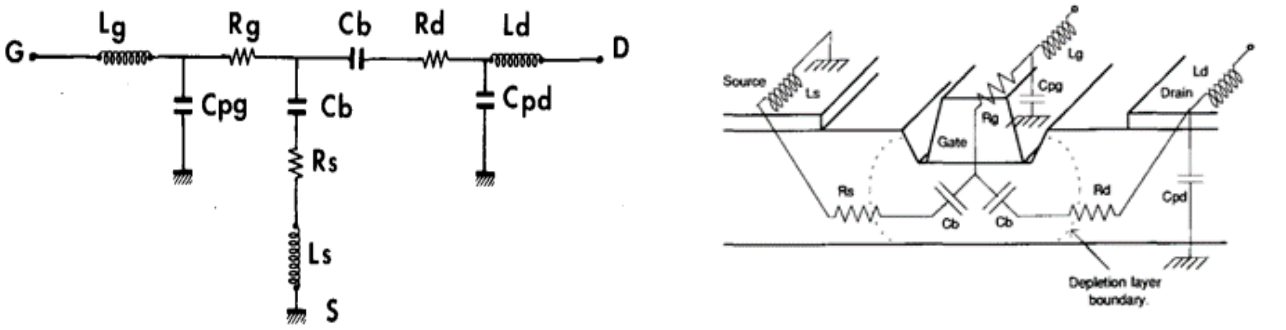
There are three common methods

1. Dambrine method
2. White method
3. Open test

1) Dambrine method

Dambrine et al. were the first to introduce a method to calculate the different elements of small-signal elements from the low-frequency measurement data. It was developed to avoid error in the optimization process [63].

He suggested that there is no conductance in the channel and parasitic gate pad capacitance (C_{pgs}) cancels at V_{ds}=0 and V_g < cut-off voltage where C_b represents the fringing capacitance due to the depletion layer extension on both sides of the gate as shown in Figure 3-7.



a) *Small-Signal equivalent circuit of a FET at zero drain bias voltage and gate voltage lower than the pinch-off voltage*

b) *Schematic cross-section of MESFET at V_{ds} = 0, showing the physical origin of elements for the equivalent circuit of Dambrine et al.*

Figure 3-7: Extraction of Parasitic capacitance [63]

For low frequency, the inductance and resistance do not influence the Y-Parameters, and we can extract the capacitance by the following equations.

$$Img(Y_{11}) = j\omega(C_{pg} + 2C_b) \quad (3\text{-}7)$$

$$Img(Y_{12}) = img(Y_{21}) = -j\omega C_b \quad (3\text{-}8)$$

$$Img(Y_{22}) = j\omega(C_{pd} + C_b) \quad (3\text{-}9)$$

For more simplicity, the following equations give the direct parasitic capacitances values:

$$C_{pg} = \frac{Img(Y_{11}+2Y_{12})}{\omega} \quad (3\text{-}10)$$

$$C_{pd} = \frac{Img(Y_{22}+Y_{12})}{\omega} \quad (3\text{-}11)$$

$$C_b = -\frac{Img(Y_{12})}{\omega} = -\frac{Img(Y_{12})}{\omega} \quad (3\text{-}12)$$

2) White method

According to White [70], the Dambrine equivalent circuit does not give asymmetric nature when we look at the input and output port. Also, C_b describes the total depletion region capacitance, which only includes drain and source. Still, it did not include gate depletion, so he proposed a new equivalent model shown in Figure 3-8.

He introduced three fringing capacitance C_b for the gate, drain, and source. The originality of these capacitances is shown in the cross-section of MESFET at V_{ds}=0, given in Figure 3-9.

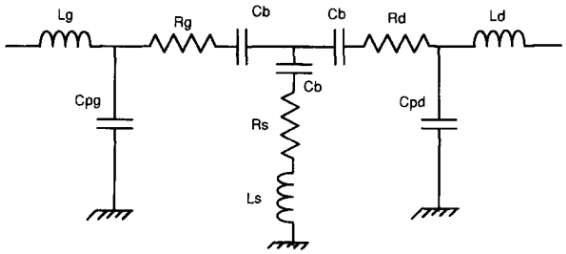


Figure 3-8: Improved equivalent circuit for pinched-off FET at V_{ds} = 0 [70]

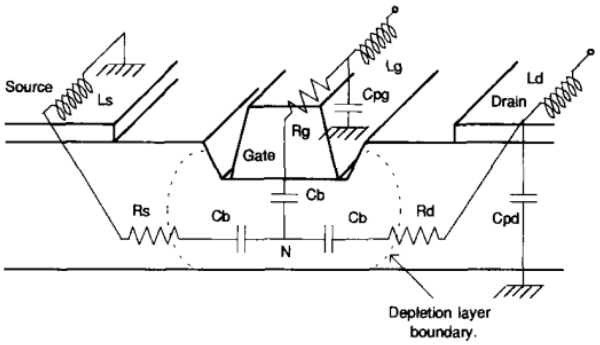


Figure 3-9: Schematic cross-section of MESFET at V_{ds} = 0 showing the physical origin of elements [70]

He found that by Dambrine's method, the C_{pd} is much higher than C_{pg}, but by his proposed method, $C_{pd} \approx C_{pg}$. The following set of equations was proposed to get the parasitic capacitance values:

$$Img(Y_{11}) = j\omega\left(C_{pg} + \frac{2}{3}C_b\right) \quad (3\text{-}13)$$

$$Img(Y_{12}) = img(Y_{21}) = -j\omega\frac{C_b}{3} \quad (3\text{-}14)$$

$$Img(Y_{22}) = j\omega\left(C_{pd} + \frac{2}{3}C_b\right) \quad (3\text{-}15)$$

So, the parasitic capacitances are directly obtained from the following equations:

$$C_{pg} = \frac{Img\left(Y_{11}+\frac{9}{2}Y_{12}\right)}{\omega} \quad (3\text{-}16)$$

$$C_{pd} = \frac{Img\left(Y_{22}+\frac{9}{2}Y_{12}\right)}{\omega} \quad (3\text{-}17)$$

$$C_b = -\frac{3Img(Y_{12})}{\omega} = -\frac{3Img(Y_{12})}{\omega} \quad (3\text{-}18)$$

3) Open Test

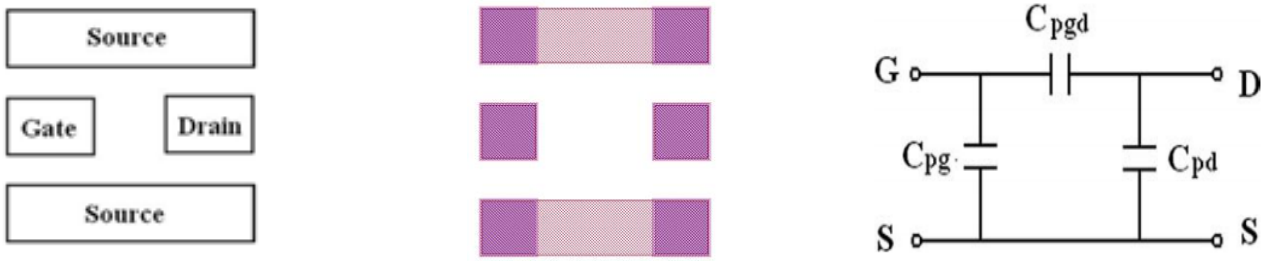
Another method to determine pad capacitances is based on an open test structure in which the pad capacitances are determined by measuring the dummy device or open structure. Those measurements are modeled by the network of the capacitances [71]. The open test structure, the layout, and its equivalent circuit are shown in Figure 3-10. These capacitance values come from the pad connection, measurement equipment, probes, and probe tip to device contact transition, so we don't need the device layout inside this structure.

The Y parameters of the Open test can be expressed as follows:

$$Img(Y_{11}) = j\omega(C_{pg} + C_{pgd}) \quad (3\text{-}19)$$

$$Img(Y_{12}) = img(Y_{21}) = -j\omega C_{pgd} \quad (3\text{-}20)$$

$$Img(Y_{22}) = jw(C_{pd} + C_{pgd}) \quad (3\text{-}21)$$



a) Open test Structure *b) Layout* *c) Equivalent Circuit*

Figure 3-10: The equivalent circuit model of the open test structure

The Pad capacitances can be directly obtained by using the following equations:

$$C_{pg} = \frac{Img(Y_{11}+Y_{12})}{\omega} \quad (3\text{-}22)$$

$$C_{pd} = \frac{Img(Y_{22}+Y_{12})}{\omega} \quad (3\text{-}23)$$

$$C_{pgd} = -\frac{Img(Y_{12})}{\omega} = -\frac{Img(Y_{12})}{\omega} \quad (3\text{-}24)$$

We have extracted pad capacitances between 2-10GHz by using all the above methods given in Table 3-8. As compared to the other two methods, values obtained by the open test method are more accurate because the size of the pad for gate and drain is the same, so we obtained quite similar values in this case. Also, it allows us to determine the small capacitance between the gate and drains pads, so based on the above analysis, we adopted an open test structure to determine pad capacitances.

Table 3-8: Pad Capacitances extracted by Dambrine, White and Open Test method

Capacitance/Method	**Dambrine**	**White**	**Open**
C_{pgs} (pF)	55.15	1.103	0.0154
C_{pds} (pF)	34.83	90.83	0.0156
C_{pgd} (pF)	-	-	0.744×10^{-3}

3.3.3.1.2 Extrinsic inductance

Commonly there are three main methods to extract or determine the values of extrinsic inductances L_g, L_s, L_d, which are the following:

1. Short test
2. Forward bias cold-FET method
3. Reverse bias cut-off method

1) Short test:

We can determine the parasitic device-connection impedances by measuring a test structure that consisted of the pads, device feed, and short channel for the transistor [71]. The test structure is modeled by a T-network, which has a series of resistances and inductances. The short test structure and equivalent model is given in Figure 3-11.

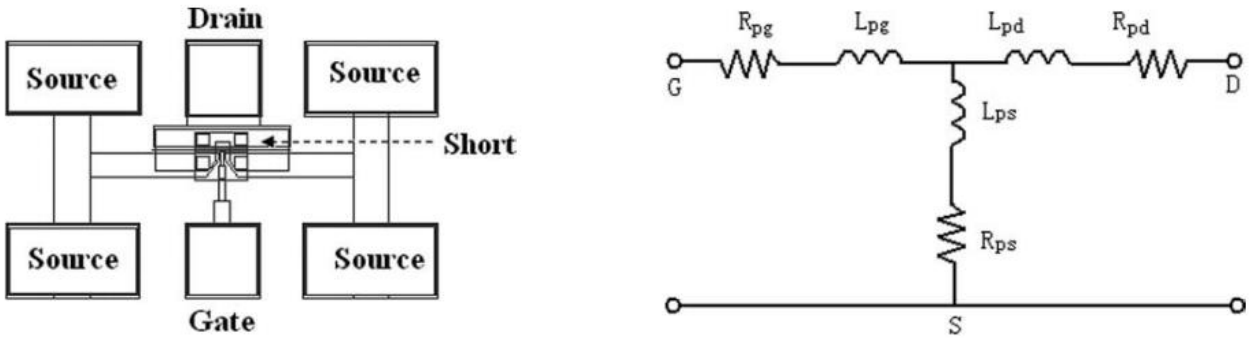
By the above model, the extrinsic inductance can be extracted by the following equations:

$$L_{pg} = \frac{Imag(Z_{11}-Z_{12})}{\omega} \quad (3\text{-}25)$$

$$L_{pd} = \frac{Imag(Z_{22}-Z_{21})}{\omega} \quad (3\text{-}26)$$

$$L_{ps} = \frac{Img(Z_{21})}{\omega} = \frac{Imag(Z_{12})}{\omega} \quad (3\text{-}27)$$

This test structure can also be used to check the feedlines losses to verify they are small enough to ignore. The real part of the above model gives us the feedlines resistance or feedlines losses. Still, we can neglect them by considered those resistances very small as compared to the access resistances.



a) Short test Structure *b) Equivalent circuit model*

Figure 3-11: Short test structure and an equivalent model.

2) Forward-biased cold-FET method

The typically high gate to source voltage is applied in this method, while zero at the drain to source. As a result, the device behaves as a passive component, which means that it has no intrinsic

capacitances and transconductance [63] to get the extrinsic inductances directly by the following equation.

$$L_g = \frac{Imag(Z_{11}-Z_{12})}{\omega} \quad (3\text{-}28)$$

$$L_d = \frac{Imag(Z_{22}-Z_{12})}{\omega} \quad (3\text{-}29)$$

$$L_s = \frac{Imag(Z_{12})}{\omega} \quad (3\text{-}30)$$

3) Reverse-biased cut-off method

The conventional forward-biased cold-FET method, applying a high forward bias point, does not work for GaN. The gate differential resistances usually require very high gate forward basing to eliminate the channel's capacitance. However, this causes unrecoverable damage to the gate. Overcome this issue, the inductances and resistances are extracted by applying a negative gate bias voltage closer to the gate's threshold voltage [72], [73].

The following equations are used to extract inductances by linear curve fitting the imaginary impedances over ω^2:

$$img(\omega Z_{11}) = \omega^2(L_s + L_g) - \left(\frac{1}{C_s} + \frac{1}{C_g}\right) \quad (3\text{-}31)$$

$$img(\omega Z_{22}) = \omega^2(L_s + L_g) - \left(\frac{1}{C_s} + \frac{1}{C_d}\right) \quad (3\text{-}32)$$

$$img(\omega Z_{12}) = \omega^2 L_s - \frac{1}{C_s} \quad (3\text{-}33)$$

The reverse-biased cut-off method has chosen because it does not put the device under stress, which causes damage to the device performance, like in the forward-biased cold-FET method. Similarly, a short test method is avoided because we need to have a short test structure of the device, so it is convenient to go with the reverse-biased cut-off method.

3.3.3.1.3 Extrinsic resistances

Extrinsic or access resistances are significant and not easy to extract. The RF or DC current-voltage performance depends on the accuracy of these resistance values: R_d, R_s, and R_g associated with drain, source, and gate, respectively. Common methods to find the access resistances are:

1. DC measurement methods
2. Reverse-biased Cold FET methods

1) DC measurement methods

Different works have been published for this method, but in each case, the primary assumption is that the Schottky diode resistance is considered to the equivalent of extrinsic resistances [73]–[78].

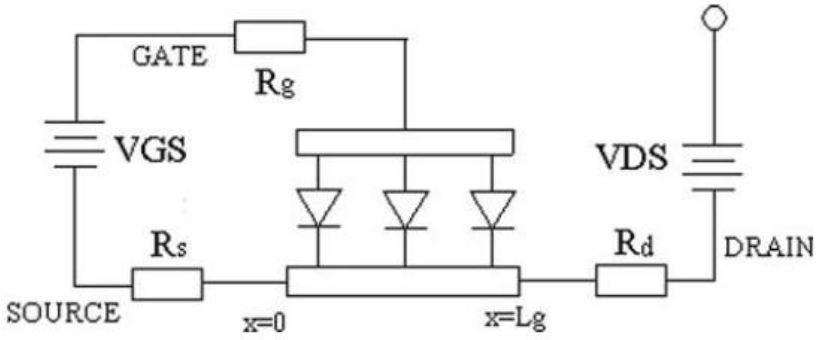


Figure 3-12: The schematic for source resistance measurement representing distributed channel, R_d and R_s for measuring $I_g(V_{ds})$ and $I_g(V_{gs})$ [75]

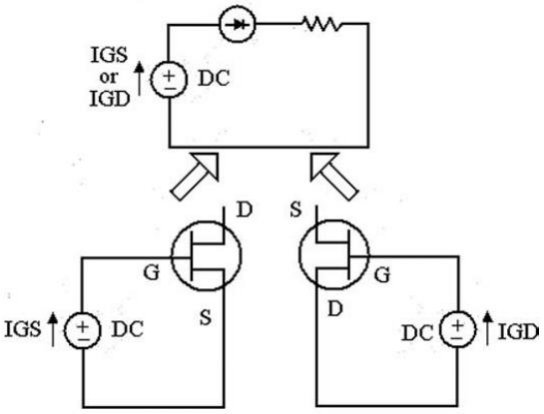


Figure 3-13: Schottky diode model for FET with a floating drain or source [75]

Figure 3-12 is the schematic for source resistance measurement, representing channel resistance R_c and R_s, R_d [75]. The gate of the device is considered as a distributed diode model and $I_d >> I_g$. The channel resistance is not dependent on the position, so for determining R_s and R_d, we need two measurements $I_g(V_{ds})$ and $I_g(V_{gs})$, with the floating drain and source [75], [76], [78]. Figure 3-13 explains the measurement technique.

2) Reverse-biased Cold FET methods

This method is based on the device's symmetry at zero drains to a source bias voltage, but the high negative gate to source voltage (close to threshold voltage). It was initially derived for the extraction of the extrinsic parameters of GaAs MESFET. In this method, the distributed RC network is considered under the gate. The effect of parasitic Schottky barrier capacitance is ignored because of the high value of the Schottky barrier resistance used by [63] but derived initially from [74].

$$Z_{11} = R_g + R_s + j\omega\left(L_g + L_s\right) + \frac{1}{j\omega}\left(\frac{1}{C_g} + \frac{1}{C_s}\right) + \delta Z_g \qquad (3\text{-}34)$$

$$Z_{22} = R_d + R_s + j\omega(L_d + L_s) + \frac{1}{j\omega}\left(\frac{1}{C_d} + \frac{1}{C_s}\right) + \delta Z_d \qquad (3\text{-}35)$$

$$Z_{12} = Z_{21} = R_s + j\omega L_s + \frac{1}{j\omega C_s} + \delta Z_s \qquad (3\text{-}36)$$

Where

$$\delta Z_g = \delta R_g + \delta R_s + jw\left(\delta L_g + \delta L_s\right)$$

$$\delta Z_d = \delta R_d + \delta R_s + jw(\delta L_d + \delta L_s)$$
$$\delta Z_s = \delta R_s + jw\delta L_s$$

Ignoring the correction term for intrinsic parameters δZ_g, δZ_d, $\delta Z_s$and multiplying with ω^2 then the real part is:

$$\omega Re[Z_{11}] = \omega(R_s + R_g) \quad (3\text{-}37)$$

$$\omega Re[Z_{22}] = \omega(R_d + R_s) \quad (3\text{-}38)$$

$$\omega Re[Z_{12}] = \omega R_s \quad (3\text{-}39)$$

The cold-FET method is chosen for the extrinsic resistance measurement due to its simplicity and direct approach. Besides that, we can extract these resistance values from the same measurement file, which we have used for extrinsic inductance value extraction.

3.3.3.2 Extraction methods for intrinsic parameters:

The typical intrinsic model with the leakage between forwarding gate-source resistance (R_{gfs}) and forward gate-drain resistance (R_{fgd}) is given in Figure 3-14. For the extraction of intrinsic parameters, we need to have the intrinsic Y matrix. For this purpose, we need to de-embed the extrinsic parameters from the measurement file [63].

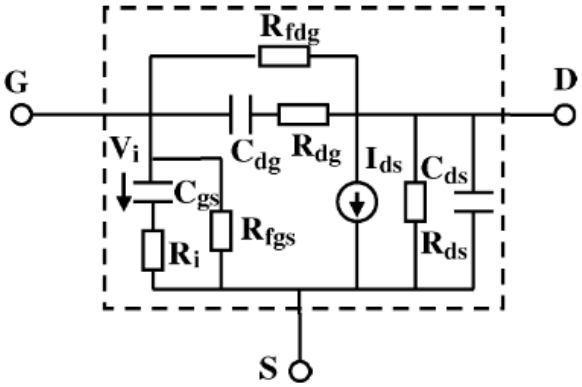


Figure 3-14: Intrinsic part of the proposed 18-element small-signal model [72]

3.3.3.2.1 De-embedding of extrinsic components

The de-embedding is done in the following way:

1. We have the Y extrinsic matrix Y_{Pad} from measurement obtained from S-measurement
2. Pad capacitances are in π-network or pi-network, so it's easy to make subtraction through the admittance matrix.

$$Y_{Pad} = j\omega \begin{bmatrix} C_{pg+}C_{pgd} & -C_{pgd} \\ -C_{pgd} & C_{pd} + C_{pgd} \end{bmatrix} \quad (3\text{-}40)$$

$$Y_{Pad\ De-embed} = Y_{meas} - Y_{Pad} \quad (3\text{-}41)$$

3. To de-embed Inductance, since these are in delta(Δ)-network shape, so the impedance matrix is a better choice, so first, convert $Y_{Pad\ De-embed}$ convert into $Z_{Pad\ De-embed}$ then subtract $Z_{Inductance}$ from it.

$$Z_{Inductance} = j\omega \begin{bmatrix} L_{g+}L_s & L_s \\ L_s & L_{d+}L_s \end{bmatrix} \quad (3\text{-}42)$$

$$Z_{Inductance\ De-embed} = Z_{Pad\ De-embed} - Z_{Inductance} \quad (3\text{-}43)$$

4. Like inductance, access resistances are also in the Δ-network. As a result, we can de-embed in the same way.

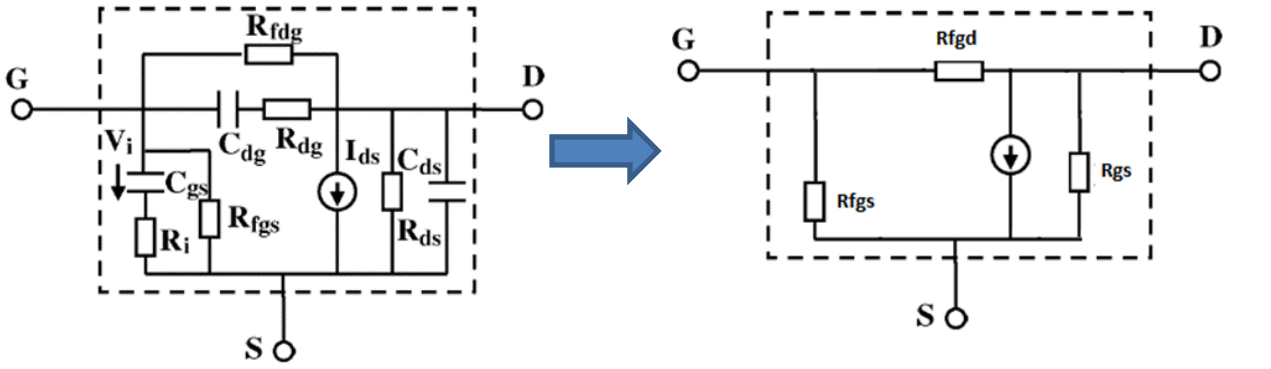
$$Z_{Access_R} = \begin{bmatrix} R_{g+}R_s & R_s \\ R_s & R_{d+}R_s \end{bmatrix} \quad (3\text{-}44)$$

$$Z_{Int} = Z_{Inductance_{De-embed}} - Z_{Access_R} \quad (3\text{-}45)$$

We could de-embed parasitic inductance and access resistances together to simplify steps. From Z_{Int} the matrix we can easily have Y_{Int} from which we can extract the intrinsic components.

3.3.3.2.2 Extraction procedure of the intrinsic components

After having the intrinsic impedance/admittance, we can extract the intrinsic parameters: Cgs, Cds, Cgd, Rgs, Rgd, Rds, gm, and t, and leakage resistance R_{fgs} and R_{fgd}. These leakage resistances can be extracted easily at low frequency by the equations because capacitors C_{gs} and C_{ds} become open circuit and lead to the circuit given in Figure 3-15, as shown below.



Small-signal model *a) A simplified circuit for extraction of resistances*

Figure 3-15: Intrinsic structure and an equivalent model.

Procedure:

1. Extract the R_{fgs} and R_{fdg} at low frequencies (400MHz-1200MHz)

$$R_{fdg} = -\frac{1}{real(Yint(1,2))} \quad (3\text{-}46)$$

$$R_{fgs} = \frac{1}{real(Yint(1,1)+Yint(1,2))} \quad (3\text{-}47)$$

where 1:port-1 and 2: port-2 inside Y_{int}

2. De-embed these and get Y intrinsic without leakage, as shown in Figure 3-16. After using the usual eight elements equations (3.46-3.51) given below for extraction of the remaining element.

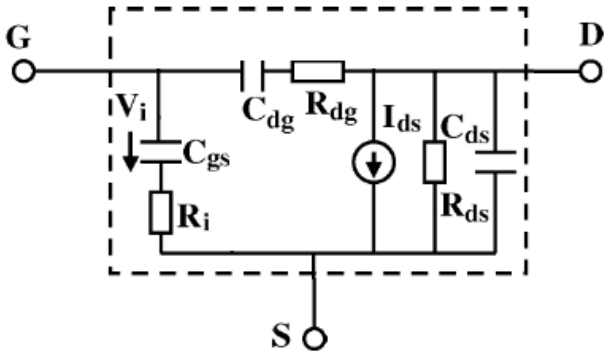


Figure 3-16: Classical Small-Signal Model

Small leakage current typically in the nA scale leads to high values of the R_{fgs} and R_{fgd}, which give us an open circuit; consequently, we can ignore them. There are different methods and set of the equation in the literature for the remaining eight-element extractions of the intrinsic components.

For example, in [72], they defined intrinsic functions for each intrinsic component at different frequencies to extract their values at all frequencies points. These set of equations are given below:

$$C_{gs}R_i = \frac{real(Y_1(\omega+\Delta\omega)-Y_1(\omega))}{(\omega+\Delta\omega)\times imag(Y_1(\omega+\Delta\omega))-\omega imag(Y_1(\omega))} \quad (3\text{-}48)$$

$$R_{fgs}{}^{-1} = real[Y_1(\omega)] - \omega imag[Y_1(\omega)]\ (C_{gs}R_i) \quad (3\text{-}49)$$

$$\omega C_{gs} = imag[Y_1(\omega)] \times \left[1 + \left(\omega C_{gs}R_i\right)^2\right] \quad (3\text{-}50)$$

where $Y_1 = Y_{11,int} + Y_{12,int}$

Similarly, for $C_{gd}, R_{gd}\ and\ R_{fgd}$

$$C_{gd}R_{gd} = \frac{real(Y_2(\omega+\Delta\omega)-Y_2(\omega))}{(\omega+\Delta\omega)\times imag[Y_2(\omega+\Delta\omega)]-\omega imag[Y_2(\omega)]} \quad (3\text{-}51)$$

$$R_{fgd}{}^{-1} = real[Y_2(\omega)] - \omega imag[Y_2(\omega)]\ (C_{gd}R_{gd}) \quad (3\text{-}52)$$

$$\omega C_{gd} = imag[Y_2(\omega)] \times \left[1 + \left(\omega C_{gs}R_i\right)^2\right] \quad (3\text{-}53)$$

where $Y_2 = -Y_{12,int}$

A sufficient number of frequency points are required to have enough data points to avoid errors introduced by measurement. The remaining components $R_{ds}{}^{-1}, C_{ds}, g_{m,int}\ and\ \tau$ can be found by the following set of equations:

$$R_{ds}{}^{-1} = real\left[Y_{12,int} + Y_{22,int}\right] \quad (3\text{-}54)$$

$$\omega . C_{ds} = imag\left[Y_{12,int} + Y_{22,int}\right] \quad (3\text{-}55)$$

$$g_{m,int} = \left|\left(Y_{12,int} + Y_{21,int}\right)\left[1 + j\omega\left(C_{gs}R_i\right)\right]\right| \quad (3\text{-}56)$$

$$\omega\tau = tan^{-1}\left[\frac{imag\{(Y_{12,int}+Y_{21,int})[1+j\omega(C_{gs}R_i)\}}{real\{(Y_{12,int}+Y_{21,int})[1+j\omega(C_{gs}R_i)\}}\right] \quad (3\text{-}57)$$

The extracted intrinsic parameters with the equations, as mentioned above, are shown in Figure 3-17. The intrinsic parameters are independent of frequency, particularly R_{dg} and R_i, flat even at lower frequencies due to R_{fdg} and R_{fgs} parameters. The independence of these parameters from frequency also indicates that the extrinsic parameters are properly de-embedded.

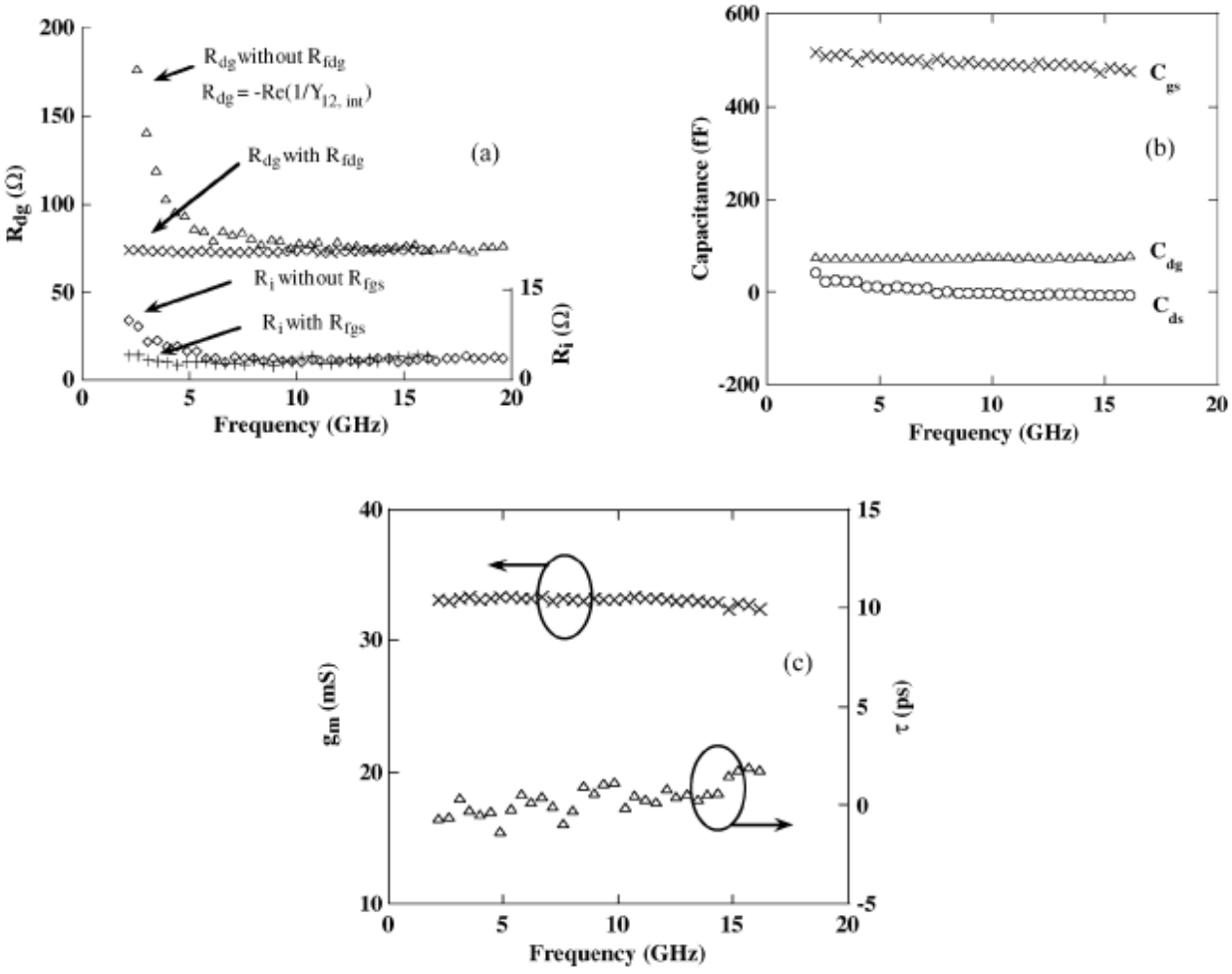


Figure 3-17: Optimized intrinsic elements from the data measured at V_{DS}= 4 V, V_{GS} = -3 V, and frequencies from 2 to 20 GHz. (a) R_i and R_{dg}, with and without the differential resistances R_{fdg} and R_{fgs} considered. (b) C_{dg}, C_{gs}, and C_{ds}. (c) g_m and τ [72].

Another way is given in [64] they explained to extract by linear interpolation and claimed that the model also includes the decency on low frequency. Besides the difference in extraction technique in this method, they considered leakage resistance only across the capacitances (C_{gs} and C_{gd}). For this method, the following set of the equation is used.

The admittance between gate-source is given:

$$Y_{gs} = Y_{11,int} + Y_{12,int} = \frac{G_{fgs}+j\omega C_{gs}}{1+R_i.G_{fgs}+j\omega.R_i.C_{gs}} \quad (3\text{-}58)$$

By defining a new variable D as

$$D = \frac{|Y_{gs}|^2}{imag[Y_{gs}]} = \frac{{G_{fgs}}^2}{\omega C_{gs}} + \omega C_{gs} \quad (3\text{-}59)$$

and by multiplying both sides with ω

$$\omega D = \frac{\omega|Y_{gs}|^2}{imag[Y_{gs}]} = \frac{{G_{fgs}}^2}{C_{gs}} + \omega^2 C_{gs} \quad (3\text{-}60)$$

C_{gs} can be determined by the slope of the curve if plotted vs ω^2 by the linear fitting. However, by redefining D' as:

$$\omega D' = \frac{\omega|Y_{gs}|^2}{imag[Y_{gs}]} = \frac{G_{fgs}(1+R_i G_{fgs})}{C_{gs}} + \omega^2 R_i C_{gs} - j\omega \quad (3\text{-}61)$$

We can find R_i from the real part, by linear fitting and G_{fgs} also from the real part but at low frequencies (MHz range).

The admittance between gate-drain is given:

$$Y_{gd} = -Y_{12,int} = \frac{G_{fgd}+j\omega C_{gd}}{1+R_{gd}.G_{fgd}+j\omega.R_{gd}.C_{gd}} \quad (3\text{-}62)$$

In the same way, as did above, we can have $G_{fgd}, R_{gd}\ and\ C_{gd}$.

The transconductance branch admittance is:

$$Y_{gm} = Y_{21,int} - Y_{12,int} = \frac{G_m e^{-j\omega}}{1+R_i G_{fgs}+j\omega C_{gs}} \quad (3\text{-}63)$$

By redefining D'' as:

$$D'' = \left|\frac{Y_{gs}}{Y_{gm}}\right|^2 = \left(\frac{G_{fgs}}{G_m}\right)^2 + \left(\frac{C_{gs}}{G_m}\right)^2 \omega^2 \quad (3\text{-}64)$$

g_m can be found by the slope of live verses ω^2 and τ can be extracted by the following equation:

$$D'' = \left(G_{fgs} + j\omega C_{gs}\right)\frac{Y_{gm}}{Y_{gs}} = G_m e^{-j\omega\tau} \quad (3\text{-}65)$$

C_{ds} and G_{ds} can be determined by the admittance matrix between drain-source from imaginary and real parts, respectively, by linear fitting given below in Figure 3-18. The non-linear capacitance and transconductance are independent of frequency mean they are extracted well.

$$Y_{ds} = Y_{22,int} - Y_{12,int} = G_{ds} + j\omega C_{ds} \quad (3\text{-}66)$$

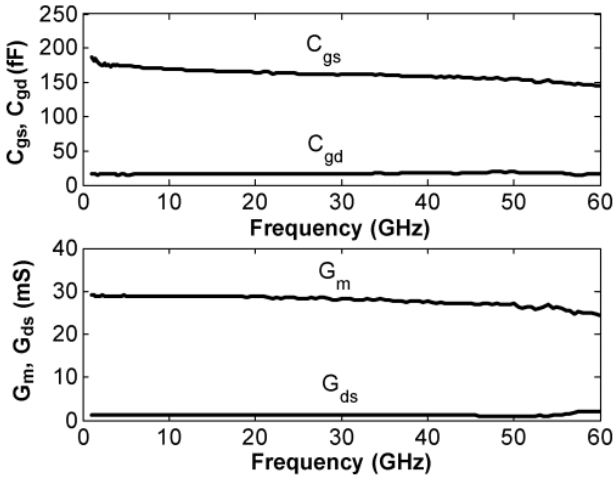


Figure 3-18: Extracted intrinsic capacitances and conductances versus frequency, at V = 1:0 V and V = 10:0 V, for a 0.5 um GaN HEMT with a 250 um gatewidth [72].

But all these extraction procedures are somehow related to the GaAs model extraction [79], [80]. The most straightforward set of the equations are the following, which I am using in my model:

$$C_{gd} = \frac{1}{\omega Imag\left(\frac{1}{Y_{12}^{DUT,int}}\right)} \tag{3-67}$$

$$C_{gs} = \frac{1}{\omega Imag\left(\frac{1}{Y_{11}^{DUT,int}+Y_{12}^{DUT,int}}\right)} \tag{3-68}$$

$$C_{ds} = \frac{Imag\left(Y_{12}^{DUT,int}+Y_{22}^{DUT,int}\right)}{\omega} \tag{3-69}$$

$$R_{gs} = Real\left(\frac{1}{Y_{11}^{DUT,int}+Y_{12}^{DUT,int}}\right) \tag{3-70}$$

$$R_{ds} = Real\left(\frac{1}{Y_{12}^{DUT,int}+Y_{22}^{DUT,int}}\right) \tag{3-71}$$

$$g_m = \left|\frac{\left(Y_{12}^{DUT,int}-Y_{21}^{DUT,int}\right)\left(Y_{11}^{DUT,int}+Y_{12}^{DUT,int}\right)}{Imag\left(Y_{11}^{DUT,int}+Y_{12}^{DUT,int}\right)}\right| \tag{3-72}$$

$$\tau = \frac{\frac{\pi}{2}-phase\left(Y_{12}^{DUT,int}-Y_{21}^{DUT,int}\right)+phase\left(Y_{11}^{DUT,int}+Y_{12}^{DUT,int}\right)}{\omega} \tag{3-73}$$

$$R_{gd} = -Real\left(\frac{1}{Y_{12}^{DUT,int}}\right) \tag{3-74}$$

All intrinsic elements are supposed to be independent of frequency. If they are not flat, they depend on the frequency, and extracted extrinsic parameters are not correct. Matlab can be beneficial to make this process optimization. After optimization, we take value only where these components are independent of frequency, and from there, we can construct the model Y matrix. The results of the extraction will be presented in Chapters 4 and 5 in detail.

3.3.3.3 Cut-off frequencies:

Once we have the small-signal parameters, we can estimate the current gain cut-off frequency f_T and power gain cutoff frequency f_{max}. The current gain cut-off frequency is given as [81]

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \quad (3\text{-}75)$$

It can be improved by reducing C_{gs} or by increasing g_m which can be done by increasing the electron velocity and/or reducing gate length. C_{gd} has small variation as compared to C_{gs} means C_{gs} has more influence on f_T.

Power gain cut-off frequency f_{max} at which the power gain of the device reduces to unity is given [82]

$$f_{max} = \frac{f_T}{2\sqrt{(R_g+R_i+R_s).g_{ds}+2\pi f_T R_g C_{gd}}} \quad (3\text{-}76)$$

To improve f_{max} we also need to minimize the parasitic resistance R_s, R_g and C_{gd}.

3.3.4 Large signal modeling

3.3.4.1 Current source modeling

The intrinsic current source consists of a function describing Drain current I_d with respect to bias and temperature [83] such as:

$$I_d = Wqn_s\left(V_{gs}^{int}\right)v\left(V_{ds}^{int},T\right) \quad (3\text{-}77)$$

Where

q: electron charge,
W: total gate width,
n_s: electron density
v: electron drifts velocity.
A_1, A_2, A_3: Constant, fitting parameters

Electron density is expressed as follows:

$$n_S\left(V_{gs}\right) = n_{s_0}.A_1.ln\left(1+exp\left(\frac{V_{gs}+A_2}{A_3}\right)\right) \quad (3\text{-}78)$$

The electron drift velocity makes use of the Canali model [84], which yields:

$$v\left(V_{ds}^{int},T\right) = \frac{\mu(T).E\left(V_{ds}^{int}\right).v_{SAT}(T)}{\left(\left(\mu(T).E\left(V_{ds}^{int}\right)\right)^{\beta}+v_{SAT}^{\beta}(T)\right)^{\frac{1}{\beta}}} \quad (3\text{-}79)$$

Where E is the longitudinal electric field expressed as:

$$E\left(V_{ds}^{int}\right) = \frac{V_{ds}^{int}}{L_g} \quad (3\text{-}80)$$

and μ and v_{SAT} are the mobility and the saturation drift electron velocity respectively. From [85], it is deduced that μ dependent on the temperature for thermal modeling.

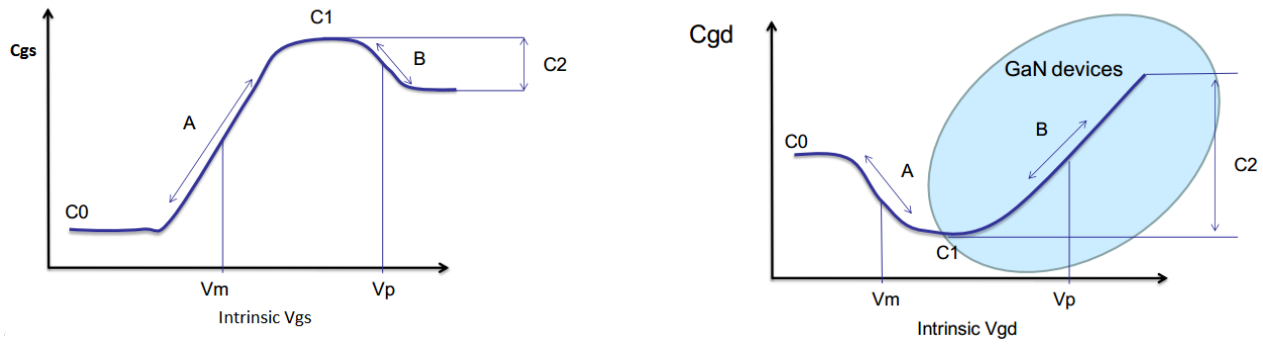
$$\mu(T) = \mu_0.\left(\frac{T}{T_0}\right)^{-\alpha} \quad (3\text{-}81)$$

$$v_{SAT}\ (T) = \frac{v_{SAT_0}}{1+a_n\left(\frac{T}{T_0}-1\right)} \quad (3\text{-}82)$$

There are other methods for large-signal current source models such as Curtice [86], [87], Statz model [88], and Angelov model [89], [90]. For comparison, Statz gives a nice fit for the current source's saturation region but is not accurate for the linear region and doesn't give a decent g_m model. The Curtice model for current has a problem from low to high V_{gs} similarly very bad for transconductance modeling. Angelov model gives a very nice fit for both current and transconductance.

3.3.4.2 Nonlinear capacitance modeling

Angelov model [89], [90], also model C_{gs} and C_{gd}. This model is based on the empirical model, and each non-linear capacitance C_{gs} and C_{gd} depends on both V_{gs} and V_{ds}. However, Forestier et al. [91] have shown that non-linear capacitance dependency on one variable is enough. The error is within the limit compared to these capacitances dependence on both V_{gs} and V_{ds}. This model is a compact model in which C_{gs} depends on V_{gs}, and C_{gd} depends on V_{gd}. The typical behavior of these capacitances is shown in Figure 3-19, where A and B are the line slope while C1 is constant.



a) Cgs vs. Vgs *b) Cgd vs. Vgd*

Figure 3-19: General behavior of non-linear capacitances vs. voltages

The modeling equation of these nonlinear capacitances are the following where A and B are slopes:

$$C_{gs} = C_{gs0} + \frac{C_{gs1}-C_{gs0}}{2}\left[1+tanh\left(A.\left(V_{gs}+V_m\right)\right)\right] - \frac{C_{gs2}}{2}\left[1+tanh\left(B.\left(V_{gs}+V_p\right)\right)\right] \quad (3\text{-}83)$$

$$C_{gd} = C_{gd0} + \frac{C_{gd1}-C_{gd0}}{2}\left[1+tanh\left(A.\left(V_{gs}+V_m\right)\right)\right] - \frac{C_{gs2}}{2}\left[1+tanh\left(B.\left(V_{gd}+V_p\right)\right)\right] \quad (3\text{-}84)$$

The charge equations:

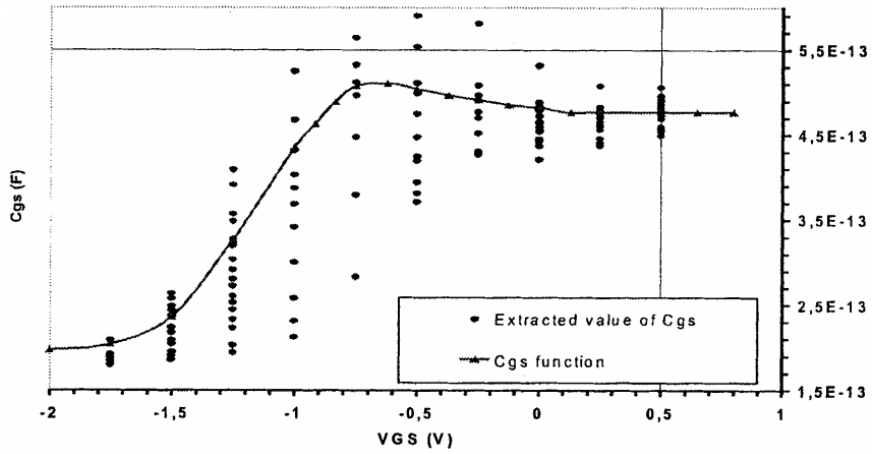
$$Q_{gs} = \int C_{gs}(V_{gs})\, dV_{gs} \qquad (3\text{-}85)$$

$$Q_{gs} = C_{gs0}V_{gs} + \frac{C_{gs1}-C_{gs0}}{2}\left[V_{gs} + \frac{Log\{\cos h(A.(V_{gs}+V_m))\}}{A}\right] - \frac{C_{gs2}}{2}\left[V_{gs} + \frac{Log\{\cos h(B.(V_{gs}+V_p))\}}{B}\right] \qquad (3\text{-}86)$$

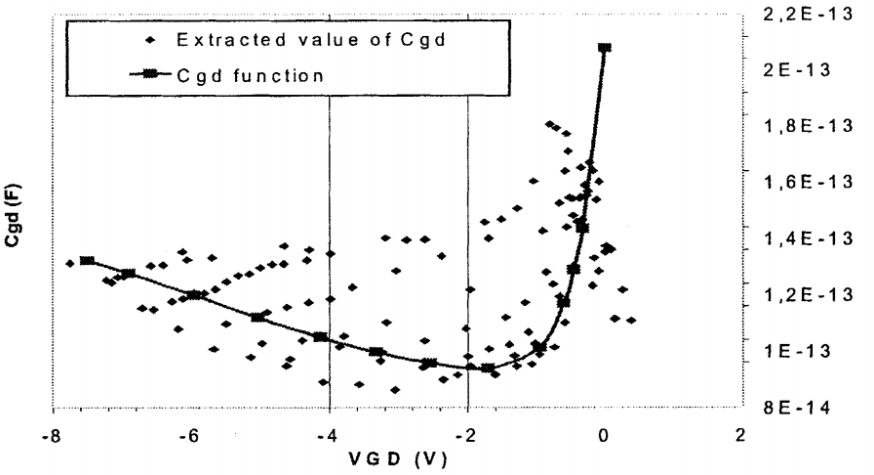
$$Q_{gd} = \int C_{gd}(V_{gd})\, dV_{gd} \qquad (3\text{-}87)$$

$$Q_{gd} = C_{gd0}V_{gs} + \frac{C_{gd1}-C_{gd0}}{2}\left[V_{gd} + \frac{Log\{cosh(A.(V_{gd}+V_m))\}}{A}\right] - \frac{C_{gd2}}{2}\left[V_{gs} + \frac{Log\{cosh(B.(V_{gs}+V_p))\}}{B}\right] \qquad (3\text{-}88)$$

The modeled and extracted capacitances are shown in Figure 3-20 from [91]:



a) Several data points show a variation of C_{gd} vs. V_{gd} with a fitting curve



b) Several data points show a variation of C_{gs} vs. V_{gs} with fitting curve

Figure 3-20: Comparison of non-linear Capacitances [91] (a) C_{gd} vs. V_{gd} and (b) C_{gs} vs. V_{gs}.

Having stated all about the device's modeling, we realized that the problem lies with large gate resistance device modeling. All traditional techniques are developed and used for small gate width transistors that were correct in the past. Due to technology advances and higher power-hunger demand to go the higher gate width to benefit the advantages offered by GaN devices fully. The traditional gate resistance model is based on lumped components that need to reconsider as the gate's width goes into hundreds of microns, more than the usual tens of microns size. We proposed a new model based on a distributed gate along the transistor's width to overcome this issue, which is a better representation physically. The intrinsic parameters are considered distributed as well; however, they remain constant throughout the structure, as shown in Figure 3-21. The model extraction procedure and the size of gate width vs. modeling differences are demonstrated in Chapter 4.

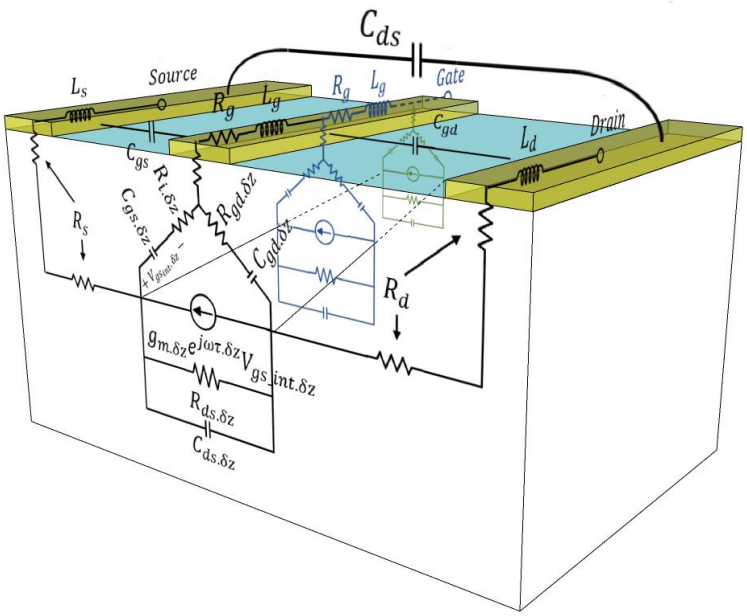


Figure 3-21: 3D representation of AlGaN/GaN HEMT structure and the proposed new large-signal electrical model.

To summarize out all methods, we have used the following methods for extraction of the parameters: The pad capacitances are extracted from open test structure through cold pinch-off on-wafer measurement [71]. While access resistance R_s and R_d are obtained by reverse-biased cut-off method (cold-FET) [35, 36]. Gate metal sheet resistance ($R_{g\square}$) is directly measured by using on wafer 4-probes measurement setup. The access inductances L_s, L_d, and L_g, are extracted by the cold-FET method [32, 37]. All intrinsic parameters extracted from the newly developed distributed gate resistance method described in Chapter 4 with intrinsic parameter equations defined in [79], [80], after de-embedding the extrinsic parameters [92]. The intrinsic Drain current I_d with respect to bias and temperature in modeled by Adrien et al. [83]. Forestier et al. [91] have provided that non-linear capacitances model which is being used in our approach because of its dependency on one bias voltage. Results for current source and capacitances modeling has been presented in Chapter 5 with details.

Chapter 4: Introduction to distributive gate resistance

Introduction

This article contributes to the thesis by demonstrating the small-signal modeling based on distributive gate resistance modeling. It presents the development and validation of the distributive gate resistance model. A new set of equations were derived for the intrinsic matrix based on distributed gate resistance. The distributed model extraction procedure and extraction methods are explained from extrinsic parameters to an intrinsic level. Afterward, in the results, a comparison is presented between the classical model (lumped model) and the distributed model. A comparison is done between the measured, the classic, and distributed model for f_T and f_{max} for four developments (0.25, 0.5, 1, and 2mm).

The group members fabricated the devices; however, I was part of the meetings to discuss the technological challenges and difficulties. Once received fabricated wafers, my contribution was to performed DC and RF measurements to characterize the device. It also includes the development of the new model; then later performed a comparison between simulated results and measurement data.

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Résumé

Ce papier présente une nouvelle méthode pour extraire les caractéristiques intrinsèques à deux ports d'un transistor à haute mobilité électronique en connaissant la distribution de la résistance de la grille et sa résistance carrée. La procédure est directe. elle consiste à séparer (de-embedding) les éléments parasites extrinsèques et les résistances d'accès, à mesurer la résistance carrée de la grille et de finalement extraire les paramètres intrinsèques en utilisant un modèle d'équation proposé. Elle peut être intégré dans la plupart des approches de modélisation en utilisant des schémas électriques équivalents. Cette méthode originale est menée expérimentalement sur des MOSHEMT AlGaN / GaN sur substrat Si présentant quatre largeurs de grille différentes W (0,25, 0,5, 1, 2 mm). L'intérêt d'une telle procédure d'extraction est de montrer sa pertinence pour la modélisation des transistors de puissance GaN dont la largeur de grille est supérieure à 500 µm, cde qui indique sa forte pertinence pour la modélisation des transistor GaN de grande largeur de grille pour l'électronique de puissance. Dans le cas de fT et fmax, le modèle classique présente des variations allant jusqu'à 17,5% et 9,2% par rapport à la mesure, tandis que le modèle distribué ne présente que 2,8% et 1,3% respectivement à W = 2 mm, ce qui souligne l'importance de modèle de la grille distribuée pour les dispositifs large de GaN HEMT.

Large Periphery GaN HEMTs Modeling Using Distributed Gate Resistance

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Keywords: GaN, HEMT, modeling, distributed gate resistance

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4.1 Abstract

This paper reports on a new method to extract the intrinsic two-port characteristics of a high-electron-mobility-transistor considering the gate resistance distributed nature, knowing the gate metal sheet resistance. The procedure is straightforward. It consists of de-embedded the extrinsic parasitic elements and access resistances, measures the gate metal sheet resistance, and finally extracting the intrinsic parameters by a proposed set of direct equations. It can be integrated into most modeling approaches using electrical equivalent schematics. This original method is experimentally conducted on AlGaN/GaN MOSHEMTs on Si substrate featuring four different gate widths W (0.25, 0.5, 1, 2mm). The interest of such an extraction procedure is shown for devices with gate width above 500µm, which indicates its strong relevance for the modeling of large gate width GaN transistors for power electronics. In the case of f_T and f_{max}, the classical model has variation up-to 17.5% and 9.2% with respect to measurement. In comparison, the distributed model has only 2.8% and 1.3% respectively at W=2mm, which emphasized the significance of the distributed gate resistance model for large periphery GaN HEMT devices.

4.2 Introduction

GaN HEMT technology appears to be a very promising candidate for the future of power electronics, and RF integrated electronics owing to GaN semiconductor very favorable transport properties and breakdown voltage leading to an efficient high-power system [93]. The significance of this technology further increases due to its advancement in high-power wireless applications [94], THz power applications [95]–[97], space [98], and power electronics applications [99].

Scaling of current rating for power applications requires increasing the HEMTs total gate widths in order to minimize on-state losses by diminishing on-resistance. A consequence of increasing the device periphery is the increase of parasitic elements such as the extrinsic inductances, capacitances, and gate resistance.

Increasing the number of fingers leads to a decrease in the total gate resistance but adds to the design complexity. Precise modeling of the effect of long gate effects is thus required to choose the best trade-off. For sufficiently small devices, linear dependencies of the parasitic elements with the

total gate width can be assumed. However, some works highlighted the need to consider a distributed model for simulation, extraction of extrinsic and intrinsic elements [100]–[102].

Several works have pointed out the necessities of using a distributed model of the internal gate resistance for Field Effect Transistors (FETs) featuring long gate fingers (W_f) mostly for the CMOS technology [103]–[106] and large gate-periphery GaN HEMTs [107]. Such works have expressed the benefits of such representation to accurately model the impact of gate resistance on cut-off frequency (f_T), the maximum frequency of oscillation (f_{max}) [105], noise parameters [106], and transconductance [108]. To our knowledge, state-of-the-art GaN MMIC circuits use models with lumped gate resistance [109]–[113]. This paper makes it possible for the first time to highlight the interest of considering the distributed gate resistance on the performance of the GaN transistor and MMIC associated with it.

Recent progress in GaN HEMTs for power electronics [114]–[117] have pushed for very large periphery devices with large finger widths and large input capacitance (C_{iss}). For power switching, gate resistance has a drastic effect on switching times [118] and losses [119] in reason of the high displacement gate current occurring during commutation. Layout optimization [120] to maximize both power density and switching performance is required and thus considers the finger width as a crucial parameter to ensure acceptable values of R_g.

Consequently, precise modeling of the gate resistance for large finger widths is necessary and must account for the distributed effect on the transistor input capacitance charge. However, in modeling, strong similarities remain between such devices and the ones used for RF applications. The representation of the gate access resistance still consists of a lumped element [121], as shown in Figure 4-1. Furthermore, extraction of access resistances and intrinsic elements also consider a lumped representation of R_g [122].

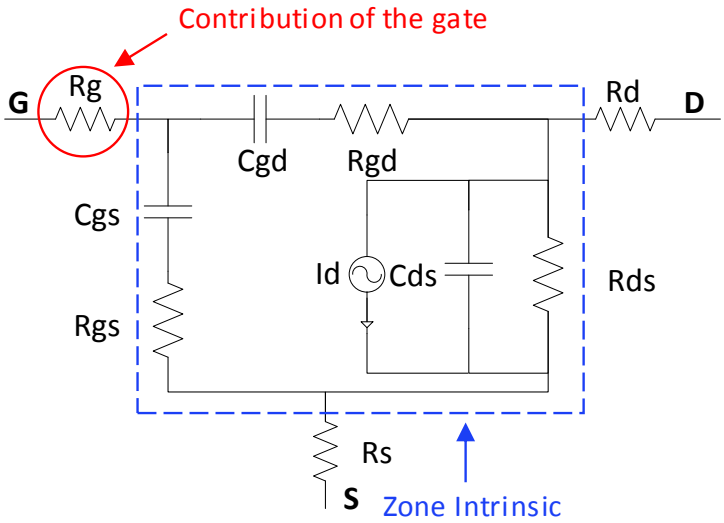


Figure 4-1: Classic small-signal model.

The linear gate resistance modeling is given in Eq. (1) [105], [123] where N is the number of fingers, W is the width, and L is the length of the transistor, and $R_{\square}$ is the sheet resistance of the gate metal. This equation is derived on the assumption that the gate width is small and assumes a lumped gate resistance equal to 1/3 of the total gate resistance in the case where the gate finger is connected only at one end and equal to 1/12 when the gate is connected at both ends [123].

$$R_g = \frac{R_{\square} W}{3N^2 L} \qquad (4\text{-}1)$$

In this letter, we introduce an original general method to extract the intrinsic characteristics of a HEMT considering R_g as a distributed element, as shown in Figure 4-2. To the author's knowledge, this is the first time that such a method is presented for GaN HEMTs. While studies have already dealt with the distributed effect of R_g for the matter of simulation accuracy [108] or for the extraction of specific intrinsic representations [106], this work presents a general procedure adaptable to any further modeling of the intrinsic region. Moreover, this paper accesses the applicability of this distributed gate resistance modeling technique for small and large-periphery GaN HEMT devices to determine suitable width from which this technique gives a better representation of gate resistance as compared to the classical (lumped) model.

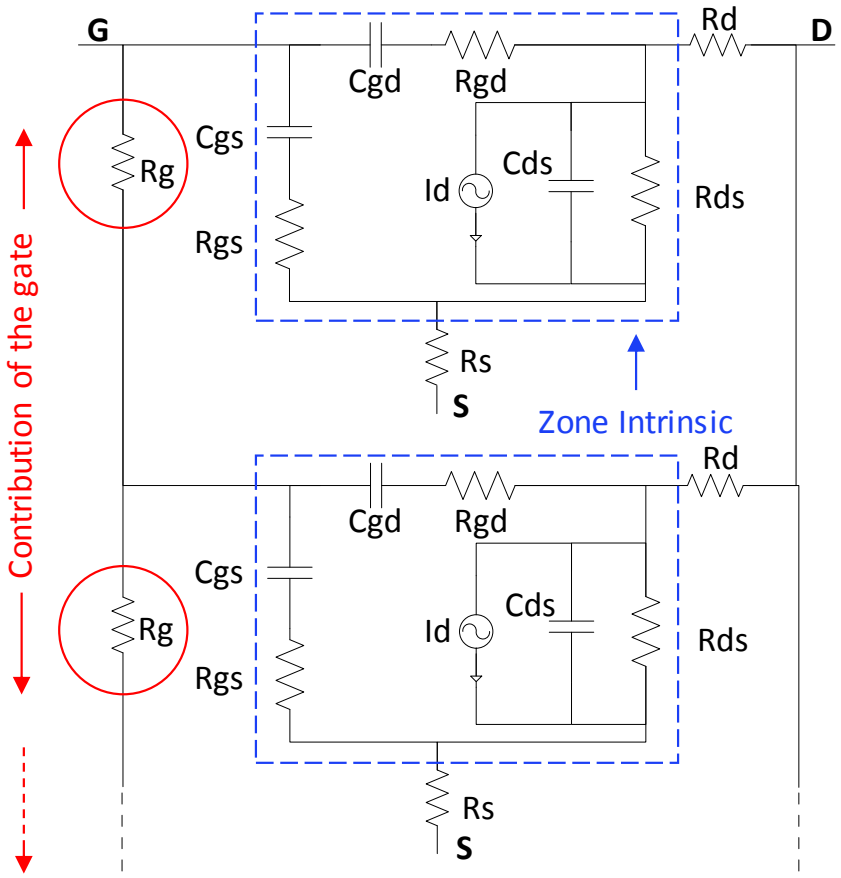


Figure 4-2: A proposed approach for distributed gate resistance

The proposed method is experimentally conducted on GaN HEMT devices with significant variations on the gate width (W) parameter and demonstrates its potential for the modeling of large-scale high-power transistors. The detail is given in the experimental results section.

4.3 Demonstration and extraction procedure

4.3.1 Assumptions and demonstration

In this work, the intrinsic characteristic of the transistor denominate the characteristics under the gate electrode and include the access regions (commonly represented by the resistance R_s and R_d). The device characteristics are meant to be properly de-embedded of parasitic elements, such as the

electrical potentials V_G, V_D, and V_S are located at the beginning of the gate finger, at the drain access region edge, and at the source access region edge, respectively. This analysis relies on two assumptions:

1. The intrinsic characteristic is assumed constant, along with the HEMT width. The thermal effect variations at the transistor edge are ignored since accounted for a negligible part of the overall characteristics of large-area devices. Also, the intrinsic characteristics of non-linear effects are neglected since the intrinsic static gate leakage current is assumed low enough to not cause a significant difference in intrinsic gate potential.

2. The drain and source are considered equipotential. The resistive and inductive effects located between the drain and source intrinsic potentials are considered as extrinsic lumped elements [108] and thus de-embedded in a classical manner [63]. Gate inductive effect can be easily taken into account by adding an imaginary part to R_g in the further calculations.

The equivalent schematic for a one-finger device is represented in Fig. 4-3 which gives a block diagram representation. The gate resistance per unit length ($R_\square$) is considered uniformly distributed. From [108], the admittance parameters of the device characteristics Y yields:

$$\mathrm{Y} = \begin{pmatrix} \mathrm{Y_{gg}} & \mathrm{Y_{gd}} & \mathrm{Y_{gs}} \\ \mathrm{Y_{dg}} & \mathrm{Y_{dd}} & \mathrm{Y_{ds}} \\ \mathrm{Y_{sg}} & \mathrm{Y_{sd}} & \mathrm{Y_{ss}} \end{pmatrix}$$

$$= \begin{pmatrix} \mathrm{Y_{gg}^{int}K} & \mathrm{Y_{gd}^{int}K} & \mathrm{Y_{gs}^{int}K} \\ \mathrm{Y_{dg}^{int}K} & \frac{\mathrm{Y_{dg}^{int}Y_{gd}^{int}}}{\mathrm{Y_{gg}^{int}}}(\mathrm{K}-\mathrm{W}) + \mathrm{Y_{dd}^{int}W} & \frac{\mathrm{Y_{dg}^{int}Y_{gs}^{int}}}{\mathrm{Y_{gg}^{int}}}(\mathrm{K}-\mathrm{W}) + \mathrm{Y_{ds}^{int}W} \\ \mathrm{Y_{sg}^{int}K} & \frac{\mathrm{Y_{sg}^{int}Y_{gd}^{int}}}{\mathrm{Y_{gg}^{int}}}(\mathrm{K}-\mathrm{W}) + \mathrm{Y_{sd}^{int}W} & \frac{\mathrm{Y_{sg}^{int}Y_{gs}^{int}}}{\mathrm{Y_{gg}^{int}}}(\mathrm{K}-\mathrm{W}) + \mathrm{Y_{ss}^{int}W} \end{pmatrix} \quad (4\text{-}2)$$

Where $K = \frac{\tanh\left(\sqrt{WR_\square Y_{gg}^{int}}\right)}{N\sqrt{WR_g Y_{gg}^{int}}}$ with N the number of fingers.

The device impedance parameters $Z = Y^{-1}$ yield the following relation with the intrinsic parameters Z^{int} and Y^{int}:

$$Z_{xx}^{int} = Z_{xx}\big|_{xx\neq gg,\ xx\neq dd,\ xx\neq ds,\ xx\neq sd} \quad (4\text{-}3)$$

$$Z_{gg}^{int} = (Z_{dd}Z_{ss} - Z_{ds}Z_{sd} + Z_{gd}Z_{dg}Z_{ss}Y_{gg}^{int} - Z_{gd}Z_{ds}Z_{sg}Y_{gg}^{int} - Z_{gs}Z_{dg}Z_{sd}Y_{gg}^{int} + Z_{gs}Z_{dd}Z_{sg}Y_{gg}^{int}/(Z_{dd}Z_{ss}Y_{gg}^{int} - Z_{ds}Z_{sd}Y_{gg}^{int})) \quad (4\text{-}4)$$

The new procedure starts by determining Y_{gg}^{int} by solving $f\left(Y_{gg}^{int}\right) = Y_{gg}$ where $f(x)$ is a bijection of $\mathbb{C} \to \mathbb{C}$ such as:

$$f(x) = \frac{\sqrt{x}}{N\sqrt{WR_{g\square}}} \tanh\left(\sqrt{WR_{g\square}x}\right) \quad (4\text{-}5)$$

The complete impedance intrinsic parameters can then be determined by using Eq. (3) and Eq. (4).

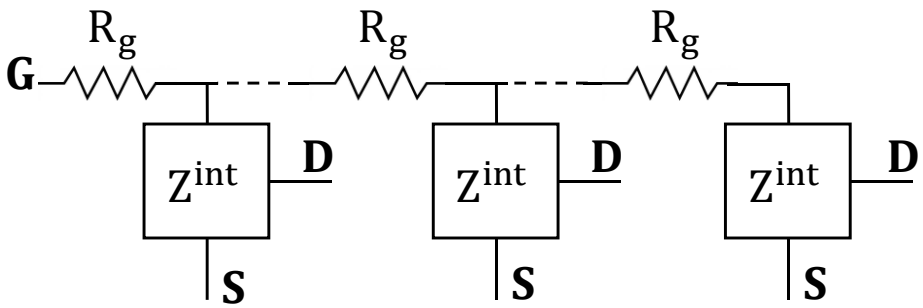


Figure 4-3: Three-ports equivalent schematics of a one-finger transistor with the considered assumptions

4.3.2 Two-port common-source case

In the case of a two-port electrical characterization in common-source (CS), the admittance parameters yield (6) from [124].

$$\begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} = \begin{pmatrix} Y_{gg} & Y_{gd} \\ Y_{dg} & Y_{dd} \end{pmatrix} \quad (4\text{-}6)$$

Equations of the admittance parameters for the device characteristics can be then derived straightforwardly from Eq. (2), Eq. (3), and Eq. (6) as:

$$Z_{xx}^{int} = Z_{xx}\big|_{xx\neq 11} \quad (4\text{-}7)$$

$$Z_{11}^{int} = (Z_{22} + Y_{11}^{int}.Z_{12}.Z_{21})/(Y_{11}^{int}.Z_{22}) \quad (4\text{-}8)$$

Where Y_{11}^{int} must be determined by solving $f\left(Y_{11}^{int}\right) = Y_{11}$.

In this new approach, the use of Eq. (3) and Eq. (4) or Eq. (7) and Eq. (8) depends on transistor topology, common-gate or common-source respectively, to avoid conversion of one topology from other by analytical expressions. The difference between the presented extraction technique and [106], [108] is a new set of impedance equations for two-port characterization, enabling a straightforward extraction of the intrinsic characteristics. Besides intrinsic parameters, most importantly, it enables us to determine the intrinsic matrix and, as a result, this is adaptable to whatever the intrinsic schematic.

4.4 Extraction procedure

Figure 4-4 describes the extraction procedure considering three major steps:

Step 1: Extrinsic parameters: The pad capacitances are extracted from the open test structure through cold pinch-off on-wafer measurement [71]. While access resistance R_s and R_d are obtained by reverse-biased cut-off method (cold-FET) [35, 36]. Gate metal sheet resistance $R_{g\square}$ is directly measured by using on wafer 4-probes measurement setup. The access inductances L_s, L_d, and L_g, are extracted by the cold-FET method [32, 37].

Step 2: Intrinsic parameters: After de-embedding the extrinsic parameters, the complete intrinsic parameters can be determined by using Eq. (3) and Eq. (4) or by Eq. (7) and Eq. (8) depending on the transistor's topology. Results for the 2-mm wide HEMT are indicated in Fig. 5.

Step 3: Simulation of the proposed model in advance design system (ADS) with all extracted intrinsic and extrinsic parameter values. The modeled S-parameters enable determination of the current-gain and power maximum gain and thus current cut-off frequency (f_T) and maximum frequency (f_{max}) respectively.

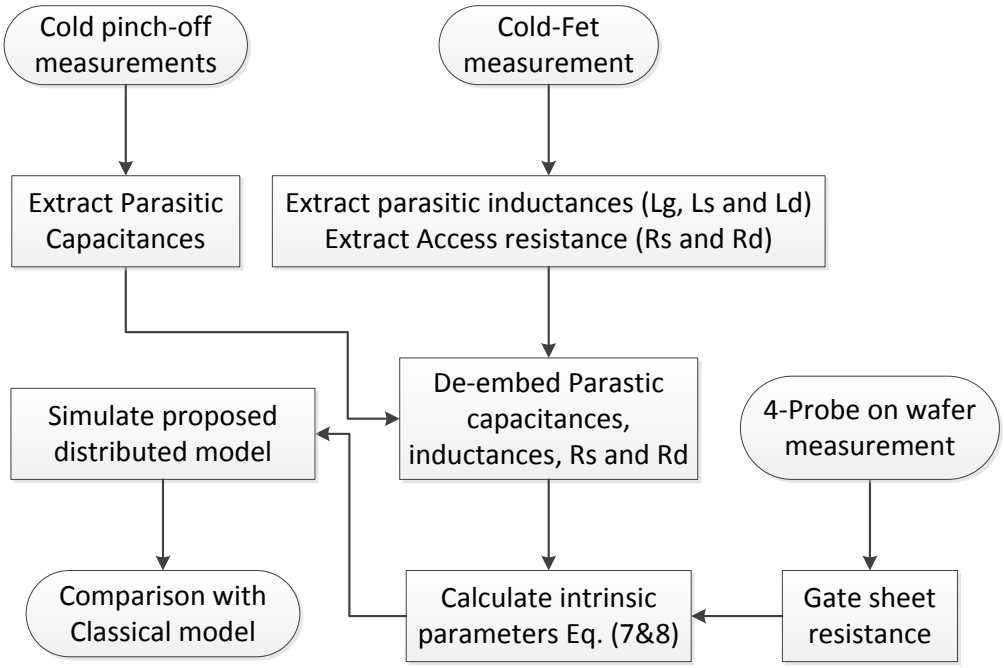


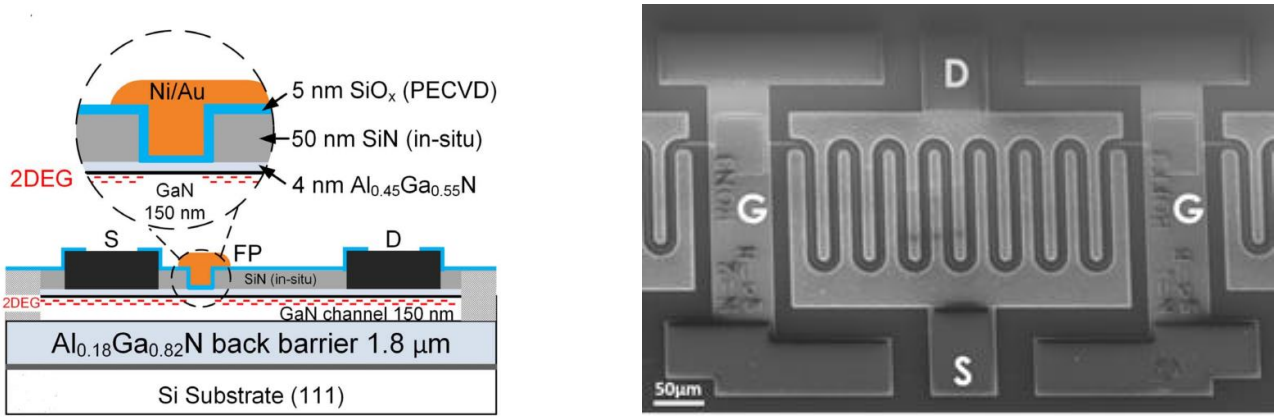
Figure 4-4: Flowchart of the distributed model's extraction procedure.

4.5 Experimental results

4.5.1 Devices under test

Devices under test are Normally-ON transistors with AlGaN/GaN MOS-HEMTs structures fabricated on a Si substrate and commercially available HEMT wafer (supplied by EpiGaN) by using metal-organic chemical vapor deposition technique (MOCVD) [125]. We have designed and fabricated these devices in our lab.

Our transistors have isolation oxide-gate, gate with meander shape, and field-plate with gamma shape. The epitaxial structure consists of a 5mm buffer, a 150nm thick undoped GaN channel layer, and a thin 4nm $Al_{0.45}Ga_{0.55}N$ top barrier layer. It is capped with a 50nm thick in-situ SiN layer. The fabrication process is detailed in references [38, 39]. The gate length (L_g) is 1.5um, gate-drain length (L_{gd}) is 6um, and source-gate length (L_{sg}) is 1.5um with four different widths (W) 0.125mm, 0.25mm, 0.5mm, and 1mm/finger. Figure 4-5 shows the schematic of the fabricated MOSHEMT with a) Normally-ON AlGaN/GaN structure information and b) SEM image of the fabricated device for W=2mm, L_{gd}=6µm, and L_{sd}=9µm.



a) Normally-ON AlGaN/GaN device [125]

b) SEM image of fabricated MOSHEMT, W=2mm with L_{gd}=6µm and Lsd=9µm

Figure 4-5: Schematic and SEM image of the fabricated MOSHEMT device.

4.5.2 Results and discussion

The proposed method is experimentally conducted on two fingers normally-on GaN MOSHEMT devices with four different widths W (0.25, 0.5, 1, 2mm). The comparison is done between classical and distributed models based on the extraction of all intrinsic parameters and to see a variation in modeled f_T and f_{max} for each width with respect to measurement data, as given in Table 4-1. The distributed model demonstrates its potential for the modeling of large-scale high-power transistors, as shown in Figure 4-6, Figure 4-7, and Figure 4-8 for W=2mm.

Figure 4-8 gives a comparison of all intrinsic parameters (C_{gd}, C_{gs}, C_{ds}, g_m, R_{gd}, R_{gs}, g_{ds}, and t) between both models. Intrinsic parameters are less variant with frequency in the case of the distributed model, particularly for gm, Cgd, Cgs, and gds. This reduced frequency dependence indicates that the intrinsic element extraction corresponds better to the physical characteristic of the HEMT since the intrinsic elements should ideally be frequency independent. Furthermore, the lesser frequency variations of the intrinsic elements benefit the overall modeling by granting a better accuracy on a broader frequency range.

Figure 4-6 shows a current-gain vs. frequency plot for measurement, classic, and distributed model. The zoomed area in the figure showed that there is a significant difference between the measured and classic model fit curve. Figure 4-7 gives the plot between maximum gain and frequency to see the variation of maximum oscillation frequency fit with all models. The distributed model gives a better fit for f_T and f_{max}.

In the case of f_T, the classical model is better for smaller widths, but for larger widths, it starts deviating and gives a 17.5% error with respect to measurements. In comparison, the distributed model gives a maximum of 2.8% error only.

Table 4-1: FT and fmax for measured, classic, and distributed model with different widths.

		Frequency [GHz]				
W (mm)	**Data**	**Measured**	**Class. Model**	**Distri. Model**	**E_r_Clas (%)**	**E_r_Dist (%)**
0.25	f_T	3.95	3.91	4.06	≈1.01	≈1.2
	f_{max}	8.45	8.45	8.41	–	≈0.4
0.5	f_T	3.95	3.86	4.05	2.28	2.53
	f_{max}	7.20	7.11	7.25	1.25	0.69
1	f_T	4.06	3.61	4.10	11.08	0.98
	f_{max}	5.20	4.86	5.15	6.54	0.96
2	f_T	3.95	3.26	4.06	17.47	2.78
	f_{max}	3.15	2.86	3.11	9.20	1.27

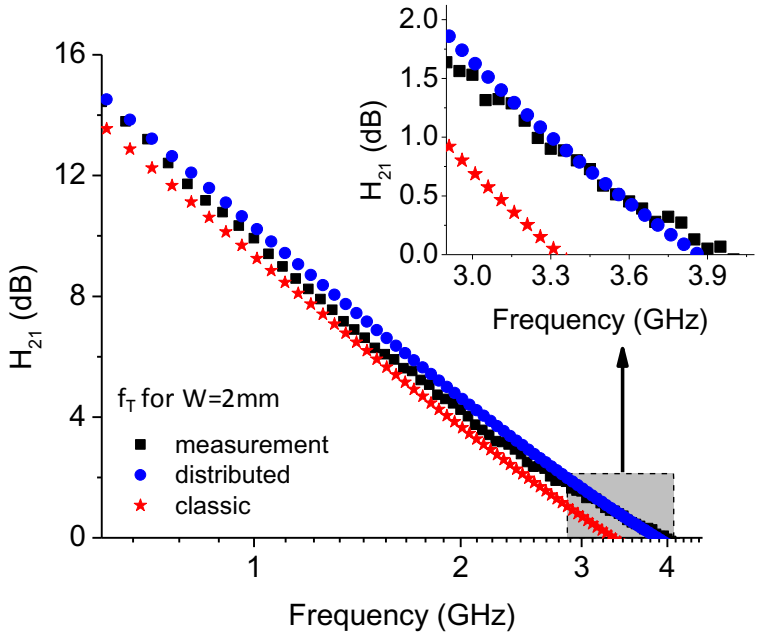


Figure 4-6: Current gain H_{21} (dB) vs. frequency (GHz) for a measured, classic, and distributed model with W=2mm.

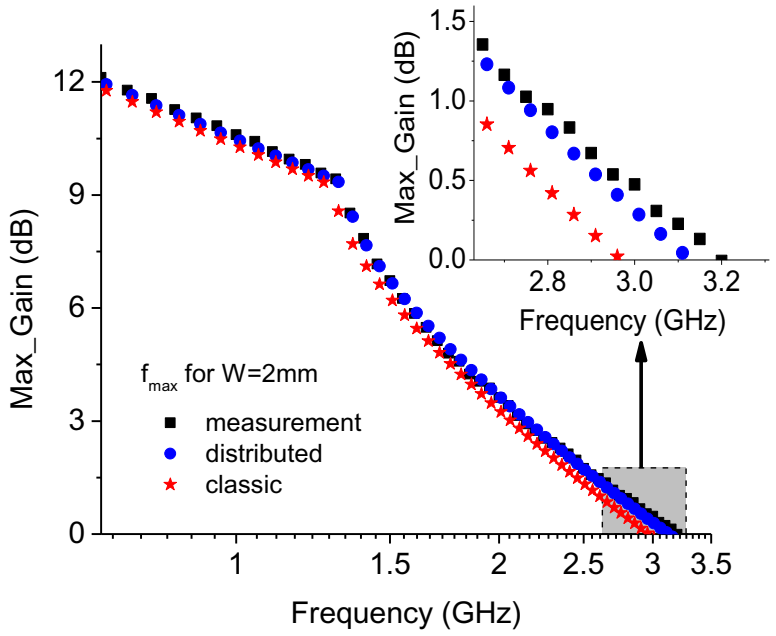


Figure 4-7: Maximum gain (dB) vs. frequency (GHz) for a measured, classic, and distributed model with W=2mm.

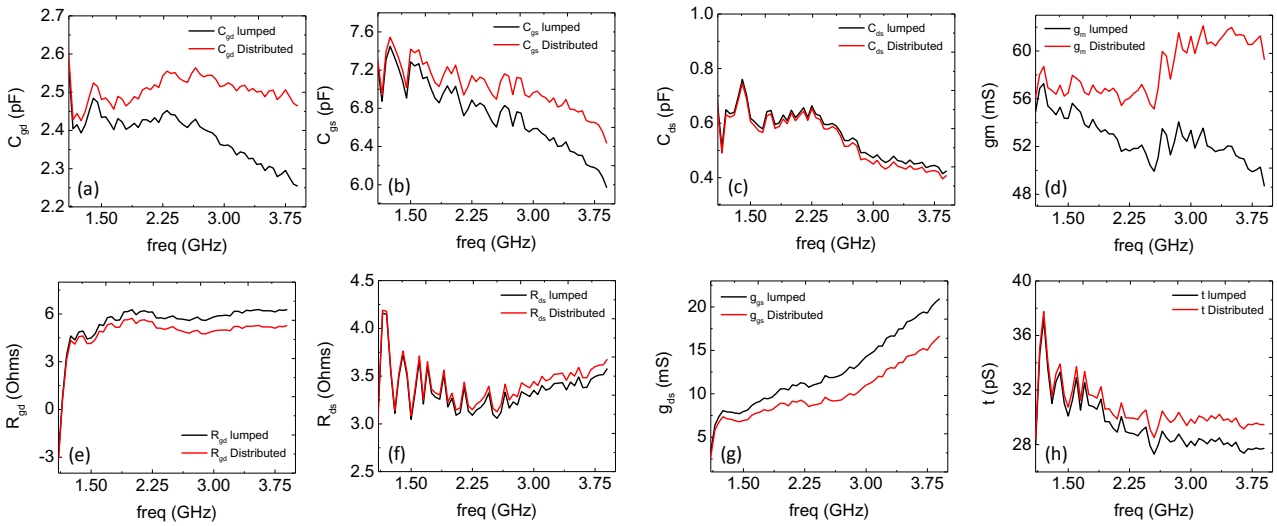


Figure 4-8: Comparison between classical model (black) and distributed model (red) for extraction of all intrinsic parameters C_{gd} (a), C_{gs}(b), C_{ds}(c), g_m (d), R_{gd} (e), R_{ds} (f), g_{ds} (g) and t (h) for W=2mm.

A similar pattern is noticed for f_{max} that error increased with width and the classical model gives more error 9.2% as compared to the distributed model 1.3%. To illustrate this behavior further, a plot between error (%) and the gate width is given in Figure 4-9. We can see clearly that the classical model is a better choice in area 1 (W < 0.5µm). However, area 2 (W > 0.5µm) showed that the distributed model is more adequate; as a result, we can conclude that the classical model is sufficient for smaller width, but it is not valid or gives more error above 500µm width.

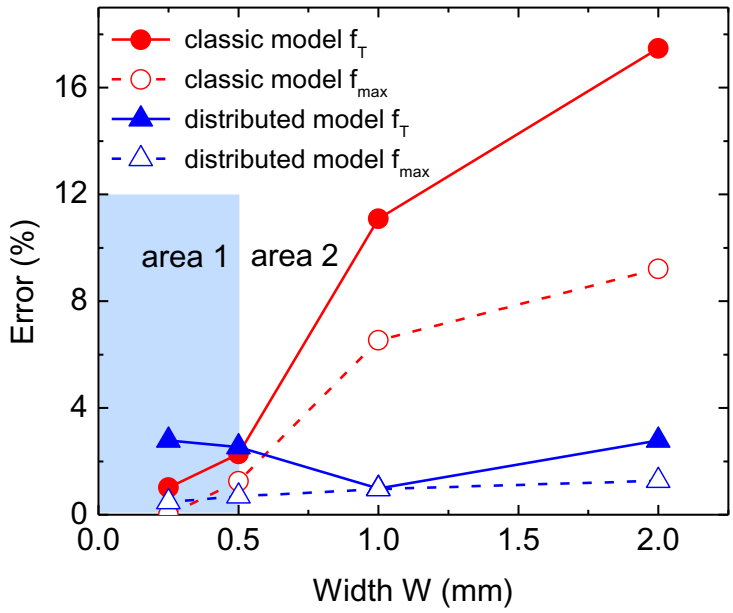


Figure 4-9: Error (%) vs. width W (mm) between the classic and distributed model for f_T and f_{max}.

4.6 Conclusion

In this work, we demonstrated an interest in distributed gate resistance modeling for large periphery GaN HEMTs devices. The proposed extraction methodology takes into account the distributed nature of the gate resistance, which is demonstrated to significantly improve the modeling of dynamic characteristics of large periphery devices. This technique is more suitable or applicable for devices that have gate width (W>0.5mm, N=2), and it is scalable regardless of the intrinsic topology. The advantages of this method are described with experimental results in the form of intrinsic parameters' extraction with less dependency on frequency, improvement in f_T and f_{max} modeling by reducing error from 17.5% to 2.8% and 9.2% to 1.3%, respectively with respect to measurement results. We showed that for a large gate width above 500um, a distributed model is a better choice for precise and accurate modeling of the gate resistance.

4.7 Acknowledgments

We gratefully acknowledge the funding support from Fonds de Recherches du Québec - Nature, technologies, and from the Natural Sciences and Engineering Research Council of Canada.

Chapter 5: Scalable small-signal modeling

Introduction

This article contributes to the thesis by demonstrating the small-signal model's scalability based on distributive gate resistance modeling. The relation of the extrinsic and intrinsic parameters to a bias voltage, frequency, and development (W) of the transistor is explained. The access resistance scalability is presented with four developments (0.25, 0.5, 1, and 2mm). Afterward, all intrinsic parameters variation versus frequency is shown for four developments. A comparison between the measurement and simulated distributed model's S-parameters is presented again for four development based on intrinsic parameters extraction. Afterward, an error is calculated for validation purposes.

The group members fabricated the devices; however, I was part of the meetings to discuss the technological challenges and difficulties. Once received fabricated wafers, my contribution was to performed DC and RF measurements to characterize the device. It also includes the development of the new model; then later performed a comparison between simulated results and measurement data to check and validate the model's scalability.

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Résumé

Ce papier présente la modélisation évolutive des petits signaux des transistors à haute mobilité électronique AlGaN / GaN (HEMT) basée sur un modèle de résistance de grille distribuée. Un modèle de résistance de grille distribuée (DGRM) est utilisé pour modéliser la grille large des HEMT à base de GaN avec différentes largeurs de grille. Un modèle a petit signal analytique entièrement évolutif est développé à partir des résultats expérimentaux. Des paramètres intrinsèques, indépendants de la fréquence, ont été mis en évidence. De plus, les paramètres S sont obtenus à partir de la modélisation et des mesures pour vérifier le modèle. Le bon accord entre les résultats mesurés et simulés indique que ce modèle est précis, stable et comparativement plus représentatif de l'évolution réelle de la résistance locale dans la grille. Le DGRM évolutif proposé serait utile pour la modélisation précise et évolutive de grands signaux de large périphérie des HEMT GaN pour une application RF haute puissance.

Scalable small-signal modeling of AlGaN/GaN HEMT based on distributed gate resistance

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Keywords: scalable, distributive gate, small-signal modeling, gallium nitride, high electron-mobility transistors, radiofrequency

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5.1 Abstract

This paper reports on scalable small-signal modeling of AlGaN/GaN high-electron-mobility transistors (HEMTs) based on the distributed gate resistance model. A distributed gate resistance model (DGRM) is used to model a large periphery of GaN HEMT with various gate widths. A fully scalable analytical small-signal model is developed with the experimental results. Intrinsic parameters, independent of the frequency, have been shown. Furthermore, S-parameters are obtained from the modeling and measurements to verify the model. The good agreement between the measured and the simulated results indicate that this model is accurate, stable, and comparatively more representative of the real evolution of local resistance in the gate. The proposed scalable DGRM would be useful for accurate, scalable large-signal modeling of large periphery GaN HEMTs for high power RF applications.

5.2 Introduction

Gallium nitride (GaN) outstanding properties (high break down voltage, high electron velocity) are very attractive for power amplifiers, millimeter-wave integrated circuits (MMIC) [127], and next-generation information communication systems [128]. These circuits need an accurate description of the High-Electron-Mobility-Transistor (HEMT) in the form of a reliable and accurate large-signal model that requires a small-signal model to develop it. Hence, a precise and stable small-signal model is very important to design an MMIC and to optimize the circuits fabrication process.

Several works have been done on scalable small-signal modeling (SSSM) in the literature, such as a comparative study on small-signal modeling (SSM) [129], FET's compact small-signal modeling [130], SSM based on optimization [131], on-wafer scaled GaAs HEMTs SSM [132], mmW modeling approach for pHEMTs [133] and GaN HEMT SSM [134] based on a direct parameter extraction algorithm [135], [136]. However, none of these works have used a distributed gate in the SSM modeling.

Another important point to note is that those works conducted experiments on a much smaller gate width as compared to our devices because increasing HEMTs total gate width brings its own

modeling challenges. For longer gate fingers, transistors distributed effects have to take into account to accurately model devices. These effects lead to modify the classical HEMT small-signal model [92]. The approach of [92] makes it possible to develop high power and more reliable circuits.

The objective of this paper is to implement and validate the scalability of a distributive gate resistance model into a small signal model for different widths of transistors which are missing in [92]. In this article, this study is being applied on two fingers AlGaN/GaN HEMTs devices of four different widths (0.25, 0.5, 1, 2mm). To accomplish this goal, we present a comparative analysis of the analytical modeling technique as compared to measured data. Then, we showed that the distributed gate resistance model is suitable for scalable small signal modeling.

5.3 Description and extraction procedure

The small-signal equivalent model used for AlGaN/GaN HEMT is shown in Figure 5-1, which is composed of extrinsic parameters and intrinsic elements. Pad capacitances (C_{pgs}, C_{pgd}, C_{pds}), parasitic inductances (L_g, L_s, L_d), and access resistances (R_g, R_s, and R_d) are called extrinsic parameters. Intrinsic capacitances C_{gs}, Cg_d, C_{ds}, charging resistances R_i or R_{gs}, R_{ds} and R_{ds}, transconductance g_m and transconductance delay time or constant- τ correspond to intrinsic components.

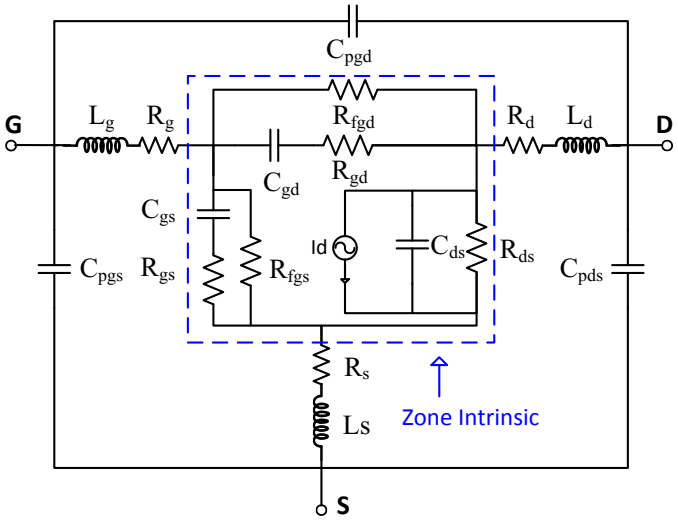


Figure 5-1: Small signal equivalent model for AlGaN/GaN HEMT

5.3.1 Parameter description and relation with bias voltage, frequency, and gate width (W):

R_s and R_d originate from the 2DEG sheet resistance and contact resistances while R_g comes from the metallization resistance of gate Schottky contact. C_{pgs}, C_{pgd}, and C_{pds} are the parasitic capacitances due to the pad's connections. g_m and g_{ds} are intrinsic and output transconductance respectively. The capacitances C_{gs} and C_{gd} reflect the change in the depletion charge with changes in V_{gs} and V_{gd} respectively. C_{ds} accounts for the geometric capacitance effects between the source and drain electrodes normally it is smaller than C_{gs} and C_{gd}. Smaller charging resistances are needed to have faster devices in terms of current and maximal frequency oscillation which are associated with intrinsic capacitances respectively. The time delay τ corresponds to the time which the drain current needs to respond to the change in gate voltage.

For proper scalable modeling, it is important to know the relation of all above-mentioned parameters behavior with respect to the bias voltage, frequency, and width of the gate given in Table 5-1. The analysis lies on the following assumption:

a) Pad capacitances and parasitic inductances are assumed constant for all different widths' transistors due to the same size of measurement's pad.

b) intrinsic characteristics are considered constant along the width of HEMT. The equivalent distributive gate resistance schematic for a one-finger device is represented in Figure 5-2, which gives a block diagram representation [92].

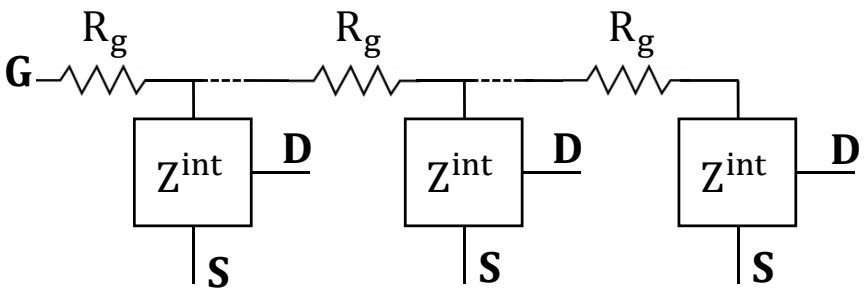


Figure 5-2: Distributive gate equivalent schematics of a one-finger transistor with the considered assumptions.

5.3.2 Devices under test

Devices under tests are Normally-ON transistors with AlGaN/GaN MOS-HEMTs structures fabricated on a Si substrate. The fabrication process and device structure are detailed in references [51], [125]. The gate length (L_g) is 1.5µm, gate-drain length (L_{gd}) is 6µm, and source-gate length (L_{sg}) is 1.5µm with four different widths (W) 0.125mm, 0.25mm, 0.5mm, and 1mm/finger. Figure 5-3 shows an SEM image of two fingers fabricated devices for W=2mm.

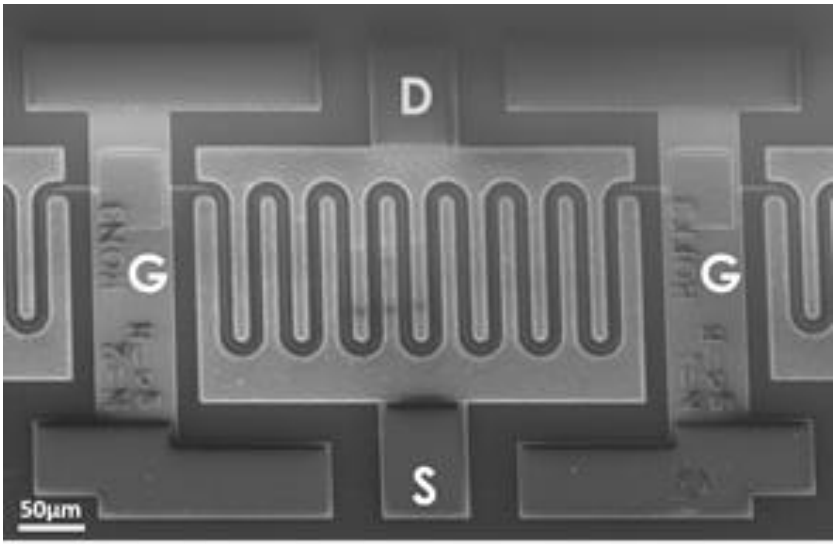


Figure 5-3: SEM image of two fingers fabricated MOSHEMT, W=2mm with L_{gd}=6µm and L_{sd}=9µm

Table 5-1 Small signal parameters vs. bias vol., frequency and gate width

Parameters	Bias	Freq	Gate Width
L_g^*	Independent	Independent	Increase with W
L_s	Independent	Independent	Increase with W
L_d	Independent	Independent	Increase with W
R_g	Independent	Independent	Proportional
R_s	Independent	Independent	Inverse Proportional
R_d	Independent	Independent	Inverse Proportional
C_{pgs}	Independent	Independent	Increase with W
C_{pgd}	Independent	Independent	Increase with W
C_{pds}	Independent	Independent	Increase with W
R_{gs}	Independent	Independent	Inverse Proportional
R_{ds}	Independent	Independent	Inverse Proportional
R_{gd}	Independent	Independent	Inverse Proportional
g_m	Dependent	Independent	Proportional
C_{gs}	Dependent	Independent	Proportional
C_{gd}	Dependent	Independent	Proportional
τ	Dependent	Independent	Increase with W

Note: *L_g is gate inductance while L_g is the gate length

5.3.3 Extrinsic parameter extraction

The pad capacitances are extracted from open test structure through cold pinch-off on-wafer measurement [71], and the access inductances are extracted by the cold-FET method [63], [74] are given in Table 5-2. Gate metal sheet resistance $R_{g\square}$ is directly measured by using an on-wafer 4-probes measurement setup. Access resistance R_s and R_d are obtained by reverse-biased cut-off method (cold-FET) [71], [72] for four different widths shown in Figure 5-4, and good linear fitting curves are obtained for scaling purpose.

Table 5-2 Extracted pad capacitances and inductances values

C_{pgs}	C_{pds}	C_{pgd}	L_s	L_d	L_g
15.43fF	15.56fF	0.744fF	11pH	15pH	34pH

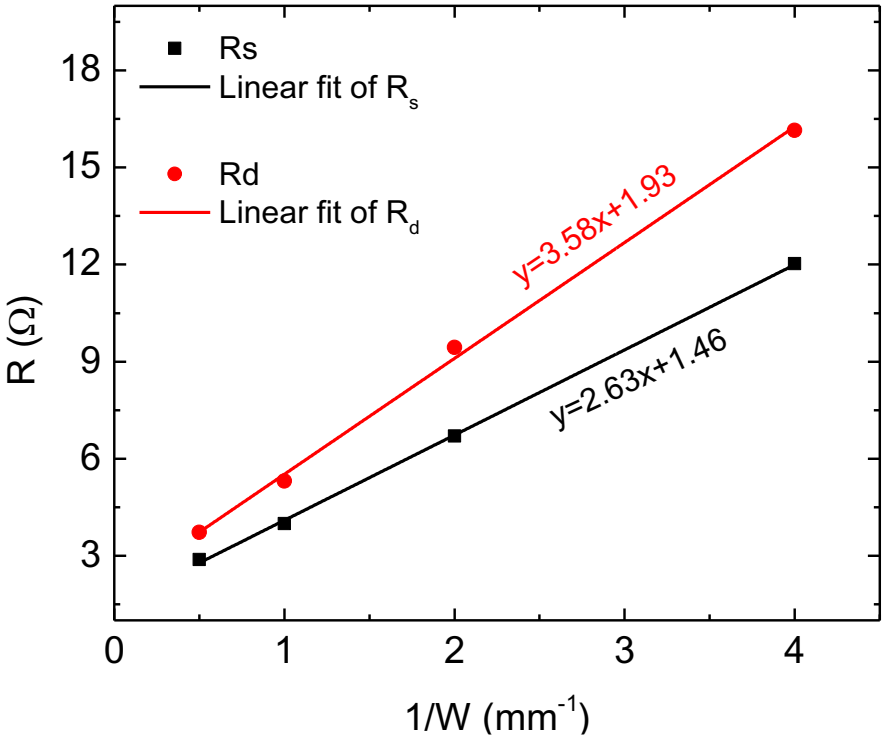


Figure 5-4: Resistances (R_s and R_d) vs. 1/W for scaling

5.3.4 Intrinsic parameter extraction

All intrinsic parameters extracted with intrinsic parameters equations defined in [79], [80] are computed from matrix obtained from equations (5-1) to (5-4) after de-embedding the extrinsic parameters [92].

$$Z_{xx}^{int} = Z_{xx}\big|_{xx\neq gg,\ xx\neq dd,\ xx\neq ds,\ xx\neq sd} \tag{5-1}$$

$$\begin{aligned} Z_{gg}^{int} = {} & (Z_{dd}Z_{ss} - Z_{ds}Z_{sd} + Z_{gd}Z_{dg}Z_{ss}Y_{gg}^{int} \\ & -Z_{gd}Z_{ds}Z_{sg}Y_{gg}^{int} - Z_{gs}Z_{dg}Z_{sd}Y_{gg}^{int} \\ & +Z_{gs}Z_{dd}Z_{sg}Y_{gg}^{int}/(Z_{dd}Z_{ss}Y_{gg}^{int} - Z_{ds}Z_{sd}Y_{gg}^{int})) \end{aligned} \tag{5-2}$$

$$f\left(Y_{gg}^{int}\right) = Y_{gg} \tag{5-3}$$

Where $f(x)$ is a bijection of $\mathbb{C} \rightarrow \mathbb{C}$ such as:

$$f(x) = \frac{\sqrt{x}}{N_f\sqrt{WR_{g\square}}} \tanh\left(\sqrt{WR_{g\square}x}\right) \quad (5\text{-}4)$$

Then scaling of the parameters is done based on the relations, as mentioned in Table 1. It is important to know that C_{gs}, Cg_d, C_{ds}, $R_{gs,}$ and g_m values are determined at low frequencies (0.55-3GHz) while R_{gd}, $R_{ds,}$ and τ vales at high frequencies (6-10 GHz) because at these frequencies, they play a more dominant role.

Optimization and comparison of S-parameters are done based on the error function given below in (11) and (12) where i=(1,2), j=(1,2), and the total number of frequency points N_f, 190 in our case.

$$E_{ij} = \frac{1}{N_f}\sum_f 100\left|\frac{S_{ijmeas}(f) - S_{ijmodel}(f)}{S_{ijmeas}(f)}\right| \quad (5\text{-}5)$$

$$E_{Total} = \frac{(S_{11} + S_{12} + S_{21} + S_{22})}{4} \quad (5\text{-}6)$$

The simulation of the proposed model is done in the advance design system (ADS) software with all extracted intrinsic and extrinsic parameter values.

5.4 Results and discussions

The method is experimentally conducted on two fingers, normally-on AlGaN/GaN MOSHEMT devices with four different gate widths (0.25, 0.5, 1, 2mm). There are 1, 2, 5, and 11 numbers of distributed cells used for modeling of W=0.25, 0.5, 1, and 2mm transistors, respectively, to reach the convergence of the model. The comparison is done on the level of the intrinsic parameters to see their dependence on frequency and on S-parameters between measured and modeled to check the validity of the method.

Figure 5-5 shows all the intrinsic parameters C_{gs}, C_{gd}, C_{ds}, R_{gs}, R_{gd}, $R_{ds,}$ $g_{m,}$ and τ vs. frequency for each W at V_{gs}=2.5V and V_{ds}=16V bias point. After optimization, thanks to the new approach, we obtained quite satisfactory results for four different widths as; clearly, we can see there is a decent degree of independence of these parameters from the variation of frequency, which indicates the better representation of HEMT's physical characteristic. For example, C_{gd} and C_{gs} curves are quite constant with frequency to take their mean value as well as g_m and other parameters. Furthermore, a comparison is done between measured and simulated S-parameters based on the percentage error function.

Table 5-3 gives the details of the error at each S-parameters of four widths. The maximum error is 5.80% for S_{11} of 2mm width transistor. There is a slight increase in error as we go from smaller to higher W but still, it is in the acceptable range because the total error is 1.48%, 2.05%, 3.55%, and 3.54% for 0.25mm, 0.5mm, 1mm, and 2mm widths' transistor respectively which is less than 4% which lead to a conclusion that the predict the behavior of the device appropriately.

Table 5-3 Error between measured and Simulated S-parameters vs. widths

$W_{(mm)}$ \ S_{ij}	E_S_{11}(%)	E_S_{12}(%)	E_S_{21}(%)	E_S_{22}(%)
0.25	2.21	0.16	1.42	2.14
0.5	4.01	1.15	2.25	0.80
1	5.25	3.47	0.34	5.13
2	5.80	3.83	1.59	2.94

Figure 5-6, Figure 5-7, Figure 5-8, and Figure 5-9 show a comparison between measured and modeled S-parameters (S_{11}, S_{12}, S_{21}, and S_{22}) for W=0.25, 0.5, 1, and 2mm respectively at V_{gs}=2.5V and V_{ds}=16V. There are little discrepancies in S_{21} for lower frequencies close to 900MHz, as we can see clearly in Figure 5-6 and Figure 5-8 even than the error is 1.42% and 1.59%, respectively. Besides, those results are quite satisfactory and encouraging for scalable modeling devices based on distributive gate resistance.

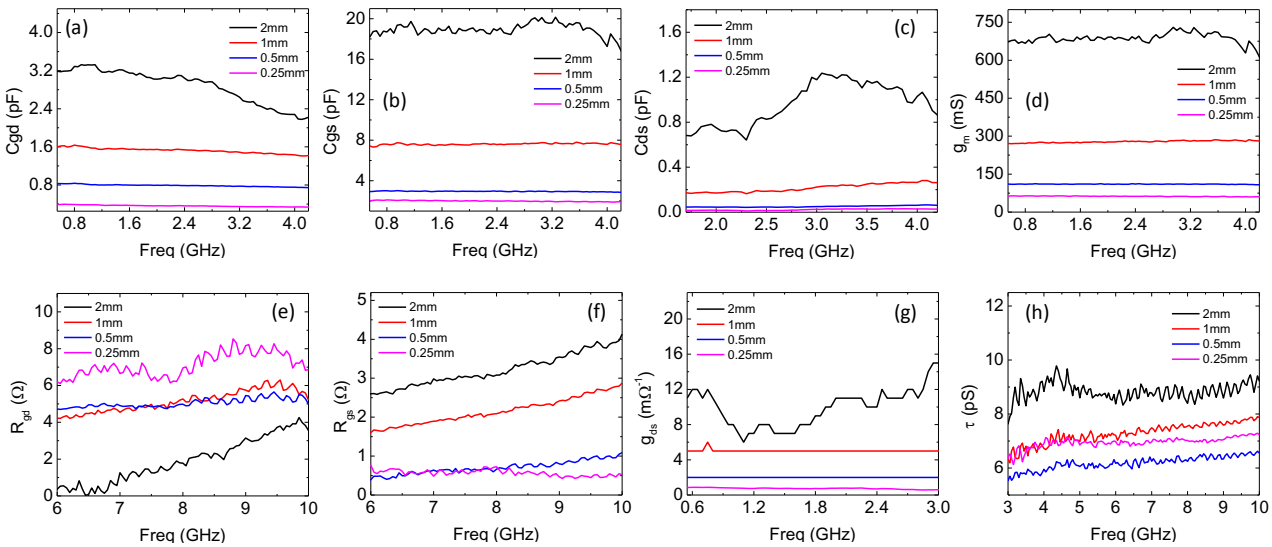


Figure 5-5: Behavior of all extracted intrinsic parameters C_{gd}(a), C_{gs}(b), C_{ds}(c), g_m(d), R_{gd}(e), R_{ds}(f), g_{ds}(g) and τ(h) vs. the frequency for W=0.25, 0.5, 1 and 2mm at V_{gs}=2.5V and V_{ds}=16V.

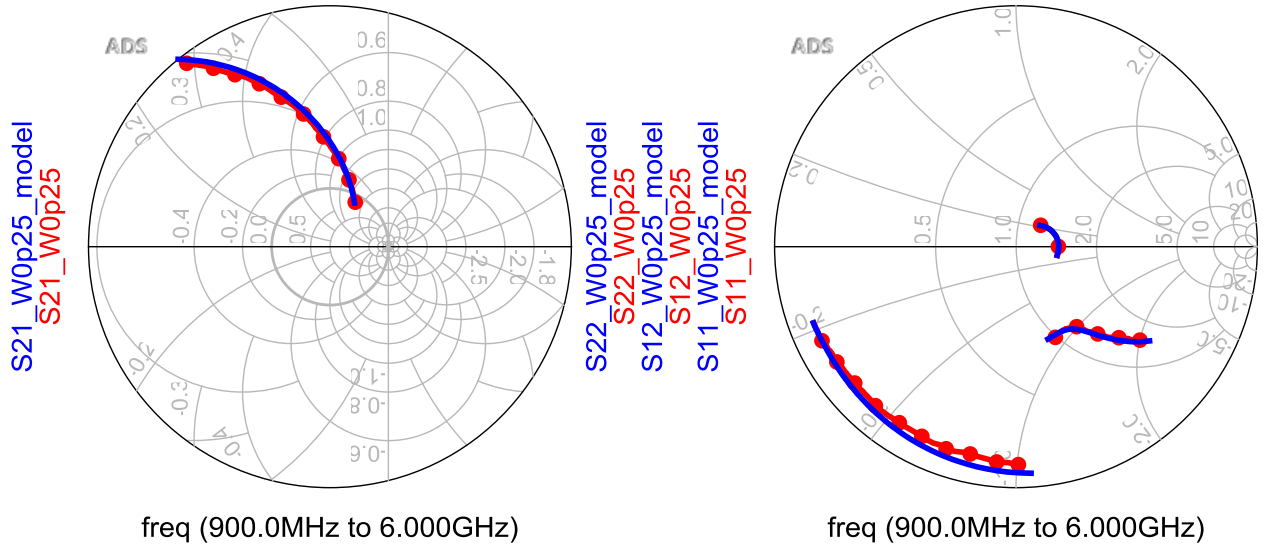


Figure 5-6: Comparison between measured and modeled S-parameters (S_{11}, S_{12}, S_{21}, and S_{22}) for W=0.25mm at V_{gs}=2.5V and V_{ds}=16V.

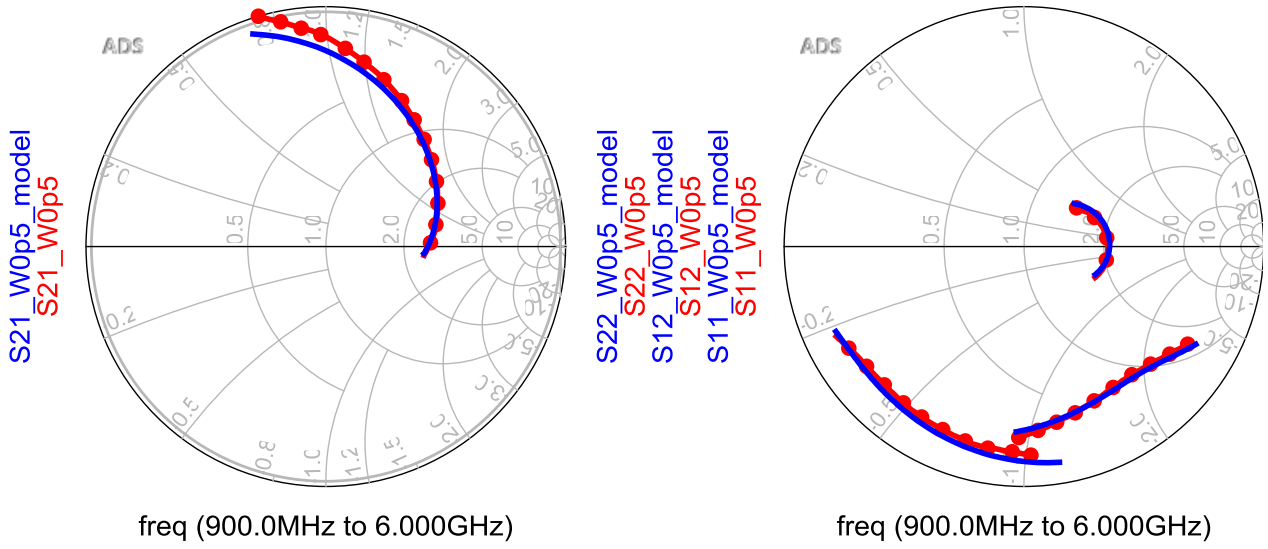


Figure 5-7: Comparison between measured and modeled S-parameters (S_{11}, S_{12}, S_{21}, and S_{22}) for W=0.5mm at V_{gs}=2.5V and V_{ds}=16V.

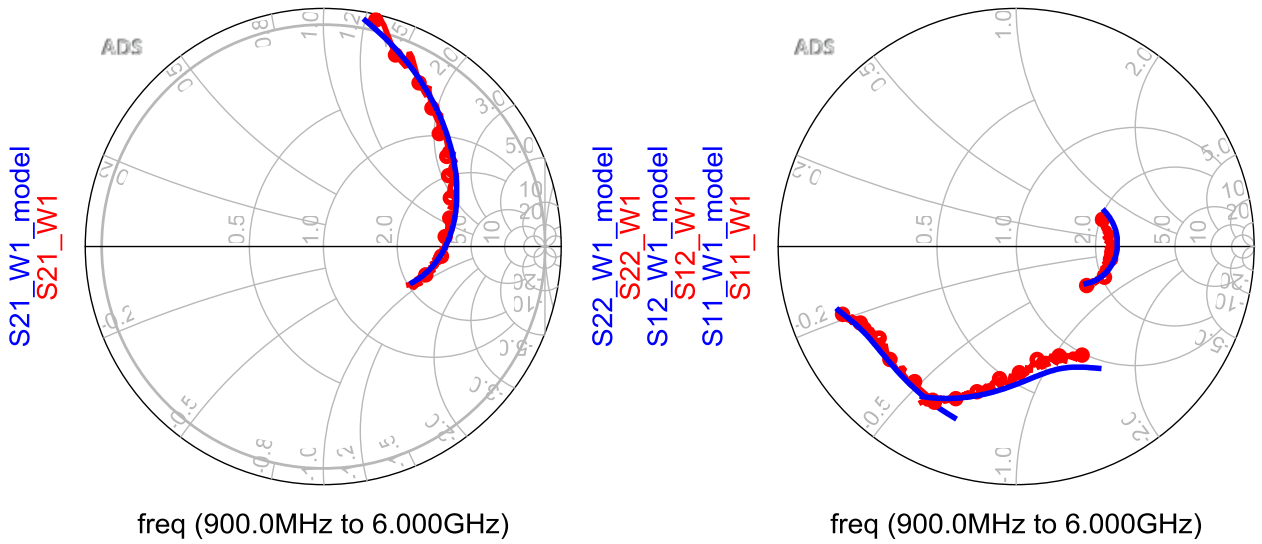


Figure 5-8: Comparison between measured and modeled S-parameters (S_{11}, S_{12}, S_{21}, and S_{22}) for W=1mm at V_{gs}=2.5V and V_{ds}=16V.

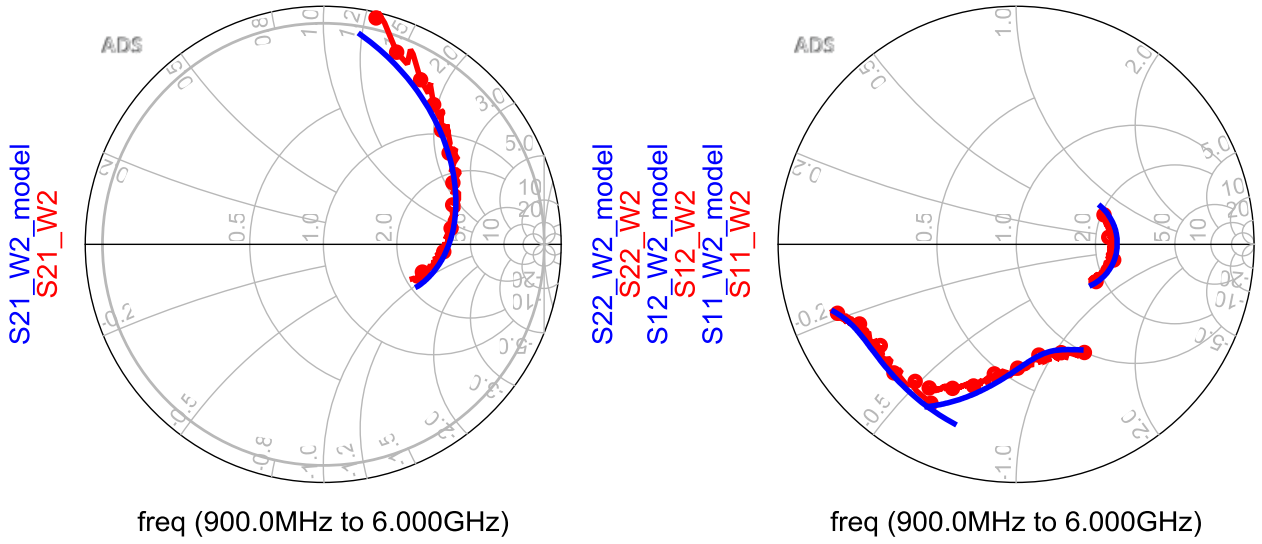


Figure 5-9: Comparison between measured and modeled S-parameters (S_{11}, S_{12}, S_{21}, and S_{22}) for W=2mm at V_{gs}=2.5V and V_{ds}=16V.

5.5 Conclusion

In this work, we have successfully implemented the scalability of distributed gate resistance into a small signal model of AlGaN/GaN HEMTs devices, and the results are quite satisfactory. Intrinsic parameters are reasonably independent of the frequency. The scalability of the model is presented from access resistance (R_s and R_d) to scalable SSM in the form of S-parameters for four different gate widths. Moreover, the comparison of S-parameters between measured and simulated gave a total error of less than 4%, which indicates that this model is accurate, stable, and comparatively clear in physical significance. This approach would be helpful for the successful implementation of distributed gate resistance into large-signal modeling of large periphery GaN HEMTs for high power RF applications.

5.6 Acknowledgment

We gratefully acknowledge the funding support from Fonds de Recherches du Québec - Nature, technologies, and from the Natural Sciences and Engineering Research Council of Canada.

Chapter 6: Large Signal Model Validation

In this chapter, the large-signal model of AlGaN/GaN HEMT is being validated. The model is derived from the physically relevant distributed small-signal model described in the last chapter. First, the large-signal model equivalent circuit will be described. Next, the procedure of the model element extraction will be explained. Afterward, a comparison between the measured and simulated models for different parameters will be presented.

In the large-signal model of AlGaN/GaN MOSHEMT shown in Figure 6-1, C_{gs} depends on the V_{gs}, C_{gd} depends on V_{gs}, and $I_{ds}(I_d)$ depends on V_{ds} for different V_{gs}. For large-signal modeling, we need to develop a model that successfully predicts the device's non-linear behavior, especially with the gate and drain voltage variation.

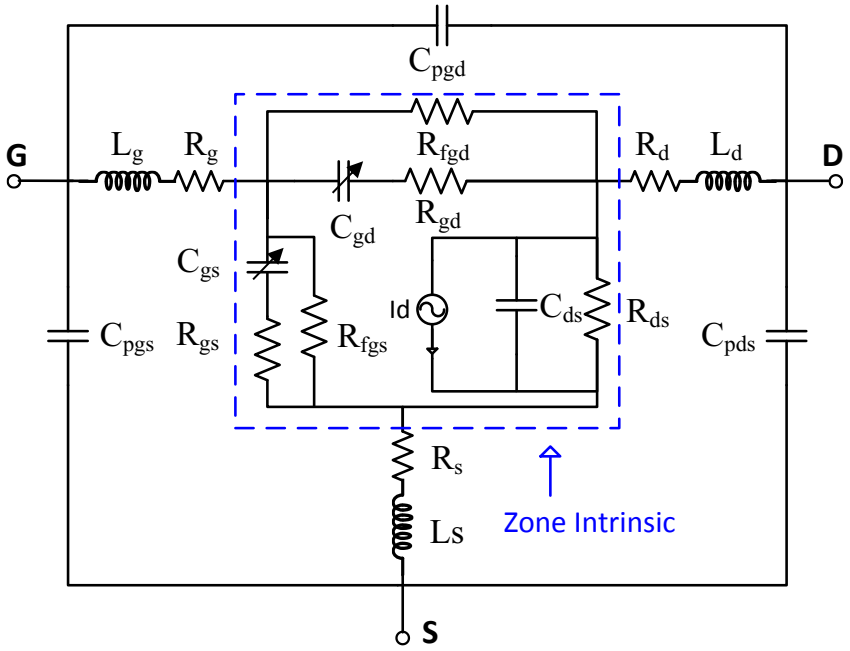


Figure 6-1: Equivalent electrical model for AlGaN/GaN MOSHEMT with non-linear capacitances and current source.

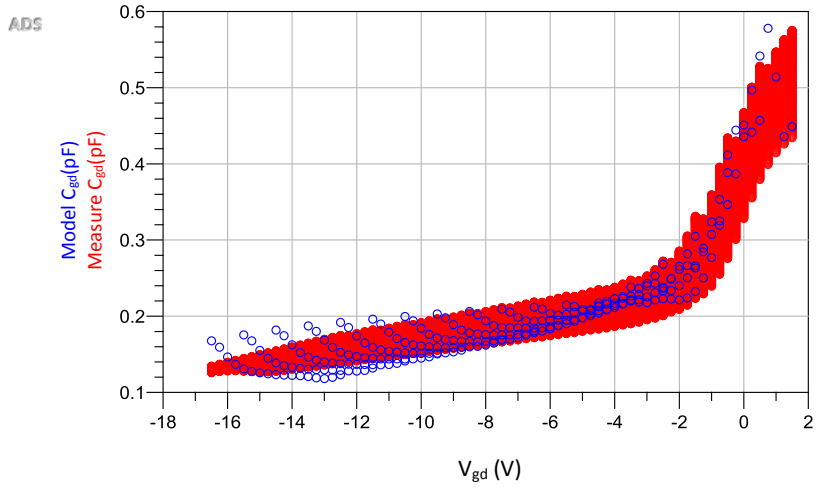
6.1 Non-linear Capacitance modeling

The modeling equations from Forestier et *al*. [91] are given below, which are used to model these nonlinear capacitances.

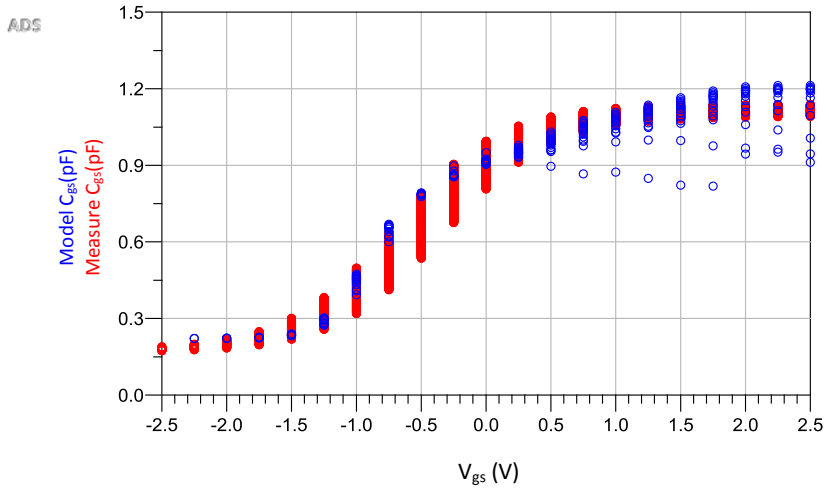
$$C_{gs} = C_{gs0} + \frac{C_{gs1}-C_{gs0}}{2}\left[1 + tanh\left(A.\left(V_{gs} + V_m\right)\right)\right] - \frac{C_{gs2}}{2}\left[1 + tanh\left(B.\left(V_{gs} + V_p\right)\right)\right] \quad (6\text{-}1)$$

$$C_{gd} = C_{gd0} + \frac{C_{gd1}-C_{gd0}}{2}\left[1 + tanh\left(A.\left(V_{gs} + V_m\right)\right)\right] - \frac{C_{gs2}}{2}\left[1 + tanh\left(B.\left(V_{gd} + V_p\right)\right)\right] \quad (6\text{-}2)$$

There has been a good match between measured and simulated capacitances for both Cgs and Cgd as we can see the results presented in Figure 6-2 below.



a) Cgd vs. Vgd



b) Cgs vs. Vgs.

Figure 6-2: Comparison of non-linear capacitances (C_{gs} and C_{gd}) between measured and modeled.

6.2 Transient self-heating and Drain current modeling

The intrinsic current source consists of a function describing drain current I_d with respect to bias and temperature [83] given below in Eq.(6-3). The details are given in chapter 3. Since our work is development and research, this model, based on physic, is adopted for current source modeling.

$$I_d = Wqn_s\left(V_{gs}^{int}\right)v\left(V_{ds}^{int}, T\right) \qquad (6\text{-}3)$$

For including thermal effect in the modeling, the T factor is modeled according to [137]. The device is divided into 3-zones where zone-1 is near-gate propagation, zone-2 is inter-finger crosstalk, and zone-3 is a heat sink, as shown in Figure 6-3. The thermal effect is modeled with modeling equations from all zones. We can see that as the device heated up for higher voltages. The model predicts the behavior well shown in Figure 6-4. Since our modeling focus was in the saturation region, we did not include the trap effect in the current source because its effect is more visible and vital for the ohmic region. Consequently, measurements are mostly performed with the CW waveform.

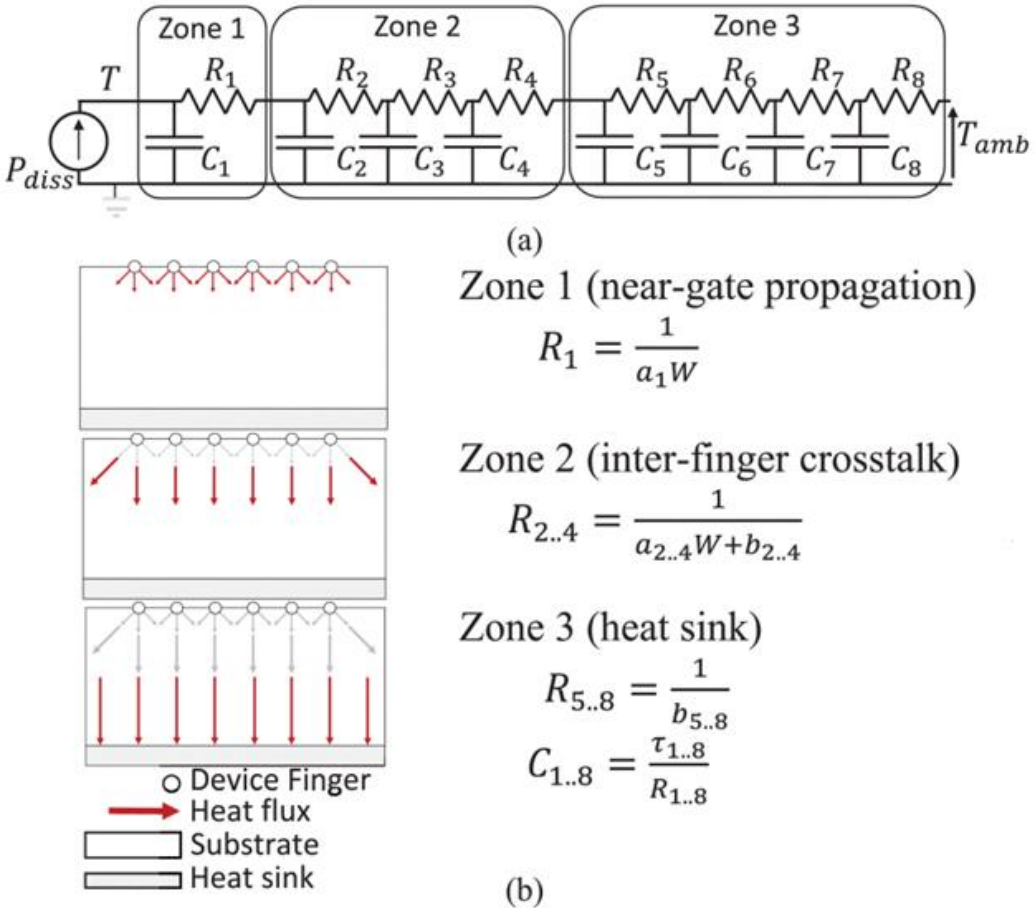


Figure 6-3: (a) Equivalent thermal model based on an eight-order Cauer topology and subdivided into three zones. (b) Representation of the three-time periods of the heat flux propagation corresponding to the three zones of the model.

In Figure 6-4, the plot of measurement and model for the current source is given. It gives a good match besides knee voltage because of the king's effect (a sudden increase of rising drains current). Our focus for modeling devices is in the saturation region because of the application we had in mind, such as the power amplifier design. V_{gs} varies from -2.5V to 2.5V with 0.25V step while V_{ds} varies from 0-15V with a step of 0.25V.

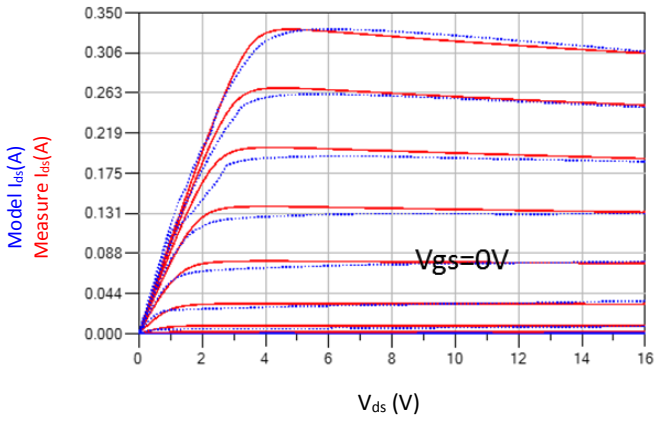


Figure 6-4: Comparison between measurement and mod I_d(A) vs. V_{ds}(V) for different V_{gs}(V).

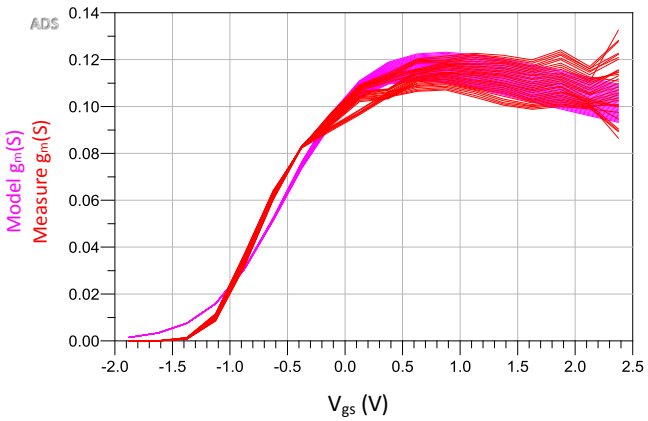
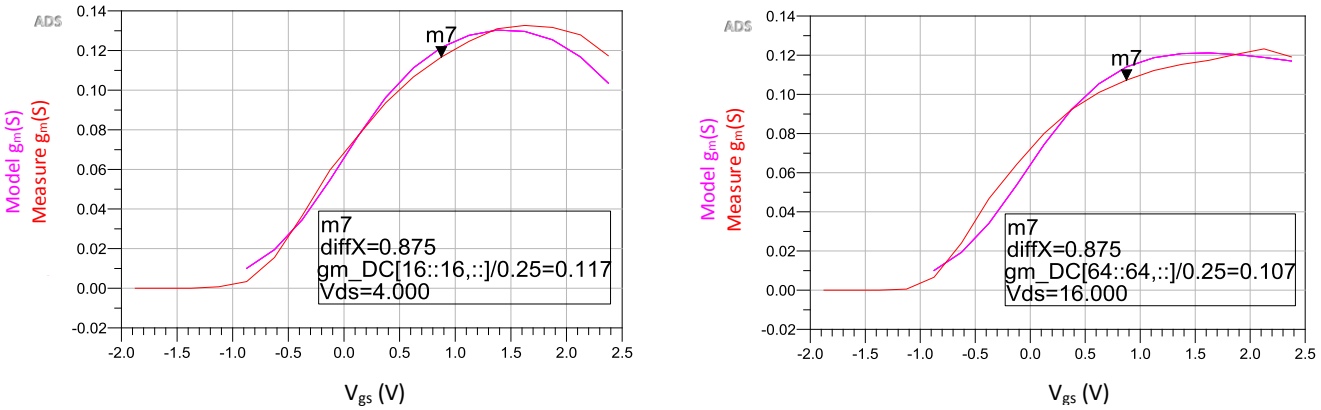


Figure 6-5: Comparison between measured and modeled for Transconductance(S) vs. V_{gs}(V).

It is essential to know that transconductance (g_m) is modeled correctly. The variation follows as we give a higher drain voltage, which has been further presented in Figure 6-5. Furthermore, results are highlighted with V_{ds}= 4 and 16V. It shows a decent fit between measured and simulated results, as shown in Figure 6-6.

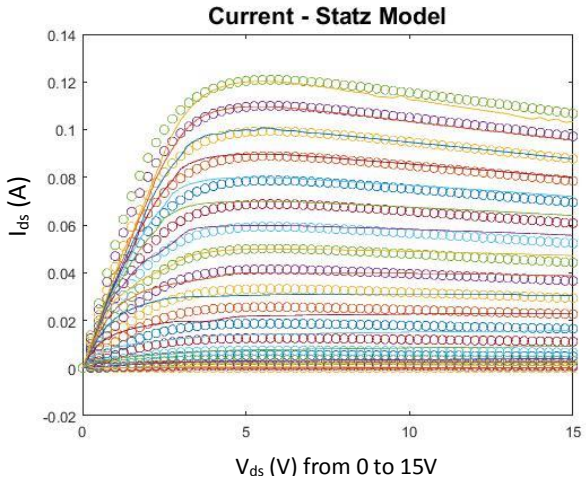


(a) Transconductance(S) vs V_{gs}(V) at V_{ds}=4V *(b) Transconductance(S) vs V_{gs}(V) at V_{ds}=16V*

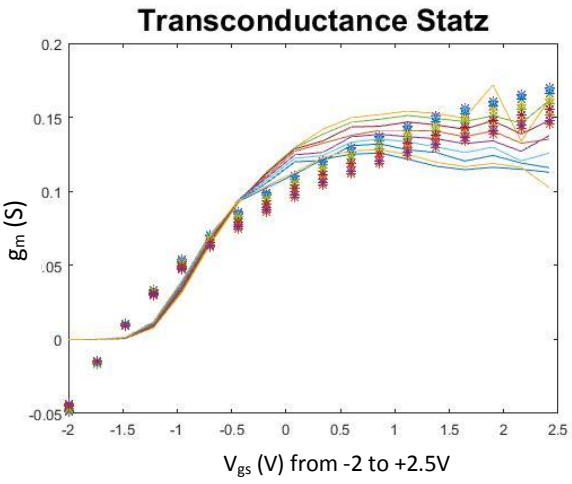
Figure 6-6: Comparison between measurement and model Transconductance(S) vs. V_{gs}(V) at specific V_{ds}(V).

There are other analytical methods for large-signal current source models such as Curtice [86], [87], Statz model earlier [88], and Angelov model [89], [90]. For comparison, we compared the current source and transconductance for the above mentioned three methods.

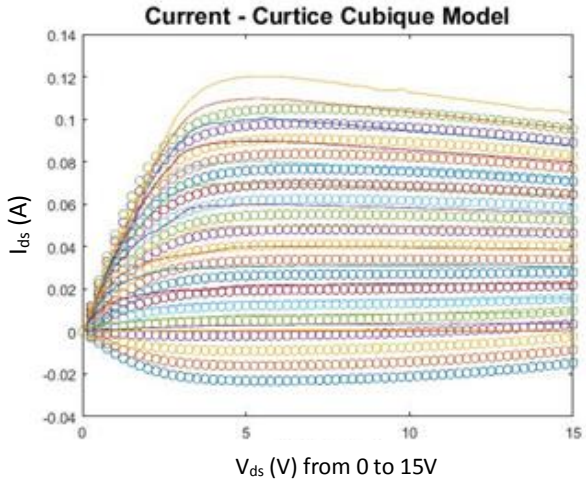
Statz gives a nice fit for the current source's saturation region but not accurate for the linear region and doesn't give a decent gm model. The Curtice model for current has a problem from low to high V_{gs} similarly very bad for transconductance modeling, as shown in Figure 6-7(c, d). This model considers time constant in it. The bad matching in transconductance comes from the derivative of the time constant, which becomes zero. However, the Angelov model gives a very nice fit for both current and transconductance, as shown in Figure 6-7(e, f). This solution with the Angelov model is very close to that found by means of a neural network or genetic algorithm.



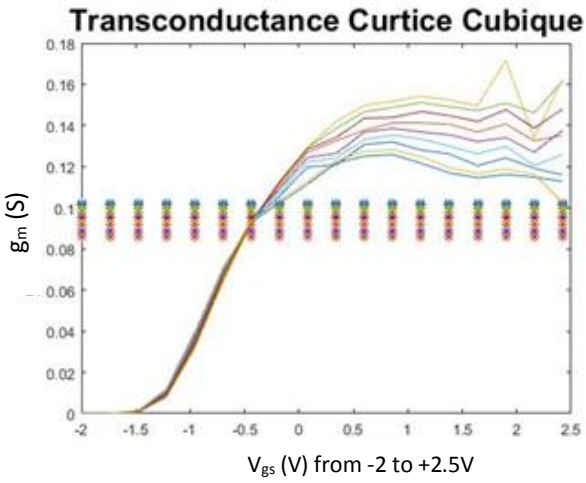
a) Statz Current model



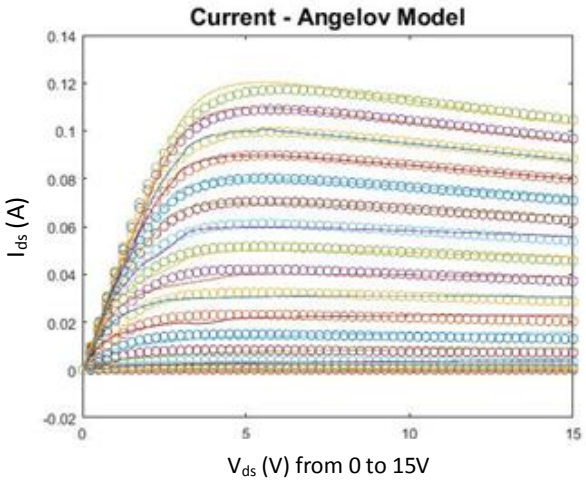
b) Statz Transconductance



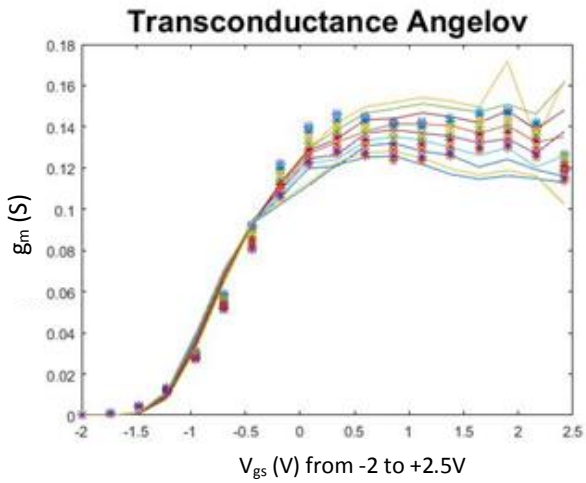
c) Curtice Current Model



d) Curtice Transconductance



e) Angelov Current Model



f) Angelov Transconductance

Figure 6-7: Comparison between Curtice, Statz, and Angelov model for current source I_{ds}(A) vs. V_{ds}(V) and transconductance (S) vs. V_{gs}(V). The dotted lines are fitting curves, while solid lines are from the measurement.

6.3 Model Convergence

We tried to study the convergence of the model and see the impact of the different network numbers for several gate widths (0.25, 0.5, 1, and 2mm), as shown in Figure 6-8. As we can see for smaller gate width transistors, the number of distributed networks does not have much impact. However, for higher gate width transistor (2mm), we can see a convergence around 11 networks for $f_{max,}$ which means there is no change in f_{max} as we increase the number of distributed networks from 11 to 27. In short, we can calculate the number of networks required for different width of the transistor for convergence purposes.

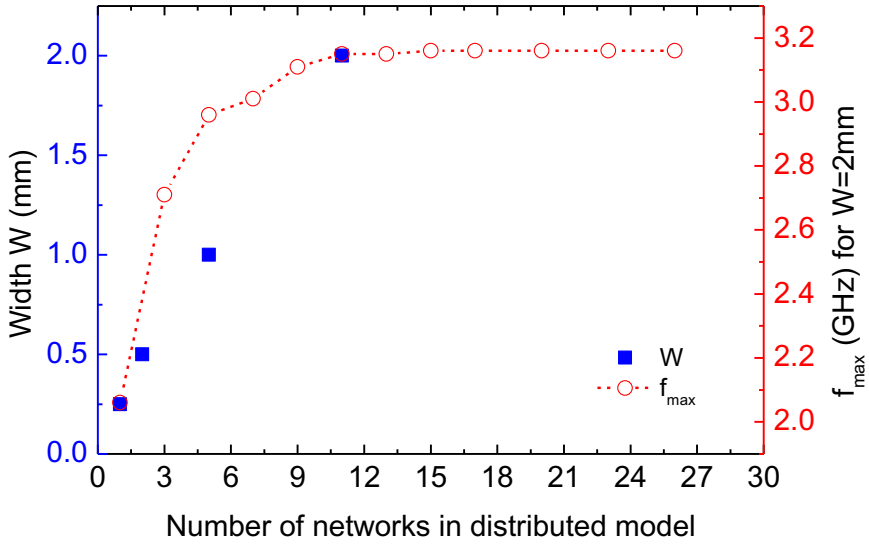


Figure 6-8 A number of distributed network vs. widths (0.25, 0.5, 1, and 2mm) of the transistors and f_{max} for large gate width 2mm.

6.4 Circuit level model validation

After developing and validating AlGaN/GaN MOSHEMT model, the next step is to develop the circuit. For this purpose, we decided to design a high-power amplifier (HPA). There are several topologies for HPA design, depending on different criteria. Each one has its own advantages or

disadvantages. A comparison between simple HPA topologies is given below in Table 6-1. These topologies are single-ended, balanced, and differential/push-pull.

Single-ended has low complexity and low cost but provided lower performance in the low output saturation power. The balanced topology is suitable for mid-range power and offers good impedance matching, etc. However, it leads to more complex design and higher power losses. Similarly, Deferential/push-pull topology offers higher power. At the same, it's more complicated and increases the high cost for the design.

The single-ended topology shown in Figure 6-9 is chosen for its simplicity and low cost because our goal is to validate PDK at the circuit level. It contains an input and output matching network along with source and load resistances.

Table 6-1: Comparison of different topologies of the Power Amplifier

Topology	Advantages	Disadvantages
Single-ended	• Low complexity • Reduce cost	• Reduced performance compared to other HPA topologies
Balanced	• High output saturation power and 1dB compression point. • Excellent impedance matching. • Improved reliability and stability	• Additional components are required. • Losses of couplers reduce overall HPA performance. • Increased costs.
Differential/ Push-pull	• Higher output saturated power and 1 dB compression point.	• Consumes more static power than single-ended. • Increased cost.

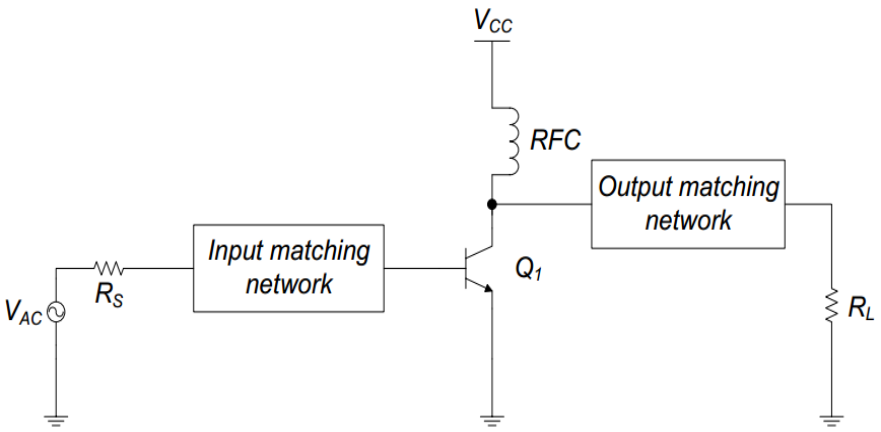
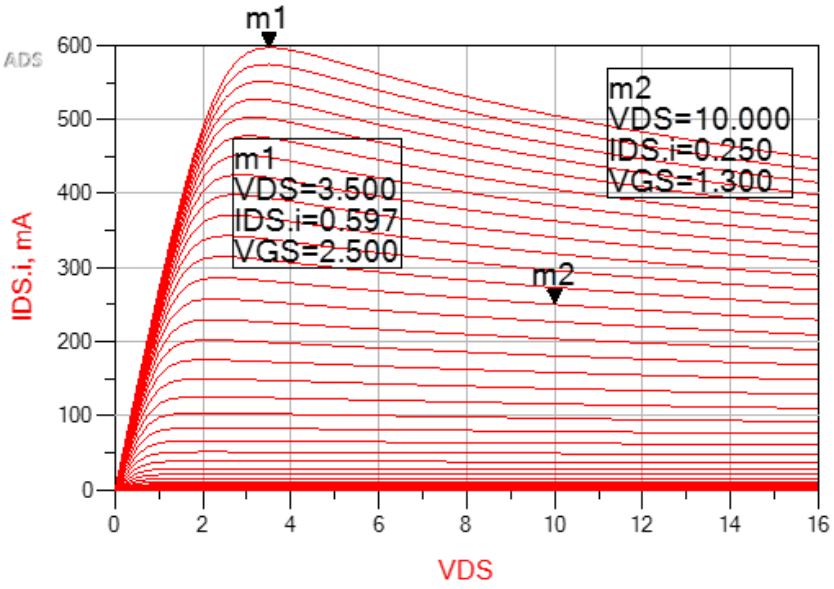


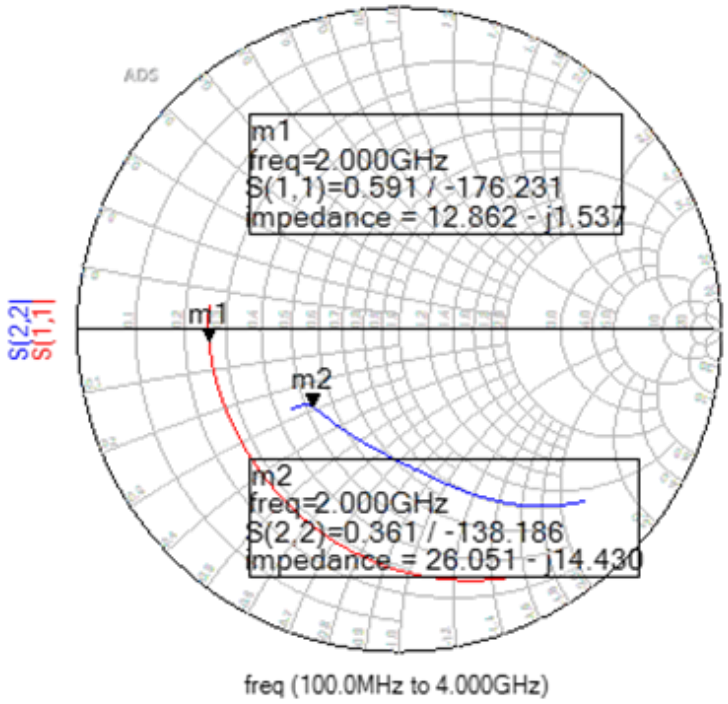
Figure 6-9: Single-ended topology for a power amplifier.

6.4.1 Simulation and layout of the HPA design

Design started by choosing an appropriate bias point after deciding that design application. We chose class A HPA with bias point V_{ds}=10V and V_{gs}=1.3V for a higher power. The current Ids are found 250mA, as shown in Figure 6-10(a). Once the bias point is selected, the next step is to determine impedances at the center frequency (2GHz). The S-parameters, particularly reflection parameters at input S_{11} and output S_{22} for frequency range 0.1GHz-4GHz, are presented in the smith chart shown in Figure 6-10(b). The selected impedance at 2GHz is from S_{11}= 12.86-j1.54 and S_{22}= 26.05-j14.43.



a) Ids (mA) vs. Vds (V)



b) Smith Chart for S11 and S22

Figure 6-10: I_{ds} (mA) vs. V_{ds} (V) plot for 2mm width gate transistor from -2.5V to +2.5V.

The circuit is simulated in ADS system software. The final schematic with the respective input and output network of lumped components is shown in Figure 6-11 below. At the input, the combination of inductance with capacitance in the π-network is used for matching networks. It provides relatively more bandwidth for matching networks. C_1 and C_4 are being used to block DC supply, while L_2 and L_3 have the same values to filter the AC supply.

The goal was to design an HPA with high linearity and more power. The band of frequency was chosen around 2GHz, which is to be precise between 1.7GHz-2.3GHz. The following values of these components are found after simulation:

C_1=1pF, C_2=C_3=0.3pF, C_4=10pF, C_5=0.9pF, L_1=2.6nH, L_2=L_3=120nH, L_4=7.5nH and L_5=1.3nH.

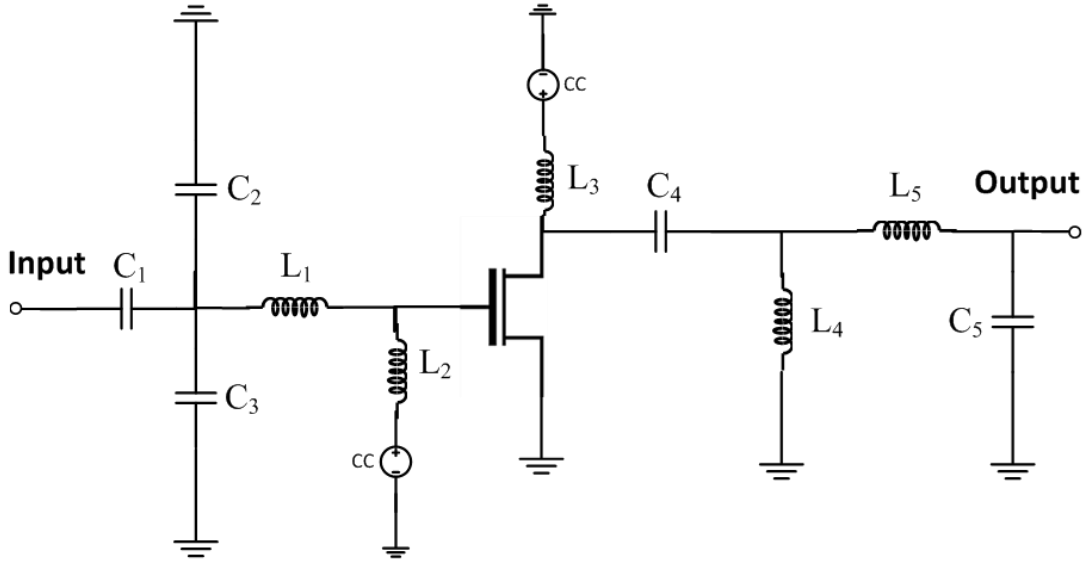
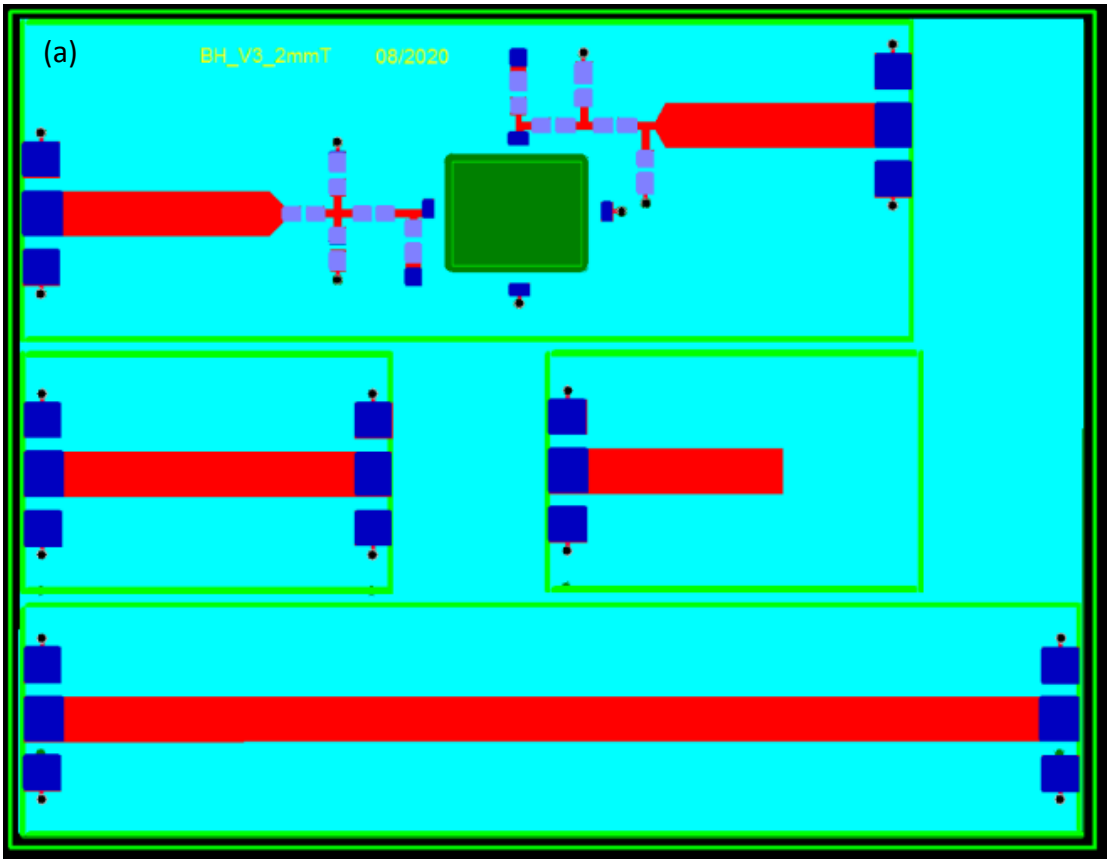


Figure 6-11: Schematic of the PA with lumped components.

The circuit's final layout is shown in Figure 6-12, which contains a full HPA based on PCB technology with Rogers substrate. It contains the de-embedding network for the transmission, which is designed by keeping in mind the TRL method. The additional transmission line was added for measurement with universal test fixture 3680K, which has a minimum 0.5cm substrate length also space between signal and ground about 300μm. The de-embedding network contains through, open, and line.

The comparison is done between measured and simulated S-parameters at input S_{11} and at output S_{22} for checking input and output matching of the device. Since the focus was 1.5GHz-2.1GHz, the matching networks are shifted towards the lower frequencies for both input and output, as shown in Figure 6-13(a). The reason behind such behavior or mismatching is the wire bond effect, which was not considered while simulating the HPA. Aluminum wires are being used for wire bonding, and about 3.5mm to connect the die with PCB. The Aluminum has higher resistance, or it is less conductive than the gold that resulted in the decrease of the HPA gain in the required bandwidth compared to the simulation that can be seen in Figure 6-13(b). We can see the gain variation of the device from 1.2GHz to 2.3GHz. The maximum variation of the gain from the simulation is about 1.75dB, which is reasonable for such a long wire bonding.

Besides that, we tried to see whether it follows the 1dB compression point of the HPA or not. For this purpose, we have plotted Pout simulated and measured at several frequencies, as shown in Figure 6-14. Measured P_{out} follows the pattern of the simulated $P_{out,}$ but it's slightly less. Unfortunately, we could not put HPA into saturation due to the Signal generator's limitation, which has max P_{out} +17dBm. Nevertheless, the HPA design's purpose was to see whether it follows the simulation to validate the transistor model, which clearly can be seen as a reasonable matching with simulation.



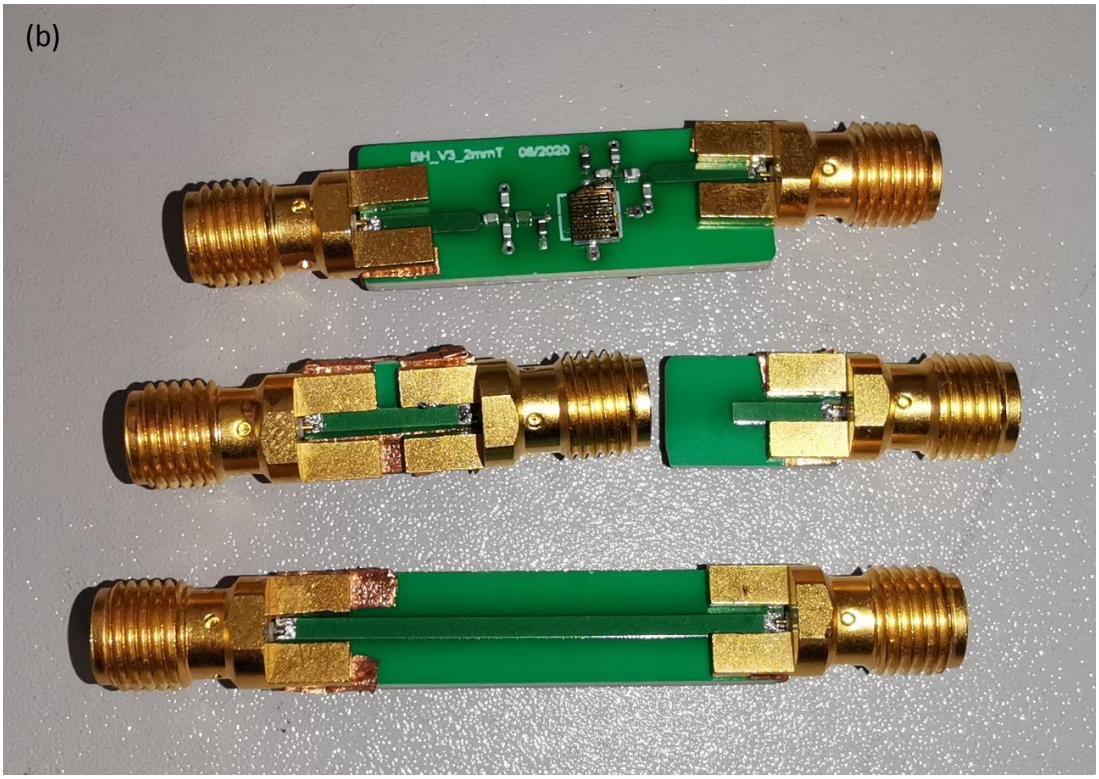
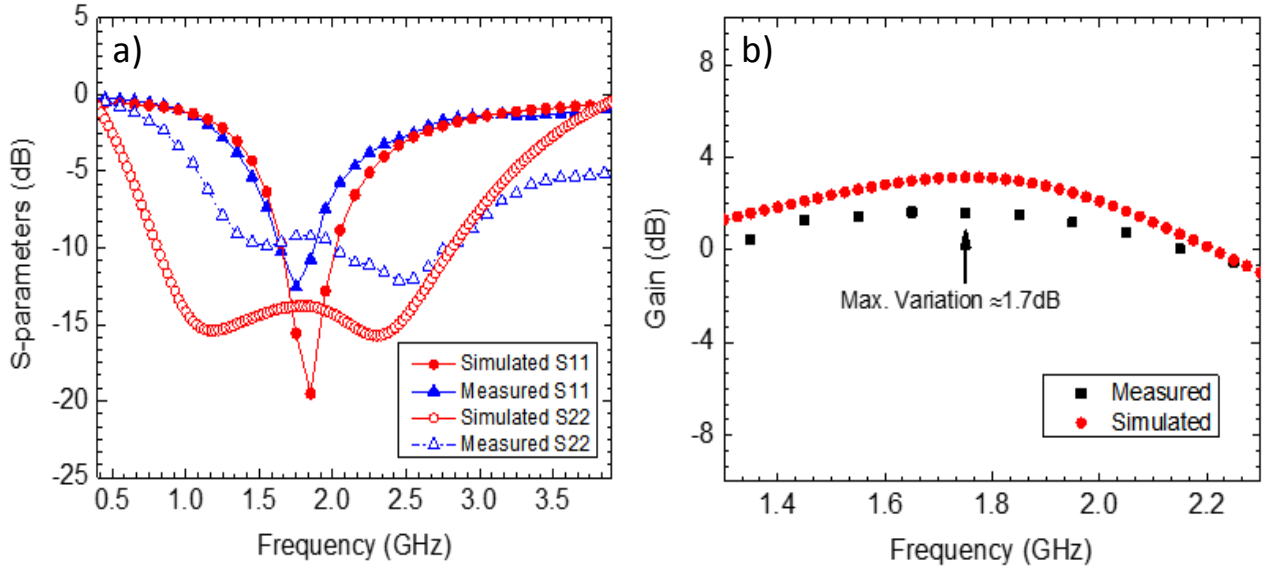


Figure 6-12: The amplifier final a) Layout and de-embedding network (Dimensions of board are 30mm×23mm). b) Hardware prototype.



a) Matching of S_{11}(dB) and S_{22}(dB)

b) S_{21}(dB) plot for gain

Figure 6-13: Impedance matching represented for (a) S_{11} and S_{22} from 0.1GHz-4GHz and (b) S_{21} from 1.6GHz- 2.1GHz.

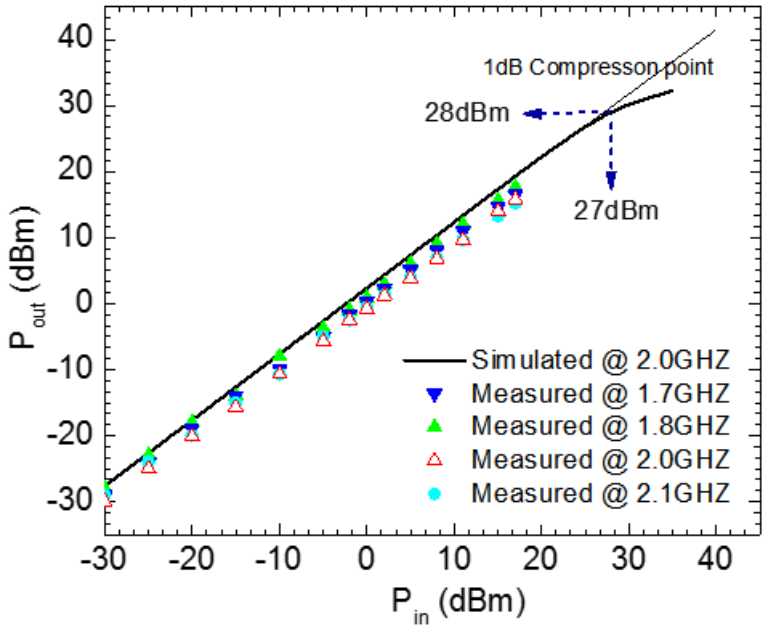


Figure 6-14: Shows the simulated vs. measured P_{out} vs. P_{in}(dBm).

Conclusion and Future Work

This thesis work was focused on the essential steps for realizing MMICs by developing PDK for GaN HEMT technology. First, DC and RF characterization work was conducted on HEMTs using an AlGaN/GaN heterojunction MOSHEMT on a silicon substrate. Based on the DC and RF characterization, the de-embedded of the passive components was done. Afterward, the gate resistance model-based distributed network made it possible to design large gate width devices to fulfill the need for more power demand. Subsequently, the HEMTs model has been verified by comparison with small signal and large signal measurements at 2 GHz. Once validation is done, all the models and mask designs partners have been integrated into a design kit under the ADS software. Finally, PDK is validated by designing PA with PCB technology.

The perspectives opened up by this work are manifold. The development of a design tool kit allows the design of simulated integrated circuits from established analytical models and the EM simulation tool to consider the couplings between elements. It will be interesting to use such a device in MMIC design to develop a circuit for different applications such as a high-power amplifier at S-band frequency.

A study can be carried out by manufacturing passive devices such as inductance, capacitance, or resistance and MOSHEMT transistor for a circuit of HPA. The different topology of HPA can be considered for such design as GaN is known for low noise along with high power, so circuit design of lower noise PA(LNA) and high power PA (HPA) separately with MMIC technology will allow us thoroughly evaluate the PDK, as well as this exercise, can bring out the process usefulness in the industry. The above-proposed study will demonstrate the process for particular application-based circuits to highlight the advantages of our technologies; meanwhile, by its critical review, we can improve the process to the PDK.

Conclusion et perspectives

Le travail au cours de cette thèse de doctorat s'est concentré sur les étapes essentielles à la réalisation des MMICs par un développement PDK pour la technologie GaN HEMT. En premier, une caractérisation DC et RF a été réalisée sur les HEMTS en utilisant l'hétérojonction MOSHEMT AlGaN/GaN sur un substrat en silicium. A travers une caractérisation DC et RF, la séparation (de-embeding) des composantes passives a été accompli. Ensuite, un développement d'un model a réseau distribué de la résistance de grille a permis la conception d'une grille large pour accommoder le besoin de la haute puissance. En plus, le model HEMT a été vérifié par une comparaison avec des mesures de petits et larges signaux à une fréquence de 2 GHz. Après, tous les modèles et la conception des masques ont été intégrés dans un outil de conception dans ADS. Finalement, PDK a été validé par une conception de PA sur technologie PCB.

Les perspectives de ce travail sont multiples. Le développement d'un outil de conception qui permet l'utilisation des circuits-intégrés simulés à partir d'un modèle analytique avec un simulateur EM pour prendre en considération les couplages entre les différents éléments. Effectivement, ceci est intéressant comme outil de développement et conception des MMIC pour les différentes applications de haute puissance sur la bande de fréquence S.

Une étude peut être réalisée en fabricant des composants passifs comme une inductance, condensateur ou résistance avec un transistor MOSHEMT pour un circuit HPA. Différentes topologies des HPA peuvent être considérées pour cette conception, en tirant profit du bruit faible et la haute puissance du GaN pour une conception des circuits à faible bruit PA(LNA) et à haute puissance PA(HPA). La technologie MMIC va nous permettre d'évaluer le PDK ainsi que l'étude de l'utilité dans des applications industrielles. L'étude proposée peut démontrer le procédé pour une application du circuit particulière, et ainsi mettre en évidence les avantages de notre technologie et améliorer les procédés du PDK à travers une évaluation critique.

List of Publication

Journal Papers:

- **Online**

Bilal Hassan, Adrien Cutivet, Meriem Bouchilaoun, Christophe Rodriguez, Ali Soltani, François Boone, and Hassan Maher, "Large Periphery GaN HEMTs Modeling Using Distributed Gate Resistance," *Phys. Status Solidi A*, vol. 216, no. 1, p. 1800505, 2019.

Bilal Hassan, Adrien Cutivet, Christophe Rodriguez, Flavien Cozette, Ali Soltani, Hassan Maher, François Boone, "Scalable small-signal modeling of AlGaN/GaN HEMT based on distributed gate resistance," 2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2019, Nashville, Tennessee, USA. IEEE Conference Proceeding.

Adrien Cutivet, Meriem Bouchilaoun, Bilal Hassan, Christophe Rodriguez, Ali Soltani, Francois Boone, and Hassan Maher, "Thermal Transient Extraction for GaN HEMTs by Frequency-Resolved Gate Resistance Thermometry with Sub-100 ns Time Resolution," *Phys. Status Solidi A*, vol. 216, no. 1, Jan. 2019.

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- **Under review**

Flavien Cozette, Bilal Hassan, Christophe Rodriguez, Eric Frayssinet, Rémi Comyn, François Lecourt, Nicolas Defrance, Natalie Labat, Francois Boone, Ali Soltani, Abdelatif Jaouad, Yvon Cordier, Hassan Maher, "New barrier layer design for the fabrication of GaN-MIS-HEMT Normally-off transistor," Semiconductor Science and Technology, Oct. 2020

- **In preparation**

Bilal Hassan, Adrien Cutivet, Flavien Cozette, Meriem Bouchilaoun, Christophe Rodriguez, Ali Soltani, François Boone, and Hassan Maher, "Large Signal Modeling of Large Periphery AlGaN/GaN HEMTs with Distributed Gate" IEEE Transactions on Electron Devices

Scientific Activities:

- **Oral presentation**

Bilal Hassan, Adrien Cutivet, Meriem Bouchilaoun, Christophe Rodriguez, Ali Soltani, François Boone, Hassan Maher, "Large Periphery GaN HEMTs Modeling Using Distributed Gate Resistance", 2018, Autrans, France. Colloque LN2 2018.

Bilal Hassan, Adrien Cutivet, Christophe Rodriguez, Flavien Cozette, Ali Soltani, Hassan Maher, François Boone, "Scalable small-signal modeling of AlGaN/GaN HEMT based on distributed gate

resistance," 2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2019, Nashville, Tennessee, USA

- **Poster presentation**

Bilal Hassan, Adrien Cutivet, Meriem Bouchilaoun, Christophe Rodriguez, Ali Soltani, François Boone, Hassan Maher, "Large Periphery GaN HEMTs Modeling Using Distributed Gate Resistance", 2018 Compound Semiconductor Week (CSW2018), 2018, Boston, USA.

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