# An Energy-Efficient Integration of a Digital Modulator and a Class-D Amplifier

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**Abstract:** Energy consumption is always a key feature in devices powered by electric accumulators. The power amplifier is the most energy-demanding module in mobile devices, portable appliances, static transceivers, and even nodes used in underwater acoustic networks. These devices incorporate a modulator, typically a pulse-width modulation (PWM) and a class-D power amplifier, for higher efficiency. We propose a technique to integrate the modulator of a transmitter and PW-modulator of a class-D amplifier to improve the overall efficiency of the system. This integrated set operates as an up-converter, phase modulator (PM), and binary phase-shift keying (BPSK) modulator under certain conditions. The theoretical concept is verified using Matlab and a model is designed and simulated in Simulink. For validation purposes, an electronic circuit is built and tested using Multisim. The results obtained by simulations and circuit implementation show that the proposed integrated system is an energy-efficient and cost-effective solution compared to conventional techniques.

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## 1. Introduction

With the increasing demand for mobility, more devices incorporating digital wireless communication systems are being operated by electric accumulators (batteries), e.g., human surveillance to crops monitoring, and aerial drones to autonomous underwater vehicles (AUVs). Preserving an accumulator's energy is of paramount importance in difficult-to-access areas, which is also the case in underwater communication systems. If the system incorporates a communication transceiver, the most energy-consuming element is the power amplifier that follows the modulator. Designers have conceived different technologies for power amplification, which are denominated into classes and denoted by capital letters: Class A, B, AB, and D. Class-D amplifiers are the most efficient in terms of power, with values on the order of 90% in practical designs [1], and are preferred in applications where autonomy is essential.

A traditional class-D amplifier consists of an analog modulator of a digital carrier followed by a switch circuit that drives the current from a DC power supply. This current passes to the load through a filter that retrieves the baseband signal. Due to their complexity, class-D amplifiers are not appropriate for small signals, but in power applications, they are the best choice because of their low losses. Obviously, the power delivered to the load is sensitive to the voltage of the DC source, and the switch has to be able to drive high current. In many of their applications, class-D amplifiers are used at high fidelity (hi-fi, 20 Hz–20 kHz) frequencies and the retrieving filter is a low-pass filter (LPF). If the amplifier is intended to be at the output stage of an ultrasonic communication system, a band-pass filter (BPF) is incorporated.

Usually, a PW-modulator is available at the input stage of a class-D amplifier. The frequency of the digital carrier of the PW-modulator must be greater than the highest frequency of the analog input signal, typically ten times. However, again, if the amplifier is part of a digital communication system, the analog input signal to the amplifier will be the output signal of a digital modulator that could be a phase-shift keying (PSK) or a frequency-shift keying (FSK) modulator. That is, the digital signal at the input of the communication transmitter will modulate an analog carrier, modulate again a digital carrier at a much higher frequency, and finally be restored to the digital modulated signal.

In our proposed design, integration of a PW-modulator of a class-D amplifier and BPF provides (a) signal amplification, (b) filtering, and (c) generation of a PSK-modulated output. The digital signal applied at the input of the class-D amplifier directly drives the power switch. This novelty in the design prevents the need of modulation before amplification, which makes the proposed design energy efficient as well as inexpensive. Finally, a BPF is used instead of a LPF at the output of the class-D amplifier to obtain an amplified PSK-modulated signal. This complex modulation is performed on a real-time basis using the ability of the class-D amplifier to provide high-efficiency in order to prolong battery life [2].

The remaining article is structured as follows. Section 2 briefly explains the state-of-the-art. Section 3 provides the theoretical background. Section 4 discusses the block diagram of the integrated system. Section 5 presents the experimental setup and results. Finally, Section 6 has the concluding remarks.

## 2. State-of-the-Art

In the past few years, several class-D amplifier designs and modulation schemes have been presented, and some of them are briefly discussed in the following section.

The class-D amplifier [3] is based on a digital pulse-width modulator. It receives digital input data and uses a digital loop filter to reduce distortion and mitigate the need of an analog-to-digital converter. The system is designed for low output power up to 1.2 W, and to keep away from the necessities of additional filtering, a sigma-delta modulator is used. The proposed system is designed using complementary metal–oxide–semiconductor (CMOS) technology and has been tested to drive a load of an 8 Ω speaker with a signal-to-noise ratio (SNR) of 99.9 dB with 91% efficiency.

A class-D amplifier based on the delta-sigma modulator with uniform pulse-width modulation is presented in [4]. The major design blocks are an interpolation filter, digital delta-sigma modulator, uniform pulse-width modulator, driver circuitry, and power stage. A 1-bit, 6th-order noise shaping modulator with a uniform pulse-width modulator quantizer is used along with the pole moving technique to balance the modulator and make the noise transfer function more determined. The system has been simulated with a 1 kHz sine wave, and a 120 dB SNR has been achieved.

In [5], a high-power pulse-width modulation model based on the class-D amplifier is discussed. To eliminate the effect of 3rd and 5th harmonics, the proposed triple-pulse model is designed by adding two narrow pulses with an equivalent comparative to the original single pulse. Initially, the model is verified by simulations, and then a platform is designed with underwater acoustic transducers submerged in a water tank to test the functionality of the system. From the experiments, it was found that the proposed amplifier consumes low power, which reduces 41% of the 3rd and 5th harmonic energy [5].

A class-D amplifier using pulse-width modulation is designed in [6]. The system consists of modulation, and power and filter stages. In this research, two modulation techniques: (a) Pulse-width modulation and (b) pulse density modulation, are used. The system has been verified by PSpice simulations to test the total harmonic distortion using both modulation techniques with a 1 kHz test tone and switching frequency in the range of 300–800 kHz. From the simulations, it was found that the total harmonic distortion of the pulse density modulation is less at higher frequencies.

A low-voltage class-D amplifier design is presented in [7]. The objective of the research is to propose a class-D amplifier for audio applications with minimum distortion. The analysis is performed using a

pulse density modulation (PDM) technique for different test tone frequency ranges from 0.7 to 5 kHz with three amplitudes, 0.5, 0.8, and 1.0 V, using the carrier frequency range of 500–2000 kHz. From the results, it was found that the total harmonic distortion is a function of both amplitude and frequency of the test tone. For the highest switching frequency, i.e., 2000 kHz, and at the smallest amplitude of the input signal, the lowest value of total harmonic distortion was achieved at less than 1%.

## 3. Theoretical Background

PW-modulations can be classified according to several criteria. The first is pulse values, which can be symmetric or asymmetric. The former means $V_L = 0$ V and the later means $V_L = -V_H$, where $V_L$ and $V_H$ are, respectively, the low and high levels of the output voltage. The symmetric case is slightly more complex to generate from the circuit point of view, and its frequency spectrum has a much lower DC component and larger fundamental and harmonic components. However, other than that, it has little influence on the frequency spectrum of the modulated signal.

A second criterion is related to the fact that the input is a continuous signal but the output signal is a train of pulses, which means that the input signal has been somehow sampled at certain instants. The way sampling is performed also has an impact on the frequency spectrum. There are two options, the so-called uniform sampling, when it is synchronous with the system clock, or the natural sampling, which happens when simple circuits are used to modulate the pulses, i.e., when sampling is achieved by a simple comparator circuit and is not synchronous with the system clock. The basic block diagram of a PW-modulator is shown in Figure 1 [8]. Of course, the average sampling frequency over a long period of time is the frequency of the system clock.
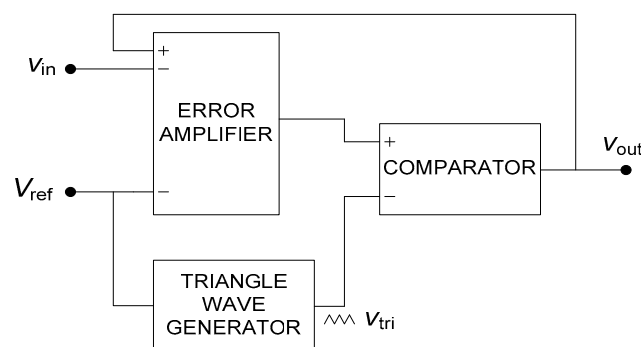


**Figure 1.** Basic block diagram of a PW-modulator [8].

The third criterion is related to how the sample modulates the output pulses. The samples can determine the positions of either the leading edges, the trailing edges, or both. In the double-edge case, the position of both edges can be symmetrically determined by a single sample or each of them can be determined by two consecutive samples.

Song and Sarwate determined the frequency spectra of different possible PW-modulations [9]. A brief summary of their work is presented here, for the sake of completeness. Let us assume the following conditions: (i) Symmetric pulse amplitudes are −1 and 1 V. (ii) The input signal $x(t)$ is frequency-limited, the module of its maximum amplitude is 1 V, and it has no DC component. (iii) The modulation index is 100% and the idle duty cycle is 50%. (iv) The pulse repetition frequency $f_c$ (better than sampling frequency in natural sampling) is at least $\pi$ times the maximum frequency of the input signal. Under these conditions, the Fourier expansions of the natural sampling of the PW-modulated signals are [9]:

$$p_{\text{TE}}(t) = x(t) + \sum_{k=1}^{\infty} \frac{2}{k\pi} \left[ \sin(2\pi k f_c t) - (-1)^k \sin(2\pi k f_c t - k\pi x(t)) \right], \tag{1}$$

$$p_{\text{LE}}(t) = x(t) + \sum_{k=1}^{\infty} \frac{2}{k\pi} \left[ (-1)^k \sin(2\pi k f_c t + k\pi x(t)) - \sin(2\pi k f_c t) \right], \tag{2}$$

$$p_{\text{DE}}(t) = x(t) + \sum_{k=1}^{\infty} \frac{2(-1)^k}{k\pi} \left[ \sin\left(2\pi k f_c t + k\pi \frac{x(t)+1}{2}\right) - \sin\left(2\pi k f_c t - k\pi \frac{x(t)+1}{2}\right) \right], \tag{3}$$

where the subscripts TE, LE, and DE stand, respectively, for the trailing-edge, leading-edge, and double-edge (asymmetric version). If the trigonometric identities,

$$\sin \alpha \pm \sin \beta = 2 \sin \frac{1}{2}(\alpha \pm \beta) \cos \frac{1}{2}(\alpha \mp \beta), \tag{4}$$

$$\sin(\alpha + \beta) = \sin \alpha \cos \beta + \cos \alpha \sin \beta, \tag{5}$$

are used, every term in the summations of (1)–(3) becomes

TE, k odd :
$$\frac{4}{k\pi} \cos\left(\frac{k\pi x(t)}{2}\right) \cos\left(2\pi f_c k t - \frac{k\pi x(t)}{2} + \frac{\pi}{2}\right), \tag{6}$$

TE, k even :
$$\frac{4}{k\pi} \sin\left(\frac{k\pi x(t)}{2}\right) \cos\left(2\pi f_c k t - \frac{k\pi x(t)}{2}\right), \tag{7}$$

LE, k odd :
$$\frac{4}{k\pi} \cos\left(\frac{k\pi x(t)}{2}\right) \cos\left(2\pi f_c k t + \frac{k\pi x(t)}{2} - \frac{\pi}{2}\right), \tag{8}$$

LE, k even :
$$\frac{4}{k\pi} \sin\left(\frac{k\pi x(t)}{2}\right) \cos\left(2\pi f_c k t + \frac{k\pi x(t)}{2}\right), \tag{9}$$

DE, k odd :
$$\frac{-4}{k\pi} \sin\left(\frac{k\pi}{2}\right) \cos\left(\frac{k\pi x(t)}{2}\right) \cos(2\pi f_c k t), \tag{10}$$

DE, k even :
$$\frac{4}{k\pi} \cos\left(\frac{k\pi}{2}\right) \sin\left(\frac{k\pi x(t)}{2}\right) \cos(2\pi f_c k t). \tag{11}$$

When the six terms in (6)–(11) are observed, it is clear that all three PWM versions will include the frequency spectrum of $x(t)$ in their base band, and, as a consequence, all of them can be used in class-D amplifiers. However, we want to now bring attention to the harmonic contents. Double-edge-modulated signals have harmonic components that are amplitude-modulated by $x(t)$, while single-edge modulations have harmonic components modulated both in amplitude and phase. This remark leads to the idea of using a harmonic component to generate a simple modulation of $x(t)$.

## 4. Block Diagram of the Integrated System

### 4.1. Preferred Modulation

Angular modulation schemes such as FSK and PSK are more robust than linear techniques such as amplitude shift keying (ASK) or on–off keying (OOK) [10] while maintaining simplicity. Quadrature amplitude modulation (QAM) modulation has an increased spectral efficiency, but transceivers are more complicated and more power needs to be transmitted to achieve a similar bit-error rate (BER) [11]. Among its resources, the software-defined radio (SDR) includes direct digital synthesis (DDS), which provides sinusoidal signals with arbitrary frequency or phase [12–14]. This makes PSK a good choice for wireless links where power is a limited resource.

A switching-circuit phase modulator is shown in Figure 2 [10]. Actually, the signal at the output of the comparator block of Figure 2 is the rising edge PWM of $v_{in}$, with a carrier frequency of $2f_c$. The Flip-Flop circuit divides the number of pulses between the two.
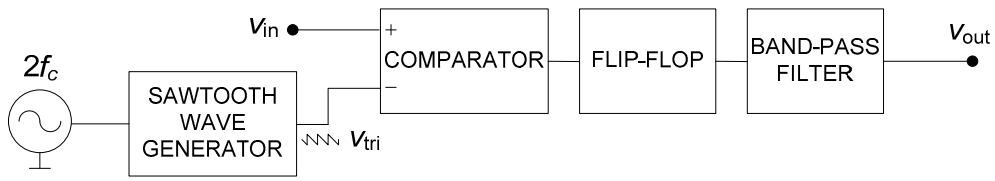
**Figure 2.** Switching-circuit phase modulator [10].

## 4.2. Integrated System

The block diagram of the class-D amplifier is shown in Figure 3. The first block in the diagram is a PW-modulator. The switching block consists of two metal-oxide semiconductor field-effect transistor (MOSFET) and the corresponding gate drivers. If the three diagrams in Figures 1–3 are compared, we realize that if the low-pass filter is replaced by a band-pass filter, the high-power output signal will be the carrier modulated in phase by $v_{in}$. To improve power efficiency of the wireless communication system, a question arises: As the class-D amplifier already contains a modulator, is it possible to directly drive the PW-modulator with a signal that, when band-pass filtered, becomes the PSK modulation of the digital input? The idea is shown schematically in Figure 4 [15]. Obviously, the coder blocks in the upper and lower parts of Figure 4 will have to be different.
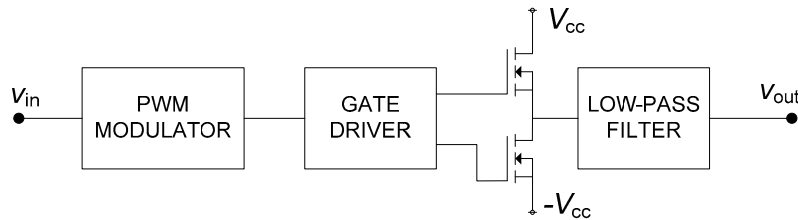


**Figure 3.** Block diagram of a half-bridge class-D power amplifier.
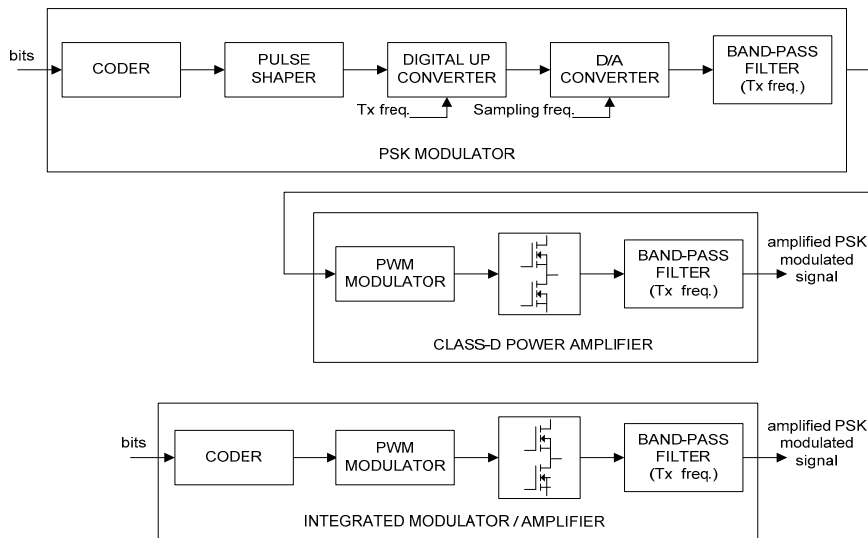


**Figure 4.** Block diagram of a PSK modulator that drives a class-D power amplifier [15].

The coder and the PW-modulator blocks of the lower part of Figure 4 have already been developed [16]. They can be implemented either with a microcontroller or a digital signal processor (DSP) unit with the architecture of Figure 5. The frequency of the clock input is N times larger than the sampling frequency. Additionally in [17], it has been used to directly feed the switching circuit of the class-D power amplifier in audio applications. The question now is how to obtain the FSK-modulated signal. At this point, we realize that by using a rectangular carrier, we can easily obtain a PSK output instead of an FSK.
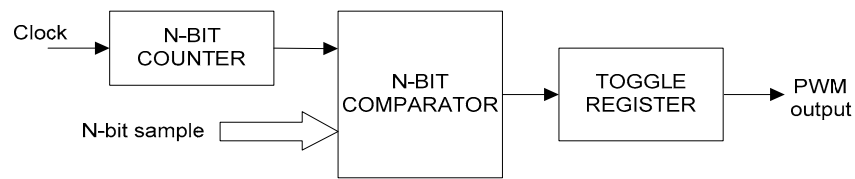
**Figure 5.** Architecture of coder and PW-modulator blocks [16].

The proposed integrated PSK modulator is sketched in Figure 6. The input data bits are converted to a bipolar voltage signal that eventually multiplies a square bipolar carrier, changing its phase according to the input bit. The square signal then drives the power bridge of the class-D amplifier, whose output goes through a band-pass filter centered at the frequency of the bipolar carrier, to obtain a PSK-modulated signal.
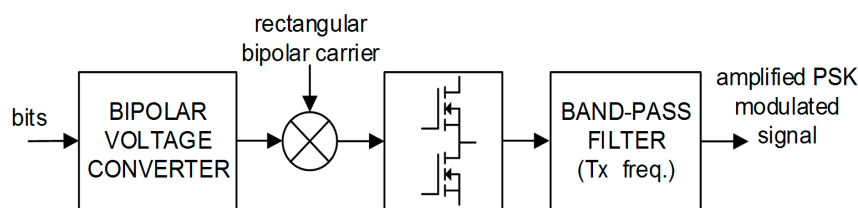


**Figure 6.** Integrated PSK modulator/amplifier (functional diagram).

## 5. Experimental Setup and Results

### 5.1. Simulation

The PSK modulator using the PWM and a band-pass filter, as shown in the lower part of Figure 4, has been simulated with the help of Matlab. The coder simply converts bits into a symmetrical normalized voltage signal (±1 V). The output band-pass filter is tuned to the carrier frequency of the PW-modulator. Figure 7 shows the input signal, the carrier, and the modulated PSK signal at the filter output. Figure 8 shows the power spectrum at the input of the band-pass filter. For the simulations, the following numbers have been used: (±1.5 V) sawtooth carrier signal, $f_c = 19.8$ kHz; bit duration time, $T_s = 0.5$ ms. The length of the simulation was 1000 bits, randomly generated. Only five bits are shown below, for the sake of clarity, but the whole simulation provided correct results.
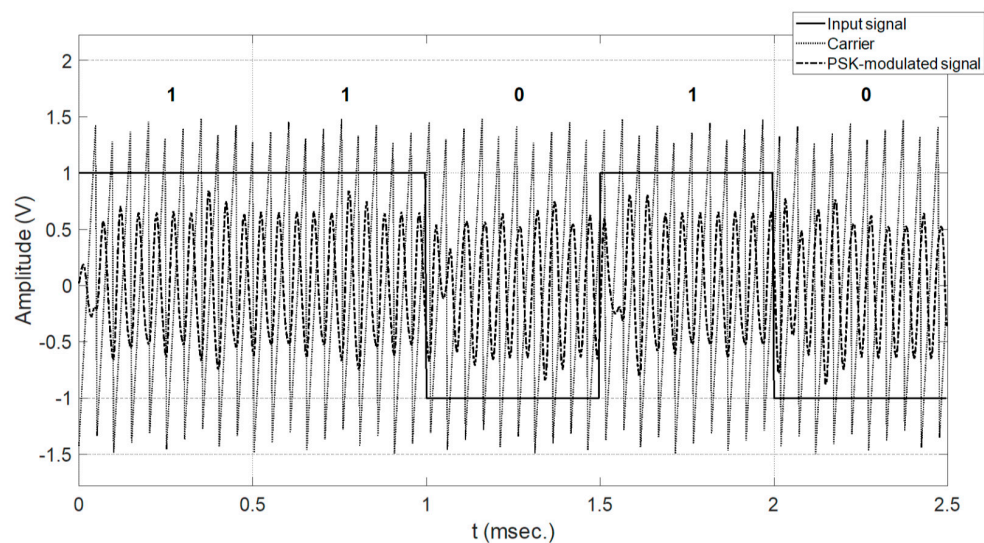


**Figure 7.** Input signal, carrier, and modulated PSK signal at the filter output of Figure 4.
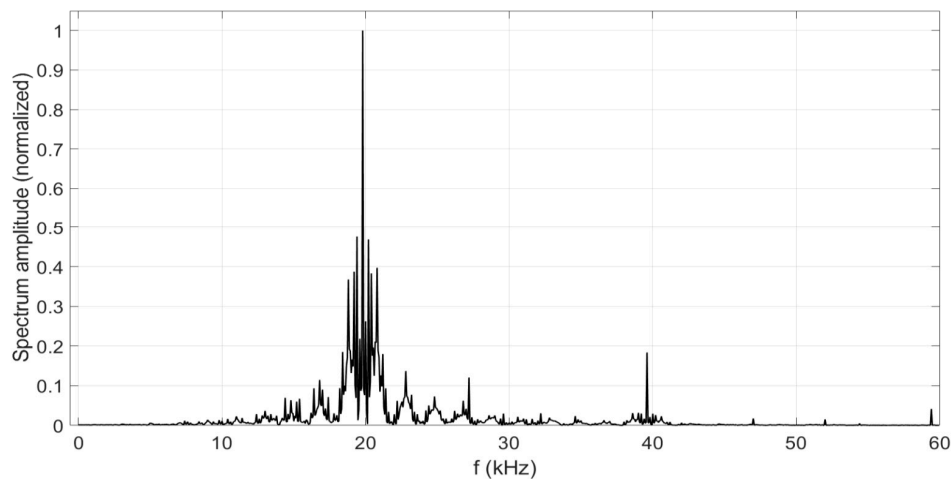
**Figure 8.** Normalized spectrum of the modulated signal at the filter output of Figure 4.

Figure 8 shows the normalized spectrum of the modulated signal at the output of the band-pass filter of the lower part of Figure 4. A MATLAB built-in PSK demodulator ("pmdemod") has been used to verify that the modulation process was correct. Figure 9 shows the same five bits shown in Figures 7 and 8 after using "pmdemod".
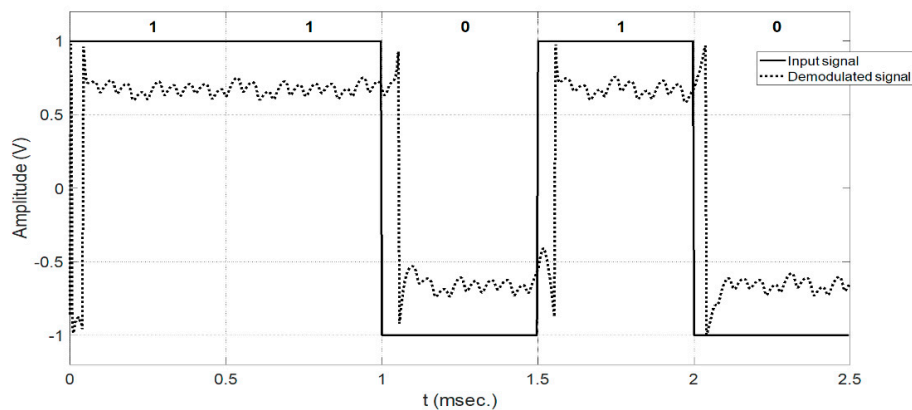


**Figure 9.** Demodulated signal, to verify the whole process.

To be doubly sure of the validity of the concept, the circuit in the lower part of Figure 4 has been designed and simulated also with the help of SIMULINK, as shown in Figure 10. A binary input signal with the bit duration time $T_s = 0.5$ ms is applied to the input of the unipolar-to-bipolar block that converts it into a symmetrical normalized voltage signal ($\pm 1$ V). This signal is compared to the sawtooth carrier frequency $f_c = 19.8$ kHz to obtain a PW-modulated signal. The signal is then converted into bipolar and a gain of 30 is provided to represent the amplification through the power stage as per the functionality of the class-D amplifier. The band-pass filter tuned to the carrier frequency of the PW-modulator output blocks undesired frequency components and provides a PSK-modulated output. A scope and spectrum analyzer are used to measure the output in time and frequency domains.
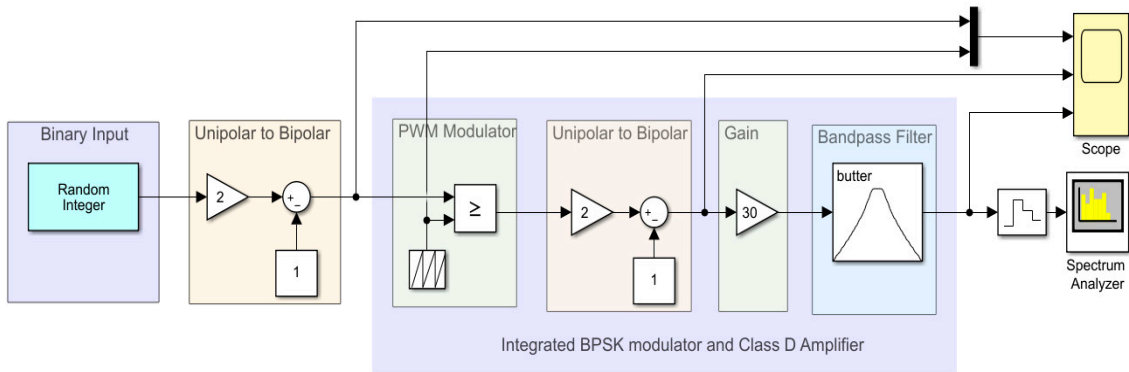
**Figure 10.** Proposed Simulink model.

Figure 11 shows the results obtained from the Simulink model in the time domain using the scope. In this figure, the binary input signal has been shown with a red color in the top part of the figure. In the same figure, the sawtooth waveform that acts as a carrier signal has been shown with a green color. The middle part of the figure is the PW-modulated signal that has been converted to a bipolar signal and is shown in blue at channel 2 of the scope. Finally, the amplified and filtered PSK-modulated output received from the band-pass filter has been shown with a purple color in the bottom part of the figure.
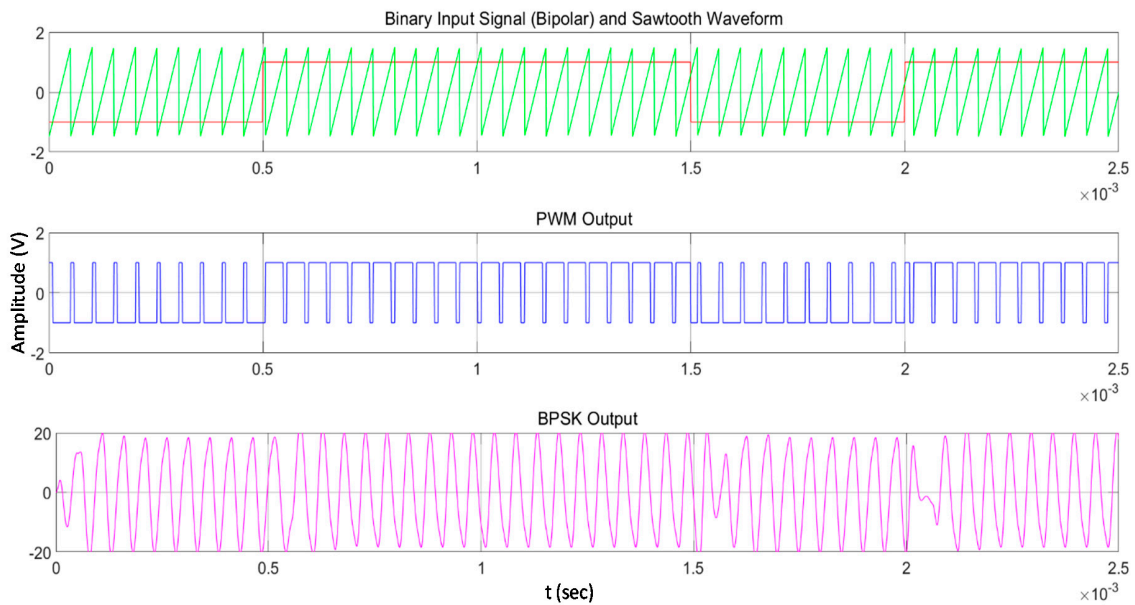


**Figure 11.** Simulation results of proposed model.

Figure 12 shows the overall power spectrum of the proposed model. As is evident, the fundamental frequency component of the system will have maximum amplitude; it can be observed that at 19.8 kHz, the third and fifth harmonics are visible at around 59 and 99 kHz, respectively. A band-pass filter tuned at the carrier frequency has been used to eliminate unwanted frequency components and to obtain a binary phase-shift keying (BPSK)-modulated output.
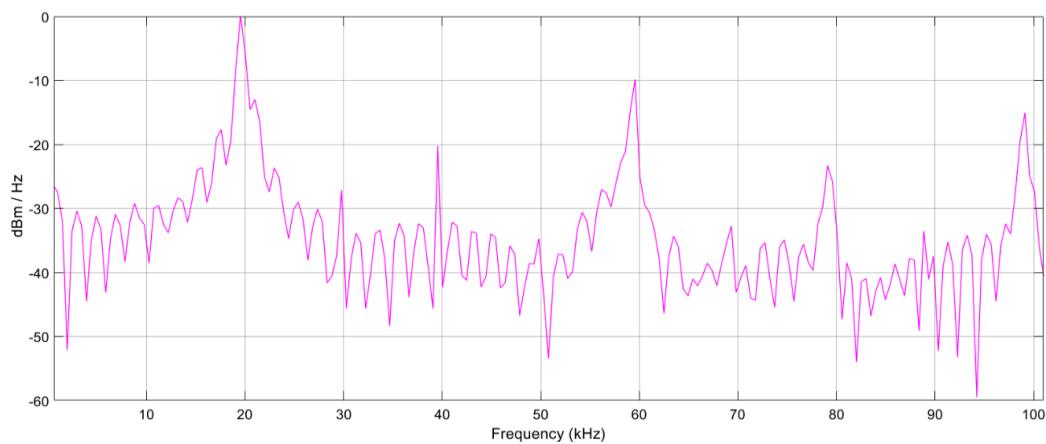
**Figure 12.** Power spectrum of proposed model.

*5.2. Prototype*

To fully demonstrate the concept, a circuit has been designed in interactive software Multisim [18] that not only provides powerful simulation and analysis, but is also used for the printed circuit board (PCB) design. A schematic of the proposed circuit prototype is shown in Figure 13. The circuit can be divided into five major blocks for better comprehension. On the left side, the 555 timer IC generates a sawtooth waveform of $f_c = 19.8$ kHz to be used as a carrier, and the OPAMP LM358 shown at the bottom adjusts the gain and offset of the waveform. The second block is the comparator where a binary input signal is applied to the $+ve$ input of the IC LM393, while the carrier is connected to the $-ve$ input. The output of the comparator is a pulse width-modulated (PWM) signal. The third block is the driver circuitry and works as a buffer and designed using IC LM358 to prevent the loading effect and to drive the fourth block, i.e., IRLZ44N Power MOSFET transistors. The amplified signal is fed into the fifth block, i.e., the second-order band-pass passive LC filter circuit removes unwanted signal components and provides an amplified PSK-modulated signal at the output.
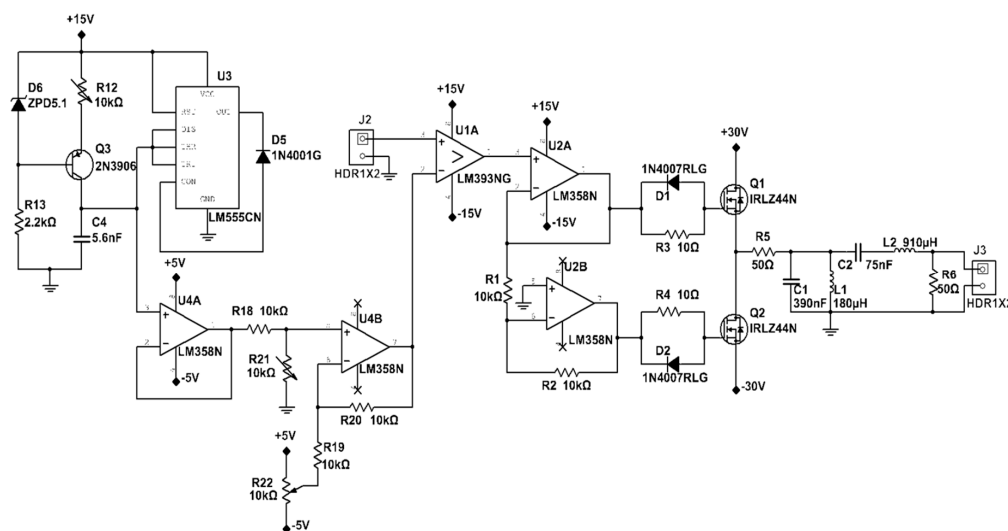


**Figure 13.** Circuit diagram of proposed design.

*5.3. Results*

Figure 14 shows the waveform acquired from testing the prototype circuit, which is similar to the waveform as obtained in Figure 11 from the simulation. The horizontal axis represents the time in seconds, while the amplitude is shown on the vertical axis in volts. The sawtooth waveform shown in green represents the carrier, i.e., the $-ve$ input of the comparator IC LM393, while the binary input

signal is shown in red applied to the +*ve* input of the comparator. The PWM output of the comparator is shown in blue and passes to the buffers to drive the power MOSFET transistors. Finally, the filter output, i.e., amplified PSK-modulated signal, is shown in purple.
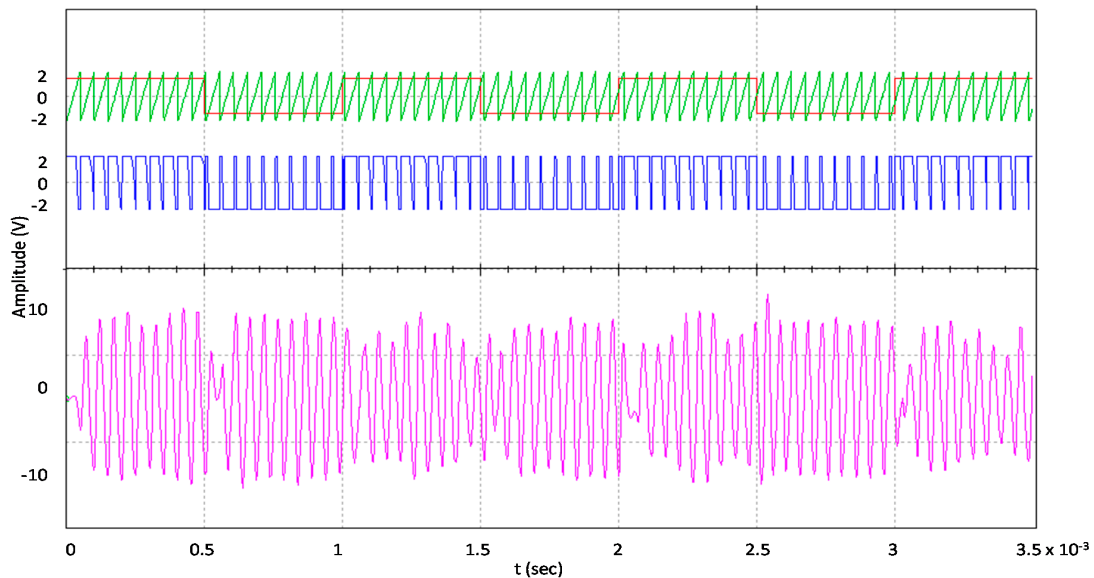


**Figure 14.** Waveform of the proposed circuit.

*5.4. Discussion*

A qualitative comparison with the state-of-the-art is presented in Table 1. The input signal type in most of the designs is analog, while our proposed amplifier design accepts a digital signal of 1 V. We have tested our design on a 2 kHz input frequency range compared to 1 kHz in many cases and 5 kHz in [6]. The switching frequency used in the state-of-the-art is in the range of 200–2000 kHz, while in our case, it is much lower, i.e., 19.8 kHz, which is a plus point. Mostly, PWM or, in some cases, PDM is used inside the class-D amplifier followed by an LPF. We used BPF that not only filters but provides PSK modulation without using any modulator block. This unique feature is the novelty of our design that reduces the cost as we did not use any modulator, as well as increases the power efficiency of the overall system. The proposed design can deliver up to 6 W under a controlled environment at room temperature.

**Table 1.** Comparison with state-of-the-art.

| Parameter | [3] | [4] | [5] | [6] | [7] | This Work |
|---|---|---|---|---|---|---|
| Input signal type | Digital | Analog | Analog | Analog | Analog | Digital |
| Input signal voltage (V) | - | - | - | 1 | 1 | 1 |
| Input signal frequency (kHz) | - | 1 | - | 1, 5 | 1 | 2 |
| Switching frequency (kHz) | 390 | 384 | 200 | 300–800 | 500–2000 | 19.8 |
| Class-D amplifier modulation | PWM | UPWM | PWM | PWM | PDM | PWM |
| Filter type | Digital | - | LPF | LPF | LPF | BPF |
| Output type | Amplified | Amplified | Amplified | Amplified | Amplified | Amplified PSK |
| Output power (W) | 1.2 | - | - | - | - | 6 |

## 6. Conclusions

In this paper, the integration of the modulator of a transmitter and PW-modulator of a class-D amplifier is presented to improve the energy efficiency of the system. The concept stems from the idea of the class-D amplifier where a power switching block is driven by a digital carrier modulated by the signal of interest. A band-pass filter is then used to obtain an amplified PSK output. The concept can be of vital importance in the ultrasound band used in applications related to underwater acoustic

communications. We use several steps to verify the concept. Initially, the hypothesis is verified using Matlab, and then a model is designed and simulated in Simulink. Finally an electronic circuit is built and experimentally tested to validate the feasibility of the concept. The results obtained by simulations and circuit implementation show that the proposed integrated system is an energy-efficient and cost-effective solution compared to existing solutions.

Future work includes optimizing the performance of the electronic circuit by adjusting various parameters and component values. We intend to use this prototype in an energy-efficient underwater acoustic modem.

**Author Contributions:** P.O. and R.T. conceived the idea, P.O. proposed the model and wrote the manuscript, M.-Á.L.-N. performed the model fitting in Matlab. M.Y.I.Z. designed and simulated the model in Simulink, built an electronic circuit in Multisim and validated the experimental results. All authors have read and agreed to the published version of the manuscript.

**Conflicts of Interest:** The authors declare no conflict of interest.

## References

1.  Honda, J.; Adams, J. Class D Audio Amplifier Basics, Application Note AN-1071. International Rectifier (USA), February 2005. Available online: https://www.infineon.com/dgdl/an-1071.pdf (accessed on 20 July 2020).
2.  Xu, D.; Zhou, G.; Huang, R.; Liu, X.; Liu, F. High Efficiency Half Bridge Class-D Audio Amplifier System with Front-end Symmetric Bipolar Outputs LLC Converter. In *IEEE Transactions on Industrial Electronics*; IEEE: Piscataway, NJ, USA, 2020.
3.  Auer, M.; Karaca, T. A Class-D Amplifier with Digital PWM and Digital Loop-Filter using a Mixed-Signal Feedback Loop. In Proceedings of the ESSCIRC 2019-IEEE 45th European Solid State Circuits Conference (ESSCIRC), Krakow, Poland, 23–26 September 2020; pp. 153–156. [CrossRef]
4.  Kuo, C.-H.; Liou, Y.-J. A Delta-Sigma Modulator with UPWM Quantizer for Digital Audio Class-D Amplifier. In Proceedings of the 2019 MIXDES-26th International Conference "Mixed Design of Integrated Circuits and Systems", Rzeszow, Poland, 27–29 June 2020; pp. 293–297. [CrossRef]
5.  Li, Y.; Duan, F.; Jiang, J.; Wang, X. High-efficiency and low-consumption underwater sonar transmitter with improved triple-pulse HP-PWM signal model based on class D amplifier. *EURASIP J. Wirel. Commun. Netw.* **2016**. [CrossRef]
6.  Galić, J.; Pešić-Brdjanin, T.; Iriškić, L. Class-D Audio Amplifier using Pulse Width Modulation. In Proceedings of the 6th Small Systems Simulation Symposium 2016, Nis, Serbia, 12–14 February 2016; pp. 133–136.
7.  Kovačević, S.; Pešić-Brdjanin, T.; Galić, J. Class D Audio Amplifier with Reduced Distortion. In Proceedings of the 2018 International Symposium on Industrial Electronics (INDEL), Banja Luka, Bosnia, Herzegovina, 1–3 November 2018; pp. 1–4. [CrossRef]
8.  Caldwell, J. Analog Pulse Width Modulation, TI Precision Designs: Verified Design (Texas Instruments Application Recommendations). June 2013. Available online: http://www.ti.com/lit/ug/slau508/slau508.pdf (accessed on 20 July 2020).
9.  Song, Z.; Sarwate, D.V. The frequency spectrum of pulse width modulated signals. *Signal Process.* **2003**, *83*, 2227–2258. [CrossRef]
10. Crilly, P.B.; Carlson, A.B. *Communication Systems*, 5th ed.; McGraw-Hill Education: New York, NY, USA, 2009.
11. Proakis, J.G.; Salehi, M.; Bauch, G. *Contemporary Communication Systems Using MATLAB*; Nelson Education: Toronto, ON, Canada, 2012.
12. Mitola, J. *Software Radio: Object-Oriented Approaches to Wireless Systems Engineering*; John Wiley & Sons: Hoboken, NJ, USA, 2000.
13. Grayver, E. *Implementing Software Defined Radio*; Springer Science & Business Media: Berlin/Heidelberg, Germany, 2012.

14. Texas Instruments Mixed-Signal Products, "FSK Modulation and Demodulation with the MSP430 Microcontroller", 1998. Application Report SLAA037. Texas Instruments. Available online: http: //www.ti.com/lit/an/slaa037/slaa037.pdf (accessed on 20 July 2020).

15. Pascual, C.; Song, Z.; Krein, P.T.; Sarwate, D.V.; Midya, P.; Roeckner, W.J. High-fidelity PWM inverter for digital audio amplification: Spectral analysis, real-time DSP implementation, and results. In *IEEE Transactions on Power Electronics*; IEEE: Piscataway, NJ, USA, 2003; Volume 18, pp. 473–485. [CrossRef]

16. Koutroulis, E.; Dollas, A.; Kalaitzakis, K. High-frequency pulse width modulation implementation using FPGA and CPLD ICs. *J. Syst. Archit.* **2006**, *52*, 332–344. [CrossRef]

17. Nguyen, K.C.; Sarwate, D.V. Up-sampling and natural sample value computation for digital pulse width modulators. In Proceedings of the 2006 40th Annual Conference on Information Sciences and Systems, Princeton, NJ, USA, 22–24 March 2006; pp. 1096–1101. [CrossRef]

18. National Instruments Multisim. Available online: https://www.ni.com/en-lb/support/downloads/software-products/download.multisim.html#312060 (accessed on 20 July 2020).