Development of a Multichannel Wideband Radar Demonstrator

By

Kevin Carr

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Dr. Carl Leuschen, Chair

Committee members

Dr. Fernando Rodriguez-Morales, Co-chair

Dr. James Stiles

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The Thesis Committee for Kevin Carr certifies
that this is the approved version of the following thesis :

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Dr. Carl Leuschen, Chair

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Abstract

With the rise of software defined radios (SDR) and the trend towards integrating more RF components into MMICs the cost and complexity of multichannel radar development has gone down. High-speed RF data converters have seen continuous increases in both sampling rate and resolution, further rendering a growing subset of components in an RF chain unnecessary. A recent development in this trend is the Xilinx RFSoC, which integrates multiple high speed data converters into the same package as an FPGA. The Center for Remote Sensing of Ice Sheets (CReSIS) is regularly upgrading its suite of sensor platforms spanning from HF depth sounders to Ka band altimeters. A radar platform was developed around the RFSoC to demonstrate the capabilities of the chip when acting as a digital backend and evaluate its role in future radar designs at CReSIS. A new ultra-wideband (UWB) FMCW RF frontend was designed that consists of multiple transmit and receive modules with a 6 GHz bandwidth centered at 5 GHz. An antenna array was constructed out of Vivaldi elements to validate radar system performance. Firmware developed for the RFSoC enables radar features such as beam forming, frequency notching, dynamic stretch processing, and variable gain correction. The feature set presented here may prove useful in future sensor platforms used for the remote sensing of snow, soil moisture, or crop canopies.

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Introduction

1.1 Background

1.1.1 Overview of CReSIS Projects

The Center for Remote Sensing of Ice Sheets (CReSIS) regularly designs and deploys radars over the polar regions for monitoring properties such as ice sheet thickness, bedrock topography, sea-ice extent, and snow accumulation. A wide array of sensors are employed spanning from VHF and UHF sounding units to Ka-band altimeters [2]. Through Operation IceBridge (OIB) some of the sensors are used in conjunction with satellite-borne altimeters (ICESat, ICESat-2) to provide continuous operation during satellite downtime and extend the measurements with higher resolution data [3]. The original OIB sensor platform included two high resolution FMCW radars for altimetry and internal layer mapping of firn, a 2 GHz - 8 GHz snow radar [4] and a 12 GHz - 18 GHz radar altimeter [5]. These systems were improved upon with the development of a higher performance 2 GHz - 18 GHz snow radar [6] that has seen continued upgrades [7]. While those radars are all airborne platforms, near-ground systems are in use as well. A 2 GHz - 18 GHz radar similar to the snow accumulation radar has been used for scattering analysis of wheat canopies [8] and a more compact system is under development for soil moisture monitoring [9].

The radar systems for snow and wheat measurements are all single channel, ultra-wide bandwidth (UWB) systems with high range resolution.[1] They are typically operated as bistatic synthetic aperture radars (SAR) with colocated horn antennas, building a depth profile in the along-track di-

[1]The FCC currently defines UWB transmissions as any with bandwidths exceeding either 500 MHz or 20% of the arithmetic center frequency.

rection and sweeping the flight path over a region to effectively cover a 2D area. The cross-track beamwidth of these systems is fixed and no processing can be done on them. The systems at CReSIS using active arrays are lower bandwidth, higher power sounding units such as the Multichannel Coherent Radar Depth Sounder (MCoRDS) [2]. MCoRDS is a multi-receiver system that carries out SAR processing in the along-track direction and array processing in the cross-track direction. This added array processing allows for more comprehensive clutter reduction and a wider effective swath which means potentially fewer passes over a region to acquire an equivalent amount of high quality data.

In general, UWB systems require components capable of operating over a wider bandwidth than narrow bandwidth systems, which can increase design complexity and cost. Expanding a UWB system into a multichannel configuration creates the additional issue of maintaining phase alignment across several channels. This is difficult for higher frequencies as the decrease in wavelength means smaller physical and digital variations can have a greater effect and the manufacturing tolerances go down. The Xilinx RFSoC eliminates much of the complexity involved in keeping the data converters of each channel synchronized leaving only physical differences in the RF chain as potential sources of phase error, but the flexibility of the digital backend should allow a system to compensate for those differences as well.

1.1.2 Summary of FMCW Operating Principles

The high range resolution of the snow and wheat radars is achieved using a frequency modulated continuous wave (FMCW) radar architecture. Introducing frequency modulation is what allows a CW radar to distinguish range in addition to velocity. A high level view of the typical setup is shown in figure 1.1.

In the case of this system, the pattern generator produces a linear FM chirp waveform (LFM), a signal that sweeps linearly in frequency over time. Nonlinear waveforms are used as well [10, 11] as they provide some advantages over traditional LFM, however the processing requirements increase the complexity beyond what is useful for this review. The LFM chirp is passed through

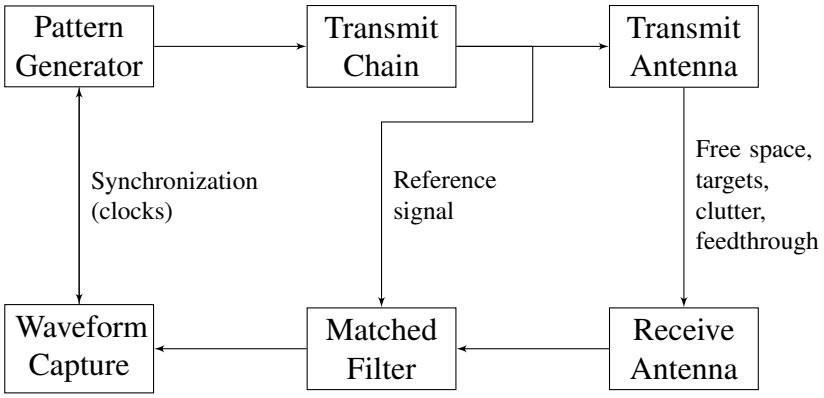

Figure 1.1: Simplified high level representation of FMCW architecture

an RF conditioning chain (typically an LNA and filter) to the transmit antenna and to a matched filter. From the transmit antenna the signal is reflected off the target back to the receive antenna. In a monostatic setup only a single antenna is present and either a circulator or a transmit/receive switch is placed in front of the antenna to handle either simultaneous transmit and receive periods or non-overlapping transmit and receive periods respectively. The matched filter is implemented in this case with an RF mixer; the transmitted signal and received signal are multiplied in the time domain to produce the sum and difference products. The behavior of the two waveforms is shown in Figure 1.2. The two diagonal lines, increasing in frequency with respect to time, represent,

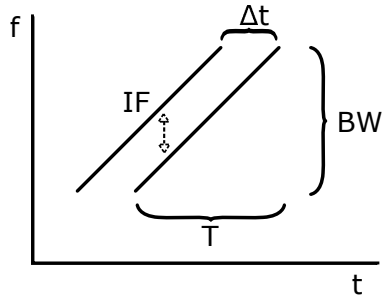

Figure 1.2: Transmit and receive LFM waveforms in FMCW operation. Horizontal axis represents time and vertical axis represents frequency.

left to right, the transmit and receive chirps. The duration of a single chirp is marked by T and the bandwidth by BW. For a given target at range R, the receive signal has been delayed in time relative to the transmit signal by $\Delta t = \frac{2R}{c}$, where c is the speed of propagation in that medium. This delay creates a difference in the instantaneous frequency of the two signals Δf that is dependent

on the range of the target and the chirp rate k.

$$k = \frac{BW}{T} \tag{1.1}$$

$$\Delta f = k\Delta t = \frac{2Rk}{c} = \frac{2R(BW)}{cT} \tag{1.2}$$

The time-domain multiplication process of the reference transmitted signal and the received signal is usually called dechirping or deramping. This difference in frequency Δf is the difference product at the output of the mixer and forms the dechirped IF signal, $f_{IF} = \Delta f$. Other matched filters can be used and with sufficiently capable hardware the returned RF chirp can be directly captured for digital dechirping.

Expressing the range as a function of the IF yields Equation 1.3. As the transmit period and bandwidth are fixed for a single chirp, the ability to resolve range is dependent on the ability to resolve the frequency of the IF. The minimum resolvable frequency difference δf is inversely proportional to the duration of the chirp, which means the range resolution is solely dependent on the bandwidth of the chirp.

$$R = \frac{f_{IF}Tc}{2(BW)} \tag{1.3}$$

$$\delta f = \frac{1}{T} \tag{1.4}$$

$$\delta R = \frac{\delta f_{IF}Tc}{2(BW)} = \frac{c}{2(BW)} \tag{1.5}$$

This expression for range resolution works well when dealing with perfectly linear and continuous LFM signals that are transmitted for a long period with respect to the range delay Δt. When one of those conditions does not hold, the resolution is degraded, and Equation 1.5 typically acquires a scalar multiplier to represent the effect. This means that range resolution is degraded when the transmitted or received signal is windowed, when the range delay is long with respect to the chirp duration, if the chirps themselves have nonlinearities, or if the propagation speed through the

medium changes.

1.2 Thesis Overview

This work presents the design for a multichannel radar system built around the Xilinx RFSoC, covering the RF frontend, the digital processing implementation, and the antenna array design. This is broken into five chapters and an appendix. After an initial introduction in the first chapter the three following chapters each detail the different aspects of the work. A final chapter presents full-system tests evaluating the operating capabilities of the radar and lists the tasks comprising future work.

Chapter 1 provides the context surrounding this work and background information necessary to understand the rest of the material presented.

Chapter 2 describes the architecture of the new radar system and the expected operating specifications. The design process for the transmitter and receiver modules is described and measurements of each modules performance in isolation are presented. Thermal performance, power consumption, and power supply are listed as well towards the end of the chapter.

Chapter 3 outlines the design procedure for the antenna arrays used by the radar. Design steps and operating characteristics are given first for an individual element and then for the full array construction. Simulation results and measurements performed in an anechoic chamber are compared. The ability to affect array performance through dielectric loading of the antennas is investigated and more chamber measurements are compared to results from simulations.

Chapter 4 describes the design of the digital backend of the radar system. Implementation details for the various capabilities enabled by the data converters are presented along with example results. This includes things like arbitrary waveform windowing and notching, gain normalization and phase correction, active phased array operation, system calibration, and dynamic stretch processing. The results of an attempt to implement mixer product minimization are presented along with analysis as to why it was unsuccessful.

Chapter 5 presents the results of the radar operation. Operation with simulated targets using

delay lines is demonstrated and used to characterize the system in a relatively controlled manner. Full system operation with the antennas follows, first showing performance detecting a single stationary target. The target is then swept across the antenna array's field of view to test beam steering performance. A second target is added to test the ability to distinguish multiple targets during steering.

Appendix A presents images of the assembled transmitter and receiver modules along with a list of the RF components used.

Appendix B presents images of the assembled radar chassis along with specifications such as the physical dimensions and weight. A photo of the final test setup is shown as well.

Appendix C presents images of the antenna test setups in the chamber along with characterizations of external components used in the antenna tests.

Chapter 2

Multichannel Radar System Design

The design of this system is centered around improving on the functionality of the original snow radar [4], which helps set a basis for the desired minimum requirements of operation. The original snow radar was an airborne bistatic FMCW radar with a 6 GHz bandwidth centered at 5 GHz. It transmitted at no more than 23 dBm and was able to penetrate around 40 m beyond the top layer of snow. While the snow system was used as a basis, the new multichannel design differs in multiple ways. Unlike the snow radar, the new design has a lower maximum output power and would require external connectorized amplifiers to reach 23 dBm. Instead of offering a continuous 6 GHz of bandwidth a stepped chirp design is used, breaking up the bandwidth into 4 individual sub-bands, represented by the bandpass filter shown in the TX chain. Figure 2.1 provides a high level block diagram of the system design.

Eight transmit and receive channels will be present. Each channel consists of two single-board modules: one for the transmit chain and one for the receive chain. This means that there will be eight of each chain of components labeled *TX* and *RX* in Figure 2.1. Correspondingly there are two data converters for each channel: one DAC for each transmit chain and one ADC for each receive chain. These data converters are all housed inside the package of the RFSoC on a single carrier board labeled *RFSoC* in the diagram. Attached to the carrier board is another single-board module holding a synthesizer that provides the LO for the upconversion stage in all of the transmitter modules. The carrier board and synthesizer board together are responsible for controlling all aspects of the radar such as power sequencing, system configuration, and digital processing. The specifics of that functionality are described in Chapter 4. For each channel there are two antennas as well. Each transmitter module directly drives an element in the antenna array

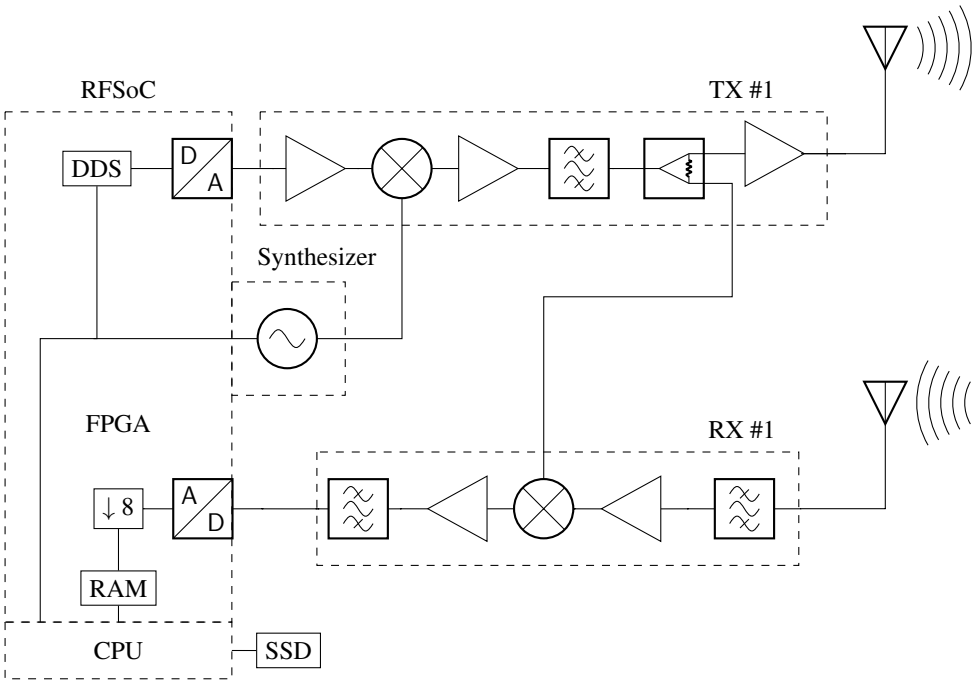

Figure 2.1: High level block diagram of radar design. Only a single transmit and receive channel is represented.

and each receiver module is directly driven by an element in the antenna array. The specifics of the antenna arrays are described in Chapter 3. This chapter discusses the design of the transmitter, receiver, and synthesizer modules.

2.1 Digital Backend Hardware

Xilinx released the Zynq UltraScale+ RFSoC (RF System on a Chip) line of products in 2018, integrating multiple high speed data converters into a single package along with programmable logic and several ARM processor cores [12]. An overview of the main features is shown in Figure 2.2. The benefits of bringing the converters into the same chip as the master FPGA are detailed in Chapter 4, but can be broadly summarized as the following improvements: reduced manufacturing complexity, lower digital implementation complexity, lower power consumption, and reduced physical size.

A development board with the ZU28DR model chip from the first generation of RFSoC released in 2018 was acquired from a third party manufacturer to investigate the performance and

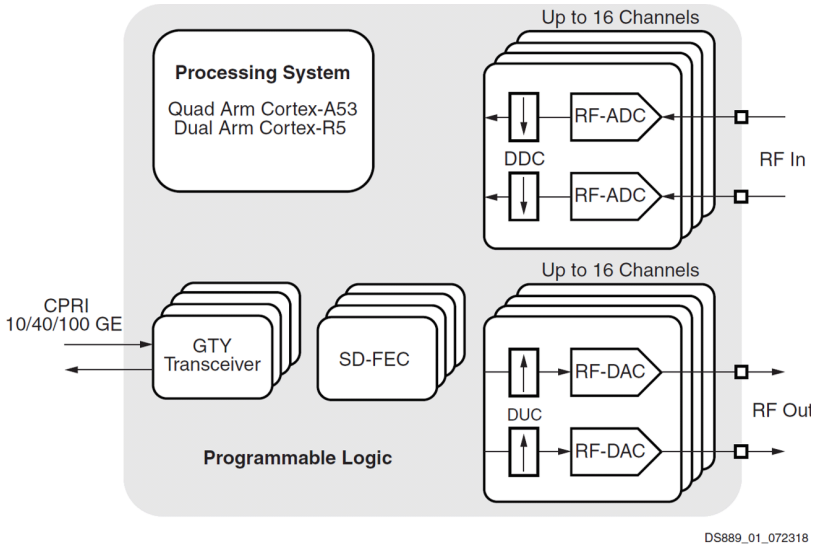

Figure 2.2: An overview of the features included in the RFSoC. Image from [1]

benefits such a device would have in the development of a radar. Sourcing from the third party manufacturer came at the cost of support among other things, but the board boasts a more compact footprint and expanded set of peripherals relative to the Xilinx reference board. The operating characteristics of the DAC and ADC modules contained in the ZU28DR RFSoC are outlined in Table 2.1.

Property	DAC	ADC
Converter Count	8	8
Max Sample Rate (GS/s)	6.554	4.096
Resolution (bits)	14	12
Interpolation/Decimation	2x, 4x, 8x	2x, 4x, 8x
Analog Bandwidth (GHz)	4	4
SFDR (dBc)	>82	>82
Channel Isolation (dBc)	-70	-70
Termination (Ω)	100	100
Full-scale Power (dBm)	1, 5	1
Absolute Maximum Input Voltage (V)	2.1	2.1

Table 2.1: Operating characteristics of RFSoC data converters [1]

2.2 Transmitter Design and Description

The digital backend of the snow radar flown during the 2018 season [7] is capable of directly producing a signal spanning the entire operating bandwidth of the radar, which means that the final conditioning consists of only a bandpass filter and amplification stage. As the DACs available in the RFSoC are not capable of operating over the desired bandwidth, a different approach must be taken. Other radars at CReSIS [4][8][6] that use a DDS with a comparatively smaller analog bandwidth rely on either a PLL based multiplier or multiple stages of discrete frequency multipliers to produce a signal with the desired bandwidth. As the multipliers and up-converters shift the frequency higher, a following down conversion stage is needed to bring the signal back into the 2-18 GHz band. There are few commercially available frequency multipliers with an input bandwidth comparable to these DACs' analog bandwidth, and use of any multiplier will introduce extra in-band signals that can be difficult to remove. On the same note, the hardware required to implement a PLL multiplier operating over such a wide bandwidth can be expensive. The corresponding down converter for both setups can also be large cost drivers in the design.

In the case of a multi-channel system, extra costs add quickly. As detailed in chapter 4, an active steering system requires precise control over the phase of the signal from individual channels. Any conditioning of the signal between the DAC and the antenna needs to be consistent and coherent across the channels to ensure a phase-aligned output at the antenna array. Meeting this requirement is accomplished most simply by using identical hardware for each channel. Any multi-channel design needs to be optimized for size and cost in order to meet the end goal of a compact system, as any increase or decrease in those parameters for the hardware of an individual channel translates out to an n-fold change, where n is the channel count.

This section presents a new compact transmitter design optimized around the multichannel digital hardware. The new design consists of eight identical transmit modules, one per DAC, and a controller board to keep the modules coherent. Each identical transmit module has a single up-conversion stage that feeds into a switched filter bank that divides the 2-8 GHz band into four over-lapping bands spanning 2.2 GHz each. The local oscillator (LO) signal used in the up-conversion is

generated by a synthesizer on the controller board that is detailed in section 2.3. Figure 2.3 shows the high level signal flow diagram for the final transmitter design with the approximate gain for each component. A comprehensive list of each component in the figure is given in Section A.2.1.

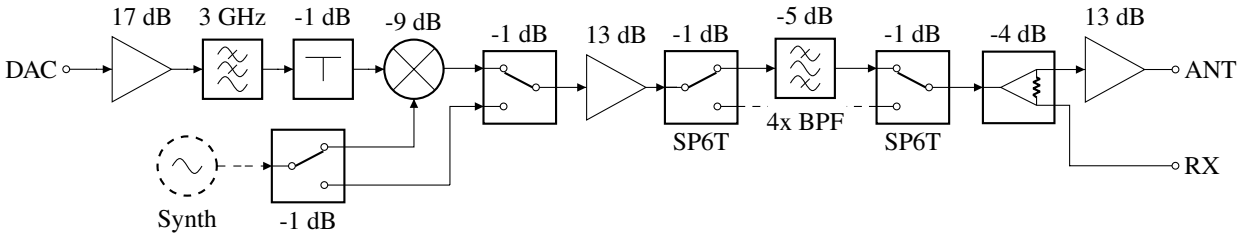

Figure 2.3: Flow diagram of transmit module

2.2.1 Transmitter IF Chain

The IF signal produced by the DAC is a chirp sweeping from 500 MHz to 2700 MHz. Various amplitude modulations are made to normalize and drop out regions for the different filter bands (see section 4.2.1), but the frequency limits are consistent. A 500 MHz gap is given between DC and the start of the chirp to provide a large enough transition region between the pass band and stop band of the filter used to cut out the LO feedthrough from the up-conversion. Below 500 MHz also happens to be where the insertion loss for the integrated balun inside the mixer starts to increase significantly [13]. A 500 MHz gap is also in place on the high side of the band as operating the DAC at 6.4 GS/s results in a Nyquist frequency of 3.2 GHz. The image then appears at 3.7 GHz, which provides 1 GHz of transition for a low-cost filter implementation to drop out the image.

The DAC blocks on the RFSoC are specified to be capable of a full-scale output power of either 1 dBm or 5 dBm depending on the supply voltage and which current mode is selected. Only the 1 dBm mode is available for use due to limitations of the carrier board. An impedance matching network and balun is placed in between the DAC terminals and the carrier off-board SSMC connector. From a simplified simulation this network should have a worst case insertion loss of 4 dB without accounting for routing and connector loss. In reality, the maximum power the DAC channels are capable of supplying off board is around -8 dBm. Post normalization this

number drops around 2 dB to -10 dBm. The mixer used has a 1 dB compression point of 15 dBm [13]. A 17 dB gain block amplifier with a low noise figure and relatively low gain roll-off is placed at the beginning of the IF chain. The reduced bandwidth requirement of the IF section means a lower cost amplifier can be used. An amplifier with a low S_{22} is desired to prevent reflections from the mixer getting back into the mixer and producing extra slightly delayed chirps, increasing the overall noise level.

A compact LTCC 3 GHz low pass filter (LPF) follows the amplifier to drop out the IF image in the second Nyquist band. In the case of DACs in the RFSoC the analog bandwidth is wide enough to allow for reasonable operation in the second Nyquist band, meaning that the analog roll-off is insufficient at curtailing the image. While operating in the second Nyquist band can be useful, in this application the image only serves to create more mixer products (see section 4.2.2). The filter chosen provides an insertion loss of at least 37 dB across 85% of the image band, and at least 20 dB over the remaining 15% [14].

The IF port is the only RF port on the mixer not buffered by an SPDT switch. The switches have an input return loss exceeding 20 dB and an insertion loss of 1 dB over the bands of interest. Inserting the switches grants an improvement in reflections relative to a direct connection between the mixer and amplifiers further down the chain. The extra insertion loss, from both the switch internals and the added routing loss, serves to attenuate potential reflections from other components as well. A wide-band, 1 dB pad is placed in front of the mixer IF port to similarly reduce reflections. The pad was chosen such that the footprint used would allow for easily changing to a pad of different value if it proved to be necessary.

2.2.2 Switched Filter Bank

The mixer used in this design, like most mixers, produces several intermodulation distortion (IMD) products that interfere with the desired signal. The mechanism behind this is covered in more detail in section 4.2.2 along with a method to reduce in-band products. That method for in-band products is implemented during the digital signal generation process and does not affect some of the out-

of-band products. Out-of band (OOB) products must be attenuated using a physical band pass filter.

The IF band defined previously is 2.2 GHz wide. Tiling that 2.2 GHz across the desired 2 GHz to 8 GHz means that the range can be covered in four bands with the necessary overlap using only two LO frequencies: 4.5 GHz and 6 GHz. The resulting bands are then the high and low sides of the up-conversion, as presented in table 2.2.

LO (GHz)	High-side (GHz)	Low-side (GHz)
4.5	5 - 7.2	1.8 - 4
6	6.5 - 8.7	3.3 - 5.5

Table 2.2: Filter band definitions

Each filter is constructed using pairs of high-pass and low-pass LTCC MMIC filters from Mini-Circuits. Premade MMIC filters were chosen for their time and cost savings. Using this stackup, microstrip filters that achieve the necessarily large fractional bandwidths would be spatially large and require tighter manufacturing tolerances. Similarly, working with discrete components for filter design at these frequencies requires accounting for all the parasitics involved in their placement and manufacturing in turn increases in complexity. The initial design of both types is also time consuming relative to working from a restricted selection of already available ICs. This restriction in available filters was influential in the selection of the two LO frequencies. The first order LO feedthrough product from the mixer is the closest and usually most powerful OOB product. Having to select the sets of filters that could transition from the pass-band to the stop-band in 500 MHz to eliminate the LO feedthrough for four different bands is the reason why there are non-uniform band overlaps of 500 MHz, 700 MHz, and 500 MHz.

Arranging the filters during the early design was carried out through a quick optimization process with simulations using manufacturer provided network parameters. Pads were placed in between certain adjacent filters to improve their impedance match.

The noticeable 9 dB roll-off is expected and is due to the compounding roll-off of the active components in the chain. High roll-off is acceptable as long as the pass-band gain remains above

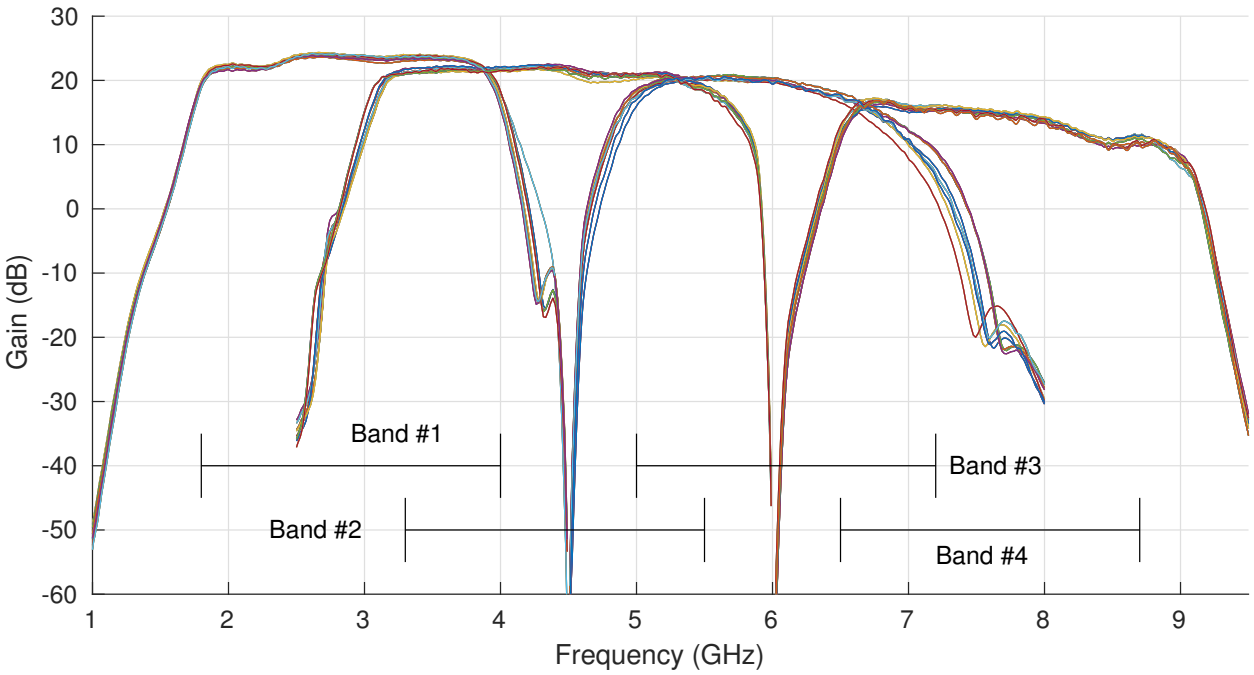

Figure 2.4: Gain of the four transmission bands of the 9 assembled transmitter boards with respect to the input sweep, as measured by a VNA at the output port intended to drive the antenna (post amplifier). The mixer LO port was driven with a 0 dBm, 4.5 GHz tone for bands 1 and 3 and a 6 GHz tone for bands 2 and 4. The IF signal was a stepped frequency sweep from 10 MHz to 3.5 GHz at a constant -10 dBm.

10 dB, which is the minimum gain required to transmit at 0 dBm given the driving power of the DAC.

In the default logic low switch state, both switches turn to a port terminated with a 50 Ω load. The terminated state serves an extra means to mute the majority of active devices in the transmitter without having to change the input signal. A passthrough channel is included as well to serve as a reference path for characterizing the devices around the filter banks without the band defined attenuation.

2.2.3 Receiver Reference Signal

The signal the receiver uses as a reference for the dechirp is expected to be identical to the transmitted signal. A 1:2 power divider is included in the transmit module to provide that reference. Since the LO port of the RX mixer does not need, and could be damaged by, the maximum power

at the transmitter output, the divider is placed in advance of the final TX gain stage. The signal routed to the receiver is around 13 dB lower than the transmitted signal and has a slightly different frequency response as it does not include the amplifier's roll-off. This means that an otherwise normalized transmit signal will appear at the receiver with a slight inverse roll-off. Fortunately the amplifier at the receive mixer's LO port means the performance of the mixer is relatively invariant to changes in the LO input power. This behavior is shown in Figure 2.5.

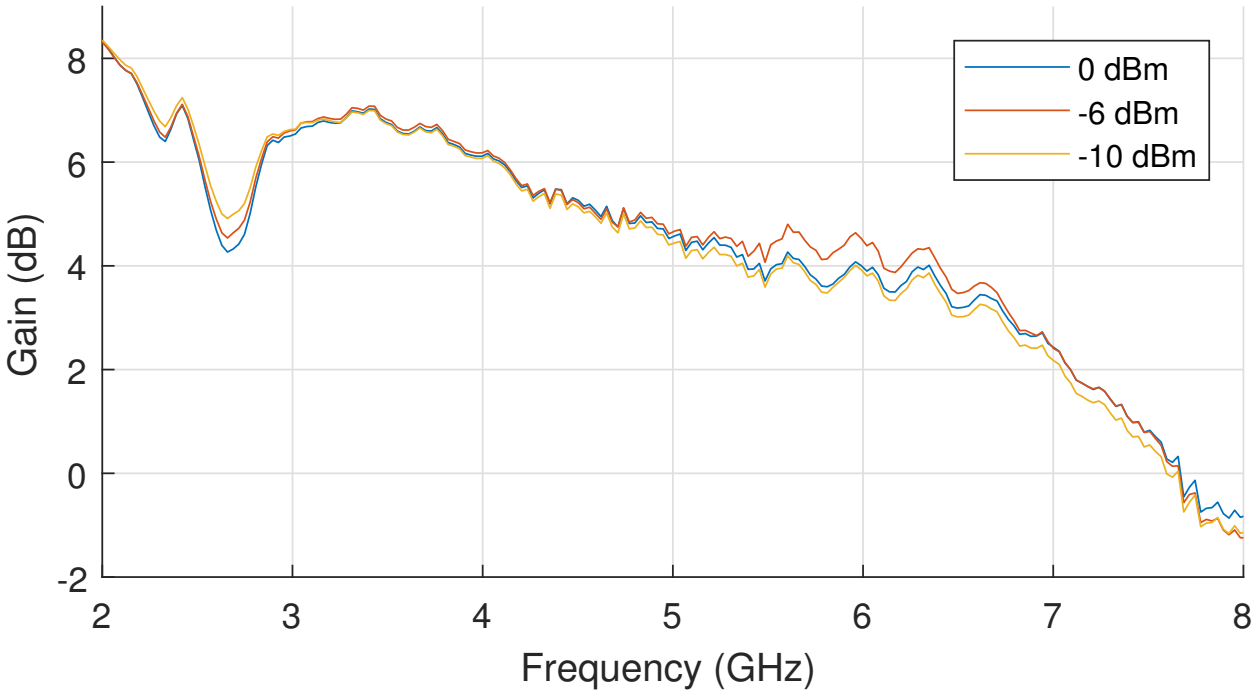

Figure 2.5: The gain of the receivers RF stage and mixer across varied levels of LO power to highlight the relatively invariant conversion loss. While constant across RF frequency, the gain from the IF stage has been approximated and subtracted out. See Figure 2.7 for the relevant component diagram.

2.2.4 Mixer Bypass

The SPDT switches sitting at the LO and RF ports of the mixer form a simple mixer bypass network. A mixer bypass feature was added to increase the potential utility of the transmit module design by allowing for operation in other radar architectures. When enabled, the signal from the LO is passed directly through to the gain blocks and filter bank. If this is used in conjunction with

an RF synthesizer capable of quickly hopping frequencies and a wide-band IQ-demodulator, a potentially low cost stepped-frequency radar could be constructed. The switched filter bank should be able to eliminate many of the harmonics that are common to some lower cost RF synthesizers and the power divider preceding the final gain block would produce the reference signal for the demodulator. The switches controlling the filter bank have sub-µs switching times[15]. Assuming that multiple frequency steps are taken inside a single band, this module should impose minimal restrictions on the maximum average frequency step-rate.

2.3 LO Generation and Digital Control

An FPGA Mezzanine Card (FMC) module was developed to provide the necessary control signals for the transmit and receive modules. The module also generates the LO signal for all of the up-converters using a single synthesizer. This module style was chosen because the only exposed connector available on the carrier board is a Vita 57.4 FMC connector.

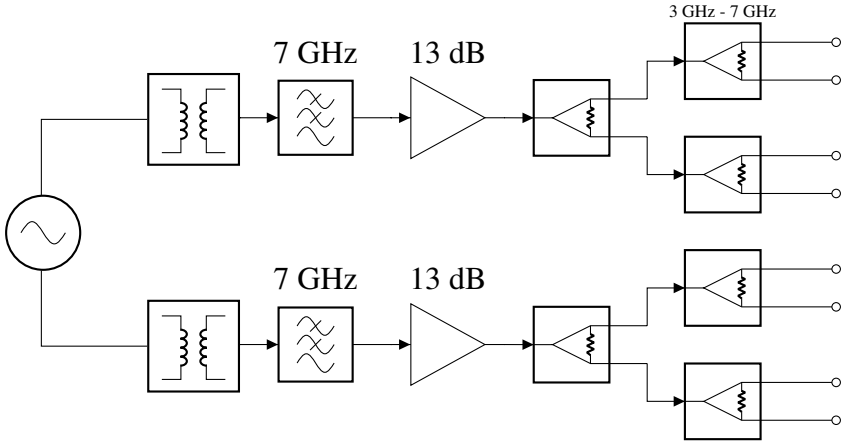

Figure 2.6: Synthesizer output chain

Figure 2.6 shows the RF conditioning chain at the outputs of the synthesizer chip. The synthesizer used is a PLL with built-in VCO that advertises low phase noise and fast PLL calibration and lock. It has two differential outputs with adjustable power up to 5 dBm. Following a balun at the output of the synthesizer the signal is passed through identical low-pass filters with a cut-off frequency of 7 GHz used to drop out the first harmonic at the lowest LO frequency: 9 GHz when

producing a 4.5 GHz tone. An amplifer is included in each chain to compensate for the 7 dB insertion loss incurred through the power splitter network. The power splitter was selected for its low phase unbalance to minimize phase error between adjacent transmit channels. The two channels of the synthesizer are phase aligned [16] so the bulk of the phase unbalance is introduced in either the splitter network or cables feeding the transmit channels.

Testing showed that the synthesizer module was capable of achieving lock in around 7 µs when the quick calibration settings were properly loaded. Since the switches on the transmit boards have a lower 10-90 RF switching time [15] the LO is only switched once during a full-bandwidth sequence of sweeps. The low and high sides of each LO are selected first before switching to the next LO frequency, resulting in the operating sequence being as follows:

1. Lock to 4.5 GHz.
2. Switch to band 1 (1.8 GHz - 4 GHz) and chirp.
3. Switch to band 3 (5 GHz - 7.2 GHz) and chirp.
4. Adjust PLL and lock to 6 GHz.
5. Switch to band 2 (3.3 GHz - 5.5 GHz) and chirp.
6. Switch to band 4 (6.5 GHz - 8.7 GHz) and chirp.

In addition to the synthesizer, the FMC module also contains multiple level translators and ribbon cable headers. The level translators are used to drive the 3.3 V logic on the transmitter boards from the 1.8 V logic on the FPGA. An additional translator is required to drive the synthesizer module as well. Extra header slots are exposed for both debugging purposes and for extending the GPIO capabilities of the carrier board for potential later additions such as external timing interfaces, other non-radar sensor control, or a GPS stream.

2.4 Receiver Design

In this work the section of the radar that performs the dechirping of the received signal and the conditioning of the IF is referred to as the receiver. FMCW radar operation allows for a straightforward receiver architecture: a mixer serves as the central component and performs the dechirping with some conditioning applied to each of the RF, LO, and IF ports.

The receiver section of the snow and wheat radars could be used in conjunction with this transmitter design, as they fully cover the bandwidth this radar is expected to operate over: both are high performance receivers that operate over 2-18 GHz. Given that bandwidth, a new low-pass filter on the RF port would be needed if those designs were to be reused in this radar as the 8-18 GHz band would only serve to raise the noise floor. In place of swapping out the band pass filter in one of those designs, a new lower cost, lower power receiver was designed and integrated into the system. Lower frequency components with smaller passbands are cheaper to acquire and reduce design constraints. Assembly time is typically reduced due to higher physical tolerances as well. The design is shown in Figure 2.7 with the associated insertion losses and filter cutoff frequencies.

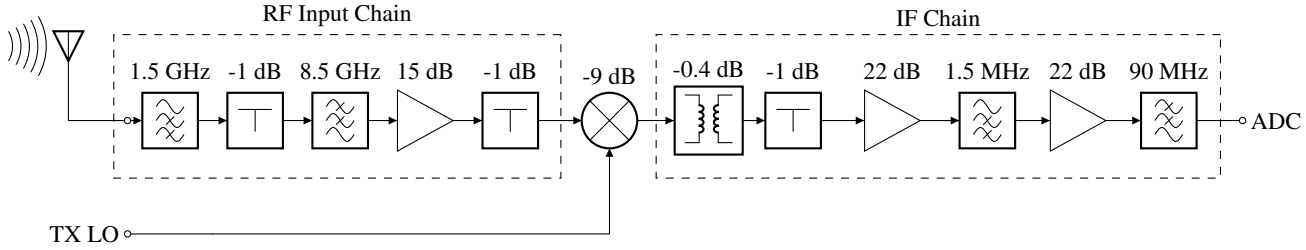

Figure 2.7: Flow diagram of receive module. All numbers in (dB) represent component gain and all numbers in (Hz) imply the cut-off frequency of the filter component.

Before finalizing and assembly this design was simulated and adjusted using ADS and manufacturer provided scattering parameters. Insertion loss from the routing was mostly ignored. From the simulations, the receiver gain in the pass band rolls off linearly from 53.2 dB at 2 GHz to 42.4 dB at 8 GHz. The estimated noise figure F_{Rx} also rolls off from 3.55 dB to 6.80 dB across the RF pass band. The estimated (thermal) noise power at the output of the receiver is given in

Equation 2.1.

$$P_n = \underbrace{F_{Rx} G_{Rx} k T_0}_{D_n} B_{IF} \tag{2.1}$$

Assuming an antenna noise temperature of $N_{ant} = -174$ dBm/Hz, a noise power density ranging from $D_n = -117.2$ dBm/Hz at 2 GHz to $D_n = -124.8$ dBm/Hz at 8 GHz can be expected. Assuming a 125 MHz IF bandwidth (using $|S_{21}| < 20$ dB as the cut-off), this works out to a total noise power around -36 dBm.

An ideal 12 bit ADC would have a maximum SNR of $6.02\text{dB} * 12 + 1.76\text{dB} = 74\text{dB}$. The 12 bit ADC has a full scale input of 1 dBm with a 100 Ω termination and a maximum noise spectral density of -147 dBFS/Hz below 240 MHz [12]. The effective IF bandwidth is 125 MHz with the FIR decimation enabled. Quantization noise power P_Q for the ADC is then $D_Q * BW = -66$ dBFS $= -65$ dBm. From section 2.2.1 the insertion loss of the balun and matching network in front of the ADC can be expected to be at least 9 dB. If a minimum quantization SNR of least 4 dB is expected then the minimum input signal power to the carrier board is -53 dBm and the maximum (full scale) input signal power is 10 dB, for a dynamic range of 63 dB.

Equation 2.2 is the calculation for the minimum discernible signal (MDS) of a system using pulse compression [17]. Pulse compressed systems introduce the compression gain G_c which is the equivalent of the time-bandwidth product of the input waveform. Pre-summing introduces the N_{presum} term which assumes multiple coherent signals will be combined digitally. N_{presum} is an integer count of the number of pre-sums performed by the system.

$$MDS = \frac{kTBF}{G_c N_{presum}} \tag{2.2}$$

Assuming a receiver temperature of 290 K, a worst case receiver noise figure of 6.8 dB, a 2.2 GHz bandwidth chirp lasting for 10 µs, an IF bandwidth B of 125 MHz, and 4 pre-sums, the receiver has a MDS of around -135 dBm. Applying the 42 dB average gain of the receiver to a -135 dBm signal results in a -93 dB signal that is 37 dB lower than the ADC limited minimum input power

to the carrier board.

2.4.1 Receiver RF Input Chain

The antennas perform moderately well over the bands of interest. Signals from outside the ideal operating bandwidth of the antennas will also be present at the output as the broadband nature of the antennas means the transition out of the usable radiating band is not sharp. A bandpass filter is needed in front of the RF port because of this. Like the transmit modules, this bandpass filter is constructed from COTS discretely packaged filters. The low pass filter is the same as the low pass filter used in the highest band of the switched filter bank in the transmitter. A multilayer organic (MLO) filter was chosen as the high pass filter. MLO packaging competes with LTCC in assembly density, as the low loss organic dielectric allows for a very dense stackup [18]. While this filter was selected in part as an evaluation and demonstration of the technology in a radar, the main selecting factors were the pass-band performance and high rejection below the cutoff. The stopband starts 150 MHz below the pass band and provides at least 44 dB of attenuation. It has a worst case insertion loss of 1.3 dB at 3.3 GHz, but for 90% of the pass band it is lower than 1 dB. At 3.3 GHz the return loss is around 7 dB which means around 20% of incident power at that frequency will be reflected back to the antennas and re-radiated. When picked up by adjacent antennas the reflections appear as extra clutter around the target, spreading out the target return. Despite this, no other COTS filter met this performance at this price point. A pad is placed in between the low and high pass filters to improve the match between them.

A LNA is included before the mixer to compensate for the bandpass filter insertion loss and conversion loss of the mixer, and to serve as a means of isolating the mixer RF port from the antennas. The LO to RF leakage in this mixer is rated as a maximum power level due to the embedded LO amplifier. At less than -25 dBm it is significantly greater than the minimum detectable signal (MDS) of the receiver [19]. The worst case inter-element coupling on the receive array is -11 dB at 2.5 GHz for immediately adjacent elements. If a -25 dBm LO-RF leakage were to pass unattenuated back to the antenna it would appear at the adjacent receiver as a -36 dBm signal, which

is significantly greater than the required MDS of the receiver. Inserting an amplifier with a low $|S_{12}|$ reduces the amount of power from the mixer making it back to the antenna. From the RF input chain simulation, the S_{12} at the worst case frequency of 2.5 GHz is -32 dB, which means the power of the signal appearing at the other receiver as previously calculated is now -68 dBm. 1 dB of padding is inserted between the amplifier and the mixer to improve the match and further attenuate reflections from the amplifier before they reach the mixer. Such reflections would result in spreading of the target spectrum. The simulated scattering parameters for the RF input chain are presented in Figure 2.8. This simulation uses manufacturer provided parameters and does not account for insertion loss from board routing.

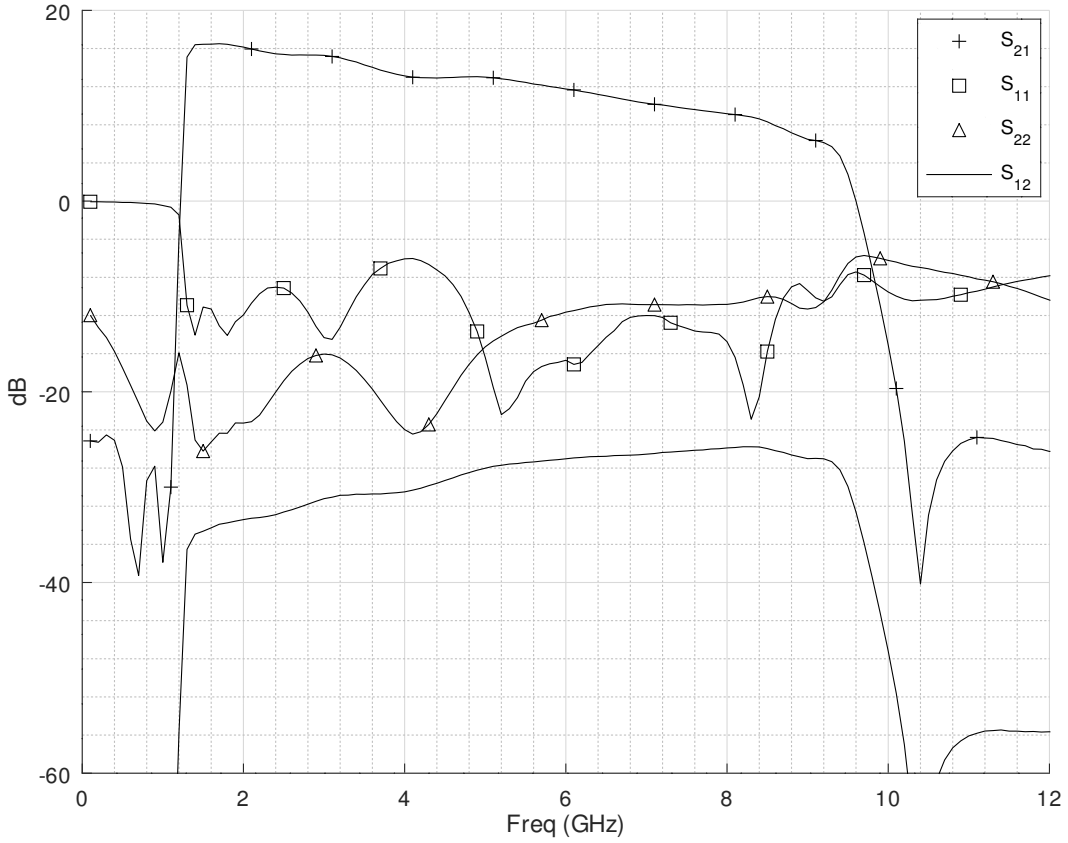

Figure 2.8: The simulated *S*-parameters for the receiver RF input chain. The markers only identify traces and do not correspond to datapoints.

The final assembly was characterized using the VNA offset frequency mode, and the final

forward gain of the assembled receiver boards is shown in Figure 2.9. The visible 9 dB roll-off is due mostly to the LNA as the mixer conversion loss only increases by 2 dB across the bandwidth. The dip at 2.8 GHz is most likely due to a mismatch between the high pass and low pass filter chain. Aside from those two issues the filters behave as desired and there is decent consistency in gain across the boards.

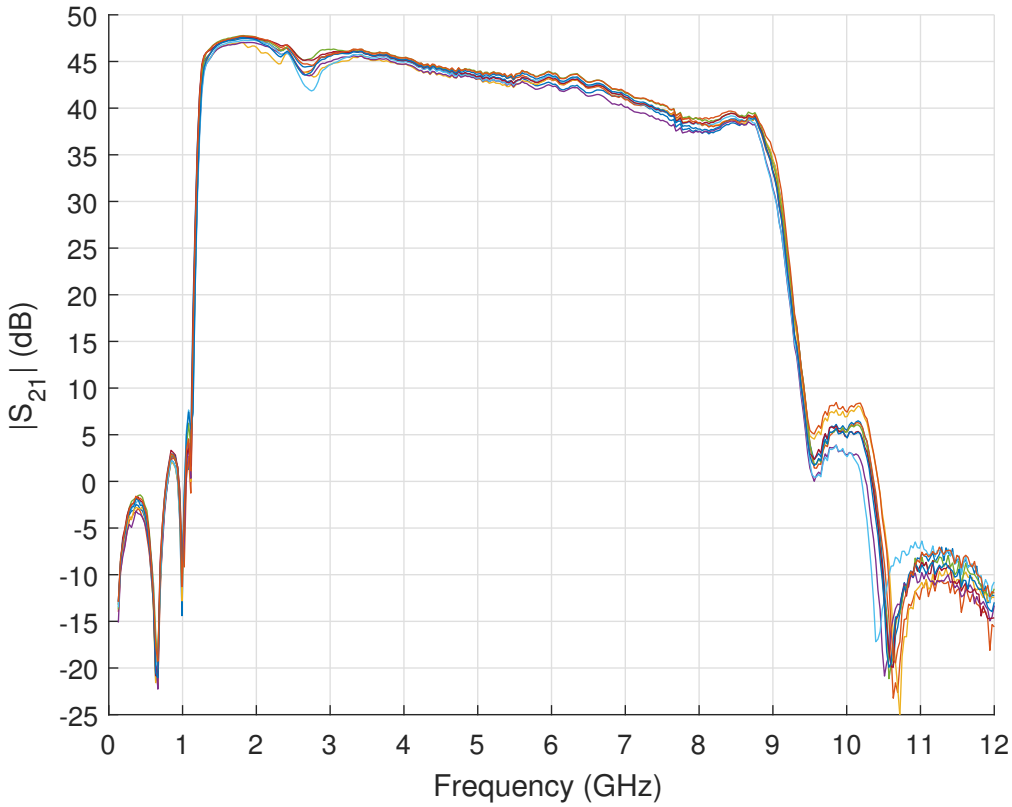

Figure 2.9: The measured gain of the receiver across 9 boards. The in-band peak at 2 GHz is 47.5 dB and the in-band minimum is 38.5 dB at 8 GHz.

The input impedance for the RF port and the IF port is shown in Figure 2.10. An acceptable return loss is seen at the RF port that improves on the expected simulated values in Figure 2.8. While plotted out to 10 GHz the IF port behavior only matters out to 250 MHz assuming out-of-band signals are sufficiently attenuated before returning to the mixer. It improves on the simulations as well and maintains >15dB return loss out to 1 GHz. The measurement stops at 10 MHz unfortunately, which means a less than ideal return loss could be visible in a valid operating region of the IF bandwidth.

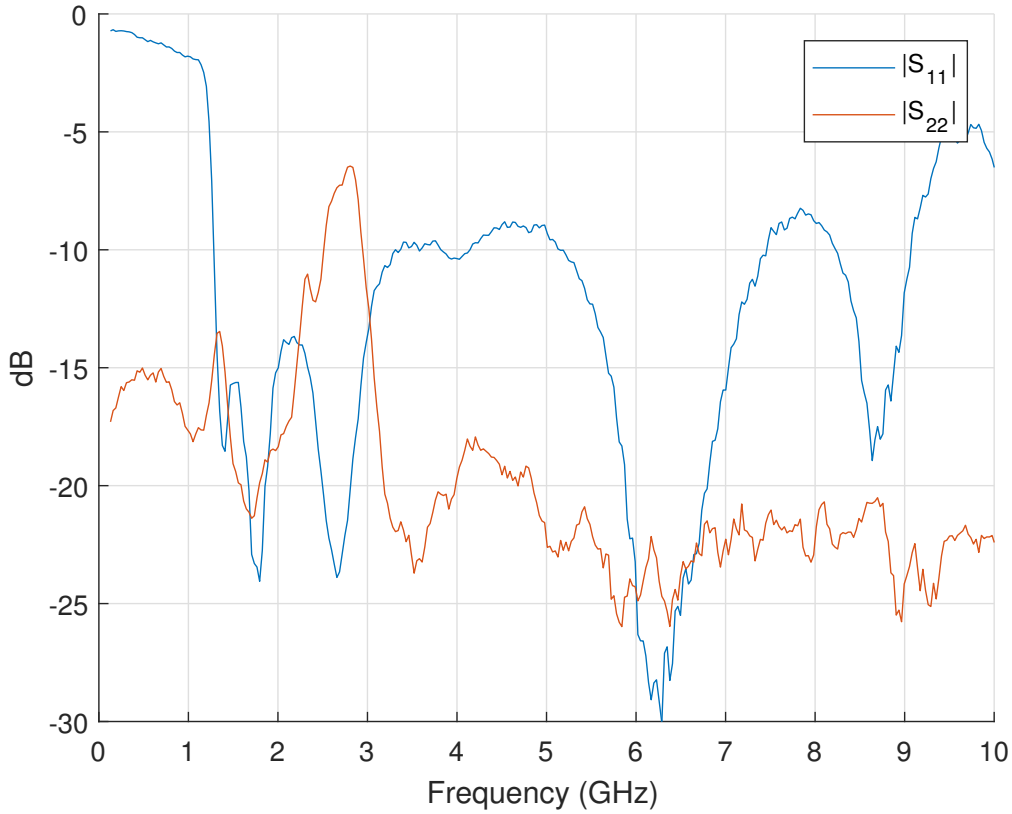

Figure 2.10: The measured input impedance for the RF and IF ports on one of the receiver boards.

2.4.2 Receiver Mixer LO Port

The reference chirp produced by the transmitter should be relatively free of OOB signals as it is already filtered by the switched filter bank. No extra filter is needed in front of the LO port of the receive mixer; nothing else is present between the off-board (SMA) connector and the LO port aside from a small matching network to block DC and improve mixer return loss. While there is an amplifier for the LO built-in to the mixer, conversion loss increases as LO power drops out of the nominal -6 dBm to 6 dBm range. The LO signal from the transmitter is designed to remain within those bounds across the bands, but insertion loss from the cable and connectors should still be considered. In 1:1 operation, where there is one receiver for every transmitter, a three and a half inch flex-rigid cable is used to connect the transmitter LO output and the receiver LO input. Knowing the length of the cable is important in establishing the reference for feedthrough interference, as discussed further in Section 2.4.3. For 2:1 operation, where there are two receivers

for every transmitter, a 2 way power divider is connected to the transmitter and receivers via six inch flex-rigid cables. The connectorized resistive power divider was selected for its low phase unbalance to reduce variations in phase between the receivers [20]. 8:1 operation uses the same divider as the one used to test the antennas described in Section C.2, but is driven by the antenna output of the transmitter in place of the LO port.

One of the largest sources of interference in an FMCW radar is feed-through that presents a shortened path to the RF input port of the dechirping mixer. Any signal that couples from the LO reference path to the RF path will present a close range false target due to the minimal time delay. This is minimized through maximizing the isolation between the RF input chain and the LO input chain on the receiver. A dense array of fencing vias was placed between the two paths on the receiver module to bring the isolation between the two above 55 dB, which is the RF-LO isolation of the mixer, the weakest link in the chain. The receiver RF-LO isolation has only been simulated using Keysight ADS and physical measurements have not been taken regarding this. Beyond the receiver module another feedthrough path exists between the transmit and receive antennas. Past airborne snow radars have achieved greater than 80 dB antenna isolation by separating the antennas several meters and encasing them in metal enclosures lined with RF absorbing tiles [6]. Such a robust setup is not feasible with a ground platform so alternative methods must be taken. Section 3.4.2 presents the isolation between the transmit and receive antenna arrays with different physical separations. The isolation is maximized, or the S_{21} is minimized, through modifications to the relative positioning of the antenna arrays.

2.4.3 Receiver IF Chain Design

In an LFM radar architecture the signal incident on the receiver from the antennas is dechirped using a reference signal generated locally, frequently sourced from the same transmitted signal. This incident signal is comprised of reflections of the transmitted signal from the various targets in the scene, along with some noise. Each reflected signal arrives at the receiver delayed by the time

required for it to travel the range (d) to the target and back:

$$t_d = \frac{2 \cdot d}{c} \tag{2.3}$$

When the received signals are mixed with the reference signal as a part of the dechirping process (the application of the matched filter) the output IF consists of tones where the frequency of each tone is directly related to the time delay and the chirp rate.

$$f_{IF} = \frac{BW_{chirp}}{T} \cdot t_d = k \cdot t_d \tag{2.4}$$

For an LFM chirp that is windowed in time, the maximum range of the system is then limited by the chirp duration T, as any reflection received after the chirp completes will have no reference to be matched with.

$$d_{max} = \frac{T \cdot c}{2} \tag{2.5}$$

The SNR for a target signal in this setup continuously decreases as the range to the target increases. This is a result of the increasing IF frequency; the overlap in time of the reference chirp and the signal from the target decreases as the time delay is increased. This assumes no stretch processing is carried out which would involve a modification to the matched filter process described previously. One example of this consists of generating a second reference chirp after the first to reduce the IF frequency for longer range targets. The received RF signal could also be directly captured, which would allow for directly applying the matched filter digitally. Both example techniques resolve the issue of range dependent SNR, but typically require either extra hardware or higher bandwidth digitizers than would otherwise be required for the architecture described above. The former technique has been tested and implemented on the snow radar deployed during the 2018 OIB season [7]. Methods for implementing both techniques with the hardware detailed in this section are described in Section 4.2.4.

Obtaining the range dependent design constraints for the IF chain requires applying Equation 2.4 to knowledge of the expected operating conditions. A radar operating at or near ground level and directed towards nadir will see close targets, with a well defined maximum range. Beyond that range it can be assumed the bulk of the response consists of off-angle clutter, multipath back scatter, and noise. As mentioned in section 2.4.2 the antenna feedthrough is a strong source of interference; the direct path from the transmit antenna to the receive antenna appears as a strong target return at the input since maintaining low antenna isolation is difficult. The IF corresponding to the feedthrough target return depends on the antenna spacing and the electrical length of the path to the antennas.

As this system is designed to be relatively compact, the antennas will be co-located with the rest of the system. For ease of handling and calculation, the transmit and receive antennas were both connected to the system using 14" (355.6 mm) flex-rigid cables with a PTFE dielectric sleeve. Assuming PTFE has a relative dielectric permittivity of $\varepsilon_r = 2.1$ the propagation speed through the cable is around 69% that of the vacuum, and the travel time for a single cable then is 1.72 ns. If the antennas are spaced 3 cm apart at the closest point and 45 cm at the farthest, then the round trip travel time for a feedthrough signal ranges from 3.54 ns to 4.94 ns. With a chirp-rate corresponding to 2 GHz in 10 µs and a zero-length reference path those times result in a feedthrough IF band of 778 kHz to 1.08 MHz for example. The reference path as implemented is a few inches long which drives the IF lower than that of the previously assumed zero-length reference path. Increasing or decreasing the length of the cable delivering the reference signal from TX to RX can be used to externally adjust the expected IF in a fashion similar to raising or lowering the chirp rate.

This system is expected to operate close to the ground, meaning targets may be present less than a meter away from the antennas. In the example given previously a 1 m target range would appear 1.47 MHz above the antenna feedthrough and a 1.5 meter target range would appear 2.2 MHz above. To attenuate the feedthrough the reference path was extended to drive the feedthrough into the stop band of a custom high pass filter. To construct the filter the coefficients were calculated for a high-pass fifth order Chebyshev filter with a 1.5 MHz 3 dB cuttoff frequency. Finding inductors

with a sufficiently high SRF that approximately met the large inductance requirements required adjusting the ideal values slightly to match what was already commercially available. Smaller inductors with a greater selection in value could be used in a high-pass filter with a greater cut-off frequency, but that would require driving the IF higher by increasing the chirp rate which would decrease the total SNR. The capacitor values were tuned accordingly in ADS and the filter was then integrated into the biasing networks of the two amplifiers. An off-the-shelf low-pass LTCC filter is placed after the final amplifier to remove clutter from beyond the maximum range and eliminate higher frequency mixer products that sit inside the analog bandwidth of the ADC.

The bulk of the gain in the receiver is placed in the IF section and not the RF front end. Lower frequency amplifiers are significantly cheaper and easier to work with. Lowering the power incident on the RF port of the mixer also has the effect of avoiding compression and increasing the power ratio of the second order products to the third order IMD products. This can be seen in Equation 4.17 in Section 4.2.2, which shows how the amplitude of the second order sum and difference products are quadratic while the third order products are cubic.

Since the IF and RF are relatively independent due to the mixer, measurement of the IF chain requires being able to generate two tones at an RF frequency and sweep their difference across the IF band. The N5222A VNA available for testing has a minimum receiver operating frequency of 10 MHz, which means an external receiver of some sort is required to characterize the low end and stop band of the IF chain. An oscilloscope was used as the external receiver and the VNA ports were manually controlled. The VNA has a single Hz tuning resolution and a power level accuracy of ± 1 dBm[21]. Configuring the VNA to output two offset CW tones, one at -45 dBm to approximate the RF return and the other at -6 dBm to drive the LO, and manually stepping one of the RF tones in frequency allows an oscilloscope to measure the power level of the IF signal. This setup serves as a rough approximation of a network analyzer with a receiver bandwidth extending down to DC. Measurements taken using this setup are shown in Figure 2.11. As the receivers in the VNA are capable of operating above 10 MHz and the roll-off on the high-pass filter is slow relative to the low-pass, the manual measurements were only taken for every 10 MHz above 10

MHz. Below 10 MHz measurements were taken every 1 MHz, and below 1.5 MHz they were taken every 100 kHz, as can be seen in Figure 2.12.

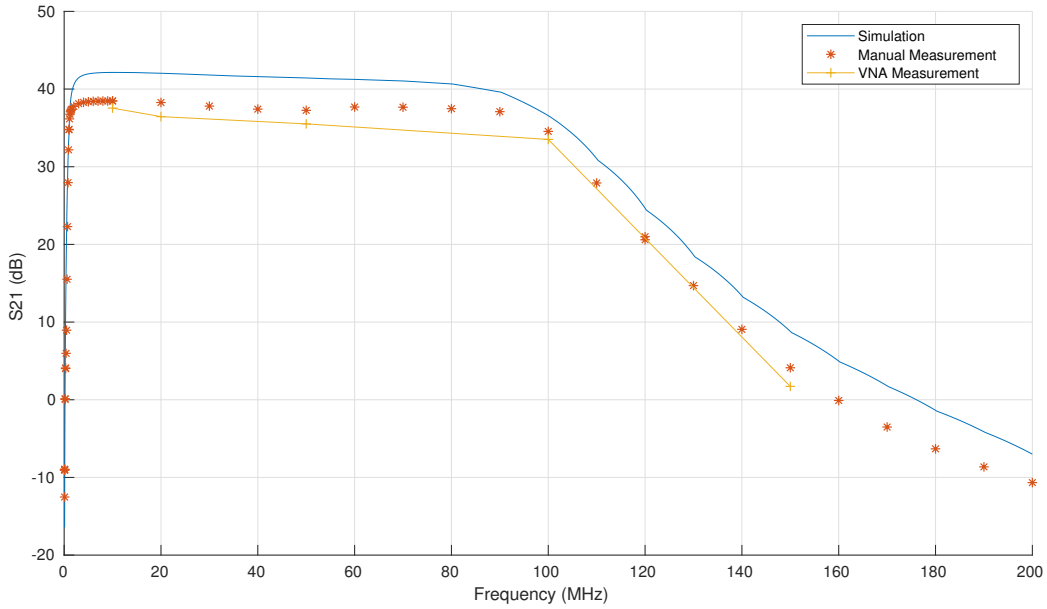

Figure 2.11: S_{21} of the receiver IF chain out to 200 MHz, as simulated and measured.

Both the manual measurements and the VNA measurements were taken with a 2 GHz tone driving the LO. The tone driving the RF port is swept from 2 GHz out to 2.2 GHz in the increments mentioned previously. 2 GHz was chosen as the gain of the RF chain can be most accurately estimated at that frequency. Manufacturer provided conversion loss for the mixer is well specified at 2 GHz, as is the gain for the LNA, the two filters, and the two attenuators. Extra insertion loss from the CPW connecting each element is lowest at 2 GHz and is simulated using ADS. This estimated gain for the RF chain is then subtracted from the oscilloscope measurements to be able to compare to the results from the IF chain simulation. The IF chain simulation includes only components following the mixer and uses de-embedded network parameters, ignoring PCB insertion loss and cable loss from the BNC cable connecting the receiver to the oscilloscope. Since the manufacturer provided network parameters are used for the amplifiers as well, the gain for each will be different depending on the tolerances of the passives used in the biasing networks for each amplifier.

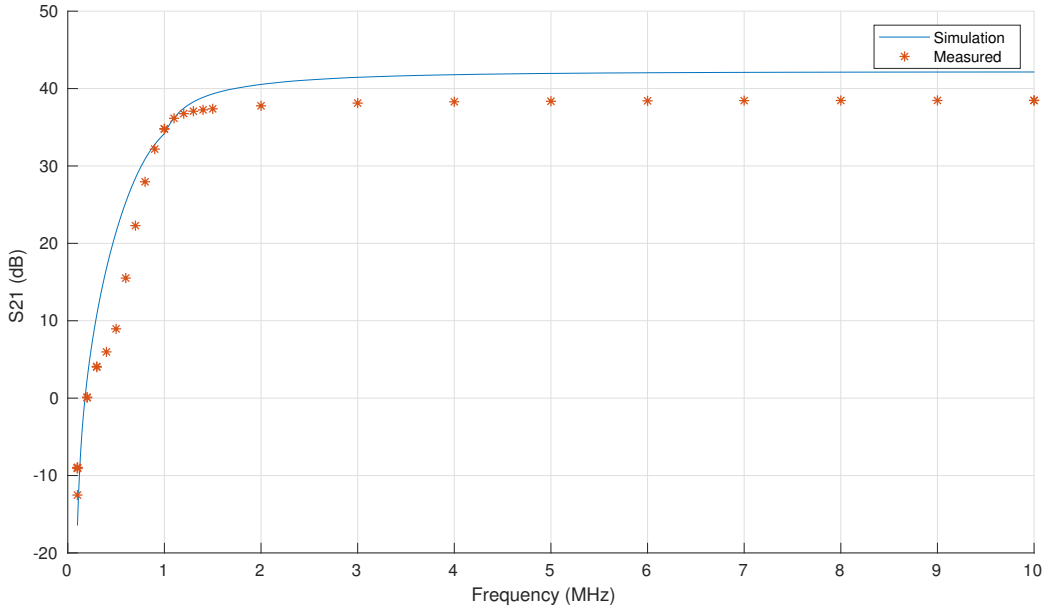

Figure 2.12: S_{21} of the receiver IF chain out to 10 MHz, as simulated and measured.

The performance of the filter as measured is acceptable. The 3-5 dB reduction in gain compared to the simulation across the majority of the pass-band is expected given the unaccounted-for embedding loss, the cable loss, and the uncalibrated manual measurements. Looking at the behavior of the high-pass filter, the 3 dB cutoff frequency is shifted down by around 300 kHz but the stop band transition is sharper from 500 kHz to 1 MHz. This is acceptable as well given the moderate tolerances of the passives used in the filter design. The behavior of the amplifiers was not otherwise characterized below 10 MHz, so some of the behavior could potentially be attributed to them. Receiver input power was -45 dBm during this test and the signal in the stopband is present at the scope input at around a couple mV, which is definitely pushing the 1 mV/div sensitivity of the scope.

2.5 System Configuration and DC Power

The system is powered by two separate power supplies: one for the digital section and one for the RF section.

A low noise soft-switching 50 W supply is used to power the transmit and receive boards. The supply outputs 6.1 V and feeds into a distribution board that breaks out into multiple connectors, one for each board. Each board has two linear regulators delivering 5 V for the amplifiers and 3.3 V for the mixers and switches. The receiver boards have automatic power sequencers to bring each component up in order while the transmitter boards rely on the carrier board to control the power sequence.

The RFSoC carrier and the synthesizer board are both powered by a recycled 500 W ATX power supply. The carrier board relies on the 12 V rail in the same way a normal PCI-e card does. The synthesizer board uses a linear regulator to bring the 5 V rail down to 3.3 V for the synthesizer and level shifters.

Under normal operation each receiver module draws around 260 mA and each transmitter module draws around 310 mA. With a 6.1 V supply that works out to around 1.59 W and 1.89 W for each receiver and transmitter respectively. All eight channels together then draw around 28 W behind the power supply. At the wall the RF section with all eight channels consumes 35 W. Dropping down to eight receive channels and two transmit channels brings the power down to 22 W. The digital section including the synthesizer draws around 52 W at the wall during normal operation.

Heat dissipation is not a significant issue; the LDOs are the greatest sources of heat on each board and reach a stable point with minimal airflow well below their rated limits. Figure 2.13 shows their 5 min temperatures without an active fan. In the final assembly airflow is directed across the modules using a 100 mm case fan.

As discussed in Section 2.2 all physical channels need to be identical for phased array operation. The cables connecting each each channel to its sources and loads all need to be of identical length. There were only enough matched-length SMA cables already on hand to route both channels to the antennas, and there were no SSMC to SMA cables available. The cables connecting the modules to the carrier board and the synthesizer board were all manually assembled using scrap cable and connectors. Doing so allowed for reducing the length of the cables to avoid slack con-

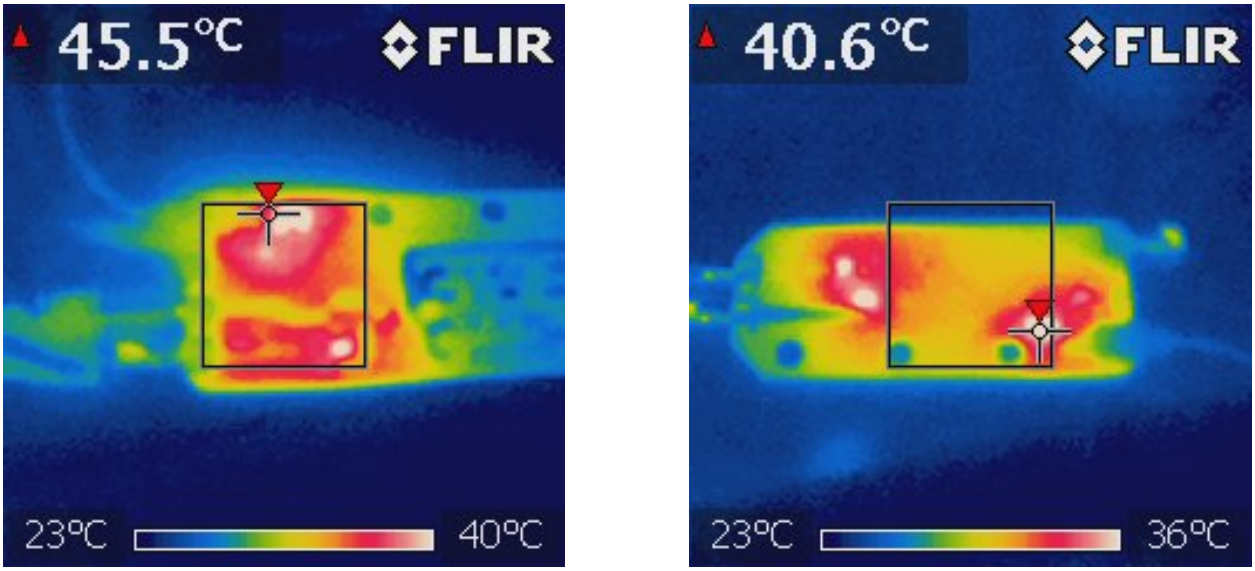

Figure 2.13: Uncalibrated IR images of the transmitter (left) and receiver (right) boards. The hottest chip is centered and the images were taken after 5 minutes of continuous operation in a 20°C room with minimal active airflow.

suming space between the carrier board and the module bank. Photos of the finished assembly can be seen in Appendix B.

Chapter 3

Antenna Array Design

3.1 Overview of Antennas in CReSIS Systems

In order for a radar to operate, an antenna of some sort is needed to radiate and receive the measured signal. The radar described in the previous sections of this document is a multichannel system that is capable of driving multiple antennas simultaneously to achieve an active electronically steered array. The snow and wheat radars currently use a pair of identical co-located horn antennas for transmit and receive [7, 8]. While the radiation characteristics of the currently used horn antennas are certainly suitable for the band this radar will operate in, they are too large to experiment with compact arrays and the cost of sourcing several of these antennas would quickly begin to dominate the total cost of this radar platform. Due to the relatively wide beamwidth, inter-element isolation is another challenge with the horn antennas that requires work to either physically attenuate the feed-through or eliminate it in processing. Past work on the antennas for the snow radar has produced arrays that perform acceptably for single channel systems, but they were not designed with the intention of beam forming and off-nadir steering [22, 23]. Several arrays have been developed with the intention of steering at CReSIS, but for lower frequency, larger, airborne systems [2]. A new antenna array has been designed to fully demonstrate the intended capabilities of this radar.

3.2 Selection of Antenna Type

As with every RF application, the most suitable antenna is defined by the expected operating conditions. In this instance the antenna will operate as a part of a wideband radar that will be

imaging ground level plants, snow, and potentially other small ground features. The entire fixture is expected to be relatively lightweight for both ease of testing and reducing load on potential future mount points. Reducing the cost of construction is important given that this will operate in an array requiring many elements. What follows is a brief overview of some of the design considerations that went into selecting the style of antenna element to be used in the array. Although the end design is a Vivaldi antenna, other antenna types were considered and explanations as to why they were not selected are presented below.

Requiring a wide usable bandwidth from a low cost design restricts the number of usable antenna styles. Of the common wideband antenna designs, only those that could be potentially manufactured on a PCB were considered.

The spiral antenna was considered early on as it is simple to produce a design with an incredibly large operating bandwidth [24]. This large operating bandwidth comes with trade offs, as the design of the antenna feed structure can become complicated and extra components may be needed to achieve a good impedance match. A side fed spiral would be needed to avoid having a perpendicular, off board feed that would increase weight and mounting complexity. Spiral antennas radiate antipodally, directing half of the radiation upwards away from the target. Inserting a cavity backing to correct that prevents wideband operation [25, 26, 27]. The spiral antenna is also circularly polarized and the returns from targets would differ from the linearly polarized interactions measured by the previous radar platforms this system is intended to be benchmarked against [28].

There are several UWB planar monopole designs that meet the bandwidth and size requirements [29, 30, 31, 32, 33, 34, 35, 36]. Most of these rely on multiple modes of radiation to cover the entire band, which depending on the mode can cause the main lobe direction and polarization to change across the bandwidth. The directivity is relatively low as well making it harder to eliminate rear-fire targets.

The Vivaldi antenna, or exponentially tapered slot antenna, serves as probably the closest planar analog to the horn antennas currently in use. Unlike the previously mentioned designs, a well

designed Vivaldi can have relatively high gain with a single end-fire main lobe centered in both azimuth and elevation across the operating bandwidth. The mechanism of radiation also inherently maintains a constant polarization across the band. It is a planar, traveling wave design that was first described in 1979 [37]. The basic structure shown in Figure 3.1 consists of a slot-line feed with a conductor-to-conductor separation that exponentially expands along the length of the slot line, effectively matching the slot line modes to modes radiating in free space. Tapered slot line antennas can be formed with geometries other than the exponential taper such as elliptical, linear, or radial tapers, but the Vivaldi classification is reserved for an exponential taper.

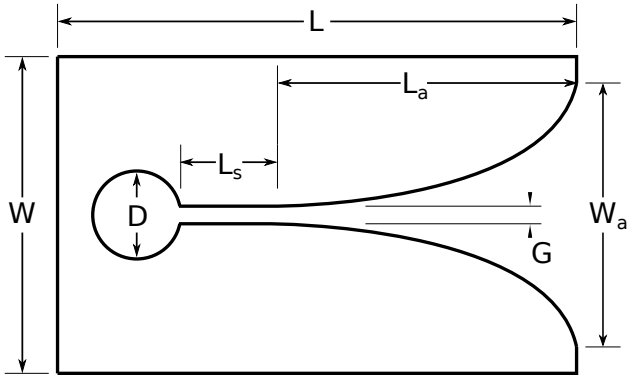

Figure 3.1: Basic Vivaldi outline with characteristic dimensions labeled.

3.3 Single Element Performance Tuning

There is a large volume of previous work on compact Vivaldi antennas operating near this band due to the FCC indoor UWB allocation from 3.1 to 10.6 GHz [38, 39, 40, 41]. This radar is expected to operate down to 2 GHz, extending below the FCC UWB allocation. [42] succeeds in obtaining the desired 6 GHz bandwidth, but comes in significantly larger than the other "compact" antennas at close to a foot in length along the E-plane. [43] presents a design that meets both the bandwidth and size requirements, but depends on an expensive substrate with a high dielectric constant ($\varepsilon_r = 10.2$), a liquid dielectric immersion, and electrical features smaller than what the available PCB mill (LPKF S103) is capable of.

Ideally the antenna would be as compact as possible to allow for reduced weight, greater flex-

ibility in relative positioning, and minimum cost. The approach taken in this work was to expand on the designs cited previously in the pursuit of extending the effective bandwidth to below 2 GHz while maintaining a compact form factor and low cost to design.

The dimensions of the final design are listed in Table 3.1.

Dimension	Value (mm)	Description
W	40	Total width of element
L	45	Total length of element
L_s	5	Length of linear slot line section
L_a	30	Length of exponential taper (aperture)
W_a	40	Width of aperture
D	8	Diameter of cavity
G	0.5	Slot line gap width

Table 3.1: Dimensions of Vivaldi antenna element.

While not a truly electrically small antenna, it does push below the general rule of thumb that the aperture width of the Vivaldi, the separation of the two halves of the taper at its greatest point, not drop below half the largest wavelength [44, 38]. In this design it stays above $\frac{\lambda}{4}$, but the physical size is one of the main factors affecting the beamwidth around 2 GHz [45].

There are four main components to the antenna: the microstrip feed and transition, the slot line and cavity, the exponential taper, and the mounting structure. Each component was simulated and optimized using the Ansys HFSS software suite. The following subsections review general parameters of the design and how they affect the performance of the antenna.

3.3.0.1 Microstrip Feed

The slot line feeding the taper is driven by a microstrip line through a coupling balun. The microstrip line in turn is driven by an edge-launch SMA connector. There are various possible designs for the microstrip/slot line balun such as the direct short, or virtually opened stubs, or fan stubs [46].

From [47], an approximate expression for determining microstrip line impedance from its phys-

ical dimensions is shown in Equation 3.1.

$$Z_0 \approx \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \tag{3.1}$$

$$\varepsilon_r = \text{Substrate relative permittivity}$$

$$h = \text{Substrate thickness (mils)}$$

$$w = \text{Microstrip line width (mils)}$$

$$t = \text{Microstrip line conductor thickness (mils)}$$

If a fixed impedance of 50 Ω is assumed and the substrate permittivity, thickness, and conductor thickness are inserted for the available panel, then the width of a 50 Ω microstrip line can be calculated. For the panel used that works out to approximately 116 mils, or 2.95 mm. Given the short length of slot line and small gap width, the width of the microstrip line at the crossing is reduced to 2 mm to reduce the transition insertion loss. This drop is moderated using a linear taper extending from the SMA connector mount point.

A stub fan balun was arrived at through a quick testing of alternatives. The sector shape was chosen over a circular stub due to the quality of match seen during initial test simulations. The radius and span of the sector was arrived at through optimization in HFSS.

The end balun design can be seen in Figure 3.2 on the right element.

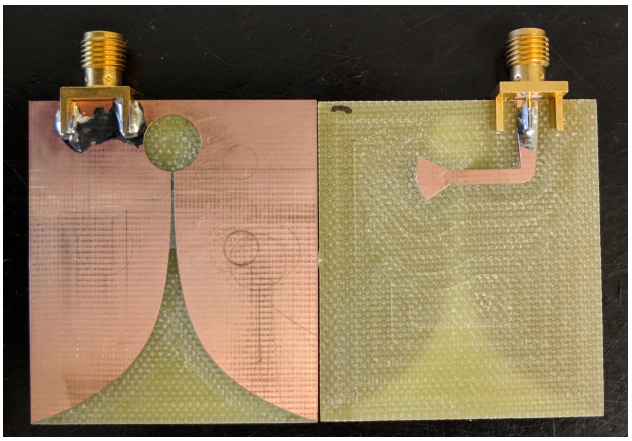

Figure 3.2: The final Vivaldi design with no mounting structure. Left shows the slot line and taper aperture and the right shows the microstrip and SMA connector feed on the opposite side.

3.3.0.2 Slot line and Taper

The exponential taper characteristic of Vivaldi antennas directly affects the radiating characteristics of the antenna, such as the gain, main lobe beamwidth, and the slot line match. The length, width, and taper-rate parameters all change the expected behavior. From [45, 48, 49], increasing the taper rate improves the return loss at lower operating frequencies. [49] also shows that increasing the aperture length improves return loss at lower frequencies as well. [50] shows that a decrease in the taper rate increases the 3 dB beamwidth. For a fixed length antenna, a decreased taper rate would imply a shortened aperture height, which makes sense when considering the previous assumption from [37] that a longer Vivaldi section will have smaller beamwidth. Equation 3.2 shows how the parameters listed in Table 3.1 define the shape of the exponential taper.

$$y(x) = \frac{G}{2} e^{x\left(\frac{1}{L_a}\right)\ln\left(\frac{W_a}{G}\right)} \tag{3.2}$$

The slot line length and size of cavity stub also affect the performance at the lower end of the bandwidth; increasing both can lead to improved performance [49]. A larger slot line stub can increase the resistance leading to a closer match and a longer linear slot line section can tighten the width of the main lobe. Although for a Vivaldi with limited depth, increasing the diameter of the slot line stub too much can increase the inductance of the short between the two halves of the slot line.

3.3.0.3 Mounting Structure

Obtaining consistent, repeatable measurements requires fixing the position of the antenna to avoid undesired variations. A mount point was formed by adding an extra 23 mm x 23 mm square tab of bare FR4 behind the slotline stub alongside the SMA connector. Holes were drilled at the far end for attaching L-brackets, but the tab itself could be clamped to or pushed into a receptacle for an interference fit.

These antennas are not perfectly end-fire; there are lobes directed toward the rear. This means

that objects placed behind the antennas will be illuminated in addition to the desired targets in front of the antennas. Assuming the objects behind the antenna are closer than the intended forward target their directly scattered responses can be discriminated by their range response. If they are static with respect to the antenna position then their response can be subtracted out with a sufficient number of samples. Near object reflections can be comparatively strong, which increases noise at the receiver as well. The main concern however is not from the direct single scattering of the rear objects, but the bistatic and multistatic scattering resulting from them. This is represented in Figure 3.3 along the clutter bistatic scatter path. A multistatic scatter path would also be present, adding an extra leg on the bistatic path to indicate a second interaction with the clutter.

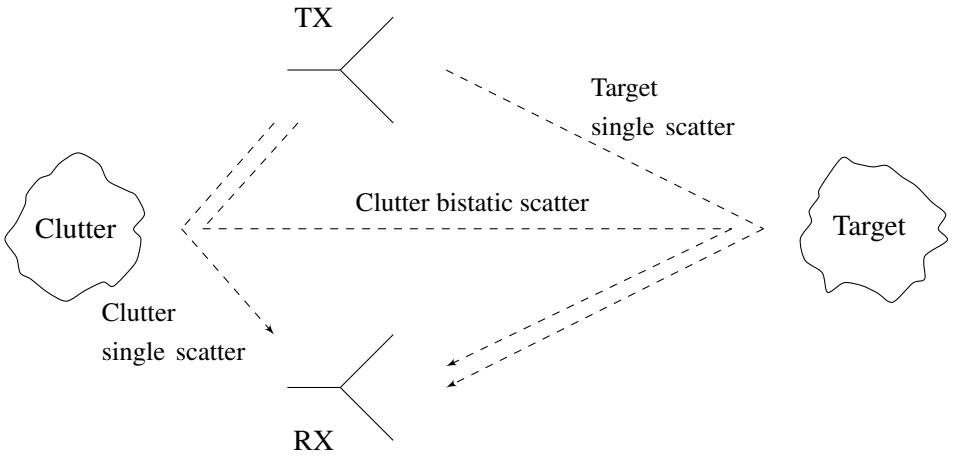

Figure 3.3: Scatter resulting from rear positioned clutter.

In the case of the mounting structure of the antennas, the bistatic scatter from the mounting structure would form range sidelobes on both sides of the target response assuming symmetric structures for TX and RX. These sidelobes would be proportional to the mounting structure backscatter. To minimize the sidelobes the structure should be designed to have minimal reflection. From simulations and quick measurements with different base plate materials, a solid aluminum mounting rail had a return 9 dB stronger than an acrylic rail. The simulation also indicated that the presence of the aluminum mounting brackets had a marginal effect on the response from the structure regardless of rail material so they were used in all further measurements. To further minimize the structure response RF absorbing material could be placed directly in between the structure and

the elements, but the 2 cm clearance afforded by the mounting tab and L-bracket would force the absorber too close and load the antennas.

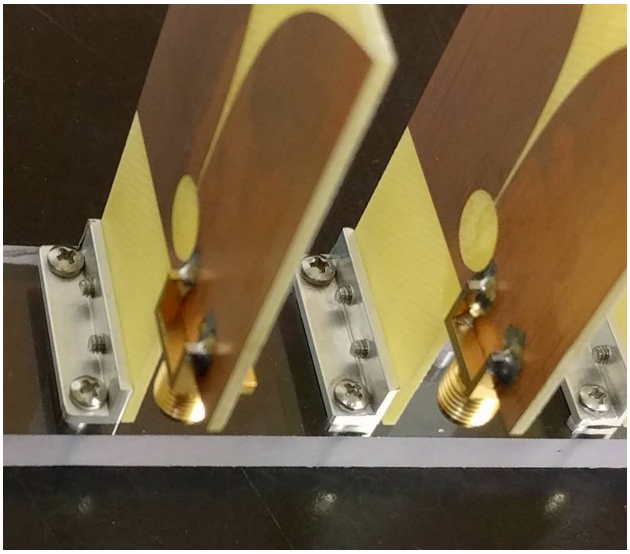

Figure 3.4: The final antenna element design attached to the mounting structure with an aluminum bracket.

Figure 3.4 shows the an offset profile view of the tab and L-bracket as a part of the array with an acrylic mounting rail.

3.3.1 Measurements

The following figures characterize the antenna using results from simulations and from measurements the anechoic chamber.The equipment setup and antenna mounting structure used to take measurements inside the chamber is detailed in Appendix C.2.

Table 3.2 gives figures describing antenna performance as simulated by HFSS. Looking at the results, the antenna is mostly useless at 1 GHz, with a poor directivity and efficiency. The main usable band extends from 3 GHz to 9 GHz, with efficiency slowly rolling off. This can also be seen in Figure 3.5, where the return loss first exceeds 10 dB at 2.4 GHz. While not visible in the plots or table, the efficiency quickly drops off beyond 9 GHz.

Freq (GHz)	dB[Directivity]	dB[Peak Gain]	dB[Realized Gain]	Beam Area	Efficiency
1	-7.768	-9.083	-12.836	75.173	0.739
2	0.293	-0.604	-4.603	11.747	0.814
3	2.660	2.246	1.901	6.811	0.909
4	3.665	3.095	2.654	5.403	0.877
5	4.689	4.089	4.046	4.270	0.871
6	7.000	6.289	6.141	2.507	0.849
7	7.340	6.473	6.375	2.318	0.819
8	7.293	6.327	6.280	2.344	0.801
9	7.844	6.543	6.431	2.064	0.741

Table 3.2: Simulated antenna performance characteristics.

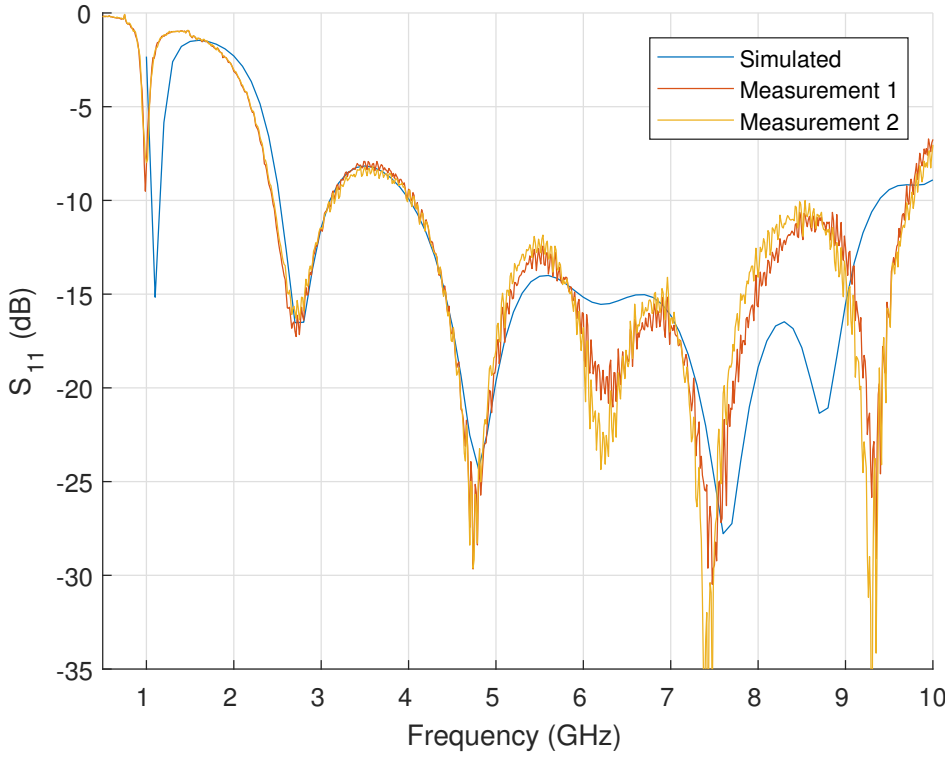

Figure 3.5: The S_{11} parameter of the antenna, as measured in the anechoic chamber and simulated. Cable loss has been calibrated out

The nulls in the measured and simulated return losses mostly line up, but the measured results seem to stretch outwards around the center band. In comparison to the simulation, actual performance is comparatively degraded beyond 7 GHz, most likely due to the substrate used and performance of the SMA-to-microstrip transition and microstrip itself.

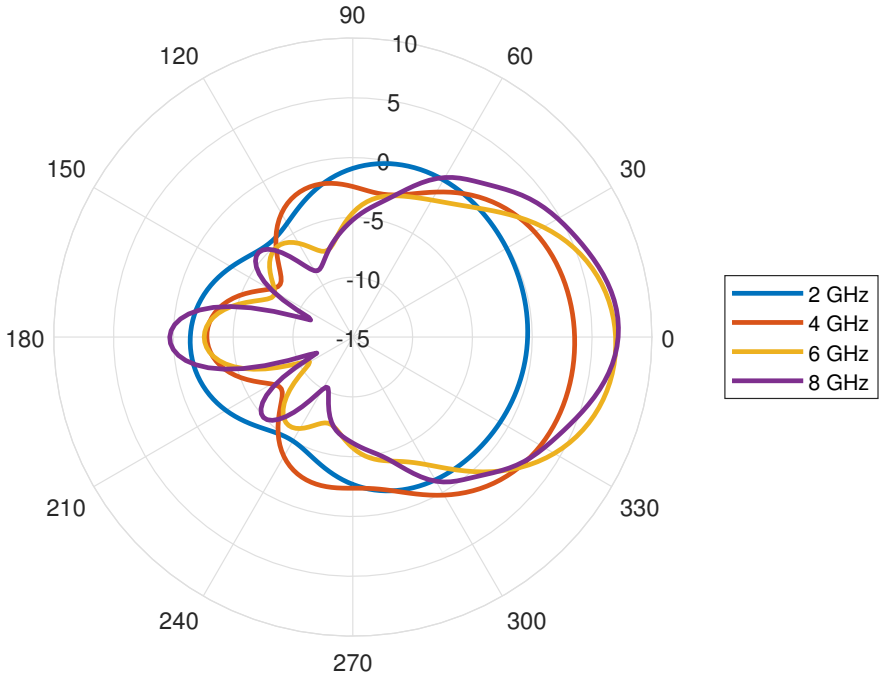

Figure 3.6: The simulated elevation sweep of the directive gain (dBi) of an antenna element. The antenna would be coplanar with this plot and oriented such that the end-fire direction vector is pointing at 0°.

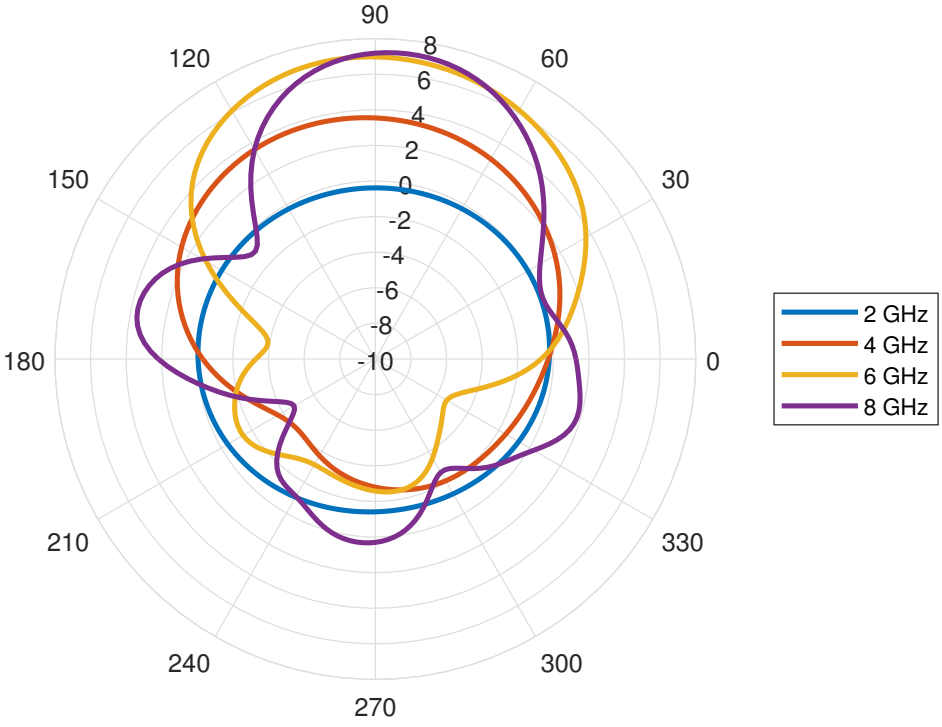

Figure 3.7: The simulated azimuth sweep of the directive gain (dBi) of an antenna element. The antenna is oriented such that the main lobe (end-fire direction) is pointing at 90°.

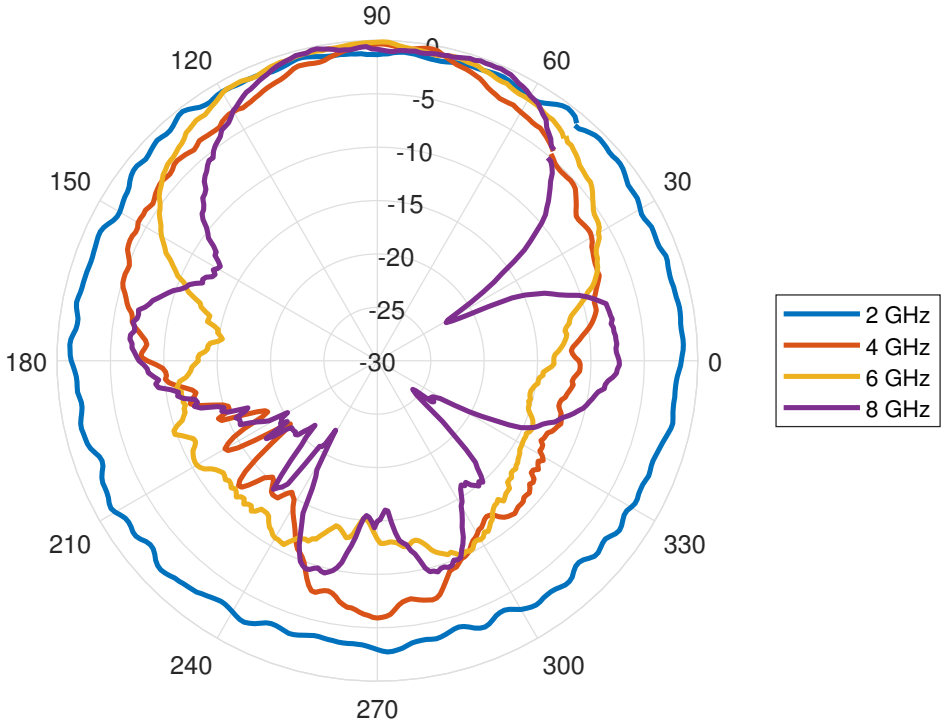

Figure 3.8: The azimuth sweep of the radiation pattern measured in an anechoic chamber. This is a relative measurement where the transmit and receive ratio is expressed in dB and then normalized such that the maximum ratio is unity.

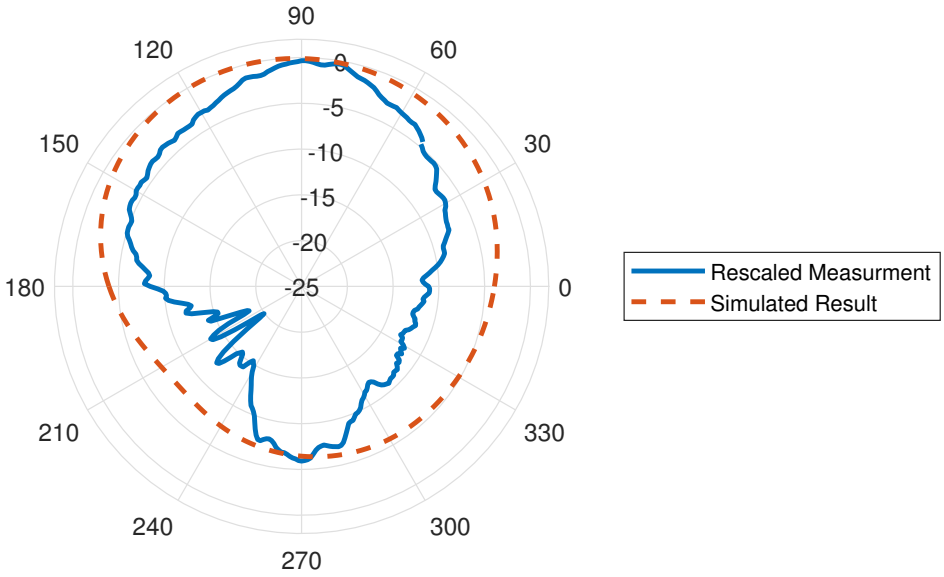

Figure 3.9: A comparison between the measured radiation pattern and simulated directive gain pattern at 4 GHz. The simulated directive gain pattern has been normalized to have equal directivity with the measured pattern.

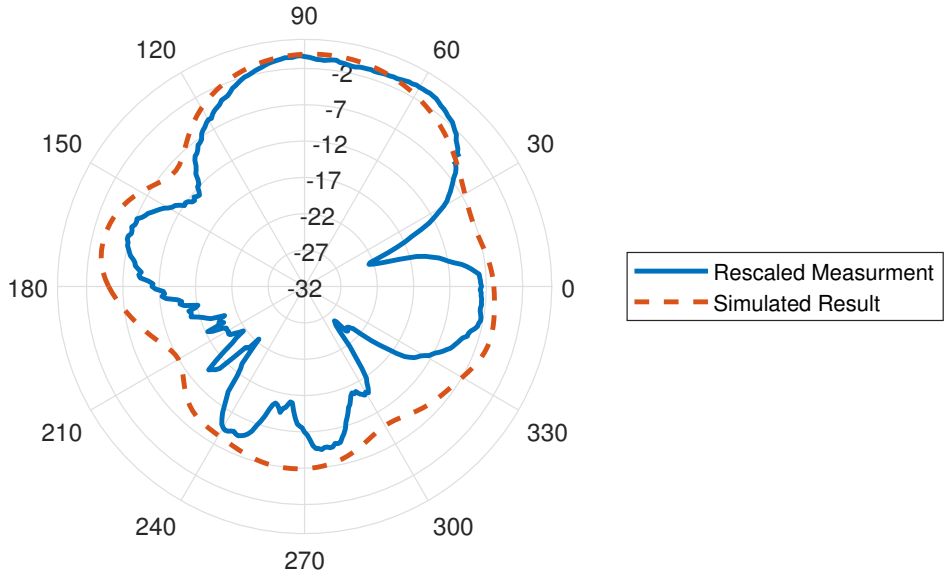

Figure 3.10: A comparison between the measured radiation pattern and simulated directive gain pattern at 8 GHz. The simulated directive gain pattern has been normalized to have equal directivity with the measured pattern.

In both Figure 3.9 and 3.10 the simulated patterns have greater directive gain than the measurements across most of the azimuth. The main lobe and back lobes are preserved however. While this could be due to variations in the measurement setup such as the variations in the antenna position, it is more likely due to the transition and microstrip line previously discussed as affecting the return loss.

3.4 Array Construction

With any antenna array the relative position, orientation, weighting, and phase of each element affect the behavior and eventual performance of the array. This array is intended to demonstrate the radar's ability to electronically steer the beam, so decent directivity and minimal grating lobes when operating as a phased array are the key metrics for evaluating array performance. With the typical ground target scene setup and sufficient back-lobe absorption, grating lobes that are at great enough angles can be ignored as any target there can range-gated out.

With Vivaldi antennas element there are two common arrangements one can use to construct a single-polarization array: coplanar in the E-plane and coplanar in the H-plane. In any practical

array implementation the elements will experience mutual coupling as each radiating element interacts with every other radiating element. From [49, 51, 23] it can be seen that mutual coupling can have significant effects on array parameters, namely the input impedance of each element and the total radiation pattern. [49] shows that Vivaldi arrays arranged coplanar in the E-plane with inter-element electrical contact have relatively high mutual coupling compared to H-plane arrays. From some simulations set up in HFSS to verify this it was also observed that E-plane arrays with electrical contact had higher mutual coupling than detached E-plane arrays as well. Those same simulations showed that an E-plane array formed with the design described in 3.3 had improved return loss over an H-plane array with equivalent spacing. Figure 3.11 shows how significant the effect is.

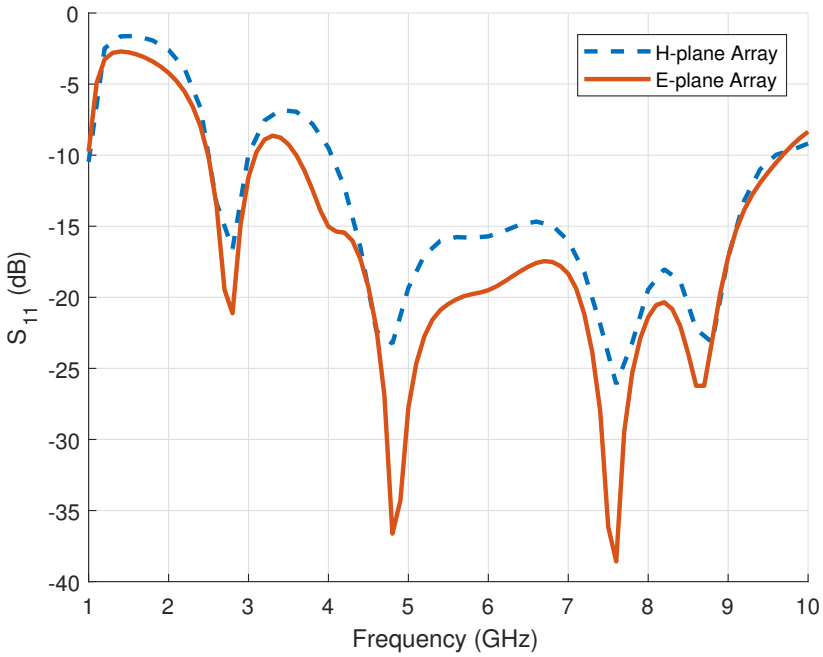

Figure 3.11: The S_{11} parameter of an E-plane and H-plane array of the Vivaldi design as simulated in HFSS with uniform phase and amplitude. The physical spacing between phase centers for both arrays is 40 cm.

An E-plane array also lacks flexibility in the relative arrangement of array elements. The entire array exists on a single continuous panel, requiring new arrays to be milled in order to test out different spacing. There is a greater limitation on the range of spacing achievable as well since the tightest element spacing possible is restricted to the E-plane width of each element. Having

the ability to test different spacing is important in this array in order to investigate phased array performance. For this reason an H-plane array configuration is used.

As mentioned previously, an H-plane array has lower net mutual coupling than a connected E-plane configuration which means that the elements in an H-plane array will have behavior more closely matching that of an individual isolated element. This is intensified as the element spacing is increased, which decreases coupling [49]. Increasing the distance between elements too far obviously will create grating lobes, and reducing the distance broadens the main lobe, increasing the 3 dB beamwidth. The main lobe beam area listed in Table 3.2 shows how the individual element main lobe shrinks with increasing frequency, behavior which applies to the array as well. Since the phase center of a Vivaldi antenna shifts with frequency one could imagine an array of Vivaldis that control their taper and flare in the H-plane to achieve a more consistent beamwidth across the bandwidth, but the manufacturing requirements for such a setup would be prohibitive. Most measurements were taken with a 3 cm element spacing as simulations showed minimal interference from grating lobes out to 30° off axis steering with that spacing.

3.4.1 Array Measurements

Table 3.3 shows the performance figures for the simulated array to be compared against those in Table 3.2. Exemplifying the array mutual coupling, the efficiency is increased in the array configuration across the bandwidth. Gain scales with the array factor and efficiency, as expected.

Freq (GHz)	dB[Directivity]	dB[Peak Gain]	dB[Peak Realized Gain]	Efficiency
1	0.924	0.793	0.775	0.858
2	5.250	4.497	2.142	0.856
3	9.723	8.934	8.788	0.919
4	15.985	14.217	12.970	0.889
5	24.584	21.820	21.799	0.888
6	35.497	30.830	30.4225	0.869
7	45.658	37.508	36.632	0.822
8	46.893	37.602	37.086	0.801
9	31.469	23.239	22.305	0.738

Table 3.3: Simulated antenna array performance characteristics.

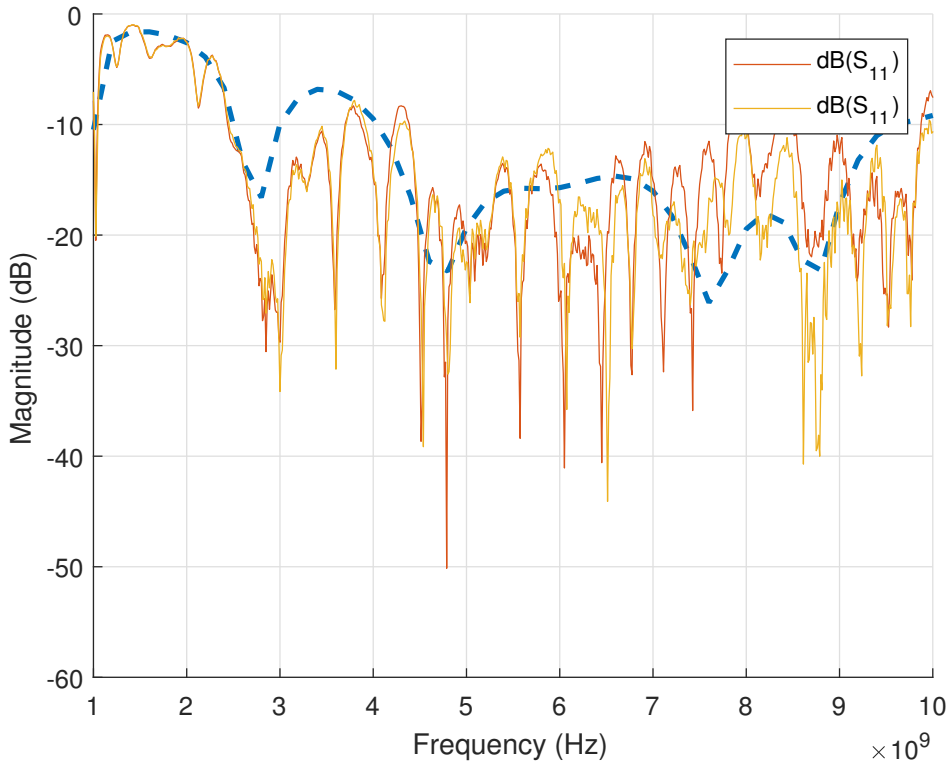

Figure 3.12: The S_{11} parameter of the two H-plane arrays compared against the simulated values. The arrays are measured from behind a 1:8 resistive power divider.

The measured $|S_{11}|$ in Figure 3.12 shows improved performance in the lower band (<3.5 GHz) and degraded performance above 6.5 GHz. This could be due to the presence of the 1:8 divider used or the cables feeding the antennas. The return loss for the divider is shown in Figure D.3.

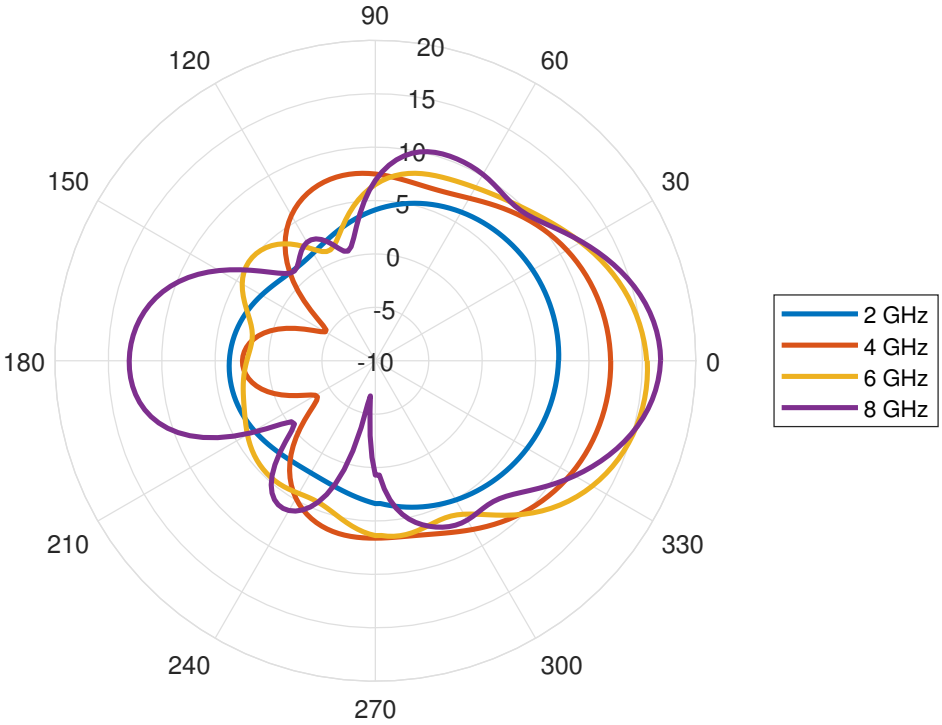

Figure 3.13: The simulated elevation cut of the directive gain pattern (dBi) of an H-plane antenna array with 3 cm element separation. $\phi = 0$

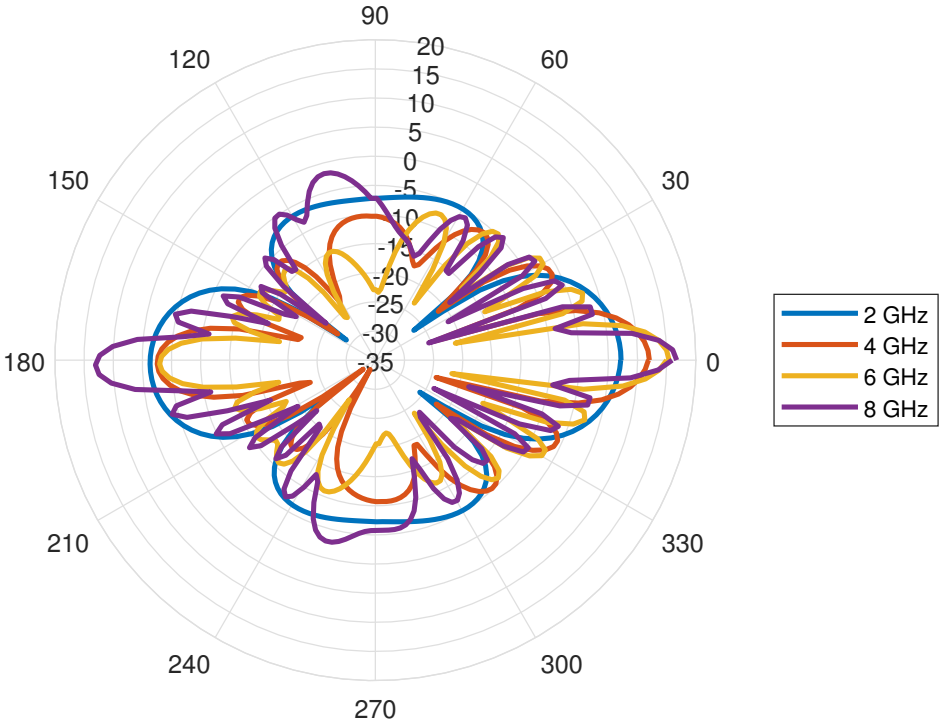

Figure 3.14: The simulated azimuth cut of the directive gain pattern (dBi) of an H-plane antenna array with 3 cm element separation. $\theta = 0$

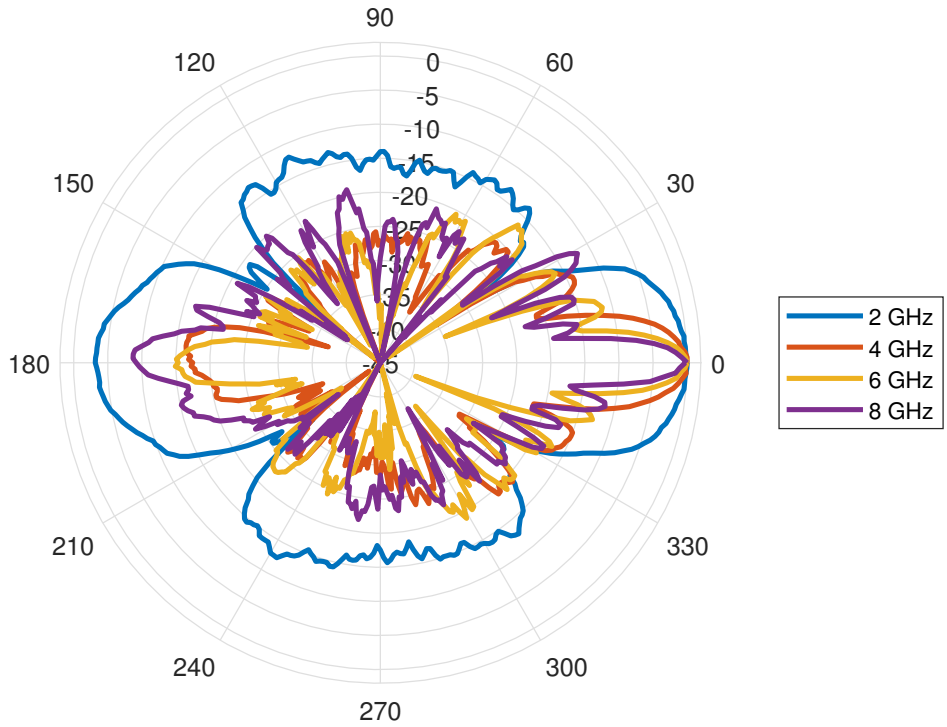

Figure 3.15: The measured azimuth radiation pattern of a 3 cm H-plane array. This is a relative measurement where the pattern is normalized so the maximum across frequencies is always unity.

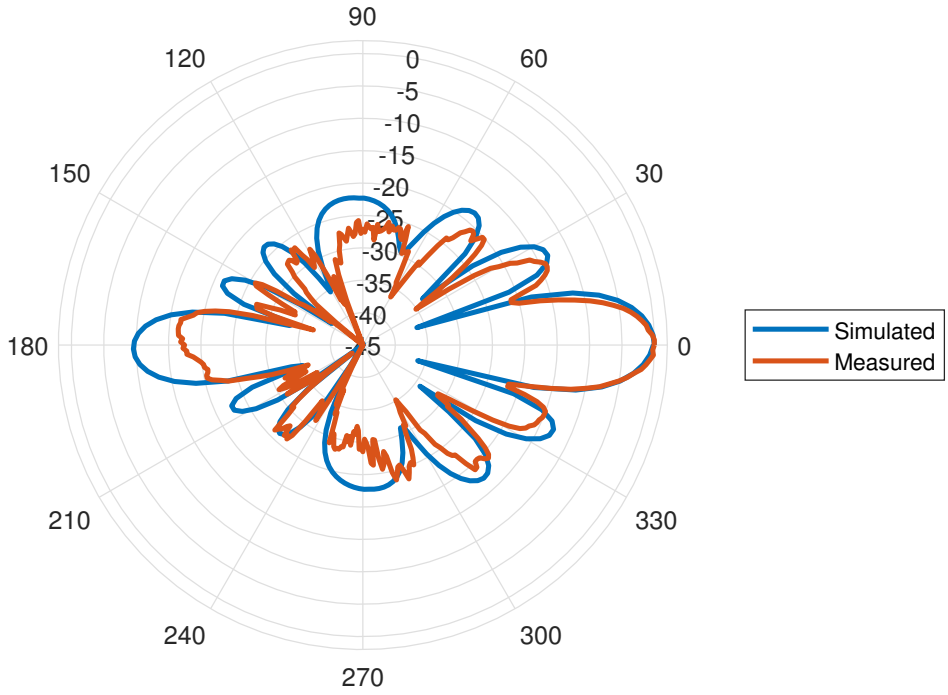

Figure 3.16: A comparison across the azimuth between the measured radiation pattern and the simulated pattern at 4 GHz. Both patterns have been normalized to have the same directivity.

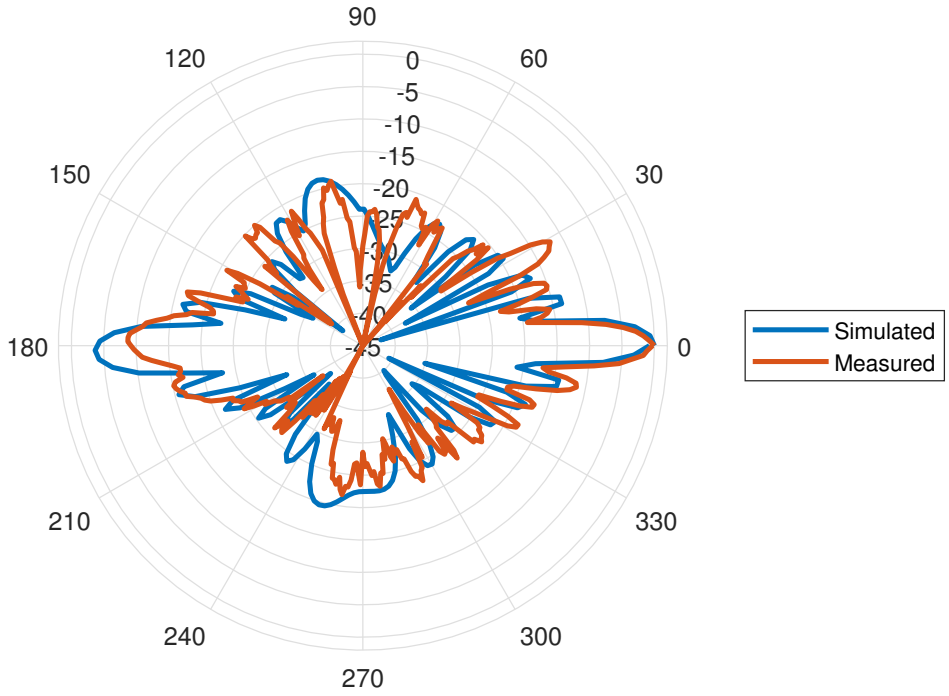

Figure 3.17: A comparison across the azimuth between the measured radiation pattern and the simulated pattern at 8 GHz. Both patterns have been normalized to have the same directivity.

In both Figure 3.16 and 3.17 there is an asymmetry between the simulated and measured strengths of the main lobe and the back lobe. The front-directed main lobe and grating lobes match more closely between the simulation and measurement than the back-directed lobes, which appear slightly weaker in the measurement. This could be due to the presence of the mounting structure and divider network in the simulation along with the relative turntable position during rear measurements. The setup shown in Section C.2 includes photos and a more detailed description of the mounting setup.

3.4.2 Inter-Array Spacing

Section 2.4.2 presents the requirement for high isolation between the TX and RX antennas. Increasing isolation between the two can be accomplished in several ways: by increasing the physical separation between the two antennas, improving directivity and reducing sidelobes, and placing RF absorbing material in the direct path.

In the final application both arrays will be directed towards the ground meaning the directions

in which the elements are arrayed will both be parallel to the ground. The two arrays are affixed parallel to each other when operating in VV or HH polarizations and orthogonal to each other when operating in VH or HV. Keeping the arrays orthogonal offers increased isolation relative to co-polarized orientations from simulations.

While isolation is increased, the cross-polarized scattering response from the targets of interest in the bands of interest is lower compared to the co-polarized response. For grass-like crop canopies one can expect up to a 15 dB reduction in the backscattering coefficient. In [52] it is shown that the cross-polarized backscattering coefficient for grass-like crops is around 15 dB below that of the co-polarized backscattering coefficient in the L-band. As another example, [53] shows the cross-polarized backscattering coefficient for snow as 10 dB less than that of the co-polarized coefficient. Initially the arrays will be co-polarized to maximize the potential response for testing, but assuming successful results a cross-polarized measurements may be taken as well.

When co-polarized the arrangement of the two arrays is restricted to some relative alignment within the same plane relative to the ground. They are kept at the same height to simplify range calculations and prevent back-feeding: where the main lobe of one array overlaps with a side-lobe of the other. In testing only two setups were considered: broadside alignment and array in-line alignment. Figure 3.18 illustrates these two setups.

The measured isolation for the in-line alignment is shown in Figure 3.19. In each of those measurements the separation between the inner two elements is 3 cm, the same spacing as the elements inside a single array. The legend describes the orientation of the two arrays with respect to each other. Aligned means the feedlines are on the same side, flipped in means they are facing each other, and flipped out implies opposite directions. Keeping the feeds facing each other has the lowest isolation, with opposite or same side orientation providing slightly higher isolation, on the order of around 1 or 2 dB for most of the band.

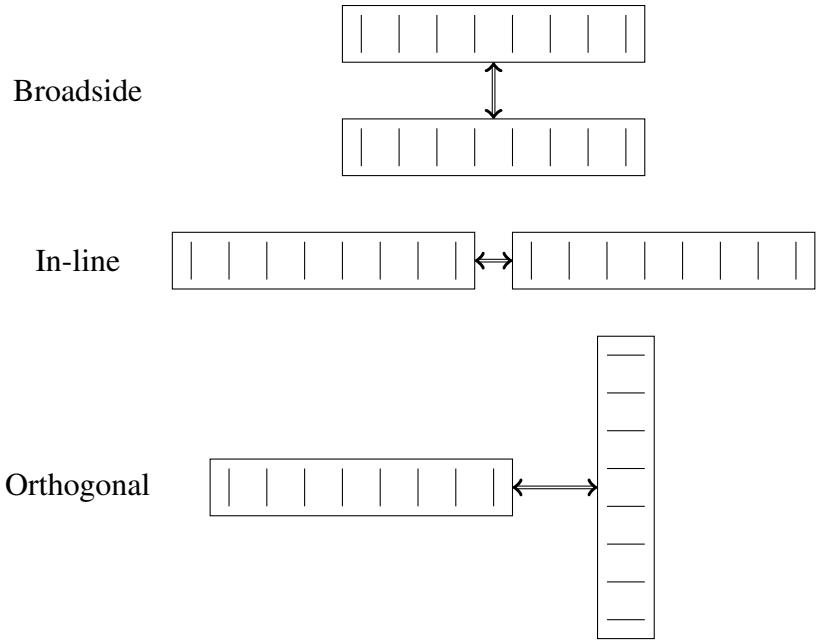

Figure 3.18: Relative array positions for broadside, in-line, and orthogonal alignment. The lines inside each rectangle represent the orientation and spacing of individual antenna elements.

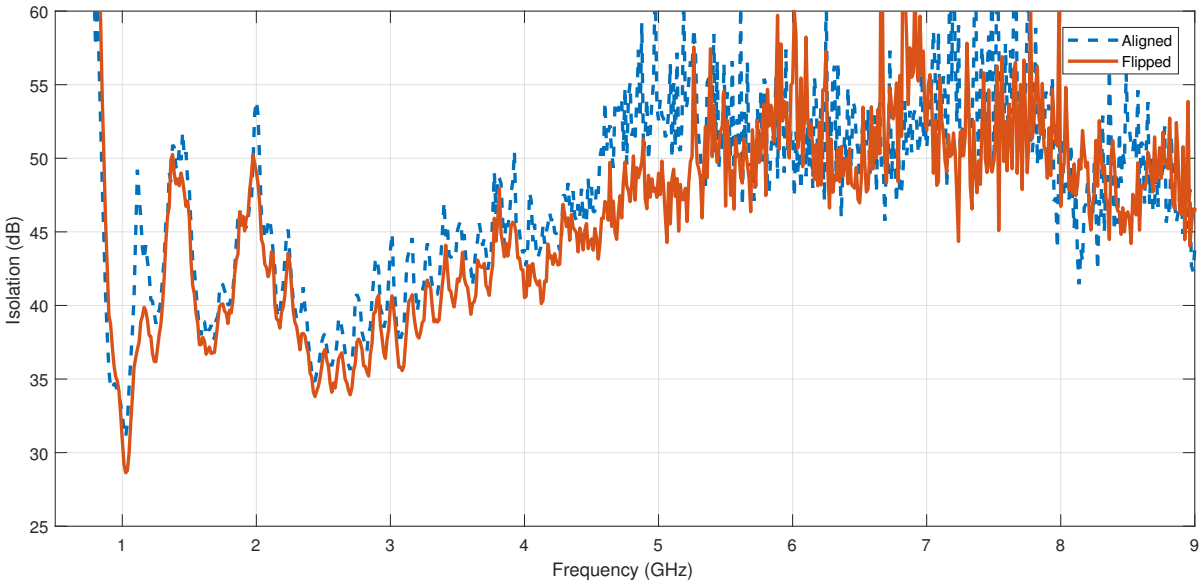

Figure 3.19: The isolation between two arrays arranged in-line (coplanar in the H-plane).

Broadside alignment in comparison offers less isolation than in-line, as can be seen in figure 3.20. Taking the center of both arrays as the points determining the relative spacing shows that for a comparable distance of around 20 cm, in-line alignment has 10 to 20 dB greater isolation across the band. Figure 3.21 shows the effects of changing the relative orientation of the two arrays at a

constant spacing.

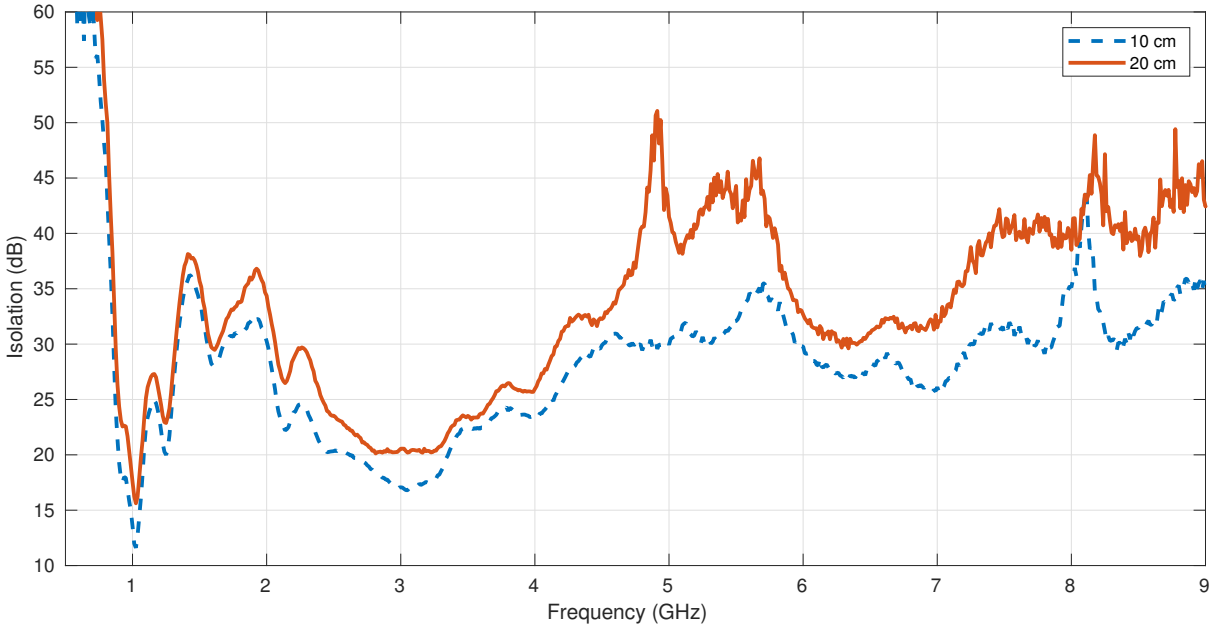

Figure 3.20: The isolation between two broadside arrays spaced 10 cm and 20 cm apart. The arrays were in the flipped orientation for both spacings.

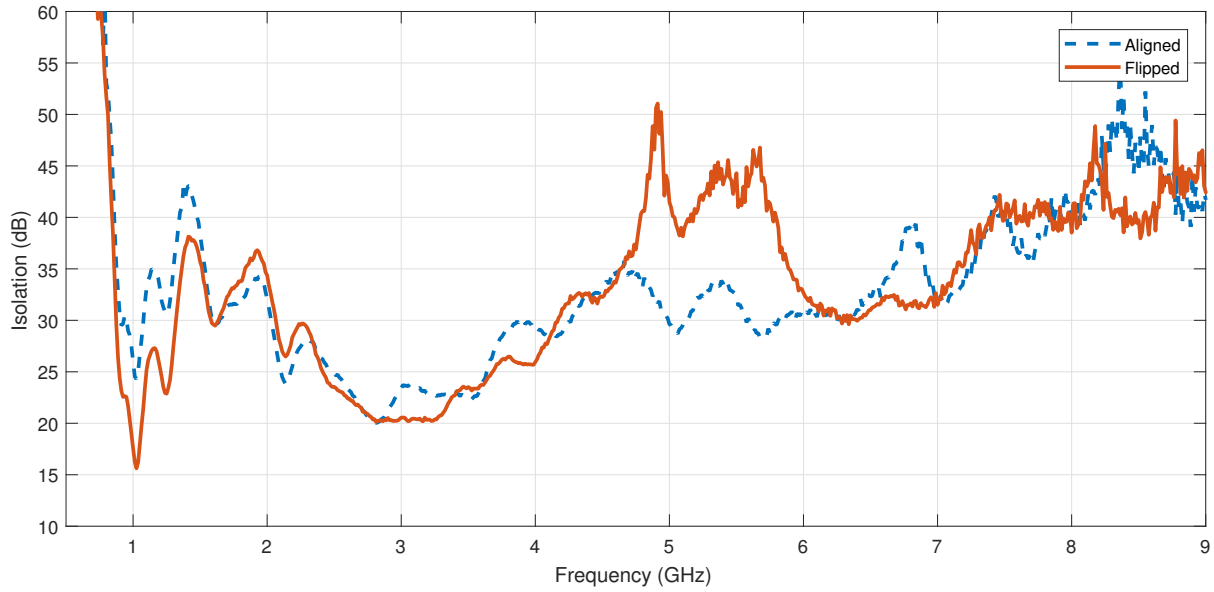

Figure 3.21: The isolation between two broadside arrays spaced 20 cm apart. Aligned indicates that the two arrays were oriented identically. Flipped indicates that one array is rotated 180° relative to the other around the end-fire axis.

From the measurements above, maximizing isolation is best done through aligning the arrays

in-line. This can pose a challenge in the array processing however, as with this configuration the radiation center of the arrays are offset in the plane of steering. As the target distance increases relative to the spacing this becomes less of an issue given the beamwidth of the array, but for close targets the spatial discrepancy for a common steering angle could be considerable if steering on both transmit and receive.

3.5 Dielectric Loading

The various parameters presented in Table 3.3 and the return loss for the array shown in Figure 3.12 all point to an antenna system that behaves sub-optimally below 2.5 GHz. The antennas were already milled out so any improvement in performance would come through either modifying the already made antennas or re-milling new ones. While the cost to make new antennas is low, the alternative path was taken and an external modifier was developed out of an interest in dielectric loading structures.

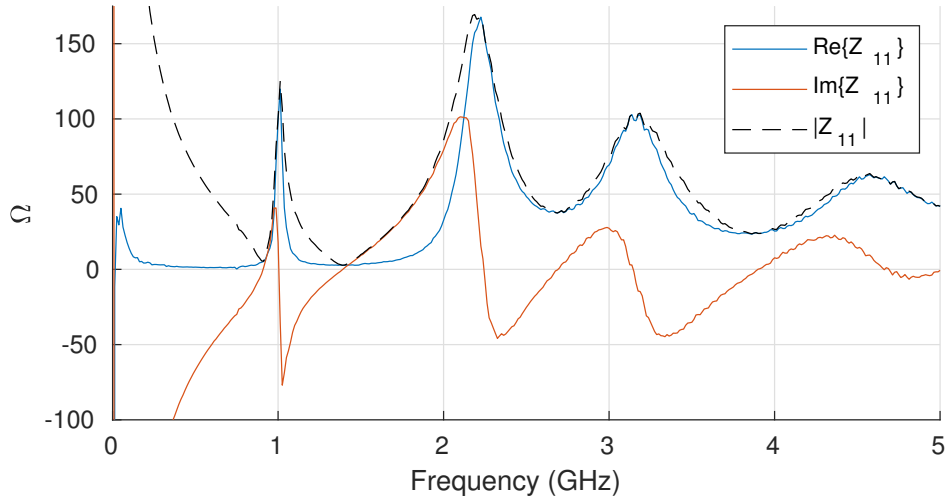

Figure 3.22: Measured input port impedance of a single antenna element.

Around the 2 GHz region of interest it is apparent in Figure 3.22 that the input impedance of the antenna is rather high, exceeding 150 Ω at a peak around 2.2 GHz. The end goal of the dielectric structure is to trim this peak in impedance without affecting the match at higher frequencies.

Under many models for planar quasi-TEM transmission lines the dielectric substrate assumed

to be present underneath the copper features is combined with the air above to approximate a homogeneous dielectric region with an effective relative permittivity ε_e that simplifies the model. Increasing the permittivity of the half space above the copper by replacing the air with a different material with a higher ε_r increases the effective permittivity as well. The phase velocity of the line is in turn decreased.

As mentioned previously, the antenna consists of a microstrip line that transitions to a slot line, and the slot line then exponentially tapers out. [51] shows that the exponential taper of the antenna can be modeled as a sequence of small slot line partitions continuously increasing in width. A closed form approximation of the characteristic impedance for a slot line and microstrip as taken from [54] and [47] is given in Equation 3.3.

$$Z_0 \approx \frac{120\pi g_s}{\sqrt{\varepsilon_e}} \tag{3.3}$$

The term g_s represents a scalar term defined in [47, 54] that is solely dependent on the geometry of the slot line or microstrip. The impedance is then inversely proportional to the effective permittivity, which means a loading structure with a higher permittivity than air will decrease the impedance of the lines.

The loading structure for a traveling wave antenna like the Vivaldi can be done in many ways: through immersion liquids [43], solid fills, or extensions of the substrates [55, 56]. Due to the availability of various easily milled plastics an enclosing attachable load structure was designed using a polycarbonate with a dielectric constant of around $\varepsilon_r = 3.4$.

[55] demonstrates how a dielectric load placed in front of a directive antenna can act as a guiding structure. Multiple front surface geometries were simulated such as a circular, elliptical, notched, keyed, and flat. From general observation of the radiation pattern the fewest reflections occurred with the flat front interface. A similar process was carried out with the back interface and a small curve was found to minimize the back lobe at 6 GHz more than any other option.

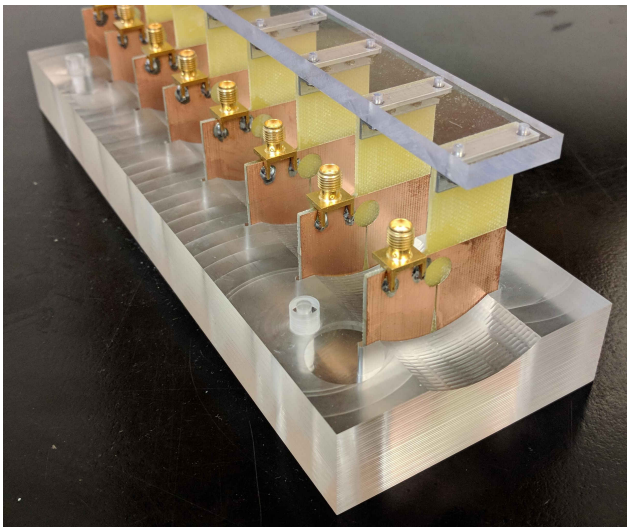

Figure 3.23: The polycarbonate dielectric loading structure with the antenna array slotted into it.

The final design is shown in Figure 3.23 and the exact dimensions for the structure are included in the appendix in Figure C.1. Table 3.4 includes antenna parameters for the loaded array to be compared with those of the unloaded array in Table 3.3. Directivity and gain are improved across the bandwidth, but the efficiency is lower. This drop in efficiency is due to a combination of dielectric loss from the surrounding polycarbonate and the reduced return loss at some of the higher frequencies.

Freq (GHz)	dB[Directivity]	dB[Peak Gain]	dB[Realized Gain]	Beam Area	Efficiency
1	1.947	1.470	0.330	6.454	0.755
2	6.976	6.239	4.943	1.801	0.894
3	9.000	8.012	5.821	1.396	0.890
4	19.912	17.779	17.431	0.631	0.893
5	26.892	22.713	19.317	0.467	0.845
6	27.972	23.134	22.634	0.449	0.827
7	37.325	30.016	28.260	0.337	0.804
8	62.844	49.491	48.362	0.200	0.788
9	30.545	21.969	20.384	0.411	0.719
10	28.810	20.281	17.779	0.436	0.703

Table 3.4: Simulated antenna array performance characteristics with the dielectric loading structure.

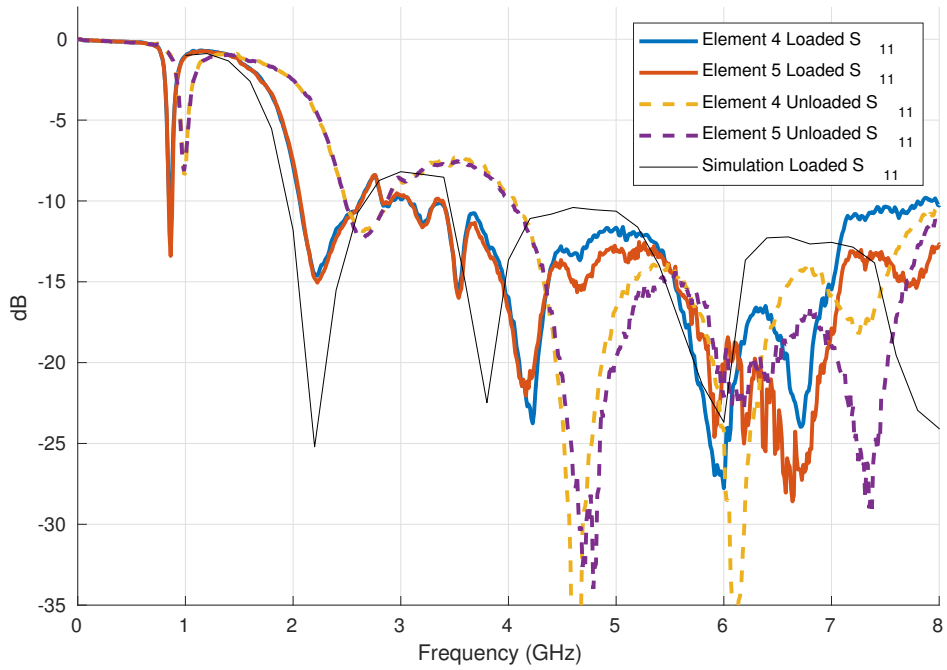

Figure 3.24: S_{11} parameter for the antenna array, both with and without the loading structure. The thin black line is from the HFSS simulation of the loading structure.

The loading structure succeeds in lowering the return loss and extending the 10 dB region down to 2.1 GHz, as visible in Figure 3.24. The measurements with the structure sit in between the simulation results and the unloaded structure however, and the higher frequency behavior is slightly worse. The input impedance is successfully lowered at 2 GHz; the 255 Ω peak is attenuated down to 160 Ω and shifted down 300 MHz. From visual inspection the impedance behavior across the bandwidth is shifted down by around 300 MHz as well, consistent with a lowering of the phase velocity.

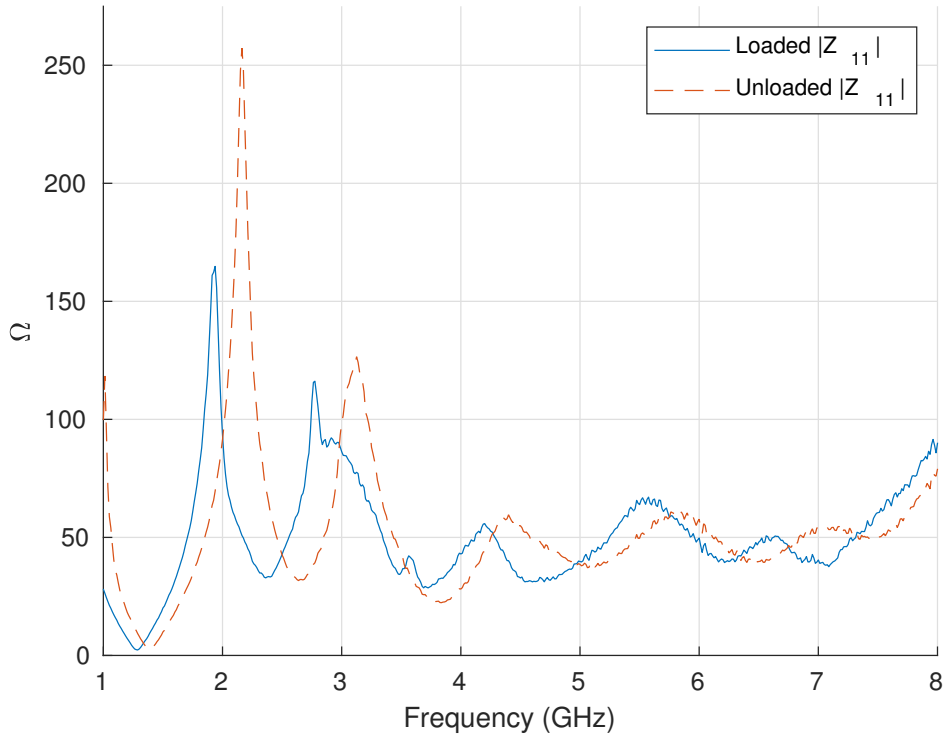

Figure 3.25: $|Z_{11}|$ for an element in the array with and without the loading structure.

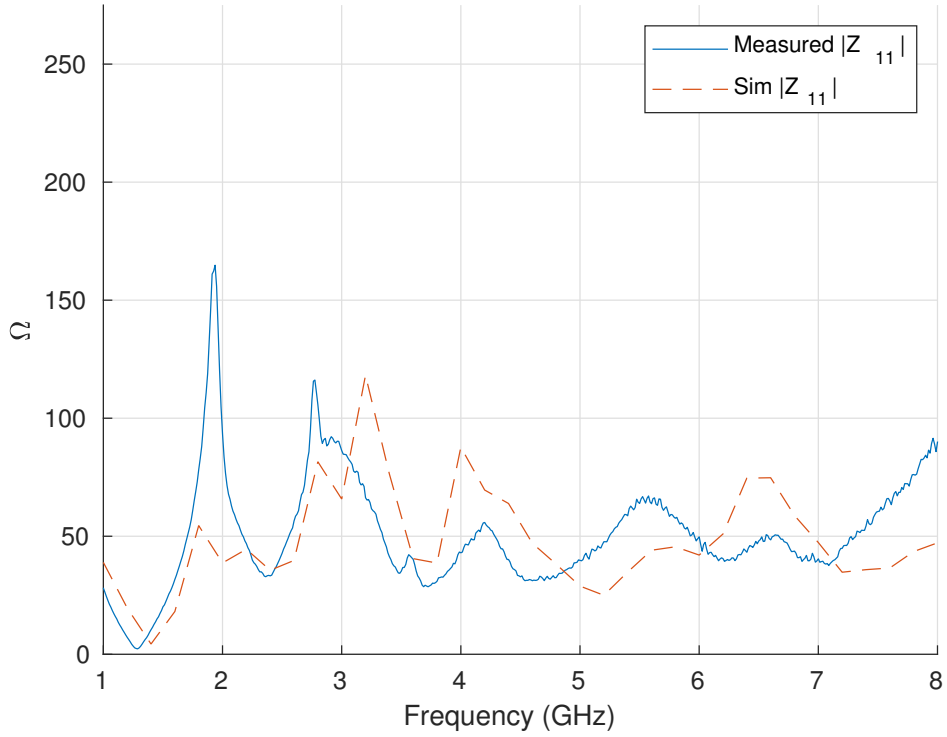

Figure 3.26: A comparison between the simulated and measured values of $|Z_{11}|$ for a loaded array.

The measured impedance peak attenuation does not quite match what was expected from the simulation, shown in 3.26, which could be caused by a few things. The polycarbonate used has an unknown dielectric loss and the slots milled out have a 1 mm air gap between the polycarbonate and the antennas themselves. The permittivity of the material itself could drift from the expected 3.4 value as well.

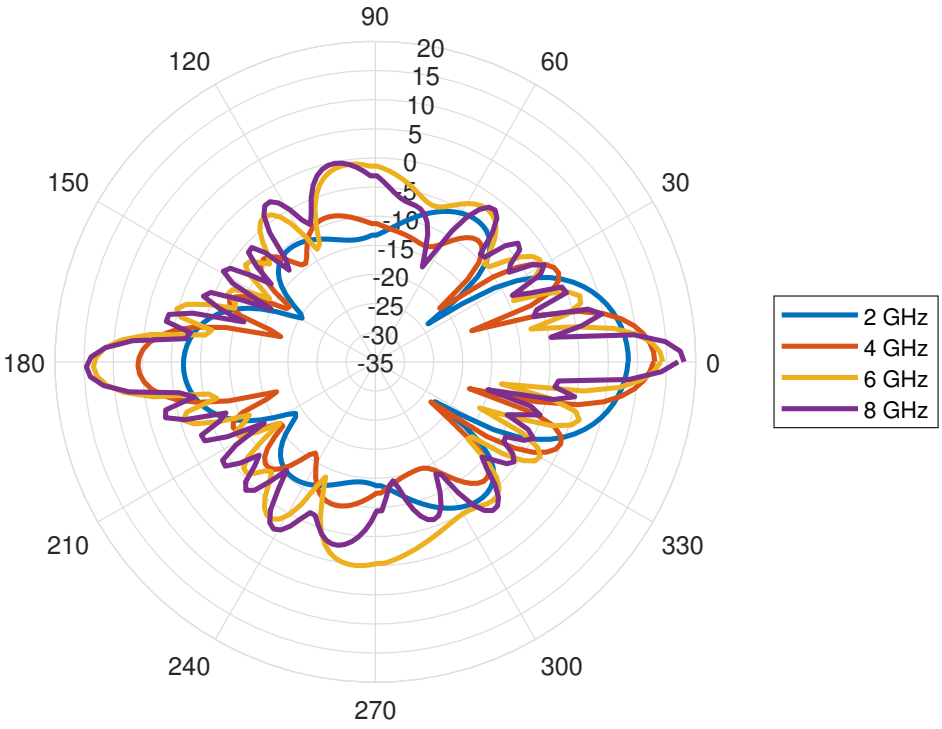

Figure 3.27: The azimuthal sweep ($\theta = 0, 0 \leq \phi \leq 2\pi$) of the directive gain pattern for the loaded array from the simulation.

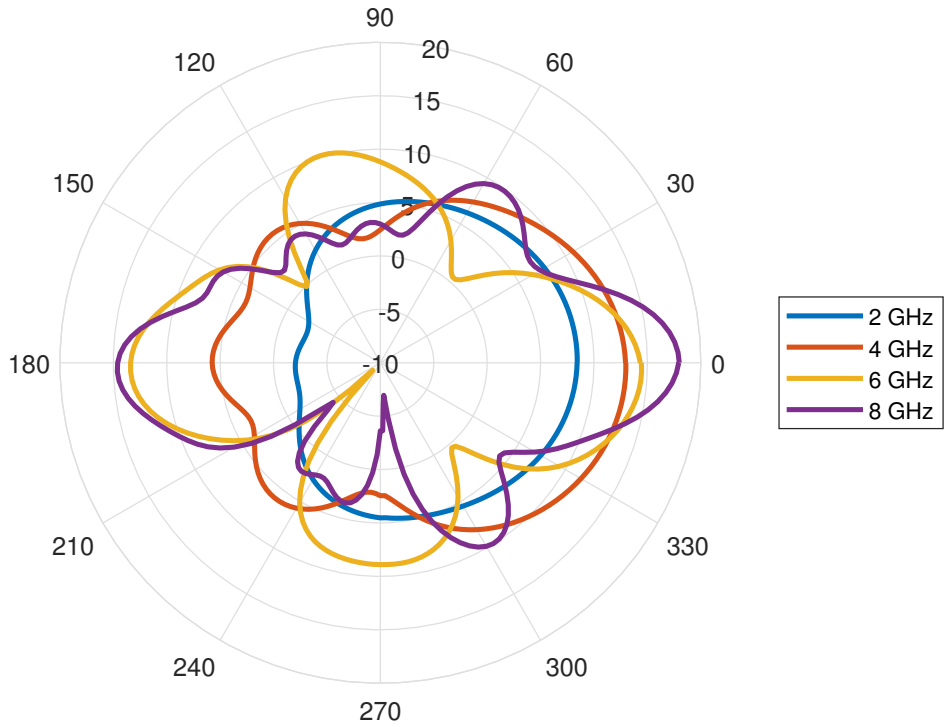

Figure 3.28: The elevation sweep ($\phi = 0, 0 \leq \theta \leq 2\pi$) of the directive gain pattern for the loaded array from the simulation.

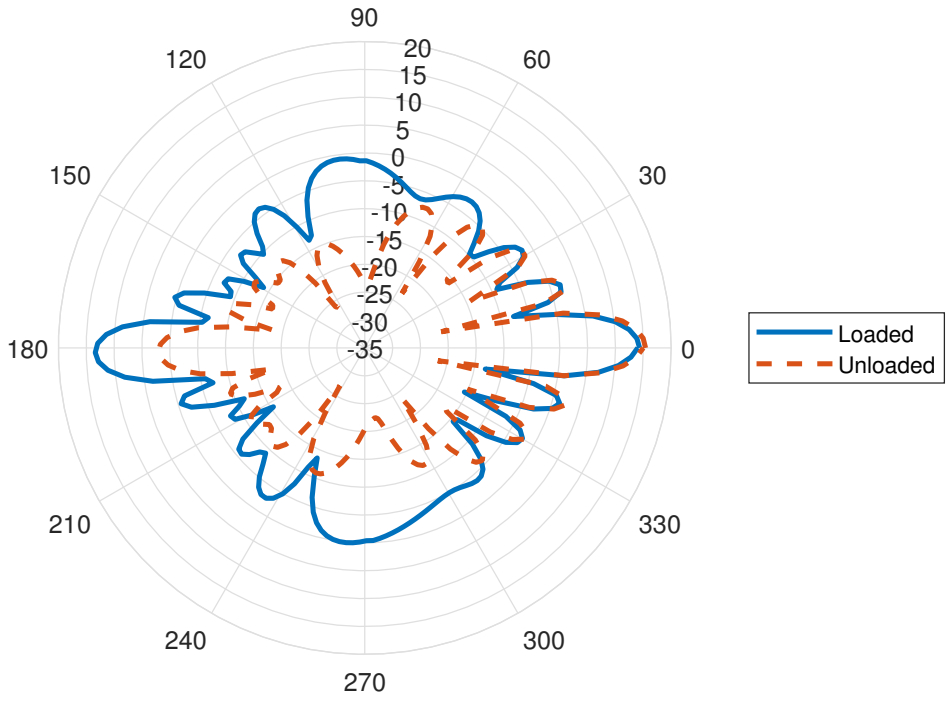

Figure 3.29: A comparison between the unloaded and loaded directive gain patterns at 6 GHz.

When comparing the radiation pattern between the loaded and unloaded arrays it is appar-

ent that the back and side lobes are stronger with the loading structure. This is highlighted in 3.29 which shows the behavior at 6 GHz. 6 GHz is around the frequency where the back lobe is strongest; there is a strong reflection centered around 5.8 GHz where the antenna radiates antipodally with the loading structure. This strengthened back lobe is the reason why the loading structure was not used in initial radar tests; it is much harder to eliminate the back lobe radiation with absorber foam given the position of the antennas relative to the chassis as shown in Figure D.1.

Chapter 4

Digital Processing Aspects and Implementation

4.1 System Operation and Storage

Continuous operation of the radar requires that the storage medium be capable of handling a data rate high enough to avoid restricting the operating characteristics of the radar. The current wheat platform radar operates at a PRF of 500 Hz with 16 presums without range gating [8]. This translates to an approximate output data rate of around 20 MB/s. An 8-channel system would increase the expected rate 8 fold and implementing range-gating would reduce it by the ratio of selected range out of maximum operating range. The output data rate can be reduced using extra presumming, range gating, or reducing the PRF, but a radar operating as a test platform ideally allows for as wide a range of operating parameters as possible.

The reference board has multiple interfaces available for getting data off the board: UART, Ethernet, USB 3.0, SDIO, SATA, PCIe, and DisplayPort. While the PHY is present for those interfaces, the readily available drivers are mostly limited to Linux implementations. As the control software for this radar is a bare-metal implementation, drivers intended for operation on Linux are not easily used. Xilinx provides reference bare-metal drivers for the UART, Ethernet, USB, and SDIO peripherals. Ignoring maximum transfer rates, the UART, Ethernet, and USB interfaces all rely on another processor to be present to write out the data to the eventual storage medium. SDIO does not have that restriction, but is limited by the maximum capacity of a single microSD card. While that is not an issue for a demonstration platform, a long term instrumentation platform would require a more robust storage interface.

Each transmitter board requires a controller to provide explicit power sequencing and filter

switching. The level shifters described in Section 2.3 that drive each signal are controlled by general purpose pins on the FPGA. These pins are controlled in the PL fabric when the DDS is continually running, and passed off to the processor when manually controlling the pulse sequence.

The synthesizer supplying the LO to the up-conversion chain is programmed by the processor through an SPI interface once on system boot-up. The initial configuration includes setting the capcode and VCO number required for the quick-recalibrate mode. Each time the LO is switched the divider register is updated and the calibration register is reset to force a VCO calibration. The processor then waits for lock detect through the GPIO controller before triggering the next chirp. This process also limits the chirp rate unnecessarily and improvements are discussed in section 5.2.2.

4.1.1 Calibration

A phased array radar relies on precise control over the relative phase of each channel. Uncontrolled variations in phase at the antennas results in spreading of the main beam [24]. As the individual RF transmit and receive channels are built to be as physically identical as possible, most of the inter-channel phase variation is introduced in the digital domain. Delivering synchronous clock signals to each converter is insufficient for achieving synchronous data in and out, as the internals of each converter can introduce variable delays. Internal elements such as variable length FIFO queues, on-chip clock routing, and PLL clock dividers and phase shifters are all sources of delay that may not be deterministic from information made externally available.

Converters implementing the JESD204b protocol rely on an external SYNC and SYSREF interface to measure the converter timing, allowing for synchronization of multiple converters. The JESD204b protocol is not simple to implement in HDL and many of the pre-made IP cores are relatively expensive [57]. The external clocking network also requires precise routing of clock signals between data converters which takes up board space. While chip dependent, achieving a deterministic latency across system resets can be a complex as well. The integration of the converters on the RFSoC solves many of these problems. Locating multiple converters on a single tile

means that only a single clocking signal is needed per tile due to the shared PLL. A single sysref signal is required for all tiles, as there is an internal sysref distribution network as a component of the Multi-Tile Synchronization (MTS) system.

The variable length routing from the SoC out to the off-board connectors also skews the signals. The reference board used in this design has connectors fanning out asymmetrically from the SoC to the edge of the board. Minimal length matching is implemented in the traces to the connectors which leaves a difference of around 3 cm between the shortest and longest paths off-board. Assuming the board's top layer substrate has a permittivity of $\varepsilon_r = 3.5$, a 3 cm distance corresponds to a time delay of 187 ps, which is 150% the duration of a period at 8 GHz, the highest operating frequency of this system. Fortunately routing skew is constant and calculating the required time delay for adjusting the signal requires only a single session of measurements per channel. Measurements were carried out by using two adjacent DAC channels to generate identical pulsed chirps that sweep the first Nyquist band. Delays between two channels were then measured using a 20 GS/s oscilloscope to capture multiple pulses and average the relative delay.

The two channels used to measure the relative delay needed to exist on the same converter tile since the PLL and digital datapath is only shared between the four converters on a single tile. Each tile has its own PLL and a potentially different digital datapath delay [58]. Comparing adjacent delays across tiles requires synchronization of the digital datapath in the DAC across tiles after startup, which is accomplished using the MTS system. MTS requires a 10 MHz synchronization clock to coordinate every tile, however the carrier board used in this system is incapable of supplying that signal. This means some approximation of MTS must be completed instead, which requires re-measuring the time delays between each tile every time the system is turned on. Once measured the time delay has to be inserted into the signal, either during the pattern generation or by modifying the DDS initial parameters. Due to the extra work required by that process the final radar design was restricted to a single DAC tile, meaning only four transmit channels were operational.

4.2 Chirp Generation

The task of generating the wideband chirp for FMCW radar operation can be an intricate task given the specific requirements for a performant radar. Past FMCW radar systems at CReSIS have used various methods of chirp generation, with the general trend of the process becoming more and more digital. Earlier incarnations of the snow radar fed a 1 GS/s DDS into a PLL which was then down or upconverted to the desired band. The current design uses a high performance AWG from Keysight, capable of directly generating the entire 2-18 GHz chirp. The remaining signal chain at that point is reduced to a series of filters and amplifiers, reducing the possible entry points for noise and interference and improving the SNR greatly [7]. Currently, an AWG capable of operating at that frequency is expensive and would dominate the financial cost of the system. Considering the physical size of the rack mounted chassis and the limited number of channels such a setup becomes less ideal for the development of a lower cost, compact system as pursued by this work.

The new transmitter design pursues a reasonable middle ground between the all-analog and all-digital chirp generation methods through a band hopping method using smaller instantaneous sub-bands. An easier-to-generate, lower bandwidth chirp is generated by a (low cost) high-speed RF DAC and then up-converted to one of multiple selectable sub-bands.

With the ever increasing feature density of VLSI and advances in IC packaging, the cost to produce a high speed, high resolution DAC has gone down. Many major manufacturers (TI, Analog, Maxim) now offer DACs with full (no interpolation) sampling rates exceeding 5 GS/s and usable analog bandwidths exceeding 4 GHz. These DACs are typically built around a current steering architecture, usually making use of unary coded current sources, binary-weighted current sources, or some hybrid of the two. Unary coded DACs operate through having 2^n driving current sources, where n is the number of bits used to resolve the input signal. Binary weighted DACs on the other hand only require n current sources, but producing an accurately weighted binary DAC requires stricter manufacturing tolerances lest the resulting analog signal levels not map linearly to the digital value. In the case of some hybrid architectures, such as the one used in this system, the first few LSBs of the signal are handled by a binary weighted source while the remaining more significant

bits are handled by a unary coded source. This can reduce the footprint of the implementation in both layout area and power consumption while still achieving accuracy similar to that of an entirely unary coded DAC [59].

The digital stream of values fed into the DAC that forms the desired output chirp is generated using an FPGA. On the FPGA there are several methods for generating the values for a chirp, two of which are considered here: direct pattern playback and DDS.

4.2.0.1 Pattern Playback

Pattern playback is not conceptually complex means of signal generation. The values are pre-computed and statically stored in some memory region. During playback the values are loaded from memory and passed directly in to the digital datapath of the DAC. It is possible for the implementation to be very simple from a HDL perspective; if the data is stored sequentially in memory then a simple counter can be used to address the values. Populating the memory region of the pattern can be done during the initial FPGA boot sequence, or a processor local to the board with shared memory access could be used for configuring during operation.

Complexity is introduced in the trade-off between memory size and bandwidth. The memory resources typically found in an FPGA such as block RAM (BRAM) and distributed RAM are capable of being arranged and pipelined to obtain high data throughput. The total capacity can be rather limited though: a 1 µs long pattern at 6.4 GS/s with 14 bit resolution works out to around 90 kb of storage required. If a single BRAM is 36 kb then at least 3 BRAMs need to be utilized to store the entire 1 µs long pattern. An FPGA with a few tens of Mb will quickly run out of available memory when channels are added on and pattern duration is increased. Including external SDRAM solves the total capacity issue, as multiple gigabyte DIMMs are commonplace, but can hit a bottleneck due to limited bandwidth. For example, DDR4 SDRAM with a 2400 MT/s interface has a data transfer bandwidth of around 19 GB/s, and a single DAC channel operating at 6.4 GS/s with 14 bit resolution requires 11.2 GB/s of compacted memory bandwidth. An extra DDR4 interface instance would be required if a second distinct pattern is needed, but the carrier

board used in this system is limited to a single DIMM.

Since each channel needs a different time delay to account for the variable routing skew on the carrier board, and that time delay is not an integer multiple of the sampling period, eight distinct patterns are needed. The architecture used is shown in Figure 4.1.

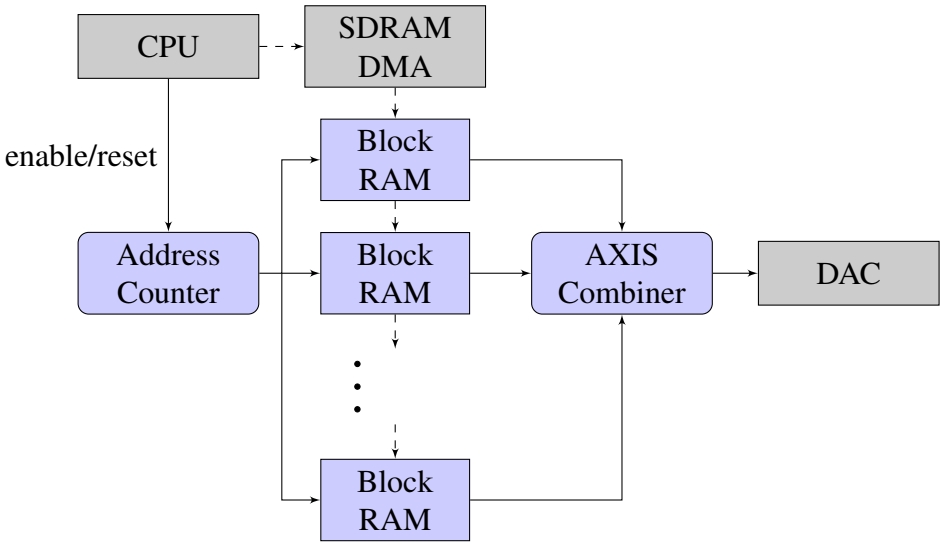

Figure 4.1: Block diagram of pattern playback to DAC.

Each BRAM instance is configured for two port operation to allow the processor to access the memory through an AXI interconnect to the programmable logic. The Zynq SoC configuration has multiple ARM Cortex-A53 cores, each with their own FPU, which simplifies the chirp generation software. Relying on the FPU to generate the pattern as it is written to the BRAM would result in several millisecond load times, so patterns are cached to regions of SDRAM and transferred to the BRAM through the DMA controller. Eight channels of the 10 µs pattern consume 8 Mb of BRAM. A transfer to swap out the pattern is done every time the band is changed to avoid monopolizing all BRAM instances in the FPGA. The theoretical maximum data transfer rate would limit the frequency of band hopping to 3 kHz, which is acceptable given that each band will have multiple pre-sums. In practice the maximum transfer rate resulted in a limit closer to 500 Hz. It should be possible to improve upon this limitation with modifications to the current setup for future work.

The limited PRF and the large resource requirements of this implementation are detractors when considering it in a system that requires rapid band switching, but the ease of configuration

makes it ideal for testing.

4.2.0.2 DDS

Direct digital synthesis (DDS) is a method for digitally generating sinusoidal signals. A basic implementation consists of a counter fed into a lookup table (LUT) or ROM containing a full period of a sinusoid, which outputs its values into a DAC. The rate at which the counter steps through a full oscillation in the ROM values determines the output frequency and is usually set by a tuning word driving the counter's phase increment. Figure 4.2 shows a basic block diagram of this setup.

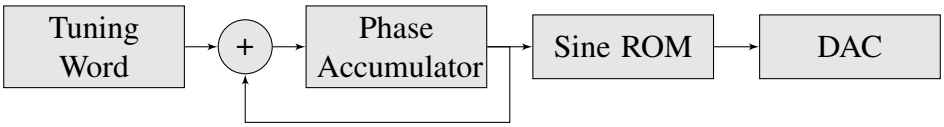

Figure 4.2: Basic DDS implementation where each element is synchronously clocked.

The counter and ROM can be implemented using discrete logic ICs for low speed signals, but RF DACs use high speed transceivers that are best interfaced with using an FPGA. Everything excepting the DAC can then be implemented in the FPGA logic. In place of an explicit ROM other algorithms such as CORDIC [60] or other approximations can be used as well, but for this implementation a simple sine LUT was used.

The depth of the sine LUT determines the frequency tuning resolution and affects the SFDR [61]. The frequency tuning resolution is also dependent on the output sampling clock:

$$\delta f = \frac{f_s}{2^n} \tag{4.1}$$

$\delta f =$ Frequency Resolution

$f_s =$ Sampling Frequency

$n =$ Phase resolution of LUT in addressable bits

The quantization of the phase that results from the limited LUT depth results in small phase errors that behave like time-domain jitter. This jitter produces harmonic spurs that then lower the SFDR. If the phase is assumed to be uniformly distributed, the best quantization is uniform. A uniform quantizer acting on a uniformly distributed input signal has an output SNR of $2^{2n}-1$. This results in a general rule of thumb that the SFDR improves by 6 dB with every added bit of phase resolution, as $10\log_{10}(2^{2n}-1) \approx 6n$ dB. Ignoring the second and third harmonic distortion, the DACs in the RFSoC are specified to have a SFDR of around 78 to 83 dBc according to [12]. The power levels of the second order and third order harmonic distortion relative to the DAC full scale power are a bit higher than the SFDR, so ideally the SFDR of the DDS output would exceed around 80 dBc. To accomplish this the LUT resolution would need to be $\lceil \frac{80}{6} \rceil = 14$ bits. A 14 bit phase resolution has a frequency tuning resolution of 390.625 kHz assuming a constant integer tuning word. The SFDR can be improved further by dithering the phase accumulator. Dithering adds noise to randomize the otherwise periodic phase error which spreads the harmonic spurs over a greater bandwidth [12].

The resolution of the values stored in the sine LUT affect the SFDR in the form of quantization noise as well, however the amplitude is not uniformly distributed in the same way as the phase. This adds an extra offset to the rule of thumb mentioned previously, but not much can be done as the quantization is imposed by the physical implementation of the DAC. The DAC has a 14 bit output resolution that, while uniform for all purposes relevant to this work, is not uniformly weighted across the bottom five LSB due to the implementation of the binary current source [59].

A 14 bit wide 14 bit addressable sine LUT storing a full period would consume 230 kb of ROM. This can be compressed by storing only the first fourth of a period, $[0, \frac{\pi}{2})$, and inverting the phase and the amplitude depending on the first two address bits. The compressed size is then equivalent to that of an uncompressed 12 bit addressable LUT, but a few extra resources are required to do the one's and two's complement operations that would accomplish the respective phase and amplitude inversions.

For CW tone generation the counter sweeps through the ROM at a constant rate. To generate a linear chirp, that rate has to change linearly. The chirp used in this radar sweeps from 500 MHz

to 2.7 GHz. A 500 MHz tone has a tuning word of 1280, and a 2.7 GHz tone has a tuning word of 6912 when using a DDS with 14 bit phase sampled at 6.4 GS/s. The tuning word will increment 5632 times over 10 µs, increasing by one every 11.36 samples, for an effective step size of 0.088 per sample. Approximating that step can be done by increasing the width of the tuning word and truncating the output. By adding 10 bits to the tuning word and multiplying all values by 1000, the step size of 88 can be added as an integer each step. A division by 1000 takes place before the truncation and is approximated by multiplying by 131 and dividing by 131072, which can be done using only addition and shift operations. The error in this approximation reduces the chirp rate to 0.999451 times that of an ideal chirp with a division by 1000.

At 6.4 GS/s the DAC sample clock exceeds that of the FPGA fabric rate, meaning sample data is clocked into the DAC in parallel at a lower clock rate. This requires implementing multiple DDS in parallel to achieve the necessary data rate. Using an input data clock of 400 MHz, 16 samples are delivered in parallel each clock cycle with each needing a separate DDS implementation. The increments for each DDS phase accumulator are then different to account for the consecutively generated samples being 16 apart in the sequence as eventually output by the DAC. Determining the tuning word and initial values for the phase accumulator can be done by discretizing the phase term

of a continuous chirp and inserting an offset term to account for the out-of-order DDS sequence.

Continuous chirp phase term:

$$\phi(t) = 2\pi(f_0 t + \frac{k}{2}t^2) \tag{4.2}$$

Time in terms of sample index (m):

$$t = \frac{m}{f_s} = \frac{m}{6.4 \times 10^9} \tag{4.3}$$

Expanding the discrete chirp phase term:

$$\phi[m] = 2^{14}(f_0\frac{m}{f_s} + \frac{k}{2}(\frac{m}{f_s})^2) \tag{4.4}$$

$$\phi[m] = 2^{14}(\frac{500 \times 10^6 m}{6.4 \times 10^9} + (1.1 \times 10^{14})(\frac{m}{6.4 \times 10^9})^2) \tag{4.5}$$

$$\phi[m] = 1280m + 0.044m^2 \tag{4.6}$$

The finite difference of the phase term yields the tuning word and its per-sample increment.

$$\delta\phi[m] = \phi[m+1] - \phi[m] \tag{4.7}$$

$$\delta\phi[m] = 1280 + 0.088m \tag{4.8}$$

Time delays can be added by introducing a time offset q into the phase term, where q is some constant fraction of a single sampling period.

$$\phi[m+q] = 1280(m+q) + 0.044(m+q)^2 \tag{4.9}$$

$$\phi[m+q] = 1280m + 1280q + 0.044m^2 + 0.088mq + 0.044q^2 \tag{4.10}$$

Tuning word values for a 16 sample parallel DDS are found by taking the finite difference for a 16

sample offset.

$$\delta_{16}\phi[m+q] = \phi[m+16] - \phi[m] \tag{4.11}$$

$$\delta_{16}\phi[m+q] = 1.408m + 1.408q + 11.264 + 20480 \tag{4.12}$$

Taking the 16 sample offset finite difference on the tuning word values results in the parallel tuning word increment of $16 \times 1.408 = 22.528$.

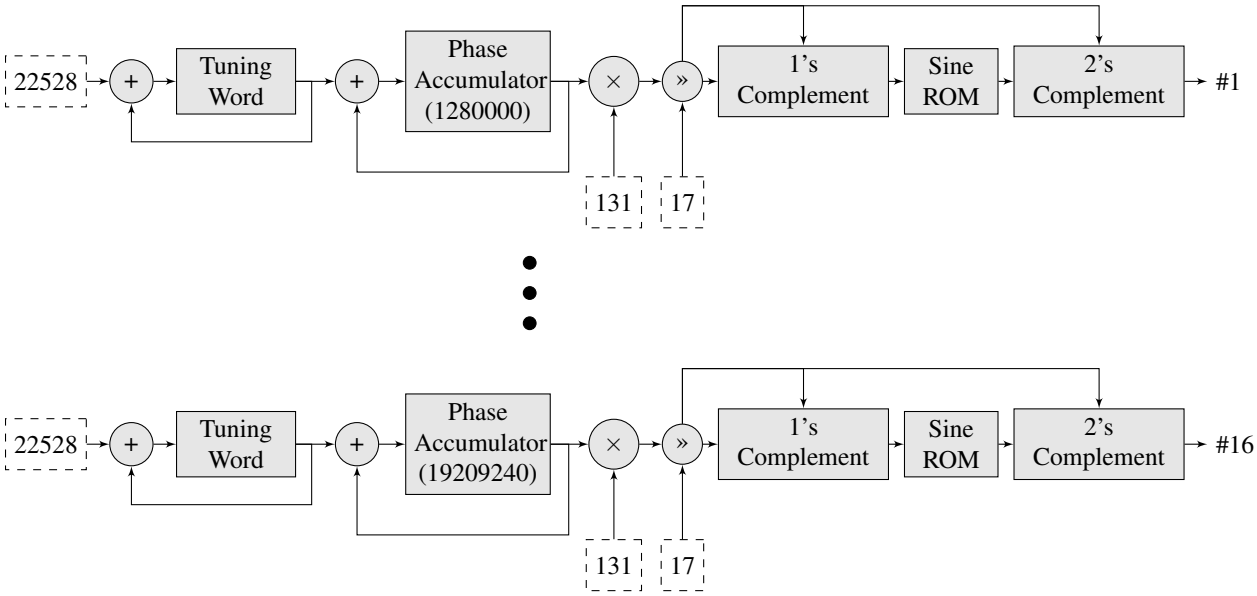

Figure 4.3: 16 sample parallel DDS implementation.

Shown in 4.3 is a complete block diagram of the parallel DDS implementation. The tuning word and phase accumulator initial values can be changed and set by the processor through an AXI4 Lite register interface. The samples at the DDS output can be fed directly in to an AXI stream combiner for delivery to the DAC input. In this system however they are first passed through a scaling stage for normalization.

4.2.1 Normalization and Frequency Notching

Any amplitude modulation of a signal introduces sideband signals that may or may not be desired. These sidebands can appear small and close to the carrier in the case of slow time modulation such

as temperature dependent gain variation, and they can also be very broadband due to higher frequency modulation such as rapid cuts and bursts in transmission. From [62] the sidelobes resulting from ripple in the power of the transmitted signal are related to the magnitude of the ripple A by Equation 4.13. It is in the best interest of any radar that the transmitted signal be free of sidelobes, as broadening of the signal reduces SNR and range resolution.

$$dBc[Sidelobe] \approx 20\log_{10}(10^{\frac{dB[A]}{20}} - 1) \tag{4.13}$$

The compressed pulse used in an LFM architecture, while drawn out in duration, is not an ideal infinite signal. The largest sources of amplitude modulation are from the start and stop of the chirp and from frequency dependent gain variations. The transmitter components do not have a constant gain across the bandwidth of the chirp, so as the signal sweeps in frequency the output power varies in time.

Both sources of modulation can be minimized through corrections applied to the input signal. Windowing the signal and smoothing the transition to full power can reduce the harmonics associated with the start and stop. Gain variation can be accounted for by accurately characterizing the gain of the transmitter and inversely adjusting the signal.

4.2.1.1 Windowing

The SNR at the output of the matched filter in an LFM radar is directly proportional to the total energy of the input signal [28]. Relative to a rectangular window, a Hann window lowers the total energy of a signal by around 4 dB, while a 10% Tukey lowers total the energy by 0.28 dB. The energy dependence of the SNR needs to be considered against the level of sidelobes resulting from the window. Using a 10 μs pulse as reference, the first sidelobe appears around -13 dBc for a rectangular window, and a 10% Tukey window makes effectively no improvement on that. A Hann window drops the first sidelobe down to -30 dBc at the cost of the main lobe broadening. The sidelobe behavior for various Tukey windows is shown in Figure 4.4.

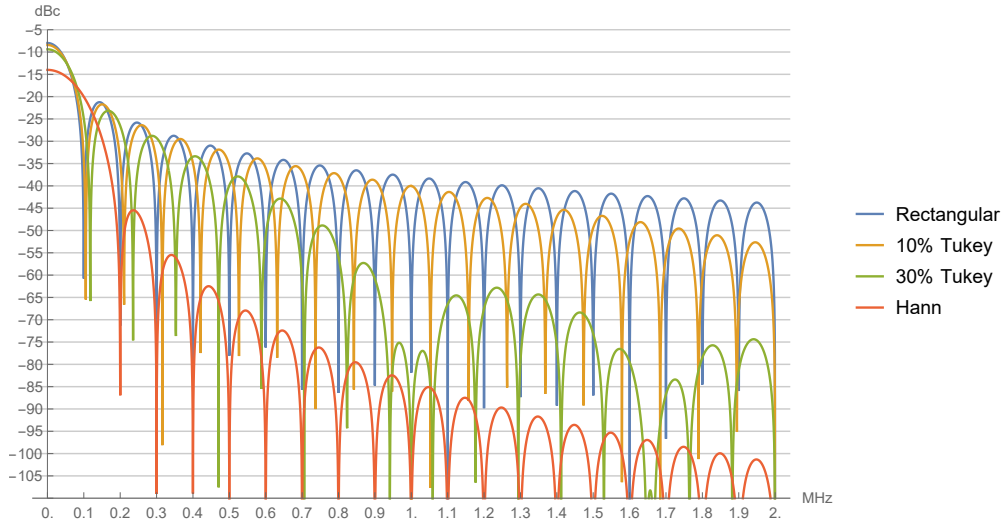

Figure 4.4: Power spectrum showing sidelobe levels for various levels of Tukey windowing for a 10 µs pulse.

Figure 4.5 demonstrates the affects of various window lengths on a continuous chirp. A 0.2 µs length Tukey window was applied to the left two transitions, a 0.1 µs window was applied to the center notch, and the right transition has a rectangular window applied. In looking at the rectangular window in the spectrogram it is apparent that the sharp cut-off results in a broadband pulse. This pulse appears in the PSD in the form of the increased gradient rolling off to the right. It is also borne out that the length of the window affects the spectral content, with the short gap in the center notch having an insufficiently long window to reach the same level of blanking as the lower frequency notch.

4.2.1.2 Normalization Measurement

Measuring gain variations of the signal is done by capturing reference chirps for each band using a high speed oscilloscope. The reference chirp as input to the DAC has a rectangular window and no other amplitude corrections to serve as a known baseline. A simple envelope detector can be applied to the captured signals to identify amplitude modulation in the time domain. The output of the detector can then be directly compared to an arbitrary window shape to obtain the necessary scaling factors in the time domain.

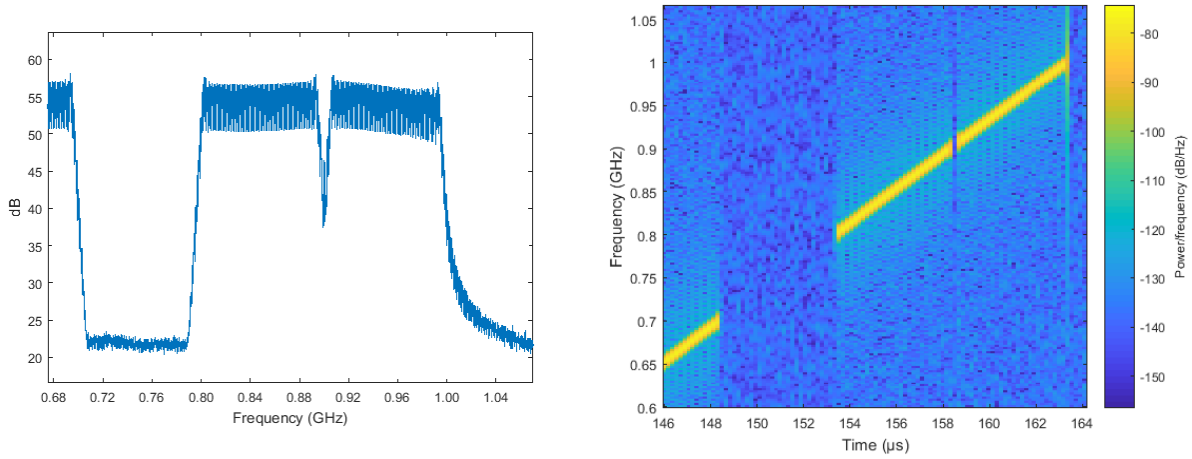

Figure 4.5: The PSD and spectrogram of a subsection of a chirp demonstrating an early attempt at frequency notching. Produced using pattern playback with a TI DAC38RF82 and recorded using a 5 GS/s oscilloscope.

Corrections can also be done in the frequency domain using a spectrum analyzer, but mapping to the time domain can require more iterative adjustments, especially if the signal has in-band spurs that would distort the power spectrum. Using S_{21} measurements of the transmitter boards and associated cables is a more viable option, but it does not account for the roll-off from the DAC carrier board.

4.2.1.3 Implementation

The normalization implementation depends on the method used to generate the signal. Correcting a signal produced by the pattern playback method described in Section 4.2.0.1 is as simple as adding in the measured scaling function any time before the pattern is written to the BRAM. Since it is not real time, the corrections can be as precise or complex as desired. In contrast, normalizing the signal produced by the DDS described in Section 4.2.0.2 requires a separate system.

A simple way to implement normalization for a DDS in the HDL is to store a pattern containing the amplitude correction in memory and apply them at the output of the DDS. As mentioned earlier, a prominent advantage of a DDS over the pattern playback is reduced memory requirements. This advantage is preserved despite the extra memory consumed by the correction pattern, as only a

single correction pattern is required across all channels if the physical transmit channels can be considered sufficiently identical. If spatial windowing of the transmit array is desired, an extra per-channel scaling constant can be included to avoid independent patterns. Depending on the requirements of the chirp, the time and amplitude resolution of the pattern can be decreased which reduces the memory footprint.

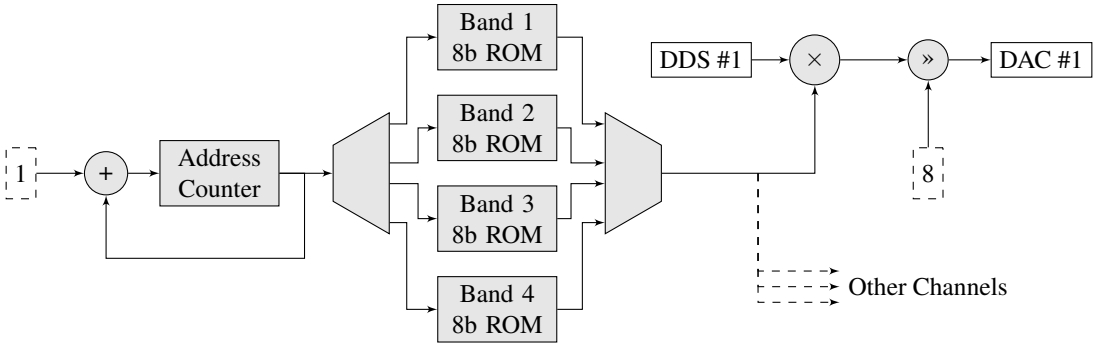

Figure 4.6: Simple structure for applying amplitude correction to DDS output.

Since each band uses a different path in the switched filter bank and the rest of the components do not have uniform gain, a separate normalization pattern is required for each band. This is shown in Figure 4.6 where the immediate pattern address is routed to a different region of block memory depending on which band the system is currently transmitting on. The pattern used is 8 bits wide and 4000 values deep, or one 8 bit level of correction per 16 samples. A 10 µs 2.2 GHz chirp sweeps across 550 kHz in 16 samples, meaning the correction can apply sub-MHz adjustments across multi-GHz bandwidths.

If the normalization pattern contains blank regions for the purpose of notching out different regions, then it may be valuable to zero out the ADC input as well. With no signal transmitted during the blank region, signals incident on the receiver mixer will have no accompanying reference signal to be correlated with and anything captured by the ADC will be noise. A calibrated delay is added to the interrupt controlling the zeroing at the ADC output to compensate for the digital data path in the converter itself, which can vary across converter configurations. Measurement of the delay can be done by transmitting a sharp impulse and timing the LO feedthrough from the receiver mixer. Inserting the blanking here as opposed to in post can be beneficial as it saves storage space

by not having to include time-stamps for when the gap begins.

Using a similar structure phase normalization could be implemented as well. Instead of producing a multiplicand to be combined with the DDS output, the output of the phase normalization BRAM would be summed with the output of the phase accumulator before the sine LUT in the DDS implementation. Given the 14 bit LUT width a phase normalization implementation would require an equivalent resolution for maximum control, taking up more space than the amplitude resolution.

4.2.1.4 Normalization Results

Figures 4.7 and 4.8 show the results of the normalization implementation described above as applied to the first band of the radar (1.8 GHz - 4 GHz). The average output power is reduced to 13.5 dBm from an un-normalized peak of around 17 dBm, but the cross-band power variation is brought down from ± 2 dB to within ± 0.2 dB. The remaining variation seen around 3.4 GHz in the normalized waveform is the result of a harmonic present in the up-converter LO that varied in frequency slightly between the two chirps resulting in an extra modulation product in that band.

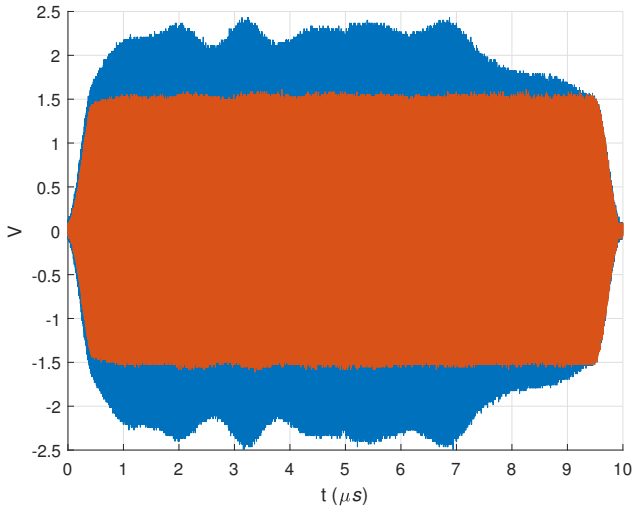

Figure 4.7: Time domain peak-to-peak amplitude of a chirp from 4 GHz to 1.8 GHz with (orange, foreground) and without (blue, background) normalization. Both have a 10% Tukey window applied. This was captured using a 50 GS/s oscilloscope.

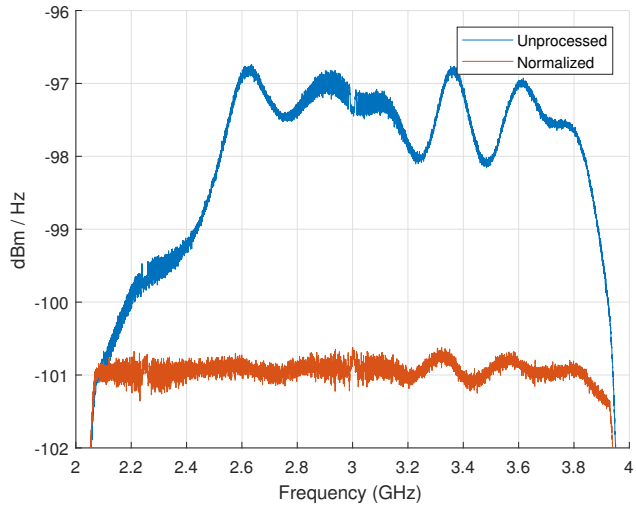

Figure 4.8: PSD of normalized and non-normalized chirps displayed over unity region of Tukey window. Orange shows the normalized results and blue shows the non-normalized results.

4.2.2 Mixer Product Minimization

To maximize the SNR of an FMCW radar it is critical for the transmitted signal to be free of other in-band spurious signals. Unwanted signals that are transmitted and passed on to the dechirping stage produce noise that can show up as false target returns. A downside to the use of the up-conversion stage as described in Section 2.2 is the reliance on an RF mixer to perform the frequency shifting, which acts as one of the largest sources of in-band spurs. With the use of a high speed DAC and characterized mixer behavior, it is possible to reduce the end effect of the spurious mixer products.

A perfect, ideal mixer would perform a straight multiplication of two input signals as shown in Equation 4.14, however such a device does not exist and physically realizable mixers are nonlinear devices.

$$s_1(t) = A\ \cos(\omega_1 t);\ s_2(t) = A\ \cos(\omega_2 t) \tag{4.14}$$

$$\begin{aligned} s_3(t) &= s_1(t)\ s_2(t) \\ &= \frac{A^2}{2}(\cos((\omega_1 - \omega_2)t) + \cos((\omega_1 + \omega_2)t)) \end{aligned} \tag{4.15}$$

Such nonlinear networks will introduce higher order products to a signal $s(t)$ incident on the network:

$$s_{NL}(t) = a_0 + a_1 s(t) + a_2 s(t)^2 + a_3 s(t)^3 + ... \tag{4.16}$$

For a simple three port diode mixer acting as an up-converter, the input signal $s(t)$ can be represented as the sum of the IF and LO signals[47]. The output of the nonlinear mixer s_{NL} will then contain mixing products of varying orders:

$$s(t) = A_{IF}\cos(\omega_{IF}t) + A_{LO}\cos(\omega_{LO}t) \tag{4.17}$$

$$\begin{aligned} s_{NL}(t) = {} & a_0 + \frac{1}{2}a_2A_{\mathrm{IF}}^2 + \frac{1}{2}a_2A_{\mathrm{LO}}^2 + \frac{3}{2}a_3A_{\mathrm{IF}}^2A_{\mathrm{LO}}\cos(t\omega_{\mathrm{LO}}) + \frac{3}{2}a_3A_{\mathrm{IF}}A_{\mathrm{LO}}^2\cos(t\omega_{\mathrm{IF}}) + \\ & a_1A_{\mathrm{IF}}\cos(t\omega_{\mathrm{IF}}) + a_1A_{\mathrm{LO}}\cos(t\omega_{\mathrm{LO}}) + \frac{3}{4}a_3A_{\mathrm{IF}}^3\cos(t\omega_{\mathrm{IF}}) + \frac{3}{4}a_3A_{\mathrm{LO}}^3\cos(t\omega_{\mathrm{LO}}) + \\ & a_2A_{\mathrm{IF}}A_{\mathrm{LO}}\cos(t\omega_{\mathrm{IF}} - t\omega_{\mathrm{LO}}) + a_2A_{\mathrm{IF}}A_{\mathrm{LO}}\cos(t\omega_{\mathrm{IF}} + t\omega_{\mathrm{LO}}) + \frac{1}{2}a_2A_{\mathrm{IF}}^2\cos(2t\omega_{\mathrm{IF}}) + \\ & \frac{1}{2}a_2A_{\mathrm{LO}}^2\cos(2t\omega_{\mathrm{LO}}) + \frac{3}{4}a_3A_{\mathrm{IF}}^2A_{\mathrm{LO}}\cos(2t\omega_{\mathrm{IF}} - t\omega_{\mathrm{LO}}) + \\ & \frac{3}{4}a_3A_{\mathrm{IF}}^2A_{\mathrm{LO}}\cos(2t\omega_{\mathrm{IF}} + t\omega_{\mathrm{LO}}) + \frac{3}{4}a_3A_{\mathrm{IF}}A_{\mathrm{LO}}^2\cos(t\omega_{\mathrm{IF}} - 2t\omega_{\mathrm{LO}}) + \\ & \frac{3}{4}a_3A_{\mathrm{IF}}A_{\mathrm{LO}}^2\cos(t\omega_{\mathrm{IF}} + 2t\omega_{\mathrm{LO}}) + \frac{1}{4}a_3A_{\mathrm{IF}}^3\cos(3t\omega_{\mathrm{IF}}) + \frac{1}{4}a_3A_{\mathrm{LO}}^3\cos(3t\omega_{\mathrm{LO}}) + ... \end{aligned} \tag{4.18}$$

In normal mixer operation the $\omega_{IF} \pm \omega_{LO}$ second order mixing products are the desired signals and lower and higher order products are typically unwanted signals referred to as intermodulation distortion (IMD). When operating over a fixed bandwidth it is possible for IMDs to exist in the desired band which causes the issues previously mentioned. The lowest band in the up-converter design for example overlaps with the operating band of the DAC, the IF signal band, which persists through to the output as a first order product. Figure 4.9 shows the output of a reference system using the same mixer as the final design[13]. The input signal is a chirp from 500 MHz to 2700 MHz, the LO is stable at 4.5 GHz, and the desired output signal sweeps down from 4 GHz to 1.8 GHz. In this figure the largest IMD is the first order IF passthrough product around 35 dB below the ideal second order difference product. The first order ω_{LO} passthrough product sits 500 MHz

above the band as designed, while the $2\omega_{IF}$, $\omega_{LO} - 2\omega_{IF}$, and $\omega_{LO} - 3\omega_{IF}$ products are visible crossing the in-band region.

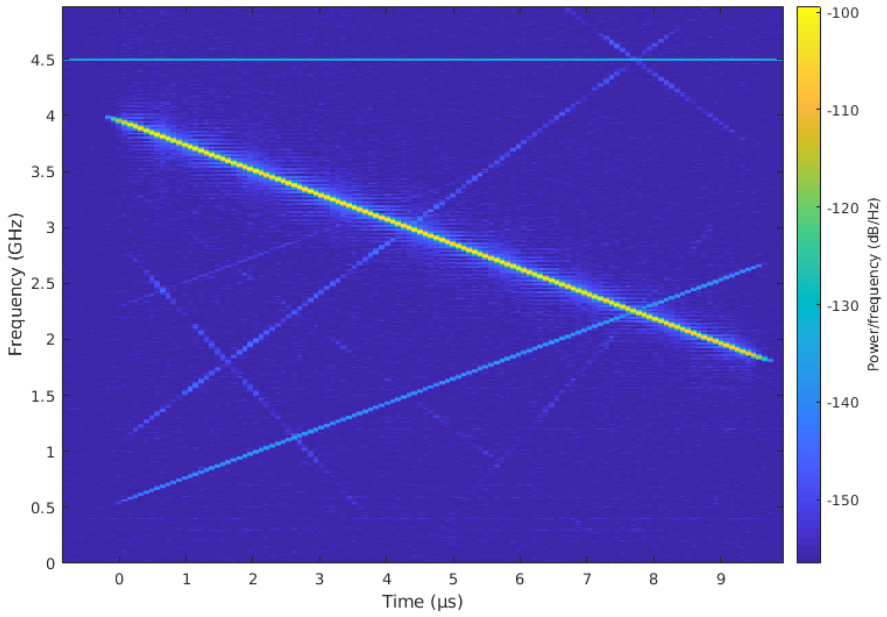

Figure 4.9: 10 µs chirp up-converted to lowest operating band using reference mixer system.

Out-of-band products can be filtered out as long as a filter can be designed that keeps the products and signal in their respective stop-bands and pass-bands. In-band products on the other hand cannot be easily filtered out, as any linear filter will also affect the desired signal and wideband nonlinear filter design is nontrivial. Some of the noise from these products can be removed post-acquisition during the coherent noise removal process, but that assumes enough data is taken to achieve the necessary averaging. Some spurs, such as the chirps with integer multiples of the original signal chirp rate, will create images stretched in range relative to the desired target that can be difficult to remove in the post processing.

With the use of an AWG like a high speed DAC it is possible to attenuate in-band IMD by including an out-of-phase image of the expected IMD product in the input signal to interact destructively once mixed. To take the mixer output displayed in Figure 4.9 as an example, the strongest IMD is the feedthrough ω_{IF} product around 30 dB below the ideal output chirp. There are also the $2\omega_{IF}$, $\omega_{LO} - 2\omega_{IF}$, and $\omega_{LO} - 3\omega_{IF}$ products appearing more than 40 dB below along with

some other, further attenuated products. A π-out-of-phase chirp from 4 GHz down to 1.8 GHz is included in the IF signal 30 dB below the main 500 MHz to 2.7 GHz chirp would be expected to interfere destructively with the mixer product.

In practice, however, the actual mixer products are not perfect harmonics and do not have a uniform gain or perfectly linear phase across the chirp bandwidth. From experimentation, generating a pure harmonic to cancel out the mixer product only eliminates certain small regions of the IMD, with some sections becoming worse due to in-phase combining or the IMD frequency being slightly off from expected. Making mixer product minimization viable would require accounting for the phase and amplitude variations as a function of frequency and developing a more precise model of the IMD than just a simple harmonic. The implementation would probably be best served through the pattern playback method as opposed to the DDS, as the DDS would require an extra DDS channel and extra normalization patterns to account for the different IMD gain. The mixer LO would also need to have high stability to properly account for the phase changes.

4.2.3 Beam Forming

As described in Chapter 2 this system will have multiple independently driven transmit and receive channels, each channel connected to an element in the antenna arrays described in Chapter 3. This configuration will be used to drive each antenna element independently to steer the main lobe of the array, with the signal variations needed to accomplish this being carried out digitally during either the initial signal generation or the response capture. This means that no control signals will be needed to modify the analog sections, which reduces complexity of assembly and operation. Controlling the radiation pattern of an antenna array is done by modifying the phase and amplitude of the signals incident on the antenna elements. This can be shown by deriving the array factor AF, which is the term that shows the behavior of an array is dependent on the geometry of the array and relative phases of driven elements in that geometry. For a given point in space r in the Fraunhofer

region, the field at that point due to a single radiating antenna at the origin is given by

$$E = F(\theta,\phi)A(r)e^{-ik\cdot r}, \tag{4.19}$$

where $F(\theta,\phi)$ represents the radiation pattern of that antenna, $A(r)$ represents the amplitude term, k is the wavenumber, and β is the phase. For a linear array of identical antenna elements like what is presented in Chapter 3, the total field due to the array of antennas is equivalent to the summation of terms for each element

$$E_{tot} = F(\theta,\phi)\sum_{n}^{N} A_n(r)e^{-i(k\cdot r_n+\beta_n)}, \tag{4.20}$$

where β_n is the excitation phase for an individual element relative to adjacent elements, and n represents the index of the element in the array of N total elements. Here the amplitude and distance terms become dependent on the geometry. Assuming a linear array in the Fraunhofer region along the z-axis of constant spacing d and constant phase increment $n\cdot\beta$, $A_n(r)$ becomes $A_c(r)A_n$ and $r_n \simeq r + nd\cos(\theta)$ where θ is the angle relative to the z-axis. With the Fraunhofer approximation, the relative amplitude difference due to array spacing can be assumed 0 and the e^{-ir} term can be pulled out of the sum and integrated into the constant amplitude term $A_c(r)$.

$$E_{tot} = F(\theta,\phi)A_c(r)\sum_{n}^{N} A_n e^{-in(kd\cos(\theta)+\beta)} \tag{4.21}$$

The radiation pattern for the array then is a product of the radiation pattern for a single element and the array factor.

$$F_{arr} = F(\theta,\phi)\sum_{n}^{N} A_n e^{-in(kd\cos(\theta)+\beta)} \tag{4.22}$$

$$= F(\theta,\phi)\cdot AF \tag{4.23}$$

This was a quick derivation of the array factor for this linear array to pull out which terms affect what aspect of the radiation pattern. To give an example, consider an 8-element, z-axis array of parallel dipoles oriented along the x-axis spaced $\frac{\lambda}{2}$ apart. In Figures 4.10 and 4.11 the radiation pattern normalized to a unit dipole for that configuration is plotted using two different phase increments to show how phase controls the steering angle. With regards to amplitude, a uniform amplitude distri-

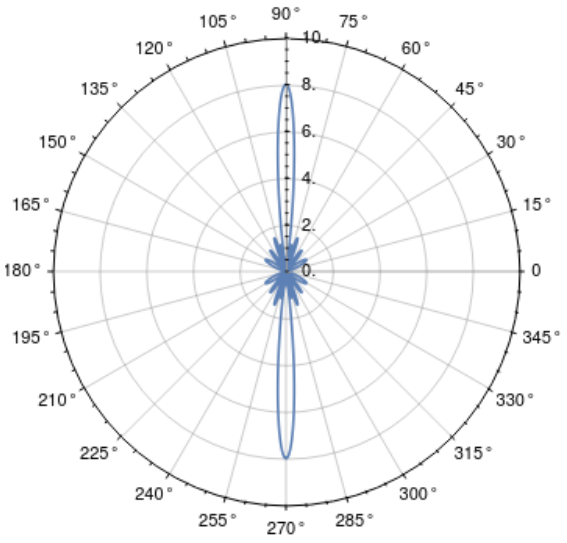

Figure 4.10: Radiation pattern when array is steered broadside, along the y-axis. $\beta = 0$

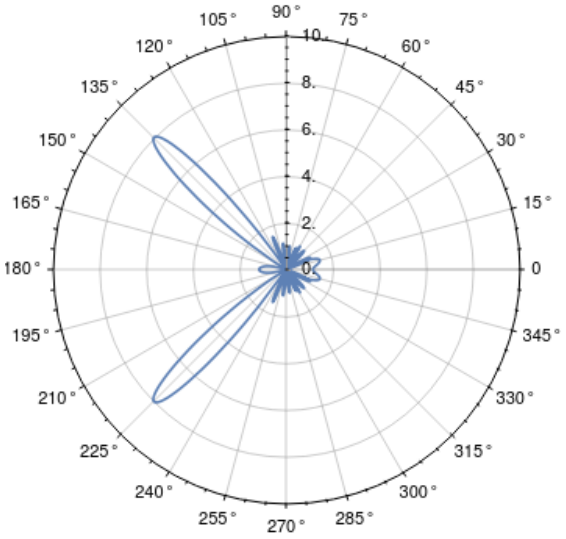

Figure 4.11: Radiation pattern when array is steered 45°off the y-axis in the yz plane, $\beta = \frac{\pi}{\sqrt{2}}$.

bution across the elements will produce the tightest main-lobe beamwidth, but other distributions such as the binomial distribution can be used to reduce side-lobe levels at the cost of broadening the main beam. This is effectively applying a windowing function to the spatial filter that is the array [24].

For the antenna array used by this radar system, control over the amplitude distribution and phase variation is handled entirely in the digital domain. Doing so digitally provides several benefits over hardware implementations. While control over the amplitude distribution can be achieved through variable-gain amplifiers and attenuators, such implementations require calibration, and potentially continuous adjustments, across the operating bandwidth to ensure the desired distribution. Use of switched attenuator banks also prevents more precise control over the distribution.

For the linear array outlined above, steering the main-lobe to an angle θ_0 through phase shifting requires producing an inter-element phase shift of $\beta = -kd\cos(\theta_0)$. As $k = \frac{2\pi}{\lambda}$, β varies linearly with frequency and in the case of a linear FM signal, linearly with time.

$$\beta(t) = -2\pi f(t)\frac{d}{c}\cos(\theta_0) \tag{4.24}$$

The term $\frac{d}{c}\cos(\theta_0)$ corresponds to the difference in time it takes for a plane wave originating from an angle θ_0 to reach adjacent elements. The dependence on this term means that frequency independent steering can also be accomplished using a time delay of identical signals. For a wideband signal it is important to account for this frequency shift, otherwise spreading of the main beam occurs. Accounting for this frequency shift using hardware phase shifters can be difficult, as things like switched filter networks, ferrite phase shifters, and variable load transmission lines result in discrete phase control which prevents fine control over immediate steering angle across frequencies. Using switched delay lines to introduce a time delay solve this issue, but the set of possible steering angles is limited by the space available to hold the delay lines.

The following sections 4.2.3.2 and 4.2.3.1 present the methods used to steer wide-band signals during signal generation and after dechirping.

4.2.3.1 Steering on Transmit

Steering on transmit involves applying the necessary time shift to the transmitted sequence before those values are passed to the DAC. Because of the calibration step and board skew, a time shift is already applied to account for the board skew and converter synchronization.

For pattern playback it is as simple as including the extra time offset when generating the chirp pattern, assuming an independent pattern is generated for each channel. If only a single channel is used then time delays can only occur in multiples of the sampling period and a shift register would be needed to carry over the necessary samples for each channel. At 6.4 GS/s the sampling period is 156.25 ps, which is too course of a time resolution to allow for fine steering.

Implementing a time delay in the DDS is the operation described in Equation 4.9. Each channel's initial tuning word and phase accumulator are changed to that of a DDS shifted by the desired delay. Given the 16 sample resolution of the normalization pattern no changes are needed to its timing, the time delays used for steering are small in comparison. If a spatial array weighting is to be applied across the array then that can be done either by using different normalization patterns or by adding an extra scalar multiplication stage after the single channel normalization pipeline.

While the necessary calibration and delay management was implemented and tested, steering on transmit was not successfully tested in this system due to the difficulty involved in achieving a precise calibration across tiles.

4.2.3.2 Steering on Receive

Since MTS is not functional the only way to align the ADCs across tiles is to generate synchronous calibration pulses to each ADC every time the converters are initialized. To do so without manually changing the internal radar connections would require an external RF switch to select the calibration source and the receiver IF port. Fortunately steering on receive is still possible despite the lack of ADC calibration. This is possible because the difference in phase introduced between elements is large relative to the phase error introduced by the unsynchronized ADCs.

The following derivation of the time-domain dechirping process demonstrates how this phase is carried through to the IF at the receiver output.

Consider a chirp $g(t)$ and a target at range R. The round trip delay for the transmitted signal q assumes a monostatic transmit and receive antenna array with respect to the plane of steering.

$$g(t) = \sin\left(2\pi\left(f_0 t + \frac{k}{2}t^2\right)\right) \tag{4.25}$$

$$q = \frac{2R}{c} \tag{4.26}$$

The IF signal for a single target at the output of the mixer is the product of the reference chirp (ignoring intentional delays) and a delayed copy of that chirp corresponding to the time of flight

out to the target and back to the receive antenna. The returned signal is always attenuated relative to the transmit signal and the strength of the return is dependent on the scene and the antenna performance, but for the following calculations all amplitude terms are discarded.

$$if(t) = g(t) \times g(t-q) \tag{4.27}$$

$$= \frac{1}{2}\sin\left(2\pi\left(\left(f_0 t + \frac{k}{2}t^2\right) - \left(f_0(t-q) + \frac{k}{2}(t-q)^2\right)\right)\right) \tag{4.28}$$

$$-\frac{1}{2}\sin\left(2\pi\left(\left(f_0 t + \frac{k}{2}t^2\right) + \left(f_0(t-q) + \frac{k}{2}(t-q)^2\right)\right)\right)$$

$$= if_+(t) + if_-(t) \tag{4.29}$$

Only the difference mixer product $if_-(t)$ is considered; the sum product $if_+(t)$ would be filtered out as it is far outside the operating bandwidth of the IF chain. Other mixer products resulting from nonlinear behavior are ignored as well.

$$if_-(t) = \frac{1}{2}\sin\left(2\pi\left(\left(f_0 t + \frac{k}{2}t^2\right) - \left(f_0(t-q) + \frac{k}{2}(t-q)^2\right)\right)\right) \tag{4.30}$$

$$= \frac{1}{2}\sin\left(2\pi\left(kqt + \frac{k}{2}q^2 + f_0 q\right)\right) \tag{4.31}$$

For targets off bore-sight of the antenna array an extra time delay is introduced between elements of the array to account for the total path difference of the signal. This relies on the planar wave approximation assuming a single far-field target and ignores the phase center variations of the array elements. It also assumes that the reference chirp provided to each receiver is identical, which implies that in a situation where the transmit signal is steered as well a separate channel must be used to provide the coherent reference signal.

$$if_-(t)_n = \frac{1}{2}\sin\left(2\pi\left(kt\left(q + \frac{d\cos(\theta)}{c}\right) + \frac{k}{2}\left(q + \frac{d\cos(\theta)}{c}\right)^2 + f_0\left(q + \frac{d\cos(\theta)}{c}\right)\right)\right) \tag{4.32}$$

Like earlier the angle θ is the angle of steering relative to the array axis. Expanding and rearranging

the phase of the IF highlights the array dependent phase terms that appear.

$$2\pi\left(\left(kqt+\frac{kq^2}{2}+f_0q\right)+\underbrace{\frac{kd}{c}\cos(\theta)t}_{\text{Frequency offset}}+\underbrace{\frac{kd}{c}\cos(\theta)q}_{\text{Time offset}}+\frac{d^2}{c^2}\cos^2(\theta)+\underbrace{\frac{d}{c}\cos(\theta)f_0}_{\text{Phase offset}}\right) \tag{4.33}$$

Left to right, the first three terms in parenthesis are that of an IF unaffected by any steering.

The first term following those represents the shift in frequency expected from a target that is slightly closer or farther depending on its position relative to the specific array element. This value is maximized when a target is completely in line with the array, $\theta = 0^\circ$. For an array with 3 cm spacing the variation between adjacent elements will never exceed ± 22 kHz assuming a 10 µs 2.2 GHz chirp. This chirp bandwidth will have a maximum range resolution of 6.8 cm and will be incapable of resolving the exact range variation between immediately adjacent elements.

The next term affecting the phase comes from the time delay due to the array geometry dependent arrival. The same concept that applies to the frequency shift applies here, the maximum time delay difference between adjacent elements for a 3 cm array will never exceed 100 ps, which would require a sampling frequency exceeding 10 GS/s to distinguish individual elements.

The third term can be disregarded as it is on the order of 10^{-20}. The final term, labeled phase offset, is the term that allows for steering on receive without proper ADC synchronization. With an f_0 of 5 GHz, for example, the phase shifts by ± 0.42 rad as the steering angle sweeps from 60° to 120° off the array axis. Obviously this phase is dependent on the target frequency, which results in higher (target) frequencies seeing a smaller proportional time shift. To demonstrate, shifting a 2 MHz signal by 0.42 rad corresponds to a time shift of 33 ns while a 50 MHz signal shifted by the same phase would correspond to a time shift of 1.3 ns. ADCs with effective sampling rates of 250 MS/s can only resolve 4 ns differences, and from systems tests the error in timing between each corresponds to approximately ± 2 ns. This means steering resolution is reduced for greater target ranges.

All steering in this work is done in post processing and the results are presented in section 5.1.

A linear phase gradient is applied across the output of the FFT of the return for each channel and then all channels are summed to produce the range product for a single steering angle. If azimuthal spatial distortion is acceptable then a constant time shift can be applied in place of the linear phase gradient, which will map greater ranges into a smaller sector. There is no benefit beyond the reduced resource usage of the constant time shift.

4.2.4 Stretch Processing

In section 2.4.3 it is discussed how the receiver IF can be shifted in frequency by adjusting the length of the reference path that feeds a copy of the transmitted signal to the receiver for dechirping. There it was discussed in the context of reducing the effect of antenna feedthrough and other clutter in close proximity to the antennas.

The purpose of the reference path length adjustment is to introduce a time delay in the reference signal. The time delay from a fixed physical path obviously can not be adjusted during operation and introduces loss from the required length of cable. Both of these issues can be solved by using an extra transmit channel to produce the reference signal with the desired delay digitally. The digital delay can be easily changed during operation with high precision in the same way that is done for the calibration and beam steering.

With the limited number of DACs on the RFSoC an extra channel is not available if all eight channels are used for steering on transmit. A smaller or sparser transmit array would be needed to free up a channel to provide the reference signal.

If the total delay is greater than the LFM pulse width then noise from antenna feedthrough is no longer a concern, and the largest source of feedthrough noise is dependent on the isolation between the reference transmitter and the receivers. With such a delay it is also possible for the radar to operate in a monostatic configuration with a single antenna array, making use of a transmit/receive switch [63].

As the delay is generated digitally it can be adjusted rapidly to keep the target within the narrow bandwidth of the IF. This would involve a range tracking setup with a feedback loop. A simple

implementation would consist of a peak detector that continuously tracks the target peak in the FFT of the responses. As the peak drifts out of a preset range the delay would be proportionally updated to re-center the target. The updated delay would then be stored with the chirp to serve as a range reference point. This setup could be done in the processor or in the FPGA depending on the required response time and available resources [64].

4.3 Response Capture and Processing

The IF as produced at the output of the receivers is connected directly to the ADC ports on the carrier board. These ports have a matching network identical to that of the DAC interfaces. As mentioned in Section 2.2.1 these networks should have, in theory, around 4 dB of insertion loss, but in practice they demonstrate up to a little more than twice that. The 12 bit ADCs have a full scale input signal power of 1 dBm at their input with an absolute maximum input power of 3 dBm [12]. Each ADC tile is provided a 400 MHz reference clock and an internal PLL is used to produce a 2 GS/s sample clock. Internal 8x FIR decimation filters are enabled to reduce the effective sample rate to 250 MS/s and eliminate spurs in the higher Nyquist zones. The corresponding Nyquist frequency for the decimated output sits above the stop band of the receiver IF low pass filter. 2500 samples are captured from each ADC every 10 µs chirp. Each sample is 12 bits of data aligned in 16 bit words so 5 kB of uncompacted data is generated from each channel every chirp. If pre-summing is enabled then a separate buffer will be enabled to store the accumulation of the past n chirps for a pre-summing factor of nx. The word size in this buffer is increased to $12 + \log_2 n$ to accommodate the end sum. After pre-summing this data is temporarily stored in block RAM buffers in the PL before being transferred out to the DDR4 accessible to the PS. A processor interrupt is generated when the transfer is completed and a DMA SDIO transfer is initiated to dump the data out to a Micro SD card. The data transfer rate of the SD card is the limiting factor in the chain of memory transfers. Assuming no processing such as pre-summing or range gating takes place and there is a 50 MB/s maximum continuous SD write speed then the corresponding maximum PRF is 1250 Hz. In practice the data is pre-summed and depending on the application range gating may be used,

both of which significantly reduce the total data rate.

4.3.1 Digital Range Gating

As shown in Section 2.4.3 the maximum range for an LFM pulse with no extra processing is $\frac{T \cdot c}{2}$. A 10 µs pulse will have a maximum range of 1.5 km. Regardless of the degraded SNR at that range, a radar operating near ground level like this system does not need information from beyond the useful range. The maximum useful range for this system is in the tens of meters: the height of the system along with a few meters to account for the soil penetration depth. This is why returns from beyond 80 meter are increasingly attenuated with the low-pass filter in the receiver IF chain.

Discarding information from greater ranges can be done to reduce the data rate and allow for more efficient processing later on. Since greater ranges in an LFM system translate to higher frequencies, this can be achieved through decimation and filtering to discard the higher frequencies digitally. If the IF was sampled at the rate required to capture the maximum range IF, around 4 GS/s, then 80 kB of data would be generated on every channel for each pulse. At the desired operating PRF this starts to exceed DDR4 transfer bandwidths and is difficult to work around. If the ADCs could be clocked at lower speeds that would lower the data rate and reduce the Nyquist sampling frequency, but there is a benefit to oversampling at the ADC input and relying on digital processing. By oversampling first and then decimating digitally, signals that would otherwise appear in the higher Nyquist zones of the final (desired) sampling rate would appear in the first Nyquist zone at the higher oversampling frequency and could then be digitally filtered out. This prevents them from being folded down into the first Nyquist zone at the input of the ADC and reduces the requirements on the receiver's low-pass filter. The ADCs in the RFSoC can only be clocked as low as 1 GS/s which means that at a minimum at least 5x oversampling will occur given the 100 MHz low-pass receiver filter.

To avoid processor dependent configuration of the ADC during operation, the ADCs are clocked at 2 GS/s and the maximum 8x internal FIR decimation is enabled. This results in an effective 250 MS/s at the output of the hard digital datapath, which makes the first Nyquist zone only slightly

larger than the maximum usable bandwidth at the output of the receiver. Any further band pass sampling can then be set in configurable filters implemented in the FPGA, which would not be processor dependent [65].

An alternative approach to using traditional decimation filters for range gating is to first switch to the frequency domain. By first applying a DFT to the sampled signal, specific frequencies (ranges) can be selected for (and others eliminated) simply by dropping the series of points outside the desired range. If one is willing to continue with only the single-sided spectrum and drop phase information then this method has half the total data storage requirements when compared to the output of a simple decimation filter. Bringing the DFT into the FPGA can save processing time if a DFT was expected to be performed later anyway, such as during post-processing. Having this information readily available also allows for fast peak detection, which can be used for target range estimation and altimetry. This becomes more useful if the system height is significantly variable to the degree that the target may fall out of the ranges set by the physical IF filter. Adjustment could then occur by changing the chirp rate to raise/lower the target IF frequency or by switching a filter bank on the receiver, if the receivers were designed with a switchable filter bank.

4.3.2 Stepped Chirp Processing

The dechirped outputs from each of the four bands this radar operates over are stored separately for later processing. On their own each chirp has a 2.2 GHz bandwidth, which produces a theoretical range resolution of around 6.8 cm. The four bands together span 6.9 GHz from 1.8 GHz to 8.7 GHz. A chirp with that bandwidth would have a theoretical range resolution of around 2.2 cm, three times the resolving capability of an individual band. With a band hopping system like this the individual sub-chirps can be combined to achieve a greater synthetic bandwidth that is proportional to the sum of the non-overlapping instantaneous bandwidths. The process can be performed in the time domain [66, 67] or the frequency domain [68], and with a different front-end architecture it can be performed either before or after the dechirp operation.

This system is set up to only allow for this processing digitally. Whether that occurs in real

time or is post-processed is implementation dependent, and for this test platform all processing was done in post. The steps used to synthesize the wideband chirp in the time domain are as follows:

1. Collect the time domain sequence of samples of the dechirped output for each band. This sequence can be the raw data or after processing for beam steering.

2. Apply phase correction to $n-1$ of the sequences to align their phase across bands.

3. Optionally normalize the total energy of each sequence to compensate for band dependent gain variations in the RF chain.

4. Window each sequence so that no sharp transitions between bands occur during the next step. A Tukey window is used and the tapers of the window are aligned with the time domain regions of the bands that overlap in frequency with an adjacent band.

5. Concatenate the sequences in order of increasing band center frequency to simulate the shift in time.

6. Apply a DFT to the concatenated sequence.

While all tests and intended applications of this radar rely on the assumption of a completely static scene, [69] provides a review of the various processing methods and proposes new compensation methods for non-static scenes.

Interestingly, [68] discusses stepped chirp waveforms in the context of avoiding time domain steering under the presumption of high cost of implementation, something this system avoids through the advantage of the data converter banks in the RFSoC. While this system uses a stepped chirp system in the pursuit of reduced cost as well, the driving factor is not the time domain steering but the avoidance of the second down conversion chain discussed in Section 2.2.

The results of the resolution improvement through the synthetic bandwidth of the combined chirps are presented in Section 5.1.1.2.

Chapter 5

Results and Conclusion

Throughout this work individual components were tested, characterized, and validated, typically in isolation from each other. This chapter presents the tests and results of the full system operating as a radar in a test environment. Future work on the system is presented as well, discussing the characterization, improvements, and potential future actions that should be taken to bring this radar out of the demonstrator stage and into operation as an active sensor platform.

The original goal was to have a system capable of beam steering on both transmit and receive. For the reasons given in 4.2.3.1 the goal of steering on transmit was put on hiatus until those issues are resolved. The storage restriction was not resolved either and all test results were acquired at a lower PRF (100 Hz) than the originally planned PRF of 1 kHz. In all the following presented results the waveform generated by the DAC is a normalized chirp with a 10% Tukey window. The same normalization pattern was used across all channels, so the variations present in Figure 2.4 would apply to the waveforms as well.

Operation of the radar was controlled by a nearby laptop through the UART interface to the carrier board. A simple shell was implemented on one of the RFSoC's ARM cores that took commands from the UART for configuring and operating the radar.

5.1 Testing and Performance

Bringing the radar to a functional test state was separated into multiple stages to avoid damage to any one component. Once the power sequencing capability of the RFSoC and synthesizer board was validated the transmitter modules were connected. The output power of the reference signal

used for the receiver LO was checked to prevent damage to the receiver mixer. Normalization was then carried out following the procedure described in Section 4.2.1. The receiver modules were then powered on, the antenna input port was terminated, and the reference path from the transmitter was connected to check noise levels from the receiver. Delay line tests were then carried out with an oscilloscope in place of the ADC to check the range of power to be expected at the output of the receiver module. Once validated the whole system was connected and full system testing began.

5.1.1 Delay Line Tests

Output from initial delay line testing was captured using a 20 GS/s oscilloscope to avoid damage to the ADC in the event that insufficient attenuation was included in the delay line. The final stage amplifier in the IF chain has a 1 dB compression point at 3.7 dBm [70] which indicates the amplifier is capable of exceeding the absolute maximum ratings of the ADC when saturated. To compensate for this in later tests a 10 dB attenuator is placed at the IF output to serve as an extra protection against destroying the ADC.

The delay line used was formed with the 8.23 m length of low-loss cable used for antenna testing along with a 2 m length of cable, three discrete connectorized attenuators, and two 14" flex-rigid cables all connected using female-female SMA adapters. The three attenuators provided 60 dB of attenuation and the cables provided an extra 5 dB to 11 dB of insertion loss across the band, as displayed in Figure 5.1.

A 10 µs chirp was transmitted across band 2 at 3 dBm. The extra 2 m cable was added and removed to test range discrimination, the results of which are shown in Figures 5.2 and 5.3.

Figure 5.2 shows the target returns out to 150 MHz to highlight the visible roll-off of the 100 MHz IF filter and to establish the clear noise floor just below -70 dBm. The actual targets are the focus of Figure 5.3.

In this test there is no antenna; the transmit and receive are directly connected through the delay line and the LO path is a 3.5" cable. The peaks for the two targets appear at 8.15 MHz and 9.85 MHz. With the chirp rate used those correspond to time-of-flights of 39.6 ns and 47.9 ns

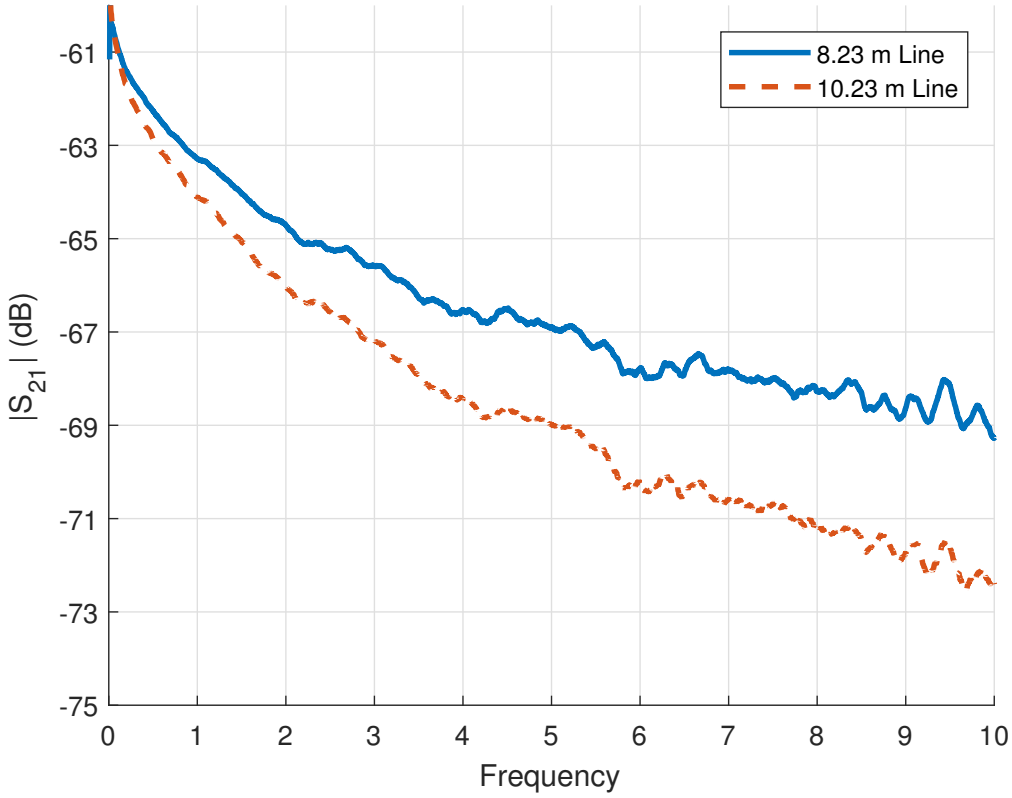

Figure 5.1: The $|S_{21}|$ of the delay line with and without the extra 2 m cable.

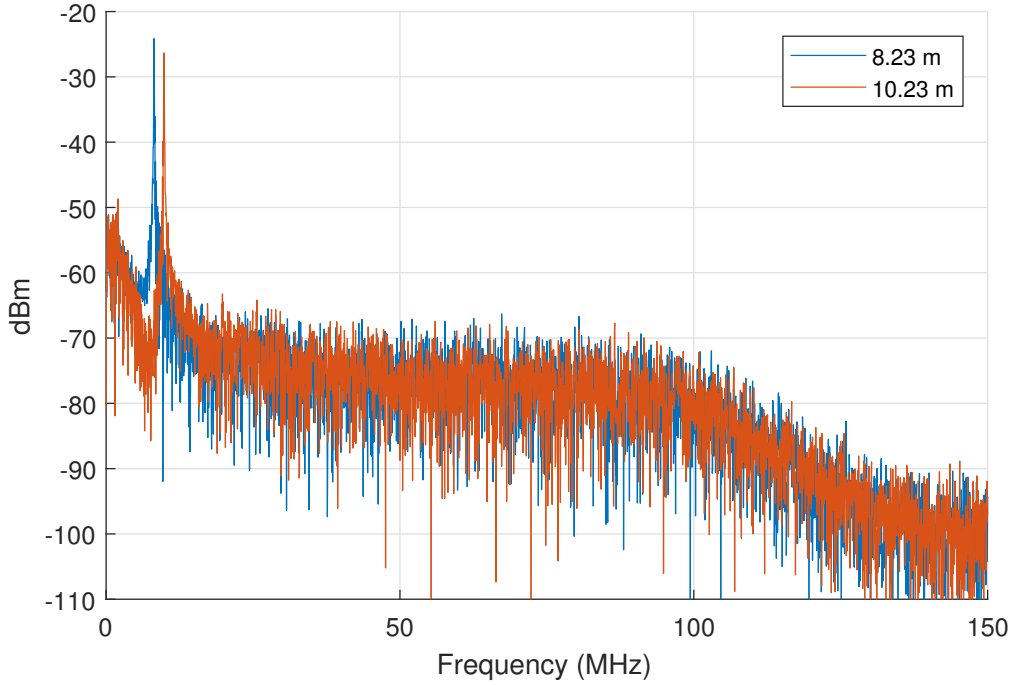

Figure 5.2: Initial single-channel delay line tests in band 2 using two cable lengths. Transmit power of 0 dBm and total attenuation of around 68 dB.

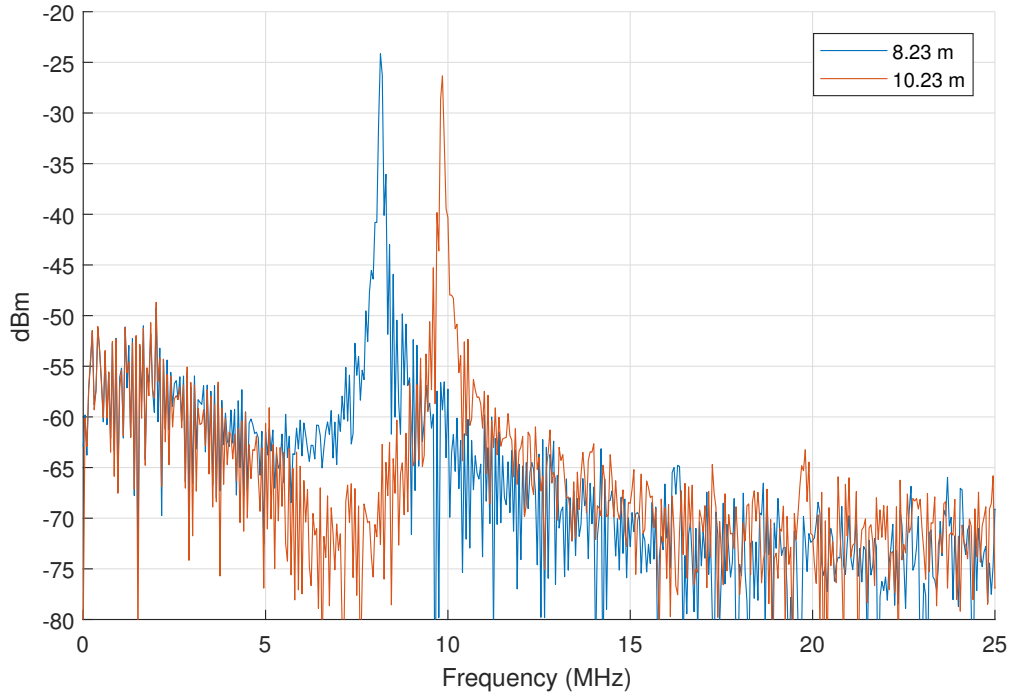

Figure 5.3: Initial single-channel delay line tests in band 2 using two cable lengths. Transmit power of 0 dBm and total attenuation of around 68 dB.

respectively. With the known lengths of 8.23 m and 10.23 m, the effective speeds of propagation are 0.69c and 0.71c, which line up with the expected speed of propagation of 0.70c from the datasheet of the 8.23 m length of cable.

Leakage between the receive and reference paths is apparent given the linear ramp 15 dB down to the noise floor from DC to 7 MHz. This is consistent across all measurements taken so far and is most likely due to the level of isolation between the two paths on the receiver board. In this initial test there was no physical isolation between the two boards and they were placed side by side on the same anti-static mat. Later tests had the aluminum mounting structure inserted in between.

Beyond 7 MHz the SNR approaches 40 dB however, which is adequate given the existing 60-70 dB of insertion loss from the delay line.

5.1.1.1 Full System Tests

The previous delay line results confirmed that the output signal power would not exceed the absolute maximum of the ADC, but a 10 dB attenuator was included regardless as a means of being

overly cautious. The added attenuator results in fewer effective bits in the detector given that the expected maximum signal power will not reach full-scale range; only around 4-7 bits are actually used across all bands. This is compensated for in part by pre-summing, or taking multiple coherent samples of the same target and summing them. Pre-summing serves as a means to increase the pulse-compression gain (Eq. 5.1 [28]) through a synthetic increase in the pulse duration τ.

$$G_{pcomp} = \frac{SNR_{out}}{SNR_{in}} = \tau BW \tag{5.1}$$

The results in Figure 5.4 have been pre-summed 50 times to compensate for the reduced effective bits and to bring out the side-lobes that would otherwise be buried beneath noise.

The amount of band-dependent roll-off is within the expected range. The feedthrough return is strongest in the lowest band, and weakest in the greatest band. RF-LO isolation in the mixer is lowest across that band, so the LO isolation from the RF frontend of the receiver must be lower at that frequency. The first explicitly defined sidelobes appear around 25 dB down from the target peak. From Section 4.2.1.1 the sidelobes are expected to show up around 10-15 dB down, but due to the limited range resolution of the system they appear here as broadening of the main lobe.

While the return corresponding to twice the delay-line length is present in all bands, it is strongest in the first and third bands. This response is caused by a reflection first by something near the receiver input port and then again by something near the transmitter output port before the reflection passes through the attenuator block. The spacing between the pair of reflections visible in band 3 suggests it may be due to the adapters used to connect the different cables. An extra target appears around the 50th range bin in the 10.23 delay line. It is the correct range for a sub-harmonic of the mixer, however no such harmonic is measured at the output and there is no corresponding product on the shorter delay line, which implies it may be the result of a physical change in the delay line.

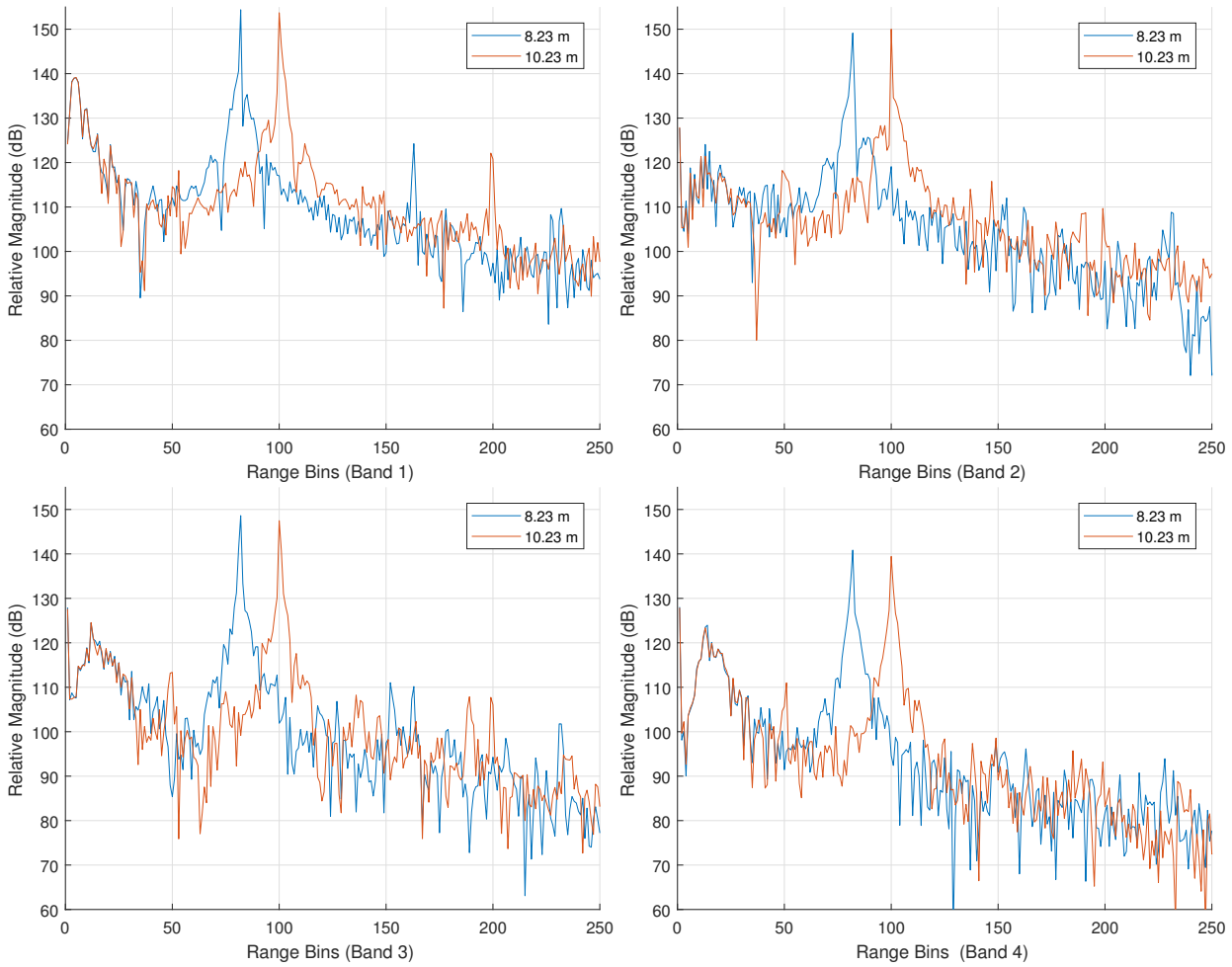

Figure 5.4: Delay line test for all four bands in normal operation (captured by ADC as opposed to scope).

5.1.1.2 Synthetic Resolution

Carrying out the process described in Section 4.3.2 allows for improved resolution through combining the response from each band. Figures 5.5 and 5.6 compare the resolved features between the first band response and the synthetic bandwidth product. In Figure 5.5 it is apparent that there are targets present that may not register in a single band. Looking only at the delay line target the side-lobes are well defined and the 3 dB width of the target peak is reduced. The SNR is improved in line with the increase in the time-bandwidth product as well.

The process of combining the responses to form the synthetic bandwidth is a source of side-lobes as well, given the ripple in amplitude introduced by stitching together the responses from

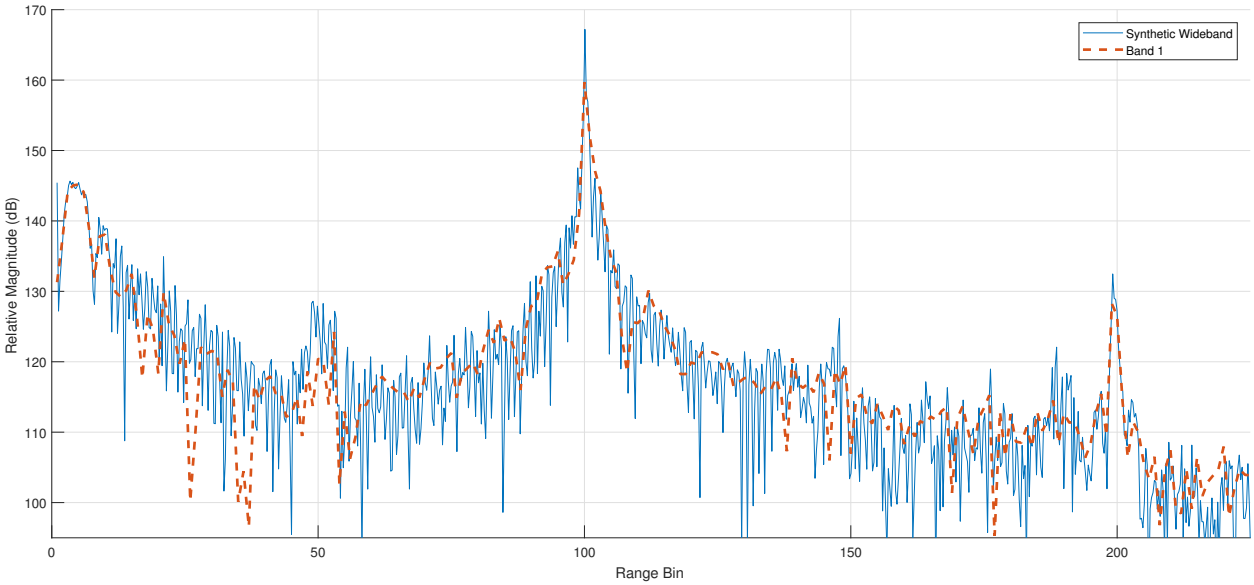

Figure 5.5: Single band response and combined band response of the 10.23 m delay line.

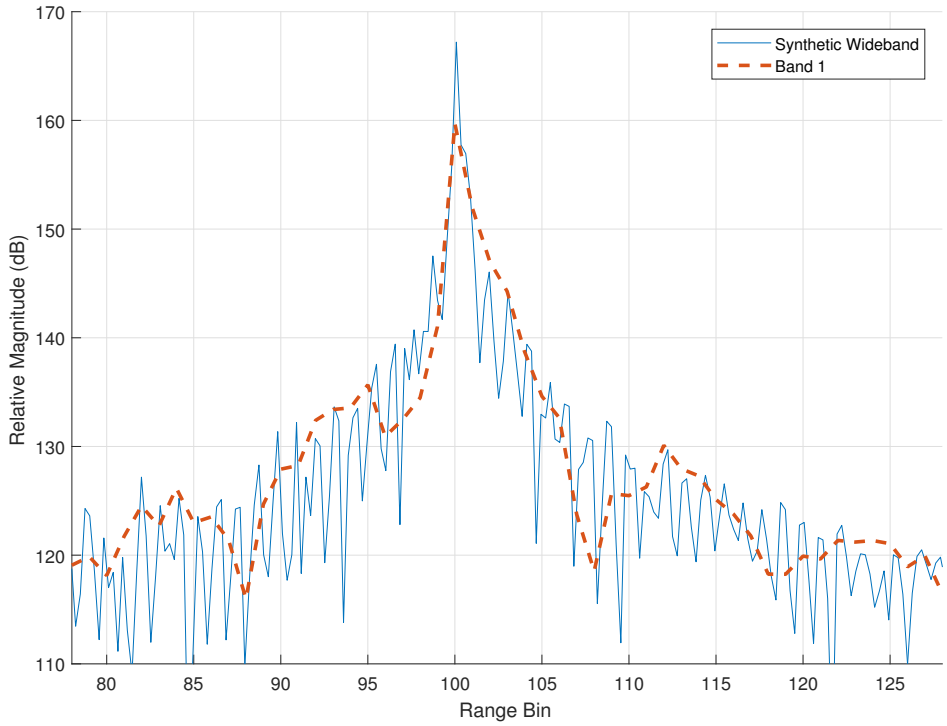

Figure 5.6: Single band response and combined band response of the 10.23 m delay line.

each band. To help establish the difference between the sidelobes and targets the delay line setup was measured with a VNA and overlaid with the synthetic bandwidth product in Figure 5.7. The first explicit peak after the target is visible in the VNA measurement as well implying it may be a

physical return from the delay line, possibly a reflection between the attenuators. The small peaks before the target however are not visible and should be considered range sidelobes. The radar also shows several targets that are not seen in the VNA measurement such as the half-range target mentioned earlier. Extra cables were present during the VNA measurement which might change the match that is otherwise presented by the radar ports.

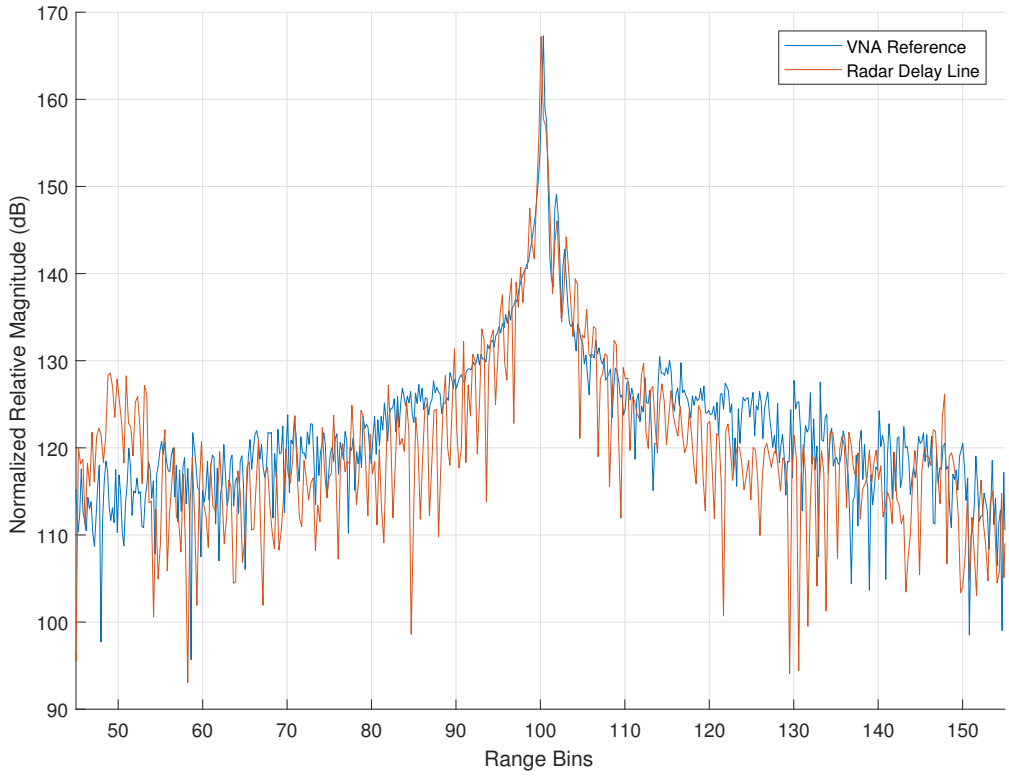

Figure 5.7: 10.23 m delay line as measured by the radar and by a 26 GHz VNA. The VNA measurement has been normalized and aligned with the radar target response to compensate for the added cables.

5.1.2 Static Single Target

The targets in the following tests are copper pipes 35.5 cm long and 5.4 cm in diameter. Copper pipes were chosen as the target as they approximate a PEC cylinder, which has a well defined RCS that is easily approximated by Equation 5.2 from [71]. This assumes the length of the cylinder is

oriented vertically and the bistatic scatterometer is VV polarized.

$$\sigma \approx \left(\frac{2l^2}{\lambda}\right)\left(\frac{2\lambda}{\pi}\right)\left|\sum_{n=0}^{+\infty}\varepsilon_n \frac{J_n(\beta a)}{H_n^{(2)}(\beta a)}\cos(n\phi)\right|^2 \tag{5.2}$$

$$\varepsilon_n = \begin{cases} 1, & n = 0 \\ 2, & n \neq 0 \end{cases}$$

a =Radius of cylinder

l =Length of cylinder

λ =Wavelength of incident wave

ϕ =Bistatic scattering angle

β =Phase constant $(\frac{2\pi}{\lambda})$

J_n =Bessel function of the first kind

$H_n^{(2)}$ =Hankel function of the second kind

In all tests the centers of the antenna arrays are spaced 28 cm apart. The target was placed 2 m from the antennas yielding a bistatic scattering angle of 8° from the center of the transmit array to the center of the receive array. At greater ranges and off-center angles this angle goes to zero. Figure 5.8 shows the range of RCS values this bistatic angle sweeps out.

The test setup used to take the measurement is described in Appendix D.

Figure 5.9 contains the results of the single static cylinder target test presented per band. The data presented is the unprocessed sum of the eight channels across 16 pre-sums. From an initial glance the apparent roll-off of the response across the bands is in line with the 8 dB roll-off due to the normalized transmit bands along with the further 9 dB in roll-off in the receiver LNA. The consistent peak around the 57th range bin is where the ceiling of the test room is expected to appear. An informal verification of said peak's identity was carried out by re-running the test with RF-absorbing foam placed above the antenna elements in the direct path to the ceiling: the return lowered by around 30 dB with minimal effect on the other range returns. The target is present at

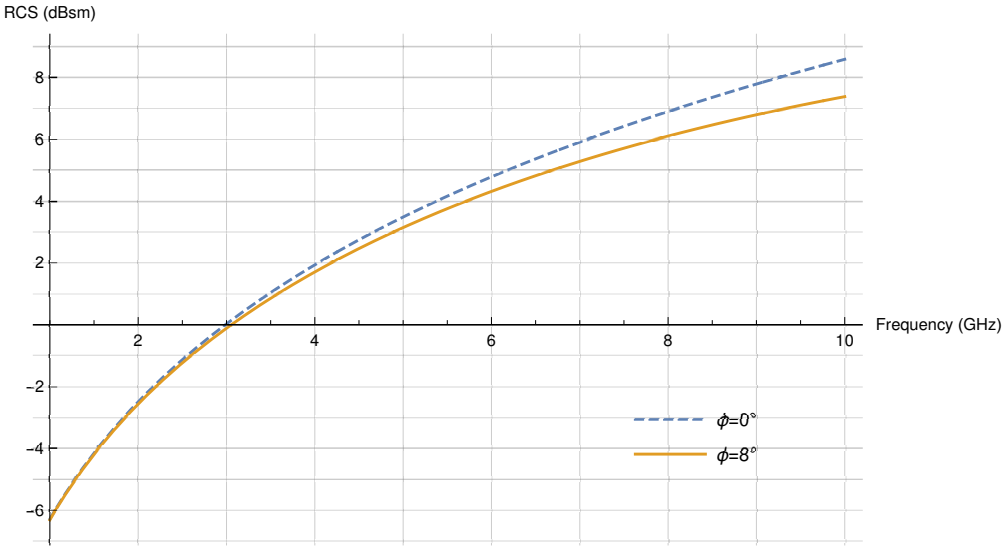

Figure 5.8: Calculated co-polarized radar cross section of a 35.5 cm x 5.4 cm cylinder.

the 29th and 30th range bins, visible as the primary point where the signal with the target differs from the signal without the target. From band 1 to band 4 the difference between the target peak and the background increases from 6 dB to 15 dB. Part of that increase is due to the increased RCS of the target at higher frequency and part is due to the increased gain of the antennas at the higher frequency.

Since this is a relatively controlled test environment the radar system was not moved between the empty and target-present measurements. Returns from the background scene can then be subtracted out to partially isolate the return of the target. Figure 5.10 shows the improvement in the target/clutter ratio by subtracting out the background scene in the time domain for each band. In all bands the target response is elevated above the response of the ceiling, which was the next-strongest target.

Steering on receive for the single target is shown in Figure 5.11. The target is present in all bands, however the clutter from the background scene is strongest relative to the target in the first band. As mentioned before, this is due to the RCS of the target and gain of the antennas decreasing with lower frequencies. The grating lobes that appear when steering off-axis are strongly visible in the higher three bands as the ring that extends out from the center target. This ring is also caused in part by the unaligned phase of the ADC clocks mentioned in Section 4.2.3.2. Steering 90° off-axis

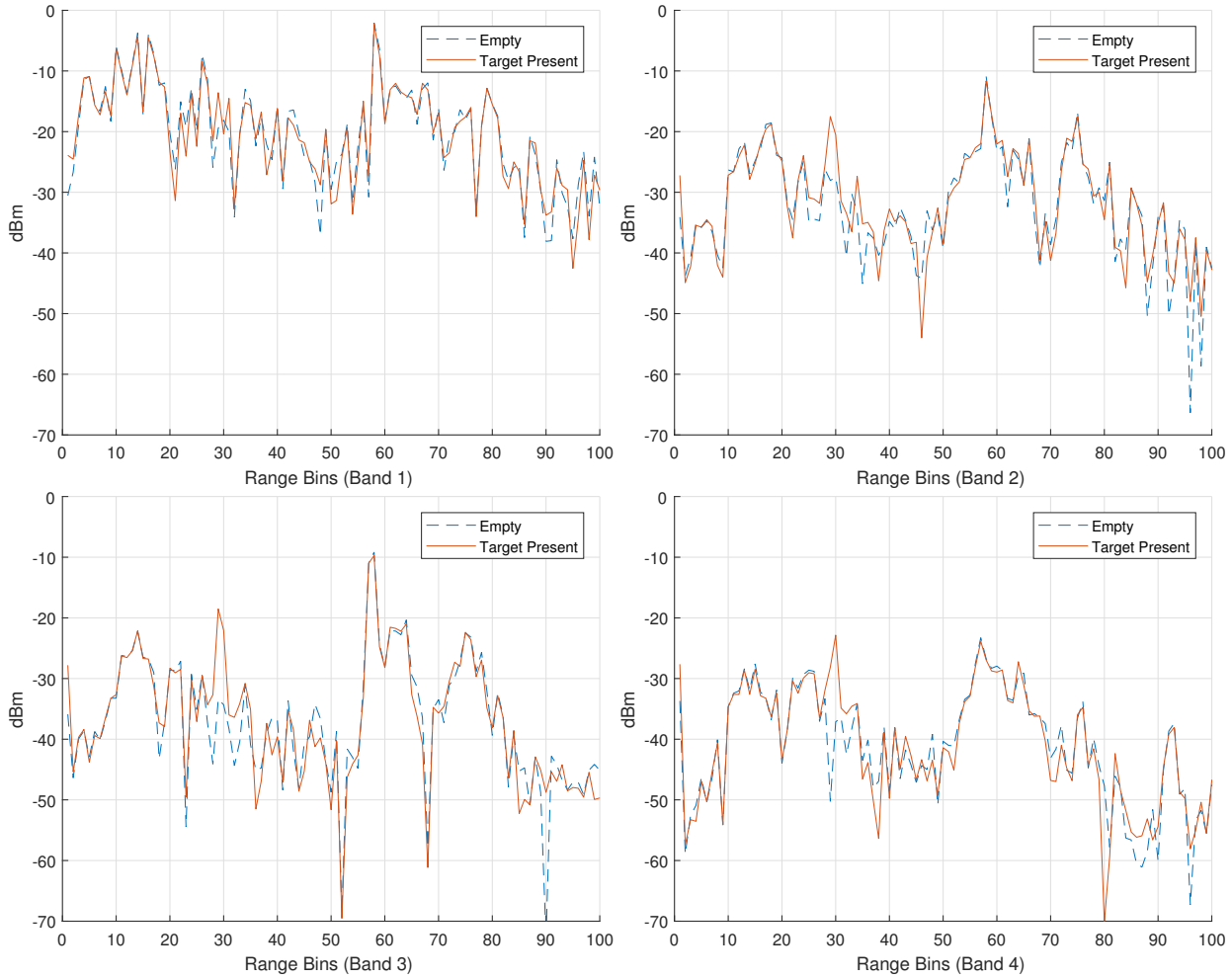

Figure 5.9: Range profiles from each band for a single target at 2 m range. Returns without a target present are included to highlight what should be considered background clutter. Each range bin corresponds to 6.8 cm.

is not feasible with this array and any targets that appear around either 0° or 180° in the plots are the result of phased array sidelobes that overpower the (steered) main beam.

5.1.3 Dynamic Single Target

The same target used in the static test was moved across the floor in a straight line 25 times in 4" increments, taking a measurement at each position. The target is 2 m away from the antennas at its closest and sweeps out what should be a 60° swath from the perspective of the array center. The results are shown for band 3 in Figure 5.12. While the sequence is not exactly represented well in

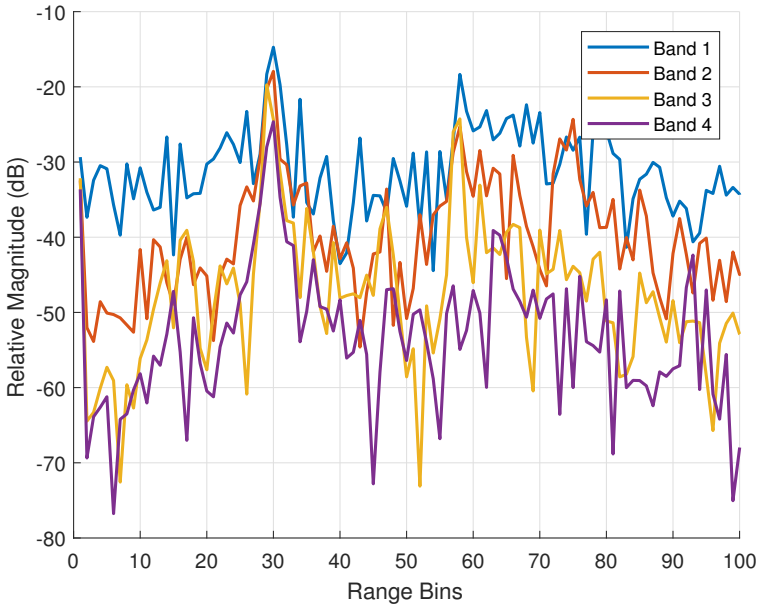

Figure 5.10: Background scene subtraction for each band for a centered target. The target was placed 2 m out directly in front of the arrays and should appear around the 29th and 30th range bins.

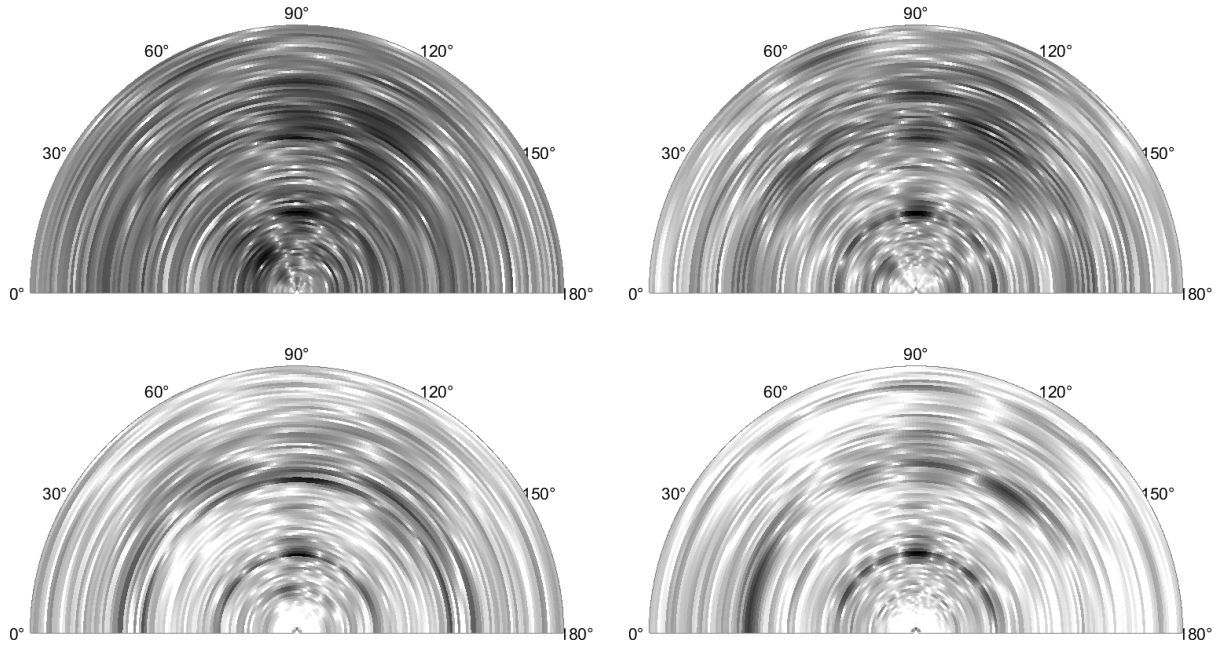

Figure 5.11: Steering applied to the received data from bands 1 through 4. The color scale for each image covers a 40 dB range from the greatest magnitude in the return (darkest) to 40 dB less (lightest). 100 range bins (6.8 m) are shown and no spatial windowing was applied to the array.

this format, the motion of the main target should be distinguishable across the series.

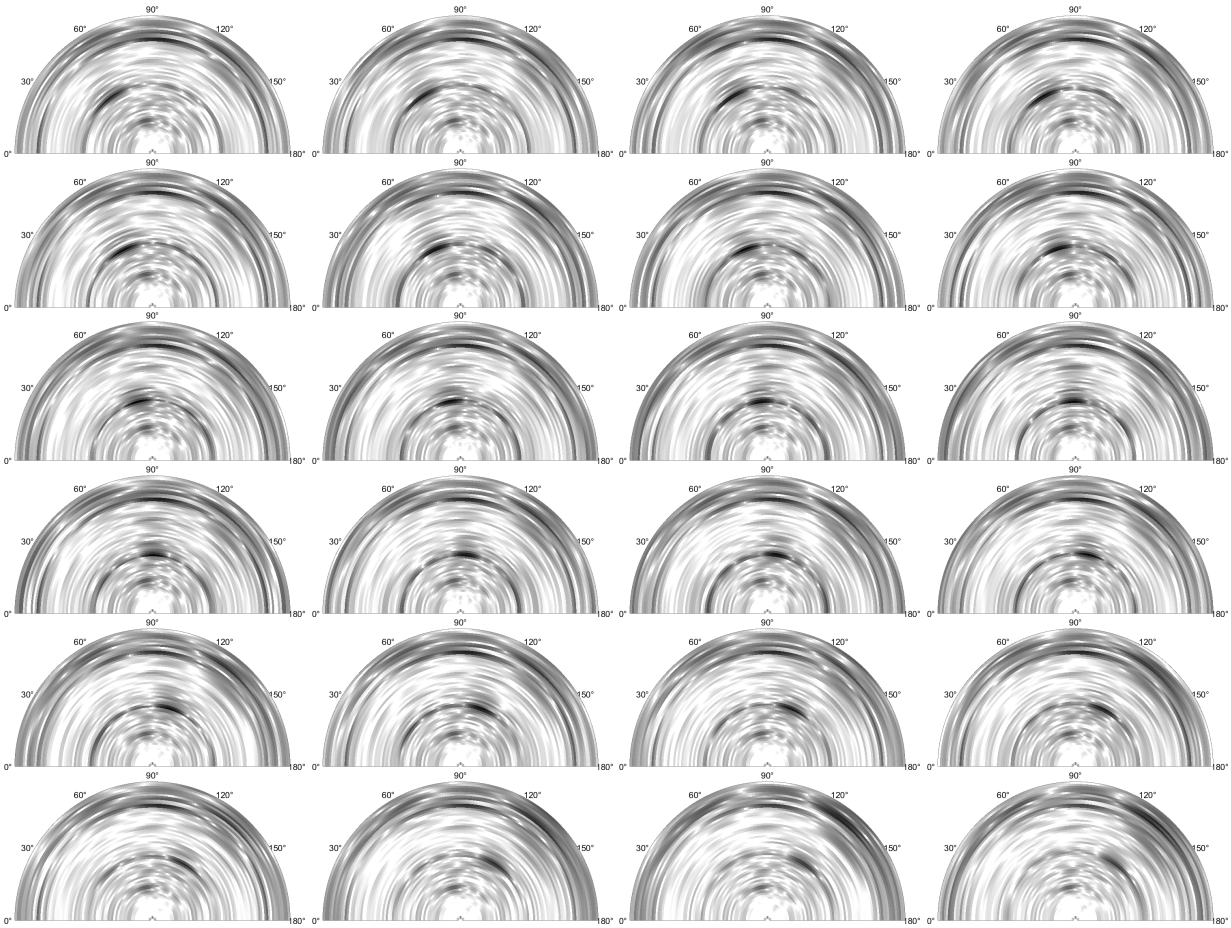

Figure 5.12: Single target moved linearly across 60° of the arrays FOV. Sequence follows left to right, top to bottom. Each image shows 70 range bins of the third band (4.76 m) and all have the same fixed color scale spanning 40 dB.

5.1.4 Dynamic Multi Target

An informal test to evaluate the system's ability to distinguish two near targets was performed by spacing two cylinder targets 60 cm apart and rotating them around each other. Figure 5.13 shows 180° of rotation in 12 increments. The last row of the sequence is fainter as the cart was jostled between the measurements preventing a consistent background subtraction. When the two targets are at the equal ranges from the antenna they are difficult to distinguish given the width of the main-beam and the grating lobes that form during steering. Once they are rotated out of the same

range they are easily distinguished.

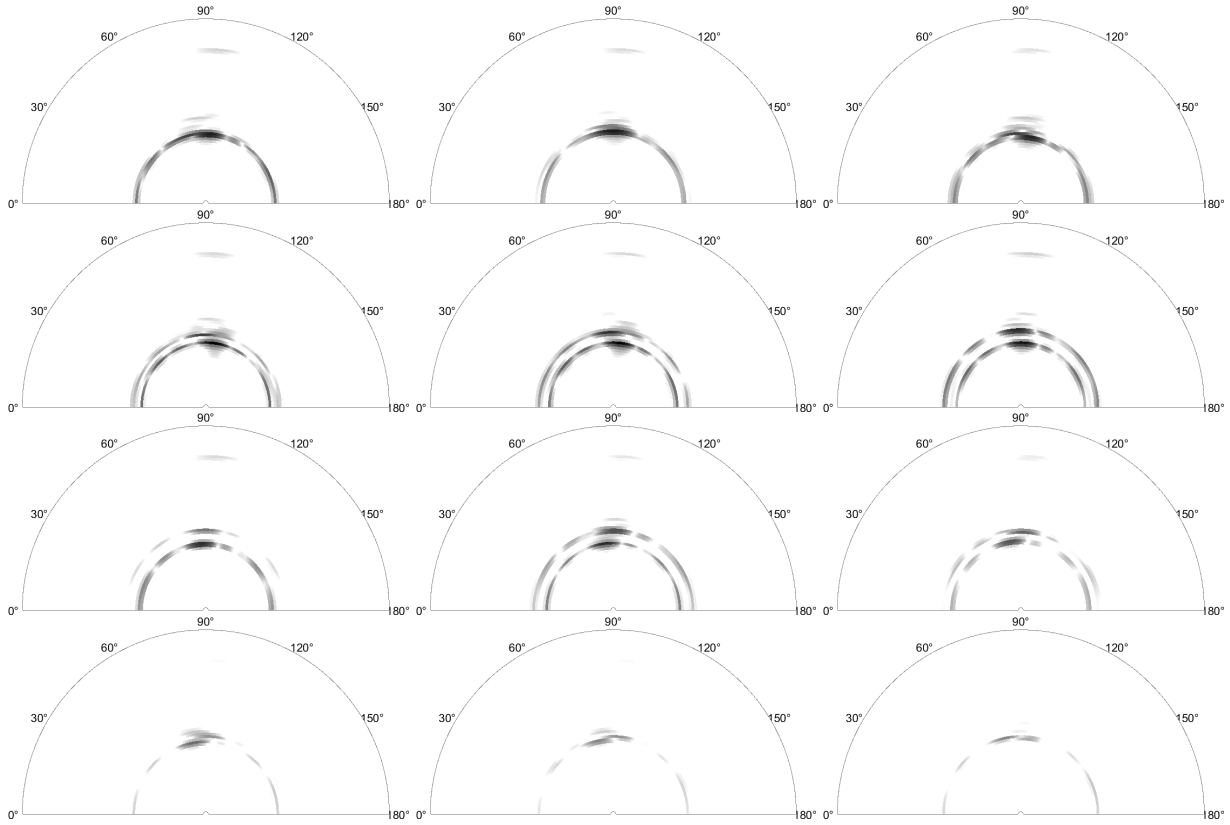

Figure 5.13: Two targets rotated around each other 180°. Sequence follows left to right, top to bottom. Each image shows 70 range bins of the third band (4.76 m) and all have the same fixed color scale spanning 30 dB.

5.2 Continued Operation and Future Work

The results of the steering tests show that the radar is, at the very least, functioning and that the RFSoC is capable of acting as the digital backend for a multi-channel radar. In order for it to serve as a stable instrumentation platform more work must be done. This includes continued characterization of the current system and extends out to improvements on the current design. The issues identified in the design in previous chapters need to be resolved as well. Most of what follows should be read as a to-do list.

5.2.1 Characterization

Various aspects of the system still need to be characterized before the system can be brought into regular use. These are presented in the following sections categorized by radar subsystem.

5.2.1.1 RF Frontend

- Measurements with a calibrated noise source should be taken for the receiver and transmitter as the noise figure estimates relied on the manufacturer provided de-embedded figures.
- Obtain a more accurate value for the receiver saturation point. Would then be able to determine the dynamic range.
- Characterize switching performance of the SP6T switches used in the transmitter filter bank. Verify the expected switching times and the RF behavior during switch.
- Make a test board using the 4 layer FR408 stackup with specific lengths of CPW, CPWG, strip line, and microstrip line to accurately characterize the insertion loss and variability of the stackup. Validate it with a simulation in HFSS and use low-loss press-fit connector probes.
- Get precise measurements of the cables connecting the RF boards to the RFSoC carrier. Would require a SSMC-SMA adapter for the VNA.

5.2.1.2 Antennas

- Take pattern measurements with the dielectric load.
- Take pattern measurements across elevation cut for both single-element and array.
- Get pattern measurements for the array where only the two center elements are driven, all other elements terminated.
- Take inter-array isolation measurements with absorber square placed in between the arrays.

- Take improved cross-polarization measurements for both single-element and array. Previous cross-polarized patterns were without a preamp, and were worthless due to residing mostly below the noise floor.
- Verify transient response from the two backplanes using the VNA.
- Take pattern measurements with radar chassis behind antennas.
- Precisely measure the dielectric properties of the polycarbonate used in the dielectric loading structure.

5.2.1.3 Radar Measurements

- Take measurements over open environment: grass, snow, soil. Requires longer cables to further separate antenna array from chassis.
- Take steered pattern measurements. Have radar setup in chamber emit tones at various frequencies at various angles on turn table to measure steering sidelobes.
- Take cross-polarized radar measurements with calibrated targets and soft targets.
- Perform multi-target delay line measurements. Use splitters and cables of slightly differing lengths to verify range resolution for both single bands and synthetic bandwidth.
- Take single-channel measurements with horn antennas used in the past.
- Calibrate stretch processing algorithm using optical delay line.

5.2.2 Design Improvements

Through testing and assembly of the system many potential improvements and fixes were identified. Some are required for the system to become fully operational, others are to address long-term maintenance needs, and still others can just be considered nice-to-haves.

5.2.2.1 RF Improvements

- Fix the biasing issue present on the synthesizer output ports. Once fixed, perform repeated measurements of VCO lock time over a long duration (>1 hour) to validate for continuous performance in a remote system.
- Add power sequencers to the transmitter modules.
- Change the ribbon cable header to a right angle mount style so a single ribbon cable can be shared across all modules. Synthesizer board can then be further compacted with fewer headers.
- Taper the filter landing pad transitions for the LTCC filters with greater than 4 GHz cut-off frequency. Should reduce insertion loss and further minimize reflection.
- Increase thickness of soldermask strips at the edge of IC landing pads on transmitter board. The 2 mil strips used on the first transmitter revision were too thin while the 5 mil strips used on the receiver modules were sufficient.
- Align the SMA connectors on the transmit and receive modules with respect to their mount points, that way they can be kept flush and mated with fixed panel-mount connectors.
- Create a front-plate for the radar and add panel-mount connectors for the RF section. Should help decouple the RF modules from the antennas both mechanically and electrically.
- Add an extra mount point or two on the other side of the transmit and receive modules to eliminate strain from flexing and dampen vibration.
- Replace the high-pass filters used in the lowest transmitter band with the MLO filter used on the receiver. It is more compact, higher performance, and can be ordered in single-unit quantities.
- Switch to nano-fit connectors for power input. More robust connections in a smaller form-factor.

- Reroute the trace carrying the mixer enable signal. This trace has internally broken on two of the nine assembled transmitter boards. It is a simple repair but should be addressed in the design.

- Route synthesizer clock from FPGA clock ports instead of the clock distribution chip. This assumes the clock distribution chip remains unconfigured.

- Find a wide-band LNA with less roll-off than the one used on the receiver.

- Consider switching to a lower bandwidth synthesizer. This should come with lower cost, which might make it advantageous to place two on the same board and use an RF switch to switch between them. Eliminates relying on VCO recalibration process and creates more deterministic LO switch time.

5.2.2.2 Antenna Improvements

- Switch to lower loss, thinner substrate with greater dielectric constant. Would allow for thinner, higher performance microstrip feed that would interfere less with slot-line behavior.

- Expand aperture height and increase length slightly. Increasing the aperture height (extending the taper) should improve performance around the low end of the bandwidth and increasing length should improve the gain [37].

- Integrate a power divider onto a two-element coplanar array. The two-element coplanar array will increase directivity in the E-plane while still allowing for the same H-plane array construction.

- Experiment with adding an exterior bevel to the taper to help deal with low frequency match [38].

5.2.2.3 Digital Improvements

- Fix DMA transfer from BRAM to PS-accessible DDR4. The slow AXI4 throughput from BRAM out to the PS is the current bottleneck preventing faster write speeds and higher non-presummed PRF.
- Develop feedback loop bringing FFT output in the FPGA to a peak detector in the processor to adjust the delay on the second reference signal and corresponding ADC capture time.
- Correctly configure the clock distribution IC on the carrier board. Would then enable the FPGA accessible DDR4 along with other peripherals.
- Get Linux working on RFSoC. Would then be able to take advantage of pre-existing interface drivers for SATA, Ethernet, Displayport, etc. Multi-core processing would also be easier.
- Integrate GPS and IMU data into radar captures. Critical for SAR functionality.
- Enable DDS normalization pattern adjustment from PS.
- Complete and test the implementation for DDS phase normalization.
- Find a carrier board capable of providing the correct MTS clock for the RFSoC.
- Load RFSoC bitstream into onboard QSPI flash to avoid reloading over JTAG on every reboot of the system.
- Once the storage setup is fixed the PRF should be set in the FPGA.
- Develop a more accurate model of mixer products to see greater improvement in the mixer product cancellation.
- Consider adding calibration loopback path; set aside one transmit and receive pair along with an extra transmitter to calibrate from the perspective of the receiver.

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Appendix A

RF Modules and Carrier Board

A.1 PCB Stackup and Assembly

The transmitter, receiver, and synthesizer boards were all designed around a four layer FR408 stackup. Isola FR408 is rated to have a relative permittivity of around 3.66 across the operating band and a dielectric loss tangent ($\tan\delta$) of around 0.0127 [72]. Rogers RO4350B laminates with a comparable permittivity have a $\tan\delta$ closer to 0.0021 by comparison [73]. Rogers materials are mentioned as previous CReSIS systems have been built on them, and if RO4003C or RO4350B were to be used in these modules the cost would be around four to eight times the cost of the FR408 stackup used.

Assembly was carried out manually by applying 60-40 solder paste to the boards using a steel stencil. All components excepting off-board connectors were then placed by hand and the boards were passed through an IR reflow oven. After a brief cooling period and joint inspection off-board connectors were installed and soldered using a handheld iron.

An exception to the above process, the FMC connector on the synthesizer module has lead-free solder charges that require a reflow temperature exceeding the capabilities of the reflow oven. To work around this it was installed using a hotplate that was manually adjusted and monitored to follow a time-stretched approximation of the manufacturer (Samtec) provided reflow profile. During the first attempt the connector reflowed correctly but small regions on the board away from the connector internally delaminated. On inspection no connections were broken or shorted, but the mechanical failure could easily lead to future board failure. Caution was taken during the second attempt to avoid delamination by insulating the rest of the board from the hot plate and

reducing the total time spent on the plate. From visual inspection no delamination occurred, the solder charges properly reflowed, and all pins on the FMC connector were electrically connected. As the lead free solder has a melting point outside the range of the reflow oven the board could be flipped connector-side-down on a mounting block and passed through the oven to reflow all other electrical components on the side opposite the FMC connector.

A.2 Transmitter Module

Figure A.1 shows an assembled transmitter module. The two pin connector on the top left is the main power connector; an input voltage ranging between 6 V and 12 V is expected given the linear regulators used. The header pins immediately below the power connector are used for digital control of the system through the ribbon cable connected back to the synthesizer module. Four lines are present to control the RF switches, one for the mixer, and one for the soft-start linear regulator. All digital control lines are +3.3 V CMOS logic. The top left SMA connector is the input connector for delivering the LO signal to the mixer. It is immediately incident on the mixer bypass switch however, so it could serve as the input source when bypassing the upconversion stage. The bottom left SMA connector receives the input signal during upconversion. It feeds immediately into the amplifier and filter chain preceding the mixer IF port. The top right SMA connector is the RF output port, and the bottom right SMA connector is the receiver reference signal (LO) output port. Both supply the same signal, however between the splitter feeding the two ports and the RF output port there is an extra amplifier for driving the antennas.

A.2.1 Transmitter Components

An emphasis was placed on cost when evaluating components for this design. Every component included is an off-the-shelf item that can be found through at least two major suppliers. This means that acquiring replacement components does not involve long lead times and the cost of building spare modules is minimized. If future CReSIS systems make use of this module there should be

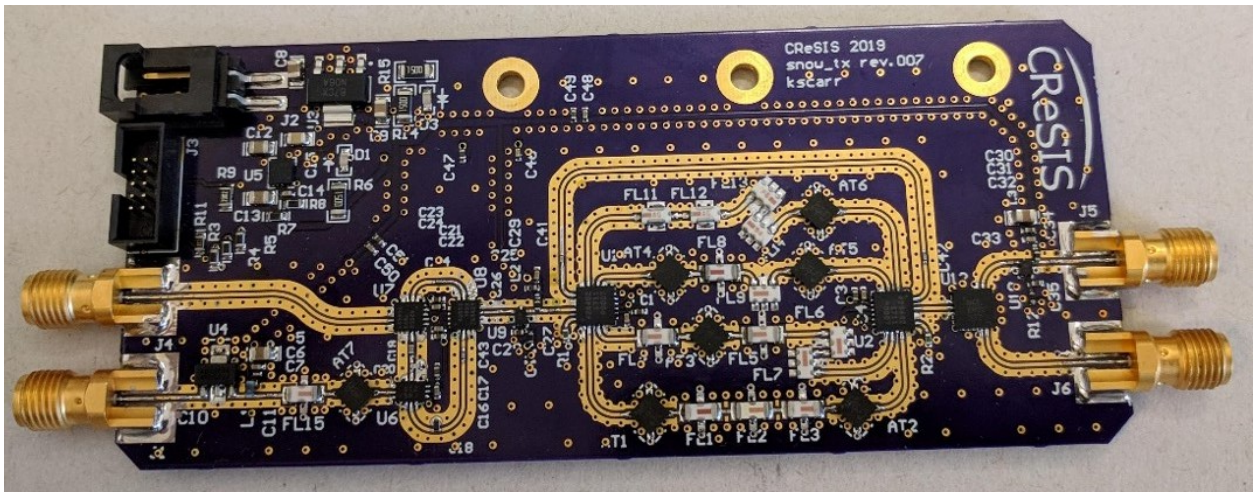

Figure A.1: Photo of single transmit module

few barriers to producing an arbitrary number of them. Table A.1 lists the main RF components used in a single transmitter module.

Quantity	Part Number	Function and Description
1	ADL5544	IF stage 30 MHz to 6 GHz 17 dB Gain Block
1	LFCN-2850	3 GHz LPF to cut out IF image
7	GAT-1+	1 dB pad to improve match and reduce reflections
2	PE42553	8 GHz SPDT switch for mixer passthrough
1	LTC5549	2-14 GHz Active mixer
2	MAAM-011206	DC-15 GHz 13.5 dB Gain Block
2	PE426462A	10 MHz - 8 GHz SP6T for filter bank control
1	EP2C+	1.8-12.5 GHz power splitter for RX LO
1	LFCN-3800+	Filter bank 1: 3.8 GHz LPF
1	LFCN-3400+	Filter bank 1: 3.4 GHz LPF
1	HFCN-1910+	Filter bank 1: 1.9 GHz HPF
2	LFCN-5000+	Filter bank 2: 5 GHz LPF
2	HFCN-3100+	Filter bank 2: 3.1 GHz HPF
1	LFCN-6400+	Filter bank 3: 6.4 GHz LPF
1	HFCN-5050+	Filter bank 3: 5 GHz HPF
2	LFCN-8400+	Filter bank 4: 8.4 GHz LPF
2	HFCN-672+	Filter bank 4: 6 GHz HPF

Table A.1: Components used in the transmitter module. HPF = high pass filter, LPF = low pass filter.

A.3 Receiver Module

Figure A.2 shows an assembled receiver module. The header pins on the bottom right are reserved for debugging purposes; primarily to provide control in the event the power sequencing ICs fail. The power connector beneath it is the same as the one on the transmitter module. The SMA connector on the top right is the IF output of the receiver that sources the dechirped output to the digitizer, in this case the ADCs on the RFSoC carrier board. The SMA connector on the top left is the RF input, to be driven by an antenna element. It feeds in to the 2 GHz - 8 GHz bandpass RF input filter. The SMA connector on the bottom left is the LO input for the reference signal supplied by a transmitter module. It connects directly to the mixer through a DC block.

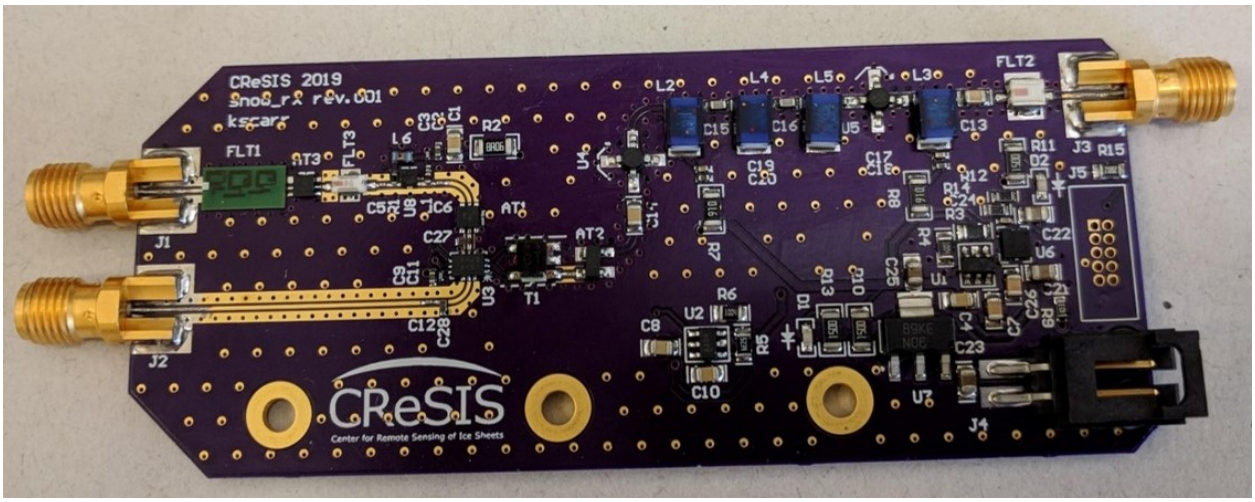

Figure A.2: Photo of single receiver module

A.3.1 Receiver Components

The receiver module shares as many components with the transmitter module as possible: the power supplies are the same and most decoupling and biasing networks share components. Table A.2 lists the main RF components used on the receiver.

Quantity	Part Number	Function and Description
1	HF0BA1440A700	1.4 GHz HPF
2	YAT-1+	1 dB pad to improve match
1	LFCN-8400+	8.4 GHz LPF
1	GRF3044	100 MHz - 12 GHz 16 dB LNA
1	LTC5548	2-14 GHz Active mixer (IF: DC - 6 GHz)
1	LAT-1+	1 dB pad to improve match
1	TC1-6X+	350 MHz Transformer serving as IF balun
2	MAR-6SM+	2 GHz 22 dB gain block for IF
1	LFCV-52+	90 MHz LPF for IF

Table A.2: Components used in the receiver module. HPF = high pass filter, LPF = low pass filter.

A.4 Synthesizer Module

Figure A.3 shows the synthesizer module. As of this writing the biasing issue is still present, and the synthesizer fails to obtain a clean lock. The biasing section should be reworked to either replace the inductors or switch to a single-ended source. Beyond the biasing issue it would probably be best in the long run to switch to an architecture with two cheaper synthesizers behind an RF switch to avoid continuously re-calibrating the VCO. Aside from the synthesizer, an LMX2594, and the GP2X1+ splitters all other components such as the gain blocks and filters are carried over from the transmitter modules.

Future synthesizer modules may be best served by being assembled by a professional board house. This is due to the reflow requirements imposed by the 580-pin FMC connector which uses lead-free solder. The Samtec recommended reflow temperature profile exceeds the operating capability of the CReSIS in-house reflow oven, requiring any soldering to be taken care of in an ad-hoc fashion on a hot-plate. Failure to actively monitor the temperature can easily lead to delamination and other heat related damage to the synthesizer PCB.

A.5 RFSoC Carrier Board

The RFSoC carrier board is an HTG-ZRF8 designed and manufactured by Hitech Global. As shown in Figure A.4 the synthesizer module is mated with the carrier on the top right through a

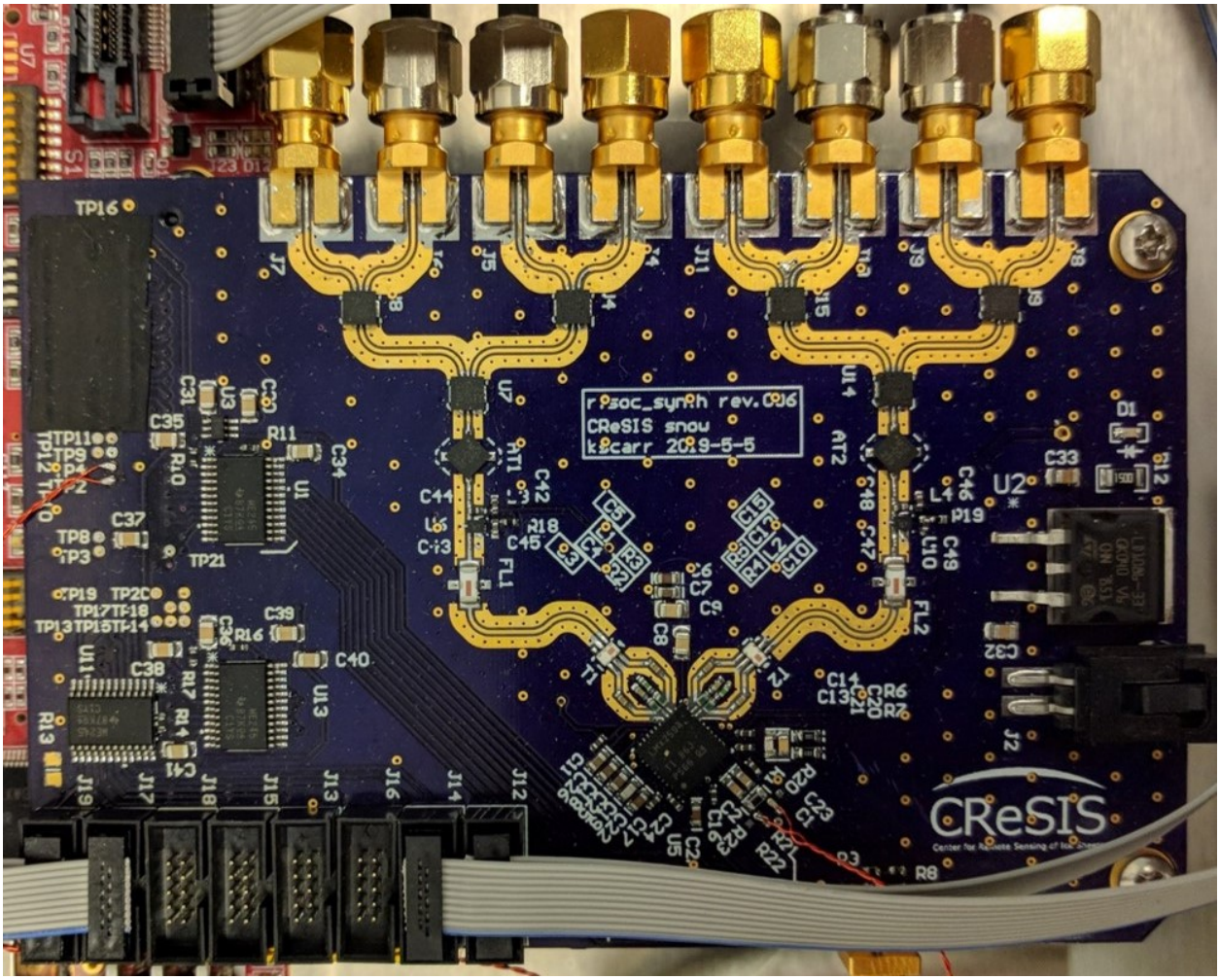

Figure A.3: Photo of the synthesizer module

VITA 57.4 FMC interface. RF ports for the data converters are exposed through the 16 SSMC connectors on the left side. The PCIe interface on the bottom edge of the card was left unused, but could be if the system were ever rebuilt around an x86 PC.

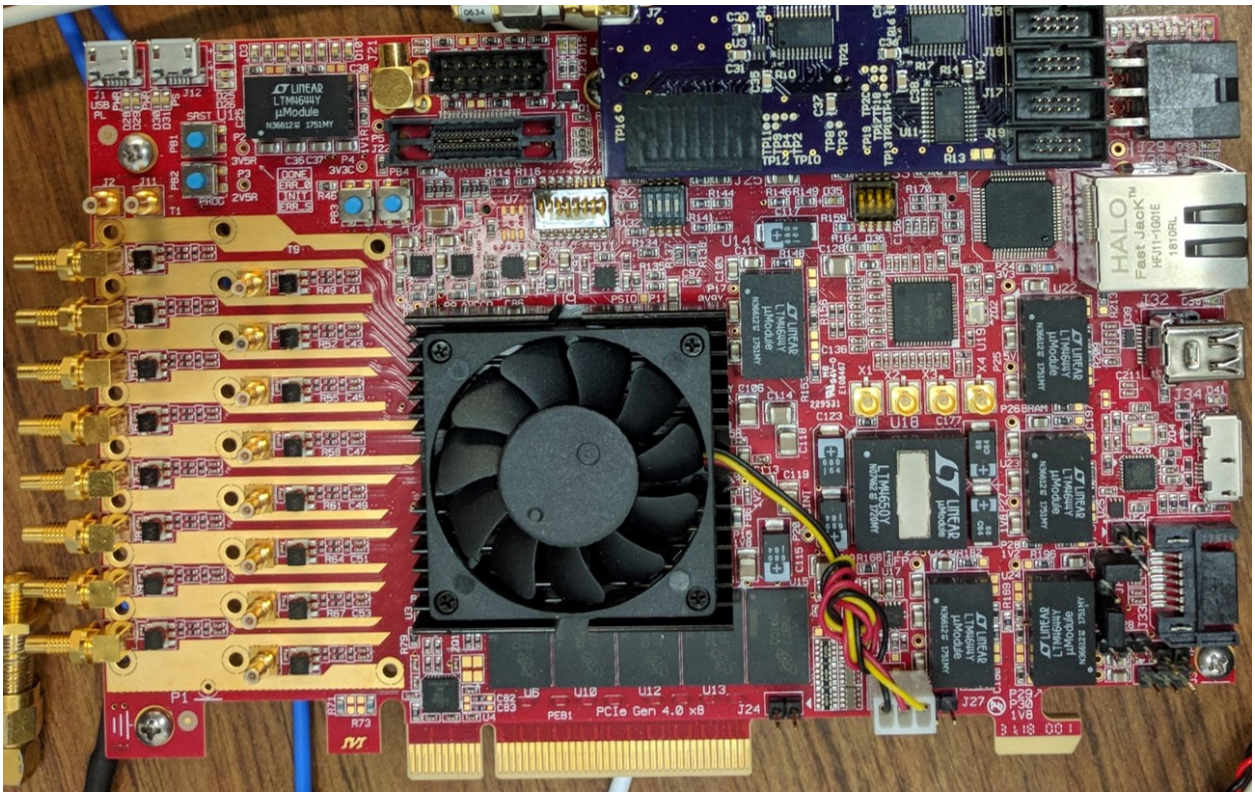

Figure A.4: Photo of the RFSoC carrier board

Appendix B

Radar Chassis Assembly

For ease of testing and to demonstrate standalone operation the full system was integrated into a single chassis. The assembled chassis with the top plate removed is shown in Figure B.1. The RFSoC and RF assembly are visible in the bottom half and connected using 10" cables with male SMA and SSMC connectors that were manually cut and assembled to ensure matching lengths. The cables feeding connecting from the synthesizer board are 11" SMA-SMA cables that were also manually cut and length matched. The ATX power supply is mounted directly to the back panel and unused cables are tucked underneath. This is considered acceptable as there is no air-intake on the bottom that would be otherwise blocked by the tucked cables. Mains power is passed through a basic filter at the chassis socket directly into another low noise filter visible underneath the Xilinx Platform Cable programmer. This low noise filter then feeds in to a Daitron 50W soft switching supply that is used to provide the power for the RF boards. It branches out to two distribution boards developed at CReSIS for a previous project. In lieu of a full face plate on the front a small 4" plate was cut out to hold the power supply switches and a USB type B connector for the system UART. As noted in Section 5.2.2 a proper face plate should eventually be cut out to relieve connection stress from the RF modules.

The RF modules are all vertically mounted on aluminum L-brackets on top of a solid aluminum plate as shown in Figure B.2. The two plates are fixed together using 3" screws tightened with nuts on the top and bottom. A second hole is present on the plates to allow for mounting to the bottom of the chassis. Rubber pads are present on the bottom plate to elevate the plate above the nuts and potentially dampen some vibration. Given the single-sided mounting position of the L-brackets there is some flex present on the RF modules. While easy enough to work around, this flex could

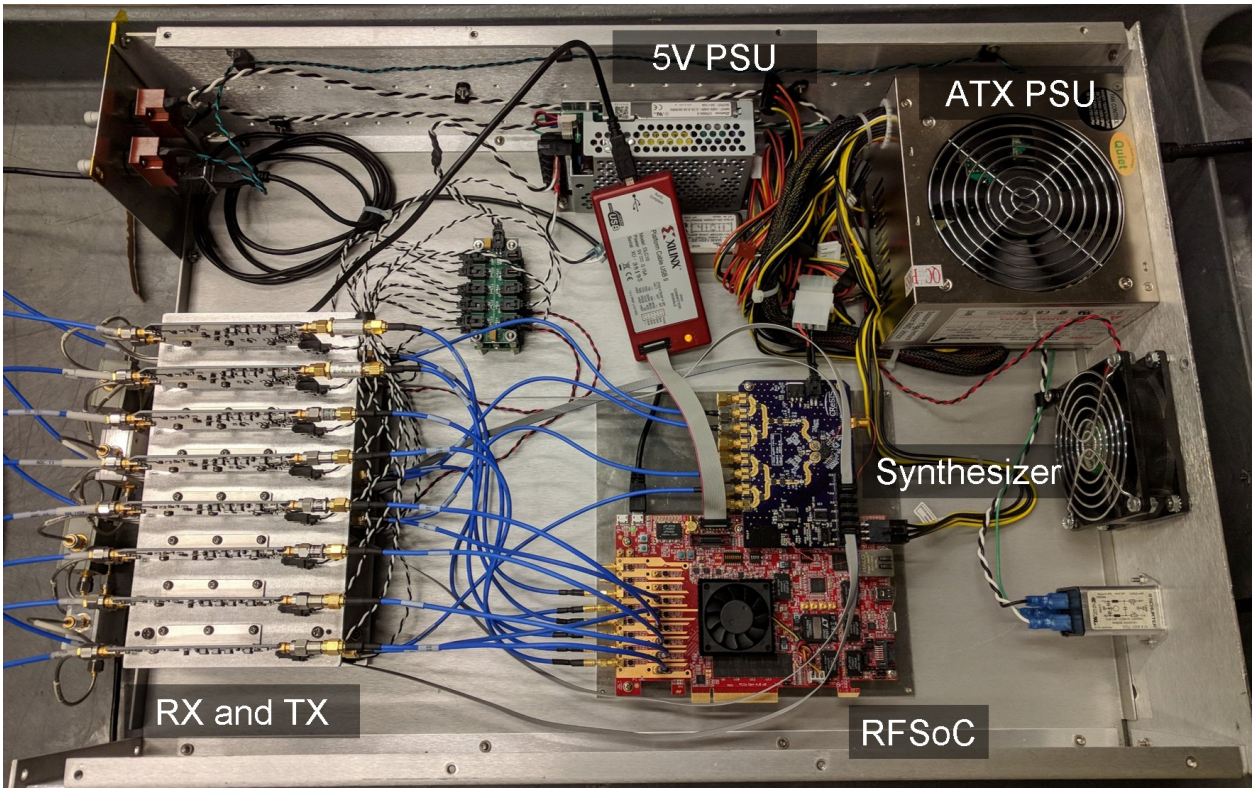

Figure B.1: Image of the assembled radar chassis

cause component failure through joint cracking. Future modules should include mount points on both sides.

The receiver modules were mounted above the transmitter modules due to the placement of the reference signal ports on each module. With the transmit on bottom and the receiver on top the two reference ports are both on the inside, allowing for direct connection using a single 3" SMA-SMA cable. In the final setup where only two transmit channels were in use those shorter cables were not used, and the double-stacked setup could have been foregone in favor of a shallower assembly.

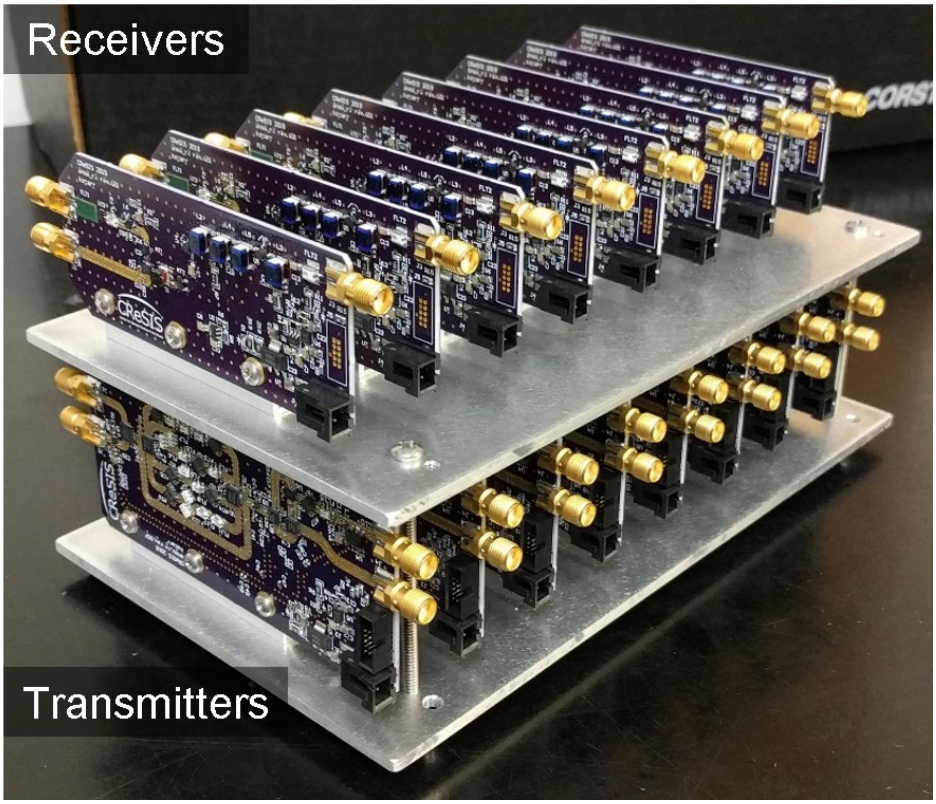

Figure B.2: Profile view of the RF module assembly

Appendix C

Antenna Testing Setup

C.1 Antenna Loading Structure

The dimensions of the loading structure and the exact material used are shown in Figure C.1. The antennas are designed to slide in to the slots and rest flush against the bottom, however the relative position of the antennas can be adjusted to change the effect of the loading structure. Mounting holes were added at each of the four corners to provide a means for mechanical relief with respect to the array backplane, however no testing made use of that structure.

C.2 Antenna Chamber Measurements

When testing the antennas in the chamber each antenna was placed on a styrofoam mounting structure shown in Figures C.3 and C.4. The antenna feed consisted of a chain of PTFE low loss cables, one 8.23 m long PE-P300LL cable and a pair of 1 m long UT-085C-Form cables. The insertion loss for theses cables is rated at less than 0.59 $\mathrm{dB\,m^{-1}}$ for the former and less than 2 $\mathrm{dB\,m^{-1}}$ for the latter. Including the cable between the chamber wall and the VNA it works out to around 10 dB of insertion loss purely from the cables. The presence of the female-to-female SMA connectors between each cable significantly increased the cable loss however, which can be seen in Figure C.2. S_{11} measurements of the antennas all had this cable loss calibrated out using an Agilent E-cal kit, but pattern measurements were taken with no calibration and normalized after the fact. A 26 dB wideband preamp with uniform gain was placed immediately following the network analyzer to compensate for both cable loss and antenna efficiency.

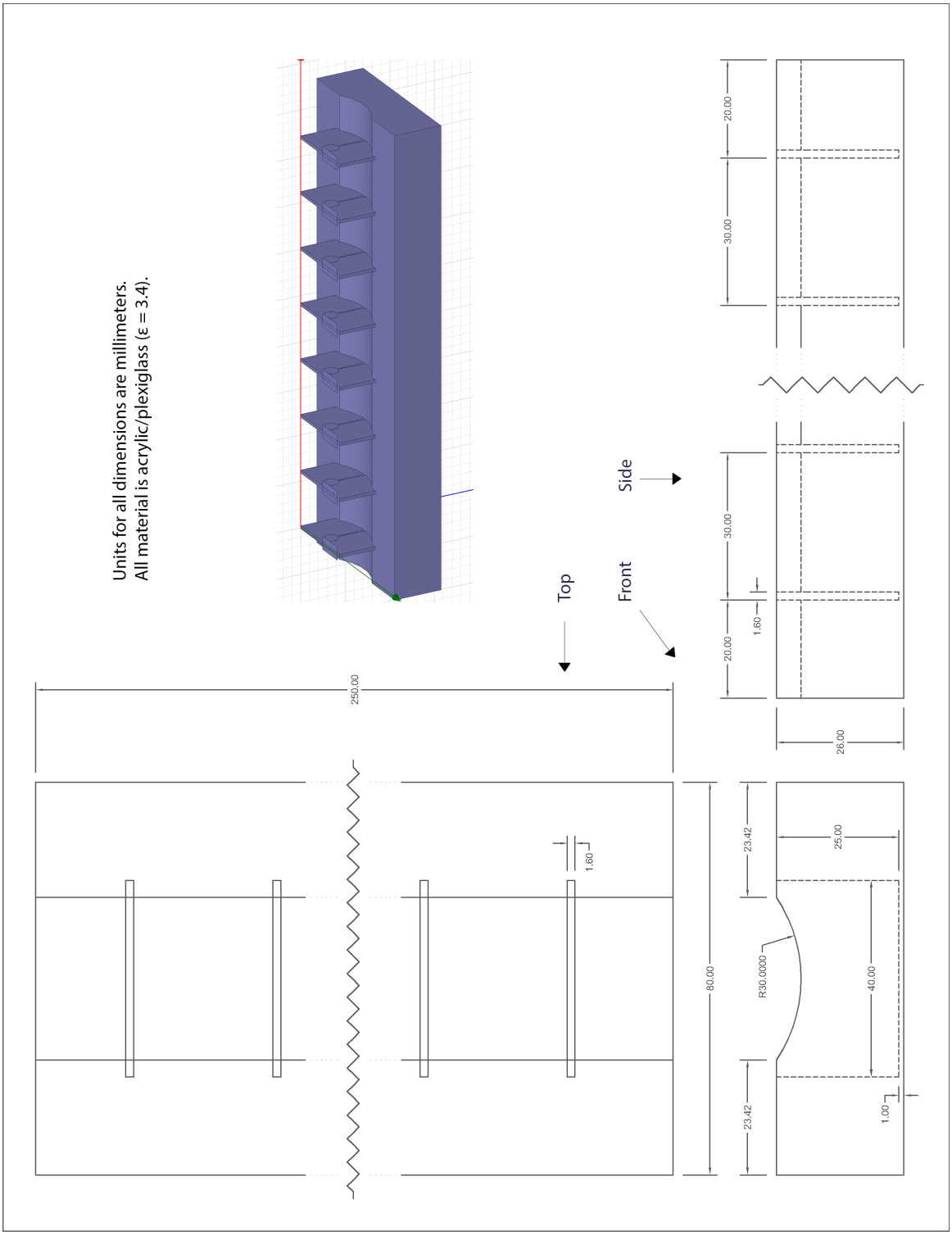

Figure C.1: Dimensions of the loading structure as tested.

The styrofoam structure was placed along the outer edge of the turntable to reduce potential ground reflections from the table over the sweep of the antenna's main lobe. This position changes

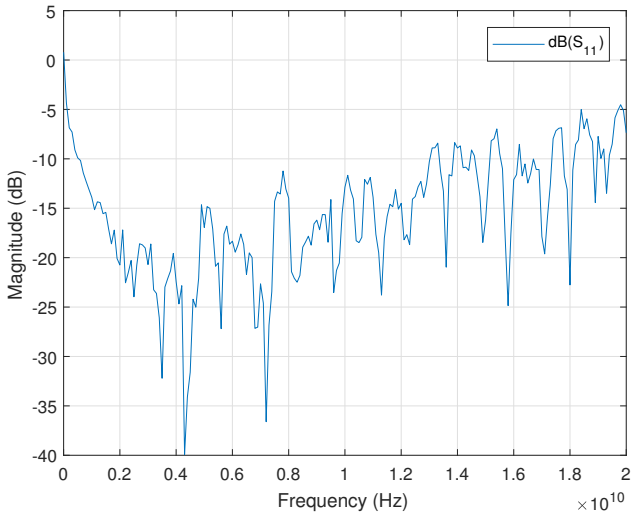

Figure C.2: Measured $|S_{11}|$ parameter of antenna feed cables with an open attached in place of an antenna.

the relative angle of the antenna to the wall antenna and introduces a drift in reported/actual angular position that peaks at 5° at the lateral extents. This drift explains the shrinking-in effect of the grating lobes seen in Figures 3.16 and 3.17.

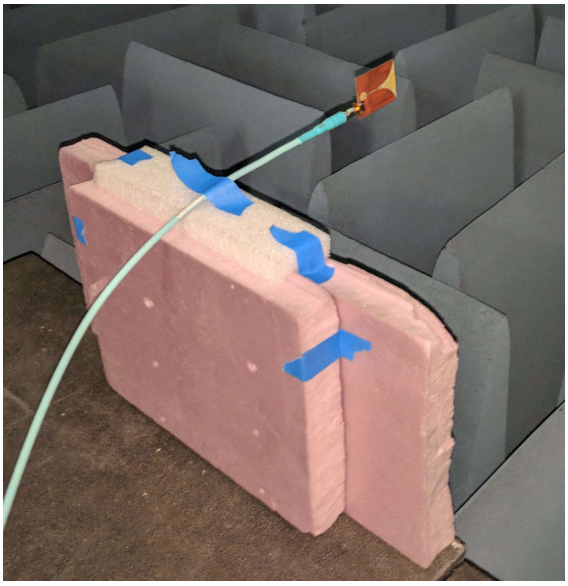

Figure C.3: Single element mounting structure. More tape was added to increase stability of foam blocks and the feed cable was firmly affixed to the turntable to prevent pulling during table stepping.

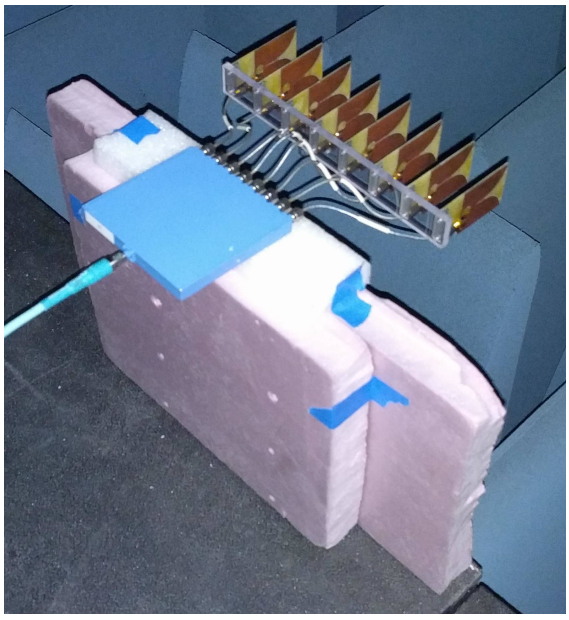

Figure C.4: Power splitter and array mounting structure. Like the single element, more tape was present during the actual measurements and the cable was properly attached to the table.

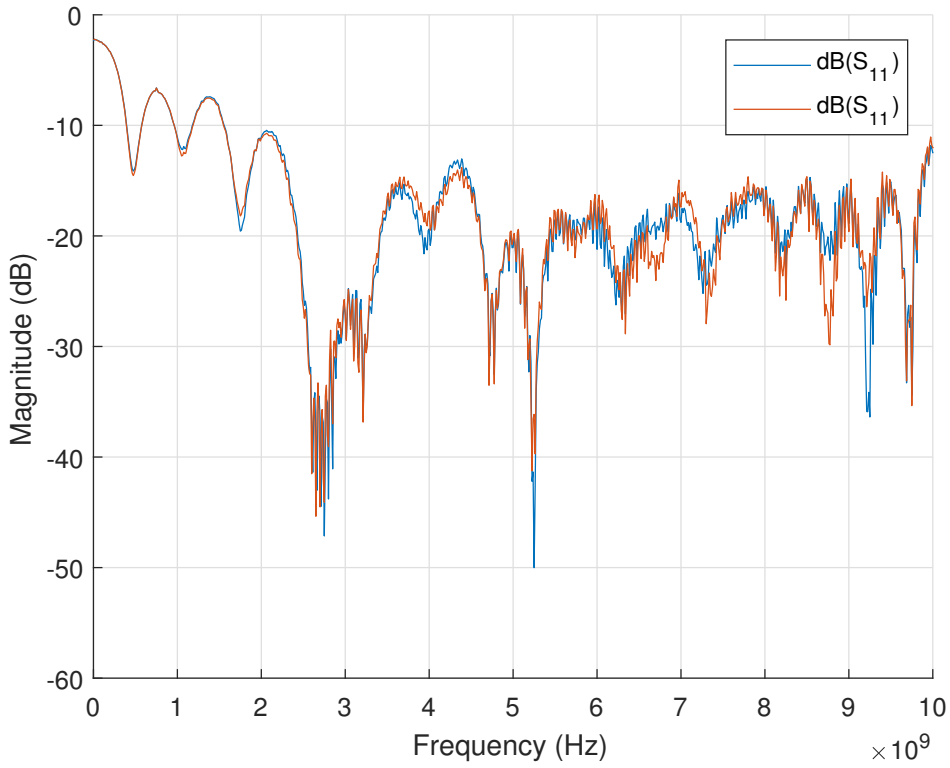

Figure C.5: Measured $|S_{11}|$ of Pulsar Microwave 1:8 power divider/combiner used for testing radiation performance of the antenna arrays.

Appendix D

Full System Testing Setup

The results presented in Chapter 5 were taken with the array setup shown in Figure D.1. The array on the right had the two center elements driven while the surrounding elements were all terminated in broadband 50 Ω loads. The receive array on the left had every element directly feeding a receiver. A 1:8 power splitter, the same one used in the antenna measurements, was used to break out the reference signal from a single transmitter module out to the eight receive modules. 3 dB of attenuation was added to the splitter to drop the power down to the level of an equivalent transmitter reference port. The second reference transmit channel is phase aligned with the first through the manual delay measurements as described in Section 4.1.1.

Foam was placed around the antennas during testing in an attempt to eliminate some of the clutter from the surrounding environment. Since the antennas have non-negligible sidelobes the metal shelving present on the left and right sides of the test setup would have interfered as strong targets in the result. Two inch thick RF absorbing foam was placed to the left and right of the antennas on top of boxes and on the floor immediately underneath. A small wedge was kept in between the transmit and receive arrays to further increase the isolation beyond the results presented in Section 3.4.2.

The target was placed on a wooden stake braced by a large polyethylene foam block. For the multi-target results an identical second pipe-on-stake target was placed in one of the other visible holes in the foam block. In this photo the pipe is 2 m away from the antennas and 15 cm out from the absorber wall. The 2.54 m sweep performed in the dynamic single target test started just to the left of the absorber wall and finished just to the right of it.

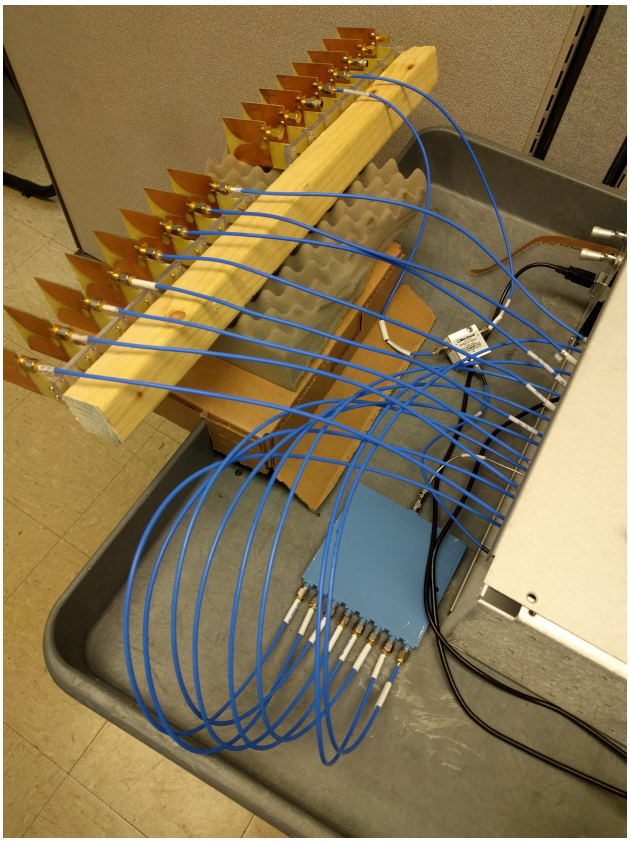

Figure D.1: Photo of the antenna configuration used for system testing

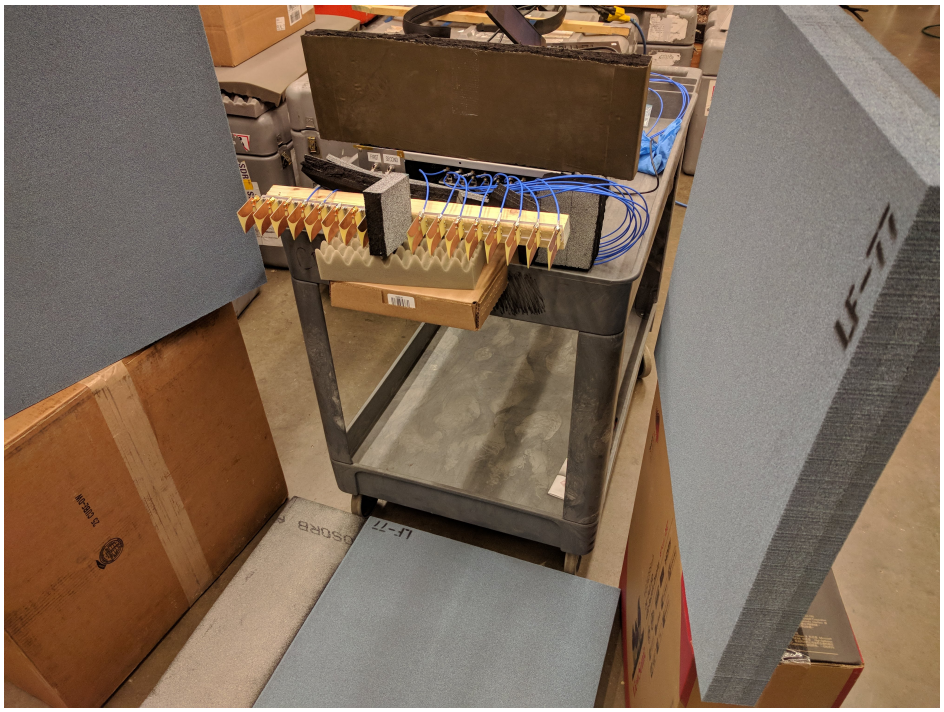

Figure D.2: Photo of the placement of RF absorbing foam around the radar

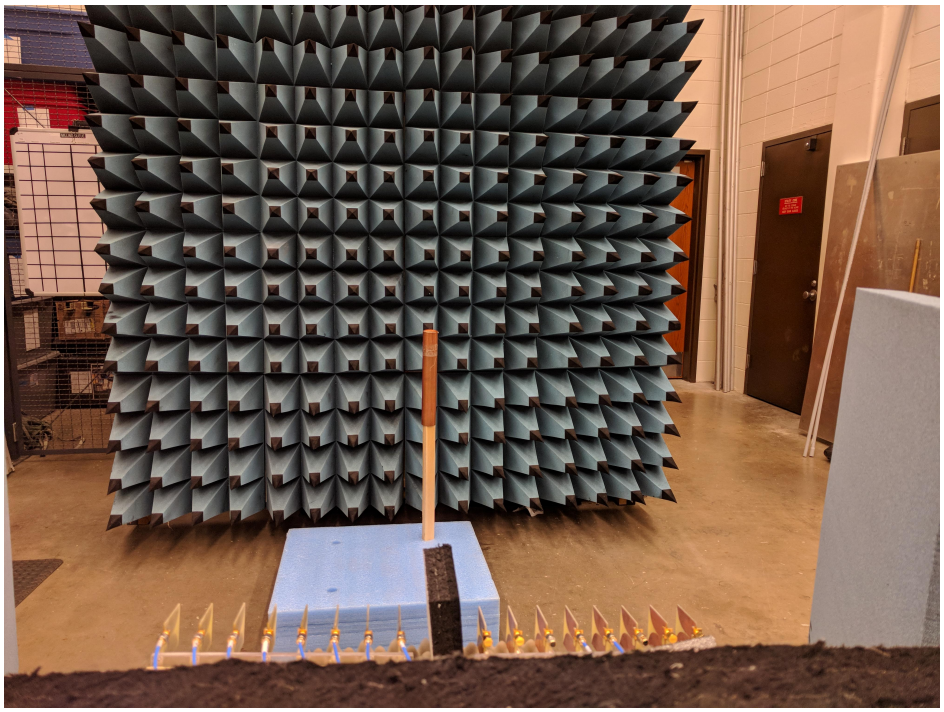

Figure D.3: Photo of the target and its placement relative to the radar. The wall of absorber is visible in the background.