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Modeling of gate capacitance of GaN-based trench-gate vertical metal-oxide-semiconductor devices

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We propose a model for the gate capacitance of GaN-based trench-gate metal-oxide-semiconductor transistors, based on combined measurements, analytical calculations and TCAD simulations. The trench capacitance is found to be equivalent to four different capacitors, used to model the various regions with different doping and orientation of the semiconductor/dielectric interface. In addition, we demonstrate and explain the characteristic double-hump behavior of the G-D and G-DS capacitance of trench-MOSFETs. Lastly, a TCAD simulation results accurately reproduce the experimental data, thus confirming the interpretation on the double hump behavior, and providing insight on the electron density at the gate interface. © 2020 The Japan Society of Applied Physics

GaN power devices have emerged as a novel technology^{1–5)} for application in high-efficiency power converters.^{6–8)} When aiming at high-voltage and high-power ratings, lateral GaN devices have some limitations,^{9–11)} such as the area occupancy and the sensitivity to surface trapping effects.^{12,13)} On the other hand, vertical devices allow to reach high-power densities and high currents without suffering surface trapping; the epitaxial stack can be grown on GaN substrates (vertical devices)^{14–19)} or on silicon substrates (semi-vertical technology).^{20–23)} This latter is a promising solution,²⁴⁾ since it allows to substantially reduce the fabrication costs.⁸⁾ One of the most promising vertical device structure is the trench-gate MOSFET; in order to limit the switching losses, it is fundamental to optimize device design, aiming to minimize the gate capacitance.^{25,26)} In a trench-MOSFET, the gate capacitance depends on the properties of the 3D trench, and its evaluation is not straightforward. Despite the importance of this topic, no study on the gate capacitance has been presented to date in the literature. The aim of this paper is to fill this gap, by presenting the first investigation on the shape of the capacitance–voltage characteristics of GaN-based trench-MOSFETs. We propose an analytical model for the gate capacitance and demonstrate the existence of a double-hump in the C_{GD} – V_{GS} curves. This effect is explained by considering the formation of electron layers in different semiconductor regions, as confirmed by TCAD simulation.

The tested devices are semi-vertical GaN-based transistors, grown on a 200 mm silicon substrate. The active region of the device is composed (top to bottom) of an $n^+/p/n^-/n^+$ GaN stack, as shown in Fig. 1. The 250 nm thick top n^+ layer is electrically connected to the source of the device, and acts as the access region to the inversion channel of the device, which is formed in the 400 nm thick p-layer. The 750 nm thick lowly doped n-layer represents the drift region, which undergoes depletion when the device is biased in the OFF-state. Lastly, the n^+ bottom layer favors the lateral carrier transport toward the drain deep-via, which routes the

electrons back to the top surface of the device. The buried n^+ layer lies on a complex strain-relief stack grown on a silicon substrate.

The gate module is a metal-oxide-semiconductor (MOS) stack, which controls the formation of an electron inversion layer in the p-GaN layer in a quasi-vertical plane. The gate dielectric is a 35 nm thick Al_2O_3 layer and is deposited on the sidewalls and on the bottom of a 950 nm deep etched trench. The length of the trench (Lgt in Fig. 1) is 4 μm , while its width (W) is 500 μm . The tested device has two gate fingers.

The gate CV measurements were carried out by means of a Keysight 4980A in three different configurations, defined as G-S, G-D, and G-DS, which are: source grounded and drain floating, source floating and drain grounded, and both drain and source grounded, respectively. The frequency and the amplitude settings of the AC signal were respectively 1 kHz and 50 mV.

In addition to the experimental tests, a TCAD simulation was carried out using the tool Sentaurus by Synopsys. The simulated structure is a simplified fully-vertical $n^+/p/n^-$ structure with the drain contact on the bottom. The geometrical and doping details of the device were reproduced. The gate capacitance behavior was simulated with both source and drain grounded (G-DS configuration).

Since the same gate-potential controls the electrostatic condition of differently doped semiconductors, the total gate dielectric capacitance was modeled by considering four different capacitive contributions depending both on the GaN/dielectric interface plane and on the semiconductor doping-type, as illustrated in Fig. 1. C_{n^+} , C_p , C_{n^-} and C_B represent the capacitance between the gate metal and the n^+ layer, the p-type layer, the n-layer (on the sidewall) and the n^- bulk (on the bottom), respectively.

The capacitances calculations were computed by multiplying the dielectric/GaN interface area of each contribution by the capacitance per unit of area; this latter was calculated as:

$$C_{\text{area}} = \frac{\epsilon_0 \cdot \epsilon_r}{t_{\text{ox}}} = 2.35 \cdot 10^{-7} \text{ F cm}^{-2} \quad (1)$$



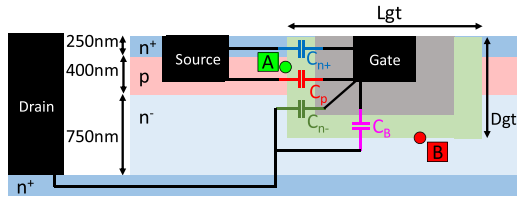


Fig. 1. (Color online) Schematic cross-section of the devices under analysis. Equivalent circuit of the gate trench capacitance, where the four capacitive contributions are highlighted.

The value of the relative permittivity ϵ_r of Al_2O_3 used for the calculation is 9.3.²⁷⁾

The dielectric/GaN interface area of each contribution was calculated by multiplying the total perimeter of the gate trenches [Eq. (2)] by the thickness of the respective layer corrected by the sidewall angle. The bottom area is calculated as shown in Eq. (3)

$$\text{Perimeter} = 2 \cdot (2 \cdot W + 2 \cdot \text{Lgt}) \quad (2)$$

$$A_{\text{bottom}} = 2 \cdot (W \cdot \text{Lgt}) \quad (3)$$

The gate capacitance was experimentally measured by sweeping the gate bias V_G from -5 to $+5$ V. Figure 2(a) shows the behavior of the gate capacitance measured in the G-S configuration (gate biased, source grounded and drain floating) as a function of the applied gate voltage (green line). The capacitance level is below 2 pF until the gate bias (V_G) reaches 3 V; beyond this voltage level, which corresponds to the threshold voltage (V_{th}) of the device under analysis, the capacitance sharply increases higher than 14 pF. The strong dependence on V_{th} indicates that the formation of the inversion channel in the p-GaN plays a key role in the gate CV. Moreover, it is worth noticing that, for gate voltages higher than V_{th} , the capacitance level approaches the analytical value of the total gate capacitance, which is 14.2 pF ($=C_{n+} + C_p + C_{n-} + C_B$). This demonstrates that the inversion channel in the p-layer short-circuits the accumulation channel present in the n^+ and in the n^- layers. In this condition, the whole gate dielectric is included between the gate metal and an electron sheet of charge in the whole trench area. Since the four capacitive contributions are thus connected in parallel, the equivalent gate capacitance is the sum of C_{n+} , C_p , C_{n-} , C_B [Fig. 2(c)].

Table I. Analytically calculated areas and capacitances values.

	Area [$\times 10^{-6} \text{ cm}^2$]	Capacitance [pF]
C_{n+}	5.36	1.26
C_p	8.58	2.02
C_{n-}	6.43	1.51
C_B	40	9.4

Measuring the gate capacitance in the G-D (gate biased, drain grounded and source floating) configuration leads to the observation of a double hump behavior [Fig. 2(a), red line]. The capacitance level is about 4 pF for negative voltages, from where a hump appears between 0 and 2 V which increases up to 11 pF. The measured capacitance after this first hump is the sum of C_{n-} and C_B with a theoretical value of 10.9 pF, as indicated in the box in Fig. 2(a). Indeed, within this voltage range, the inversion channel is not formed yet, meaning that the capacitance variation originates from the n^- drift region; the equivalent electric circuit is shown in Fig. 2(b). As the gate voltage increases, the n^- doped region shifts from a weak depletion regime to an accumulation regime, and an electron layer is formed at the n GaN/dielectric interface. Around V_{th} the capacitance shows a second hump, and it increases to 14.2 pF. As the inversion channel forms in the p-doped layer, a continuous channel is formed from n^+ -GaN to the bottom n^- -GaN, and the whole gate dielectric is included, over the whole trench area, between a sheet of electrons and the gate metal; this results in a total gate capacitance of 14.2 pF, as previously calculated.

The third tested measurement configuration is the G-DS, (gate biased, drain and source grounded) whose behavior is shown in Fig. 2(a), black line. At negative gate bias, only the n^+ -layer/dielectric interface might be in the accumulation regime, while the p^- and n^- -layers are in depletion. This means that the measured capacitance is the depletion capacitance of the semiconductor around the trench except for the n^+ -layer related gate area. As the gate voltage increases toward 2 V, the n^- doped region shifts from a weak depletion regime to an accumulation regime thus resulting in the increasing capacitance observed in the G-D configuration. Finally, as the gate voltage approaches V_{th} , the capacitance shows a second hump related to the formation of the inversion channel in the p-doped layer. At gate biases above the threshold, the whole gate trench area is included

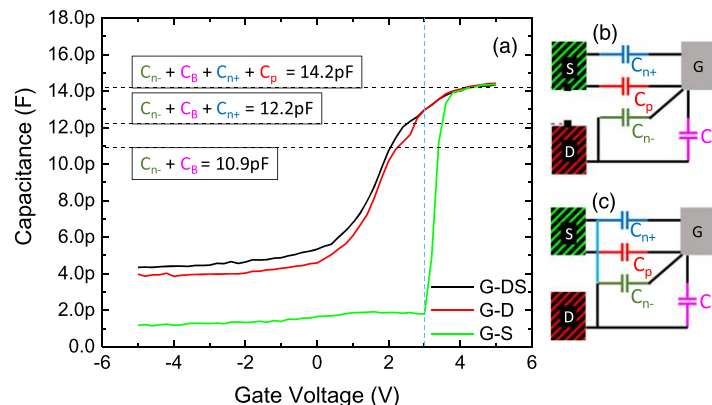


Fig. 2. (Color online) (a) Gate capacitance behavior measured with three different connection configurations, which are G-S, G-D, and G-DS. (b) Equivalent circuit either below the threshold voltage and (c) above the threshold voltage; blue line highlights the shorting caused by the inversion channel of the device.

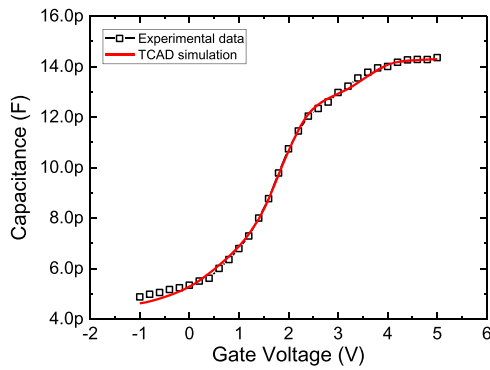


Fig. 3. (Color online) Comparison between TCAD simulation of the gate capacitance behavior in the G-DS configuration, depicted by the red line, and the measured data, represented by black squares.

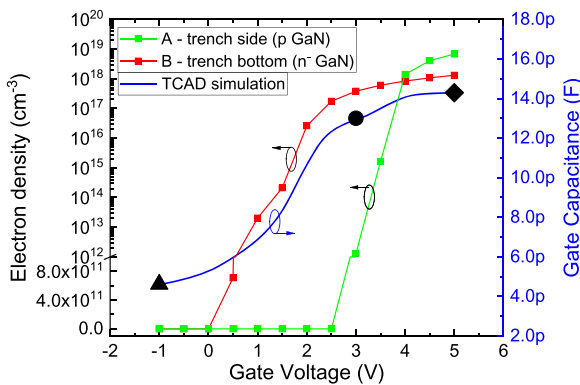


Fig. 4. (Color online) Electron density obtained from the simulation on the trench side either on the p-GaN layer (A in Fig. 1) and at the bottom of the trench (B in Fig. 1). Blue line represents the simulated gate CV; triangle, circle and diamond markers pin-point the gate voltages at which the cross-section view of the electron density is shown in Fig. 5.

between the gate metal and a sheet of electrons. The resulting capacitance is slightly higher than 14 pF, which again, is in agreement with the analytical calculations of the total trench capacitance, i.e. 14.2 pF. It is worth noticing [Fig. 2(a)] that, for gate voltages below V_{th} , there is an offset between the capacitance measured in the G-D configuration, and the one measured in the G-DS configuration; this offset is related to the C_{n+} capacitance, whose contribution is always present in the G-DS configuration, whereas it is only measured at gate voltages higher than V_{th} in the G-D configuration. This hypothesis is confirmed by comparing the theoretical values

at $V_G = 2$ V (indicated inside the pink and the blue boxes) in Fig. 2.

The TCAD simulation of the gate capacitance over the applied gate voltage was carried out by simulating the G-DS configuration. Figure 3 shows that the simulation is able to accurately reproduce the experimental data, including the double hump behavior previously described.

In order to confirm the model discussed in the previous section, the electron density at the dielectric/semiconductor interface was extrapolated at the trench bottom (marker B in Figs. 1 and 5) and in the p-doped layer, where the channel of the transistor is formed (marker A in Figs. 1 and 5). Figure 4 shows the behavior of the electron density at A and B as a function of the gate bias, and as a function of the CV behavior. The electron density at the bottom of the trench starts increasing at about $V_G = 1$ V (Fig. 4, red line), in correspondence with the first capacitance hump, which is thus related to the formation of an accumulation layer on the trench bottom. The latter acts as a planar plate of a capacitor composed by the gate metal and the gate dielectric. A similar dependence between the onset of the second hump in the CV and the electron density in the p-GaN region can be observed in Fig. 4 (green line). In this case, the electrons in p-GaN layer, which is the channel of the device, originates from an inversion regime.

Three cross sections of the simulated structure with a color map indicating the electron density profile at $V_G = -1$ V, 3 V, and 5 V (respectively triangle, circle and diamond markers in Fig. 4) are shown in Fig. 5. It is worth noticing that at $V_G = -1$ V the semiconductor close to the trench is completely depleted, whereas an accumulation layer is formed in the n⁻-doped GaN at $V_G = 3$ V. In this gate bias condition, the inversion layer in the p-GaN is not formed yet. Lastly, as the gate bias becomes higher than V_{th} and the inversion layer is formed, an electron layer is present along the whole trench area.

Concluding, this paper proposes a model explaining the gate capacitance behavior of a vertical trench-gate MOS device. The gate capacitance was split in four capacitive elements that contribute to the total gate capacitance, depending on the condition of the GaN at the dielectric/semiconductor interface. Moreover, a TCAD simulation which accurately reproduces the experimental results, shows the variation of the electron density in different regions of the device under varying gate bias conditions.

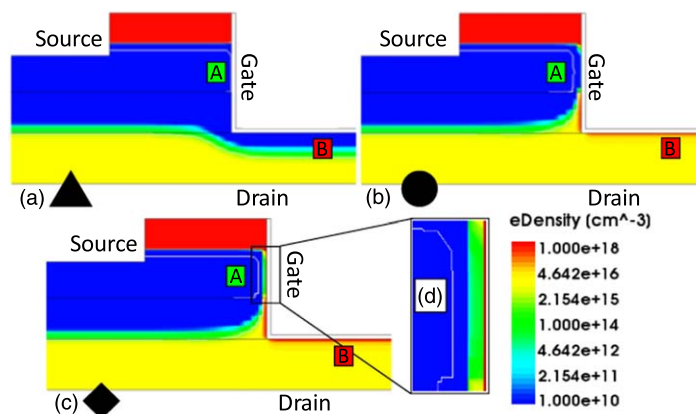


Fig. 5. (Color online) Cross-section view of the electron density at three different bias conditions, which are $V_G = -1$ V (a), $V_G = 3$ V (b), $V_G = 5$ V (c).

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