

Surface-Potential-Based Compact Model for the Gate Current of p-GaN Gate HEMTs

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Abstract—The gate leakage current of p-GaN gate HEMTs is modeled based on surface potential calculations. The model accurately describes the bias and temperature dependence of the gate leakage. Thermionic emission is the main mechanism of the gate current in forward bias operation while hopping transport component is the main mechanism of gate current in reverse bias operation. This newly developed gate current model was implemented in Verilog-A. A good agreement between the simulations and experimental data demonstrates the accuracy of the model.

Index Terms—Equivalent circuit model, gate current, p-GaN gate high-electron mobility transistors, transport model.

I. INTRODUCTION

TO DATE, AlGaIn/GaN heterojunctions grown on large-size and low-cost silicon substrates are the building blocks of GaN-based high power devices [1]–[3]. In circuits, enhancement-mode (E-mode) transistors are preferred for their normally OFF characteristics and ease of implementation. One of the approaches to obtain E-mode transistors is to use a p-GaN gate that lifts up the conduction band at the channel surface in equilibrium [4]. Now the p-GaN gate devices are the first commercialized E-mode devices due to their good stability, high threshold voltage, and low ON-resistance. On top of the p-GaN gate, the metallization layer can be an ohmic metal or a Schottky metal contact to the p-GaN. Using Schottky metal is superior to the ohmic metal in terms of higher V_{th} and lower gate leakage current. However, the gate current in p-GaN-gated HEMTs is higher than in metal insulator semiconductor high electron mobility transistors (MISHEMTs) where a gate dielectric is used. This high gate leakage current [5]–[10] can cause electrical reliability problems and result in reduced device performance, such as degradation of breakdown voltage [11], and an increase in noise figure [12].

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It is important to develop a physics-based gate leakage current model, especially in circuits where the gate current can significantly charge the gate capacitor, or the gate terminal is loaded with high impedance [13]. Accurate modeling of the gate current is also useful in the design of digital and analog circuits and power-switching devices because the gate current can cause erroneous circuit operation at negative drain current, affecting the circuit function. Therefore, an in-depth investigation of the gate leakage is necessary. So far, there is no physics-based model to describe the gate leakage in p-GaN gate HEMTs.

The conventional empirical models such as the Curtice model [14], the Statz model [15], and the Angelov–Chalmers model [16] are mostly empirical curve-fitting models. The table-based models [17] hardly describe the whole characteristic of the gate current for they lack predictive capability and are strictly limited to the test system and condition. Two industrial standard models were recently elected by the Compact Model Council (CMC): the MIT Virtual Source GaN model [18], originally developed for highly scaled Si-FETs with a quasi-ballistic mode of transport, adopting a different interpretation of the carrier velocity by using an empirical saturation function for GaN HEMTs. The second one is the advanced SPICE model (ASM) [19], using a surface-potential (SP)-based approach to capture terminal characteristics in GaN HEMTs by solving Schrödinger–Poisson coupled equations. Recently, a charge-based HEMT model was developed by Ecole Polytechnique Federale de Lausanne (EPFL) [20] starting from a physics-based model for regular silicon FETs and adding new physical quantities typical for HEMTs. This model uses all the techniques of MOSFET compact models regarding the numerical efficiency and convergence robustness.

Previously, we have reported a SP-based model for Schottky gate GaN HEMTs [21], which solved the problem of elaborating computations of the SP by using an approximate analytical solution [22]. In this article, we present an SP-based model for p-GaN gate HEMTs which consider explicitly within the Poisson equation all possible induced charges: the polarization charge at the AlGaIn/GaN interface, the active Mg doping in the GaN channel caused by out-diffusion and holes. Our SP-based model can precisely describe the dc characteristics in different operation regions with the detailed device physics of p-GaN gate HEMTs. Furthermore, this work also discusses further insights into the gate leakage and the electrostatic potential distribution within the p-GaN gate-stack. We propose a model in which two junctions are connected in series (the Schottky junction is connected in series with the heterojunction), to correctly describe the carrier transport

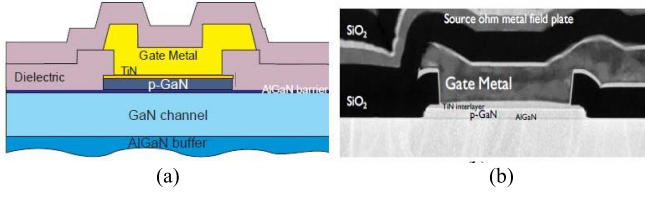


Fig. 1. (a) Schematic and (b) X-TEM micrograph of a Schottky metal/p-GaN gate AlGaIn/GaN HEMT.

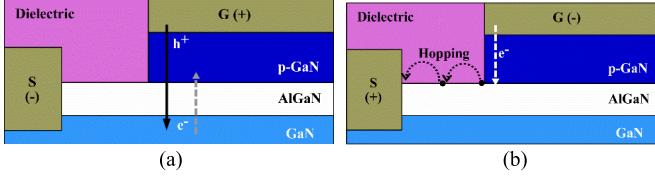


Fig. 2. Schematic cross-sectional views showing the gate current conduction mechanism under different V_G . (a) $V_G > 0$ V and (b) $V_G < 0$ V.

characteristics in the p-GaN gate HEMTs [5]. A reverse bias gate leakage current conduction mechanism based on the hopping transport (HT) and a forward-bias gate leakage current conduction mechanism based on thermionic emission (TE) are presented. The model is valid for all operation conditions. The gate current model is implemented in our SP-based compact model for p-GaN gate HEMTs, which is in excellent agreement with experimental data at different temperatures.

This article is organized as follows. In Section II, we present the device structure and SP calculations. We verify the SP-based model against the measurement data. In Section III, we focus on the gate current calculation and verification. The derivation of the current equations for TE and HT and the gate current equivalent circuit model are presented. The model implementation, parameter extraction, and experimental validation are shown. Finally, the conclusion is drawn in Section IV.

II. DEVICE STRUCTURE AND SP CALCULATIONS

The p-GaN gate HEMTs were fabricated in IMEC's 200-mm pilot line using an Au-free process flow; details of the process flow are described in [23]. The schematic cross section of a Schottky metal/p-GaN gate HEMT is shown in Fig. 1. Fig. 2 depicts the schematic cross-sectional view of the p-GaN gate HEMT under different V_G .

In order to obtain the electrostatic potential of the p-GaN gate HEMTs, the 1-D Poisson equation is solved in the GaN channel layer, in which the carrier density was determined by the polarization charges and the p-GaN gate at equilibrium. The Poisson equation includes possible carriers' density under the approximation that the charge in the GaN channel layer dominates the potential bending. The potential φ is evaluated in the gradual channel approximation, which assumes that the variation of the electric field along the channel (y -direction) is much less than that in the x -direction. The coordinate x is measured from the AlGaIn–GaN interface in the direction perpendicular to this interface.

For completeness, we included holes in the Poisson equation

$$d^2\varphi/dx^2 = q/\varepsilon_{\text{GaN}} \cdot (n_{\text{GaN}} + N_{\text{Mg}} - p_{\text{GaN}}) \quad (1)$$

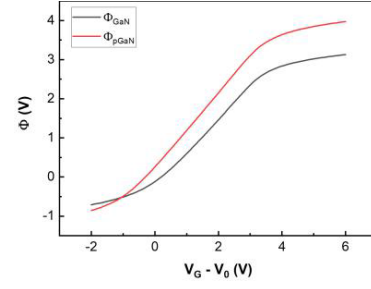


Fig. 3. Calculated φ_{GaN} and φ_{pGaN} with $V_G - V_0$.

where ε_{GaN} is the permittivity of GaN, N_{Mg} is the unintended Mg doping in the channel caused by out-diffusion, n_{GaN} and p_{GaN} are the electrons and holes charge density in the GaN channel layer, respectively. The n_{GaN} and p_{GaN} are written as

$$n_{\text{GaN}} = n_{i_ \text{GaN}} \cdot \exp[(\varphi - \Phi_F - V_C)/V_T] \quad (2)$$

$$p_{\text{GaN}} = n_{i_ \text{GaN}} \cdot \exp[(-\varphi + \Phi_F)/V_T] \quad (3)$$

with $n_{i_ \text{GaN}}$ is the intrinsic carrier density, V_C is the voltage applied between the channel and the substrate, $\Phi_F = V_T(\ln(N_0/n_i) + 2^{-1.5}(N_0/n_i))$ [24] is the quasi-Fermi potential. The channel carrier density N_0 is approximately equal to the sum of electron density and hole density, V_T is the thermal voltage ($= kT/q$).

The boundary conditions are

$$\varphi(x) = 0 \quad \text{for } x \rightarrow \infty \quad (4)$$

$$d\varphi(x)/dx = 0 \quad \text{for } x \rightarrow \infty. \quad (5)$$

At the surface, $x = 0$, $\varphi = \varphi_{\text{GaN}}$. With the two-order integral of (1), we can get the alternative form (6), which is called the SP equation (SPE)

$$V_G - V_0 - \varphi_{\text{GaN}} = \gamma \sqrt{\frac{\frac{\varphi_{\text{GaN}}}{V_T} N_{\text{Mg}} + n_{i_ \text{GaN}} \exp\left(\frac{-\Phi_F - V_C}{V_T}\right) \left[\exp\left(\frac{\varphi_{\text{GaN}}}{V_T}\right) - 1\right]}{+ n_{i_ \text{GaN}} \exp\left(\frac{\Phi_F}{V_T}\right) \left[\exp\left(-\frac{\varphi_{\text{GaN}}}{V_T}\right) - 1\right]}} \quad (6)$$

In (6), γ is the body factor, φ_{GaN} is the SP at the AlGaIn/GaN layer interface, V_0 is a fitting parameter such that the $\varphi_{\text{GaN}} = 0$ when $V_G = V_0$.

Equation (6) describes all regions of GaN HEMT operation. We use an advanced noniterative algorithm [22] to solve (6) and get the analytical approximation of φ_{GaN} which is an implicit function of the gate bias voltage. The analytical algorithm is adopted in our model in order to eliminate the internal iterative loops and corresponding convergence issues, resulting in computationally efficient calculations. This algorithm includes the third-order Taylor expansion and subsequent linearization of the square root. In addition, the closed-form analytical approximation for the SP uses smoothing functions [25] to connect asymptotic solutions of (6) in sub-threshold and other operation conditions. A detailed derivation can be found in [22].

With the same noniterative methodology [22], the analytical approximation of the SP at the p-GaN/AlGaIn layer interface φ_{pGaN} can be calculated. The results are shown in Fig. 3.

In the p-GaN gate HEMTs compact model, the gradual-channel approximation is used. This current model adopts the

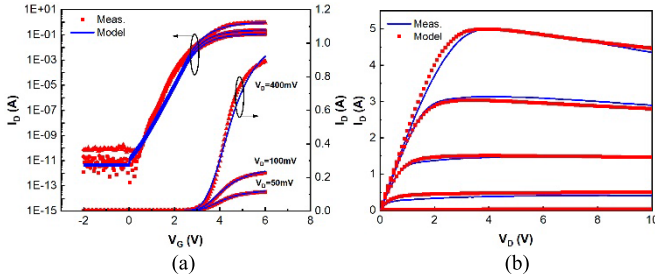


Fig. 4. I - V characteristic of the SP-based model. (a) I_D - V_G with V_D from 0.05 to 0.4 V. (b) I_D - V_D with V_G from 0 to 7 V.

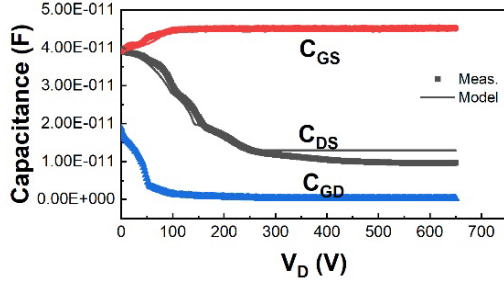


Fig. 5. C - V characteristics of the SP-based model (line) are compared with measurement data (dot) as a function of the drain voltage V_D .

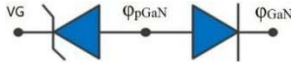


Fig. 6. Two-junctions equivalent circuit model of the gate structure of the p-GaN gate HEMT.

channel current equation of the thin layer charge model [26]

$$I_D = -\mu W \left(q_i \cdot \frac{d\phi_{\text{GaN}}}{dy} - V_T \cdot \frac{dq_i}{dy} \right) \quad (7)$$

where I_D is the drain current, q_i is the charge density in the GaN channel, μ is the electron mobility, and W is the gate width.

We have validated the proposed SP-based compact model using I - V and C - V measurement data of a four-field plate p-GaN gate high-power HEMT device with a total width of 36 mm and a gatelength of 1.5 μm . The model is in good agreement with the measured currents and capacitances as shown in Figs. 4 and 5.

III. GATE CURRENT MODEL

A. Two-Junctions Equivalent Circuit Model

In p-GaN gate HEMTs, the gate contact metal (TiN) and p-GaN form a Schottky junction that can effectively reduce the gate current of the HEMTs in the ON-state. The p-GaN and AlGaIn/GaN layer form a p-GaN/n-GaN junction. Therefore, in this article, we propose a two-junction model in which the Schottky junction is connected in series with a heterojunction [p(p-GaN)-n(AlGaIn/GaN)] as shown in Fig. 6.

B. TE Model

At $V_G > 0$ V, the Schottky junction is reverse biased while the p-GaN/n-GaN junction is forward biased. The reverse thermally assisted tunneling current through the Schottky junction and TE over the heterojunction as depicted in Fig. 2(a) [5].

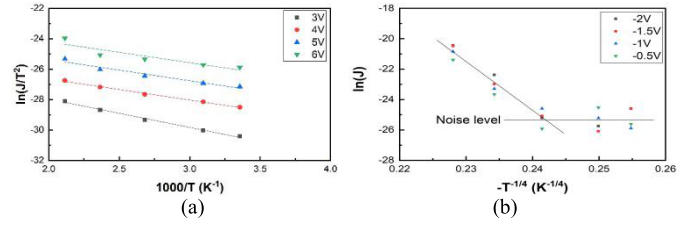


Fig. 7. Measured gate current versus temperatures for (a) $V_G > 0$ V and (b) $V_G < 0$ V.

TABLE I

GATE CURRENT PARAMETERS AT 300 K

Parameter	J_{TE0}	n_{TE}	J_{HT0}	n_{HT}
Extracted	1e-15	0.12	2e-12	14

The temperature dependence of the measured gate leakage current exhibits a linear behavior of $\ln(J/T^2)$ versus T^{-1} at $V_G > 0$ V as seen in Fig. 7(a). Hence, the gate current can be expressed as [27]

$$J_{TE} = \text{Area} \cdot J_{TE0} \cdot T^2 \cdot \left[\exp\left(\frac{\phi_{\text{pGaIn}} - \phi_{\text{GaIn}}}{n_{TE} \cdot V_T}\right) - 1 \right] \quad (8)$$

where Area is the area of the gate, J_{TE0} is the forward saturation current density, which depends on the AlGaIn barrier height; and n_{TE} is the ideality factor.

C. HT Model

At $V_G < 0$ V, the Schottky junction is forward biased while the p-GaN/n-GaN junction is reverse biased, and the gate current is determined by the reverse leakage current in the heterojunction. The gate current is perimeter dependent [5], indicating that the gate leakage path is at the edge of the p-GaN gate, where electrons have a large probability to transport along the AlGaIn surface through hopping to the source-drain, as in Fig. 2(b) [18]. Meanwhile, the gate leakage current at $V_G < 0$ V shows an exponential relationship with temperature ($\ln(J) \propto \exp(-T^{-0.25})$) from the measurement data in Fig. 7(b), which also proves the existence of the hopping mechanism [28].

Based on the discussion above, we develop a HT model and determine the gate current empirically by the following equation:

$$J_{HT} = \text{Peri} \cdot J_{HT0} \cdot \left[\exp\left(\frac{\phi_{\text{pGaIn}}}{n_{HT} \cdot V_T}\right) - 1 \right] \cdot \exp[-T^{-\alpha}] \quad (9)$$

where Peri is the perimeter of the gate, J_{HT0} is the reverse saturation current density which is dependent on the p-GaN barrier height, n_{HT} is the ideality factor, and α is the temperature coefficient of $\alpha = 0.25$.

D. Parameter Extraction and Experimental Validation

Due to the different charge transport mechanisms, the gate current has two components, namely the TE and HT components. Each component has its own set of parameters, the values of which are given in Table I.

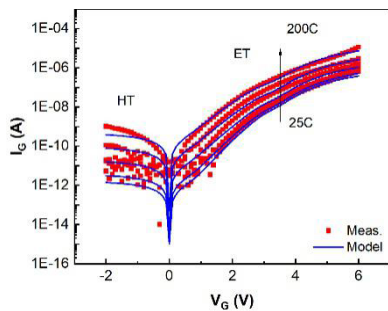


Fig. 8. Measurement (dots) and simulation (lines) data of gate current at different temperatures.

The calculated SP of the p-GaN layer and the GaN channel, $\phi_{p\text{GaN}}$ and ϕ_{GaN} in Fig. 3 can be used to find the gate current determined by the thermal emission equation at $V_G > 0$ V, and by the HT equation at $V_G < 0$ V. The model can be easily implemented in Verilog-A. In Fig. 8, the gate current model is verified against the measured gate current at different temperatures from room temperature to 200 °C at $V_{\text{DS}} = 0.1$ V. The figure shows an excellent agreement between the model and the measurement for both branches of $V_G > 0$ V and $V_G < 0$ V.

IV. CONCLUSION

In this article, we have investigated the mechanisms of gate leakage current behavior based on the proposed physical model in p-GaN gate HEMTs. HT and TE are proposed to describe the gate I leakage conduction mechanisms. The gate leakage current is modeled and implemented in a physical SP-based p-GaN gate HEMTs compact model. The model and measurements exhibited a good agreement for different temperatures. This model is ready to be deployed in the SP-based p-GaN gate HEMTs model and is an important step toward developing a complete compact model for these devices.

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