High-density interconnect technology assessment of printed circuit boards for space applications

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Abstract
High density interconnect (HDI) printed circuit boards (PCBs) and associated assemblies are essential to allow space projects to benefit from the ever increasing complexity and functionality of modern integrated circuits such as field programmable gate arrays (FPGAs), digital signal processors (DSPs) and application processors. Increasing demands for functionality translate into higher signal speeds combined with an increasing number of I/Os. To limit the overall package size, the contact pad pitch of the components is reduced. The combination of a high number of I/Os with a reduced pitch places additional demands onto the PCB, requiring the use of laser drilled microvias, high aspect ratio core vias and small track width and spacing. While the associated advanced manufacturing processes have been widely used in commercial, automotive, medical and military applications; reconciling these advancements in capability with the reliability requirements for space remains a challenge. Two categories of HDI technology are considered: two levels of staggered microvias (basic HDI) and (up to) three levels of stacked microvias (complex HDI). In this paper, the qualification of the basic HDI technology in accordance with ECSS-Q-ST-70-60C is described. At 1.0 mm pitch, the technology passes all testing successfully. At 0.8 mm pitch, failures are encountered during interconnection stress testing (IST) and conductive anodic filament (CAF) testing. These failures provide the basis for updating the design rules for HDI PCBs.

Introduction

Two main drivers are commonly identified for HDI PCBs: (1) the small pitch and high number of I/Os of key components and (2) the increasing performance of these components resulting in high-speed signal lines on the boards. The use of microvias allows to reduce the length of the signal path, improving both signal integrity and power integrity. Critical nets may suffer from crosstalk due to the dense routing within the fanout. The routing of differential pairs in between the pins of a 1.0 mm pitch component requires fine line widths and spacing. Differential pair routing in between the buried vias for 0.8 mm pitch components is no longer possible. The pairs need to be split within the fanout area and the effect on signal integrity will depend on the length of the split. The change in width on single-ended nets, as well as a change in the spacing and/or trace widths of a differential pair will cause an impedance discontinuity. Choosing the appropriate layer build-up and via types will thus improve both route-ability and signal integrity.

An important consideration in the definition of technology parameters for HDI PCBs is that component pitch and the number of I/Os cannot be addressed independently. A high pin count component (> 1000 pins) with 1.0 mm pitch can require the use of microvias to reduce the total layer count or to improve the shielding of controlled impedance lines. On the other hand, the escape routing of a 0.5 mm pitch component with only two rows of solder balls can be performed without microvias and fine line widths and spacing. Increasing the layer count to be able to route one or more high pin count components will result in an increase in PCB thickness, which impacts the minimum via drill diameter through limitations on the via aspect ratio and thus again restricts routing possibilities.

In order to define the HDI technology parameters, the specifications of area array devices (AADs) used in past, present and future space projects need to be known. Looking into the complex components for space that are currently under development, the ceramic column grid array (CCGA) with a pitch of 1.0 mm will remain the package of choice for the coming years. This is, for example, the case for the new Xilinx FPGA (RT-ZU19EG: CCGA1752) [1], the CNES VT65 telecom ASIC (CCGA1752) [2] and European Space Agency's (ESA) Next Generation Microprocessor (NGMP, CCGA625) [3]. Column grid arrays with smaller pitch (0.8 mm) have been demonstrated in R&D [4], although no commercial implementations have been found. Ceramic ball grid arrays (CBGAs) with non-collapsing, high Pb solder balls are used in military and aerospace applications [5]. At 0.8 mm pitch and beyond (0.5 mm), ceramic (i.e. hermetic) packages become a reliability risk as the smaller

solder balls can no longer support the coefficient of thermal expansion (CTE) difference between package and board. A recent NASA study therefore investigated the reliability of plastic ball grid arrays (PBGAs) with up to 1704 pins at 1.0 mm pitch and 432 I/Os at 0.4 mm pitch [6].

Increasing the capability for dense routing, signal integrity at high speeds and a high number of I/Os undoubtedly has its impact on reliability. Reducing line width and spacing, via pad size and drill diameters all influence the manufacturing yield and quality and thus present a reliability risk. New materials need to be introduced to corroborate the increasing capability demands without diminishing the reliability standards.

High-density interconnect PCBs have been used for over three decades and are currently applied in all markets. Numerous studies on HDI technology and its reliability have been published. The returning theme in almost all HDI technology studies is that the technology can be very reliable, if manufactured properly. Process control and quality assurance are key to reliable HDI PCBs.

HDI technology parameters

To derive the requirements for HDI PCBs in space projects, stakeholders such as prime satellite contractors, equipment manufacturers, space agencies, ESA qualified PCB manufacturers, ESA technical officers and independent CAF experts were consulted. The starting point was the current HDI PCB section of the PCB and Assembly Technologies Roadmap for Space Applications [7]. A questionnaire was compiled to determine the drivers and technology parameters for HDI PCBs for near-term space projects (2018-2020) and future space projects (2020-2025). Feedback from the PCB/SMT working group members and other stakeholders was requested to specify the technological need while keeping in mind the possible repercussions on manufacturability and reliability. Starting from the functional requirements and component needs for future space projects, a set of advanced technology parameters is derived.

From the stakeholder feedback, it became clear that the split into technology for near-term and future projects was not satisfactory as higher complexity was required in the near-term as well. The decision was made to differentiate between *basic HDI technology*, intended for qualification within the project, and *complex HDI technology* including more advanced technology parameters. The stakeholders confirmed the large FPGA components, based on 1.0 mm pitch CCGA packages with up to 1752 pins, as primary drivers for the basic HDI technology. In addition, AADs with 0.8 mm pitch and a few hundred I/Os should be compatible with the basic HDI technology. Other driving components are small passives (0402 chip components) and fine-pitch lead frame components (QFP 0.5 mm) when routing space is limited. In future projects, components will have up to 2000 to 3000 I/Os and will use AADs with 0.8 and 1.0 mm pitch. These will likely be non-hermetic polymer based packages (PBGA), as a package size of 45 mm x 45 mm for ceramic packages is the limit in terms of CTE mismatch. A further reduction in pitch to 0.5 mm pitch is expected for low I/O (200 – 300) and for memory devices.

The HDI technology parameters for basic and complex HDI can be found in Table 1. The basic HDI technology consists of a single-sequence core with two levels of copper-filled microvias. Two levels of microvias is considered sufficient to route the AADs with 0.8 mm and 1.0 mm pitch. To minimize the reliability risk, the microvias are staggered with respect to each other and to the buried via in the core. Filling of core vias with prepreg from the HDI layers is preferred and two sheets of prepreg are applied.

The complex HDI technology will use three levels of microvias. The microvia configuration of choice is the semi-stacked option consisting of two stacked microvias plus one staggered microvia. Stacking three levels of microvias is considered a reliability risk. An IST prescreening is performed within the project to determine if the semi-stacked microvia configuration can meet the required reliability. If this is not the case, the full staggered configuration will be used as backup solution. Via plugging and capping will be used for the buried vias in the complex HDI technology. The effect on reliability of removing the non-functional pads and back drilling of the buried vias will be investigated as part of the complex HDI technology evaluation.

Polyimide remains the material of choice for HDI PCBs in space applications. To accommodate the needs for RF and high-speed digital applications, Panasonic Megtron 6 is included in the complex HDI technology evaluation. Low in-plane CTE materials are not seen as a priority for HDI in future projects. The use of a single sheet of prepreg for the microvias will be evaluated.

Solder mask is a requirement for the complex HDI technology. Other surface finishes (ENIG, ENIPIG, ENEPIG, and EPIG) are of interest, but the focus of the project is not to evaluate alternative surface finishes. The complex HDI technology will be evaluated with both ENIG and ENEPIG (one finish per base material).

Table 1 - HDI technology parameters for basic and complex HDI technology

Technology parameter	basic HDI	complex HDI
Conductor width and spacing, as-designed	75 µm line width and 75 µm spacing on non-plated inner layers (17 µm Cu foil); 120 µm line width and 100 µm spacing on plated inner layers (12 µm Cu foil with plating).	50 µm line width and 50 µm spacing on non-plated inner layers (12 µm Cu foil); 100 µm line width and 100 µm spacing on plated inner layers (12 µm Cu foil with plating).
Configuration of microvias	Two levels of microvias, staggered, Cu filled, 175 µm diameter as-designed.	Three levels of microvias, Cu filled, 125 µm diameter as-designed. Semi-stacked preferred, all staggered as backup.
Number of layers	≤ 20	≤ 26
Construction of HDI layers	Staggered to core, two sheets of prepreg.	Staggered to core, one sheet of prepreg.
Aspect ratio of core vias	≤ 8	≤ 10
PCB thickness	2.8 mm	Approx. 3 mm
Filling medium for core vias	Prepreg (from HDI layers)	Via plugging (with cap plating)
Construction of core	Single sequence, 300 µm drill diameter and 600 µm pad diameter for buried vias.	Single sequence, 250 µm drill diameter and 550 µm pad diameter for buried vias.
Back drilling	No	Back drilling on core
Presence of non-functional pads	As per ECSS-Q-ST-70-12C [8]	Full pad stack removed on core vias
Dielectric material	Polyimide (Ventec VT-901)	Polyimide (Ventec VT-901)
RF material	No	Panasonic Megtron 6
Surface finish and solder mask	SnPb, no solder mask	ENIG or ENEPIG with solder mask

Project plan

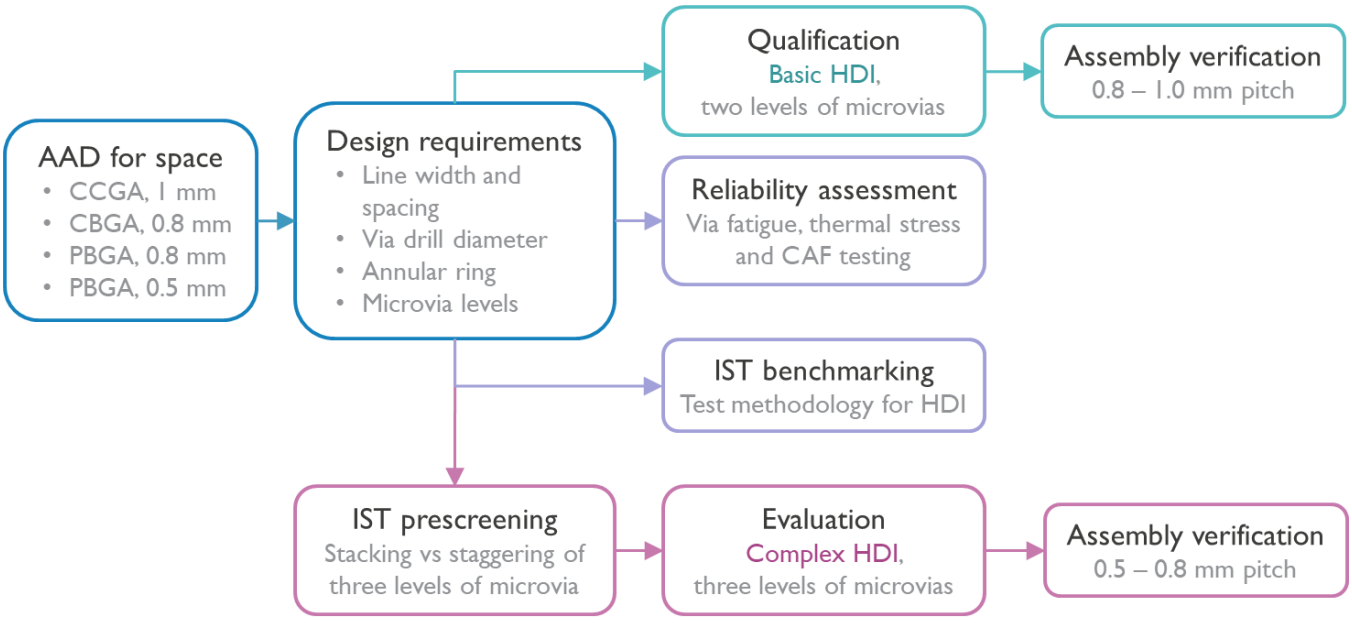


Figure 1 - Overall concept for the HDIPCB project

Figure 1 shows the overall concept for the HDIPCB project. During a stakeholder workshop, the relevant AADs for space applications were identified. Based on the mechanical (pitch, number of pins) and functional (data rate, controlled impedance) requirements of these components, the technology parameters and associated design rules were determined. The goal is to achieve qualification status for the basic HDI technology. The PCB qualification is followed by assembly verification for 1.0 mm pitch CCGA1752 and 0.8 mm pitch CBGA323 components. Before launching the evaluation of the complex HDI technology, an IST prescreening will be performed to decide on the use of stacked or staggered microvias. The evaluation of the complex HDI technology may lead to formal qualification for all or a subset of the technology features, depending on the occurrence of nonconformances in the evaluation. The subsequent assembly verification for 0.8 mm and 0.5 mm pitch PBGA components will be approached in the same manner, with the focus on evaluating the performance and identifying uncertainties.

Next to the qualification and assembly verification activities, an extensive HDI reliability assessment is performed. The study focusses on three aspects: thermal reliability, microvia testing and CAF testing. The via fatigue and thermal stress evaluations will be correlated with modelling of the bare PCB. For CAF testing, a dedicated test vehicle is designed to match the requirements of the HDI technology parameters. An extensive test campaign using thermal cycling, convection and vapor phase reflow assembly simulation, and interconnection stress testing (IST) will be undertaken.

In this paper, the test vehicles, test methods and test results for the HDI qualification in accordance with ECSS-Q-ST-70-60C [9] are described. The outcome of thermal cycling, IST and CAF testing is discussed. Other activities within this project will be published elsewhere over the course of the project.

Test Vehicles

The Qualification Test Vehicle (QTV) consists of a full panel design, including the following features.

- Test structures for HDI qualification test flow
    - Coupon A/B with through-going vias and component holes
    - Coupons B1, B2 and B3 for the microvia level 1, microvia level 2 and the buried vias, respectively
    - Coupon E for intralayer insulation resistance and dielectric withstanding voltage
    - Coupon H for interlayer insulation resistance and dielectric withstanding voltage
    - Coupon P for peel strength on outer layers
    - TVX and SLX procurement IST coupons
- Coupons for outgoing inspection as detailed in clauses 8.2.2 and 8.2.3 of ECSS-Q-ST-70-60 [9]
- BGA coupon which mimics (part of) an actual HDI PCB design
    - Real and daisy-chain component fanout for 1.0 mm and 0.8 mm pitch component
        - CCGA, 1.0 mm pitch, 1752 I/Os (Xilinx Virtex 5QV FPGA)
        - CBGA, 0.8 mm pitch, 323 I/Os (Teledyne e2v EV12AQ600 ADC)
    - Routing to Axon Nano-D (1.27 mm) and Smiths connectors KVPX (1.35 mm)

The BGA coupon (Figure 2) mimics (part of) an actual HDI PCB design and acts as “PCB” for the qualification test flow. The real component fanout for 1.0 mm and 0.8 mm pitch components are based on the actual pinout diagrams for the Xilinx Virtex 5QV FPGA and the Teledyne e2v EV12AQ600 ADC, respectively. Controlled impedance differential pair routing was applied to all relevant output pins. As high-density connectors can impose restriction on routing and are thus also driving components for HDI, two candidates are included in the BGA coupon. The differential pair interconnections of the Xilinx Virtex 5QV FPGA component fanout are routed to eight KVPX connectors. The fanout of the Teledyne e2v EV12AQ600 is combined with the Axon nano-D connector.

Two levels of staggered microvias can be implemented in different ways. For the 1.0 mm pitch fanout, the component pad is placed directly above the buried via. The microvia between layer 1 and 2 is placed partially inside the component pad. The capture pad of the microvia between layer 2 and 3 is tangent to the target pad of microvia 1-2. The target pad of microvia 2-3 is connected to the buried via using a short trace. The advantage of this microvia configuration is that microvia 1-2 is not located above the buried via, although the short trace between microvia 2-3 and the buried via sees higher stress than when the pads are tangent. The same configuration cannot be applied for the 0.8 mm pitch fanout as there is not enough space next to the buried via. The component pad, with microvia 1-2 partially inside the pad, is located above the buried via. Due to the smaller pad size, the microvia 1-2 is located above the buried via which is considered a reliability risk. The target pad of microvia 2-3 is placed tangent to the pad of the buried via on the opposite side of the buried via.

Two IST coupon designs are included on the panel to cover the most critical design features of the BGA coupon. Next to a TVX coupon for through-going vias, an SLX coupon with buried vias and microvias at 0.8 mm pitch is included (microvia configuration as described above). This SLX coupon contains three sense circuits: buried via (S1), buried plus microvias (S2), and staggered microvias (S3). The coupons are placed on the panel in close proximity of the BGA coupons.

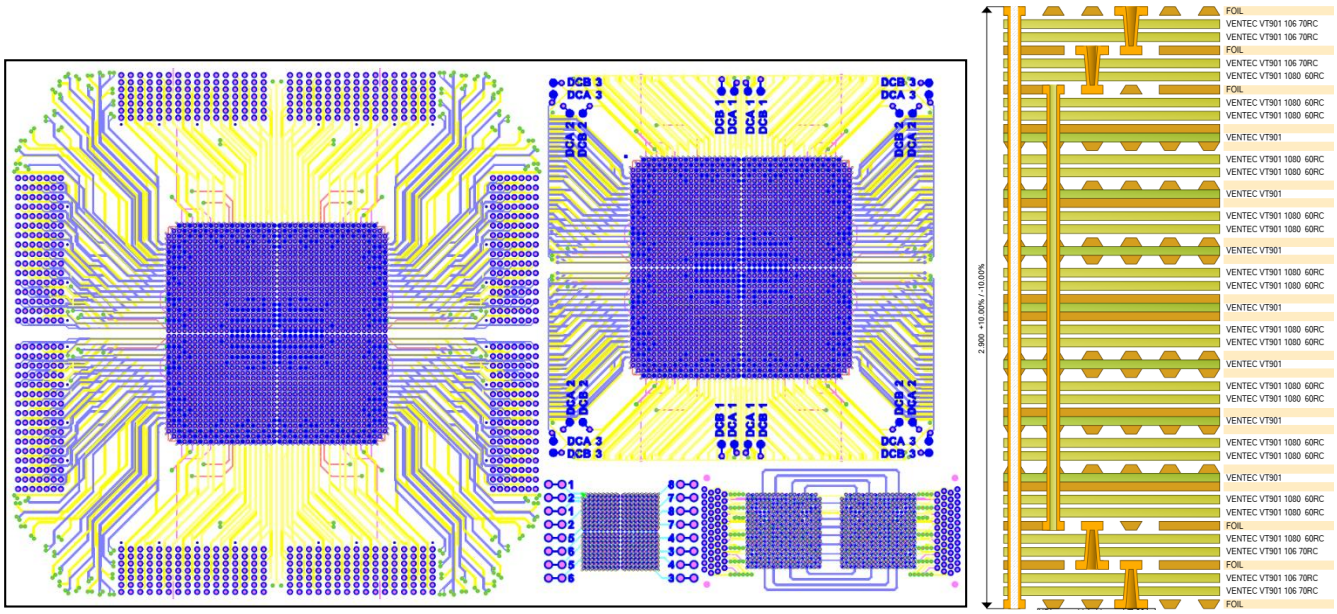


Figure 2 - BGA coupon with real and daisy-chain component fanout for 1.0 mm and 0.8 mm pitch component *(left)* **and build-up of the qualification test vehicle** *(right)*

To assess the CAF performance of a given HDI PCB technology, an HDI CAF test vehicle is required that resembles the final product as much as possible (build-up, via configuration, routing…). The HDI component fanout is represented by including buried vias with a pitch of 0.8 mm and 1.0 mm and microvias with a pitch of 0.5 mm. The highest CAF risk for through-going vias on HDI PCBs are the high-density connectors with a pitch of 1.27 mm. The minimum distance between a via and a ground plane for buried vias and through-going vias is defined by the design rules for minimum conductor spacing (75 µm for basic HDI and 50 µm for complex HDI). The drill diameter for buried vias (0.3 mm) and through-going vias (0.5 mm) is copied from the qualification test vehicle design for the basic HDI technology.

Microvias are considered less prone to CAF due to the use of laser drilling instead of mechanical drilling and their smaller diameter results in a smaller contact area with the glass fibers. Nevertheless, the wall-to-wall spacing of a microvia with 125 µm drill diameter at 0.5 mm pitch is only 375 µm. This is far below the wall-to-wall spacing seen for buried vias or PTHs. To assess this risk, a dedicated microvia test structure is added to the HDI CAF test vehicle. Due to the independent drilling processes, stacked microvias are not considered a higher risk for CAF compared to staggered microvias.

Six types of via-to-via test structures are included in the HDI CAF test vehicle: 0.3 mm drill buried vias with 0.8 mm pitch in a straight and a staggered alignment[1], 0.3 mm drill buried vias with 1.0 mm pitch straight and staggered, 0.5 mm drill through-going via with 1.27 mm pitch straight and the microvias with 0.5 mm pitch straight. A number of these test structures are duplicated to cover both the warp and weft fiber direction.

Although via-to-via filament growth is regarded as the dominant form of CAF, via-to-plane test structures remain relevant for HDI. Four via-to-plane test structures are designed with buried vias or PTHs. The diameter of the antipad is the sum of the pad diameter and two times the minimum as-designed spacing for basic HDI (75 µm) or complex HDI (50 µm). In the case of the buried vias (0.6 mm pad diameter), the antipad diameters will be 0.75 mm and 0.7 mm. For the PTHs (0.8 mm pad diameter), this becomes 0.95 mm and 0.9 mm. The test structures consist of 17x17 vias with all internal non-functional pads removed to ensure the failure mechanism is from hole wall to conductor.

A single design is used to cover both the basic HDI and the complex HDI technology. To mimic the presence of an additional microvia layer, a dummy lamination is performed before the PTH drilling. This covers the risk of material embrittlement as a result of multiple laminations, affecting the quality of the drilled holes.

[1] *Straight* alignment refers to vias which are directly adjacent, while the *staggered* alignment offsets the second via with half of the pitch. The term staggered can create confusion with the microvia configuration. IPC-9691B uses the terms *in-line* and *diagonal*, respectively.

The layout of the HDI CAF TV is shown in Figure 1. The distance between connected vias of a given test structure is varied to avoid possible alignment with the glass fiber bundles, resulting in worst-case (or best-case) performance. For the same reason, additional spacing between groups of vias in staggered test structures is foreseen.

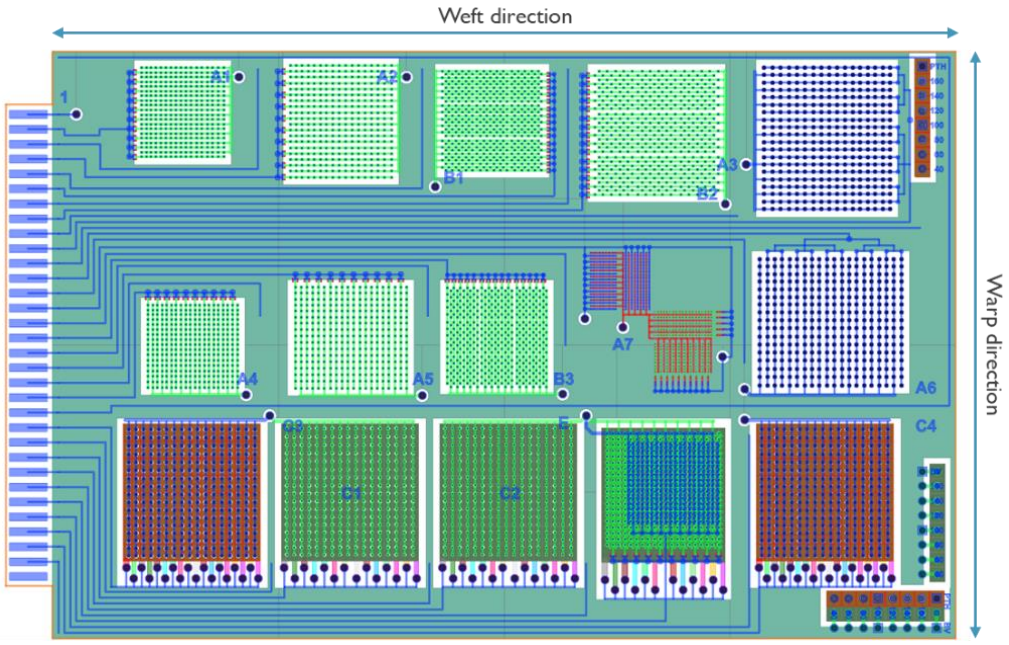


Figure 3 - Design and build-up of the HDI CAF test vehicle

Test Methods

The qualification test vehicle is subjected to the qualification test flow for HDI technology as defined in ECSS-Q-ST-70-60C. Group 1 (visual inspection and non-destructive test) consists of visual inspection, dimensional verification, impedance test, cleanliness and electrical testing. Peel testing is performed in group 2 (miscellaneous testing) and group 3 (thermal stress) covers microsectioning before and after solder bath float and rework simulation, and IST. Group 4 (assembly and life test) combines reflow simulation, rework simulation and thermal cycling. ECM testing is part of group 5. A selection of test methods is described in more details below.

Within the ECSS-Q-ST-70-60C standard, IST is an important test method to evaluate the quality of a via (PTH, blind, buried and microvia). The test method is applied for process monitoring, procurement and qualification. IST is a form of current-induced thermal cycling and is described in IPC-TM-650-2.6.26 (Method A). The coupon is heated using a power circuit and the resistance of the structures under test is monitored continuously via the sense circuit(s) of the coupon. The coupon design should represent the PCB technology of highest complexity and cover all aspects of a given design or technology that are expected to affect thermal endurance.

Before cycling, the coupons are subjected to six times preconditioning to 230 °C using a “superheat” circuit. This meandering circuit on the outer layers of the coupon is used to mimic the assembly process. The temperature of 230 °C is chosen to represent SnPb assembly and the six preconditioning cycles should cover the worst-case number of assembly, repair and rework operations. Blind, buried and through-going vias are cycled from room temperature to 150 °C (epoxy-based materials) or 170 °C (polyimide) in a 3-minute heating and 2-minute cooling cycle. The testing is stopped as soon as one of the sensing circuits reaches a 5 % increase in resistance at high temperature compared to the first cycle. Based on an acceleration study, it was determined that an IST endurance of ≥ 400 cycles should be reached for blind, buried and through-going vias.

Microvia testing using IST follows a different approach. As microvias experience lower stress levels during cycling, the test temperature needs to be increased to apply sufficient stress to the microvia. For epoxy-based materials, a test temperature of 190 °C is used, while for polyimide testing is performed to 210 °C. This stress level is no longer related to the mission profile, but applied to determine if the manufacturing quality of the microvia is adequate. Until recently, it was believed that the microvia would fail either early (less than 100 cycles) or not at all. An IST endurance of ≥ 100 cycles was specified with a maximum increase in resistance of 4 %. After encountering failures on microvias that successfully passed the 100 cycles and observing wear-out type failure mechanisms in microvias after a few hundred cycles, it was decided to increase the threshold to 400 cycles, in line with the standard vias. This is furthermore motivated by the microvia reliability concerns described in IPC-WP-023 [10].

An additional caveat with IST of microvias is that the standard power circuit cannot be used to heat the coupon. The (buried) vias within the power circuit would obviously fail before the microvias. For microvia testing, the coupon can be heated using the superheat circuit or the power can be connected directly to a sense circuit containing the microvias. The drawback of the latter is that only one circuit can be tested at a time, but the temperature of the microvia can be better controlled. ECSS-Q-ST-70-60C specifies power-on-sense as the preferred method, based on the recommendation from PWB Interconnect Solutions Inc. (Ottawa, Canada).

The reference test method for evaluating thermal reliability remains thermal cycling. This is performed in a single chamber system at ambient pressure. The test samples are subjected to reflow simulation (two times vapor phase reflow at 215 °C) and rework simulation (ten times manual soldering) after baking for 8 hours at 120 °C. Following the reflow and rework simulation, the coupons are submitted to 500 cycles from -55 °C to +100 °C (10°/min and 15 min dwell time). As this is commonly applied for project qualification, a shorter test consisting of 200 cycles from -60 °C to +140 °C is also applied. Electrical monitoring of daisy chains can be performed during testing in addition to the required evaluation method of microsectioning afterwards.

ECSS-Q-ST-70-60C specifies the following protocol for CAF testing.

- Ambient phase using the parameters: 24h, 25°C, 50% RH, 0V;
- Preconditioning phase using the parameters: 96h, 85°C, 75% RH, 0V;
- CAF phase using the parameters: 500h, 85°C, 75% RH, 50V;
- Ambient phase using the parameters: 24h, 25°C, 50% RH, 0V.

The overall approach is in line with IPC-TM-650 2.6.25B, with two noticeable exceptions. The test voltage of 50 V is chosen to follow the guideline of two times the maximum voltage for HDI technology (in fact, the maximum voltage is 30 V, but 50 V is deemed a more standardized test voltage). The test applies a relative humidity of 75% RH which is less than the 85% RH specified in 2.6.25B. But this still provides some margin and acceleration of test compared to the maximum relative humidity of 65 % in clean rooms for ground testing and assembly. Sample preparation before testing consists of electrical registration measurement and baking, followed by six times vapor phase reflow at 215 °C, ultrasonic cleaning and again baking for 8 hours at 120 °C.

Test Results

Table 2. Summary of test results

Group	Sample	Test	Result
Group1	All coupons from three panels	Visual inspection	OK
	All coupons from three panels	Dimensional verification	OK
	All coupons from three panels	Impedance test	OK
	All coupons from three panels	Cleanliness	OK
	All coupons from three panels	High resistance electrical test	OK
	All coupons from three panels	Continuity test	OK
Group 2	One coupon	Peel test	OK
Group 3	Three coupons from three panels	Microsectioning – as received	OK
	Three coupons from three panels	Microsectioning – after thermal stress	OK
	Three coupons from nine panels	IST	NOK
Group 4	Two PCBs from two panels	Insulation resistance – initial	OK
	Two PCBs from two panels	Dielectric withstanding voltage – initial	OK
	Two PCBs from two panels	Insulation resistance – after thermal cycling	OK
	Two PCBs from two panels	Dielectric withstanding voltage – after thermal cycling	OK
	Two PCBs from two panels	Peel test – after thermal cycling	OK
	Two PCBs from two panels	Microsectioning – after thermal cycling	OK
Group 5	Four samples	THB testing	OK
	Ten samples	CAF testing	NOK
Group 6	One PCB from one panel	Microsectioning – after thermal cycling	OK

Three panels were selected from the QTV manufacturing batch and subjected to the tests described above. Each panel contains three IST coupons (one TVX and two SLX coupons), two BGA coupons and two times the dedicated test structures for HDI qualification test flow (coupons A/B, Bn, E, H and P). For CAF testing, 10 samples of the HDI CAF test vehicle were manufactured. All manufacturing was performed by ACB (Dendermonde, Belgium).

Nine coupons from three different panels are subjected to IST. Plated through holes and through-going vias are evaluated on coupons TVX3A, 6A and 9A. Buried vias are tested on coupons SLX3A, 6A and 9A and coupons SLX3B, 6B and 9B are used for microvia evaluation. Prior to testing the microvias, the buried vias on coupons SLX3B, 6B and 9B are subjected to 500 cycles to 170 °C (with preconditioning) to reflect the test conditions for procurement.

The IST results are shown in Table 3 to Table 6. The through-going vias on the TVX coupon reach between 596 and 741 cycles. This is well above the requirement of 400 cycles, although a 500 µm via in a 2.8 mm thick polyimide board could be expected to sustain longer testing. The pitch ("grid") of the vias in the test coupon was 1.27 mm to represent the high-density connector layout, which could explain the lower number of cycles that is reached compared to previous testing at a larger grid.

The SLX coupons contain three sense circuits. Sense 1 (buried vias only) and sense 2 (buried vias and microvias) were monitored during testing of the buried vias. Testing is stopped when both sense circuits have reached the acceptance criteria of 5 % resistance increase. Sense 3 (microvias only) is used for microvia testing (power-on-sense). The buried vias have an aspect ratio close to eight (300 µm drill diameter in a 2.4 mm thick core). The number of cycles reached are between 449 and 560, which is above the requirement and in line with expectations. Pre-cycling for the buried vias on the microvia test coupons (SLX3B, 6B and 9B) shows a similar result of 407 to >500 cycles. The required endurance is reached on all coupons, although the margin on coupon SLX3B is slim.

Two out of the three coupons for microvia testing reach the required 400 cycles. Testing of these coupons was stopped after 500 cycles to 210 °C. Coupon SLX3B failed after 285 cycles and does not reach the required endurance. As the failure could not be located using thermal imaging, failure analysis is performed by microsectioning the entire coupon row by row. Optical inspection revealed cracks near the target pad of microvia 1-2 (Figure 4). These cracks are observed on two microvias in the central zone of the coupon. The other microvia levels in this zone did not show any cracks. In other areas of the coupon, no cracks were detected on any of the microvia levels. Microvia 1-2 in the SLX coupon is located partially above the buried via (0.8 mm pitch fanout configuration). The thermal expansion as a result of the temperature excursions create stress at the base of the microvia. This effect is aggravated by the presence of the resin-filled buried via below. If the microvias in coupon SLX3B is slightly misaligned and thus overlaps more with the buried via compared to the other panels, this could explain the early failure.

Table 3 - Results for through vias tested at 170 °C after six times preconditioning to 230 °C

Coupon	Pwr Cycles	Pwr %	S1 Cycle	S1 %	Result
TVX3A	n.a.	2.0	596	5	PASS
TVX6A	n.a.	1.8	626	5	PASS
TVX9A	n.a.	1.5	741	5	PASS

Table 4 - Results for buried vias tested at 170 °C after six times preconditioning to 230 °C

Coupon	Pwr Cycles	Pwr %	S1 Cycle	S1 %	S2 Cycle	S2 %	Result
SLX3A	n.a.	1.6	493	5	528	5	PASS
SLX6A	n.a.	2.6	449	5	450	5	PASS
SLX9A	n.a.	2.1	559	5	560	5	PASS

Table 5 - Results for pre-cycling of buried vias after six times preconditioning to 230 °C

Coupon	Pwr Cycles	Pwr %	S1 Cycle	S1 %	S2 Cycle	S2 %	Result
SLX3B	n.a.	2.6	407	5	407	5	PASS
SLX6B	500	0.8	500	3.6	500	3.5	PASS
SLX9B	500	1.2	500	4.8	481	5	PASS

Table 6 - Results for microvias tested at 210 °C after six times preconditioning to 230 °C and 500 cycles at 170 °C

Coupon	Pwr S3 Cycles	Pwr S3 %	Sense H Cycle	Sense H %	Result
SLX3B	285	4	n.a.	3.1	FAIL
SLX6B	500	2.3	500	1.3	PASS
SLX9B	500	3.0	500	2.4	PASS

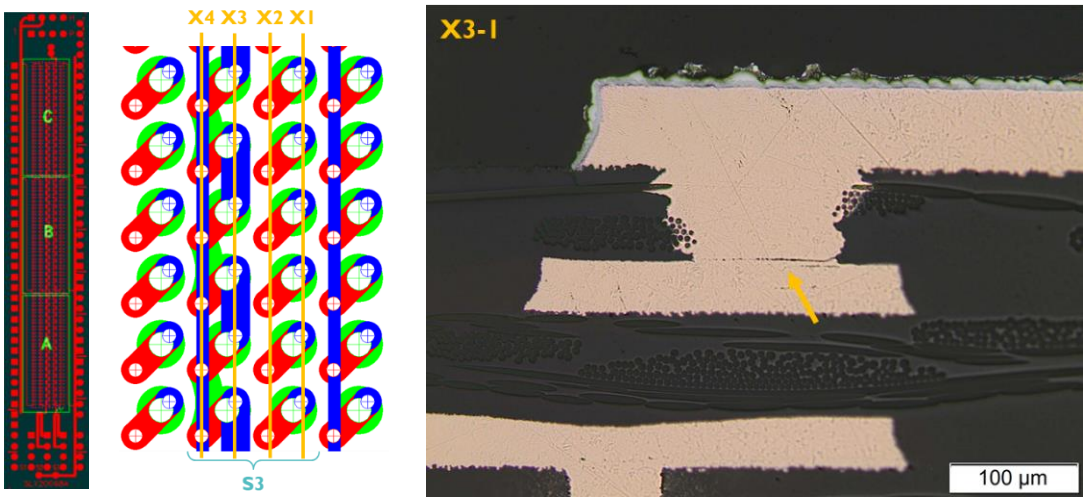
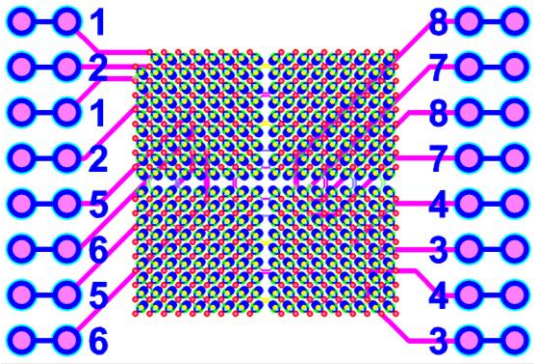


Figure 4 - Crack found at the base of the microvia after microsectioing of coupon SLX3B

Three BGA coupons are submitted to the assembly and life test flow. The test samples are subjected to reflow simulation (two times vapor phase reflow at 215 °C). In addition, rework simulation (ten times manual soldering) is performed on plated through holes of the high-density connectors on the BGA coupon (two times four PTHs). All coupons were baked for 8 hours at 120 °C before reflow and rework simulation. BGA6A and 9B are subjected to 500 cycles from -55 °C to +100 °C, while BGA6B is subjected to 200 cycles from -60 °C to +140 °C. Thermocouples are attached to all BGA coupons to monitor the board temperature during testing. The interconnection resistance of the daisy chains in the 0.8 mm pitch fanout is monitored during testing (four-point resistance measurement every 5 seconds using Keithley 3706A Systems Switch/Multimeter). The final evaluation is performed by microsectioning.

Figure 5 shows the details of the daisy chains in the 0.8 mm pitch fanout used for electrical monitoring. DC1 connects all the vias in the outer row of the component fanout, DC2 connects all the vias in the second row, and so on. Only the buried vias are included in the daisy chains and the number of buried vias per chain is indicated in the table on the right.



Chain	# vias	Chain	# vias
DC1	68	DC5	36
DC2	60	DC6	28
DC3	52	DC7	18
DC4	44	DC8	24

Figure 5 - Layout and number of vias of the daisy chains in the 0.8 mm pitch fanout

Electrical monitoring during thermal cycling (**Error! Not a valid bookmark self-reference.** and Table 8) showed only a minimal increase in resistance for both temperature ranges. This confirms the positive IST results for the buried vias. Microsectioning did not reveal any cracks initiating in the barrel of the buried via nor any anomalies in the microvias.

Table 7 - Results of the electrical monitoring during thermal cycling (500 cycles from -55 °C to +100 °C)

Board	Chain	R (Ω) at room temperature	R (Ω) at high T first cycle	R (Ω) at high T last cycle	Resistance increase (%)
BGA6A	DC1	0,801	1,045	1,058	1,2%
BGA6A	DC2	0,725	0,946	0,958	1,3%
BGA6A	DC3	0,616	0,803	0,813	1,3%
BGA6A	DC4	0,546	0,712	0,721	1,3%
BGA6A	DC5	0,429	0,559	0,567	1,5%
BGA6A	DC6	0,372	0,484	0,491	1,5%
BGA6A	DC7	0,278	0,361	0,368	1,8%
BGA6A	DC8	0,263	0,341	0,347	1,8%
BGA9B	DC1	0,824	1,056	1,086	2,8%
BGA9B	DC2	0,744	0,953	0,980	2,8%
BGA9B	DC3	0,635	0,814	0,836	2,8%
BGA9B	DC4	0,564	0,722	0,742	2,8%
BGA9B	DC5	0,445	0,570	0,586	2,8%
BGA9B	DC6	0,383	0,490	0,504	2,8%
BGA9B	DC7	0,273	0,350	0,360	2,8%
BGA9B	DC8	0,255	0,326	0,335	2,9%

Table 8 - Results of the electrical monitoring during thermal cycling (200 cycles from -60 °C to +140 °C)

Board	Chain	R (Ω) at room temperature	R (Ω) at high T first cycle	R (Ω) at high T last cycle	Resistance increase (%)
BGA6B	DC1	0,817	1,190	1,200	0,84%
BGA6B	DC2	0,740	1,078	1,087	0,85%
BGA6B	DC3	0,632	0,920	0,928	0,88%
BGA6B	DC4	0,559	0,814	0,821	0,87%
BGA6B	DC5	0,441	0,641	0,647	0,91%
BGA6B	DC6	0,385	0,560	0,565	0,87%
BGA6B	DC7	0,295	0,429	0,433	0,97%
BGA6B	DC8	0,276	0,402	0,405	0,94%

The CAF testing is performed on 10 samples in a CTS CS-40/200 climate chamber using a Gen3 Systems Auto-SIR 256 with a 256-channel test rack. Sample preparation started with measurement of the registration on the electrical test structures included on the test vehicle. A maximum misregistration of ≤ 60 µm was measured for the PTHs on three samples. For all other samples as well as for all the buried vias on all samples, the misregistration was below the lowest detectable level of 40 µm. Subsequently, the samples were submitted to reflow simulation (six times reflow at 215 °C). After reflow simulation, the samples were visually inspected and cleaned using isopropyl alcohol (IPA). Finally, the samples are placed in the oven for baking (8 hours at 120 °C).

The samples were mounted in the test rack and kept in the chamber for 24 hours before raising the temperature (85 °C) and the humidity (75 % RH). The first measurement is performed just before the temperature is increased. During the preconditioning phase (85 °C and 75 % RH without bias), measurements are taken every 24 hours. After 96 hours of soaking, the actual CAF phase starts and a bias voltage of 50 V is applied to the samples. Measurements are now taken from all samples every 15 minutes. The test continues for 500 hours, after which the bias is switched off and the measurement programs stops. The temperature and humidity are reduced to 25 °C and 50 % RH. The samples are kept inside the chamber for an additional 24 hours, when the final measurement is performed.

A detailed overview of the HDI CAF test results and associated failure analysis will be published elsewhere. As an example, Figure 6 shows the results for buried vias in a straight configuration with a pitch of 0.8 mm and 1.0 mm for both the warp and weft direction of the glass fibers. Figure 7 shows the results for the microvia test structure.

The failure criteria is a drop in resistance of more than one decade compared to the baseline resistance after 96 hours of soaking. No failures are observed between microvias at 0.5 mm pitch, buried vias at 1.0 mm pitch or PTHs at 1.27 mm pitch. Some failures occur between buried vias at 0.8 mm pitch. Most failures are detected in the via-to-plane test structures, especially for the PTHs. There is no significant difference between the antipad diameter for basic and complex HDI (75 µm vs 50 µm spacing). The exact nature of these failures is not yet known at the time of writing of this paper and failure analysis is ongoing.

A dedicated test vehicle was designed to match the requirements of the HDI technology parameters. The design of this HDI CAF TV differs significantly from the more widely used IPC test coupons and derivations. The layer count is twice as high (20 layers versus 10 layers typically), doubling the number of opportunities for CAF, affecting drill quality and introducing a higher risk for contamination with foreign material. The use of sequential lamination (risk of embrittlement) and internal plated layers (thick copper) makes achieving a good drill quality more challenging and as such, better represents the actual board.

The rationale behind this test vehicle and, by extension, the CAF test methodology can be debated. CAF testing can be performed at different levels: material evaluation, qualification of a given design and material at a selected manufacturer or as a batch release for each procurement. While material screening, at possibly elevated stress levels, is relevant for material development and comparison, it is insufficient since it does not take into account the manufacturing. Some experts are of the opinion that CAF is batch related and should therefore be done as part of the release procedure during outgoing test. In the ECSS working group, CAF testing as part of a qualification test flow was deemed an adequate compromise. The possible variations in manufacturing can be considered covered by the use of qualified manufacturers having a PID (process identification document). The CAF risk of a given design needs to be reviewed case by case to ensure that the qualification testing covers (i.e. is representative of worst-case or highest technological capability) for the procured PCB design.

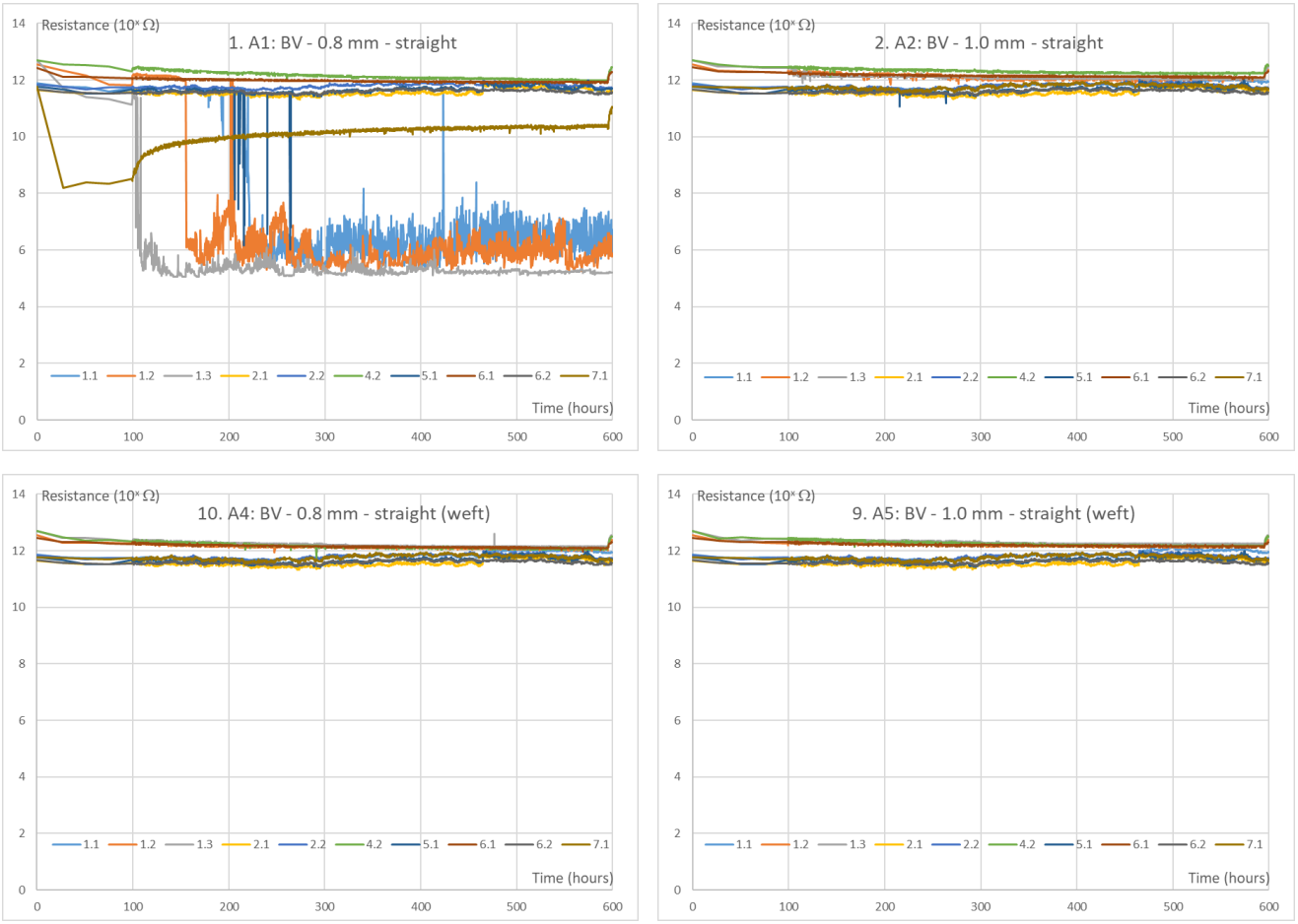


Figure 6 – CAF test results for buried vias in a straight configuration with a pitch of 0.8 mm *(left)* **and 1.0 mm** *(right)* **for both the warp** *(upper row)* **and weft direction** *(bottom row)* **of the glass fibers**

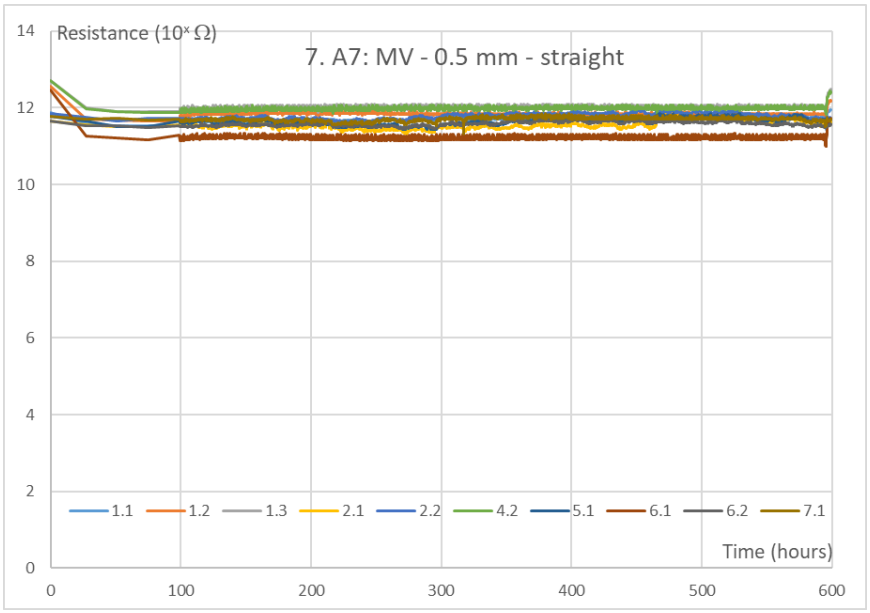


Figure 7 – CAF test results for microvias in a straight configuration with a pitch of 0.5 mm

Conclusion

During the stakeholder workshop, the relevant AADs for space applications were identified. Based on the mechanical and functional requirements of these components, the technology parameters and associated design rules were determined. Two categories of HDI technology are considered: two levels of staggered microvias (basic HDI) and (up to) three levels of stacked microvias (complex HDI).

This paper presents the main results of the qualification test flow for the basic HDI technology. The through-going vias and buried vias reach the required IST endurance of 400 cycles. The microvia configuration for the 0.8 m pitch fanout might be the cause of the early failure in IST. Electrical monitoring during thermal cycling showed only a minimal increase in resistance for both temperature ranges. Microsectioning after cycling did not reveal any cracks initiating in the barrel of the buried via nor any anomalies in the microvias. For the CAF testing, no failures are observed between microvias at 0.5 mm pitch, buried vias at 1.0 mm pitch or PTHs at 1.27 mm pitch. Some failures occur between buried vias at 0.8 mm pitch. Most failures are detected in the via-to-plane test structures, especially for the PTHs. All other tests in the qualification test flow were passed successfully.

The qualification of the basic HDI technology is only the first step in this extensive study on HDI technology for space applications. An extensive reliability assessment is underway. Various test methods for microvias will be evaluated in order to arrive at a test flow that can assure an adequate confidence level for both procurement and qualification.

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