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The construction of a high-voltage (up to 1000 V) bipolar metal-oxide-semiconductor field-effect transistor square-wave generator is described. This generator is capable of producing both positive and negative going square waves with variable amplitude, repetition rate, and width. The circuit was designed for ferroelectrics research, however other applications are possible. The rise time of the prototype was 200 ns which was quite satisfactory for the present ferroelectric research project however the rise time can be decreased to 50 ns if necessary. The reader with a modest knowledge of electronics should be able to construct the circuit. Possible pitfalls and critical points are discussed.

I. INTRODUCTION

A high-voltage (up to 1000 V) bipolar solid-state square-wave generator will be described. Aside from the simple solid-state design the most unique feature of this generator is its ability to produce both positive and negative polarities. The rise time of the prototype circuit was 200 ns. If necessary, the rise time could approach 50 ns. The period of the bipolar pulse pair is variable as is the time between positive and negative pulses. The amplitude is also variable. The generator was designed for ferroelectrics research, however other applications are possible. If bipolar pulses are not required simpler designs are available. A monopolar solid-state circuit is described by Bernius and Chutjian.[1,2] Commercial manufacturers include Cober[3] (a tube design), and Directed Energy (solid-state design).[4] In some cases it may be possible to build a bipolar generator using two monopolar generators.

The circuit is described from the standpoint of an experimental physicist, not from the standpoint of an electrical engineer. The reader, with a modest knowledge of electronics at the level of Horowitz and Hill,[5] should be able to construct the circuit. Possible pitfalls and critical points are discussed.

II. BACKGROUND

Typically ferroelectrics are studied by applying a series of square waves to a ferroelectric capacitor and monitoring the current as a function of time in a series resistor. This current is known as the switching current and was first reported by Mertz.[6] The square-wave generator used in such studies should have the following characteristics:

(i) high voltage: This depends on the coercive field of the ferroelectric and the thickness of the sample.

(ii) low output impedance: a high output impedance will contribute to the "width" of the RC peak which should be kept to a minimum so as not to mask the switching current.

(iii) fast rise time: obviously we desire a pulse which reaches its full value well before the switching current peak.

Another important characteristic is flexibility, that is, the ability to choose, repetition rate, amplitude, and time between polarities.

Three circuit designs which could accomplish the aforementioned objectives immediately present themselves: high-voltage tubes, mercury-wetted relays, and high-voltage metal-oxide semiconductor field-effect transistors (MOSFETs). High-voltage tubes are becoming less commonplace for a number of reasons including high power consumption, relatively high cost, and reliability. Mercury-wetted relays have been employed by some investigators.[7,8] These relays were typically driven at line voltage frequencies, 50 or 60 Hz. In cases where switching at these frequencies can damage the crystal, a logic circuit could be used to drive the relays.[9,10] These relays offer the advantage of extremely fast rise times, on the order of a nanosecond, depending on the attention to construction.[11] Their disadvantages include a finite lifetime and limited voltage, on the order of 100 V. While in typical application these disadvantages can be overcome with arc suppression circuitry, such circuitry is not appropriate for ferroelectric applications, one problem being an increase in the rise time of the applied pulse. High-voltage MOSFETs are relatively new compared to the other two alternatives. At the present 1000-V MOSFETs are the highest available ratings. They offer the simplicity in design and reliability typical of solid-state circuitry. The rise time is approximately 50 ns, depending on factors which will be discussed later.

III. CIRCUIT DESIGN

The circuit will be described beginning at the output and working backwards. Figures 1 and 2 represent a complete circuit except for the high-voltage power supply. It should be pointed out that neither the plus or minus of the

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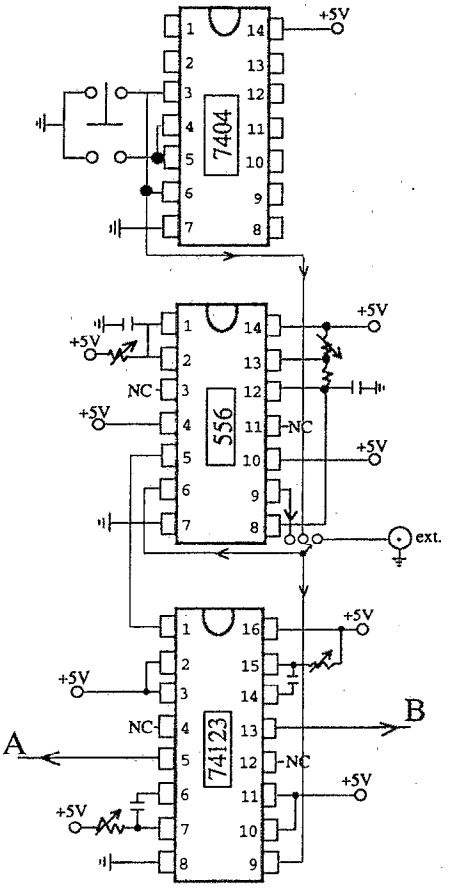

FIG. 1. The logic circuit for producing pulses A and B delayed with respect to each other by an amount D. The circuit can be triggered externally, by single-shot push-button, or by an internal repetitive trigger.

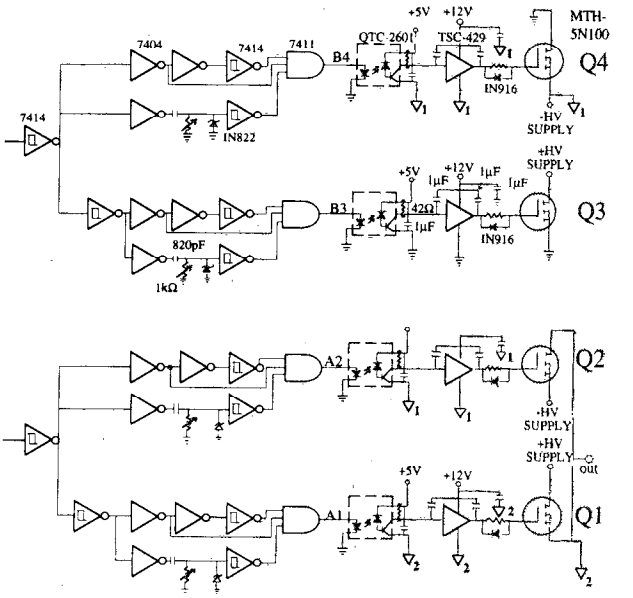

FIG. 2. The complete circuit excluding logic circuit depicted in Fig. 1. The four branches are almost identical. Two branches are inverted with respect to the other two. The commons after the optical isolators are referenced to different points. A brief delay d is provided by the RC combination preceding the third input into the 7411.

high-voltage power supply should be referenced to ground in order to avoid electrical shorts, as revealed by careful examination of Fig. 3.

The heart of the generator is made up of the four high-voltage MOSFETs $Q1$, $Q2$, $Q3$, and $Q4$ shown in Fig. 4. The configuration is somewhat similar to a flying capacitor invertor circuit. This arrangement takes advantage of the diode properties of a MOSFET in the off state. Even if the plus and minus outputs of the high-voltage power supply are isolated from ground, as mentioned above, care must be taken to avoid another short circuit situation resulting from ($Q1$ and $Q3$) or ($Q2$ and $Q4$) being on at the same time. This condition can occur in the case of improper timing, however, it can also occur due to overlap of the finite rise and fall times of the MOSFETs. The short delay (a few hundred nanoseconds) depicted as d in Fig. 5 remedies this problem by producing the intermediate state shown in Fig. 3. This problem is discussed in Bernius and Chutjian's second paper.[2] The different possibilities are represented in Fig. 3 and described by Table I.

The remainder of the circuit is simply the low-voltage drive circuit for turning the MOSFETs on and off in the correct sequence. A timing schematic is given in Fig. 5.

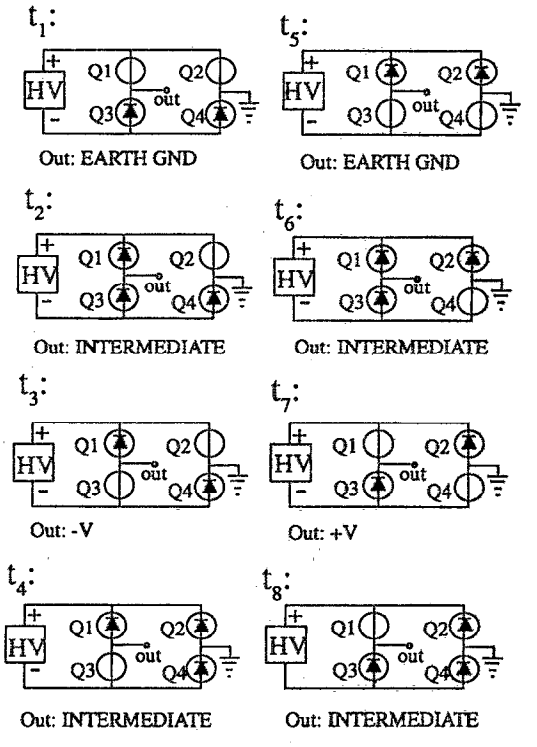

FIG. 3. The time-sequenced states of the four MOSFETs with corresponding outputs. The intermediate state is brief, allowing enough time to prevent a particular MOSFET rise time from overlapping with another MOSFET fall time, therefore shorting out the power supply during this overlap.

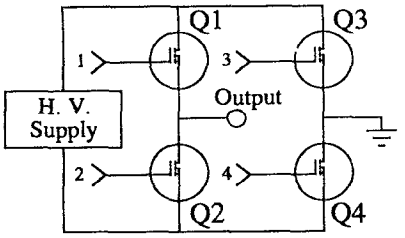

FIG. 4. A schematic showing the four high-voltage MOSFETs which form the heart of the circuit.

The t_1 through t_8 designations are correlated with the different configurationals shown in Fig. 3. The monostable and astable vibrator circuit shown in Fig. 1 produces a pair of pulses, A and B, which are delayed with respect to one another. This long delay D should not be confused with the short delay d. This timing could be accomplished by any number of suitable circuits. The circuit also provides for three methods of triggering the circuit; (a) single-shot push-button, (b) external source, (c) internal repetitive triggering. Any number of references[12] can aid in the selection of proper resistor and capacitor combinations to produce the desired timing.

Pulses A and B are further divided to produce a total of four pulses $A1$, $A2$, $B3$, and $B4$; see Fig. 5. Pulses $A1$ and $A2$ are inverted with respect to each other, as are $B3$ and $B4$. Moreover $A1$ and $A2$ are slightly delayed d with respect to each other, likewise for B. The numbers 1, 2, 3, and 4 correspond to the MOSFETs which are being driven by each pulse. The short delay d is accomplished by the 820-pF capacitor and the 1-$k\Omega$ variable resistor on each of the four branches. As mentioned before, the purpose of this slight delay is to prevent the shorting of the power supply due to the rise time of one MOSFET overlapping with the fall time of the other.

Figure 6 shows a representative rise time. The rise of the circuit is purposely over damped to avoid overshoot.

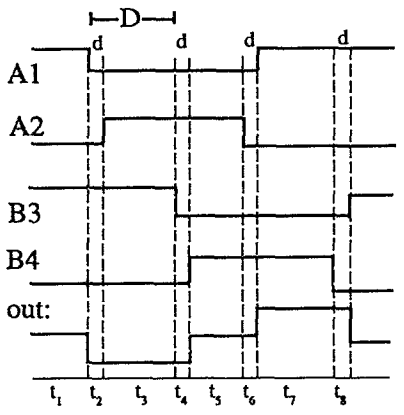

FIG. 5. A timing diagram showing MOSFET drive pulses and the high-voltage output. The various times t_1 through t_8 correspond to the various configurations in Fig. 3 and Table I. The long delay D between $A1$ and $B3$ determines the time the output is at ground. The short delay d is greatly exaggerated and prevents overlapping rise times and fall times in the MOSFETs.

TABLE I. Time sequence of MOSFET states, corresponding to Fig. 3.

Time	Q1	Q2	Q3	Q4	Output
t_1	on	on	off	off	ground
t_2	off	on	off	off	intermediate
t_3	off	on	on	off	neg. high voltage
t_4	off	off	on	off	intermediate
t_5	off	off	on	on	ground
t_6	off	off	off	on	intermediate
t_7	on	off	off	on	pos. high voltage
t_8	on	off	off	off	intermediate

Rise times of approximately 200 ns were quite acceptable in this particular ferroelectric application, while overshoot was not desirable.

IV. KEY POINTS

Note that the sources of all but one of the MOSFETS are not connected to ground. Therefore, the gate drivers are not connected to ground, consequently the optoisolators are used to communicate the drive signal from the low-voltage logic circuit (which is referenced to ground) to the gate divers.

Switching these voltages at these speeds can produce radio frequency noise. In fact, it may be advisable to physically separate the multivibrator circuit from the other circuitry. This also facilitates alternative timing drives such as from a computer, since the four wires carrying the logic level signals can be easily disconnected or reconnected. Good grounds and shielding are also needed.

The speed of the circuit is primarily determined by the rate at which the gate capacitances are charged. Consequentially, the selection of a high current gate driver is important. The TSC-429 by Teledyne Semiconductor was selected because of its high-speed (30 ns) and high-current output (1.5 A). The TCS-4426 is a tougher design and pin

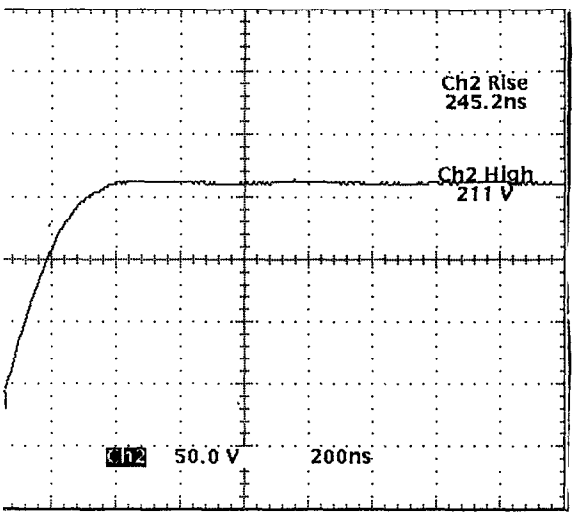

FIG. 6. An oscilloscope trace depicting a typical rise time of the square wave. The leading edge of the 211-V square wave has a rise time of 245.2 ns. The lack of overshoot or ringing is due to intentional overdamping. If ringing or overshoot can be tolerated the rise time could be improved.

compatible with the TSC-429. The driver should be as close, physically, to the MOSFET as possible. In the future some manufactures may incorporate gate drives into MOSFET designs. A fast optoisolator was also selected.

Depending on the nature of the high-voltage power supply it may be advisable to use a capacitor bank close to the MOSFETs to ease peak demands on the power supply as well as reduce ringing in the output.

Note that only one of the MOSFETs has its source connected to ground; in fact, the source of one MOSFET is tied to the output. This makes it necessary for the power supplies for the associated gate drivers and optical isolators to be referenced to output, positive high voltage, negative high voltage, and ground, respectively. Because of this, careful attention has to be paid to insulation characteristics of these power supplies which is not normally the case.

It should be possible to increase the voltage capabilities of the circuit by adding an additional MOSFET in series to each of the four original MOSFETs. This modification was not necessary for the present application. An article by Miro Glogolja and John Kerr should aid in this.[13]

ACKNOWLEDGMENTS

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